國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

應用於超寬頻系統之可調頻低雜訊放大器

Broadband Tunable Low Noise Amplifier for Ultra-Wideband

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中 華 民 國 九十四 年 七 月

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摘要

本篇論文主要是利用標準 0.18μm CMOS 製程設計應用於超寬頻系統前端接收器之可調頻低雜訊放大器。第一顆晶片，設計適用於接收端超寬頻系統之可調頻率放大器被設計與分析，利用柴比雪夫濾波器設計達到寬頻之輸入阻抗匹配，利用電晶體可變電容來調變頻率。量測結果顯示可調變頻率範圍縮小，且操作頻率往低頻移動，可調頻率為 5.1GHz 到 6.8GHz 有最高功率增益(S21) 7.4dB，以及最低雜訊指數 5.7dB，消耗之功率為 19.51mW。依據第一顆晶片量測結果，經過驗證反察，發現可變電容的容值比預期大且可調變範圍比預期小，原因出在模擬的可變電容模組和所佈局的模組不同而產生，因此，第二顆晶片修正可變電容模組，且加上切換 MIM 電容，增加可調頻率範圍；並改用諧振匹配原理達到輸入寬頻阻抗匹配，降低雜訊指數和功率消耗，修正晶片量測結果顯示，可調頻率為 6.3GHz 到 9.4GHz，最高增益 9.3dB，發生在 9.4GHz，平均雜訊指數為 4.5dB，消耗功率為 17.44mW。接著為了達到 3GHz 到 8GHz 之超寬頻可調頻率，考慮可變電容之可調範圍的先天限制，因此，第三顆晶片結合 MEMS 電感的高 Q 特性，設

計切換電感負載，達到更寬頻之調頻設計。比較前兩顆切換 MIM 電容和第三顆切換 MEMS 電感的 LNA 設計，MEMS 高 Q 特性的優勢，明顯使電路達到高增益且超寬可調頻率，及低雜訊，低功率的設計目的。

Broadband Tunable Low Noise Amplifier for Ultra-Wideband System

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ABSTRACT

The objective of this thesis is aimed at design of low noise amplifier (LNA) with tunable output frequency for the ultra-wideband (UWB) receiver system using standard 0.18um CMOS process.

Three LNA circuits have been implemented. In the first chip, a wideband tunable low noise amplifier is analyzed and designed using the Chebyshev filter design to achieve broadband input impedance matching and a MOS varactor provides frequency tuning capability. The measured data show that the tunable frequency range is from 5.1GHz to 6.8GHz, narrower and lower as compared to the designed values. The frequency drift is due to the inconsistency of the varactor models in the circuit simulator and the circuit layout. Therefore, the second chip is designed to revise the tunable mechanism. The measurement data of the second chip shows that the frequency tunable range is 6.3GHz to 9.3GHz.

To extend the tunable frequency range to 3GHz to 8GHz and still maintain the high power gain is limited by the poor quality factor of the large MIM capacitor value.

Therefore, the high Q micromachined inductors are integrated with the third chip to achieve the wideband tunable range and good noise performance. Furthermore, power consumption is reduced by an external capacitor placed across the gate and the source ports of the input transistor.

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陳仰鵑

九十四年 七月

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E
S
A
1896

Chapter 1

Introduction

1.1 Ultra-Wideband Communication System

The ultra-wideband (UWB) system is an emerging high-speed and low-power wireless communication approved by Federal Communication Commission (FCC) in 2002 for commercial applications in the frequency range from 3.1- to 10.6-GHz. The IEEE 802.15.3a task group (also called "TG3a") is developing an UWB standard. Two primary contenders been left after July 2003 meeting are the OFDM-based multiband approach and the dual-band Impulse Radio spread spectrum approach. The multibanded UWB has greater flexibility in coexisting with other international wireless systems and future government regulators, and could avoid transmitting in already occupied bands. The UWB frequency band from 3.1 to 10.6 GHz of the multiband-OFDM access method is divided into several smaller bands. Each of these bands must have a bandwidth greater than 500 MHz to obey the FCC definition of UWB and each band uses frequency hopping to facilitate multiples access [1, 2]. The division of the UWB frequency spectrum into sub-bands is illustrated in Fig. 1.1.The frequency operation for Mode 1 device allocates in 3.1GHz to 5GHz and the one for Mode 2 device allots to 3.1-8GHz.

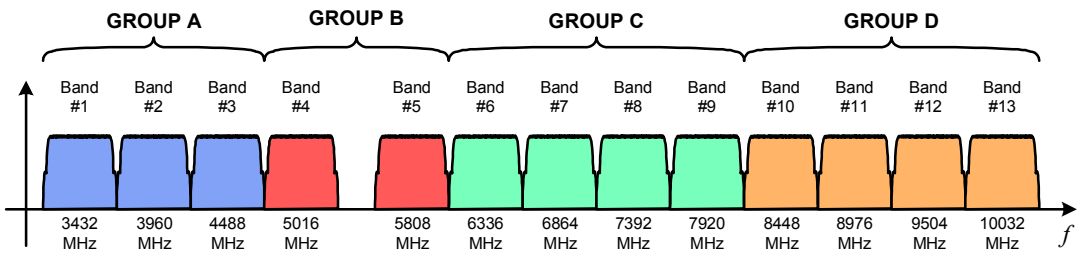


Fig. 1.1 Multiband spectrum allocation.

1.2 Motivation

As introduced in Section 1.1, UWB is becoming more attractive for low cost consumer communication applications and that allows overlying existing narrowband systems to result in a much more efficient use of the available spectrum. Thus, UWB is developed to provide a specification for a low complexity, low cost, low power consumption, and high data rate wireless connectivity among devices within or entering the personal operating space and also addressed the quality of service capabilities required to support multimedia data types.

One of the proposed leading standards for UWB spectrum allocation is a multi-band with frequency hopping. Nevertheless, the robust multipath tolerance needs to combat inter-carrier interference and tight linear constraint. To relax the linearity limitation of the next stage, the low noise amplifier in the receiver path of the UWB frequency hopping system followed with a frequency tunable load is proposed to reject the out of band interference and to increase the dynamic range.

To design a wideband LNA followed by tunable load providing flatness gain over several GHz is a critical challenge for design. In this thesis, we emphasize on the minimum noise figure, gain flatness and ultra-wideband tunable range of the low noise amplifier at low power level.

1.3 Thesis Organization

This thesis discusses about the tunable LNA design and implementation for the UWB frequency hopping system.

In Chapter 2, fundamentals of conventional low noise amplifiers will be introduced. And theoretical MOSFET noise model and noise theory are presented.

In Chapter 3, an ultra-wideband tunable LNA is presented in section 3.2, and in section 3.3 the amended circuit is proposed to enhance the tunable range, and then the tunable LNA integrated with high Q MEMS inductors is discussed in section 3.4.

In Chapter 4, to conclude the tunable LNA design. In Chapter 5, the future work is described. Some issues that should be noted for future works on this topic are also summarize.

Chapter 2

The Fundamentals in LNA Design

Fundamentals of the low noise amplifier will be introduced. In section 2.1 illustrates the noise sources in MOSFET [3, 4]. The design basic of the low noise amplifier is discussed in section 2.2 [3, 4].

2.1 Noise in MOSFET

The noise performance of LNA is the first consideration because it represents a lower limit to the signal amplified by a circuit without significant deterioration in signal quality. The various sources of electronic noise are considered, and MOSFET's noise model will be described here.

The noise process of thermal noise is random, and we would expect a dependence on the absolute temperature, T. It turns out that thermal noise power is exactly proportional to T. The every physical resistor has a noise source associated with thermal noise. The thermal noise can be represented by $\overline{v^2} = 4kTR\Delta f$ or $\overline{i^2} = 4kT(1/R)\Delta f$, where k is Boltzmann's constant and Δf is the noise bandwidth in hertz.

Since MOSFETs are essentially voltage-controlled resistors, they exhibit thermal noise. Thus, detailed theoretical considerations lead to the following expression for the drain current noise of FETs:

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f, \qquad (2\text{-}1)$$

where g_{d0} is the drain-source conductance at zero V_{DS}. The parameter γ has a value of unity at zero V_{DS} and, in long devices, decreases toward a value of 2/3 in saturation.

Note that the drain current noise at zero V_{DS} is precisely that of an ordinary conductance of value g_{d0}. Unfortunately, γ is greater then 2/3 for short channel device, and thus the value will lead to worsen the noise performance as the technology proceeds.

Gate noise, $\overline{i_g^2}$ is another kind of thermal noise due to the thermal agitation of channel charge. The fluctuating channel potential couples capacitively into the gate terminal, leading to a noisy gate current. Although this noise is negligible at low frequencies, it can dominate at radio frequencies. The gate current noise may be expressed as

$$\overline{i_g^2}=4kT\delta g_g\Delta f\,, \tag{2-2}$$

where $g_g=\dfrac{\omega^2 C_{gs}^2}{5g_{d0}}$.

And δ is the coefficient of gate noise, classically equal to 4/3 for long-channel devices while 4 to 6 in short channel one. The gate noise is partially correlated with the drain noise, with a correlation coefficient expressed as

$$c\equiv\frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_d^2}\,\overline{i_g^2}}}\approx -0.395j\,. \tag{2-3}$$

The value of -0.395j is exact for long-channel devices. The correlation can be treated by expressing the gate noise as the sum of two components, the first of which is fully correlated with the drain noise, and the second of which is uncorrelated with the drain noise. Hence, the gate noise is re-expressed as

$$\frac{\overline{i_g^2}}{\Delta f}=4kT\delta g_g(1-|c|^2)+4kT\delta g_g|c|^2\,. \tag{2-4}$$

Because of the correlation, special attention must be paid to the reference polarity of the correlated component.

Charge trapping leads to the flicker noise, which is a type of noise found in all active devices. These traps capture and release carriers in a random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequencies. In electronic devices, 1/f noise (flicker noise) arises from a number of different mechanisms, and is most prominent in devices that are sensitive to surface phenomena. Charge trapping phenomena are usually invoked to explain 1/f noise in transistors. Some types of defects and certain impurities can randomly trap and release charge. The trapping times are distributed in a way that can lead to a 1/f noise spectrum in both MOS and bipolar transistors. Larger MOSFETs exhibit less 1/f noise because their larger gate capacitance smooth the fluctuation in the channel charge. Here, if good 1/f noise performance is to be obtained from MOSFETs, the largest practical device sizes must be used (for a given gm). The mean-square 1/f drain noise current is given by

$$\overline{i_n^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \approx \frac{K}{f} \omega_T^2 \cdot A \cdot \Delta f, \tag{2-5}$$

where A (=WL) is the area of the gate and K is a device-specific constant. Thus, a larger dimension size and a thinner dielectric lead to small 1/f noise.

2.2 Low Noise Amplifiers Basic

To satisfy the targets of LNA design are minimizing the noise figure, providing gain with sufficient linearity and providing a stable 50Ω input impedance matching to terminate an unknown length of transmission line which delivers signal from the antenna to the amplifier. Several kinds of the LNA architectures are illustrated below. The additional constraint of low power consumption and noise performance further complicate the design process.

2.2.1 Low Noise Amplifier Topology and Basic

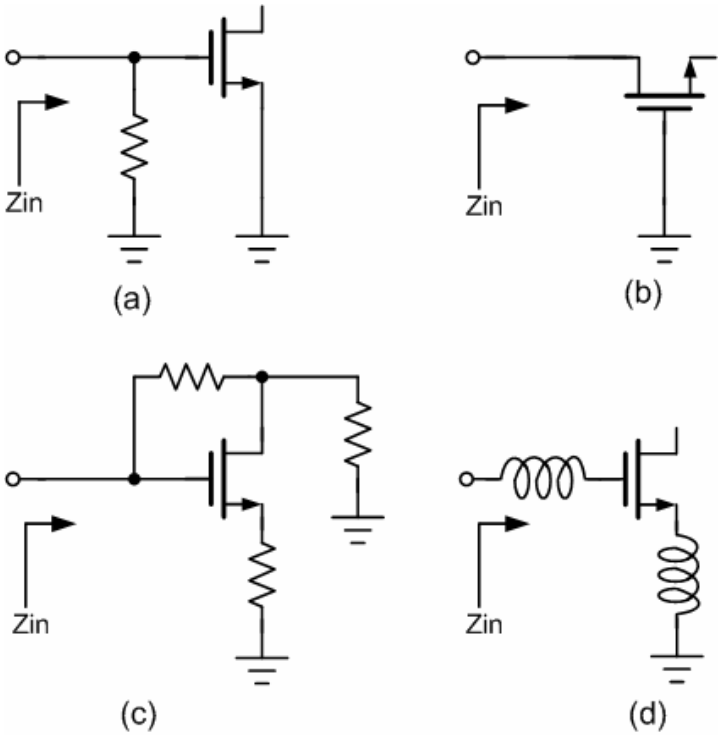


Fig 2.1 Common LNA architectures. (a) Resistive termination (b) 1/g_m termination (c) Shunt - series feedback (d) Inductive degeneration [3].

The four basic topologies of low noise amplifiers for 50 ohm input impedance matching are shown in Fig. 2.1. Fig. 2.1(a) uses 50Ω resistive termination of the input port to provide impedance matching. Unfortunately, the use of real resistors in this fashion has a deleterious effect on the amplifier's noise figure. Fig. 2.1(b) uses a

common gate stage as the input termination. It's also called $1/g_m$ termination architecture. Assuming matched conditions, yields the following lower bounds on noise factor for CMOS amplifiers:

$$F=1+\frac{\gamma}{\alpha}\geq\frac{5}{3}=2.2\text{dB}\text{, where}\,\alpha=\frac{g_m}{g_{d0}}.$$

In CMOS expressions, γ is the coefficient of channel thermal noise, g_m is the device transconductance, and g_{d0} is the zero bias drain conductance. For long channel devices, $\gamma=2/3$, $\alpha=1$. But in short channel MOS devices, γ can be greater than one, and α can be much less than one. Accordingly, the minimum theoretically achievable noise figures tend to be around 3dB or greater in practice.

The third topology is shown in Fig. 2.1(c). This architecture uses resistive shunt and series feedback to set the input and output impedances of the LNA. Amplifiers using shunt-series feedback often have high power dissipation compared to others with similar noise performance. Intuitively, the higher power is partially due to the fact that shunt series amplifiers of this type are naturally broadband, and hence techniques which reduce the power consumption through LC tuning are not applicable.

Fig. 2.1(d) is desirable to have a narrowband RF signal processing, to get rid of out of band blockers. It employs inductive source degeneration to generate a real term in the input impedance. It offers the possibility of achieving the best noise performance of any architecture. That will describe in following sub-section.

2.2.2 *Inductive source degeneration LNA Analysis*

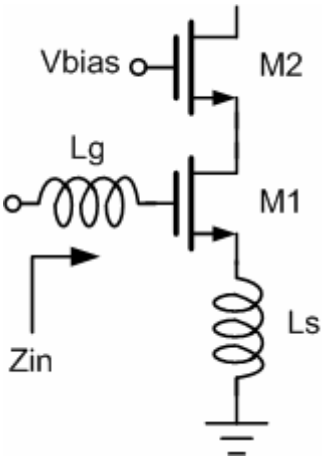


Fig. 2.2 Cascode LNA architecture.

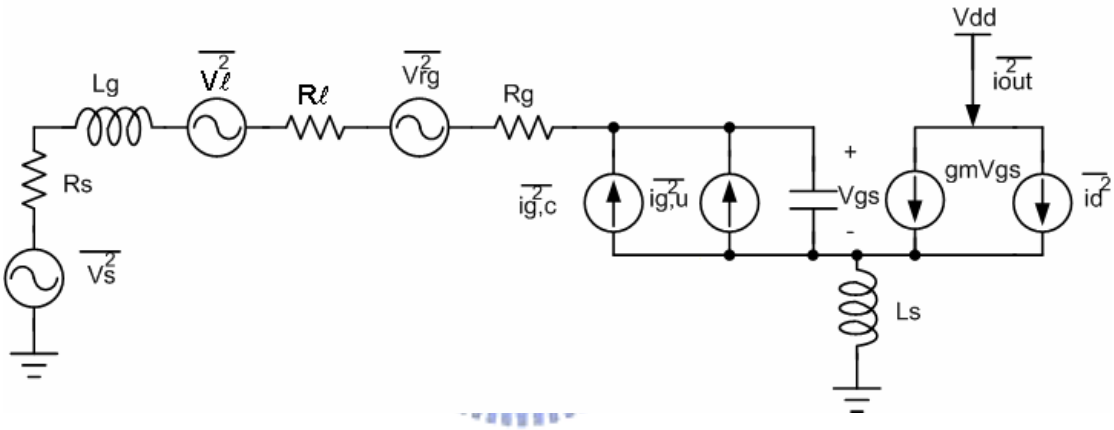


Fig. 2.3 Small-signal model for LNA noise model [3].

The basic cascode LNA architecture is shown in Fig. 2.2. The input impedance is derived as

$$Z_{in}=s(L_s+L_g)+\frac{1}{sC_{gs}}+\left(\frac{g_{m1}}{C_{gs}}\right)L_s=\omega_T L_s \quad \text{(at resonance)} \quad . \qquad (2\text{-}6)$$

The impedance matching achieved by multiplication of cutoff frequency and L_s. The noise model can be derived by analyzing the circuit shown in Fig. 2.3. R_g is the gate resistance of the NMOS device. The channel thermal noise of the device denotes $\overline{i_d^2}$. The portion of the total gate noise with and without correlating the drain noise denote $\overline{i_{g^2,c}}$ and $\overline{i_{g^2,u}}$ respectively. The noise factor is defined as

$$F=\frac{\text{Total\_output\_noise}}{\text{Total\_output\_noise\_due\_to\_the\_source}}. \quad (2\text{-}7)$$

To evaluate the output noise based on driven by a 50Ω source, the transconductance of the input stage is computed first. With the output current proportional to the voltage on C_{gs}, and noting that the input circuit takes the form of a series-resonant network

$$G_m=g_mQ_{in}=\frac{g_m}{\omega_o C_{gs}(R_s+\omega_T L_s)}=\frac{\omega_T}{2\omega_o R_s}. \quad (2\text{-}8)$$

The output noise power density due to source R_s is

$$S_{a,src}(\omega_o)=S_{src}(\omega_o)\cdot G^2_{m,eff}=\frac{4kT\omega_T^2}{\omega_o^2 R_s(1+\frac{\omega_T L_s}{R_s})^2}. \quad (2\text{-}9)$$

The output noise power density due to R_l and R_g can be expressed as

$$S_{a,R_\ell,R_g}(\omega_o)=\frac{4kT(R_\ell+R_g)\omega_T^2}{\omega_o^2 R_s^2(1+\frac{\omega_T L_s}{R_s})^2}. \quad (2\text{-}10)$$

The noise power density associated with the correlating portion of the gate noise to drain noise can be expressed as

$$S_{a,i_d,i_g,c}(\omega_o)=\kappa S_{a,i_d}(\omega_o)=\frac{4kT\gamma\kappa g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2}, \quad (2\text{-}11)$$

where

$$k=\frac{\delta\alpha^2}{5\gamma}|c|^2+\left[1-|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2,$$

$$Q_L=\frac{\omega_o(L_s+L_g)}{R_s}=\frac{1}{\omega_o R_s C_{gs}},$$

$$\alpha=\frac{g_m}{g_{d0}}. \quad (2\text{-}12)$$

The power spectral density of un-correlating gate noise and drain noise is derived as

$$S_{a,ig,u}(\omega_o)=\xi S_{a,id}(\omega_o)=\frac{4kT\gamma\xi g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2}, \tag{2-13}$$

where $\xi=\frac{\delta\alpha^2}{5\gamma}(1-|c|^2)(1+Q^2_L)$.

The noise contribution of the drain noise comes from the first device M_1 proportional to $S_{a,id}(\omega_o)$. Hence, it is convenient to define the contribution of M_1 as

$$S_{a,M1}(\omega_o)=\chi S_{a,id}(\omega_o)=\frac{4kT\gamma\chi g_{d0}}{(1+\frac{\omega_T L_s}{R_s})^2}, \tag{2-14}$$

where

$$\chi=\kappa+\xi=1-2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}}+\frac{\delta\alpha^2}{5\gamma}\left(1+Q_L^2\right). \tag{2-15}$$

Thus the modified noise factor of the device is shown as

$$F=1+\frac{R_\ell}{R_s}+\frac{R_g}{R_s}+\gamma\chi g_{d0}R_s(\frac{\omega_o}{\omega_T})^2, \tag{2-16}$$

by factoring out Q_L

$$g_{d0}Q_L=\frac{g_m}{\alpha}\frac{1}{\omega_o R_s C_{gs}}=\frac{\omega_T}{\alpha\omega_o R_s}, \tag{2-17}$$

the noise factor can be re-expressed as

$$F=1+\frac{R_\ell}{R_s}+\frac{R_g}{R_s}+\frac{\gamma}{\alpha}\frac{\chi}{Q_L}(\frac{\omega_o}{\omega_T}). \tag{2-18}$$

The equations show that χ proportional to Q_L^2. The noise factor is proportional to χ over Q_L. Thus a minimum F exists for a particular Q_L.

Chapter 3

Ultra-Wideband Tunable Low Noise Amplifier

3.1 Introduction

Some diverse topologies of low noise amplifier with output tunable load are proposed in this chapter to relax the linearity limitation of the next stage in receiver front- end and to increase the dynamic range.

Section 3.2 addresses the architecture of 6 to 10 GHz ultra-wideband tunable low noise amplifier. Section 3.3 delineates the detail description of the amended circuit based on measurement results proffered to improve the noise performance and to enhance the tunable range. High quality MEMS inductors are used to promote the noise performance and frequency tunable range over 3 to 8 GHz presented in section 3.4.

3.2 A 6 to 10 GHz UWB Tunable LNA

3.2.1 Ultra-Wideband Tunable LNA Circuit Topology

To design an LNA for the frequency hopping system, it is better to allow only the signal in the specified sub-band to pass through the path rather than signal in the entire band. In doing so, out-of-band and in-band noise is rejected such that the linearity or dynamic range requirement of the following stage can be greatly relaxed. This has been applied to LNA design in [5, 6]. In this section, an LNA is designed to operate over a wide frequency tuning range from 6GHz to 10GHz, which are the sub-bands of group C and group D in the UWB spectrum allocation. The frequency

tuning rang exceeds 4GHz, which is great larger than that of 6% in [5], and that of 35% in [6]. Given the target of frequency tuning range over several GHz, the designed LNA requires wideband input impedance matching network different from the inductive source degeneration used in the conventional narrow-band CMOS LNA [3]. In addition, gain level over the entire band must remain as flat as possible. The schematic of the proposed LNA circuit is as shown in Fig. 3.1, consisting of cascode configuration and a source-follower output buffer. The circuit achieves the wideband input matching by a three-section band-pass Chebyshev filter configuration [7]. The inter-stage inductor, L_b, improves gain flatness among sub-bands. A varactor, C_{var}, provides frequency tuning capability. Technologies to achieve the wideband tuning and gain flatness are discussed narrowly below.

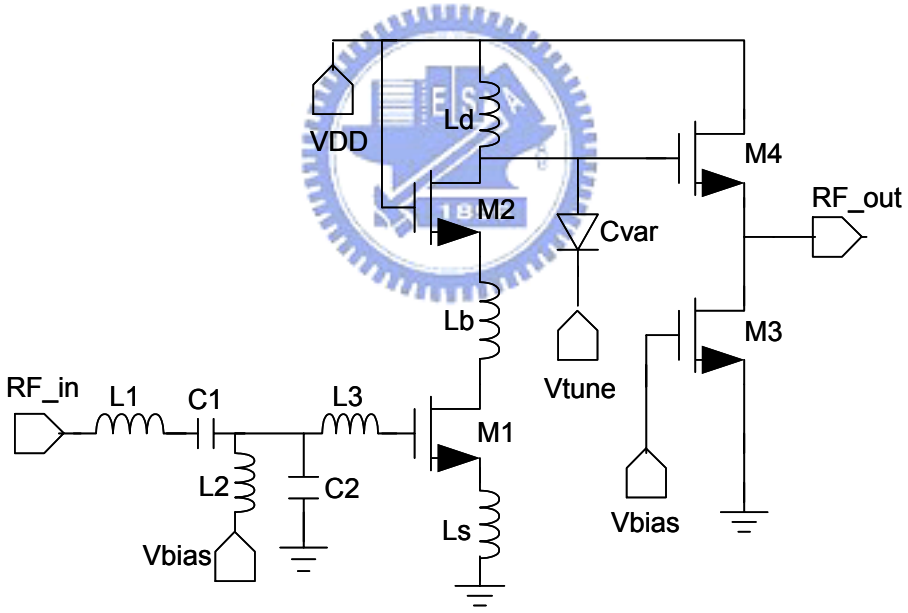


Fig. 3.1 Shematic of the poposed ultra-wideband tunable LNA.

3.2.2 Broadband Matching Techniques

The technique of filter design is employed for broadband input impedance matching. The two kinds of the most common used filter design technique are image

parameter method and insertion loss method. The first one, image parameter method, consists of a cascade of simpler two-port filter sections to provide the desired cutoff frequencies and attenuation characteristics. Thus, although the procedure is relatively simple, the design of filters by image parameter method often must be iterated many times to achieve the desired results and that will result in large chip area. The other one, insertion loss method, uses network synthesis techniques to design filters with a completely specified frequency response. The design is simplified by beginning with low-pass filter prototypes that are normalized in terms of impedance and frequency. Transformations are applied to convert the prototype designs to the desired frequency range and impedance level [8]. The insertion loss method is used to design the broadband input impedance matching for diminishing the implement cost. The Butterworth and Chebyshev filter design are two familiarly practical filter responses by used insertion loss method. The Butterworth design offers a smooth response curve with maximal flatness at zero frequency. The Chebyshev design offers a steeper response curve at the 3 dB cutoff frequency and requires fewer components. In this work, to have precipitous response curve at 3 dB cutoff frequency, the Chebyshev filter design is chosen. The design of a Chebyshev filter will begin at low-pass filter prototypes which are normalized in terms of impedance and frequency; this normalization simplifies the design. The low-pass prototypes are then scaled to the desired frequency and impedance. The design process is illustrated in Fig. 3.2.

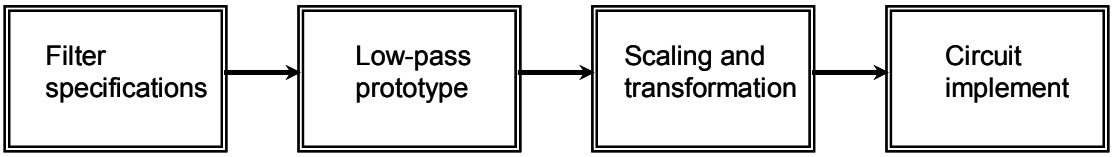


Fig. 3.2 The process of filter design.

In the insertion loss method, a filter response is defined by its insertion loss, or power loss ratio, P_{LR},

$$P_{LR}=\frac{\text{Power available from source}}{\text{Power delivered to load}}=\frac{1}{1-|\Gamma(\omega)|^2}, \tag{3-1}$$

$$|\Gamma(\omega)|^2=\frac{M(\omega^2)}{M(\omega^2)+N(\omega^2)}, \tag{3-2}$$

where M and N are real polynomials in ω^2. Substitute equation (3-2) into (3-1), thus P_{LR} can be re-expressed as

$$P_{LR}=1+\frac{M(\omega^2)}{N(\omega^2)}. \tag{3-3}$$

In this work, the Chebyshev polynomial is used to specify the insertion loss of an N-order low-pass filter as

$$P_{LR}=1+k^2T^2_N(\frac{\omega}{\omega_c}), \tag{3-4}$$

then a sharper cutoff will result. $T_N(x)$ Oscillates between ± 1 for $|x|\le 1$, and k^2 determines the pass-band ripple level. From the power loss ratio equation of Chebyshev filter, the normalized element values of L and C of low pass filter prototype can be figured out. The element definitions of the ladder circuits for low-pass filter prototypes is shown in Fig. 3.3, and the normalize values are listed in Table 3.1.

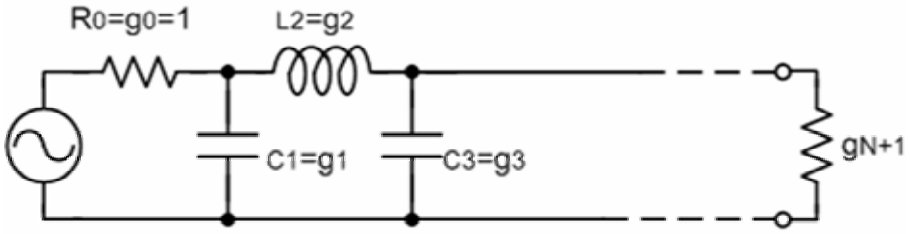


Fig. 3.3 Ladder circuit for low-pass filter prototypes and their element definitions.

Table 3.1 Element values for Chebyshev Low Pass Filter prototypes (g_0=1, ω_c=1, ripple=0.5dB)

N (order)	g_1	g_2	g_3	g_4
1	0.6986	1.0000		
2	1.4029	0.7071	1.9841	
3	1.5963	1.0967	1.5963	1.0000

Low pass filter prototypes design could be transferred to be a band-pass filter response. At the beginning, scale the impedance from unity to the load and source impedance, and also scale the frequency from unity of the low pass prototype to the cutoff frequency of the band-pass one. ω_1 and ω_2 denote the 3-dB cut-off frequency of the band-pass filter. Thus the band-pass response could be obtained as

$$\omega \leftarrow \frac{\omega_0}{\omega_2-\omega_1}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)=\frac{1}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right), \tag{3-5}$$

where $\Delta=\frac{\omega_2-\omega_1}{\omega_0}$. The resonant frequency, ω_0, could be chosen equal to the geometric mean of ω_1 and ω_2, that is $\omega_0=\sqrt{\omega_1\omega_2}$.

The low-pass prototype transfers to the band-pass filter type based on Table 3.1. The low-pass filter elements are converted to series or parallel resonant circuits. The low impedance at resonance, such as a series inductor, L_k, converts to a series LC circuit with element values of Table 3.1,

$$L_k'=\frac{L_k}{\Delta\omega_0}, \tag{3-6}$$

$$C_k'=\frac{\Delta}{\omega_0 L_k}. \tag{3-7}$$

The high impedance at resonance, such as a shunt capacitor, C_k, transfers to a shunt LC circuit with element values of Table 3.1,

$$L_k'=\frac{\Delta}{\omega_0 C_k}, \tag{3-8}$$

$$C_k' = \frac{C_k}{\Delta \omega_0}. \tag{3-9}$$

Both series and parallel resonator have the same resonant frequency of ω_0. Fig. 3.4 shows that condition, where Z_0 means the source impedance. Fig. 3.5 shows the complete transformation circuit of low-pass filter converted to band-pass filter.

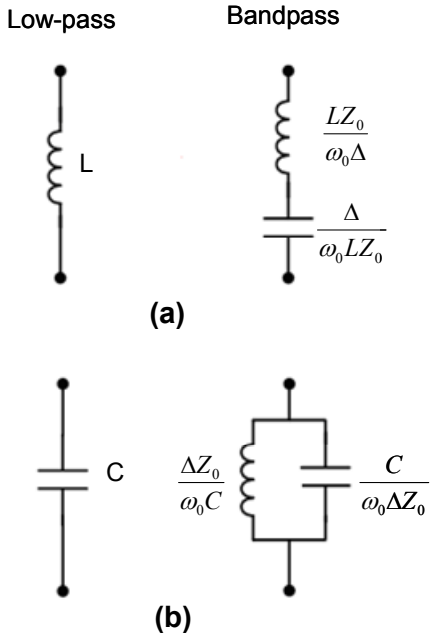


Fig. 3.4 Components convert from low pass filter to band-pass filter.

(a) Series inductor transferred to series LC

(b) Parallel capacitor transferred to shunt LC

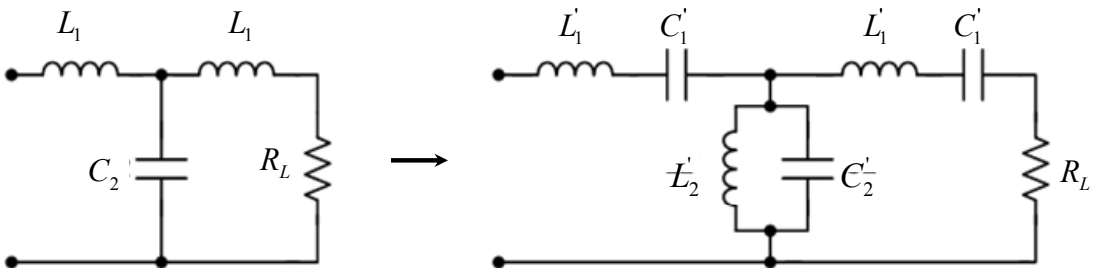


Fig. 3.5 The transformation circuit of low pass filter converted to band-pass filter.

Employ the filter design technique to do the broadband input impedance matching from 6 to 10 GHz. The small signal model of the input matching network is as shown in Fig. 3.6.

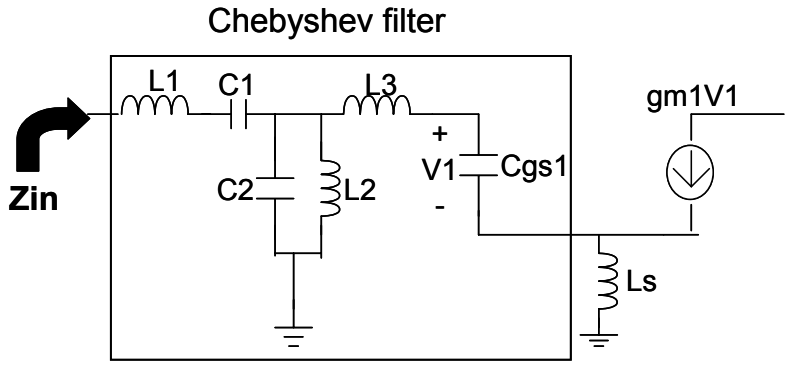


Fig. 3.6. The small signal model of the input impedance.

The filter actually makes use of the parasitic gate-source capacitance C_{gs}. The values of all elements are chosen following the third-order Chebyshev filter design which have discussed above with corner frequencies set to be 6GHz and 10GHz. The input impedance is derived as

$$Z_{in} = Z_1 + \frac{Z_2(Z_3 + \omega_T L_s)}{Z_2 + Z_3 + \omega_T L_s}, \tag{3-10}$$

where

$$Z_1 = sL_1 + \frac{1}{sC_1},\ Z_2 = sL_2 \,//\, \frac{1}{sC_2},$$

$$Z_3 = s(L_3 + L_s) + \frac{1}{sC_{\text{gs1}}},\ \omega_T = \frac{g_m}{C_{gs1}}.$$

Similar to narrow-band matching, the source inductor, L_s, results in a real resistive value equal to $g_m L_s/C_{gs1}$ to match with the source impedance of 50ohm.

The size of the transistor M1 must be selected carefully. The parasitic capacitance C_{gs1} must follow the required component value in the filter design. On the other hand, the device size must yields to sufficient noise performance and power constraint [9]. It may be necessary to adjust the filter corner frequency and choose a reasonable size in order to meet all the specifications.

3.2.3 *Tunable RLC Tank*

The frequency tuning is achieved by the first order RLC tank, as shown in Fig 3.7. Thus we could derive the impedance as below.

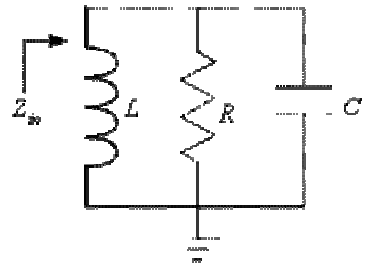


Fig. 3.7 The first order RLC tank.

$$
\begin{aligned}
Z_{in}(j\omega) &= \left(\frac{1}{j\omega L} + j\omega C + \frac{1}{R}\right)^{-1} \qquad \left(\omega_0 = \frac{1}{\sqrt{LC}},\quad Q = \frac{R}{\omega_0 L} = \omega_0 RC\right) \\
&\cong \left(\frac{1}{j(\omega_0 + \Delta\omega)L} + j(\omega_0 + \Delta\omega)C + \frac{1}{R}\right)^{-1} \qquad (Let \quad \omega = \omega_0 + \Delta\omega) \\
&\cong \left(\frac{\frac{1}{j\omega_0 L}}{1 + \frac{\Delta\omega}{\omega_0}} + j(\omega_0 + \Delta\omega)C + \frac{1}{R}\right)^{-1} \qquad \left(use \quad \frac{1}{1+x} \approx 1 - x + \ldots\right) \\
&\cong \left(\frac{1}{j\omega_0 L} - \frac{\frac{\Delta\omega}{\omega_0}}{j\omega_0 L} + j\omega_0 C + j\Delta\omega C + \frac{1}{R}\right)^{-1} \qquad \left(\because \omega_0^2 = \frac{1}{LC}\right) \\
&\cong \left(\frac{1}{R} + 2j\Delta\omega C\right)^{-1} = \frac{1}{\frac{1}{R} + 2j\Delta\omega C} \\
&\cong \frac{R}{1 + 2j\Delta\omega RC} \qquad \left(\because RC = \frac{Q}{\omega_0}\right) \\
&\cong \frac{R}{1 + 2jQ\frac{\Delta\omega}{\omega_0}} \qquad (if \quad R \to \infty) \\
&\cong \frac{1}{j2C\Delta\omega}
\end{aligned}
$$

Consequently, choose tuning L or tuning C according to the result of $Z_{in}(j\omega) \approx \frac{1}{1+2jC\Delta\omega}$. In this work, sub-band in 500MHz should be selected. Thus, the load impedance should not be steep. That is to say the quality of output tunable load must be poor. Larger C will result in narrower selective band. To fix the capacitor value while tuning the inductor, the quality of selective bands independence with

frequency, as shown in Fig. 3.8. If larger C is picked the impedance magnitude will be more precipitous, as the black line shown in Fig. 3.8. Tow of the most used ways for tunable inductors are switching and active inductors. To switch inductors will increase chip area, besides the poor Q resulting from switching parasitic resistors must be considered. There is no such issue in active inductors, but power consumption increase. To maintain low power level, hence a tunable MOS varactor capacitor is chosen to provide frequency tuning. The smaller inductor is chosen to preserve quality factor in the high frequency, as the blue line with circles shown in Fig. 3.9.

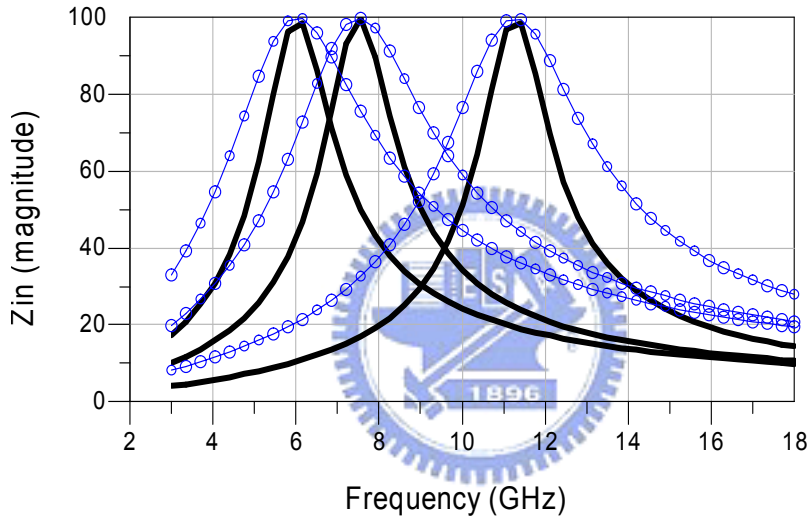


Fig. 3.8 Fix C and tuning L. (the black line shows the larger C value, and the blue line with circle shows the smaller C value.)

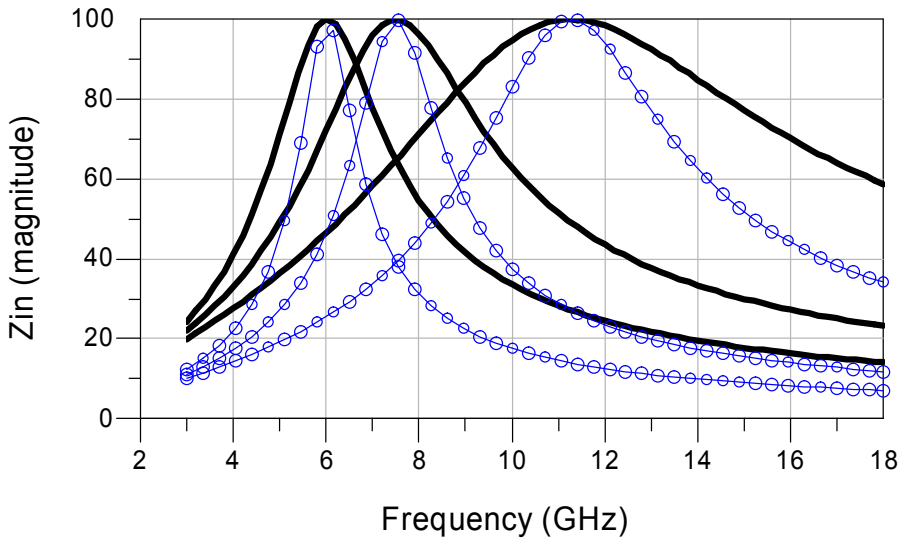


Fig. 3.9 Fix L and tuning C. (the black line shows the larger L value, and the blue line with circle shows the smaller L value.)

In this design, frequency tuning is achieved by a tunable LC tank at the output of the common-gate transistor drain. This resonator consists of a fixed-value inductor and a MOS varactor. To obtain frequency tuning over 6~10GHz, the value of the capacitance in this work varies from 0.46pF to 1.46pF. The equivalent circuit model of the LC tank is as shown in Fig. 3.10, including the gate-drain capacitor, C_{gd2}, of M_2. The resistors R_{ls}, and R_{cs}, standing for the parasitic of the inductor L_d and the varactor C_t, respectively, degrade the quality factor of the resonator. The resonance frequency and the quality factor are therefore determined as

$$\omega_0 = \frac{1}{\sqrt{L_d(C_{gd2}+C_t)}}, \tag{3-11}$$

$$Q = \frac{R_{lp} // R_{cp}}{\omega_0 L_d}, \tag{3-12}$$

where

$$R_{lp} \approx R_{ls} \cdot (Q_L^2 + 1), \quad R_{cp} \approx R_{cs} \cdot (Q_C^2 + 1),$$

$$Q_L = \frac{\omega_0 L_d}{R_{ls}}, Q_C = \frac{1}{\omega_0 R_{cs} C_t}.$$

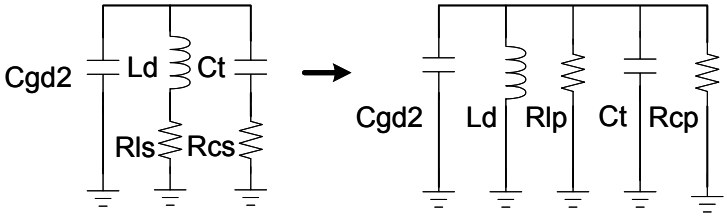


Fig. 3.10 The LC tank transformation.

3.2.4 Gain Compensation Technique

At resonant frequency, the gain of this LNA is mainly proportional to the LC tank impedance level, which can be derived as

$$Z_L = \frac{s(R_{Lp} // R_{Cp})L_d}{s^2(R_{Lp} // R_{Cp})L_d(C_{gd2} + C_t) + sL_d + (R_{Lp} // R_{Cp})}. \quad (3\text{-}13)$$

Higher Q value of the LC tank leads to larger LNA gain. Besides, the impedance level appears to be smaller at lower frequencies. To maintain gain flatness, an inductor L_b is inserted into the cascode stage to enhance the circuit transconductance, G_{m1}, at lower frequencies. The small signal model of the input stage is shown in Fig.3.11. The G_{m1} can be derived as equation (3-14).

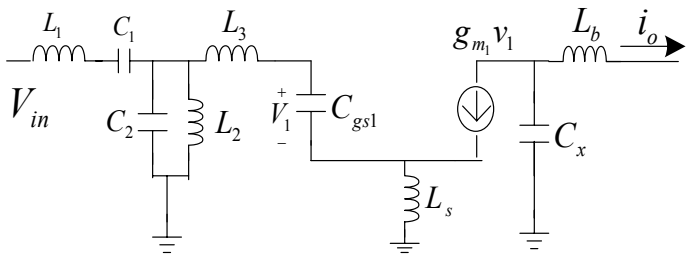


Fig.3.11 The small signal model of the input stage.

$$G_{m1} = \frac{i_o}{V_{in}} = \frac{-g_m/(s^2 L_b C_x + 1)}{s^2 L_s C_{gs1} + s(L_s g_m + C_{gs1} Z_3 + sC_{gs1} Z_1 * \frac{Z_2 + Z_3 + \omega_T L_s}{Z_2})}, \quad (3\text{–}14)$$

where

$$Z_1 = sL_1 + \frac{1}{sC_1},\ Z_2 = sL_2 // \frac{1}{sC_2},$$
$$Z_3 = s(L_3 + L_s) + \frac{1}{sC_{gs1}},\ \omega_T = \frac{g_m}{C_{gs1}},$$

C_x is the sum of the gate-to-drain capacitor and drain-to-source capacitor of M_1. The factor of $(s^2 L_b C_x + 1)$ is less than one at low frequencies such that G_{m1} is enhanced.

3.2.5 Design Considerations and Trade off

This is a tunable low noise amplifier with wideband tunable load and broadband input impedance matching. Since the C_{gs} of M_1 included into the Chebyshev broadband filter design, the capacitance must be around 250fF. Therefore, the size of M_1 is selected to conform to the broadband matching issue. In this work, 132.5um width and the 0.18um length are chosen. However, such choice leads to mismatch noise optimum and the low power level. To overcome those issues, another amended circuit is proporsed in section 3.3.

In order to compensate the smaller gain at the lower frequency which comes from the poor Q factor of the MOS varactor, the inter- stage inductor L_b included is 1.8nH to enhance the transconductance at 6~7GHz. While load impedance is higher, and then the gain is larger. Therefore, the Q factor of the load inductor, L_d, must be as larger as possible. The technique of layout optimization[9] usd increase the quality factor up to 15~16.

3.2.6 Consideration of Layout

As discussed in Section 3.2.5, the higher Q value of the inductor L_d is, the larger gain of the LNA has. Standard CMOS integrated inductors have inherently low quality factor because of serious substrate losses at GHz frequencies. The technique of layout optimization [9] is used to increase the quality factor. The symmetric two-turn inductors are built on the top most metal layer. The width of the inductor is smaller gradually from the outer circle into the inner circle to increase the internal diameter. The width of the outer circle is larger, 34um, to move the Q peak into 6-10 GHz. The quality factor is larger than 15 at 6-10GHz as shown in Fig. 3.12.

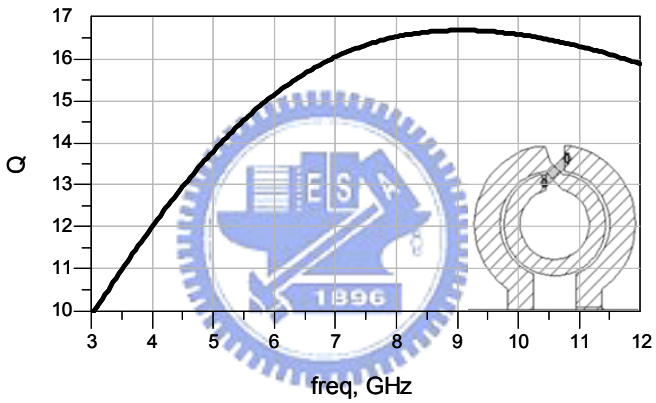


Fig. 3.12 The quality factor of the inductor L_d .

The total chip area is 0.897mm by 0.906mm. The RF input and output ports are placed on opposite sides of the chip to improve the isolation of the output to input port. The patterned ground shield is used for reduce substrate noise. All long interconnects should be minimized and built on the most top metal to minimize the substrate loss.

3.2.7 *Microphotograph of Chip*

The microphotograph of the tunable LNA circuit is shown in Figure3.13. The circuit is fabricated in the TSMC 0.18μm CMOS process technology. The die area including bonding pads is 0.897 mm by 0.906 mm.

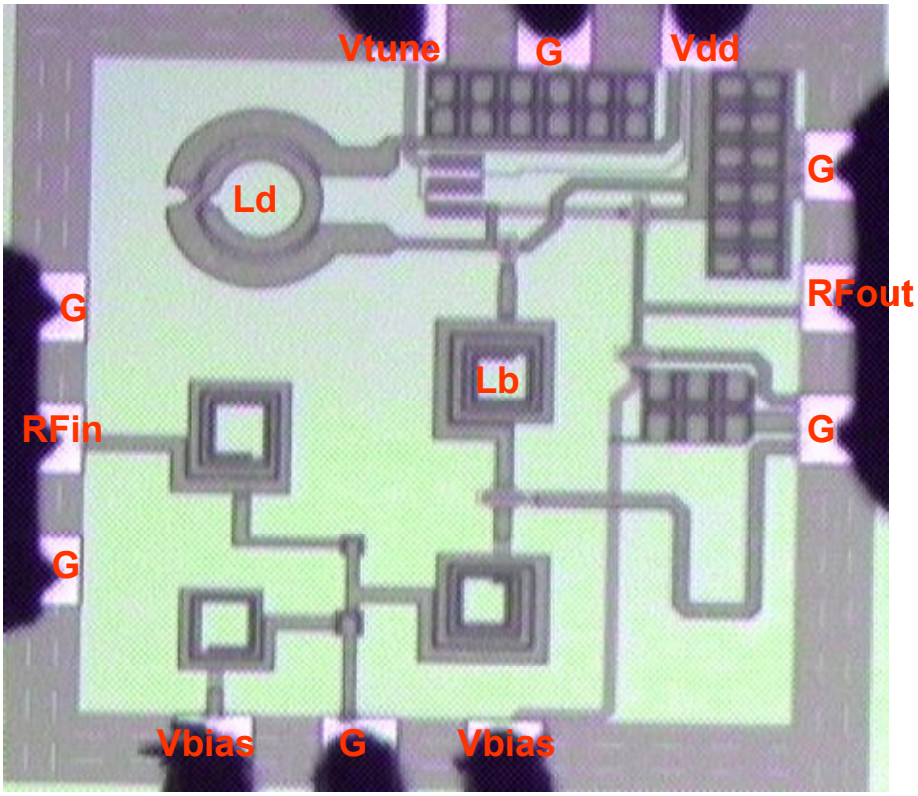


Fig. 3.13 Microphotograph of the tunable LNA.

3.2.8 *Simulation and Measurement results and Discussion*

Measurement is conducted by on-wafer RF probing. Measured results are plotted from Fig. 3.14 to Fig.3.20. Compare with simulation data, the LNA measurement results show narrower tunable range and lower operation frequency over 5.1GHz to 6.8GHz. The measured power gain S21 achieves the maximum value of 7dB at 6.8GHz. Fig. 3.14 shows that condition, the solid black line is the simulation result and the dot gray one the measurement data. The tunable frequency drifts due to

inconsistency of MOS varactor models in design kit of simulator, ADS, and layout model. The discrepancy is shown in Fig. 3.15. Obviously, the varactor capacitance of the layout model in TSMC document is larger then that of the design kit in ADS simulator. Thus the unconfirmed varactor model used results in the conflict measurement results. To re-simulate the circuit used the affirmed varactor model, and then the tunable frequency matches to the measurement data, as shown in the Fig. 3.16. The input return loss is shown in Fig. 3.17, the black line is the measurement data, and the blue line is the simulation data, and the red line with squares is the simulation with 10% drift of the inductors. After considering the 10% drift of the inductors, L_1, L_2, L_g, and L_s, and to re-simulate the circuit gets the similar trend to the measurement data. The measurement and simulation result of output return loss, S22, is shown in Fig. 3.18. Fig. 3.19 is the simulation result of noise figure. Since S11 and S21 matched at 6.8GHz only, therefore the noise figure at 6.8GHz is 5.7dB. The linearity analysis is conducted by the two tone test. Fig.3.21 is IIP3 measured data; lower power gain results in higher linearity. The total power of the tunable LNA is 19.51mW with a power supply 1.5V. Table 3.2 is the summary of measured performance and comparison to other tunable amplifier.

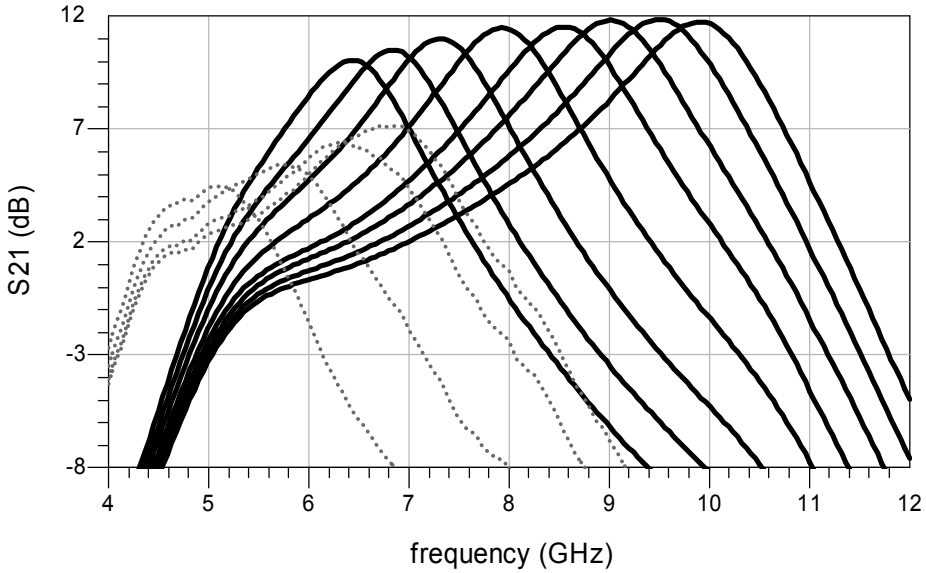


Fig. 3.14 S21 simulation and measured result of the tunable LNA. (Solid black line is the simulation result and the dot gray line is the measurement result.)

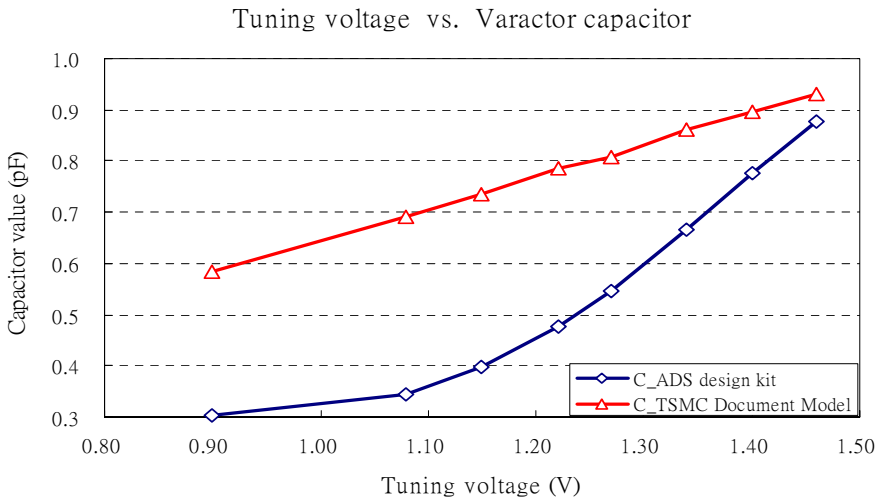


Fig. 3.15 The tuning voltage relative to the varactor capacitance

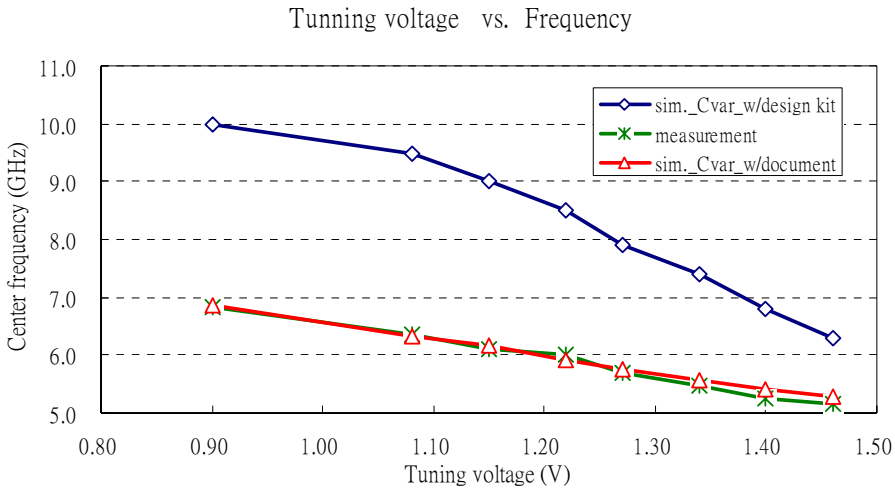


Fig. 3.16 The tuning voltage relative to the center frequency. (the blue line with diamonds is the simulation with the ADS design lit, and the red line with triangles is the simulation with the model in TSMC document, and the green line with stars is the measurement data.)

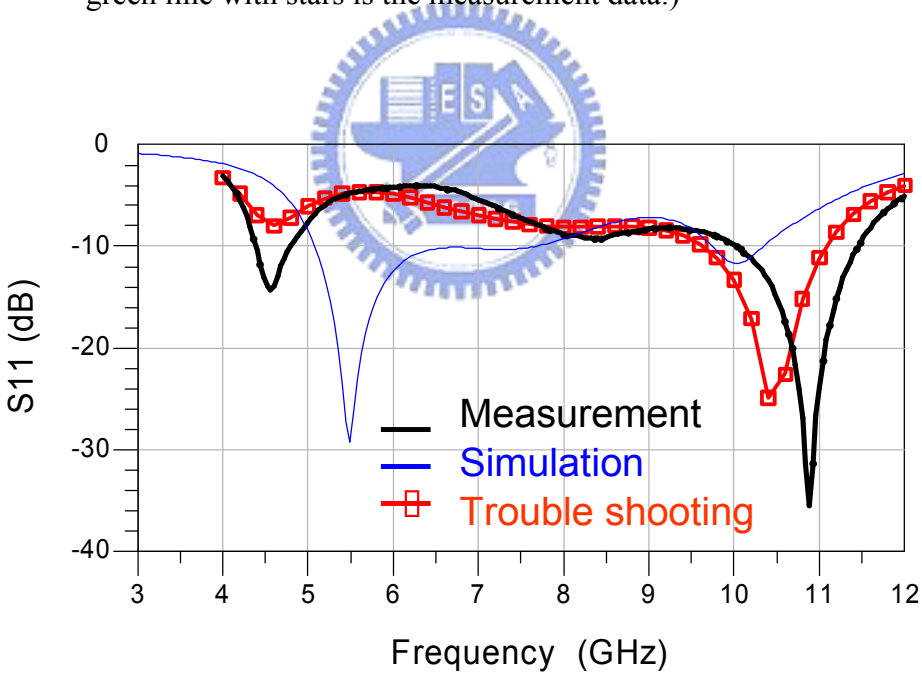
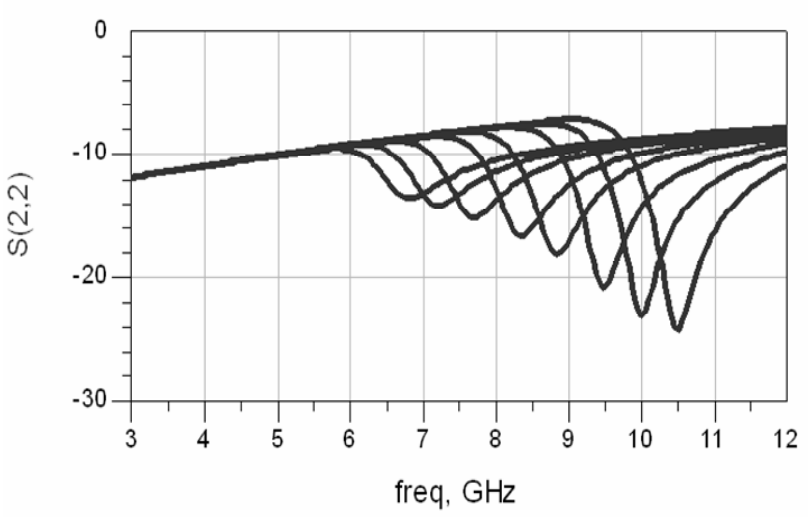
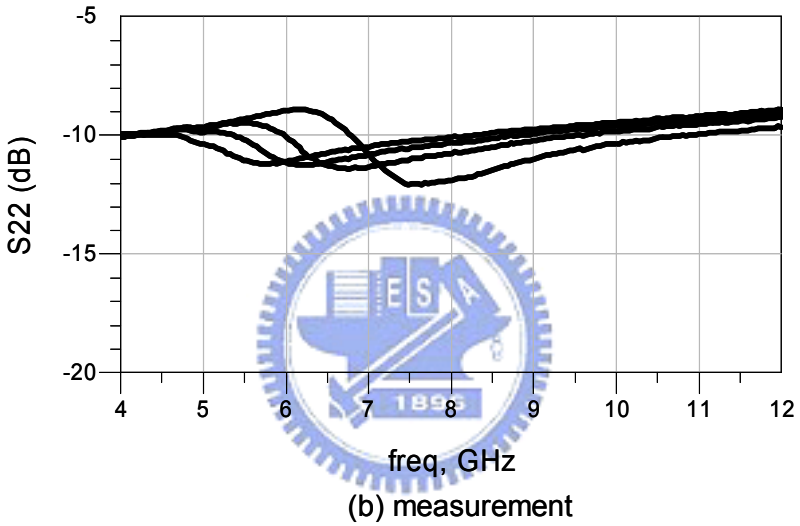


Fig. 3.17 S11 simulation and measured result of the tunable LNA.



(a) simulation



(b) measurement

Fig. 3.18 S22 simulation and measured result of the tunable LNA.

(a) The simulation result (b) The measurement result

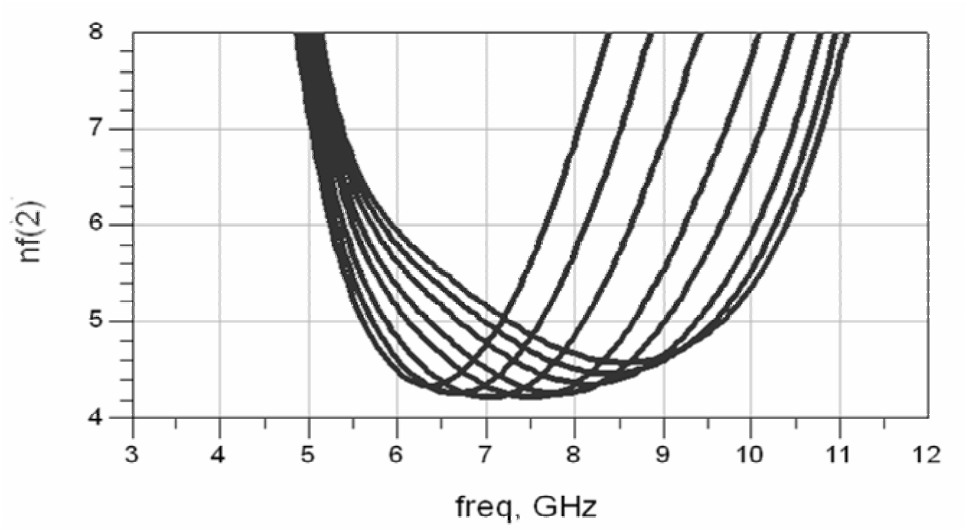


Fig. 3.19 Noise Figure simulation result.

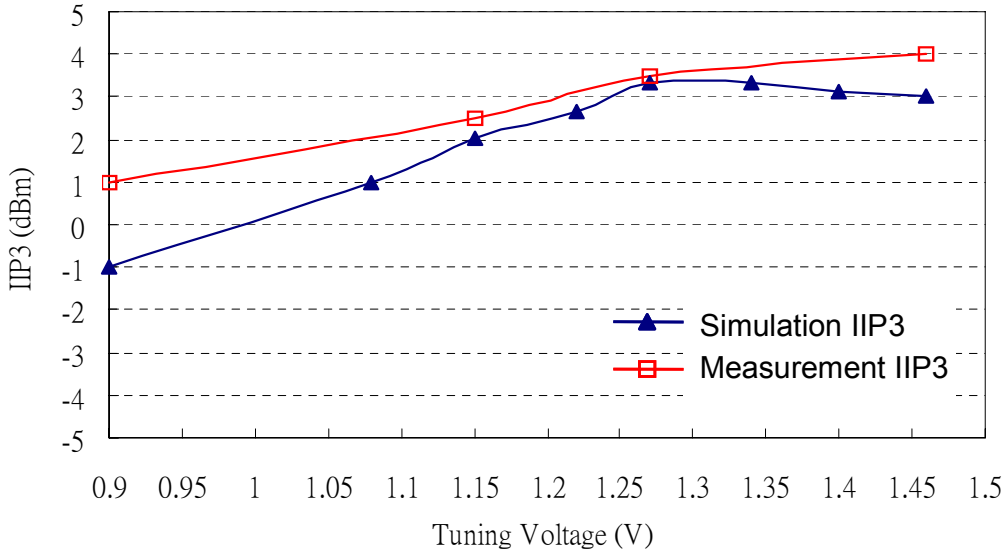


Fig. 3.20 IIP3 versus frequency simulation and measured result.

TABLE 3.2 Summary of measured performance and comparison to other tunable amplifier

Performance	**Summary and Comparison**			
	Simulation	***Measurement***	***[5] ISCAS 02***	***[6] VLSI 04***
Technology	0.18um CMOS Standard			0.25um CMOS IBM
$S_{21(max)}$	11.6 dB	7 dB (at 6.8GHz)	13.2 dB	11.7 dB
S_{11}	<-9dB	<-4 (5~7GHz) <-9 (7~11GHz)	-5.3dB	<-10dB
S_{22}	<-12dB	<-10 (5~7GHz)	-10.3dB	<-24dB
$NF_{(average)}$	4.75 dB	5.7dB (at 6.8GHz)	2.59 dB	2.6 dB
$IIP3_{(average)}$	1.15 dBm	3.2 dBm	N/A	-3.98 dBm
Center Frequency tuning range	6.0 ~ 10.0 GHz	5.1~6.8 GHz	5.6 ~ 5.96 GHz	1.4 ~ 2.0 GHz
Frequency tuning ratio	50%	28%	6%	35%
Power consumption	19.6 mW	19.51 mW	22.2 mW	40 mW

3.3 Improved 6 to 10GHz UWB Tunable LNA

Discussed in section 3.2, the frequency tunable range is narrower then simulation one. The tunable LNA is revised as shown in Fig. 3.21. The amended circuit incorporates not only enhanced band tuning range but also broadband impedance matching to improve noise performance. Since the input broadband matching in the previous circuit, Chebyshev filter design is used. The gate to source capacitor of the transconductance stage is included to consist of the Chebyshev filter. Thus, the noise optimum mismatched as mentioned in section 3.2. The revised circuit achieves wideband input impedance matching by the resonance matching technique. L_1 and C_1 are used to improve the input impedance matching bandwidth. A varactor, C_{var}, and a switch capacitor, C_{sw}, provide frequency tuning capability. M_1 and M_2 consist of cascode configuration to minimize the miller effect and to improve the isolation between the tunable load and broadband input impedance. M_3 and M_4 implement a source- follower output buffer. R_1 and R_2 are used to bias the buffer and the bypass capacitor is put on the gate of M_4 to be an ac ground path. The transconductance (G_m) of the input stage must be designed to compensate the gain discrepancy between sub-bands.

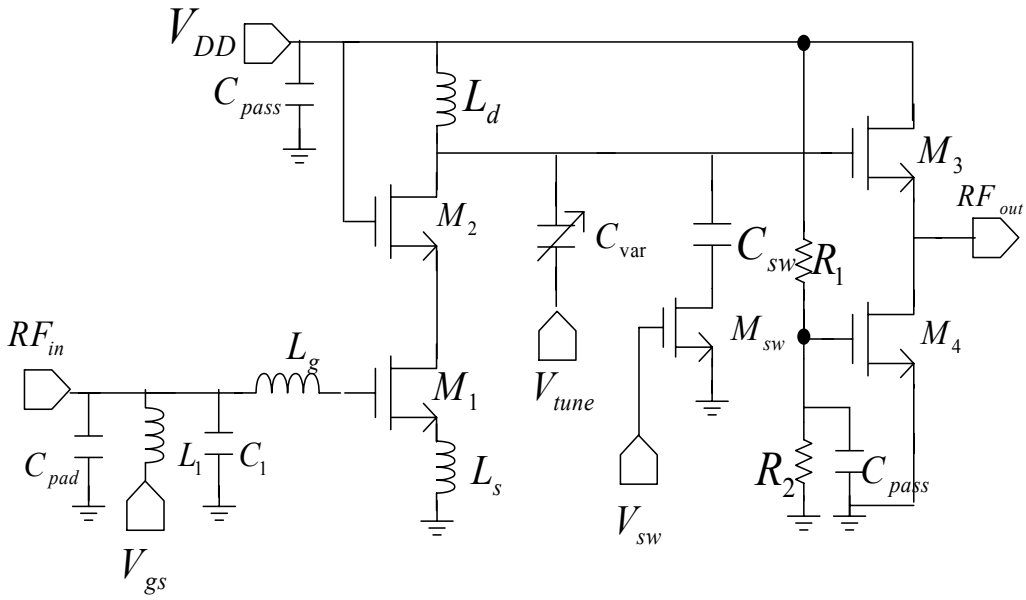


Fig. 3.21 The amended UWB tunable LNA schematic

3.3.1 Frequency Tunable Mechanism

The frequency tuning is enhanced by a switched capacitor at the output tunable load. This resonator consists of a fixed-value inductor, a tunable MOS varactor and a capacitor serial with the switching transistor. The equivalent circuit model of the tunable load is as shown in Fig. 3.22 (a), including the gate-drain capacitor, C_{gd2}, of M_2. The resistors R_{ls}, and R_{cs}, standing for the parasitic of the inductor L_d and the varactor C_{var}, respectively, degrade the quality factor of the resonator. While tuning the operation frequency in low band, the switch transistor must be turned on and the channel of M_{sw} will induce a parasitic resistance, R_{gms}, and a overlap capacitor, C_{ovgd}, as shown in Fig. 3.22 (b). At M_{sw} turned on, the ac current will flow through R_{gms}, as the red line shown in Fig. 3.22 (b) because of the impedance of R_{gms} much smaller then C_{ovgd}. When M_{sw} turns off, the overlap capacitor, $C_{ovgd,}$ is series with C_{sw} resulting in a small capacitor to operate at high frequency

tuning, as shown in Fig. 3.22 (c). Fig. 3.22(b) and (c) could be expressed in parallel form as Fig. 3.22 (d) and (e) respectively. The capacitor C_{tot1} equals to C_{gd2} plus C_{sw} and C_{tot2} equals to C_{gd2} plus C_{sw} series with C_{ovgd}. The resonance frequency and the quality factor are therefore determined as

$$\omega_{0\_swon} = \frac{1}{\sqrt{L_d (C_{tot1} + C_{\text{var}})}}, \tag{3-15}$$

$$\omega_{0\_swoff} = \frac{1}{\sqrt{L_d (C_{tot2} + C_{\text{var}})}}, \tag{3-16}$$

$$Q_{swon} = \frac{R_{lp} // R_{cp} // R_{gmp}}{\omega_0 L_d}, \tag{3-17}$$

$$Q_{swoff} = \frac{R_{lp} // R_{cp}}{\omega_0 L_d}, \tag{3-18}$$

where

$$R_{lp} \approx R_{ls} \cdot (Q_{L_d}^2 + 1), \quad R_{cp} \approx R_{cs} \cdot (Q_{C_{\text{var}}}^2 + 1), \quad R_{gmp} \approx R_{gms} \cdot (Q_{C_{sw}}^2 + 1) \quad , \tag{3–19}$$

$$Q_{L_d} = \frac{\omega_0 L_d}{R_{ls}}, \quad Q_{C_{\text{var}}} = \frac{1}{\omega_0 R_{cs} C_{\text{var}}}, \quad Q_{C_{sw}} = \frac{1}{\omega_0 R_{gms} C_{sw}}. \tag{3–20}$$

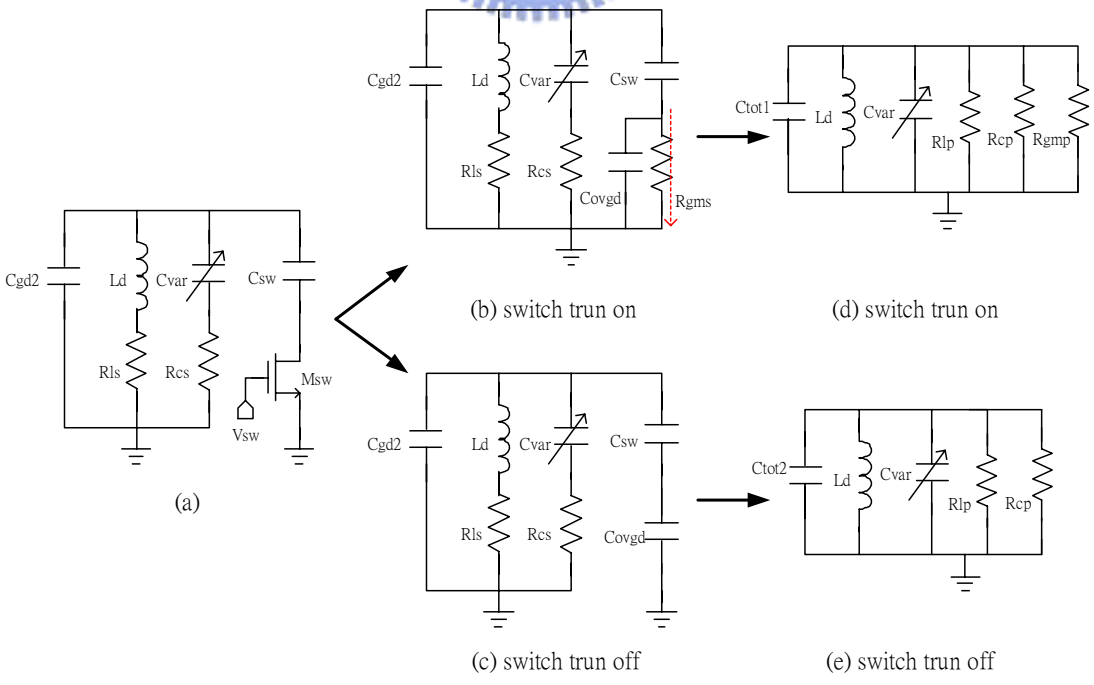


Fig. 3.22 The tunable mechanism.

3.3.2 Resonance Matching Technique

The input impedance small signal model is as shown in Fig.3.23, the well-known narrow band impedance can be derived as Z, which the impedance trend in smith chart is shown as the solid line in Fig. 3.24. At the resonant frequency, ω_0, impedance of Z is matched to 50 ohm, and while the operation frequency is upper than the resonant frequency, Z characters an inductive impedance, and otherwise characters a capacitive impedance. Tank, L_1 and C_1 is added to provide capacitive impedance in the upper operation frequency to compensate the inductive one, and the same compensation technique is in the lower operation frequency. The impedance compensation trend is the dot line, $Z^{'}$, as shown in Fig. 3.24. The broad band input impedance matching is achieved by the resonance technique.

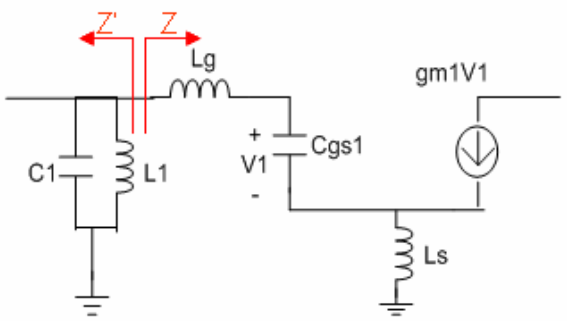


Fig. 3.23 The input impedance small signal model.

$$Z = L_s\omega_t + j\left(\omega L_s + \omega L_g - \frac{1}{\omega C_{gs1}}\right) \qquad \omega_0 = \frac{1}{\sqrt{(L_s + L_g)C_{gs1}}} \quad , \tag{3-21}$$

$$Z^{'} = \left(j\omega C_1 + \frac{1}{j\omega L_1}\right)^{-1} \quad . \tag{3-22}$$

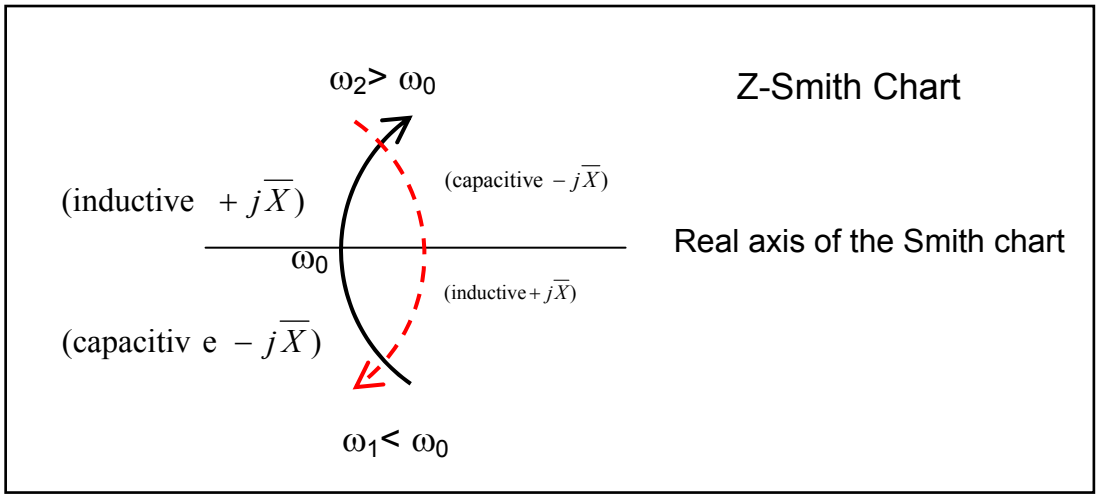


Fig. 3.24 The impedance trend in smith chart.

3.3.3 Design Considerations and Trade off

As mentioned in section 3.3.1, the tunable load impedance is different from the switch transistor turned on or off. Thus the gain of tunable LNA in this work is mainly proportional to the LC tank impedance level at resonance frequency, which can be derived as

$$Z_{L\_swon} = \frac{s(R_{Lp} // R_{Cp} // R_{gmp})L_d}{s^2(R_{Lp} // R_{Cp} // R_{gmp})L_d(C_{tot1} + C_{\text{var}}) + sL_d + (R_{Lp} // R_{Cp} // R_{gmp})}, \quad (3\text{-}23)$$

$$Z_{L\_swoff} = \frac{s(R_{Lp} // R_{Cp})L_d}{s^2(R_{Lp} // R_{Cp})L_d(C_{tot2} + C_{\text{var}}) + sL_d + (R_{Lp} // R_{Cp})}. \quad (3\text{-}24)$$

To compare equation (3-23) with (3-24), there is smaller load impedance at low frequency due to the parasitic resistance of switched transistor, R_{gmp}. The smaller load impedance level leads to the low power gain. Thus, the power gain at low frequency is enhanced by boosted the transconductance, G_{m1}, of M_1 at 6-to-7 GHz. The G_{m1} could be derived as

$$G_{\text{m1}} = \frac{i_o}{v_i} = -g_{m1}\frac{\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}, \quad (3\text{-}25)$$

$$\omega_0 = \frac{1}{\sqrt{C_{gs1}(L_s + L_g)}} \quad , \quad Q = \frac{1}{\omega_0 g_{m1} L_s} . \tag{3-26}$$

Obviously, G_{m1} is shown as a second order low pass filter. The Q value of that filter is designed to enhance G_{m1}. Besides G_{m1} to be augmented for low gain level, the high Q value of the LC tank also leads to large LNA gain. Thus, how large the parasitic resistance is must be concerned while the size of switched transistor is chosen. The larger size of switched transistor is, the smaller parasitic resistance is. But the large size of M_{sw} leads to large overlap capacitor, C_{ovgd}. That will result in the large capacitor of C_{tot2} at M_{sw} turned off, as shown in Fig 3.22(e), which comes the operation frequency drift to lower then what designed. In this work, the size of M_{sw} would be chosen at 87.5um width and 0.18 lengths. In this work, the C_{gs} of M_1 does not be included into the broadband filter design and the noise optimization could be achieved. The noise figure is optimized to be 3.23-to-3.8 dB. The source- follower buffer is biased by the voltage divided of R_1 and R_2. The process variation of resistors must be concerned to make sure the output buffer satisfied the output impedance matching to 50 ohm for measurement.

3.3.4 Consideration of Layout

The higher Q value of the inductor L_d is, the larger gain of the LNA has. The small inductor leads to the Q peak at higher frequency. In this work, small inductor value of 0.5nH is used. In order to move the Q peak into 6- to 10 GHz, the width of L_d is 34um. The total chip area is 0.825mm by 0.94mm. The RF input and output ports are placed on opposite sides of the chip to improve the isolation of the output to input port. The patterned ground shield is used for reduce substrate noise. Except L_d , all other inductors are used by the layout of TSMC supported. All long interconnects should be minimized and built on the most top metal to minimize the substrate loss.

All interconnects of the DC voltage supply has bypass capacitors to be ac ground path to reduce the parasitic inductances.

3.3.5 Microphotograph of Chip

The microphotograph of the tunable LNA circuit is shown in Figure3.25. The circuit is fabricated in the TSMC 0.18μm CMOS process technology. The die area including bonding pads is 0.825 mm by 0.94 mm.

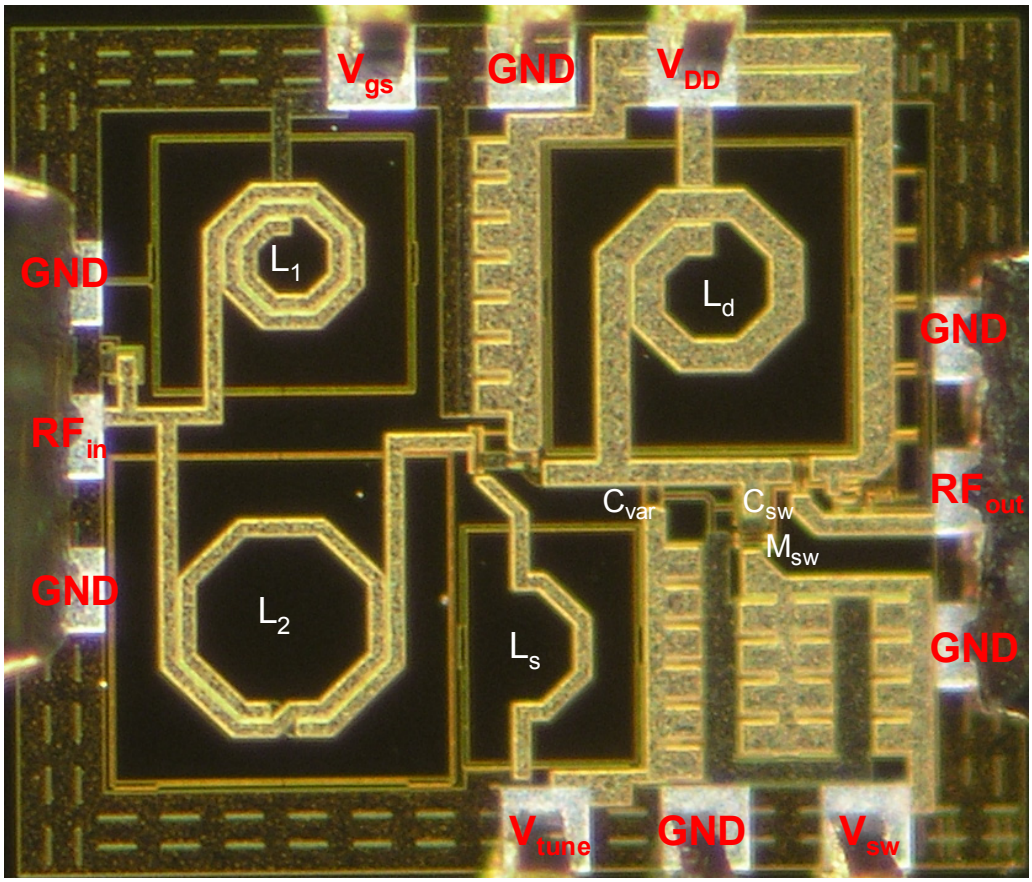
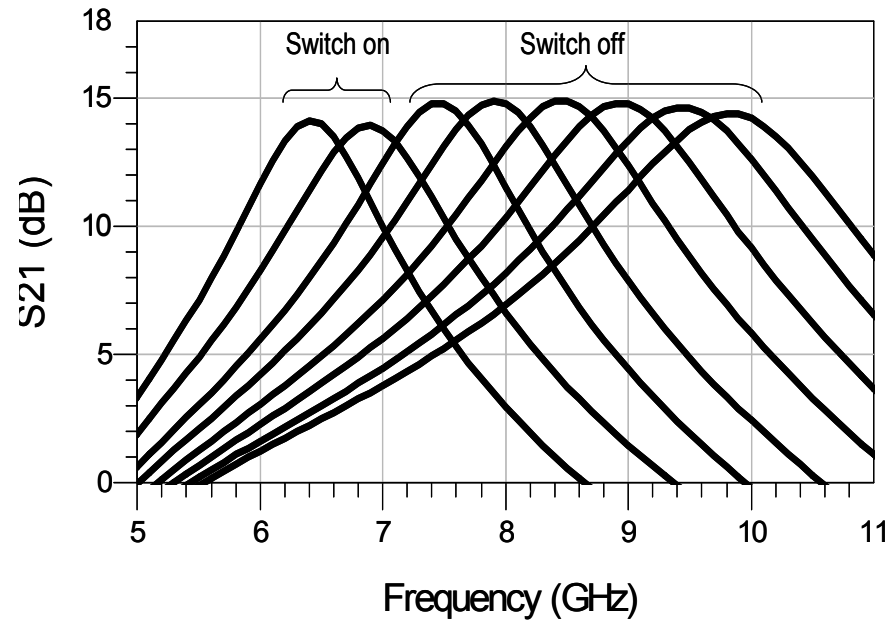


Fig. 3.25 Microphotograph of the amended tunable LNA.

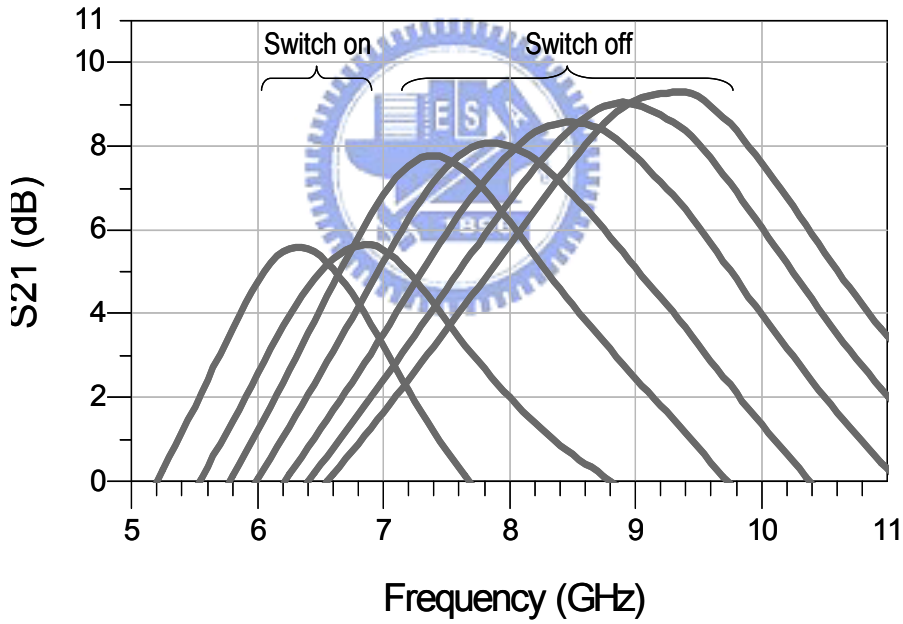
3.3.6 Simulation and Measurement results and Discussion

Measurement is conducted by on-wafer RF probing. Measured results are plotted as shown from Fig. 3.26 to Fig.3.29. The LNA measurement shows frequency tunable range from 6.3GHz to 9.3GHz, which is smaller then design due to 100fF

parasitic capacitance in the layout of the tunable LC tank load. The measured power gain S21 achieves the maximum value of 9.3dB at 9.4GHz. According to equation (3-23), while the parasitic resistance of the switched transistor is large and thus the power gain will become small. The measured gain is larger at high frequency then at low frequency due to C_{gs1} of M_1 is smaller then designed; thus comes at G_{m1} enhanced at high frequency. Fig. 3.26 shows the condition. The input return loss is shown in Fig. 3.27. As we mentioned in section 3.3.4, all the metal lines of DC bias supply need bypass capacitors to be ac ground path to reduce the parasitic inductance. However, the metal line of the gate bias for M_1 had been left out to add the ac ground path. The parasitic inductance of 10pH needs to be added. 10fF of layout parasitic capacitor of C_1 also has to be included. The smaller C_{gs1} of M_1, the added parasitic inductance and the capacitance are all together included to re-simulate the input impedance, and thus the input impedance trend is more matched to measurement results. The measurement and simulation result of output return loss, S22, is shown in Fig. 3.28. Fig. 3.29 is the simulation and measurement result of noise figure. The linearity analysis is conducted by the two tone test. Fig.3.30 is the IIP3 measured data. The total power of the tunable LNA is 17.44mW with a power supply 1.5V. Table 3.3 is the summary of measured performance and comparison to the previous tunable amplifier.

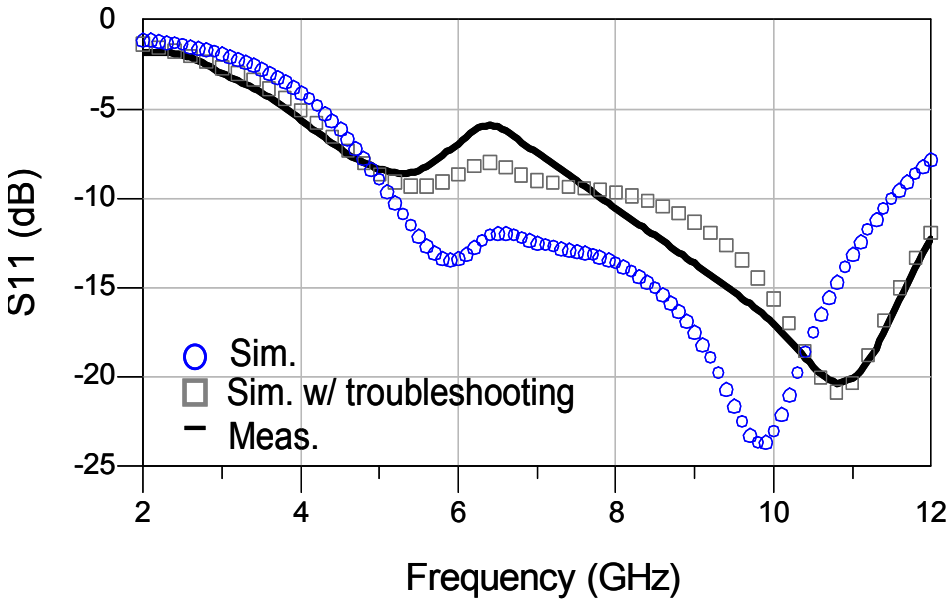


(a) S22 Simulation

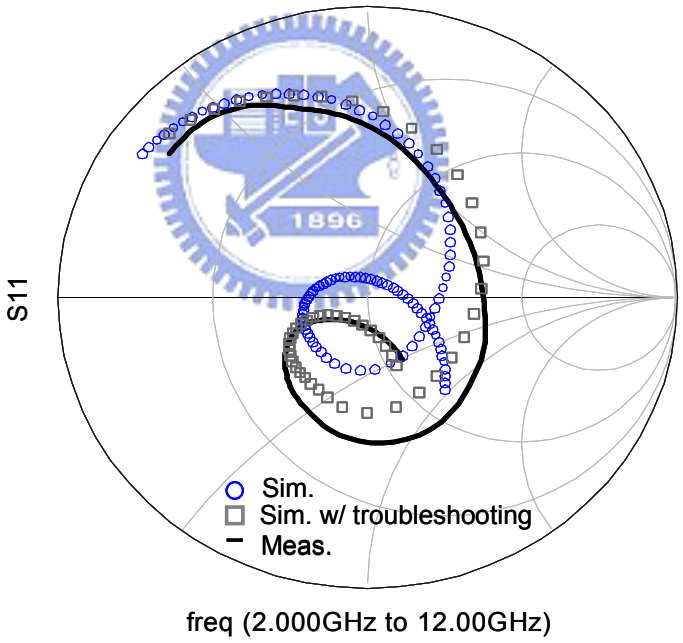


(b) S22 measurement

Fig. 3.26 S21 simulation and measured result of the amended tunable LNA, (a) is the simulation result and (b) is the measurement result.

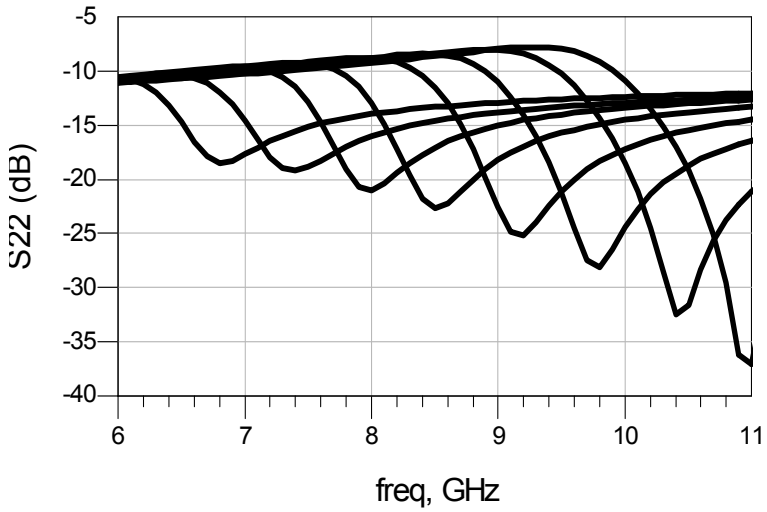


(a) S11 measurement and simulation results

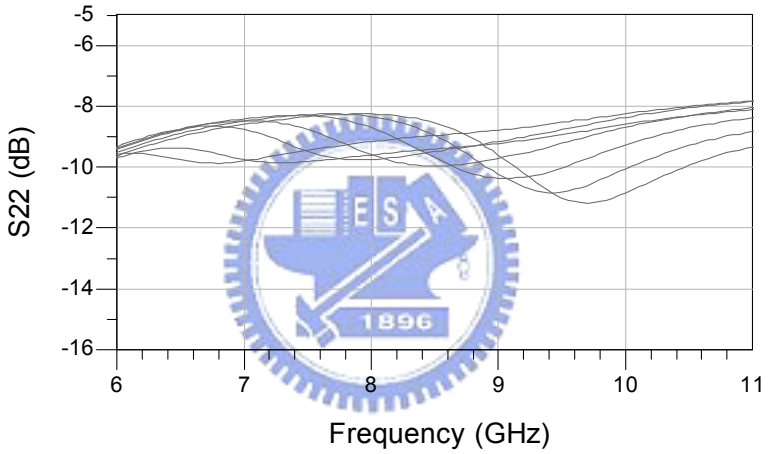


(b) S11 smith chart

Fig. 3.27 S11 simulation and measured result of the amended tunable LNA, (a) S11 measurement and simulation results and (b) S11 smith chart trend.



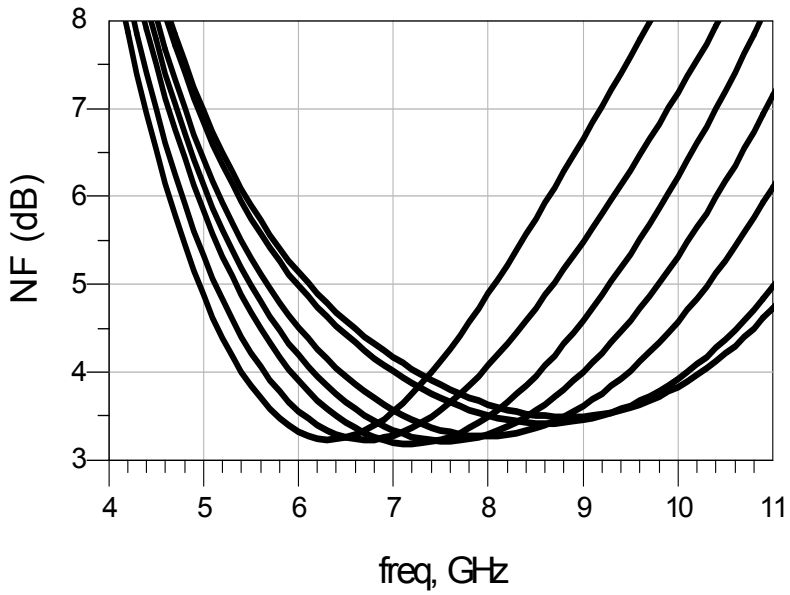
(a) S22 simulation



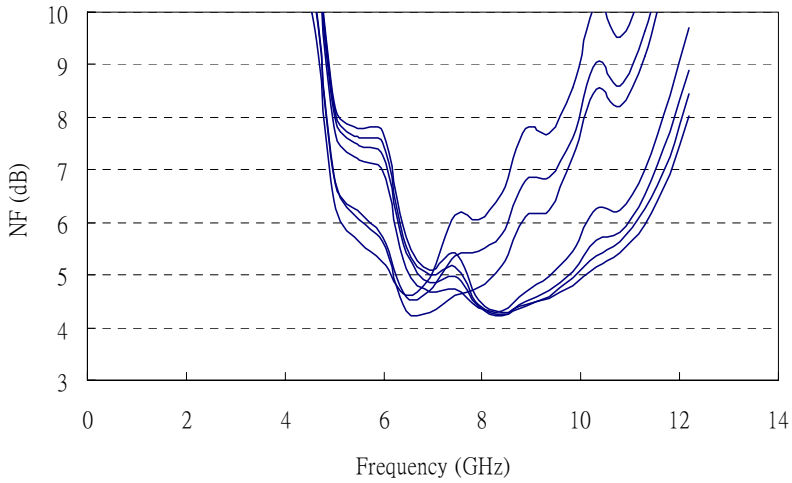
(b) S22 measurement

Fig. 3.28 S22 simulation and measured result of the amended tunable LNA.

(a) The simulation result, (b) The measurement result.



(a) NF simulation



(b) NF measurement

Fig. 3.29 Noise Figure of the amended tunable LNA. (a) simulation result (b) measurement result.

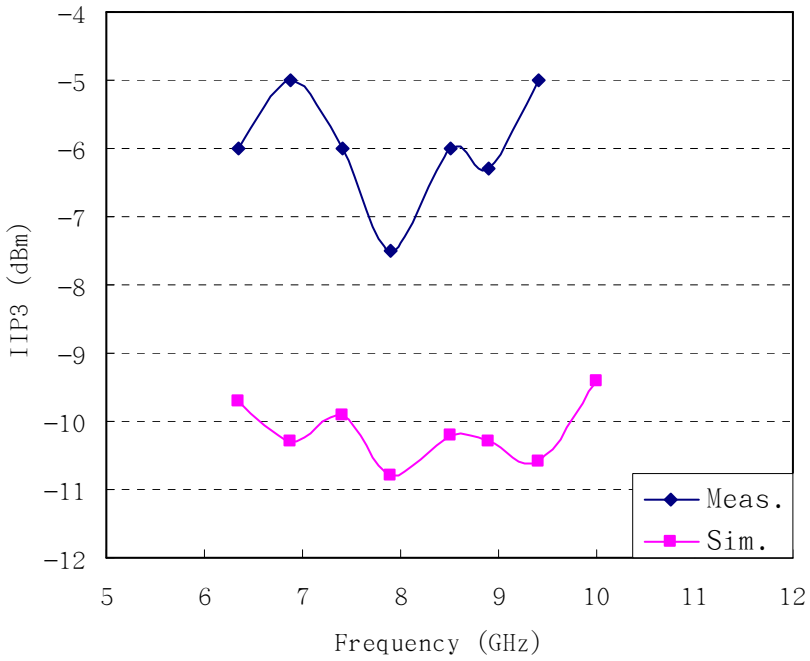


Fig. 3.30 IIP3

TABLE 3.3 Summary of measured performance and comparison to the previous tunable amplifier

Performance	Summary and Comparison			
	Section 3.2 Simulation	***Section 3.2 Measurement***	***This work Simulation***	***This work Measurement***
Technology	0.18um TSMC CMOS Standard			
Supply voltage	1.5V			
$S_{21(max)}$	11.6 dB	7 dB (at 6.8GHz)	14.9 dB	9.3 dB
S_{11}	<-9dB	<-4 (5~7GHz) <-9 (7~11GHz)	<-11dB	<-6dB
S_{22}	<-12dB	<-10 (5~7GHz)	<-15dB	<-10 dB
S_{12}	<-38 dB	< -40(5~7GHz)	<-40 dB	<-41 dB
$NF_{(average)}$	4.75 dB	5.7dB (at 6.8GHz)	3.5 dB	4.5 dB
$IIP3_{(average)}$	1.15 dBm	3.2 dBm	-10 dBm	-6 dBm
Center Frequency tuning range	6.0 ~ 10.0 GHz	5.1~6.8 GHz	6.3 ~ 10 GHz	6.3 ~ 9.4 GHz
Frequency tuning ratio	50%	28%	45.3%	39.5%
Area	0.813 mm^2		0.776 mm^2	
Power consumption	19.6 mW	19.51 mW	17.4 mW	17.44 mW

3.4 A Tunable LNA with MEMES Inductors for UWB Mode-2 Device

3.4.1 Motivation

As mentioned in section 3.2, to do the wideband frequency tuning could be achieved by switching capacitors or inductors while those components have high quality factors. Nowadays, the high performance of micromachined spiral inductors has been proposed [10]. The inductor with the underneath substrate removal has four times quality factor improvement than the conventional one. The suspended inductors with the cross membrane supporting and the underneath substrate removal have not only high Q performance but also better reliability for wideband application [11]. To do frequency tunable range from 3.1 GHz to 8 GHz, there is congenital limitation by only using MOS varactor as discussed in section 3.2. To enhance the tunable range with switched capacitor is proposed in section 3.3, but this way the poor quality factor of large capacitance will degrade the gain at low frequency. Thus, to maintain gain flatness over 5GHz is a critical consideration. In this section, switched micromachined inductors and MOS varactor used to make the frequency tunable capability. To integrate micromachined inductors with the chip die of 0.18um CMOS process, the thermo- compression boding technique is used. The LNA of frequency tuning range over 5 GHz, low noise performance and low power consumption is proposed.

3.4.2 Circuit Architecture

The schematic of the proposed LNA circuit is similar to that in section 3.2, as shown in Fig. 3.31, exception the inductor switched mechanism and the external capacitor parallel with C_{gs} of M_1 included. The wideband input matching by a three-section band-pass Chebyshev filter configuration consists of L_1, L_2, L_g, L_s, C_1,

C_2, C_{ex} and C_{gs} of M_1, where C_{ex} provides enough capacitance for satisfying the filter design issue. Micromachined inductors, L_1, L_2, and L_g have small parasitic resistance due to substrate lossless with underneath substrate removal. Thus, the thermal noise will be decreased apparently. M_{sw} is used to switch inductors. A large resister R_b is employed to provide high impedance for reducing the overlap parasitic capacitances. The micromachined inductor, L_{d1}, is utilized to provide high power gain. M_3 and M_4 implement a source- follower output buffer. R_1 and R_2 are used to bias the buffer.

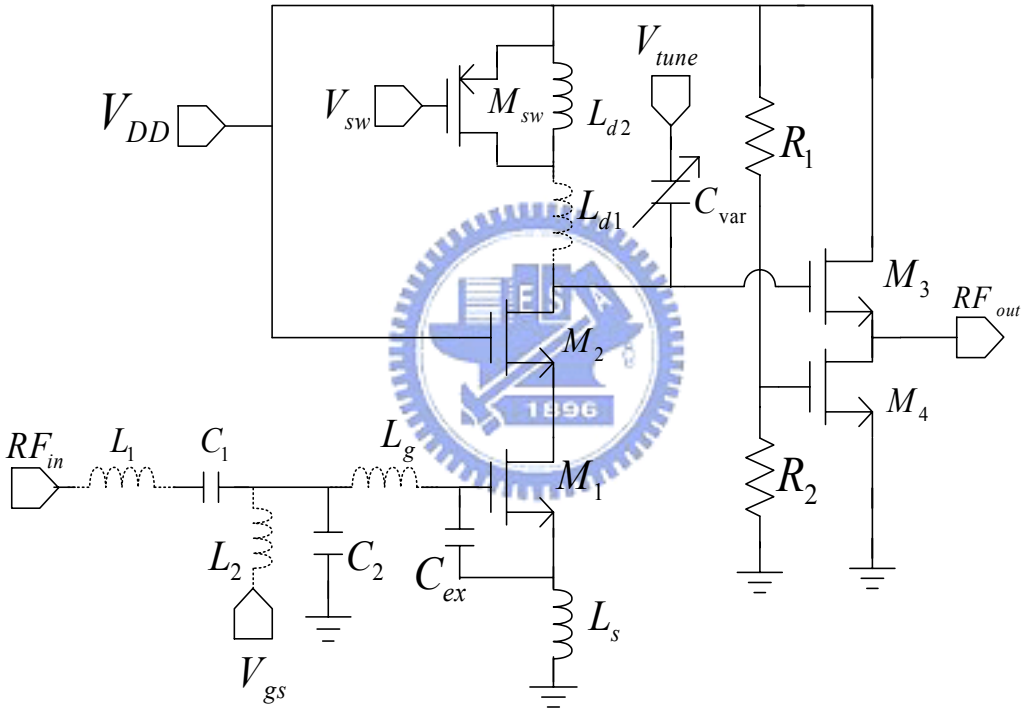


Fig. 3.31 The schematic of the tunable LNA for 3~8 GHz.

(Where inductors with dot line are MEMS fabricated.)

3.4.3 MEMS Inductors

The micromachined inductor is fabricated with underneath substrate removal to decrease the substrate loss at high frequency and that will provide a high quality factor inductor. However, the micromachined passive components tend to be affected by the external disturbance, such as air pressure, mechanical thermal force and gravity, etc. Thus, the suspended inductors with the cross membrane supporting are proposed to increase the reliability of the micromachined inductors [11]. The suspended inductor with the cross membrane supporting high Q performance of micromachined spiral inductors is shown in Fig. 3.32, and the cross view of the cross membrane inductor is shown in Fig. 3.33. The measurement result of high Q inductors is shown in Fig.3.34. The measurement shows that the Q of inductor can achieve 45, while the inductor value is around 4nH at 4~8GHz. The amazing good performance is expected to improve the circuit design for radio frequency.

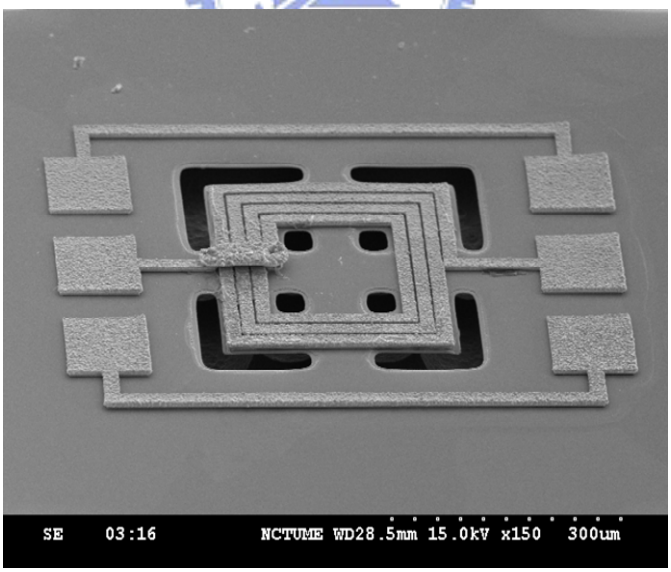


Fig. 3.32 The suspended inductor with the cross membrane supporting

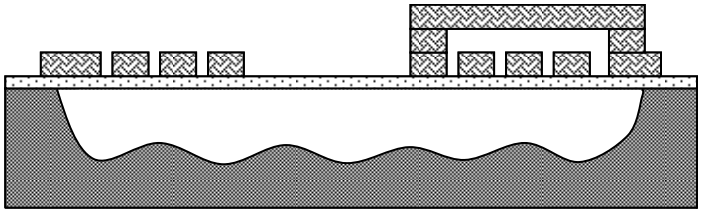


Fig. 3.33 The cross view of the cross membrane inductor.

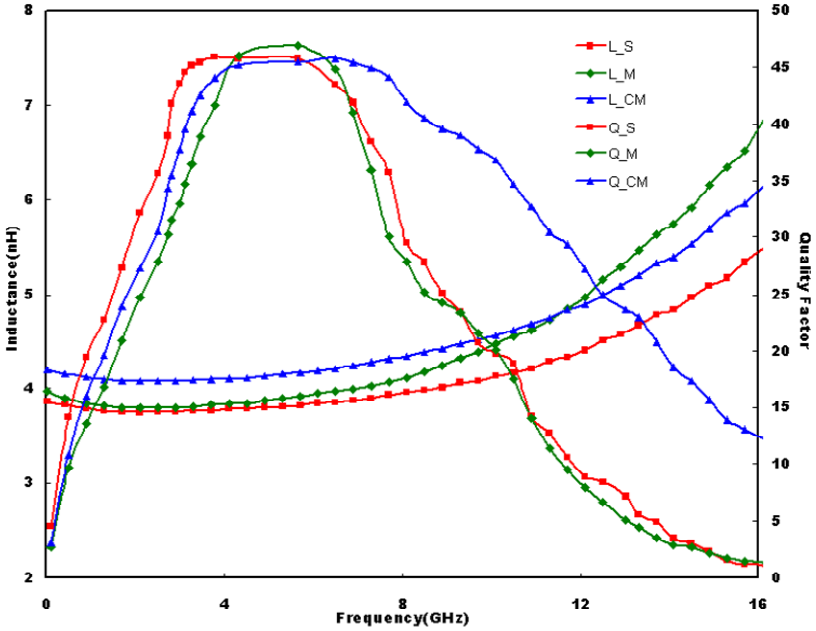


Fig. 3.34 The measurement result of the cross membrane inductor.

(Where S denotes suspend, M denotes membrane and CM denotes cross membrane.)

3.4.4 Ultra Wide-band Tunable Load

The tunable load with switched capacitor, as shown in Fig. 3.35(a), is discussed in section 3.3. The power gain is proportion to Q value of the load as mentioned in section 3.3. Therefore, using switched capacitor can not maintain gain flatness due to Q degraded for a large capacitor at low frequency. High Q MEMS inductors are used to maintain gain flatness over several GHz. Output tunable load with switched inductor consist of L_{d1}, L_{d2} and M_{sw}, as shown in Fig. 3.35(b).

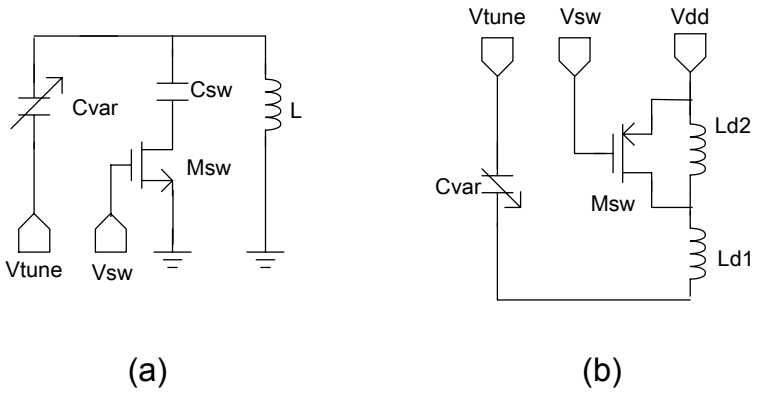


Fig. 3.35 The tunable mechanism (a) the switched capacitor, (b) the switched inductor

The equivalent model of switched inductors is shown in Fig. 3.36, where R_b is included to reduce the overlap parasitic capacitor. Fig. 3.36 (a) shows the equivalent model of switched transistor turned on. When M_{sw} turns on, the signal current will flow as the blue line path. Otherwise, while M_{sw} turns off, it will be the red path as shown in Fig. 3.36 (b).

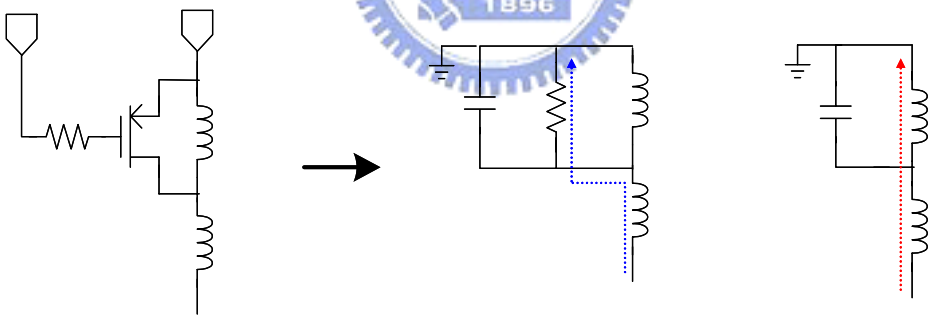


Fig. 3.36 The effected inductor, (a) switch turned on, (b) switch turned off.

When M_{sw} turns on, the effected inductance is as

$$L_{eff\_swon} \approx L_{d1}, \quad Q_{eff\_swon} = \frac{\omega L_{d1}}{R_p + R_{ls}}. \tag{3-27}$$

R_{ls} is the parasitic resistance of L_{d1}. The Q value of effected inductor will degrade by R_{ls} and R_p. As mentioned in section 3.1, Q values of L and C will affect the load

impedance level. Therefore, the high Q micromachined inductor, L_{d1}, is used to maintain high enough load impedance. While M_{sw} turns off, the effected inductor value is as

$$L_{eff\_swoff}(\omega) = L_{d1} + \frac{L_{d2}}{1-\omega^2 L_{d2} C_{ovp}} \quad . \tag{3-28}$$

Obviously, there is a self resonant frequency $\omega_{self} = \sqrt{L_{d2} C_{ovp}}$. The self resonant frequency must move over the operating frequency to diminish the effect, as shown in Fig. 3.37. Small C_{ovp} results in high self resonant frequency. Small C_{ovp} indicates small size of M_{sw}, which will increase the parasitic resistance R_p. Therefore, the optimum size of M_{sw} is a critical design in this work.

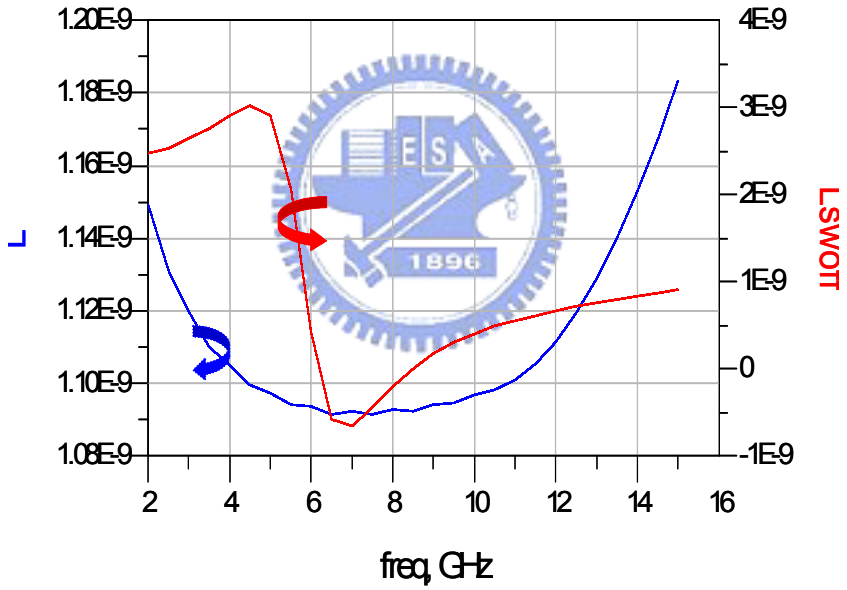


Fig. 3.37 The equivalent inductor value.

3.4.5 Noise Considerations

The broadband input matching approach in section 3.2 is trade off by the noise performance and the power consumption. To improve the noise performance, the high Q micromachined inductors are used in input broadband matching to decrease the thermal noise. The external capacitor parallel with C_{gs} of M_1 is applied

for power level decreasing. The noise model of NMOS with external capacitor is shown in Fig. 3.38(a), and the small signal model is in Fig. 3.38(b). The equivalent noise voltage and current source are derived as equation (3-29) and (3-30) for without and with external capacitor, respectively.

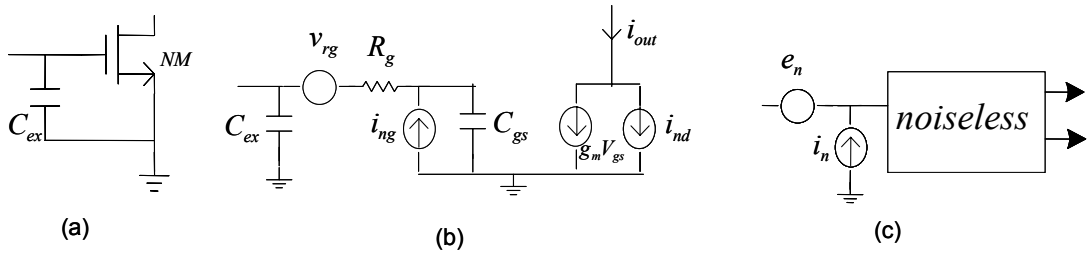


Fig. 3.38 The noise model, (a) NMOS with external capacitor, (b) the small signal noise model, (c) the equivalent noise model.

$$i_n = i_{nd}\frac{sC_{gs}}{g_m} + i_{ng}$$
$$e_n = i_{nd}\frac{1 + sC_{gs}R_g}{g_m} + i_{ng}R_g + v_{rg} \quad . \qquad (3\text{-}29)$$

$$i_{n\_c_{ex}} = i_{nd}\frac{sC_{gs}}{g_m}\left(1 + sC_t R_g\right)\frac{C_{ex}}{C_t} + i_{ng}\left(1 + sC_{ex}R_g\right) + v_{rg}sC_{ex}$$
$$e_{n\_c_{ex}} = i_{nd}\frac{1 + sC_{gs}R_g}{g_m} + i_{ng}R_g + v_{rg} \quad , \qquad (3\text{-}30)$$

where $C_t = C_{gs} + C_{ex}$.

Let the value of the gate- to- source capacitor is fixed. Compare with two conditions, $i_{n\_C_{ex}}$ is obviously smaller then i_n because of $\frac{C_{ex}}{C_t}$ lower then unity. And $e_{n\_C_{ex}}$ is also smaller then e_n due to that C_{gs} with C_{ex} is smaller then C_{gs} without C_{ex}. Thus, conclude that the noise will be decreased by external capacitor added.

3.4.6 Consideration of Layout

To test the DC current, the consideration schematic and layout is shown in Fig. 3.39 and Fig. 3.40. In Fig. 3.39, the dot line pad, V_{DD_DC} and V_{gs_DC}, is only for DC current test. The dot line between L_{d2} and drain of M_2 is used for DC current path of testing and it will be moved by laser cut. Another dot line between gate of M_1 and pad, V_{gs_DC}, is used to bias M_1, and will be removed too. L_1, L_2, L_g, and L_{d1} are fabricated in micromachined inductors. In order to bond the chip die with the micromachined inductors, the passivating layer is drawn on the connected point. All interconnect metal lines are considered for circuit design.Fig.3.40 shows the layout of the chip die.

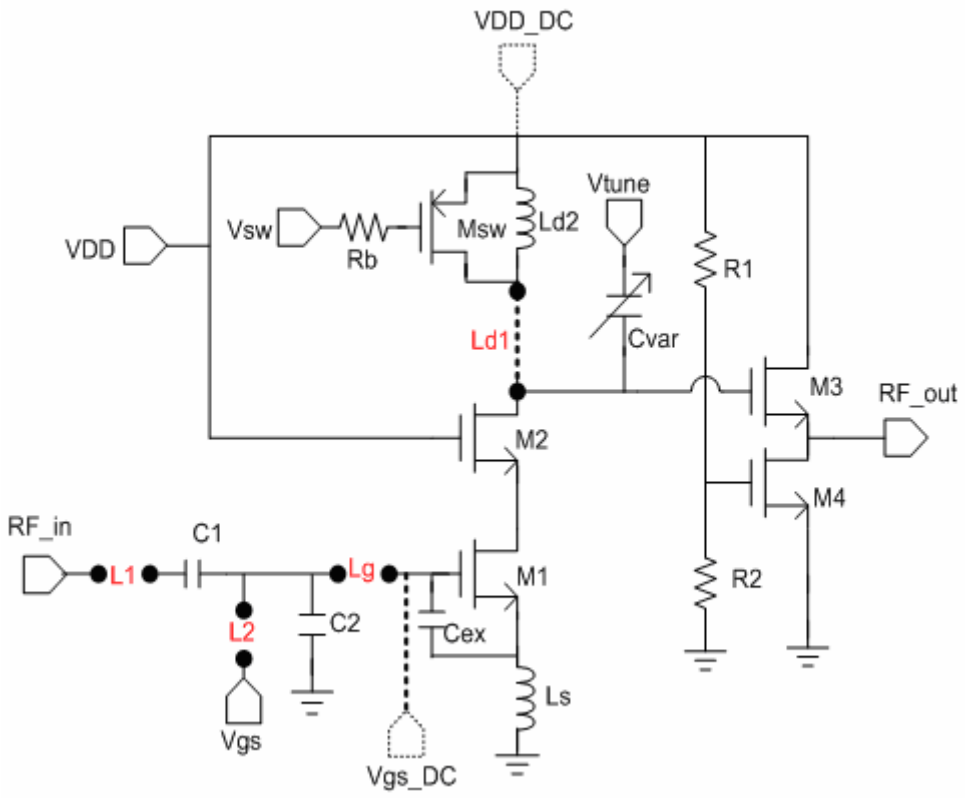


Fig. 3.39 Schematic of the tunable LNA fabricated on the chip die

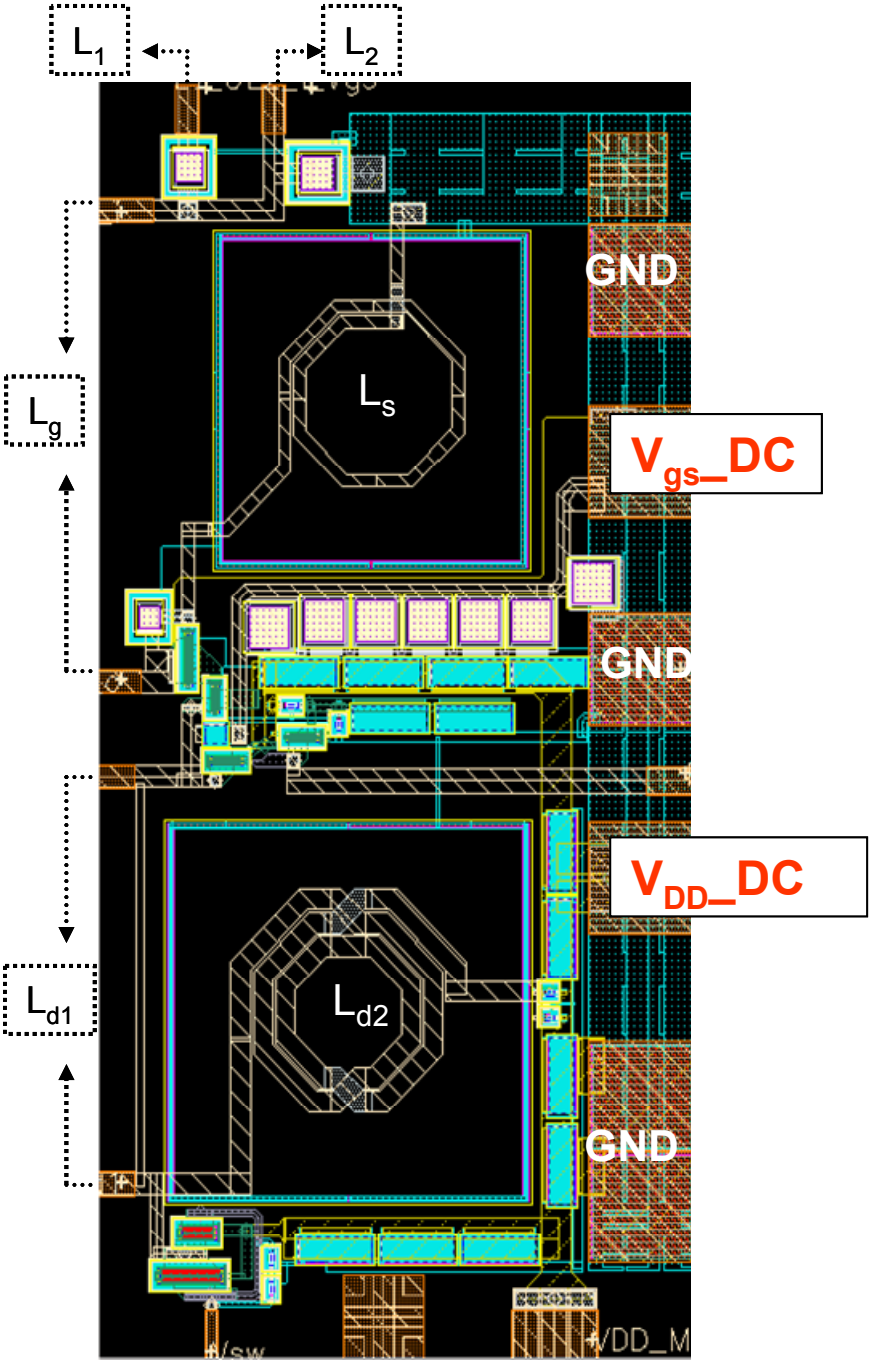


Fig. 3.40 Layout of the chip die

3.4.7 Package Integrated Technique

The complete layout of this work is shown in Fig. 3.41. All the ground pads are connected together to have the same reference plan for the chip die and the micromachined inductors mask. The thermo- compression bonding is used as shown in Fig. 3.42. The temperature is better at 375^0C for fusing the connected gold metal layer.

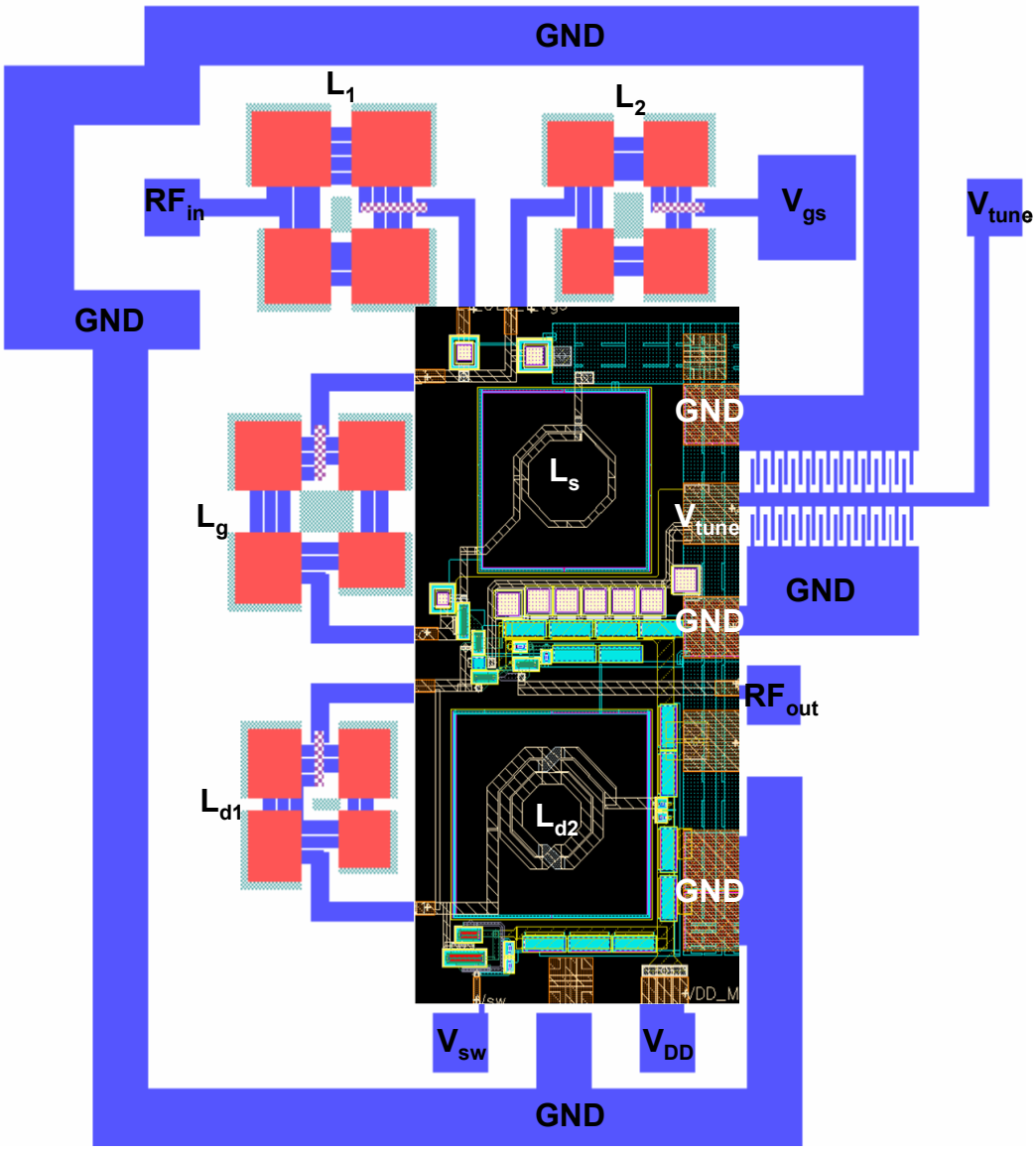


Fig. 3.41 Layout of the complete integrated circuit

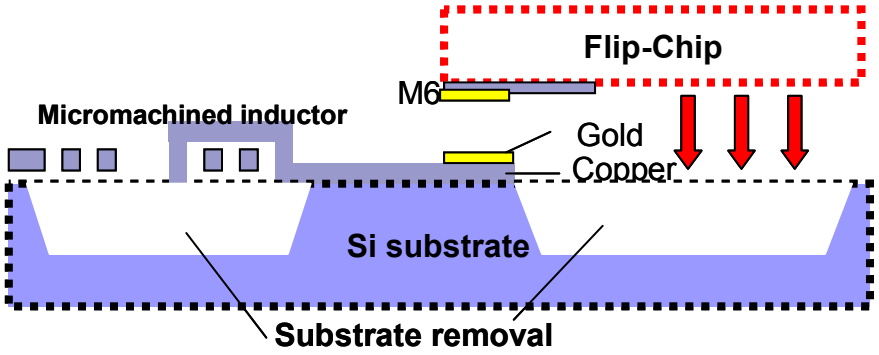


Fig. 3.42 The bonding technique

3.4.8 Simulation results and Comparison

Lastly, the simulation results and compare with that similar circuit with switched MIM capacitor summarized in section 3.2. Table 3.4 shows that.

TABLE 3.4 Summary of simulation performance and comparison to the circuit of section 3.2

Performance	**Summary and Comparison**	
	Circuit of Section 3.2 Simulation Switched with MIM Cap.	***Circuit of this work Simulation Switched with MEMS Ind.***
Technology	0.18um TSMC CMOS Standard	
Supply voltage	1.5V	
Center Frequency tuning range	3.1 ~ 8 GHz	
$S_{21(range)}$	6.5~11.1 dB	11.7~13.2
S_{11}	< -9.5 dB	<-10 dB
S_{22}	<-12 dB	<-14 dB
S_{12}	<-38 dB	<-36 dB
$NF_{(average)}$	6.2 dB	3.5 dB
$IIP3_{(average)}$	~ 0 dBm	~ -5 dBm
Power consumption	21.5 mW	10.5 mW
*$FOM_{(worse\ case)}$	0.156	0.302

$$* FOM_{LNA} = \frac{G[abs] \cdot IIP_3[mW] \cdot f[GHz]}{(NF-1)[abs] \cdot P_D[mW]}$$

Chapter 4

Conclusion

The wideband tunable LNA apply for the receiver path of UWB system was proposed and the amended tunable circuit for band tuning capability was also fabricated in standard TSMC 0.18μm CMOS process. The tunable LNA achieved tunable frequency range over 6.3 GHz to 9.3 GHz. To enhance the tunable range and to improve the noise performance, the high Q MEMES inductors were integrated with the tunable low noise amplifier in the third circuit. The tunable LNA circuit with MEMS inductors was proposed in low power level and achieved ultra- wideband frequency tunable range over 3.1GHz to 8GHz and average noise figure of 3.5dB in 10.5 mW power used.

Chapter 5

Future Work

The wideband tunable LNA with MEMS inductors for UWB Mode-2 device is taped out. While the measurement is consistent with the target proposed, the circuit can extended to a wideband tunable front- end receiver for UWB system in low noise and low power performance.

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