國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

適用於超寬頻無線通訊之高速五階轉導－電容濾波器設計

A High Speed Fifth Order Gm-C Filter

For Ultra-wideband Wireless Applications

研 究 生:楊富昌　　　　　　　Fu-Chang Yang

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中華民國九十四年六月

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碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao Tung University

In Partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronic Engineering

June, 2005

HsinChu, Taiwan, Republic of China

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摘　要

本論文完成一適用於超寬頻無線通訊之濾波器設計，以五階 elliptic 低通濾波器來達成最窄的過渡頻帶(transition band)，整個濾波器是用轉導、電容組成並採取低敏感度的 LC 階梯型電路，其中轉導電路使用對稱及非對稱差動對來改善線性度，以及負電阻技巧來增加差模輸出電阻，濾波器之全諧波失真(Total Harmonic Distortion)在 0.52V 峰對峰訊號下有-40dB，輸入相關雜訊電壓為 211.8uVrms，當考慮 20MHz 輸入訊號時，動態範圍(Dynamic Range)為 58.4 dB，消耗的功率在 1.8-v 的供應電壓下為 32.25mW 其中包括 12.1mW 的輸出緩衝器，質優值(Figure-of-Merit)為 59.75dB，此設計是以聯電 0.18 微米製程來實現，為了方便量測，整個電路是採用矽品所提供之 QFN 系列包裝，並以印刷電路板做為量測模組，量測結果頻寬為 226MHz，增益為-4.07dB 通帶起伏(ripple)為 1.32dB，功率消耗為 43.2mW。

High Speed Fifth order Gm-C Filters

For Ultra-wideband Wireless Applications

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Abstract

A 5th order CMOS high frequency elliptic low pass filter is designed to achieve narrowest transition band. The filter is composed of Gm blocks and capacitances. The symmetrical ＆ unsymmetrical differential pair increases Gm linearity, and negative impedance increases Gm differential output resistance. The total harmonic distortion (THD) of this filter is -40dB within 0.52Vp-p. Input-referred noise is 211.8uVrms. Dynamic range is 58.4dB for 20MHz input. The power consumption of filters is 32.25mW (include 12.1mW output buffer) from 1.8V supply. The figure-of-merit for the filter is 59.75dB. The filter is implemented in UMC 0.18-μm CMOS technology and has been packaged in SPIL QFN20 which is mounted on PCB board in favor of measurement. The f_{3db} is 226MHz and gain is -4.07 dB with 1.32 dB passband ripple. The power dissipation of this filter is 43.2mW.

誌 謝

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Chapter 1

Introduction

Ultra-wideband (UWB) is a new wireless technology approved by Federal

Communications Commission (FCC) in US [1]. The IEEE 802.15.3a task group (TG3a) is

currently developing a UWB standard from the proposals submitted by different companies. It

is now left with two primary proposals, Multi-Band OFDM and Direct Sequence UWB.

Figure 1.1 shows Proposed UWB transceiver block diagram for MB OFDM system. TX and

RX both need filters to suppress unwanted high frequency spectrum. For this system, the

channel bandwidth has been extended to 528MHz. With such high frequency demand, the Gm

block is ubiquitous as filter element in communication system. Because the Gm has very high

bandwidth and well suits to high frequency filter design. Many commonly used MOS circuit

simulation even does not model an upper-frequency limit in the intrinsic conversion from

gate-source voltage to drain current (except gate-drain capacitance). Unless we consider non

quasi-static or gate-resistance effects, a high-frequency limit is hardly found [2]. The elliptic

low pass filter is preferred on account of high requirement for side-band suppression in UWB

system. As the sub-channels near cutoff frequency are not used in UWB MB-OFDM

specification, the nonlinear phase property of elliptic filter is not concerned. The newly

unlicensed UWB opens doors to wireless high-speed communications and has been exciting

tremendous academic research interest.
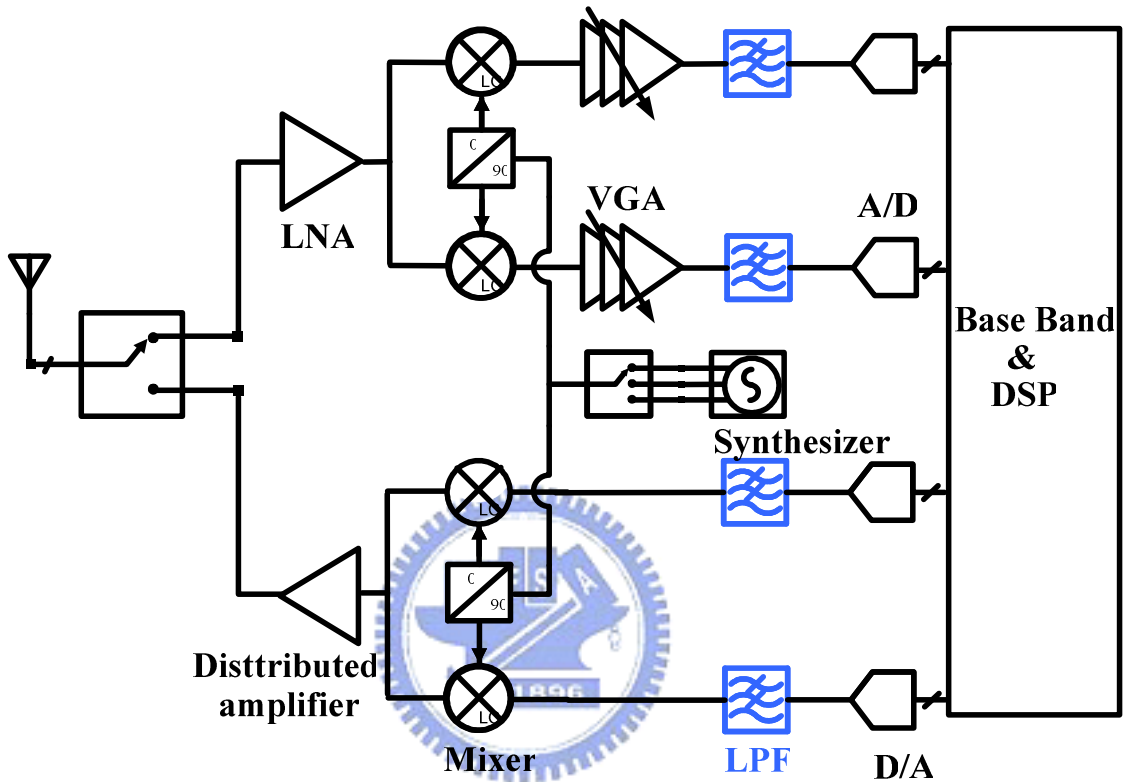
Figure 1.1 Proposed UWB transceiver block diagram

1.1 Motivation

The UWB MB-OFDM sets targets of low power consumption and low cost. The

complementary metal-oxide semiconductor (CMOS) technology is the best choice to make it

since the physical layer implemented in CMOS process consumes less power than others and

can be easily integrated with existing MAC layer implemented in CMOS technology and

consequently has lower cost. The research goal of this thesis is to implement a high speed low

pass filter in CMOS technology for wireless UWB applications. A historical overview range

from 1992 of continuous-time filters is given in Figure1.2. This overview is not intended to be

complete but only gives an impression of the progress in analog CMOS continuous-time
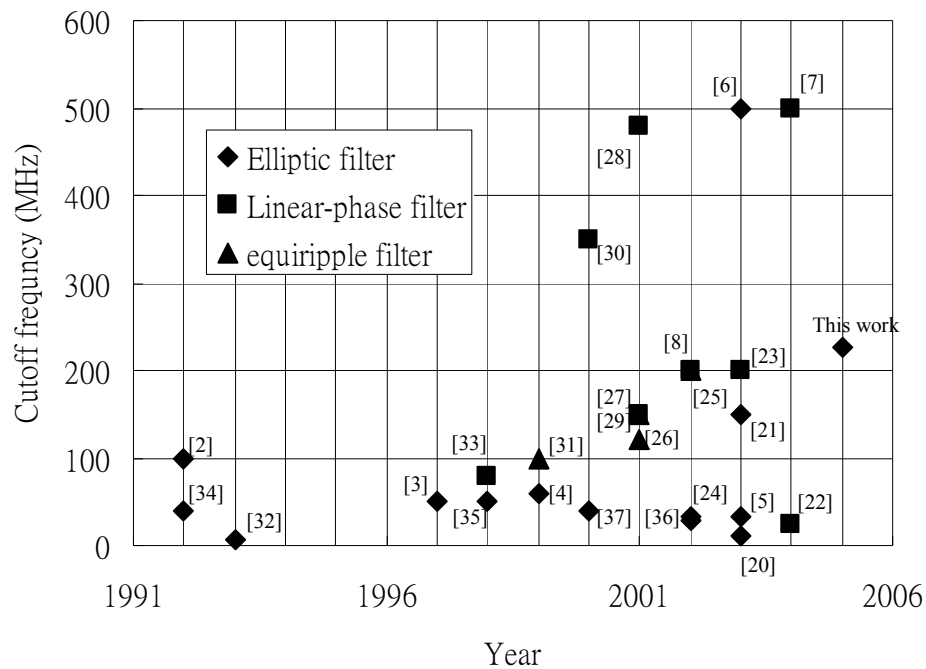
filters.

Figure 1.2 Overview of some publications on continuous-time analog monolithic filters

1.2 Specification

Filters are classified according to the functions they are to perform. For anti-aliasing

filter in UWB TX system, there needs a high frequency LPF to filter out D/A quantization

noise. The D/A sample-rate is higher than Nyquist-Rate, so the specification of the LPF for

TX path is relaxed. On the other hand, the side band frequency is very close to signal band for

UWB RX system. The transmitter & receiver specifications are shown in Figure 1.3 and 1.4.

3

LTCC BPF
BW=3-10GHz
Pout,avg=-10dBm
Pout,peak=0dBm

Distributed AMP
BW=3-10GHz
Gain=12dB
Pout,avg=-8dBm
Pout,peak=2dBm
OP1db=5dBm
OIP3=15dBm

Passive Mixer
BW=3-10GHz
ConvGain=-10dB
Pout,avg=-20dBm
Pout,peak=-10dBm

5th Elliptic LPF
F3dB = 245 MHz
In-Band ripple<1dB
-12 dB at 260Mhz
-20 dB at 300Mhz

5 bit DAC
1056MHz
Low Power(40mW)
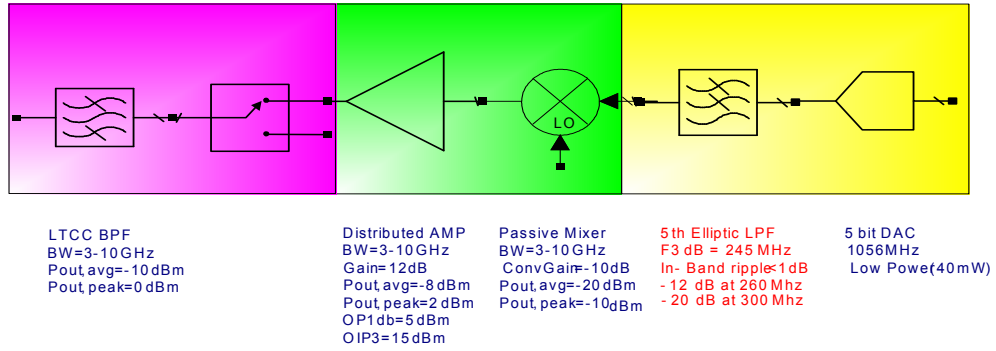
Figure 1.3 specification of TX path

LTCC BPF
BW=3-10GHz
Pout,avg=-10dBm
Pout,peak=0dBm

BandGroup1 LNA
BW=3-5GHz
Gain=25dB
NF=3 dB

BandGroup1 Mixer
BW=3-5GHz
ConvGain=0dB
NF=8 dB

PGA
Gain=25-75dB
GainCtrl=5bit

5th Elliptic LPF
F3dB = 245 MHz
In Band ripple<1dB
-12 dB at 260Mhz
-20 dB at 300Mhz

5 bit ADC
528 MHz
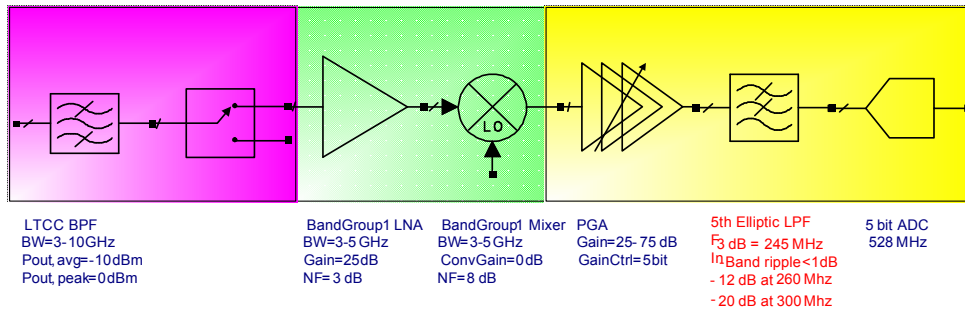
Figure 1.4 specification of RX path

1.3 Organization

The organization of this thesis is overviewed as following:

Chapter 2 gives some basic concept of high frequency filter design. Chapter 3 deals with transconductor analysis and design. High linear and high output resistance technique is introduced and the transconductor will be compared with other Gm of different linearity skills. Chapter 4 demonstrates the simulation of the proposed LC ladder filters by Gm-C topology. The high speed elliptic filter is implemented in 0.18μm CMOS technology and performs in post-simulation result in Chapter 5. In the same chapter the figure-of-merit is introduced to make a comparison with other filters. Chapter 6 concludes with a summary of contributions and suggestions for future work.

Chapter 2

Overview Of High Frequency Filters

In this chapter, some fundamental concepts in the design of high frequency filters, together with the frequency response of elliptic filters will be reviewed. Filters are classified according to the functions they perform. Since our filters are designed for the UWB receivers/transmitters, it will be focused on low pass filters in this thesis. In section 2.1, the terminology of low pass filters is described. The circuit level implementation methods are described in section 2.2.
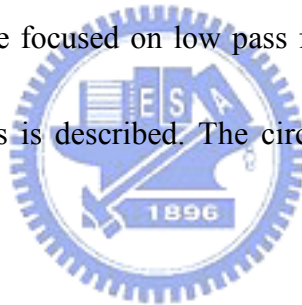
2.1 Terminology

The LPF in the UWB receiving path is required to have sharp transition band with minimum power constraint to filter out sideband noise. Figure 2.1 shows five types of 5th order LPF filters with cutoff frequency at 250MHz for comparison. Elliptic (cauer) filters are found to be the best choice owing to its ability to meet the stringent specification i.e. better sharpness. Although elliptic filters have non-linear phase response as shown in Figure 2.1(b). However, our design is targeted to a MB-OFDM UWB system, and the non-linear phase response is therefore not a critical issue in designing the LPF.
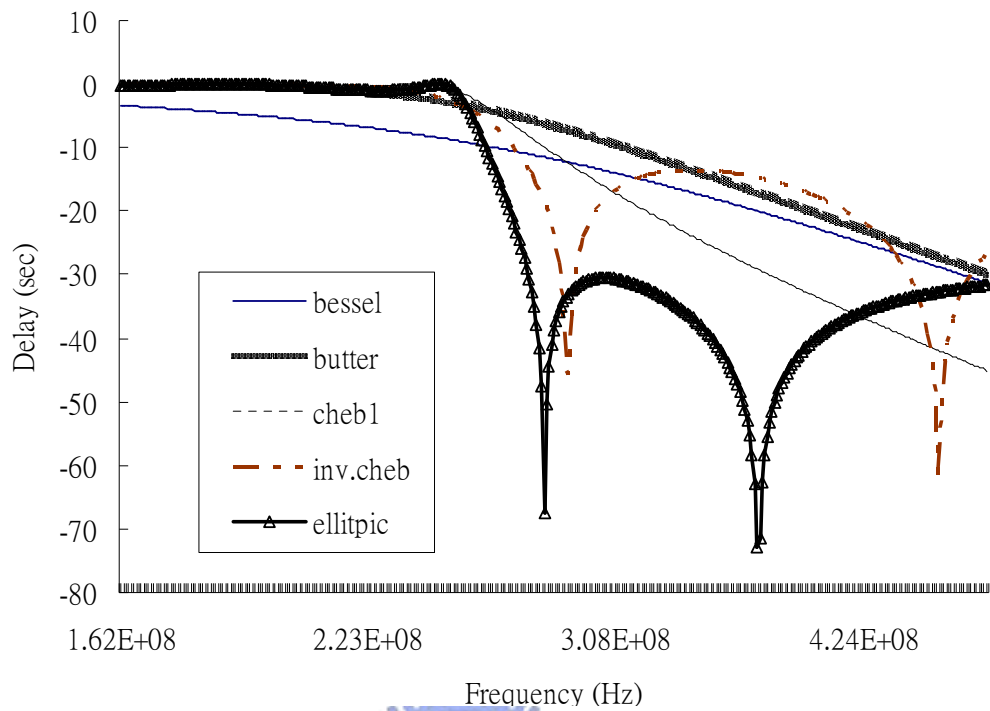
(a)Magnitude
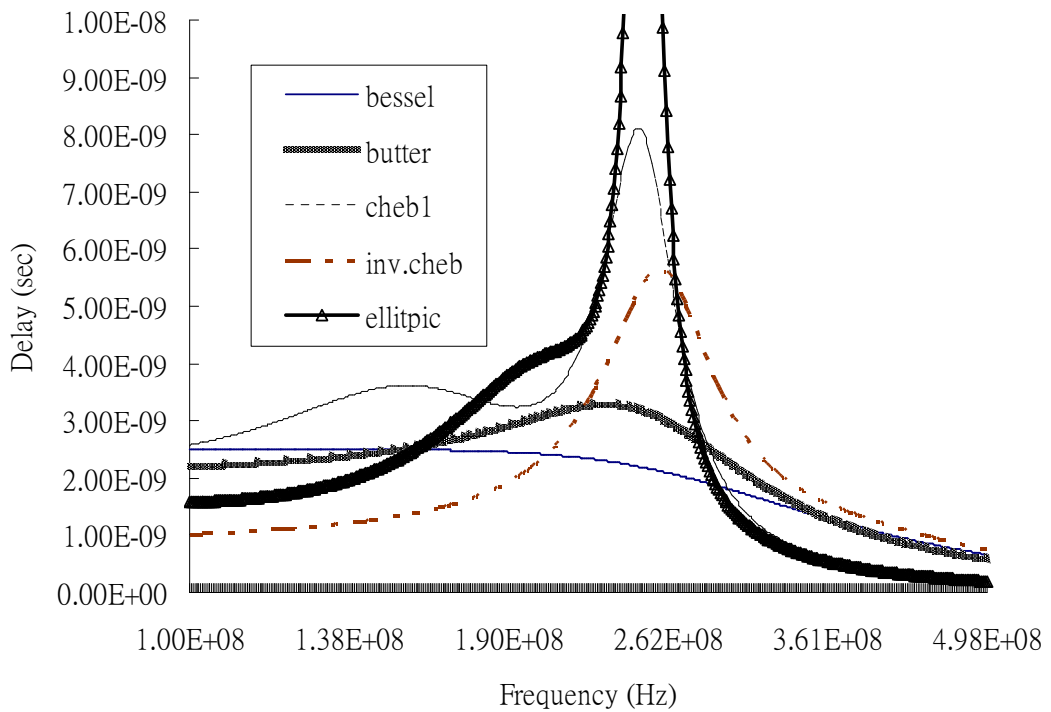
(b)Group delay

Figure 2.1 Comparisons with 5th LPF filter at same cutoff frequency

6

The transfer function of a 5th order elliptic LPF is:

$$H(s) = A \frac{(s^2 + \alpha_0)(s^2 + \alpha_1)}{s^5 + \beta_4 s^4 + \beta_3 s^3 + \beta_2 s^2 + \beta_1 s^1 + \beta_0} \qquad (2.1)$$

The transfer function has four pure imaginary zeros and five complex poles. The sharp

transition band is achieved and can be shortened by the existence of zeros in the stop band.

For very high frequency, the response sustains to reduce by one ahead of numerator:

$$H(s) \to \frac{A}{s} \qquad \text{when } s \to \infty \qquad (2.2)$$

Figure 2.2 shows the frequency response of an ideal 5th order elliptic low-pass filter.

There're five turns (fall-rise-fall-rise-fall) which causes ripples in the pass band. So are the

same turns which offer MAX attenuation in the stop band. ω_o and ω_s are edges of passband

and stopband respectively.
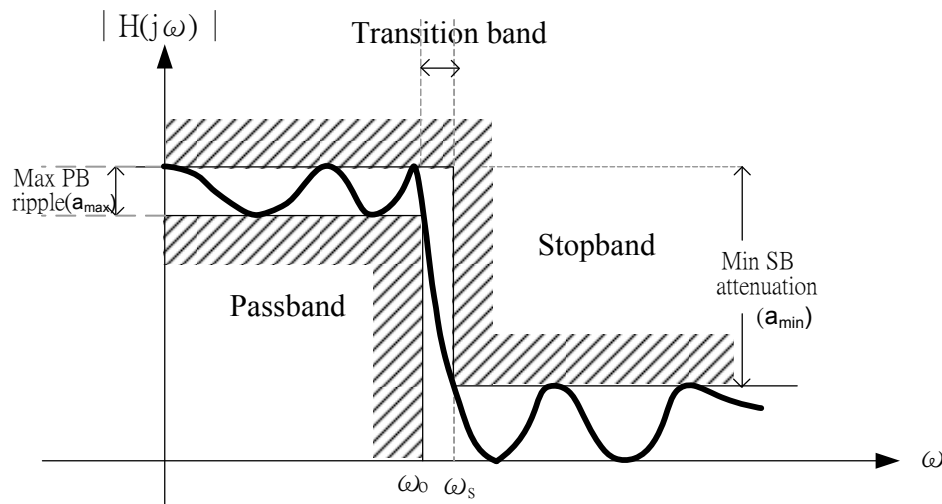
Figure 2.2 Frequency response of an ideal 5th order elliptic low-pass filter
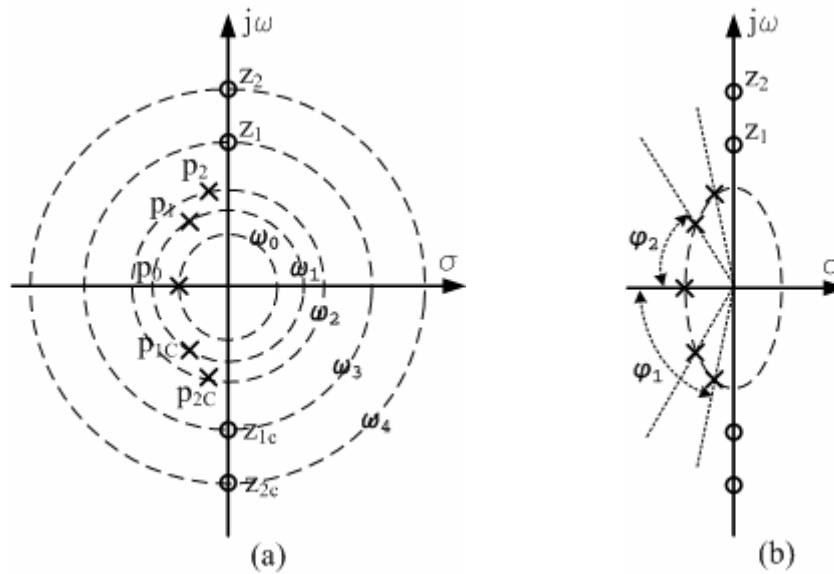
Figure 2.3 Pole-zero plots for a 5th order elliptic low-pass filter

Figure 2.3 shows pole-zero plots for the 5th order elliptic low-pass filter. The poles &

zeros are shown in frequency domain. "Elliptic filter" is called owing to all the poles lie in an

elliptic circle. The frequencies of poles & zeros can be obtained by their radiuses of Figure

2.3 (a). The quality factor of poles & zeros is obtained by the angle from each point to x-axis

in Figure 2.3 (b):

$$\varphi_i = \cos^{-1}(1/2Q) \tag{2.3}$$

The 5th elliptic LPF has zeros with very high Q (infinite in ideal case) locating in high

frequency.

2.2 Elliptic Filter Realization

Several approaches have emerged to implement elliptic filters with different usages and techniques. For simplicity, examples of the 3rd elliptic low pass filters are used in following analysis. Among all the designs, our interests are mainly in the low power design.

2.2.1 Active RC Filter

The active RC filter (using single amplifier biquad) is well-developed and shows in Figure 2.4. In modern technology, accuracy resistance value is not easy to achieve due to process variation. Another problem arising with high frequency is that active RC filters need a high bandwidth amplifier. Moreover, this design uses a large amount of resistors which not only consumes chip area, but also introduces noise.

(a) Positive type   (b) Negative type
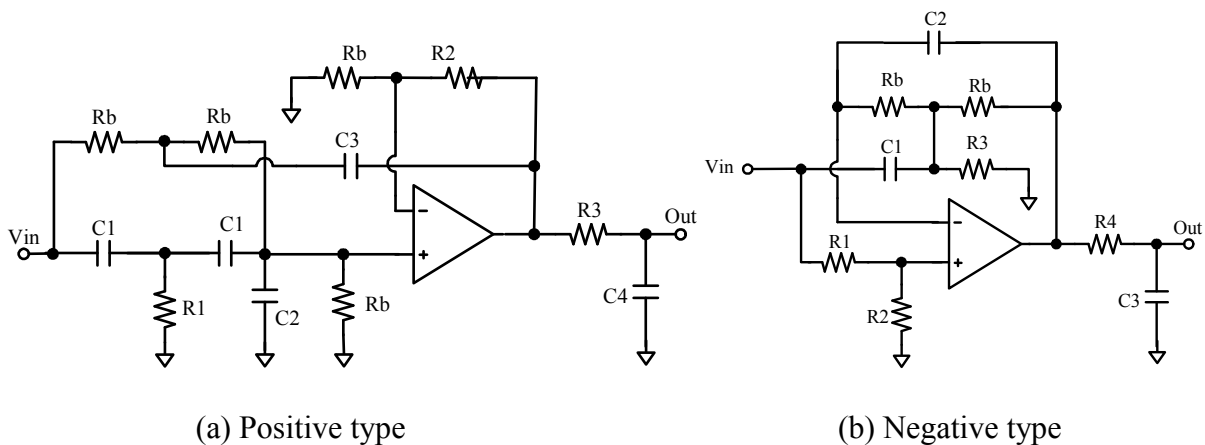
Figure 2.4 3rd order elliptic low-pass filter using SAB (single amplifier biquad)[17]

2.2.2 Switched-Capacitor Filter

In order to eliminate the process variation of resistors, another approach to implement 3rd

elliptic filter uses switched-capacitor (SC) to replace resistors as shown in figure 2.5.

(a) Positive type   (b) Negative type
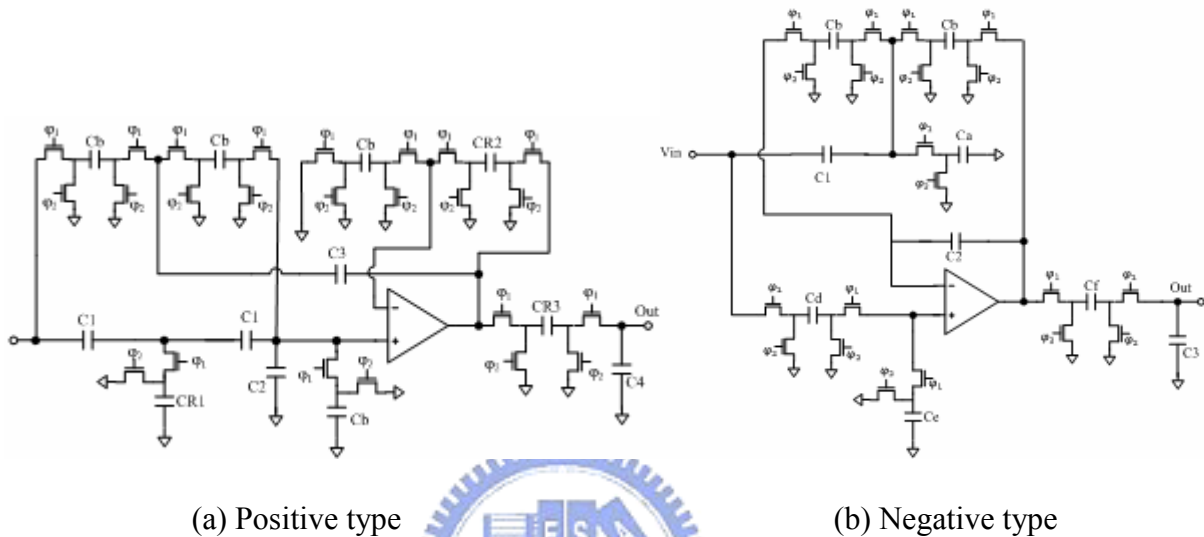
Figure 2.5 3rd order elliptic low-pass filter using Switch Capacitor (SC) filter

The design of SC filters follows fundamentally the active RC methods to obtain cutoff

frequency as mention above but avoids the use of real resistors. It relies on the fact that a

rapidly switched capacitor behaves like a resistor so that RC time constants are determined by

ratios of capacitors and by the clock frequency with which the capacitors are switched.

However, SC filter is not suitable in high frequency application. The main reason is

clock frequency limitation and finite Opamp settling time. A general rule of thumb is that the

clock frequency should be four to eight times higher than the input signal ω_i. The finite

settling time comes from slew rate and finite unity-gain frequency (ω_u) of Opamp. Slew rate

is strongly dependent on the output's step size (non-linear settling time), and our analysis

mainly focuses on finite OPamp unity-gain ω_u (linear settling time) for simplicity. ω_u should

be chosen more than five times of clock frequency, so that the Opamp has enough time to

settle. To avoid unnecessary noise aliasing and power dissipation, however ω_u should be as

small as possible. For this reason, the SC filter is restricted for low frequency applications.

2.2.3 MOSFET-C Filter

Another closely related technique is MOSFET-C filters as shown in figure 2.6.

MOSFET-C filters are similar to fully differential active-RC filters, except resistors are

replaced by equivalent MOS transistors operationg in triode region. The transistors have

smaller process variation than resistors. However, the internal node signal swing could make

transistors leave triode region. And the transistor has parasitic capacitor which should be

considered. In next section, the gm-C filter which does not need Opamp will be introduced.

(a) Positive type   (b) Negative type
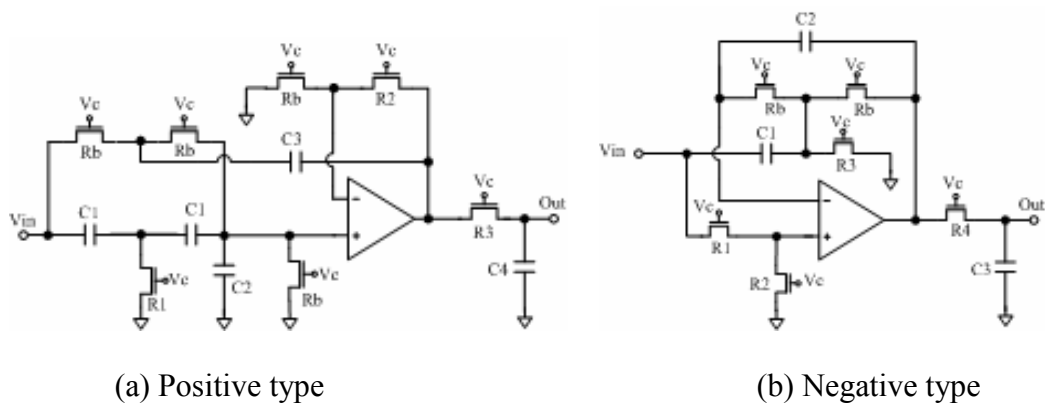
Figure 2.6 3rd order elliptic low-pass filter using MOSFET-C filter

2.2.4 Transconductance-C Filter

The last method extends to applications at hundreds of megahertz by avoiding usage of operational amplifiers and obtaining gain from transconductance amplifiers. The Gm bandwidth can be achieved to tens of GHz and suitable for high frequency filter. Transconductance amplifiers are voltage-controlled current sources (VCCS), $I_o = g_m V_i$. This method uses only Gm and capacitors and is referred to as the Gm-C method. The symbol of ideal operational transconductance amplifier (OTA or Gm) is shown in figure 2.7(a). Fiugure 2.7(b) shows its equivalent small signal circuit. The finite input/output impedance and Gm RHP-zero limitation cause non-ideal effect which will be analyzed in chapter 3. Since Gm is very suitable for HF application, this thesis mainly rivets to Gm filters.
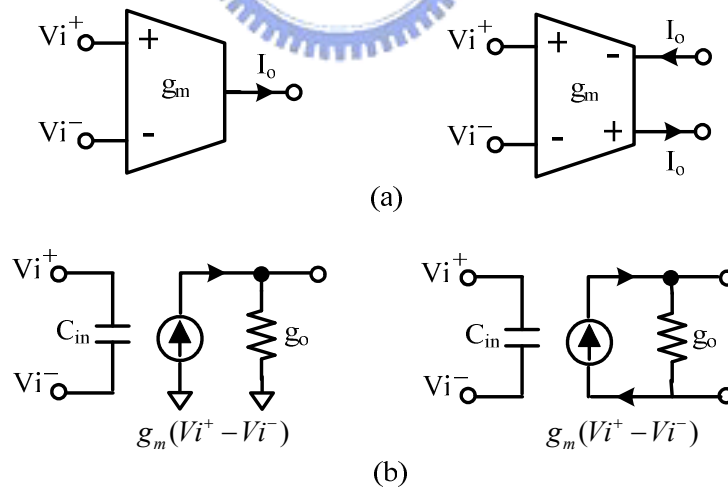
Figure 2.7 Gm. (a) Symbol. (b) Equivalent circuit of ideal OTA
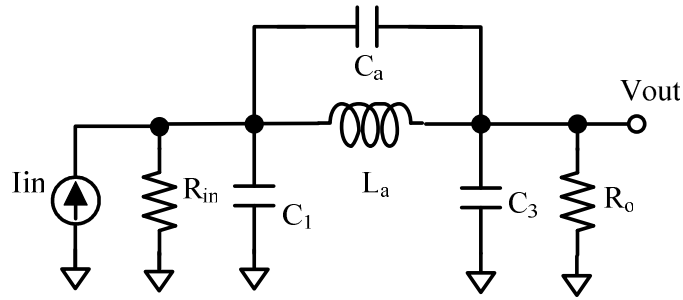
(a) 3rd LC ladder
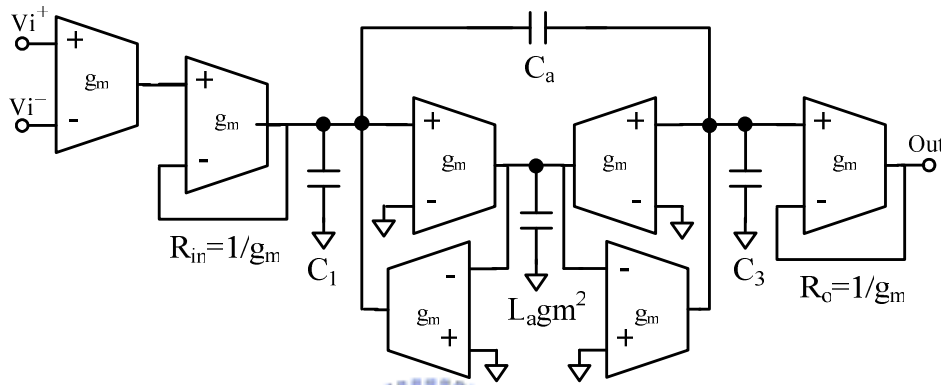
(b) Replace LR by Gm blocks

Figure 2.8 the 3rd order elliptic low-pass filter using Gm-C filter

Figure 2.8 shows different solution by Gm-C filter which comes from LC ladder filter

and replaces all the elements except capacitor to Gm. This filter is very suitable for high

frequency filter and will be analyzed in chapter 4.

There are many synthesis methods to implement Gm filters. But not all methods are

suitable for high frequency applications, since some of them have nodes without desired

capacitance to ground [2]. If a node exits without grounded capacitances to absorb the

parasitic capacitance, there will be deviations in the filter characteristic.

For good CMRR and low even order distortion, the Gm filters should be designed with

differential topology Two synthesis methods are most common used topologies. They are

cascaded biquads and LC-ladder filters. Both of them have complementary properties.

Cascaded biquads are easy to develop but suffers from sensitivity. While LC ladder filter has

very low sensitivity to component variations in the pass band.

The frequency response of a filter is determined by the values of transconductance,

capacitance, and quality factor. To maintain an accurate filter response, precise absolute

values of components are necessary. Absolute values on an integrated circuit can shift

significantly from the nominal due to process parameter variations, temperature and aging. To

maintain a reasonable level of insensitivity of filter characteristics due to parameter shifts, a

system which corrects for these effects is required. Depending on the accuracy of response

desired, many schemes with varying complexities have been proposed and implemented.

Chapter 3

Transconductor analysis and design

Transconductor is the key element in CMOS Gm-C filters. Although Gm has linearity problems, for high frequency application the resistor, inductor, and even VCOs need Gm to be the key elements. In deep-submicron technique, nonlinearity problem gets worse with the reduction of supply voltage. Linearity techniques are therefore, required. Several linearization techniques to achieve better linearity of Gm cells will be investigated in Section 3.1 and the corresponding noise will be compared through spice simulation. The negative impedance method for higher quality factor will also be delivered in Section 3.2. Finally, the proposed symmetric & un-symmetric differential pair with negative impedance will be discussed in section 3.3.

3.1 Linearity analysis of differential pairs

3.1.1 Square-law I-V relation

When MOS device is operating in saturation regions, it follows the square-law relation between drain current I_d and gate voltage V_{gs}:

$$I_d = K(V_{gs} - V_t)^2 (1 + \lambda|V_{ds}|) \quad \text{where } K = \frac{1}{2}\mu_0 C_{ox} \frac{W}{L} \tag{3.1}$$

The channel length modulation term $(1 + \lambda|V_{ds}|)$ will cause an equivalent output

impedance r_o of MOS device.
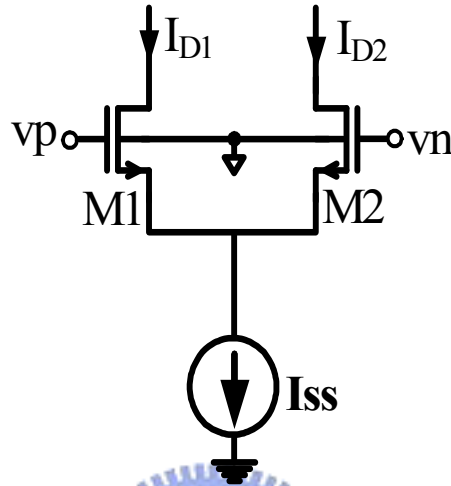
Figure 3.1 A source coupled differential pair.

Figure 3.1 shows a simple source coupled differential pair. I_{SS} is a high impedance

current source which provides good CMRR. If M1 & M2 are both matched, then the

differential output current $I_{out} = I_{D1} - I_{D2}$ is given by [9]:

$$I_{out} = 2K(V_{gs} - V_t)(vp - vn) \tag{3.2}$$

Where V_{gs} is common-mode gate-source voltage, ideally the value is constant. But

actually the source of M1 & M2 is not perfectly virtual ground. When $V_{id} = (vp-vn)$ is large, a

square term, V_{id}^2 becomes significant in $I_{D1} + I_{D2}$:

$$I_{ss} = I_{D1} + I_{D2} = K[2(V_{gs} - V_t)^2 + \frac{V_{id}^2}{2}] \tag{3.3}$$

Because of the fixed current source I_{ss}, the V_{gs} may change with V_{id}. The complete

expression of I_{out} is obtained as below:

$$I_{out} = \begin{cases} \dfrac{1}{2}V_{id}\sqrt{2I_{ss}K}\sqrt{1-\dfrac{V_{id}{}^2K}{2I_{ss}}} & \text{when } |V_{id}| \leq \sqrt{\dfrac{I_{ss}}{K}} \\ \\ I_{ss}\,\text{sgn}(V_{id}) & \text{when } |V_{id}| \geq \sqrt{\dfrac{I_{ss}}{K}} \end{cases} \qquad (3.4)$$

The transconductance value can be estimated by (3.4) and used Taylor expansion to

analyze:

$$g_m = \frac{\partial I_{out}}{\partial V_{id}} = \frac{\dfrac{1}{2}\sqrt{2I_{ss}K}(1-\dfrac{V_{id}{}^2K}{I_{ss}})}{\sqrt{1-\dfrac{V_{id}{}^2K}{2I_{ss}}}} = \frac{1}{2}(\sqrt{2I_{ss}K} - \frac{3}{2\sqrt{2}}\frac{K^{\frac{3}{2}}}{\sqrt{I_{ss}}}V_{id}{}^2 - ....) \qquad (3.5)$$

From (3.5) gm reduces with the increase of V_{id}. And gm has a small signal

approximation value of $\dfrac{1}{2}\sqrt{2I_{ss}K}$, when V_{id} is small.

3.1.2 Body effect

The sources of M1& M2 of the differential pair have a voltage difference V_{SB} with respect to the substrate in CMOS process. So the V_t of each transistor has to be modified as [9]:

$$V_T = V_{T0} + \gamma[\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}] = V_{FB} + 2\phi F + \gamma\sqrt{V_{SB} + 2\phi_F} \quad (3.6)$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_{SUB}}}{C_{ox}} \quad (3.7)$$

Where *Nsub* is the doping concentration, ε_{si} is the silicon dielectric constant, *q* is electron charge, V_{FB} is the flat-band voltage, ϕF is the difference between the Fermi level and the intrinsic level and V_{TO} is the original threshold voltage without body effect.

From the I-V relationship of (3.3), the body effect is considered and the V_{SB} varies with Vid. Then the non-linear characteristic of a differential pair is no longer a simple square-law relation. This could affect the linearization techniques such as active biasing or unbalanced gm cell that will be introduced later. For small signal amplitudes smaller than 100 mV, the simple I-V relationship can still hold. Therefore, the linearization techniques using compensation of non-linearity can only work for a limited range.

3.1.3 Mobility degradation from vertical field

The mobility degradation of transistors worsens the complexity of the non-linearity problem. A vertical field originating from the gate voltage exists and influences carrier velocity. In deep submicron technology the increasing vertical electric field forces the carriers in the channel closer to the surface of the silicon. The defected surface will reduce the carriers' movement. With the effect of mobility degradation, the drain current is modified as follows:

$$I_D = \frac{1}{2}\mu_{eff}C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 = \frac{1}{2}(\frac{\mu_0}{1+\theta(V_{gs} - V_t)})C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 \qquad (3.8)$$

where θ is the mobility degradation constant.

This is especially significant for short channel devices, because the gate oxide layer is very thin. Thinner gate oxide means a stronger vertical field. In order to keep the same V_t, higher doping of the substrate is implemented, which will reduce the channel effective "thickness" and therefore further degrades carrier mobility.

I_{ss} can be modified with mobility degradation as:

$$I_{ss} = I_{D1} + I_{D2} = K\frac{2(V_{gs} - V_t)^2 + \frac{V_{id}^2}{2} + \theta(V_{gs} - V_t)[2(V_{gs} - V_t)^2 + \frac{V_{id}^2}{2} - \theta(\frac{V_{id}}{2})^2]}{[1+\theta(V_{gs} - V_t)]^2 - \theta^2(\frac{V_{id}}{2})^2} \qquad (3.9)$$

The V_{gs} is a function of V_{id}. When taking mobility degradation into consideration, the mobilities between M1 and M2 in the differential pair have large difference with larger V_{id}.

The effect of mobility degradation can be alleviated by choosing processes with longer

channel devices, which have thicker oxide and therefore smaller vertical field. However the long channel device has large parasitic capacitance and doesn't achieve high frequency application. Another solution is to bias the transistors at a higher V_{gs}-V_t to gets maller percentage variation of mobility.

3.1.4 Short channel effect

For short channel devices, the electric field between source and drain can reach the field strength E_{sat} at which the velocity of the channel carriers saturates. At high fields, the carrier velocities approach the thermal velocities, and decreases with the increase of electric field. The modified expression of I_D with the pinch-off phenomenon is given as:

$$I_D = WC_{ox}(V_{gs} - V_t - V_{dsat})v_{sat} \tag{3.10}$$

In (3.10) V_{dsat} is the V_{ds} when the channel carriers achieve saturation velocity V_{sat} and is given as:

$$V_{dsat} = \frac{2\mu_{eff}L(V_{gs} - V_t)}{2\mu_{eff}L + V_{gs} - V_t} \tag{3.11}$$

where μ_{eff} is the effective mobility.

In long channel device (3.10) can be simplified to be (3.1). In deep submicron devices, the order of $(V_{gs}$-$V_t)$ in (3.1) is less than 2. This does not mean that the device is more linear, since the perfect linear relationship occurs at L=0..Furthermore, the V_{dsat} varies with V_{gs}-V_t., which makes accurate linearization very complicated.

The hot electron effects and drain-induced barrier lowering (DIBL) are also short

channel effects. Detailed analysis will be out of the scope of this thesis and thus not provided

here.

3.2 Noise analysis of a differential pair
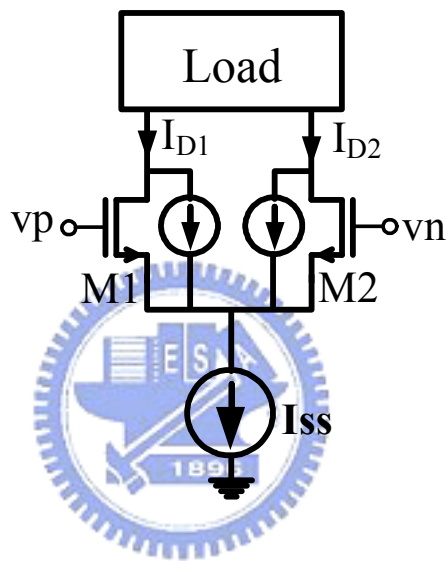
Figure3.2 The noise source of a differential pair

In Figure 3.2 the R_{out}, C_{out} and G_m of M1 and M2 are the same in this calculation. For long

channel devices, the output noise V_{n2} of each g_m cell can be expressed as [9]:

$$V_n^2 = 2\gamma \times [\frac{8}{3} KTBg_m R_{out}^2] \tag{3.12}$$

The noise power is doubled, because there are 2 branches. Note that the constant γ is 1

for long channel devices and with noiseless loading. However, the output loading has its own

noise. If short channel effects, such as hot electron effect of the long channel counterpart, are

taken into account, the value of γ can be 1 to 4 times larger than the original value

3.3 Linearization Techniques for gm cells

There are many techniques implemented to reduce the variation of g_m of differential pairs with the high swing V_{id}. In the subsection, the source degeneration [10] [11], active biasing [12], cross coupling [13], unbalanced differential pair [14], and symmetric & un-symmetric differential [5] pair will be introduced respectively.

3.3.1 Source degeneration

(a) Source degeneration   (b) Saturated transistor
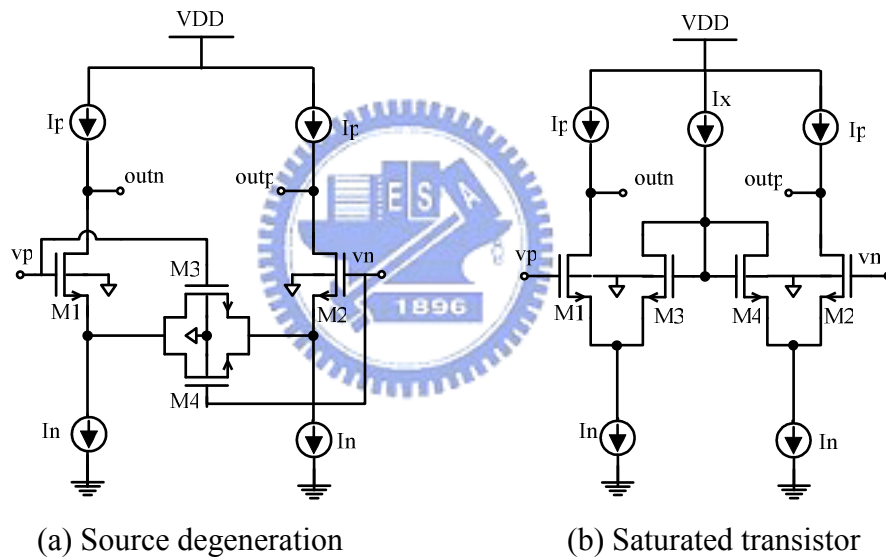
Figure3.3 Source degeneration technique

In Figure3.3 (a), the degeneration resistance can be changed dynamically with the input signal amplitude. Qualitatively, when the amplitude of the input signal rises, the triode-mode degeneration MOS resistors will be more biased to reduce the synthesized resistance and provide less degeneration. The g_m reduction from larger input signal is therefore compensated by the degeneration resistance adjustment. The transconductance relationship is expressed as follows [10]:

$$g_m = \frac{g_{m1}}{1 + (K_1 / 4K_3)} \qquad (3.13)$$

where K is $0.5\mu_n CoxW/L$

The other technique using saturated transistor as degeneration resistor shown in Figure

3.3(b), the equivalent g_m is [11]:

$$g_m = \frac{g_{m1}}{1 + g_{m1} / g_{m2}} \qquad (3.14)$$

The rise of g_m then compensates for the drop of g_m expressed in Eq. (3.5). However, the

compensation is not adaptive. Therefore it is suitable when the range of tolerance of g_m is

relatively large.

3.3.2 Active biasing

(a)   (b)
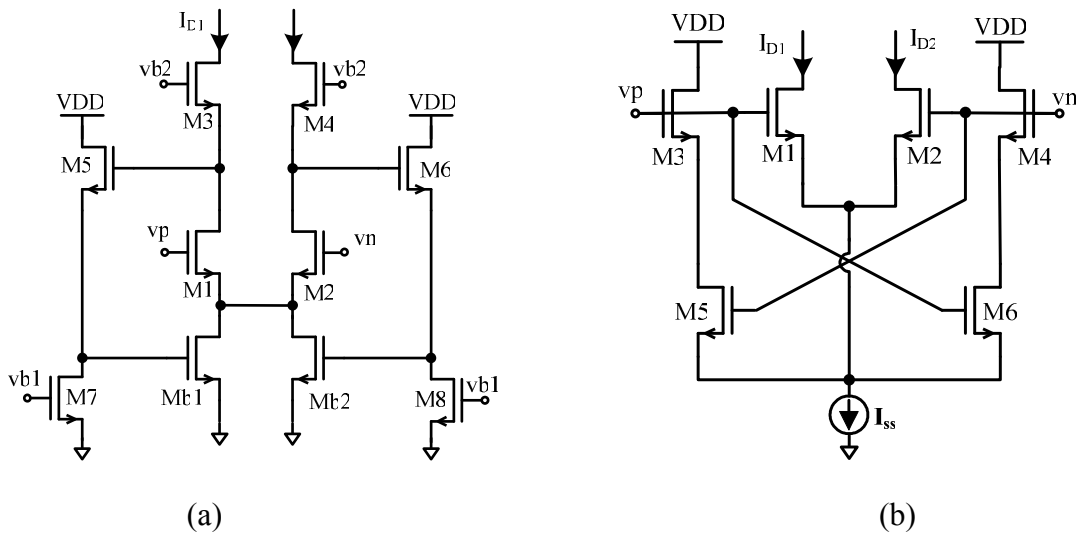
Figure3.4 Adaptive bias degeneration[12]

From (3.4) & (3.5), the nonlinear characteristic of differential pairs is observed to come

from the expression $\sqrt{1 - \frac{V_{id}^2 K}{2I_{ss}}}$. This term can be cancelled by canceling the V_{id} term in the

expression. The method is to make the biasing current compensation for the non-linear term:

$$I_{ss} = I_{DC} + K\frac{V_{id}^2}{2}$$ (3.15)

where I_{DC} is the DC bias current.

Now the bias I_{ss} supplies I_{DC} when $V_{id} = 0$ for the static bias. When there is a signal, an

additional bias current $KV_{id}^2/2$ will compensate for the drop of the g_m. This can be verified by

inserting the new I_{ss} into Eq. (3.3):

$$I_{D1} + I_{D2} = 2K(V_{gs} - V_t)^2 = I_{DC}$$ (3.16)

As a result, a constant g_m is obtained because V_{gs}-V_t of each input transistor is constant.

One of the designs is shown in Fig. 3.4(a).

In this design, all transistors are matched except M_5-M_8. For this cascoded circuit, when

there is an input signal, the same amplitude appears at the drains of M_1 and M_2 because the

loading is $1/g_{m3,4}$ and $g_{m3,4} = g_{m1,2}$. Here, $r_{o1,2} \gg 1/g_{m1,2}$ is assumed and the capacitance at that

node and the loss of the level shifter M_5-M_8 are ignored. Both gates of M_{b1} and M_{b2} sense the

differential voltage. Because the drains of M_{b1} and M_{b2} are connected together, a bias current is

obtained as in (3.2) and (3.15). The required active biasing is then established.

When the g_m cell is used for high frequency applications, say 250 MHz, the capacitance

effect at the drains of M_1 and M_2 and the sources of M_5 and M_6 will reduce the effective signal

voltage sensed by M_{b1} and M_{b2}. Therefore, the actual size of $M_{3,4}$ is smaller than that of $M_{1,2}$ to

increase the voltage gain of M_1 and M_2. This ensures that the $KV_{id}{}^2/2$ is enough to compensate

for the non-linearity.

The same linearization effect can be achieved by connecting the gates of M_{b1} and M_{b2} to

the 2 inputs respectively. But in the common-mode sense, now the conductance of M_{b1} and

M_{b2} increases in phase with the input signal. This is a kind of feed-forward and thus causes a

boost-up of the common-mode gain. As a result, CMRR drops and common-mode instability

will be resulted.

There is a modified design that can operate at a lower supply voltage. The schematic is

shown in Fig. 3.4(b). Instead of controlling the gate bias of the bias transistor M_b, a differential

pair M_3-M_6 acts as a bias current. Both pairs share the same bias current source.

When the signal amplitude is small, M_3 and M_4 are in saturation region while M_5 and M_6

are in triode region. M_3-M_6 drain out some of the bias current. When the signal amplitude is

positive and large, M_6 will go into saturation region and M_5 will be cut off. Smaller sum of the

bias current will be drained out by M_3-M_6. That means more current will be supplied to M_1

and M_2 to compensate for the drop of g_m. As a result, an active biasing is achieved.

3.3.3 Cross-coupling
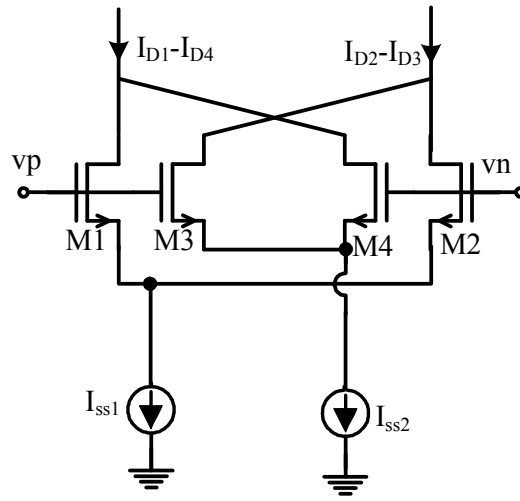
Figure3.5 Cross-coupling gm cell

A simple differential pair can cancel out the even order harmonics of distortion of I_o. The remaining odd order harmonics can be cancelled out by cross coupling 2 differential pairs with the same distortion but with different g_m values. The circuit is shown in Figure 3.5.

The 3rd order harmonic is the main concern since it is now the most significant distortion. From Eq. (3.5), the 3rd order harmonic distortion (HD3) of I_o can be obtained as:

$$HD_3 = \frac{K^{\frac{3}{2}}}{2\sqrt{2I_{ss}}} V_{id}^{\ 3} \qquad (3.17)$$

Since HD3 depends on the ratio of $K^{3/2}$ and $I_{ss}^{1/2}$ only, the distortion can be cancelled by connecting 2 differential pairs in parallel with different g_m but with the same distortion. $K_{3,4}$ and $K_{1,2}$ are related to I_{ss2} and I_{ss1} as follows:

$$\left(\frac{K_{3,4}}{K_{1,2}}\right)^3 = \frac{I_{ss2}}{I_{ss1}} \tag{3.18}$$

The corresponding effective g_m is then given by:

$$g_{meff} = g_{m1,2}\left[1 - \left(\frac{K_{3,4}}{K_{1,2}}\right)^2\right] = g_{m1.2}\left[1 - \left(\frac{I_{ss2}}{I_{ss1}}\right)^{\frac{2}{3}}\right] \tag{3.19}$$

But the non-linearity cancellation is not complete due to the difference in second order

parameters such as the mobility between the 2 differential pairs. The incomplete cancellation

is more significant when $I_{ss2} \ll I_{ss1}$ though more extra power consumption due to I_{ss2} is saved.

The perfect cancellation happens when I_{ss2} approaches I_{ss1}. Yet the resultant g_m also tends to

zero. There is also a problem of the smaller CMRR. The reason is that the differential gain is

reduced by M_3 and M_4 whereas the common-mode gain is enhanced. This can be a serious

problem for the common-mode stability if the g_m cell is used to construct gyrators for G_m-C

low pass filters. Another disadvantage is the additional noise of M_3 and M_4. The factor of the

noise to a simple differential pair is $\left[1 - \left(\frac{I_{ss2}}{I_{ss1}}\right)^{\frac{2}{3}}\right]$. But it is suitable when a very small and

linear g_m is required because the g_m is obtained from the cancellation of 2 relatively large g_m's.

3.3.4 Unbalance differential pairs
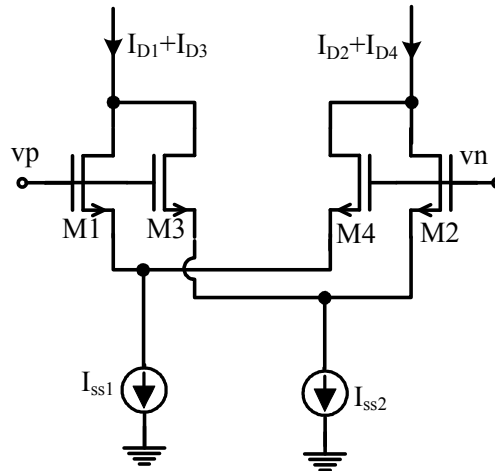
Figure3.6 Unbalance differential pairs

Two differential pairs with a symmetrical but opposite-signed input offset voltage can compensate for the drop of the g_m of each other so that a flat g_m can be obtained at a certain offset. The schematic and the basic operation principle are shown respectively in Figure 3.6

In the schematic, $K_1 = K_2$ and $K_3 = K_4$. The differential pairs $M_{1,4}$ and $M_{2,3}$ have symmetrical offset voltage because the sizes of the transistors are different in each differential pair. To find the offset voltage, the point where $I_{d1} = I_{d4}$ and $I_{d2} = I_{d3}$ has to be found:

$$I_{d1,2} = I_{d3,4} \Rightarrow K_{1,2}(V_{gs} - V_t - V_{offset})^2 = K_{3,4}(V_{gs} - V_t + V_{offset})^2$$

$$\Rightarrow V_{offset} = \frac{\sqrt{K_{1,2}} - \sqrt{K_{3,4}}}{\sqrt{K_{1,2}} + \sqrt{K_{3,4}}}(V_{gs} - V_t) \qquad (3.20)$$

If the non-linear g_m expression of (3.5) is included, the compensation is not complete due to the squared term:

$$g_{meff} = g_{m1,2} + g_{m3,4} = \frac{1}{2}\sqrt{2I_{ss}K}[\frac{(1-\frac{(V_{off}-V_{id})^2 K}{I_{ss}})}{\sqrt{1-\frac{(V_{off}-V_{id})^2 K}{2I_{ss}}}} + \frac{(1-\frac{(V_{off}+V_{id})^2 K}{I_{ss}})}{\sqrt{1-\frac{(V_{off}+V_{id})^2 K}{2I_{ss}}}}] \quad (3.21)$$

3.3.5 Symmetric and un-symmetric differential pairs
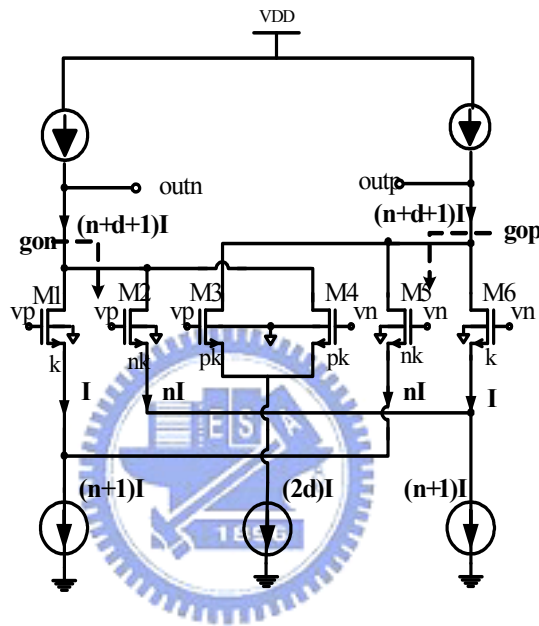
Figure3.7 Symmetric & un-symmetric pairs

The linearity technique can combine two skills in order to further improver its linearity. If we use cross-coupling and unbalance differential pairs together, then the gm core is called "Symmetric & Un-symmetric differential pairs" [5].

Figure.3.7 shows the proposed Gm by using symmetrical & unsymmetrical differential pair with negative impedance. NMOS M_5&M_1, M_2&M_6 have unsymmetrical aspect ratio n, and symmetrical pair M_3&M_4 makes gm as flat as possible. The transistors and current have different ratios:

$$M1:M2:M3=M6:M5:M4=1:n:p \qquad (3.22)$$

The detail analysis of this gm core can be seen in Appendix A.

The gm can be obtained [5]:

$$gmd = \frac{4n}{(n+1)} \frac{n-1}{\sqrt{n(n+1)}} \sqrt{\frac{I}{k}} \qquad (3.23)$$

where n is aspect ratio , I is normalized current, and $k = \frac{1}{2} \mu Cox \frac{W}{L}$.

By choosing appropriate transistor ratio n, p, and d, the range of flat gm:

$$vid \le \left| \frac{(n+1)}{n} \sqrt{\frac{I}{k}} \right| \qquad (3.24)$$

Above linearity technique can be summarized as Table 3.1 and the advantage and disadvantage of gm cells will list in it [15]:

Linearization types	Advantages	Disadvantages
Degeneration of Figure 3.3(a)	1.Simple and Fast 2.Low sensitive to common mode input signals	1.Linear range is limited to $Vin<V_{DSAT}$ 2.Not effective
Degeneration of Figure 3.3(b)	1.Wider linear range than (a) 2.Low sensitive to common mode input signals	1.More silicon area 2.Low power efficiency
Adaptive Bias	1.Small g_m variation over a wide range	1.Need good matching for biasing transistors
Cross Coupling	1.Better power efficiency than source degeneration. 2.Small g_m variation over a wide range	1.The transconductance is very small
Unbalance differential pair	1.Good power efficiency 2.Good CMRR	1. Small g_m variation for a limited range only.
Symmetric & Un-symmetric differential pair	1.Suitable for high frequency 2.Highly linear Gm	Symmetric pair wastes power

Table 3-1 Table of comparisons of various g_m cells
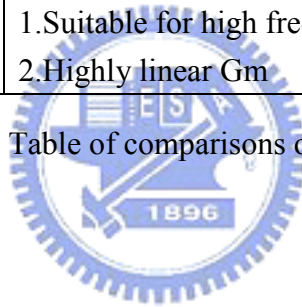
3.4 High Output Impedance Techniques for gm cells

To improve the gyrator quality factor, the gm integrator must have high DC gain with desired gm value. That is, the gm needs high output impedance. There are two techniques implemented to increase that. First technique is to cascade high R_{out} element [5]. And second one is to use negative impdeace load (NRL)[3].

3.4.1 Cascade High Rout Element
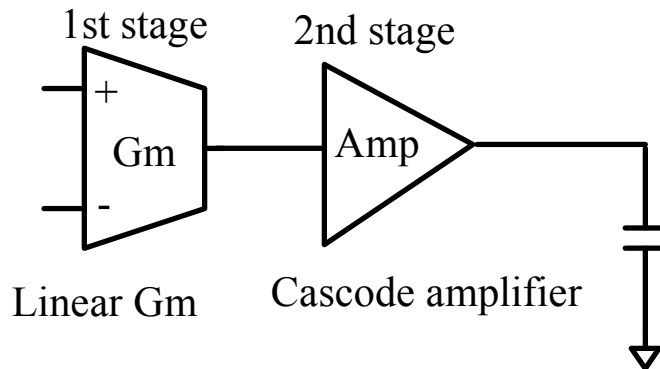
Figure 3.8 Cascoded 2nd stage to improve Rout

The high gm output impedance need cascoded MOS structure as gm load. For some linearity technique needs more voltage headroom, it is not suitable in deep sub-micron era. Some papers "separate linearity and high Rout" as shown in Figure 3.8. Although it can release the problem, the 2nd stage amplifier needs addition power and cascade reduces output swing so it's not a good solution. The best solution requires only one linear gm and has high differential gm & low common mode gain. It will be shown in next section.

3.4.2 Negative Impedance Load (NRL)
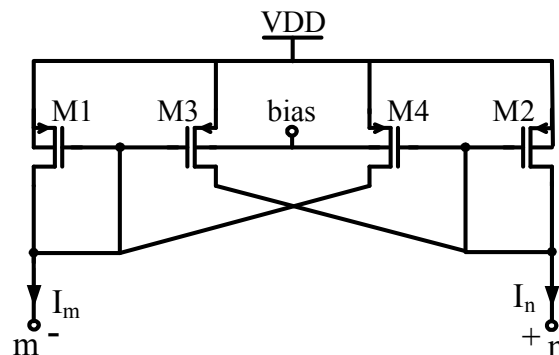
Figure3.9 Negative Impedance Load

Consider the NRL in Figure 3.9. M3 & M4 introduce local positive feedback between the output terminals m & n which generate a negative resistance to compensate the parasitic output resistance of the whole transconductance circuit. A bias voltage connects to the substrate of M3 & M4 in order to control the threshold voltage. This is a simple way to control the NRL without generating extra internal node. The voltage of bias has to be carefully limited in several hundreds milli-volts in order to prevent from latch-up.

Applying again the square-law characteristic for devices M1-M4 and (3.6), the current I_m & I_n and their difference $I_m - I_n$ are derived as:

$$I_m = I_0 + \frac{I_R}{2} = k_p \left(\left| V_{gs1} \right| - \left| V_{tp} \right| \right)^2 + k_p \left(\left| V_{gs2} \right| - \left| V_{tpx} \right| \right)^2$$

$$I_n = I_0 - \frac{I_R}{2} = k_p \left(\left| V_{gs2} \right| - \left| V_{tp} \right| \right)^2 + k_p \left(\left| V_{gs1} \right| - \left| V_{tpx} \right| \right)^2$$

$$V_{tpx} = V_{tp} + \gamma [\sqrt{V_{dd-bias} 2\phi_F} - \sqrt{2\phi_F}]$$

$$I_R = I_m - I_n = 2k_p V_{out} \gamma [\sqrt{V_{dd-bias} 2\phi_F} - \sqrt{2\phi_F}] \tag{3.25}$$

Where I_R is the differential current through the active load, $V_{out} = V_n - V_m = V_{gs2} - V_{gs1}$ is the differential output voltage, and $k_p = 0.5\mu_p C_{ox} W/L$ is the transconductance parameter.

The negative impedance is:

$$R_{NRL} = \frac{V_{out}}{-I_R} = \frac{1}{2k_p \gamma [-\sqrt{V_{dd-bias} 2\phi_F} + \sqrt{2\phi_F}]} \tag{3.26}$$

The negative impedance load can be combined with all the differential gm to increasing their output impedance as shown in Figure 3.10. In (a) the output impedance is 1/(go1+go2). If the NRL is used in (b) and design go3 = - go4, then the output impedance is infinite

(ideally). The advantage of NRL is that it only needs to bias at same current string, so it saves power.

(a) without NRL   (b) with NRL
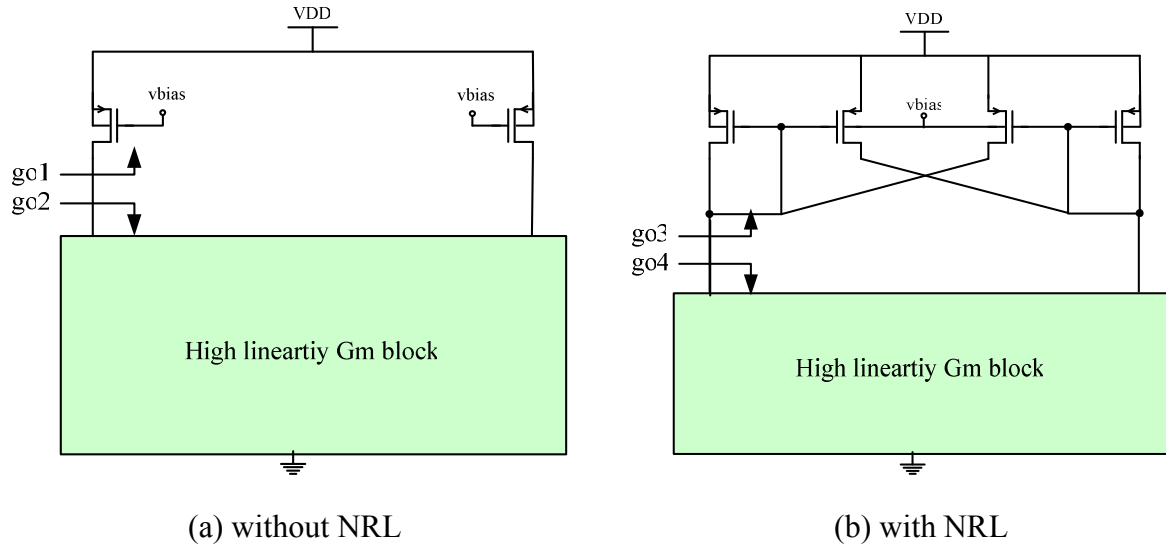
Figure3.10 Gm core with/without NRL

3.5 Symmetric & un-symmetric pairs with NRL

HF filter needs poles & zeros at higher frequency. So there has some trade-off between gm and capacitance. Because poles and gm-divide-C have direct proportion, gm value can design at a small value while capacitance also is small to maintain original pole vale. But small capacitance value means worse process variation. If we choose higher gm value, the power dissipation can not match stringent specification for UWB system.

Several high frequency CMOS Gm-C filters are introduced inverter type gm to achieve minimum node and implemented negative impedance. Nevertheless the linearity is limited due to the topology and negative impedance costs lots of power [2]. A novel circuit skill saves

power by connecting negative impedance in parallel with the output nodes of the basic Gm [3].

Because of avoiding the use of stacked devices, the Gm proposed in [4] is very suitable in low

supply voltage. But in deep submicron technology, there still needs high linearity skill to fix

serious linearity problems. In this thesis, a symmetrical & un- symmetrical differential pair

with negative impedance is introduced and a high frequency low power elliptic filter for

UWB applications can be achieved.
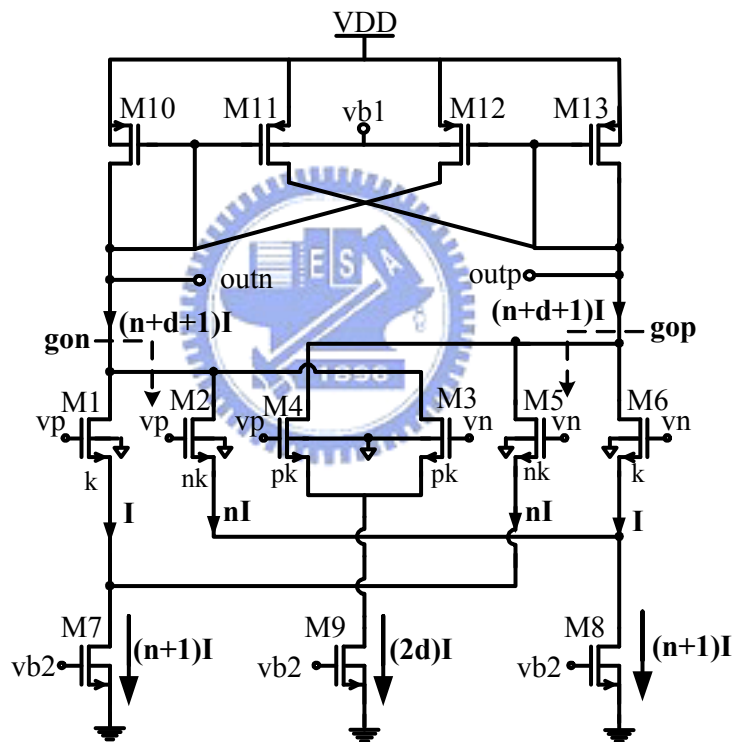
Figure3.11 Symmetric & un-symmetric with NRL

The symmetric & un-symmetric differential pair with NRL is shown in Figure 3.11.

PMOS M_{11}&M_{12} work as negative impedance load. The output impedance can be controlled

by tuning body potential vb1 of M_{11}&M_{12}.

The Gm differential and common mode gain can be shown [4]:

$$Adm = -\frac{gmd}{go' - \Delta gm} \quad , \quad Acm = \left| -\frac{gmd}{go' + \Sigma gm} \right| \tag{3.27}$$

Where gmd can be found in (3.23), $\Delta gm = gm_{12} - gm_{10}$, $\Sigma gm = gm_{12} + gm_{10}$

$$go' = gds_{10} + gds_{12} + gon, \quad gon = 1/\sum[ro_{1,2,3} + (1 + gm_{1,2,3}ro_{1,2,3})(ro_{7,8,9} + \frac{1}{gm_{5,6,4}})]$$

Equation (3.27) shows that when $go' \rightarrow \Delta gm$, the Adm will be infinite. In practice, Adm is

limited due to mismatch and process variation. And let $gmd < go' + \Sigma gm$ to make Acm <1 to

get superior CMRR. A stand-alone integrator could become unstable due to the

right-half-plane zero. Even so, a gyrator based filter built with Gm blocks will remain stable.

This is owing to the feedback loops inherent to a filter constructed with gyrators. It will be

analyzed in chapter 4 and the result shows that the RHP zero doesn't matter if negative

impedance is not too "negative".
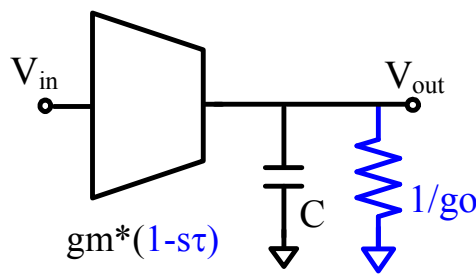
Figure3.12 non-ideal Gm-C integrator

The Gm and capacitor can be connected as integrator, for integrator is the basic

element in all the filters. If the Gm non-ideal effect like finite RHP-zero and finite output

impedance is considered as shown in Figure 3.12, than the magnitude and phase response is

Figure 3.13. The frequency with phase at -45° is the f_{3db} for integrator and -135° is Gm

RHP-zero, respectively. The -90° phase shift region is between two frequencies.

(a) — Magnitude response

(b) — Phase response
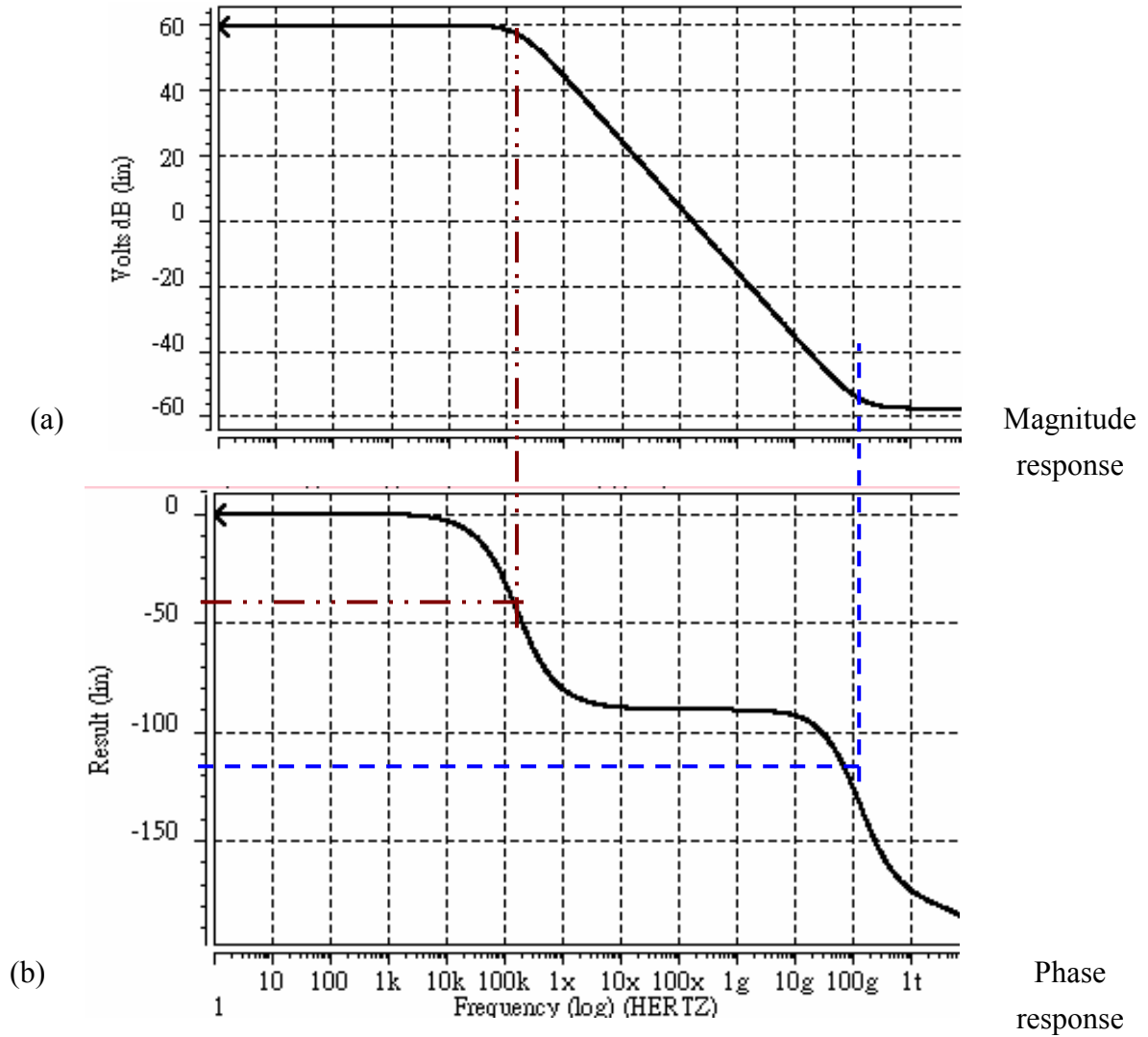
Figure 3.13 Frequency of non-ideal Gm-C integrator

The Quality factor for the integrator is shown in (3.28)

$$Q_{int}(\omega) = \tan(-\arg(H_{int}(j\omega)))$$

(3.28)

From (3.27) and (3.28), the expression for quality factor of the proposed symmetric &

un- symmetric Gm integrator is:

$$\frac{1}{Q_{\text{int}}(\omega)} = \frac{\omega_T}{\omega \cdot g_{md}}(go' - \Delta gm) - \omega \cdot \tau_{gm} \qquad (3.29)$$

where ω_T is Gm integrator unit-gain frequency, and τ_{gm} is the Gm RHP-zero. For 250MHz

filter, the $1/\tau_{gm}$ will be far in 25GHz in order to have acceptable quality factor. This limits

the linearity topology. The principle for Gm integrator can be applied to Gm-C filter.

Chapter 4

Filter Analysis & Implementation

The filter topology will be analyzed in this chapter. Some topologies exhibit excellent performance and are suitable for high frequenccy. The topology of passive elliptic LC ladder filter is introduced in Section 4.1. Section 4.2 shows the element replacement to implement high frequency filter in CMOS process. The sensitivity property will be in Section 4.3.

4.1 LC ladder filter

(a)   (b)
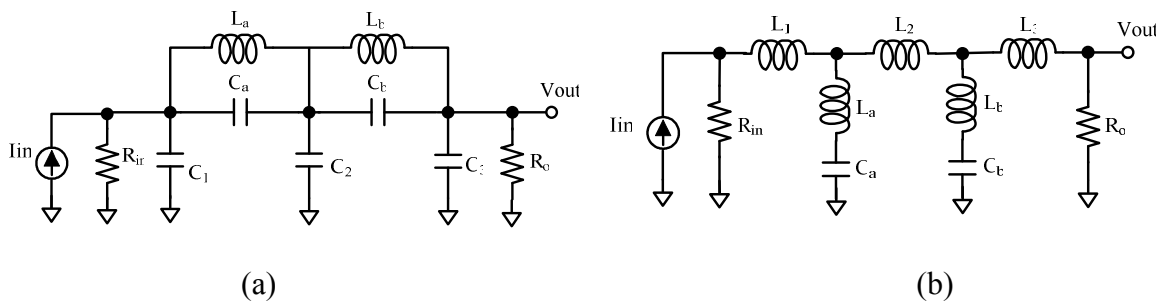
Figure 4.1 the 5th elliptic LC ladder

There are two possible topologies to implement the 5th order elliptic filter by LC ladder structure. The zeros are generated by the LC tanks at their resonant frequencies. One LC tank generates two complementary zeros. The parallel LC tank forms an "open circuit" which cuts

off the input-output path at the tank's resonant frequency. On the other hand, the serial LC

tank forms a "short circuit" at resonant frequency (zeros) as shown in Figure 4.1. The parallel

LC tank topology is preferred owing to less inductor, therefore less gyrators are used. There

are four Gms for a gyrator, so Figure 4.1(b) is power wasting topology. Moreover, serial LC

tank topology does not have desired capacitance to ground in all the nodes and will distort

frequency response. If the LC tank is lossless, there will be a very high Q zero. In the CMOS

process, the on-chip inductors have serious parasitic effect and the resistance variation is

serious. The LC ladder can't be implemented by simply putting some RLC components,

especially when the circuit is used for high frequency application. The LC ladder filter has

good sensitivity property. In previous chapter, the transconductor is introduced in the form of

inductors or resistances. The detail transfer function of 5th elliptic LC ladder filter is analyzed

in Appendix A.

4.2 LC Gm-C filter

As mentioned above, the variation of on-chip resistors is critical. And passive inductor

has parasitic resistance which can't achieve a high Q and high frequency zeros in the CMOS

process. Since these restrictions are serious, the passive element must be replaced by analog

circuits. Although circuits need power to boost and have worse linearity, there are many

circuit technique to increasing linearity in last chapter. Figure 4.2 & 4.3 show the common

replacement of resistance and inductance by Gm blocks.
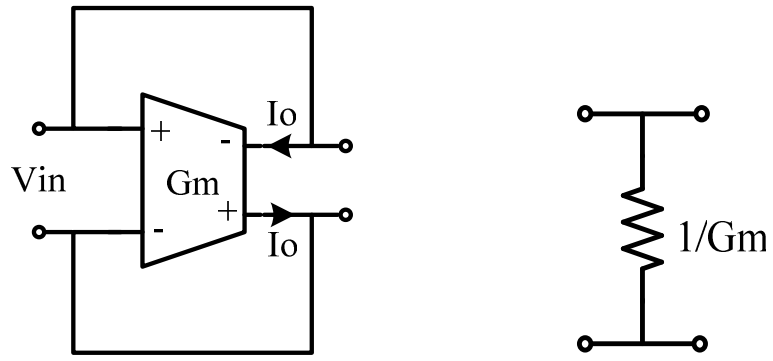
Figure 4.2 Differential Gm connected as resistance
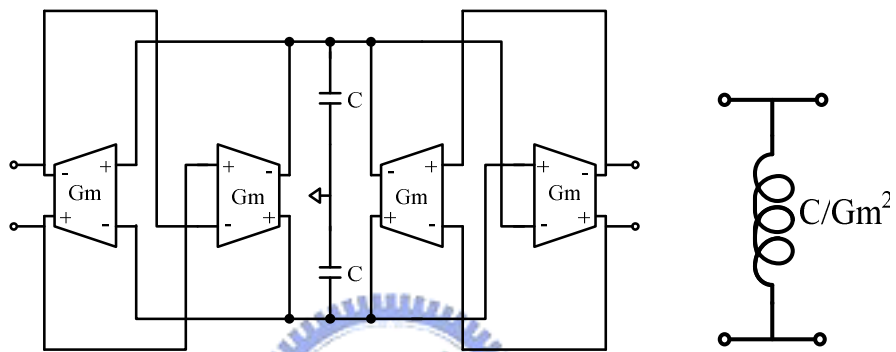
Figure 4.3 Differential Gm connected as inductance by gyrator approach

The Gm block has non-ideal effects which are finite output impedance and RHP-zero.

When Gm is connected as passive element, it will add parasitic components as shown in

Figure 4.4 and 4.5. In order to reduce g_o and increase τ, the Gm should be design by a simple

structure with some circuit to increase R_{out}.
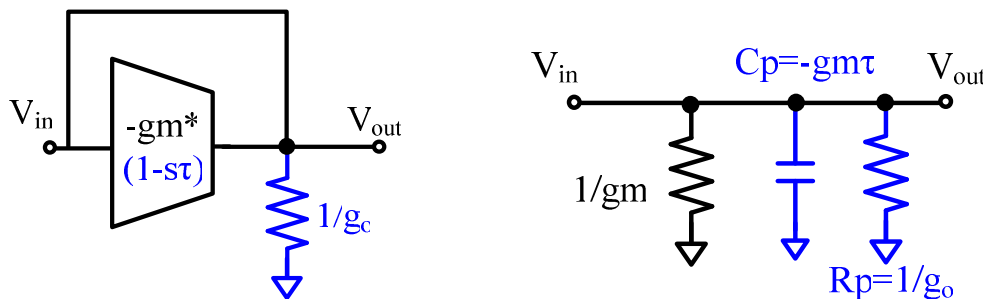
Figure 4.4 resistor implemented by non-ideal Gm with finite $1/g_o$ and RHP-zero
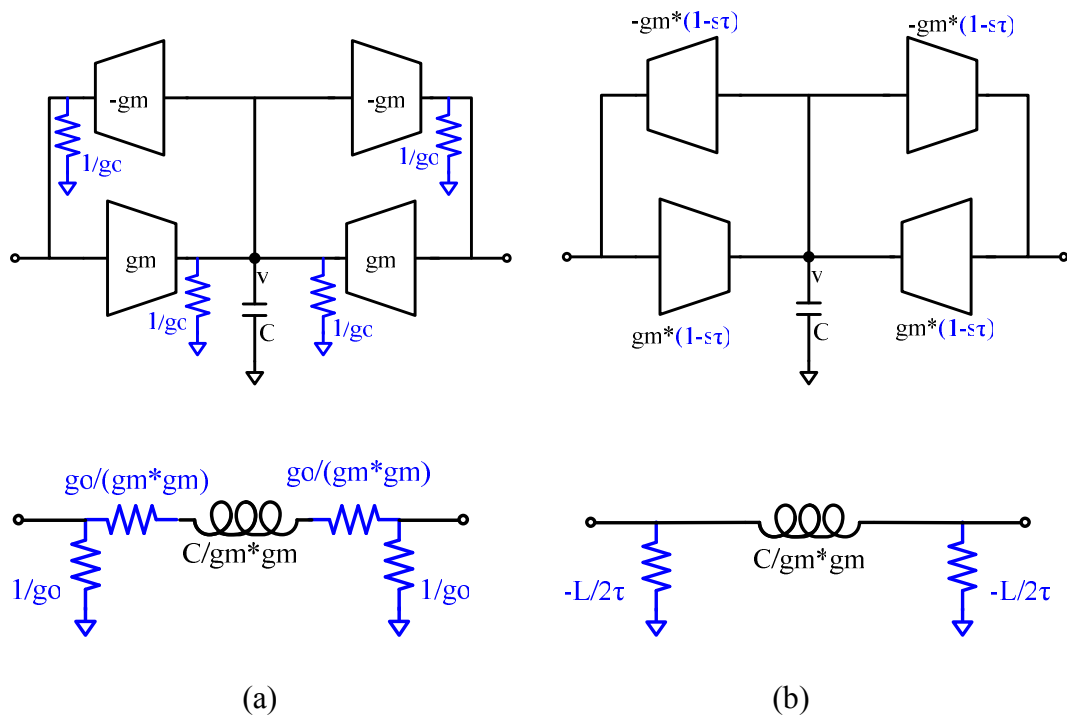
Figure 4.5 Inductor implemented by non-ideal Gm with finite (a) Rout (b) RHP-zero

The gyrator using integrator has -90° phase shift, but in chapter 3 the integrator shows

very poor behavior at low and high frequency. That is, the phase of the integrator is very far

from being -90° for frequency $f \ll f_{int3db}$ and $f \gg f_{RHP\_zero}$. We can analyze simple gyrator

shown in Figure 4.6. From (4.1) we can draw R_{in} V.S. frequency plot. The curve has two

corners which point to Gm f_{int3db} and f_{GmBW}, respectively. When signal frequency is low (f

$\ll f_{int3db}$), the gyrator acts as resistor with the value depends on R_{out} of the Gm. Even at DC

frequency, the resistor only causes little loss without changing response. But when signal

frequency is high ($f \gg f_{RHP\_zero}$), it does not matter whether the phase of the integrator is still

-90° or not : the capacitors connected to the filter nodes will short circuit them because their

impedance goes to zero, whether the integrator performs well or poorly, and we will get the

typical attenuation of the signal at high frequencies.
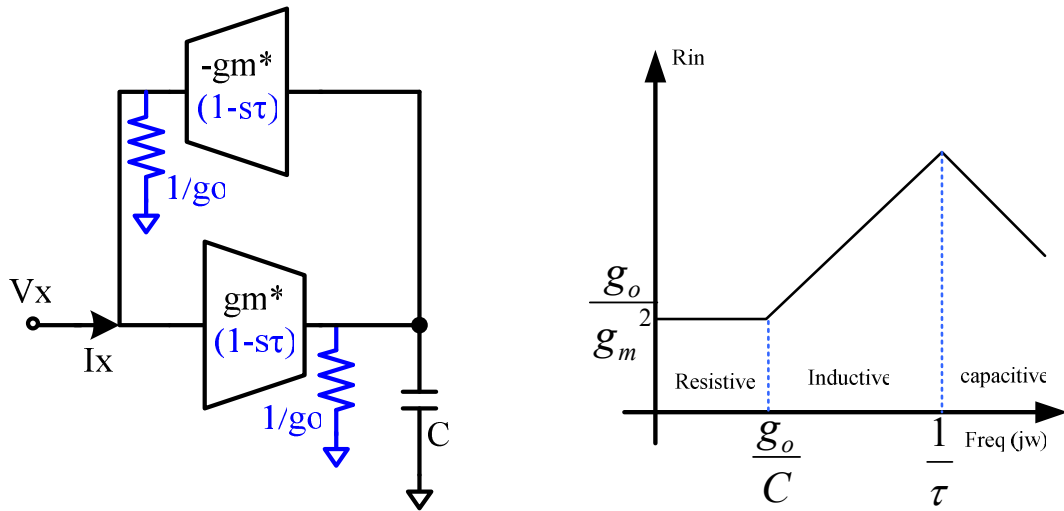
Figure 4.6 Non-ideal Gm effects the inductor

$$Vx \times [gm(1-s\tau) \times \frac{1}{sC+go}] \times [-gm(1-s\tau)] = -Ix$$

$$Rin = \frac{Vx}{Ix} = \frac{sC+go}{gm^2(1-s\tau)^2} \qquad (4.1)$$

Another question will rise if the Gm output impedance is too "negative" and the Gm will

have the right-half-plane zero. For a stand-alone integrator, it could become unstable. Even so,

a gyrator built with Gm blocks will remain stable. This is owing to the feedback loops

inherent to a filter constructed with gyrators as shown in Figure 4.7. It can be found that

gyrator based inductor input impedance R_{in} is negative at zero frequency. But when the

inductor lies in LC ladder filter, the filter response at DC will be stable due to the input/output

impedance of the filter shown in Figure 4.8. That is the Gm could be designed at negative

output impedance which is not too far from zero.

43
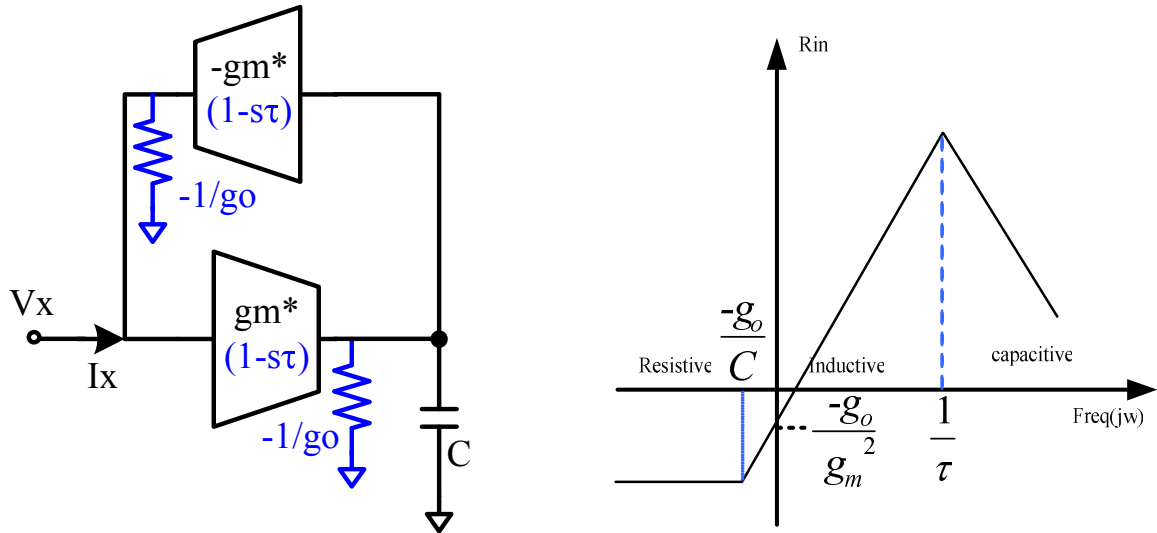
Figure 4.7 Negative impedance at DC frequency

$$H(0) = \frac{R_L}{R_S + (-R_a) + (-R_b) + R_L} > 0$$
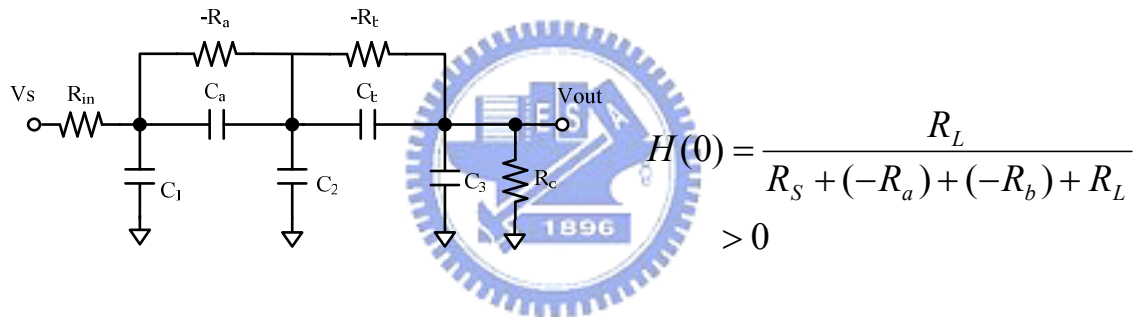
Figure 4.8 LC ladder low frequency gain with negative impedance

After element replacement, the filter has changed from Figure 4.1 to Figure 4.9. Input current source is made by Gm for its high input resistance. Grounded resistance is replaced by circuit shown in Figure 4.2. The floating inductor is made of at least four Gm. The circuit has to connect output buffer in order to load high capacitance measure equipment. The simple common source follower can be used as a buffer design for its excellent frequency response.
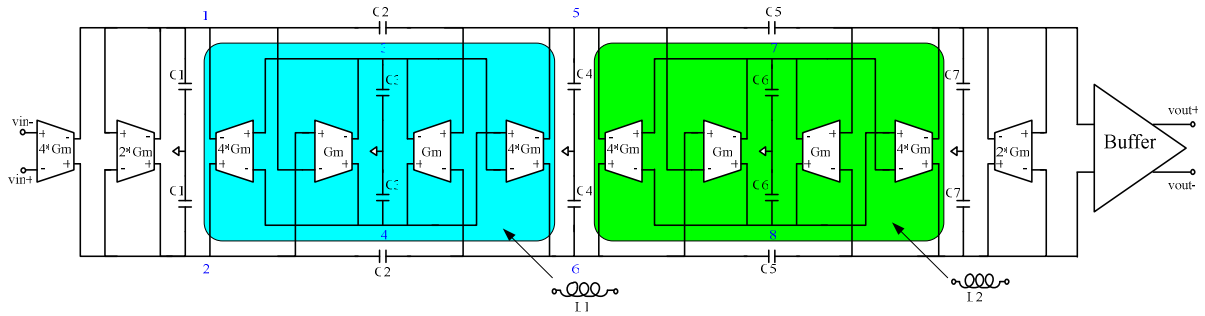
Figure 4.9 the 5th elliptic ladder filter using Gm-C technique

The internal nodes gain may be a serious problem since it could be higher than output

gain. And for UWB receiver, the filter is the last element in receiver path. The filter input

swing is very large. If the internal node swing is higher than output swing, the Gm blocks

may saturate and reduce dynamic range. The reason of internal node peaking is that it is band

pass transform function in Figure 4.10(b). The analysis is assumed using 3rd elliptic Gm-C

filter with ideal Gm and filter has the same input/output impedance. Since the most serious

internal node peaking comes from the two capacitors of gyrator circuits, there must have some

adjustment. In Figure 4.10 (a), the X & Y are defined by the connection with internal

capacitor. The output of X and the input of Y connect with the internal capacitor. For a

desired inductor value with minimum power and acceptable process variation, the internal

capacitor can be chosen as 0.4pf. Then the product of X and Y is known as $4gm^2$ and the gm

is the transconductance of unit Gm since this can relax the design complexity and variation.

Figure 4.10(b) is the internal nodes magnitude response when X = Y = 2gm. We can see Vb

has magnitude about 3 times larger than Va in the pass band and this ratio is decided by X &

Y. Consider all the information, the X/Y ratio can be found as 1/4 in Figure 4.10(c). After adjustment, the result can be shown in Figure 4.11 and we can see all the internal response is less than one except a little higher in the pass band edge.

(a)

(b)

X:Y=1:4

Assume $g_m \propto$ power

$$\begin{cases} X * Y = 4g_m{}^2 \text{ (For Cap} = 0.4\text{pF)} \\ Y > 3X \text{ (Max internal Gain vs output)} \\ X + Y = \min \end{cases}$$

(c)
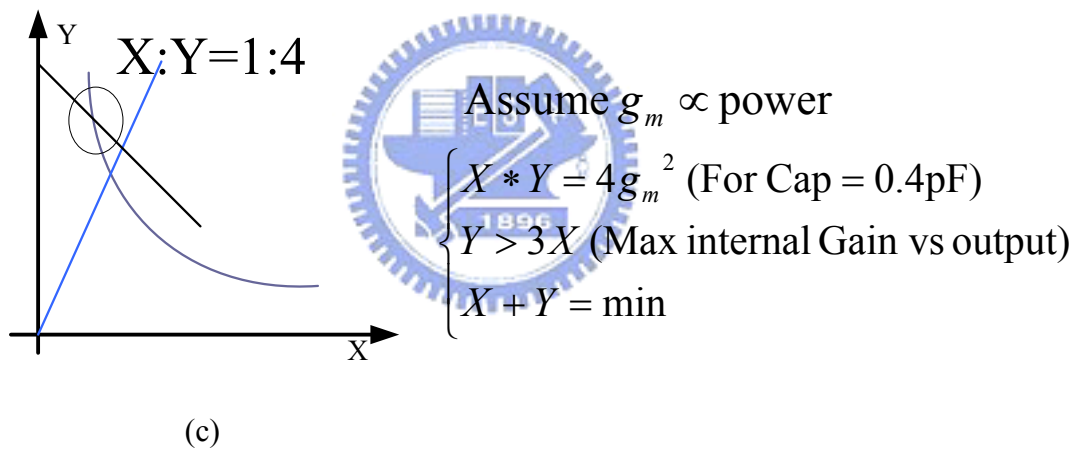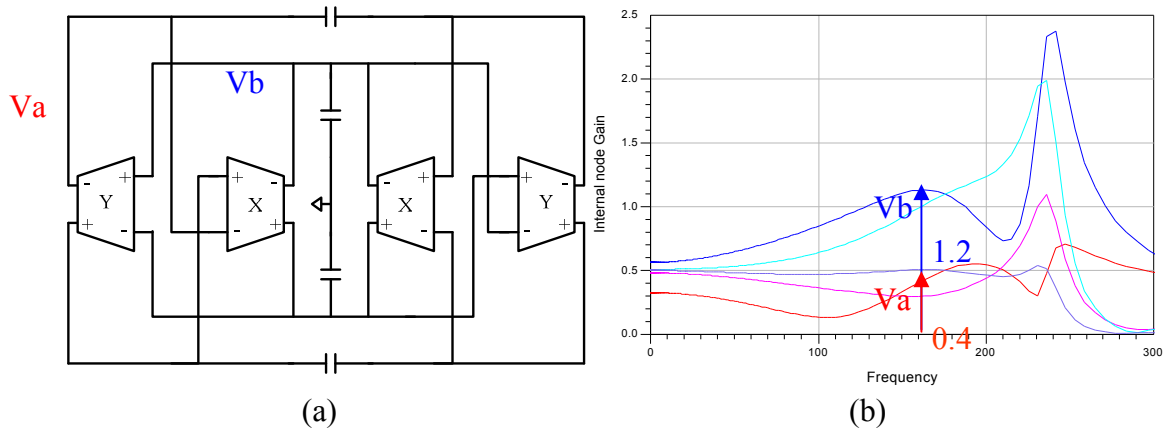
Figure 4.10 Adjust gm value in gyrator
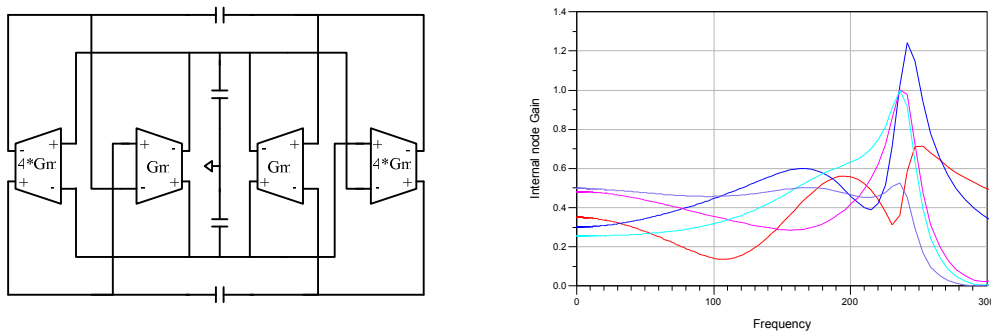
Figure 4.11 after adjusting X & Y

The LC ladder can also change to equal-ripple filter in Figure 4.12. The filter has higher

cutoff frequency than elliptic filter since the filter does not need high frequency zeros. The

magnitude response will be compared in section 4.4.
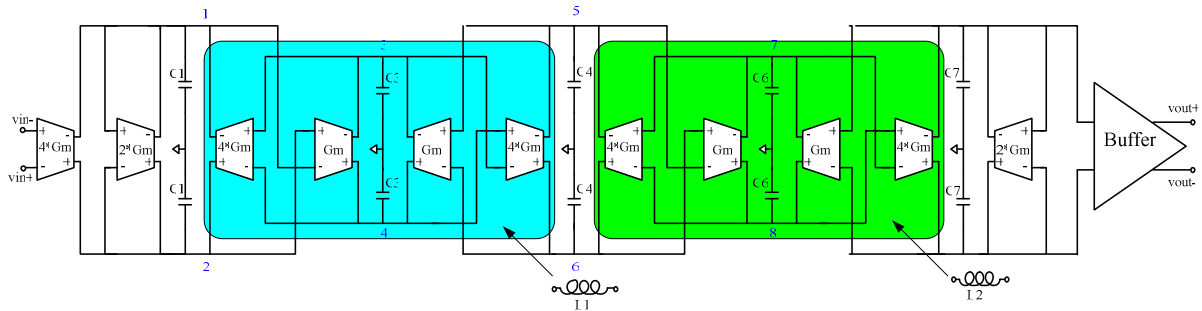
Figure 4.12 the 5th equal-ripple LC ladder filter using Gm-C technique

4.3 Sensitivity

We have to be concerned with a problem: components with exact design will generally

not be available. Maybe there are just desired components with exact value in the laboratory,

but it's generally impossible or too expensive in CMOS process. So the sensitivity has to be

analyzed especially when designing high frequency filter with high quality factor.

The definition of sensitivity of equation T with respect to x:

$$S_x^T = \frac{\partial T / T}{\partial x / x} = \frac{x}{T}\frac{\partial T}{\partial x} = \frac{\partial \ln T}{\partial \ln x} \qquad (\text{for d}(\ln u) = \frac{du}{u}) \qquad (4.2)$$

Sensitivity is the ratio of the relative error of the function T(s) to the relative

component error

From 5th order elliptic transfer function of (2.1):

$$T(s) = \frac{N(s)}{D(s)} = A \frac{(s^2 + \alpha_0)(s^2 + \alpha_1)}{s^5 + \beta_4 s^4 + \beta_3 s^3 + \beta_2 s^2 + \beta_1 s^1 + \beta_0}$$

$$= A \frac{(s - z_1)(s - z_2)(s - z_3)(s - z_4)}{(s - p_1)(s - p_2)(s - p_3)(s - p_4)(s - p_5)} \tag{4.3}$$

where A is constant and z_1&z_2, z_3&z_4, p_2&p_3, p_4&p_5 are conjugate.

To calculate the sensitivities to an element x by using (4.2) and (4.3):

$$S_x^{T(s)} = \frac{\partial \ln T(s)}{\partial \ln x} = \frac{\partial \ln(\frac{N(s)}{D(s)})}{\partial \ln x} = \frac{\partial \ln N(s)}{\partial \ln x} - \frac{\partial \ln D(s)}{\partial \ln x}$$

$$= S_x^A + x \frac{\partial}{\partial x} \{[\ln(s - z_1) + ... + \ln(s - z_4)] - [\ln(s - p_1) + ... + \ln(s - p_5)]\}$$

$$= S_x^A - [\frac{x \frac{\partial z_1}{\partial x}}{s - z_1} + ... + \frac{x \frac{\partial z_4}{\partial x}}{s - z_4}] + [\frac{x \frac{\partial p_1}{\partial x}}{s - p_1} + ... + \frac{x \frac{\partial p_5}{\partial x}}{s - p_5}] \tag{4.4}$$

$$= S_x^A - [\frac{z_1 S_x^{z_1}}{s - z_1} + ... + \frac{z_4 S_x^{z_4}}{s - z_4}] + [\frac{p_1 S_x^{p_1}}{s - p_1} + ... + \frac{p_5 S_x^{p_5}}{s - p_5}]$$

The deriving function is assumed all zeros and poles are functions of the component x of concern. If any zi or pi is independent of x, the corresponding sensitivity term is set to zero. (4.4) can be observed that the sensitivity becomes large near all the zeros and all the poles. For low pass filter the transfer function zeros are normally in the stop band, so it needs to be less concerned with the zeros. The filter DC gain is constant, so the sensitivity is always zero.

By neglecting all remaining terms:

$$S_x^{H(s)} \approx \frac{p_1 S_x^{p_1}}{s - p_1} + ... + \frac{p_5 S_x^{p_5}}{s - p_5} \tag{4.5}$$

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When s = jω and moving along the jω-axis, the $S_x^{H(s)}$ becomes large each time we move

past a zero or pole because the denominator terms $s - p_1$ and $s - z_1$ are small. The

sensitivities are normally largest at the pass band corner since in it the pole quality is the

largest in Figure2.3.

The sensitivity analysis of LC ladder filter can be found by a simple power relation.

Assume ideal passive LC ladder filter will not have power dissipation for inductors and

capacitors. In Figure 4.13, the power delivered by the source Vs to the filter, this means to the

right terminal of V_1:

$$P_1 = \left| I_1(j\omega) \right|^2 \operatorname{Re} Z_{in}(j\omega) \tag{4.6}$$

where I_1 is the current through R_{in} and Z_{in} is the impedance seen into the filter at V_1. The

maximum value of P_1 is when $Z_{in} = R_{in}$ and then $V_1 = Vs / 2$, P_1 will be:

$$P_{1,\max} = \frac{\left| Vs(j\omega) \right|^2}{4R_{in}} \tag{4.7}$$

The power delivered to the load Ro is :

$$P_{out} = \frac{\left| Vout(j\omega) \right|^2}{R_o} \tag{4.8}$$
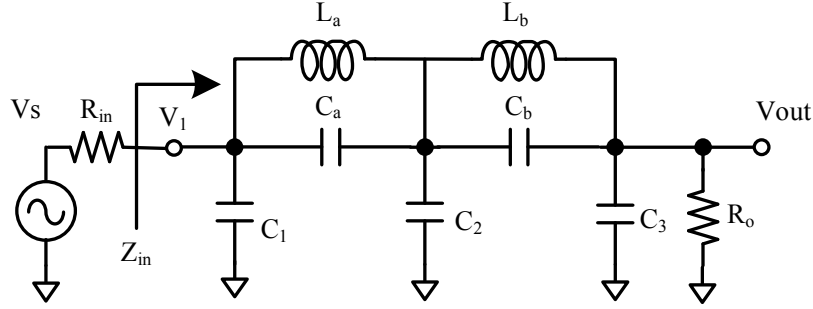
Figure 4.13 the 5th elliptic LC ladder filter working between R_{in} and R_o

Since the filter is passive, the power ratio $|H(j\omega)|^2$ is at most equal to one and is obtained

by (4.6) and (4.7):

$$|H(j\omega)|^2 = \frac{P_{out}}{P_{1,max}} = \frac{4R_{in}}{R_o}\left|\frac{Vout(j\omega)}{Vs(j\omega)}\right|^2 = \frac{4R_{in}}{R_o}|T(j\omega)|^2 \leq 1 \qquad (4.9)$$

Take square root of (4.8) and replace jω by s:

$$H(s) = 2\sqrt{\frac{R_{in}}{R_o}}T(s) \qquad (4.10)$$

The attenuation can be found fro from (4.3) & (4.9):

$$\alpha(\omega, x) = 20\log\frac{1}{|H(j\omega)|} \geq 0 \quad \text{for } |H(j\omega)| \leq 0 \qquad (4.11)$$

At some frequencies like ω_r, $|H(j\omega_r)| = 1$ and $|\alpha(j\omega_r)| = 0$ and since this is the

maximum and minimum respectively. So it is clear that:

$$\frac{\partial H(j\omega_r, x)}{\partial x} = 0 \text{ and } \frac{\partial \alpha(j\omega_r, x)}{\partial x} = 0 \qquad (4.12)$$

(4.11) follows that the sensitivity functions are zero at the frequencies at which

$|\alpha(j\omega, x)| = 0$ and $|H(j\omega, x)| = 1$. Since the value of α_{max} remain small throughout

the pass band, the sensitivity can also remain small over the pass band. Although the

sensitivity could be large in the stop band, the requirement for the loss in stop band is less

concerned. Such excellent sensitivity behavior has intrinsic advantage over active filter based

on passive ladder type. So the LC ladder topology based Gm-C filter still has excellent

sensitivity.

Chapter 5

Filter Implementation and Measurement

In the last chapter the analysis of filter has been completed. In this chapter the filter simulation, implementation and measurement will be discussed. The simulation result of Gm and filter will be introduced in Section 5.1. Circuit layout and some layout skills will be shown in Section 5.2. After layout the package and measurement plan is described at Section 5.3. The measurement result and comparisons will be given in the final section

5.1 Simulation Result

The Gm simulation result is shown in Figure 5.1(a), and Gm is flat within $\pm$ 0.375 Volt. The value of Gm is 0.529mA/V. (b) is Gm integrator with 0.5pf load and show DC voltage gain with 49.2dB. The integrator has f_{3db} = 571 kHz, f_T = 146 MHz, and $f_{RHP\text{-}zero}$ = 47.6 GHz with their phase at -45 ^{o}, -90 ^{o}, and-135 ^{o} respectively.
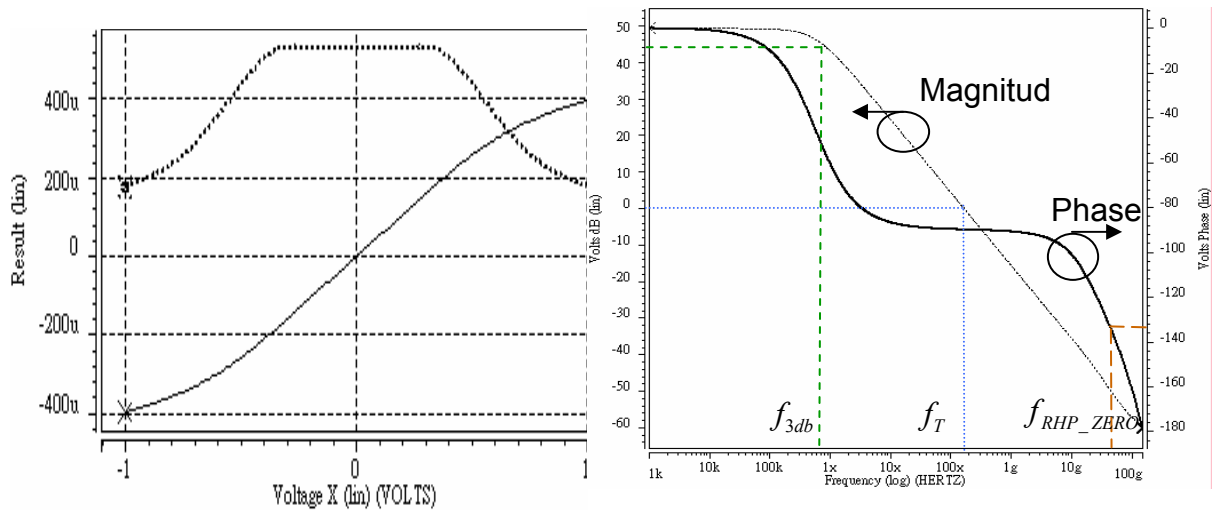
(a) Iod & Gm vs. input signal   (b) Gm integrator with 0.5pf load

Figure 5.1 Gm and Integrator simulation result

Table 5.1 shows the Gm integrator comparison with specification and the post-simulation has little f_T since post simulation considers parasitic capacitance. And the design of filter should be adjusted to meet original response.

Parameters	Specification	Pre-Simulation	Post-Simulation
DC voltage gain	45 dB	58 dB	49.2dB
Unit-gain frequency	165MHz	166 MHz	146 MHz
Integrator 3dB freq.	500 kHz	11 kHz	571 kHz

Table 5.1 Gm integrator comparison with specification
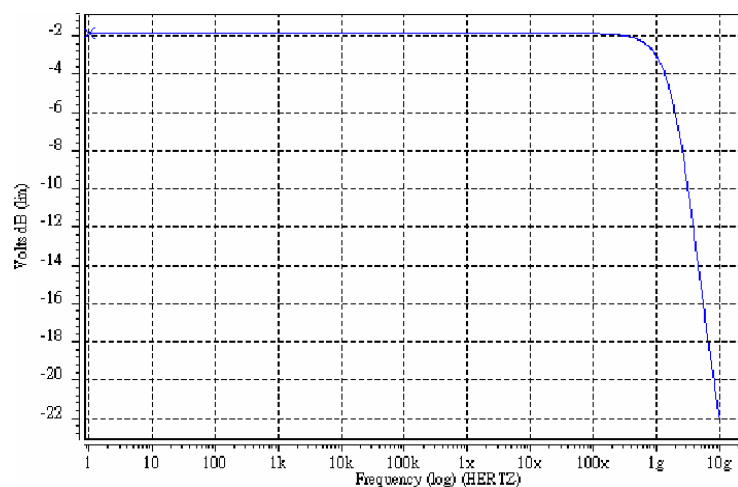
Figure 5.2 Buffer magnitude response

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The buffer magnitude response is shown in Figure 5.2. The DC gain is -1.87dB with 3dB

frequency @ 1.65GHz

The Figure 5.3 shows the 5th order elliptic ladder filter magnitude response. The pass

band loss is about 3dB due to buffer loss. For the transition band, there is -12.1dB loss

@260MHz, -36.9dB loss @300MHz The cutoff frequency is 248MHz with 0.92dB pass band

ripple. The power dissipation of this filter is 32.25mW (including buffer).
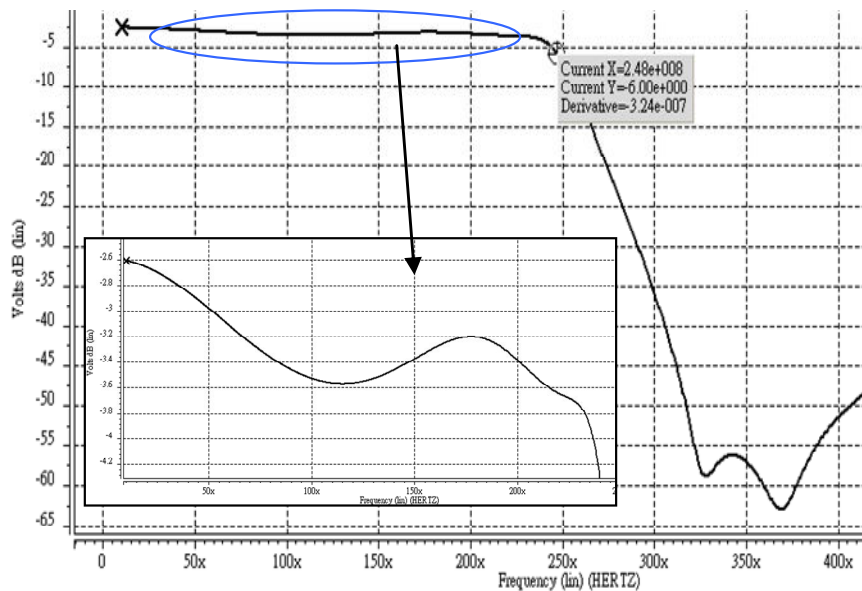
Figure 5.3 The 5th elliptic low pass filter simulation result (post-sim)

The 5th order equal-ripple LPF simulation result is shown in Figure 5.4. The cutoff

frequency is about 480MHz. The f_{3db} of equal-ripple is higher than that of elliptic since the

elliptic must generation high frequency zeros in stop band. Even so, the equal-ripple filter is

not suitable for UWB systems due to its gradual transition band.
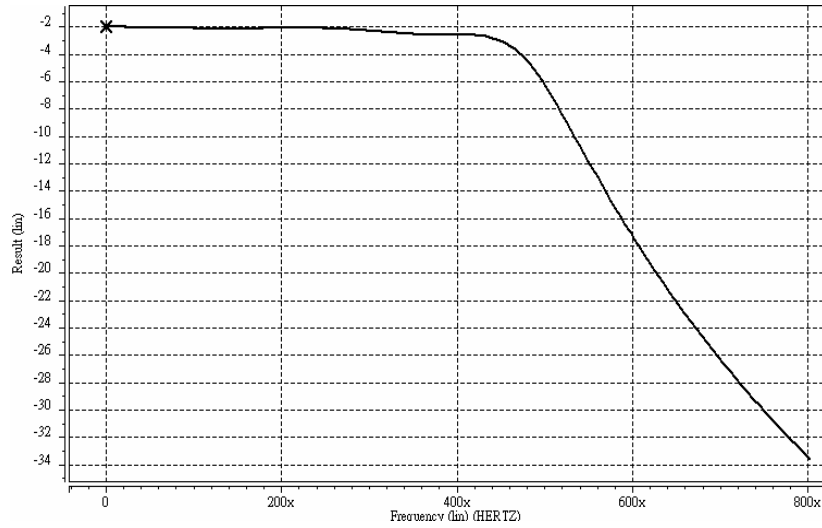
Figure 5.4 the 5th order equal-ripple low pass filter simulation result (pre-sim)
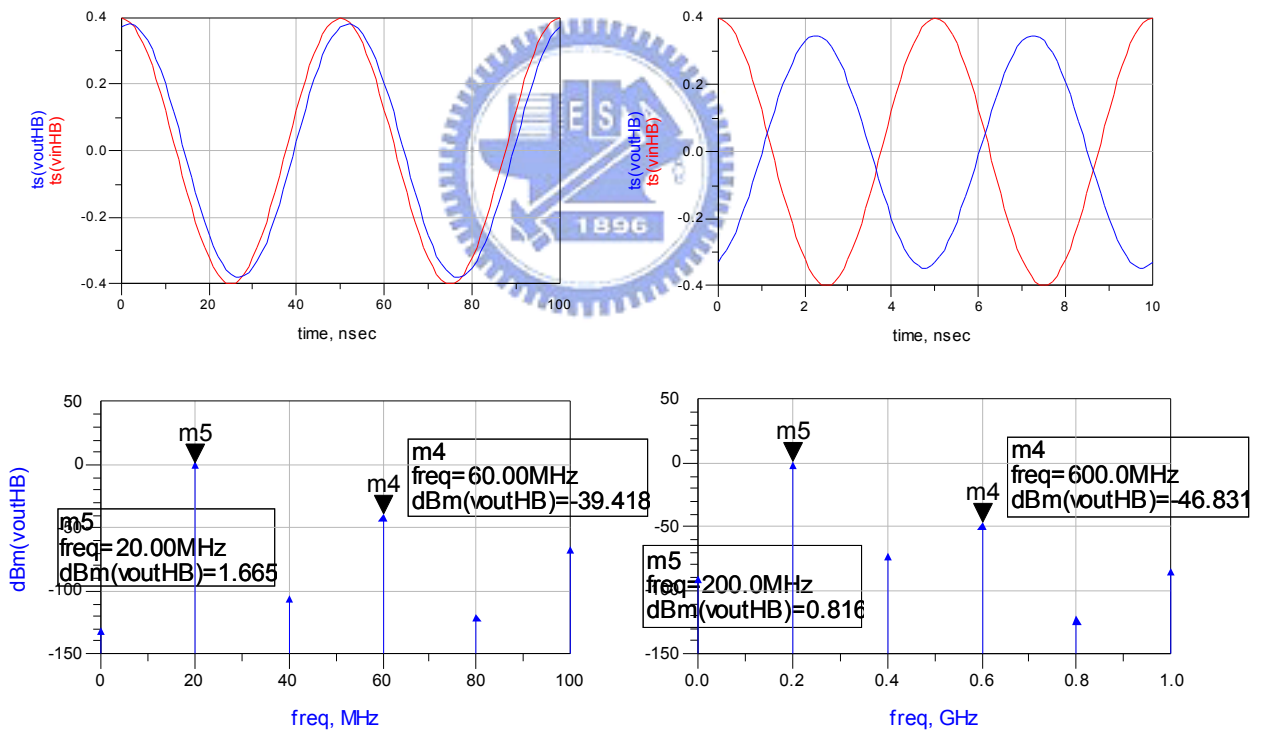
(a) Input @20MHz

(b) Input @200MHz

Figure 5.5 Transient & Harmonic Balance analysis with Vpeak=0.4Volt

The harmonic balance and transient analysis for elliptic filter are shown in Figure

5.5.Transient analysis shows timing graph and the circuit oscillation can be found in it. The graph also shows different output swing because of the ripple in pass band. The total harmonic distortion (THD) of (a) is -41.08dB, -47.65dB in (b). The THD is better when input signal is at higher frequency since the 3rd harmonic lies in stop band.

The filter comparison among specification, pre-simulation, and post-simulation is listed in Table 5.2. Although THD is worse than specification, the THD needs for 5bit ADC is about -32dB. The post-sim result is still suitable for UWB system.

Parameters	Specification	Pre-Simulation	Post-Simulation
3dB frequency	245MHz	246MHz	248 MHz
loss @ 260、300MHz	-12dB,-20dB	-17.11dB, <-40dB	-12.1dB ,-36.9dB
THD @ 0.4Vpp	-40dB	-41.7dB	-35.2dB
Pass band ripple	1dB	0.635dB	0.92dB

Table 5.2 Filter comparison with specification

Table 5.3 is the comparisons with other filters. And dynamic range (DR) is defined as:

$$DR = 20 * \log(\frac{Vi_{max}}{\sqrt{\overline{v}^2{}_{ni}}}) \qquad (5.1)$$

Where Vi_{max} is maximum undistorted root-mean-square value of *Vin* with THD=1% and $\sqrt{\overline{v}^2{}_{ni}}$ is input-referred noise.

In order to compare many filters with different specification, the figure-of-merit (FOM) is defined as below:

$$FOM = 10\log(\frac{P_{diss}}{8kT \cdot f_{3dB} \cdot N \cdot DR}) \qquad (5.2)$$

Where Pdiss is power consumption, f$_{3dB}$ is cutoff frequency, N is the order of the filter, and DR is the dynamic range.

	Technique	Bandwidth	Topology	Power	DR(dB)	V_{DD}	FOM(dB)
This work	0.18 μm	241MHz	5th elliptic	29.16mW	58.4dB	1.8V	59.75dB
[6]	0.18 μm	1GHz	5th elliptic	90mW	64dB	1.8V	55.35dB
[4]	0.8 μm	60MHz	3rd elliptic	12mW	57dB	2.7V	64.54dB
[5]-1	0.5 μm	29.6MHz	3rd elliptic	39.9mW	76dB	5V	63.28dB
[5]-2	0.5 μm	29.9MHz	3rd elliptic	46.2mW	77dB	5V	63.42dB

Table 5.3 Comparison with other filters

5.2 Circuit Layout

The layout of Gm block is shown in Figure 5.6(a) and the size is 40μmx37μm. The Gm MOS size is chosen small to reduce parasitic capacitance. Figure 5.6(b) is the output buffer with the size of 71μmx62μm. The buffer is the power hungry element, and the layout should be stressed on the current driving capacity.
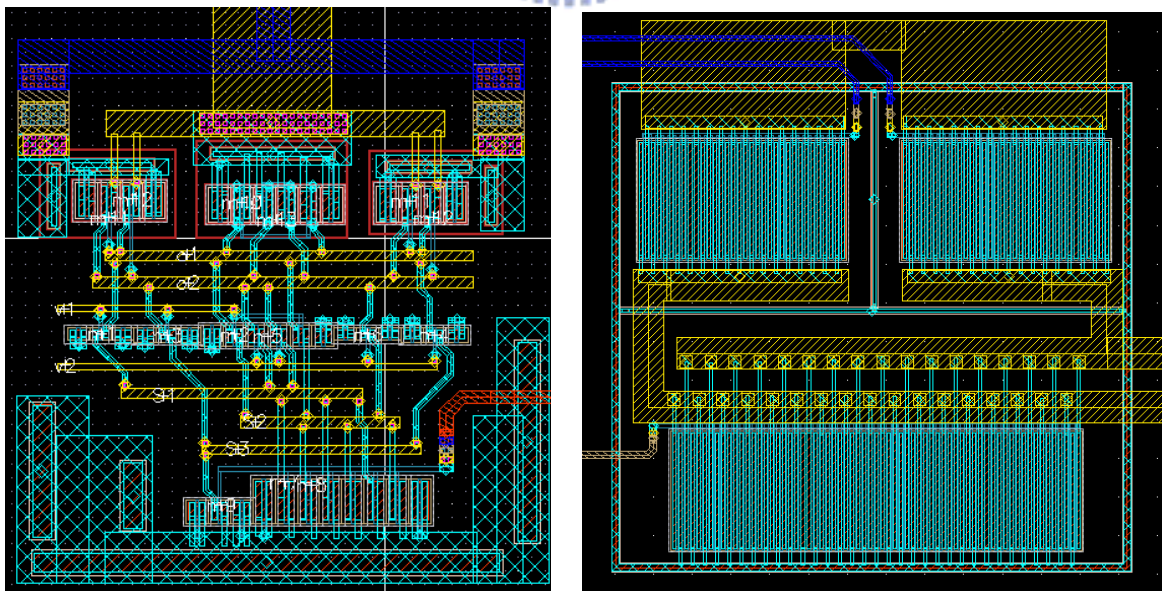
(a) Gm block   (b) Buffer block

Figure 5.6 Layouts of Gm and Buffer

The connection between other Gm blocks should be Metal3 and Metal2 with Metal1 as ground. Although the parasitic capacitance would be large than that without Metal1, the parasitic capacitance is more accurate. If the differential signal changes from Metal2 to Metal3, the two differential signal lines would not have the same parasitic capacitance as in Figure 5.7 (a). Since Gm output is current, the different capacitance will have different output voltage. The layout can be redrawn as (b), and then the parasitic capacitance will almost be equivalent.

(a) Without   (b) with

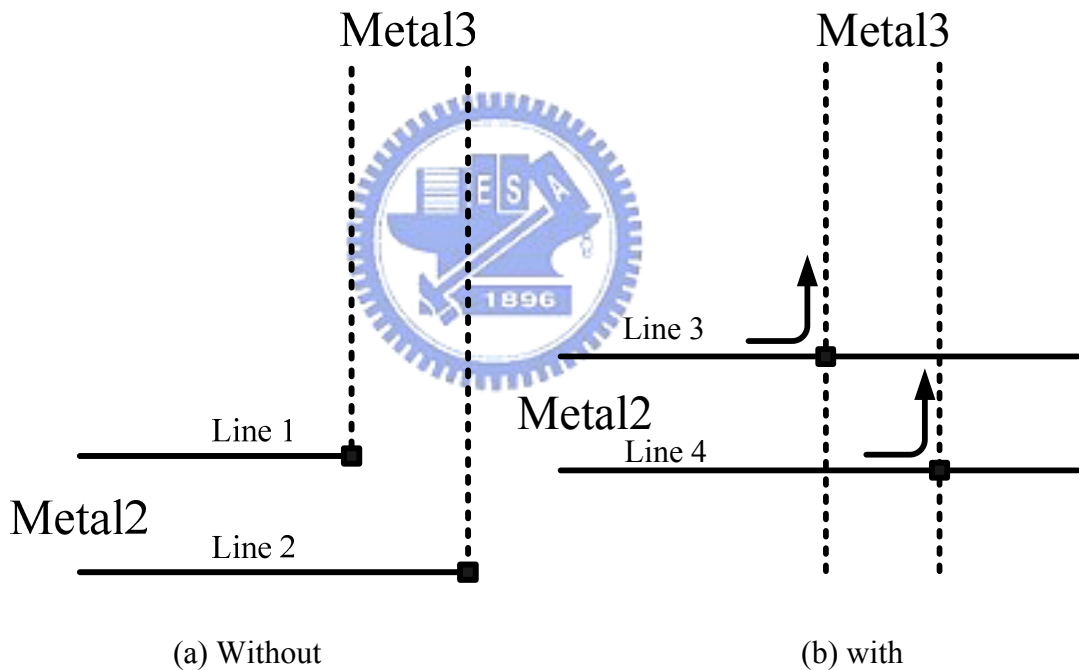Figure 5.7 Symmetry layout

Figure 5.8 is the layout of 5th order elliptic Gm-C low pass filter with the area of 850μmx300μm. The connection among all the Gm should be as close as possible to reduce parasitic capacitance of signal line. The filter has been packaged in SPIL QFN-20 in favor of measurement.
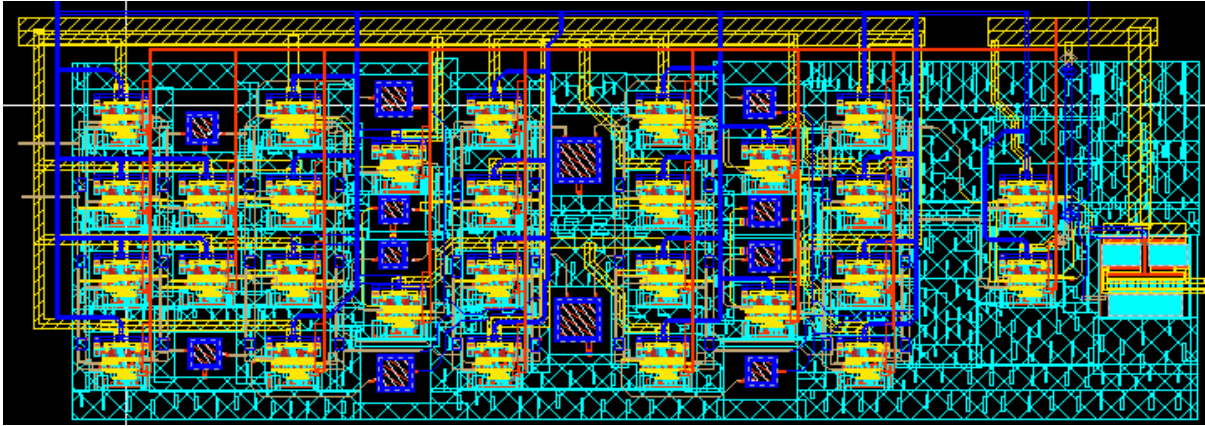
Figure 5.8 Layout of the 5th order elliptic low pass filter

5.3 Package and Measurement Plane

Electrostatic discharges (ESD) lies in I/O pins and using device to protect circuits form high-voltage, high-current stresses. The stresses can cause reliability failure in short time and the I/O circuitry of a chip would not work properly. ESD protection circuits provide low resistance paths under high-voltage conditions to dissipate the energy in ESD pulses, while in normal condition the ESD circuits would not function. The voltage limit the toleration of gate oxide voltage is only about 5V in 0.18μm process. If there were not any ESD protection circuits the gate oxide will be broken easily. Figure 5.9 shows the most popular ESD protection circuits. Diode chain protection provides ESD path through VDD or GND, and a large gate ground NMOS will break down once a large potential across the VDD and GND, and induces the charge in VDD flows through NMOS to GND.
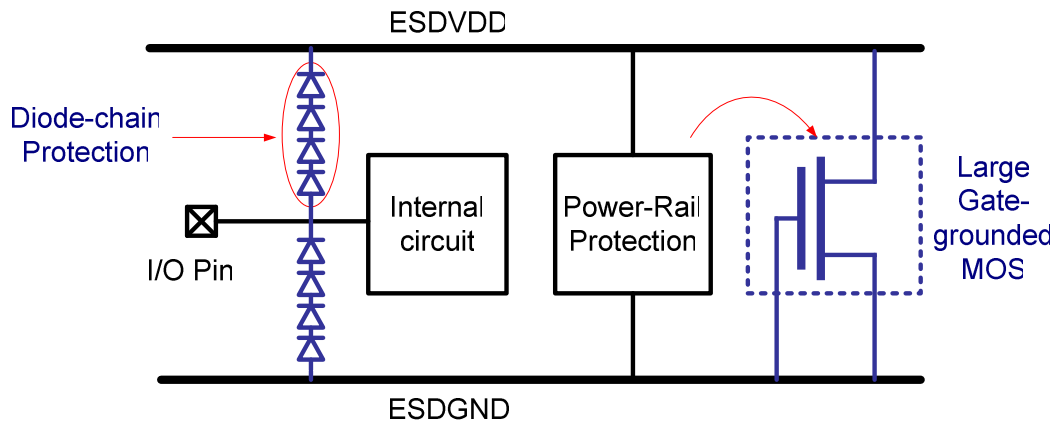
Figure 5.9 ESD protection circuits

The gate ground MOS shall prevent lightly-doped-drain which is common in deep submicron process. The distance between drain contact and boundary of gate and diffusion must be enlarged to sustain higher static charge. Contacts on guard ring are also avoided because that makes the break down of ESD device harder. The ESD circuits provided by UMC ensure 3.6kV in human body mode (HBM) test but induce about 40fF nonlinear capacitance in each pad.

Figure 5.10 Simplified package model

Figure 5.10 shows the simplified package model for each pin. Each pin has a finite self-inductance with 1-nH. Multiple bond wires and pins are used to decrease the equivalent inductance and resistance on the VDD and ground pins. A large on-chip capacitor, which is

composed of four MIM capacitors in this chip, is used to stabilize the difference between

VDD and ground, and reduces the risk of inter-stage coupling. Electrostatic discharge (ESD)

may result in CMOS devices permanent damage without protection circuits.

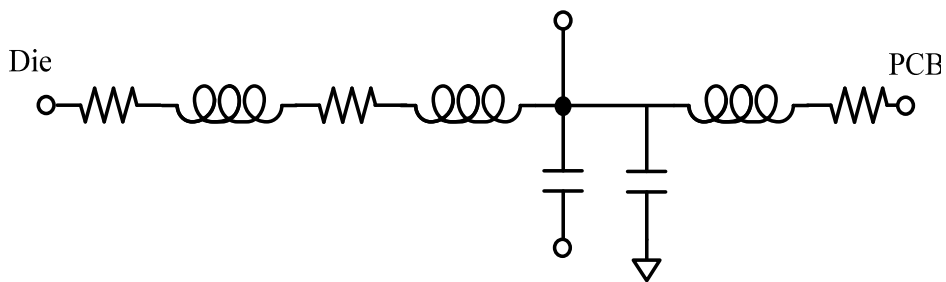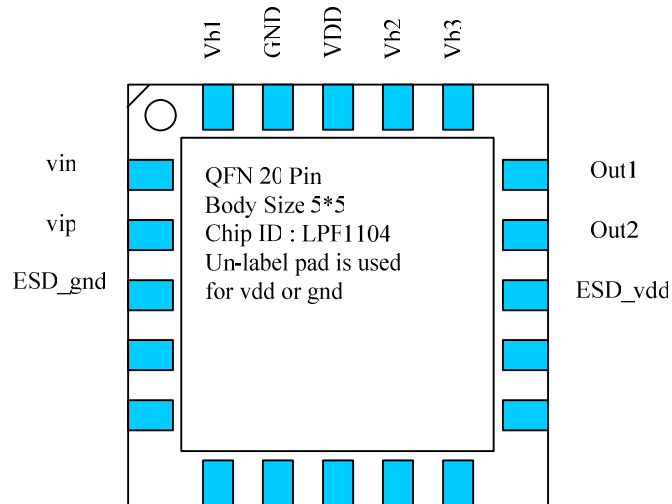Figure 5.11 Package pin assignment

Figure 5.11 is the QFN20 package pin assignment and the IC is packed by SPIL. The

chip is differential input / differential output. The un-label pads are not connected since the

lower part of chip is used as on-wafer test-key.

Fig 5.12 shows the PCB schematic design and we can see the bias path has two

capacitors connected to ground. Higher value capacitor is near power supply and lower value

is near the chip. The capacitors are using to filter out supply noise. Fig 5.13 shows the PCB

layout based on Figure 5.12 and the design is achieved by using Protel PCB. There are four

Metal layers for our PCB. The signal path has to put on top Metal and bias path can be put on

any layers.
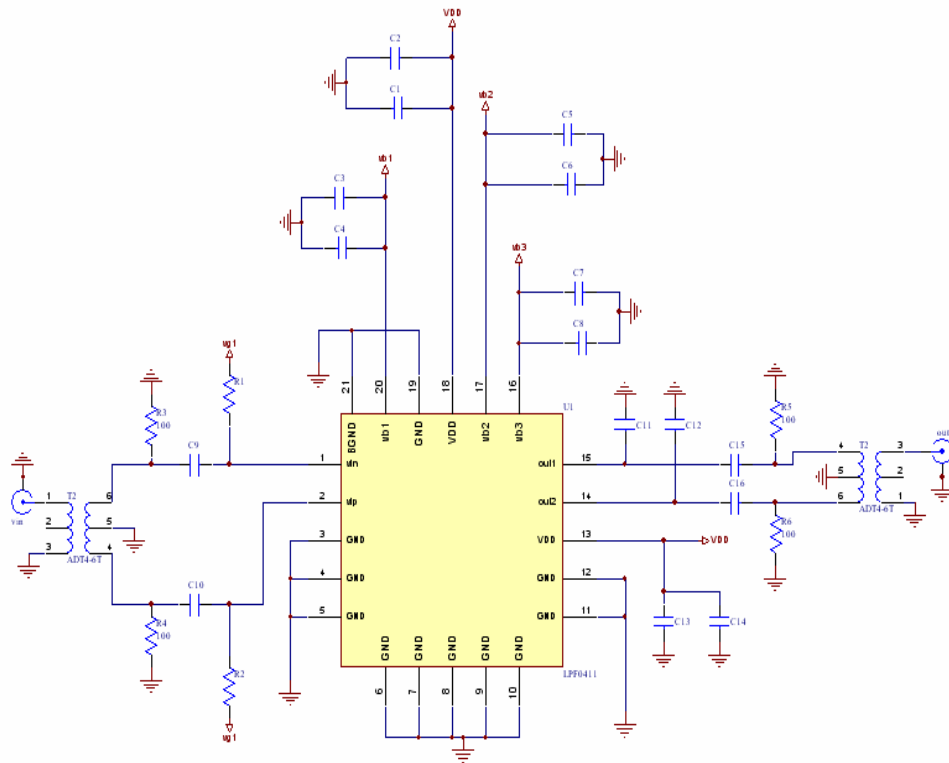
Figure 5.12 PCB Schematic
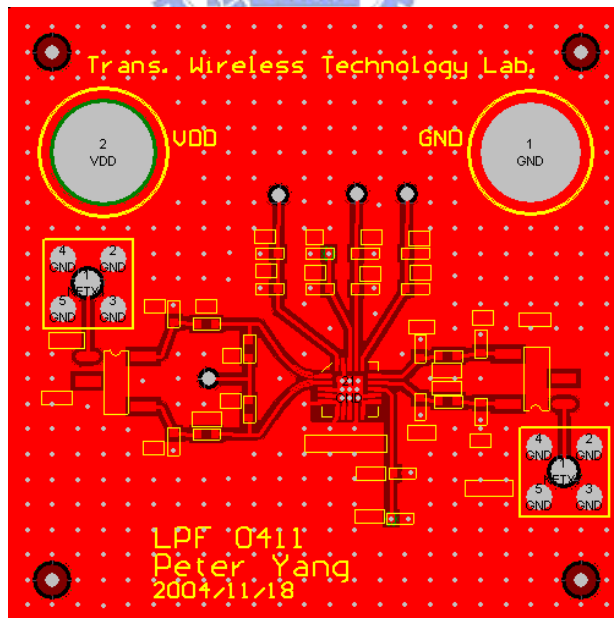
Figure 5.13 PCB layout

For measuring the timing and frequency domain parameters, the equipments needed to perform the measurement as listed below: Power Supply x 4, Spectrum Analyzer x 1, Oscilloscope x 1, and ESG x1. The measurement plan is shown in Figure 5.14. There needs two transformers for the purpose of converting differential to single end. The transformer Ohm ration is 1:4. That is, the transformer can convert 200Ohm impedance to 50Ohm. So it needs two 100 Ohm in series. Input signal uses AC couple while R1 can separate signal to ground.

The oscilloscope is used to measure most of the static parameters. Such as output swing and timing signal waveform. The spectrum analyzer is used to measure most of the frequency domain parameters, like magnitude response, total harmonic distortion (THD), one db compression point (P_{1db})
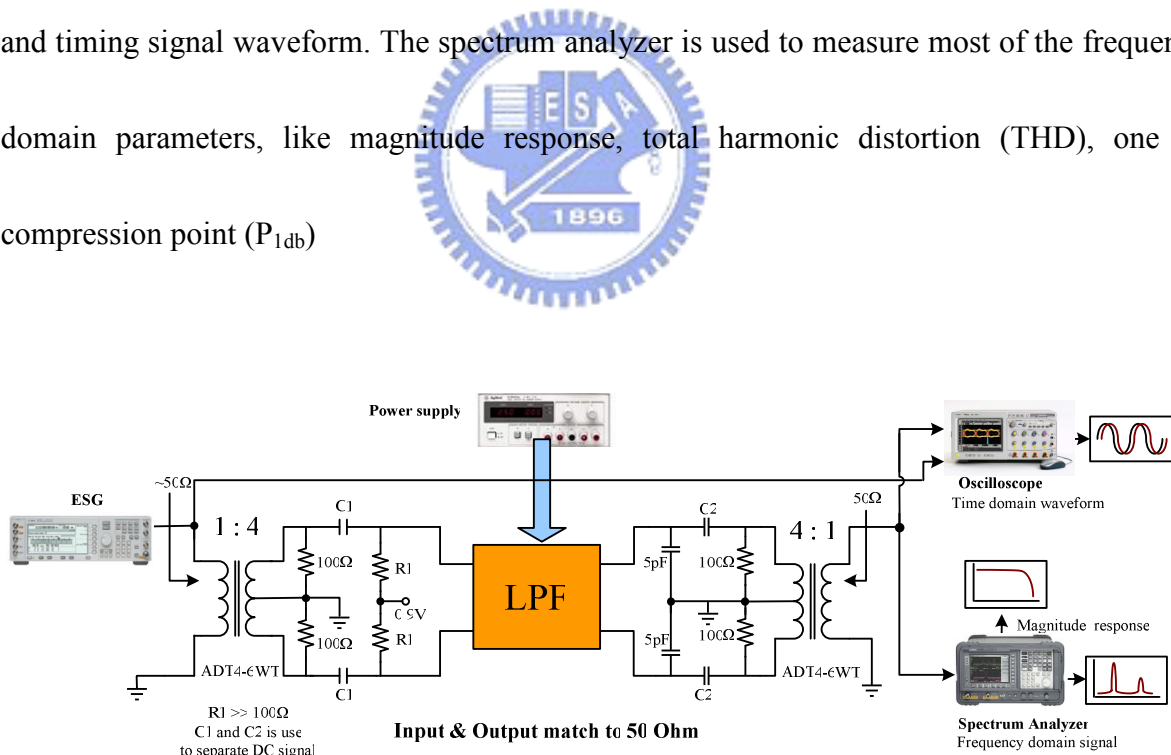
Figure 5.14 Measurement Plan

5.4 Measurement Result and Comparison

5.4.1 Magnitude Response

The magnitude response has 226 MHz bandwidth for -10dBm input as shown in Figure 5.15. The pass band gain is -4.07 dB with ±1.32 dB passband ripple. The additional loss comes from transformer and transmission line. The chip consumes 24 mA, that is, the power dissipation is 43.2mW. The difference is due the device variation since the Gm cells and capacitors are designed small in favor of high frequency application.
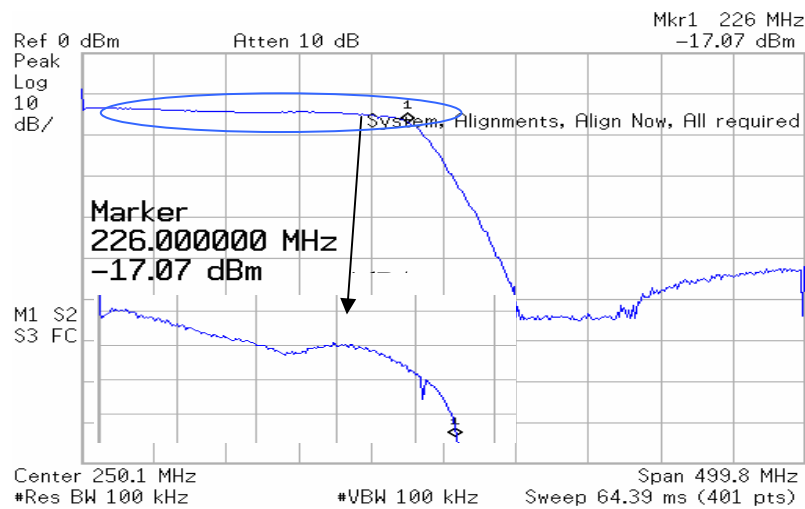
(a) Measurement Result
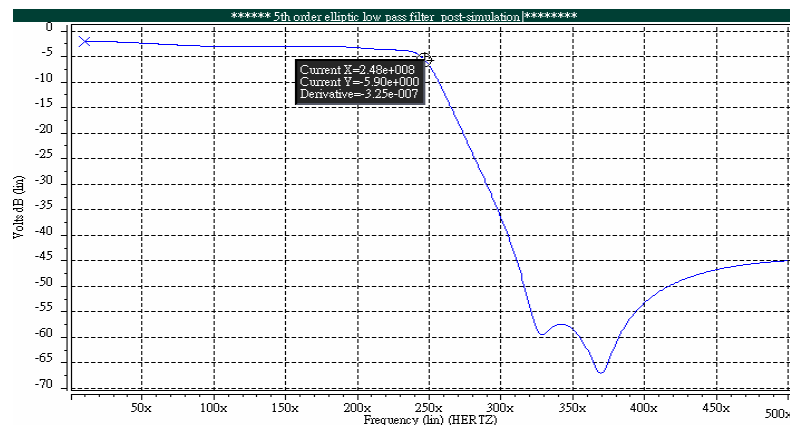
(b)Post-Simulation Result

Figure 5.15 Magnitude Response
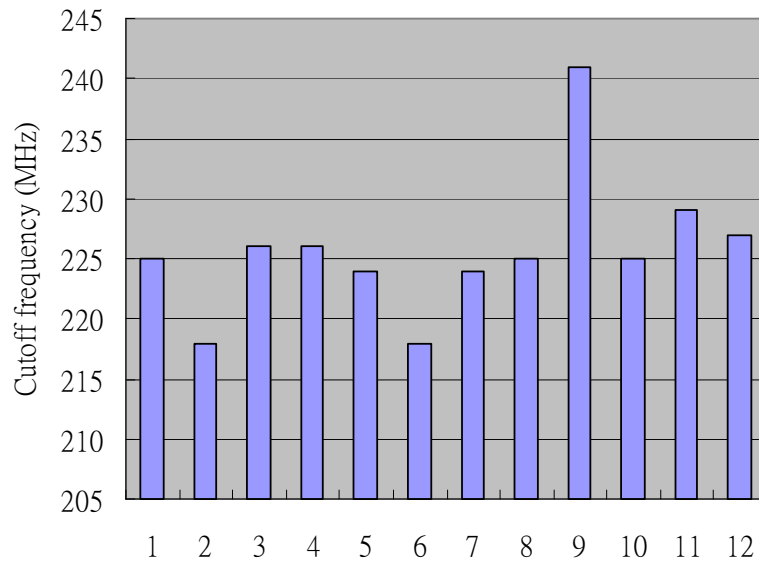
Figure 5.16 Cutoff frequency measurement results

Figure 5.16 shows the cutoff frequency measurement results. The filter cutoff frequency depends on capacitance will vary in magnitude response. Although the minimum node capacitance has been chosen as 0.4pf, the layout parasitic capacitance which comes from the metal line is about 0.15pf. Then the MIM capacitance is only about 0.25pf which the variation will become more serious. The average value of cutoff frequency is about 225MHz.

The magnitude response with low frequency is shown as Figure 5.17. Since the ESG generates signal as low as 250 kHz. The magnitude response ranges from 250 kHz to 20 MHz. The input signal is AC couple through a RC which sets frequency at 120 kHz, so the magnitude will have little loss at 250 kHz.
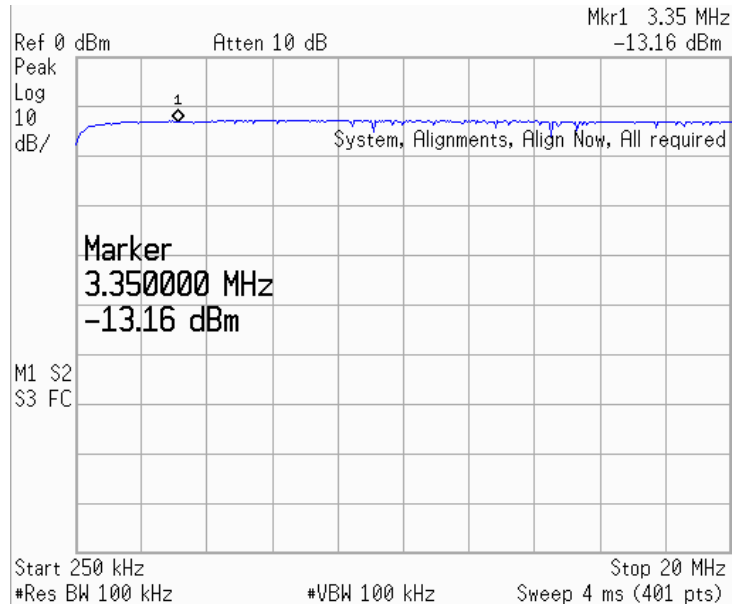
Figure 5.17 magnitude response with -10dBm input (250 kHz ~ 20MHz)

5.4.2 Harmonic Distortion

Post Layout Simulation Result:

harmonic no	frequency (hz)	fourier component	normalized component	phase (deg)	normalized phase (deg)
1	20.0000x	140.7406m	1.0000	160.5724	0.
2	40.0000x	2.0230m	14.3737m	-161.5176	-322.0900
3	60.0000x	2.2857m	16.2407m	111.8493	-48.7232
4	80.0000x	35.1593u	249.8162u	24.6367	-135.9357
5	100.0000x	99.4372u	706.5278u	-45.4337	-206.0061
6	120.0000x	20.2312u	143.7485u	-103.0937	-263.6661
7	140.0000x	48.6187u	345.4488u	73.0392	-87.5332
8	160.0000x	2.0803u	14.7808u	77.0732	-83.4992
9	180.0000x	5.3108u	37.7347u	60.6612	-99.9112

total harmonic distortion = 2.1704 percent
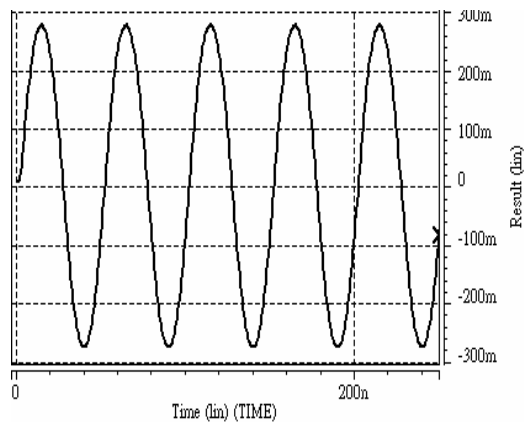
Figure 5.18 Spectrum and transient response with 0.4Vpeak input at 20MHz

harmonic no	frequency (hz)	fourier component	normalized component	phase (deg)	normalized phase (deg)
1	200.0000x	107.9739m	1.0000	-26.8116	0.
2	400.0000x	880.4545u	8.1543m	120.5986	147.4102
3	600.0000x	368.3383u	3.4114m	-155.0823	-128.2707
4	800.0000x	56.4913u	523.1937u	129.2196	156.0312
5	1.0000g	9.5287u	88.2498u	-10.6237	16.1879
6	1.2000g	3.2470u	30.0718u	18.5789	45.3905
7	1.4000g	3.1986u	29.6234u	-146.6536	-119.8420
8	1.6000g	659.5417n	6.1083u	-67.0020	-40.1904
9	1.8000g	1.4317u	13.2597u	-173.6146	-146.8030

total harmonic distortion =   885.5164m percent
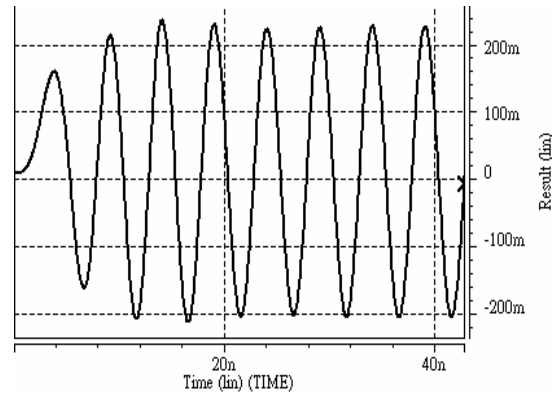
Figure 5.19 Spectrum and transient response with 0.4Vpeak input at 200MHz

Measured Result:
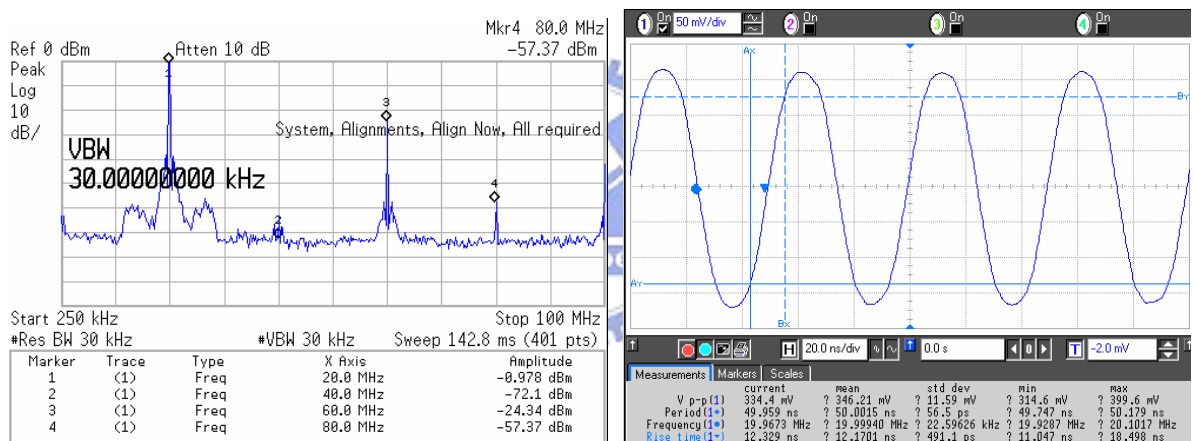
Figure 5.20 Measured spectrum and transient response with 0.4Vpeak input at 200MHz
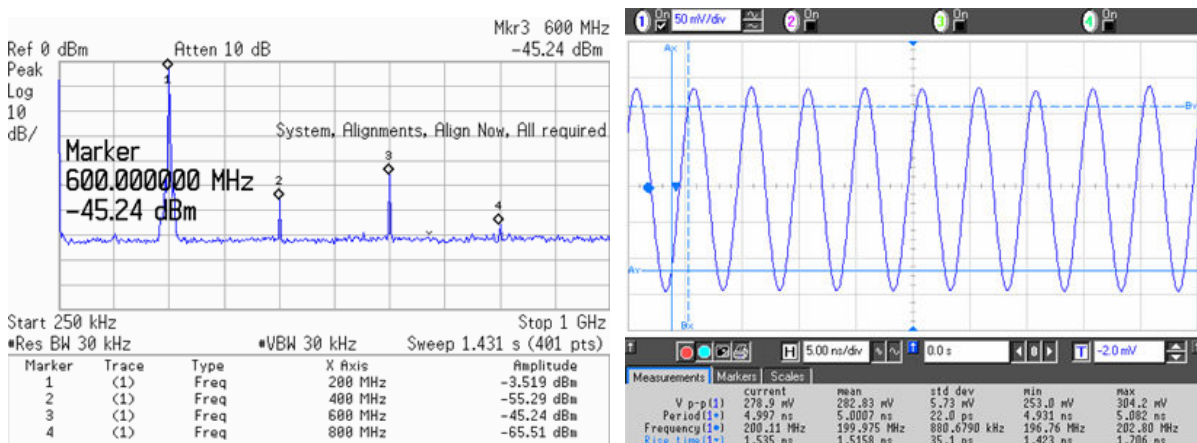
Figure 5.21 Measured spectrum and transient response with 0.4Vpeak input at 200MHz

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The simulation input signal is 0.4Vpeak, the input signal is chosen as 3dBm after

canceling the input transformer loss. Summarize from Figure 5.18 to Figure 5.21 the

harmonic distortion analysis be listed as Table 5.4.

	Figure 5.18	Figure 5.19	Figure 5.20	Figure 5.21
Total Harmonic distortion	-33.27dB	-41.06bB	-23.38dB	-41.28dB
Output swing (Vp-p)	554 mV	430 mV	334 mV	279 mV

Table 5.4 Harmonic Distortion Analysis

Since differential to single end needs output transformer which has loss about 3dB, the

measured output swing is less than post layout simulation.
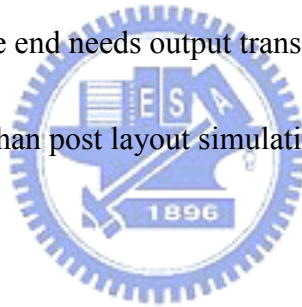
5.4.3 One dB compression point

The one dB compression point (P_{1dB}) shows in Figure 5.22. (a) and (b) are input P_{1dB} at 20MHz and 200MHz. Their values are 1.5 dBm and -1.1 dBm respectively.
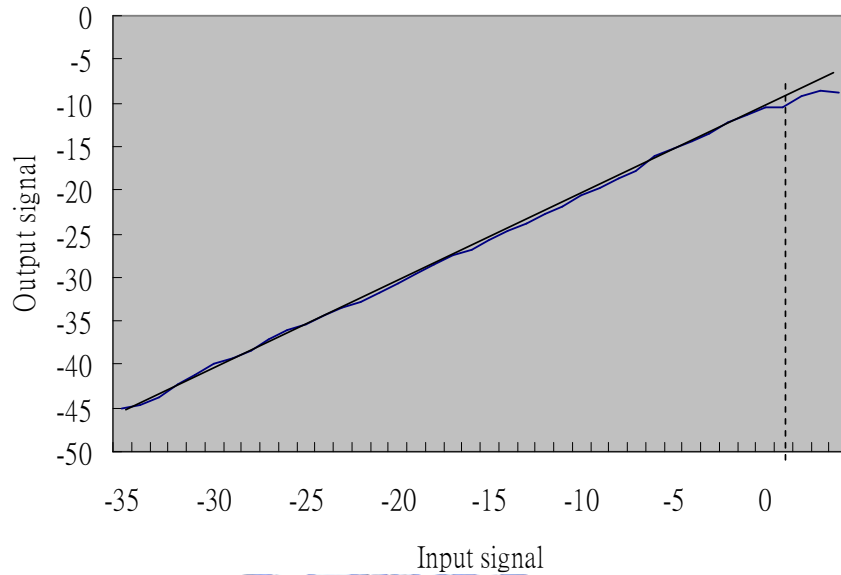
(a) P_{1dB} @ 20MHz input
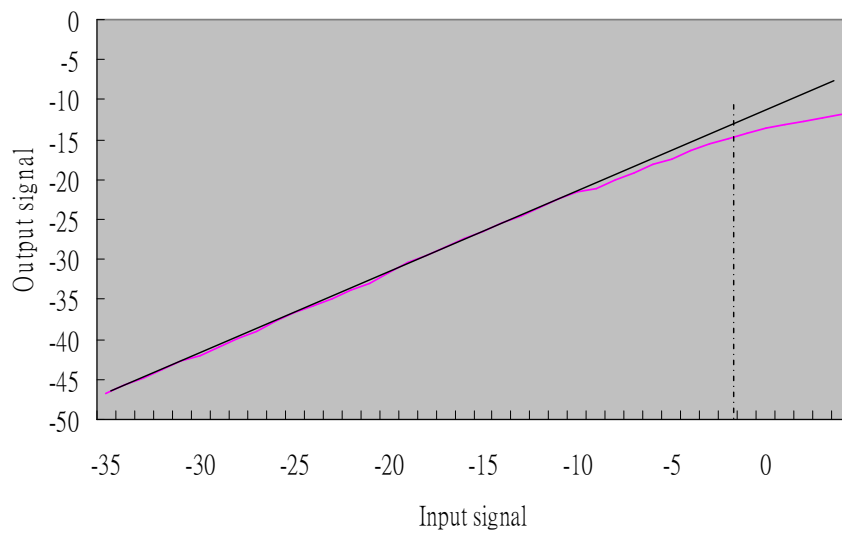
(b) P_{1dB} @ 200MHz input

Figure5.22 One dB compression point (P_{1dB})

5.4.4 Comparison

Table 5.5 is the comparison of filter with measurement, specification and post-sim. The 3dB frequency and pass band ripple do not meet specification. The reason is process variation and mismatch.

Parameters	Specification	Post-Simulation	Measurement
3dB frequency	245MHz	248 MHz	226 MHz
loss @ 260、300MHz	-12dB, -20dB	-12.1dB , -36.9dB	-15.5dB , <40dB
Power dissipation	30mW	32.25mW	43.2mW
Pass band ripple	1dB	0.92dB	1.32dB

Table 5.5 Filter comparison with specification

In order to compare many filters with the same FOM, the Dynamic Range can be obtained by P1dB as (5.3):

$$\mathrm{D}R = P_{1dB} - P_{mdos} \tag{5.3}$$

The P_{mdos} is minimum detectable output power (dBm) and is defined as:

$$\mathrm{P_{mdos}} = \mathrm{Po} + 10\log(\mathrm{BW}) + \mathrm{NF} + \mathrm{X(dB)} + \mathrm{Ga(dB)} \tag{5.4}$$

Where Po =Noise floor = -174dBm/MHz

BW = Device Operating bandwidth (Hz)

NF = Device Noise figure (dB)

X = 3dB typically

Ga = Device gain (dB)
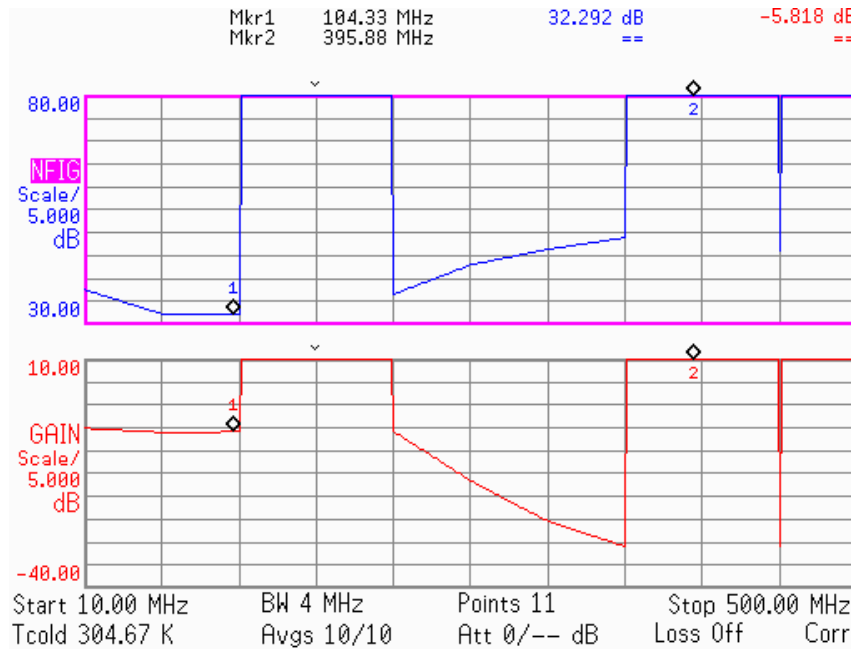
Figure5.23 Noise figure analysis

Figure 5.23 is noise figure analysis, the noise figure is 32.292dB with -5.818

passband gain. Then the dynamic range can be calculated:

$$
\begin{aligned}
\mathrm{D}R &= P_{1dB} - P_{mdos} \\
&= -1.1 + 174 - 83.54 - 32.292 - 3 + 4.07 \\
&= 58.138\text{dB}
\end{aligned}
$$

Take (5.2) to calculate FOM, the filter comparisons with measurement can be list as

Table 5.6.

	Technique	Bandwidth	Topology	Power	DR(dB)	V_{DD}	FOM(dB)
This work	0.18 μm	226MHz	5th elliptic	43.2mW	58.14dB	1.8V	61.55dB
[6]	0.18 μm	1GHz	5th elliptic	90mW	64dB	1.8V	55.35dB
[4]	0.8 μm	60MHz	3rd elliptic	12mW	57dB	2.7V	64.54dB
[5]-1	0.5 μm	29.6MHz	3rd elliptic	39.9mW	76dB	5V	63.28dB
[5]-2	0.5 μm	29.9MHz	3rd elliptic	46.2mW	77dB	5V	63.42dB

Table 5.6 Filter comparisons with measurement

Chapter 6

Conclusion and Future Work

This thesis has presented a high linear transconductor employing negative impedance load for high frequency UWB LPF. It has enabled the implementation of a 226 MHz high speed LPF in a $0.18\,\mu$m CMOS technology. This topology has been applied to the analog front-end for the UWB direct conversion receiver & transmitter which perform high speed, high linearity and wide bandwidth. In conclusion, the key contributions presented in previous chapters are summarized below.
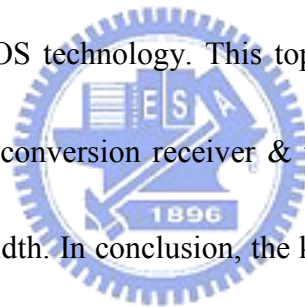
6.1　Conclusion

A high linear transconductor employing negative impedance load for high frequency UWB LPF has been presented in Chapter 3 & Chapter 4. These techniques improve the linearity and improve the harmonic distortion. Using negative impedance load makes the filter suitable for high frequency. The LPF circuit implemented in 0.18-μm CMOS process shows a 226 MHz bandwidth in Chapter 5. The filter provides a cutoff frequency of 226 MHz and pass

band ripple of ±1.32dB while drawing 43.2 mW from a 1.8-V supply. If for a SOC

application, the buffer is not needed to drive an ADC and the power consumption will be

about 36.2mW from a 1.8-V supply. Compare the filter with other spec. in Chapter 5. This

topology is applied to the RF front-end design for the UWB direct conversion transceiver.

6.2   Recommendations for Future Work

To increase the accuracy of this filter, the quality tuning and frequency tuning circuit can

be combined in the filter [15] [16] [17]. In the VCO tuning loop both frequency and quality

factors can be tuned. The VCO consists of two integrators and its frequency and quality factor

can be controlled. Figure 6.1 shows the Master-Slave frequency tuning technique by PLL.

The circuit generates the control voltage (Vtune) which makes the frequency of VCO based

on Gm-C gyrator is equal to the reference frequency. By this control voltage, the cutoff

frequency of the filter can be set to the desired value. A quality factor adjustment circuit is

also designed to compensate for the parasitic resistance shown in Figure 6.2.

There are three cases for the Q-tuning loop:

(a)If the integrators of the VCO have phase lead at the oscillating frequency ω_o

($1/Q_{int}(\omega_o) > 0$), the poles of the VCO are in the left complex half-plane. The VCO output is

a sine wave with exponentially decreasing amplitude.

(b) If the integrators of the VCO have phase lag at ω_o ($1/Q_{int}(\omega_o) < 0$), the poles of the

VCO are in the right complex half-plane. The VCO output is a sine wave with exponentially

increasing amplitude.

(c) Finally if the integrators of the VCO have no phase error at ω_o ($1/Qint(\omega_o) = 0$), the

poles of the VCO are in $j\omega$ axis. The VCO output is a sine wave with constant amplitude.

The Q-tuning loop controls the mplitude of the VCO in a way that it will oscillate with a

constant amplitude at infinite $Qint(\omega_o)$.
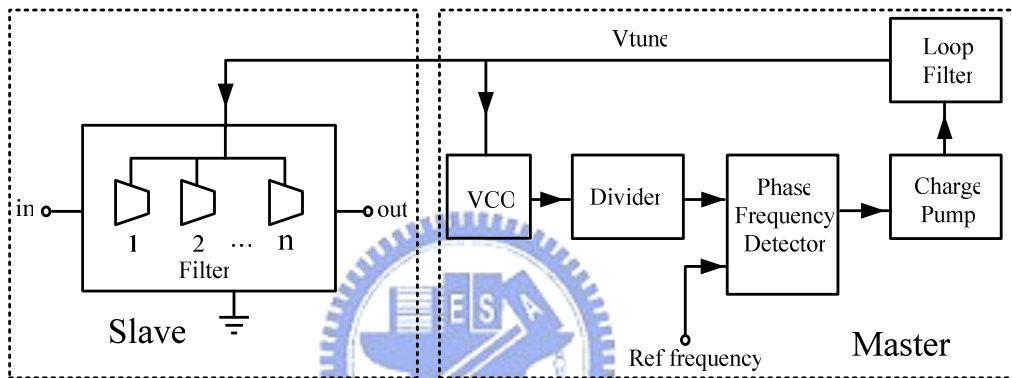
Figure 6.1 Frequency tuning technique
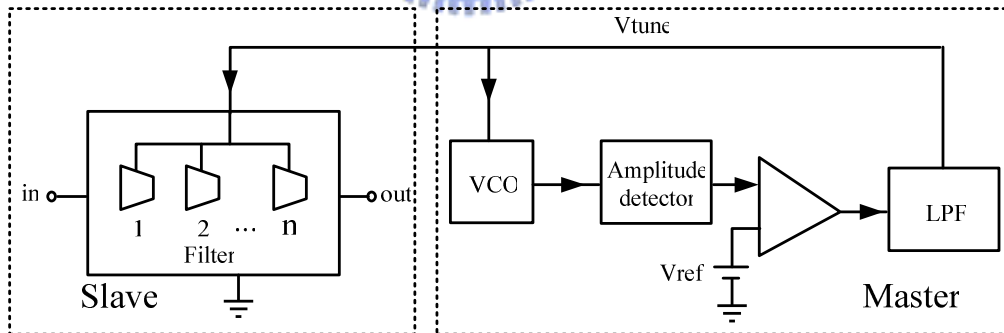
Figure 6.2 Quality tuning technique

The other way to reduce the transconductance variation due to threshold-voltage

variation is to use a threshold-voltage compensation circuit [18]. Figure 6.3 shows a

conventional current source with threshold voltage compensation. Neglect the channel length

modulation, the current source I_2 can be expressed as:

$$I_2 = k_2 (Vx - V_{t2})^2 = k_2 \left(Va + V_{tc1} - V_{t2} + \sqrt{\frac{I_{c1}}{k_{c1}} \frac{L_{c1}}{W_{c1}}} \right)^2 \qquad (6.1)$$

Then the current source is varied with the difference between V_{tc1} and V_{t2} rather than V_{t2}.

If the transistors MC1 and M2 are locally matched, the current I_2 is independent of the

threshold voltages.
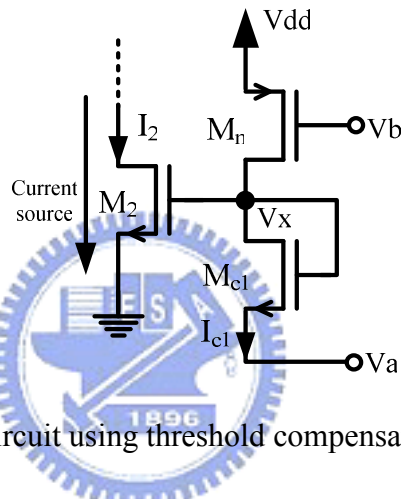
Figure 6.3 bias circuit using threshold compensation technique
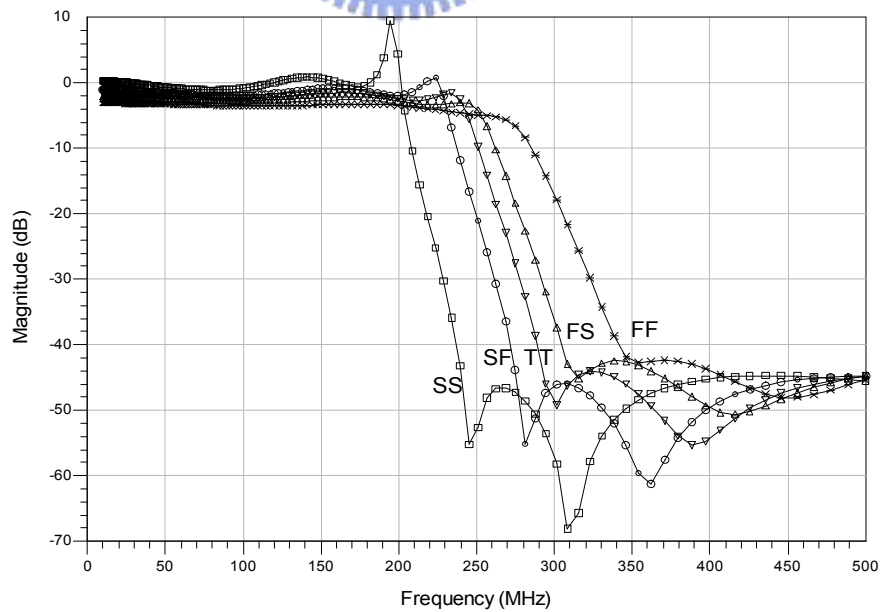
Figure 6.4 the filter magnitude response with four transistor corner cases
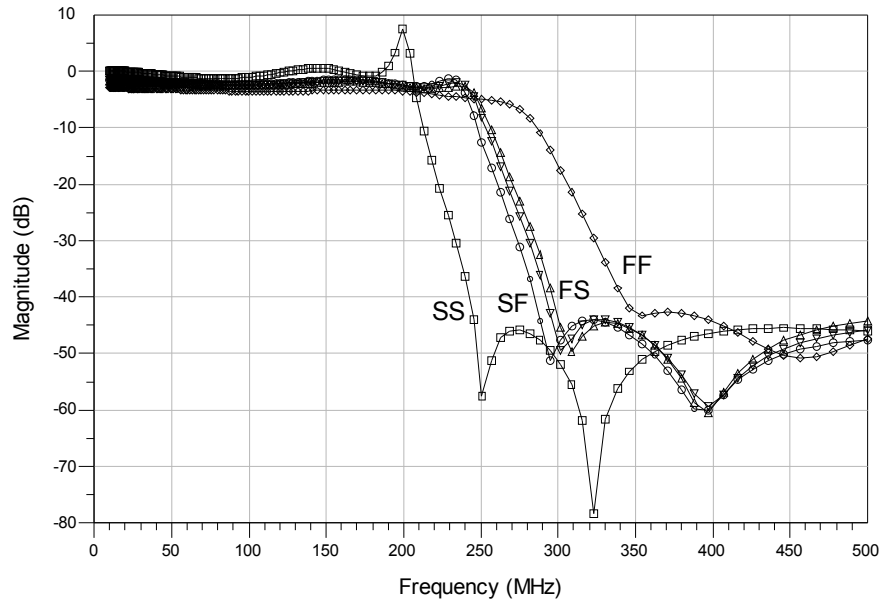
Figure 6.5 after adding voltage threshold compensation biasing circuit

If we consider the four transistor corner cases the cutoff frequency will vary from

200MHz (SS) to 270MHz (FF) as shown in Figure 6.4. After adding voltage threshold

compensation biasing circuit, the SF & FS cases will be restrained in Figure 6.5. The

implementation of this bias skill or other tuning networks will be in the Future works.

The LC ladder topology can be used as broadband matching. The original method of LC

ladder filter depends on the input / output impedance as shown in Figure 6.6. The synthesis

steps are to match input impedance to output impedance. If the LC filter load impedance is the

circuit input like Distributed Amplifier (DA), the difference of is that the DA input impedance

would change with frequency. The principle of broadband matching can make the DA input

equal to source impedance with a wide frequency range. The theory of broadband matching

may not suit for receiver for the lack of NF optimization and detail analysis can be found in

[19].

(a)General filter   (b)Broadband matching
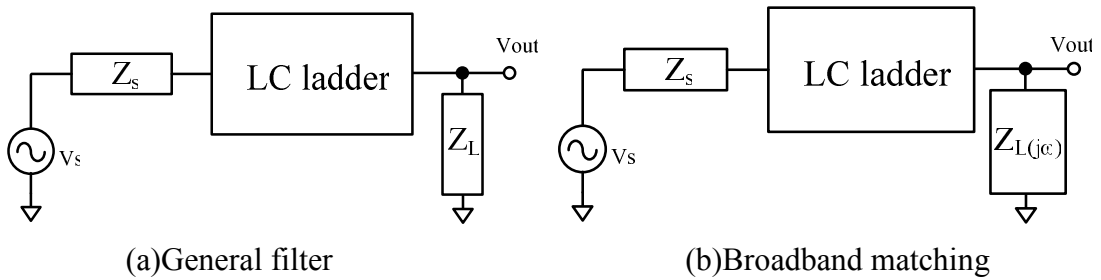
Figure 6.6 LC ladder can be used to match complex load

For high frequency applications, all the Gm blocks have to be implemented with high

output impedance and high quality factor. Since the negative impedance load can increase

differential gain and make common mode gain less than one, besides it doesn't cost additional

power. If the Gm block have RHP-zero about one hundred times higher than the most high

frequency pole or zero, adding negative impedance to other Gm is suitable for high frequency

filter.

Appendix A

Symmetric & Un-symmetric Differential Pair

The cross-coupled quad cell can be shown in Figure A.1. Assume all the MOSFET are in

the saturation region and neglect body effect. The square-law function can be characterized

as:

$$I_D = k(V_{GS} - V_{th})^2 \qquad\qquad (A.1)$$

Figure A.1 Cross-coupled quad cell

Neglect channel length modulation and second-order effects in this analysis, the pair M1

and M2 in Figure A.1 can has relation as:

$$v_p - v_n = \sqrt{\frac{I_{D1}}{k}} - \sqrt{\frac{I_{D2}}{nk}} \tag{A.2}$$

Squaring the two sides of (A.2) and for the relation that $I_{D1}+I_{D2} = (n+1)I$, then (A.2) becomes:
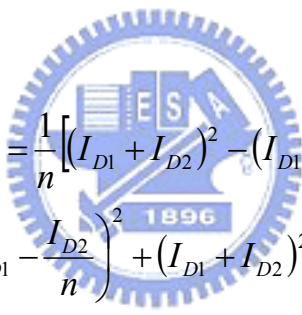
$$(v_p - v_n)^2 = \left(\sqrt{\frac{I_{D1}}{k}} - \sqrt{\frac{I_{D2}}{nk}}\right)^2 = \frac{I_{D1}}{k} - \frac{2}{k}\sqrt{\frac{I_{D1}I_{D2}}{n}} + \frac{I_{D2}}{nk} \tag{A.3}$$

After some arrangements for (A.2):

$$k(v_p - v_n)^2 - I_{D1} - \frac{I_{D2}}{n} = -2\sqrt{\frac{I_{D1}I_{D2}}{n}} \tag{A.4}$$

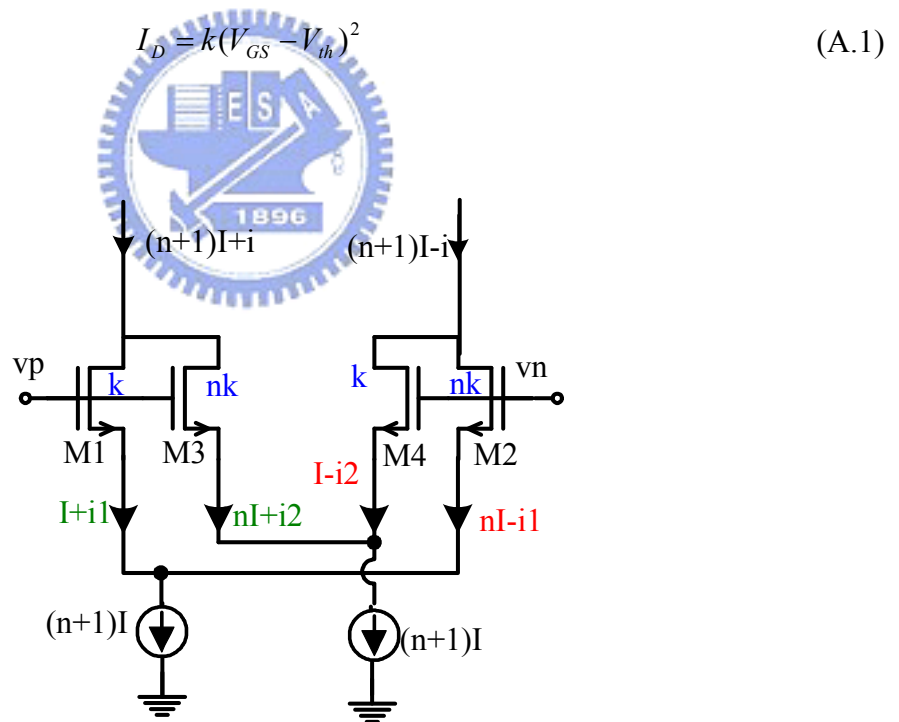Squaring the two sides of equation (A.4), and recognizing that $I_{D1}+I_{D2} = (n+1)I$, $v = (v_p-v_n)$.

(A.4) can be obtained:

$$(kv^2 - I_{D1} - \frac{I_{D2}}{n})^2 = 4\frac{I_{D1}I_{D2}}{n} = \frac{1}{n}\left[(I_{D1}+I_{D2})^2 - (I_{D1}-I_{D2})^2\right]$$

$$\Rightarrow (I_{D1} - I_{D2})^2 = -n\left(kv^2 - I_{D1} - \frac{I_{D2}}{n}\right)^2 + (I_{D1}+I_{D2})^2 \quad , I_{D1} = I+i_1, I_{D2} = nI-i_1$$

$$\Rightarrow (I+i_1 - nI+i_1)^2 = [(1-n)I + 2i_1]^2 = -n\left[kv^2 - I - i_1 - \frac{nI-i_1}{n}\right]^2 + (I+i_1 + nI-i_1)^2$$

$$= \frac{-n(knv^2 - nI - ni_1 - nI + i_1)^2}{n^2} + (1+n)^2 I^2$$

$$\Rightarrow (1-n)^2 I^2 + 4(1-n)I \cdot i_1 + 4i_1^2 = \frac{-[n(kv^2 - 2I) + i_1(1-n)]^2}{n} + (1+n)^2 I^2$$

$$\therefore 4(1-n)I \cdot i_1 + 4i_1^2 = 4nI^2 - \frac{n^2(kv^2 - 2I)^2 + 2n(kv^2 - 2I)\cdot i_1(1-n) + i_1^2(1-n)^2}{n} \tag{A.5}$$

After calculating (A.5):

$$\left[4+\frac{(1-n)^2}{n}\right]i_1^{\,2}+(1-n)\big[4I+2(kv^2-2I)\big]\cdot i_1=4nI^2-n(kv^2-2I)^2$$

$$\Rightarrow\left[\frac{(1+n)^2}{n}\right]i_1^{\,2}+(1-n)\big[2(kv^2)\big]\cdot i_1=4nI^2-n(k^2v^4-4kv^2I+4I^2) \qquad\text{(A.6)}$$

Multiply the two sides of (A.6) by $n/(n+1)^2$:

$$i_1^{\,2}+\frac{n(1-n)}{(n+1)^2}(2kv^2)i_1=\frac{4n^2}{(n+1)^2}I^2-\frac{n^2}{(n+1)^2}(k^2v^4-4kv^2I+4I^2)$$

$$\Rightarrow\left[i_1+\frac{n(1-n)kv^2}{(n+1)^2}\right]^2=\frac{n^2(4I^2-k^2v^4+4kv^2I-4I^2)}{(n+1)^2}+\frac{n^2(1-n)^2k^2v^4}{(n+1)^4}$$

$$\therefore i_1-\frac{n(n-1)kv^2}{(n+1)^2}=\sqrt{\frac{n^2(4kv^2I-k^2v^4)}{(n+1)^2}+\frac{n^2(1-n)^2k^2v^4}{(n+1)^4}}$$

$$\Rightarrow i_1=\frac{n(n-1)kv^2}{(n+1)^2}+\frac{n}{n+1}\sqrt{kv^2\left(4I-kv^2+\frac{(1-n)^2kv^2}{(n+1)^2}\right)}$$

$$\Rightarrow\frac{i_1}{I}=\frac{n(n-1)}{(n+1)^2}\frac{v^2}{\frac{I}{k}}+\frac{n}{n+1}\frac{v\sqrt{k}}{\sqrt{I}}\sqrt{4-\frac{v^2}{\frac{I}{k}}+\frac{(1-n)^2}{(n+1)^2}\frac{v^2}{\frac{I}{k}}} \qquad\text{(A.7)}$$

Let $x=v/\sqrt{(I/k)}$, $\gamma=[n(n-1)]/(n+1)^2$, (A.7) can be shown as:

$$\frac{i_1}{I}=\gamma x^2+\frac{n}{n+1}x\sqrt{4-x^2+\frac{(1-n)^2}{(n+1)^2}x^2}$$

$$=\gamma x^2+\frac{4n}{2(n+1)}x\sqrt{1-\frac{1}{4}x^2(1-\frac{(1-n)^2}{(n+1)^2})},\quad let\quad \alpha=\frac{4n}{(n+1)}$$

$$=\gamma x^2+\frac{\alpha}{2}x\sqrt{1-\frac{1}{4}x^2\left(\frac{(n^2+2n+1-1+2n-n^2)}{(n+1)^2}\right)}$$

$$=\gamma x^2+\frac{\alpha}{2}x\sqrt{1-\frac{1}{4}x^2\frac{4n}{(n+1)^2}},\quad let\quad \beta=\frac{n}{(n+1)^2}$$

$$=\gamma x^2+\frac{\alpha}{2}x\sqrt{1-\beta x^2}\equiv y_1$$

$$\text{(A.8)}$$

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For the same reason, we can deduce that:

$$\frac{i_2}{I} = -\gamma x^2 + \frac{\alpha}{2} x\sqrt{1-\beta x^2} \equiv y_2$$

$$i = i_1 + i_2 \Rightarrow y = \frac{i}{I} = \frac{i_1 + i_2}{I} = y_1 + y_2 = \alpha x\sqrt{1-\beta x^2} \qquad \text{(A.9)}$$

If the input signal level increases, M1 will first enter into cut-off region, that is,

$$I_{D1} = I + i_1 = 0$$

$$\therefore i_1 = -I \qquad y_1 = \frac{i_1}{I} = -1$$

$$I_{D2} = nI - i_1 = (n+1)I \Rightarrow kv^2 = \frac{(n+1)I}{n} \Rightarrow \frac{v^2}{\frac{I}{k}} = \frac{(n+1)}{n} \Rightarrow x = -\sqrt{\frac{(n+1)}{n}}$$

$$\therefore y_1 = -1 \qquad \text{for} \quad x < -\sqrt{\frac{n+1}{n}}$$

$$y = -1 - rx^2 + \frac{\alpha}{2} x\sqrt{1-\beta x^2} \qquad \text{for} \quad x < -\sqrt{\frac{n+1}{n}} \qquad \text{(A.10)}$$

The input signal level continues to increase, M2 will also cut-off.

$$I_{D2} = nI - i_1 = 0 \qquad I_{D1} = (n+1)I$$

$$\because (I_{D1} - I_{D2})^2 = -n\left(kv^2 - I_{D1} - \frac{I_{D2}}{n}\right)^2 + (I_{D1} + I_{D2})^2$$

$$\Rightarrow kv^2 = I_{D1} = (n+1)I \Rightarrow \frac{v^2}{\frac{I}{k}} = n+1 \Rightarrow x = -\sqrt{n+1}$$

$$\text{(A.11)}$$

From the above analysis, we can calculate the bounded value of y_1 and y_2 as following

shows.

$$y_{12} = \begin{cases} \alpha x\sqrt{1-\beta x^2}, & \text{for} \quad |x| \le \sqrt{\frac{n+1}{n}} \\[2ex] \left(1 + rx^2 + \frac{\alpha}{2} x\sqrt{1-\beta x^2}\right)\mathrm{sgn}(x), & \text{for} \quad \sqrt{\frac{n+1}{n}} < |x| \le \sqrt{n+1} \\[2ex] (n+1)\mathrm{sgn}(x), & \text{for} \quad |x| > \sqrt{n+1} \end{cases}$$

$$\text{(A.12)}$$

Having (A.12) we can determine large-signal transconductance characteristic g_{m12} by straight forward differentiation.

$$g_{m12} = \begin{cases} \alpha \dfrac{1-2\beta x^2}{\sqrt{1-\beta x^2}}, & for \quad |x| \le \sqrt{\dfrac{n+1}{n}} \\ 2rx + \dfrac{\alpha}{2} \dfrac{1-2\beta x^2}{\sqrt{1-\beta x^2}}, & for \quad \sqrt{\dfrac{n+1}{n}} < |x| \le \sqrt{n+1} \\ 0, & for \quad |x| > \sqrt{n+1} \end{cases}$$

(A.13)

A substantial increase in linearity of CMOS OTA can be obtained by using two unsymmetrical and one symmetrical differential pair as shown in Figure A.2. By proper adding and subtracting output currents in input stage, approximate cancellation of the remaining nonlinearities can be obtained.
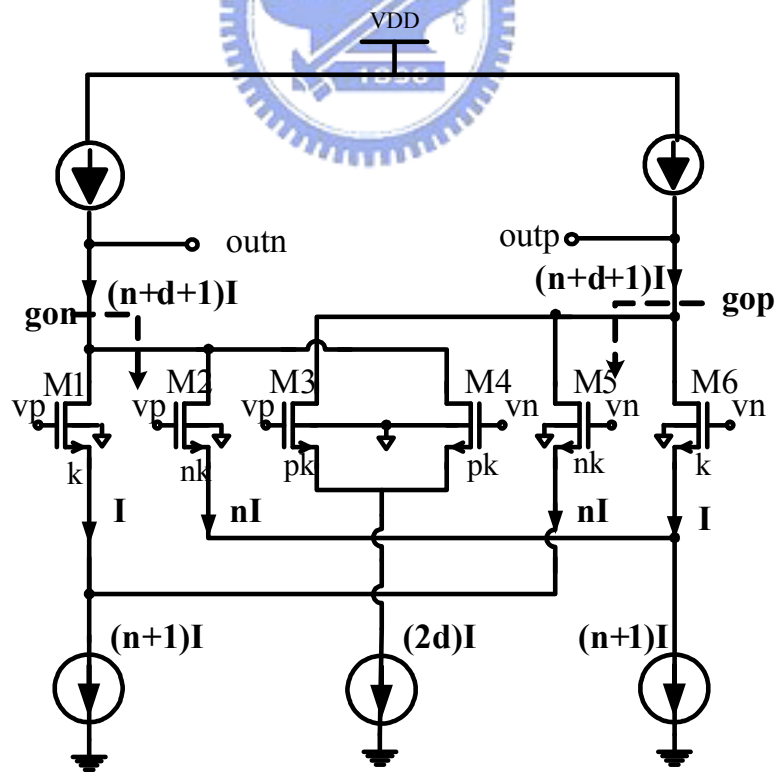

Figure A.2   Symmetric & un-symmetric differential pair

The calculation can be easily to obtain the normalized transfer function y_d of

symmetrical differential pair, which is listed below:

$$y_d = \begin{cases} x\sqrt{p(d - \dfrac{px^2}{4})}, & for \quad |x| \le \sqrt{\dfrac{2d}{p}} \\ d\,sgn(x), & for \quad |x| > \sqrt{\dfrac{2d}{p}} \end{cases}$$

(A.14)

Determine the normalized transconductance characteristic g_{md} from y_d :

$$g_{md} = \begin{cases} \sqrt{p} \cdot \dfrac{d - \dfrac{px^2}{2}}{\sqrt{d - \dfrac{px^2}{4}}}, & for \quad |x| \le \sqrt{\dfrac{2d}{p}} \\ 0, & for \quad |x| > \sqrt{\dfrac{2d}{p}} \end{cases}$$

(A.15)

The normalized transfer characteristic of the OTA is $y(x)=y_{12}(x)-y_d(x)$. Respective

transconductance characteristic is $g_m(x)=g_{m12}(x)-g_{md}(x)$. The final goal is to make y(x) as

linear as possible, which is equivalent to making $g_m(x)$ as flat as possible. According to

equation (A.13) and (A.15), g_m is fully determined by the three parameters: n, d and p. Thus,

we can impose three conditions upon the characteristics g_{m12} and g_{md} in order to determine

uniquely the values of n, d and p.

According to the normalized transfer characteristic, we have the following assumptions [5]:

1. The value of parameter n has to be chosen in such a way that g_{m12} is constant in the right neighborhood of $x=[(n+1)/n]^{0.5}$

2. The values of d and p have to be chosen in such a way that $g_{md}(x)$ vanished exactly for $x=\pm[(n+1)/n]^{0.5}$

3. The values of d and p have to be chosen in such a way that $g_{md}(0) = g_{m12}(0) - g_{m12}([(n+1)/n]^{0.5})$.

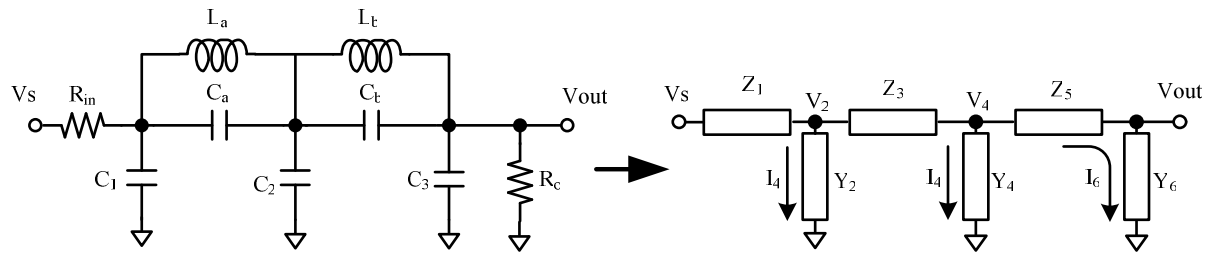From the three assumptions, we can uniquely determining the values of n, p and d as shown in table A.1.

Table A.1   OTA design parameters

n	p	d
4.236	1.288	0.796

Appendix B

LC Ladder analysis

Where $Y_{2,4} = sC_{1,2}$, $Y_6 = \dfrac{1}{R_o} + sC_5$, $Z_{3,5} = \dfrac{sL_{a,b}}{s^2 L_{a,b} C_{a,b} + 1}$

Assume no current flows from the output node. The circuit can be analyzed by using

KCL & KVL:

$$I_6 = V_{out} Y_6$$

$$V_4 = I_6 \times Z_5 + V_{out}$$

$$I_3 = V_4 \times Y_4 + I_6 = Y_4 \times V_{out} \times (1 + Z_5 Y_6) + V_{out} Y_6$$

$$V_2 = I_3 \times Z_3 + V_4$$

$$\begin{aligned}
I_1 &= V_2 \times Y_2 + I_3 = Y_2 \times [I_3 \times Z_3 + V_4] + Y_4 \times V_{out} \times (1 + Z_5 Y_6) + V_{out} \times Y_6 \\
&= Y_2 \times \{Z_3 \times [Y_4 \times V_{out} \times (1 + Z_5 Y_6) + V_{out} Y_6] + V_{out} \times (1 + Z_5 Y_6)\} \qquad \text{…….…………} (1) \\
&\quad + Y_4 \times V_{out} \times (1 + Z_5 Y_6) + V_{out} \times Y_6
\end{aligned}$$

$$Vs = I_1 \times Z_1 + V_2 \qquad \text{………………………………………………………...} (2)$$

From (1) & (2):

$$Vs = I_1 \times Z_1 + I_3 \times Z_3 + V_4$$
$$= I_1 \times Z_1 + I_3 \times Z_3 + I_6 \times Z_5 + V_{out}$$
$$= Z_1 \times \{Y_2 \times \{Z_3 \times [Y_4 \times V_{out} \times (1 + Z_5 Y_6) + V_{out} Y_6] + V_{out} \times (1 + Z_5 Y_6)\}$$
$$+ Y_4 \times V_{out} \times (1 + Z_5 Y_6) + V_{out} \times Y_6\}$$
$$+ Z_3 \times \{Y_4 \times V_{out} \times (1 + Z_5 Y_6) + V_{out} Y_6\}$$
$$+ Z_5 \times V_{out} Y_6$$
$$+ V_{out}$$

Replace all the Zi & Yi with real element

$$\frac{Vs}{V_{out}} = 1 + Z_1(Y_2 + Y_4 + Y_6) + Z_3(Y_4 + Y_6) + Z_5 Y_6 + Z_1 Y_2 Z_3(Y_4 + Y_6)$$
$$+ Z_5 Y_6(Z_1 Y_4 + Z_1 Y_2 + Z_3 Y_4) + Z_1 Y_2 Z_3 Y_4 Z_5 Y_6$$
$$= 1 + Rin \times (sC_1 + sC_2 + sC_3 + \frac{1}{Ro}) + \frac{sLa}{s^2 LaCa + 1}(sC_2 + sC_3 + \frac{1}{Ro})$$
$$+ Rin \times sC_1 \frac{sLb}{s^2 LbCb + 1}(sC_3 + \frac{1}{Ro}) + RinsC_1 \frac{sLa}{s^2 LaCa + 1}(sC_2 + sC_3 + \frac{1}{Ro})$$
$$+ Rin \times s^2 C_1 C_2 (\frac{sLa}{s^2 LaCa + 1})(\frac{sLb}{s^2 LbCb + 1})(sC_3 + \frac{1}{Ro})$$
$$+ \frac{sLb}{s^2 LbCb + 1}(Rin \times sC_2 + Rin \times sC_1 + sC_2 \frac{sLa}{s^2 LaCa + 1})(sC_3 + \frac{1}{Ro})$$
$$= (\frac{1}{s^2 LaCa + 1})(\frac{1}{s^2 LbCb + 1}) \times \{$$
$$[s^4 LaLbCaCb + s^2(LaCa + LbCb) + 1] \times (1 + sRinC_1 + sRinC_2 + sRinC_3 + \frac{Rin}{Ro}) .... (a)$$
$$+ (s2LbCb + 1) \times sLa \times [sC_2 + sC_3 + \frac{1}{Ro} + sRinC_1(sC_2 + sC_3 + \frac{1}{Ro})] .... (b)$$
$$+ (s2LaCa + 1) \times sLb \times (sC3 + \frac{1}{Ro})(1 + sRinC_1 + sRinC_2 + \frac{s^2 C_2 La}{s^2 LaCa + 1}) .... (c)$$
$$+ Rin \times sLa \times sLb \times sC_1 \times sC_2(sC_3 + \frac{1}{Ro})\} .... (d)$$

calculate (a):

$$(a) = [s^4 LaLbCaCb + s^2(LaCa + LbCb) + 1] \times (1 + sRinC_1 + sRinC_2 + sRinC_3 + \frac{Rin}{Ro})$$

$$= s^5 CaCbLaLb(RinC_1 + RinC_2 + RinC_3) + s^4 CaCbLaLb(1 + \frac{Rin}{Ro})$$

$$+ s^3(CaLa + CbLb)(RinC_1 + RinC_2 + RinC_3) + s^2(CaLa + CbLb)(1 + \frac{Rin}{Ro})$$

$$+ s(RinC_1 + RinC_2 + RinC_3) + \frac{Rin}{Ro} + 1$$

calculate (b):

$$(b) = (s2LbCb + 1) \times sLa \times [sC_2 + sC_3 + \frac{1}{Ro} + sRinC_1(sC_2 + sC_3 + \frac{1}{Ro})]$$

$$= s^5 RinC_1 CbLaLb(C_2 + C_3) + s^4 CbLaLb(C_2 + C_3 + \frac{RinC_1}{Ro})$$

$$+ s^3 La(RinC_1 C_2 + RinC_1 C_3 + \frac{CbLb}{Ro}) + s^2 La(C_2 + C_3 + \frac{RinC_1}{Ro})$$

$$+ s\frac{La}{Ro}$$

calculate (c):

$$(c) = (s2LaCa + 1) \times sLb \times (sC3 + \frac{1}{Ro})(1 + sRinC_1 + sRinC_2 + \frac{s^2 C_2 La}{s^2 LaCa + 1})$$

$$= s^5(RinC_1 C_3 CaLaLb + RinC_2 C_3 CaLaLb)$$

$$+ s^4(C_2 C_3 LaLb + C_3 CaLaLb + \frac{RinC_2 CaLaLb}{Ro} + \frac{RinC_1 CaLaLb}{Ro})$$

$$+ s^3(RinC_1 C_3 Lb + RinC_2 C_3 Lb + \frac{CaLaLb}{Ro} + \frac{C_2 LaLb}{Ro})$$

$$+ s^2(C_3 Lb + \frac{RinC_1 Lb}{Ro} + \frac{RinC_2 Lb}{Ro})$$

$$+ s\frac{Lb}{Ro}$$

calculate (d):

$$(d) = Rin \times sLa \times sLb \times sC_1 \times sC_2(sC_3 + \frac{1}{Ro})$$

$$= s^5 RinC_1 C_2 C_3 LaLb + s^4 \frac{RinC_1 C_2 LaLb}{Ro}$$

Add (a) ~ (b):

$$\frac{Vs}{V_{out}} = (\frac{1}{s^2 LaCa + 1})(\frac{1}{s^2 LbCb + 1}) \times$$

$$\{$$

$$s^5 \times (RinC_1C_2C_3LaLb + RinC_1C_3CaLaLb + RinC_2C_3CaLaLb + RinC_1C_2CbLaLb +$$
$$RinC_1C_3CbLaLb + RinC_1CaCbLaLb + RinC_2CaCbLaLb + RinC_3CaCbLaLb)$$

$$+ s^4 \times (\frac{RinC_1C_2LaLb}{Ro} + C_2C_3LaLb + C_3CaLaLb + \frac{RinC_2CaLaLb}{Ro} + \frac{RinC_1CaLaLb}{Ro} +$$
$$C_2CbLaLb + C_3CbLaLb + \frac{RinC_1CbLaLb}{Ro} + CaCbLaLb + \frac{RinCaCbLaLb}{Ro})$$

$$+ s^3 \times (RinC_1C_3Lb + RinC_2C_3Lb + \frac{CaLaLb}{Ro} + \frac{C_2LaLb}{Ro} + RinC_1C_2La +$$
$$RinC_1C_3La + \frac{LaCbLb}{Ro} + RinC_1CaLa + RinC_1CbLb + RinC_2CaLa +$$
$$RinC_2CbLb + RinC_3CaLa + RinC_3CbLb)$$

$$+ s^2 \times (C_3Lb + \frac{RinC_1Lb}{Ro} + \frac{RinC_2Lb}{Ro} + C_2La + C_3La + \frac{RinC_1La}{Ro} +$$
$$CaLa + CbLb + \frac{RinCaLa}{Ro} + \frac{RinCbLb}{Ro})$$

$$+ s^1 \times (\frac{Lb}{Ro} + \frac{La}{Ro} + RinC_1 + RinC_2 + RinC_3)$$
$$+ \frac{Rin}{Ro} + 1$$
$$\}$$

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論文題目： A High Speed Fifth Order Gm-C Filter For Ultra-wideband Wireless Applications

　　　　 適用於超寬頻無線通訊之高速五階轉導-電容濾波器設計