Temperature Effect on Ku-Band Current-Reused Common-Gate LNA in 0.13-μm CMOS Technology

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***Abstract*—This paper presents the temperature effect on a Ku-band NMOS common-gate low-noise amplifier (CG-LNA). The temperature characteristics of an NMOS transistor and spiral inductors are obtained over the temperature range from 253 to 393 K. These results show that the optimal bias condition minimizes the transconductance and drain current temperature variations. Based on these results, a current-reused CG-LNA with good temperature performance is designed. At ambient temperatures, the CG-LNA has a measured power gain of 10.3 dB and a noise figure (NF) of 4.3 dB at 15.2 GHz, while consuming 4.5 mA from a 1.3-V power supply. When the temperature varies from 253 to 393 K, the CG-LNA has a power gain variation of 3 dB, NF variation of 2 dB, and dc power consumption variation of 11.9%. This paper is the first to report the temperature effect on Ku-band CG-LNAs.**

***Index Terms*—CMOS, common gate, current reuse, low-noise amplifier (LNA), zero temperature coefficient.**

I. INTRODUCTION

DEEP-SUBMICROMETER CMOS technology offers a promising solution for highly integrated transceivers in emerging microwave and millimeter-wave broadband wireless communications. An essential design consideration in the above transceivers is to maintain the required performance over a wide range of temperatures. In the literature, only a few studies address this problem on the common-source low-noise amplifier (CS-LNA) configuration [1], [2]. Kaamouchi *et al.* evaluated the 2.4-GHz CS-LNA in 0.13-μm silicon-on-insulator (SOI) CMOS technology over a temperature range from 298 to 473 K [1]. If the transistor is properly biased at the zero-temperature-coefficient point of transconductance (ZTC_{gm}), the measured power gain variation in that study is 0.9 dB and noise figure (NF) variation is 2.3 dB over a 175-K temperature range. Another study reports an SiGe BiCMOS CS-LNA at 5.5 GHz having a power gain variation of 0.4 dB and an NF variation of 0.5 dB from 273 to 373 K by incorporating a proportional-to-absolute temperature compensation circuit [2].

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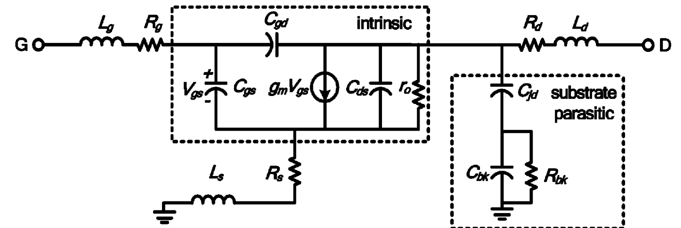

Fig. 1. Small-signal model of NMOSFET.

Recent research highlights the advantages of the common-gate low-noise amplifier (CG-LNA) for microwave and millimeter-wave applications because of its susceptibility to process tolerance [3], [4]. However, the performance variation of this CG-LNA due to the temperature effect has not been explored. This paper, therefore, designs an NMOS LNA with the stacked common-gate topology. Section II investigates the temperature variations of the NMOS transistor and spiral inductor. Section III then designs a CG-LNA to evaluate the temperature effect on circuit performance. Section IV describes the measured results. Finally, Section V provides a conclusion.

II. TEMPERATURE EFFECT ON NMOSFET AND SPIRAL INDUCTOR DEVICE CHARACTERISTICS

A. NMOS Transistor

The threshold voltage and carrier mobility strongly vary with temperature in NMOS transistors. This, in turn, results in the pronounced temperature dependence of the transconductance and noise parameter. To examine the temperature-dependence effect, this paper uses an NMOS transistor with a total gatewidth of 57.6 μm and gate-length of 0.12 μm for testing. A small-signal model including the substrate parasitic [5] is selected for device characterization, as Fig. 1 shows. In this model, the intrinsic elements include g_m, r_o, C_{ds}, C_{gs} and C_{gd}. R_g, L_g, R_s, L_s, R_d and L_d represent the extrinsic elements and C_{jd}, C_{bk} and R_{bk} represent the substrate parasitic.

1) Zero-Temperature-Coefficient Biases: Fig. 2(a) illustrates the measured drain current versus V_{gs} over the temperature range from 253 to 393 K. When V_{gs} is less than 0.3 V, the drain current varies strongly with temperature. The drain current

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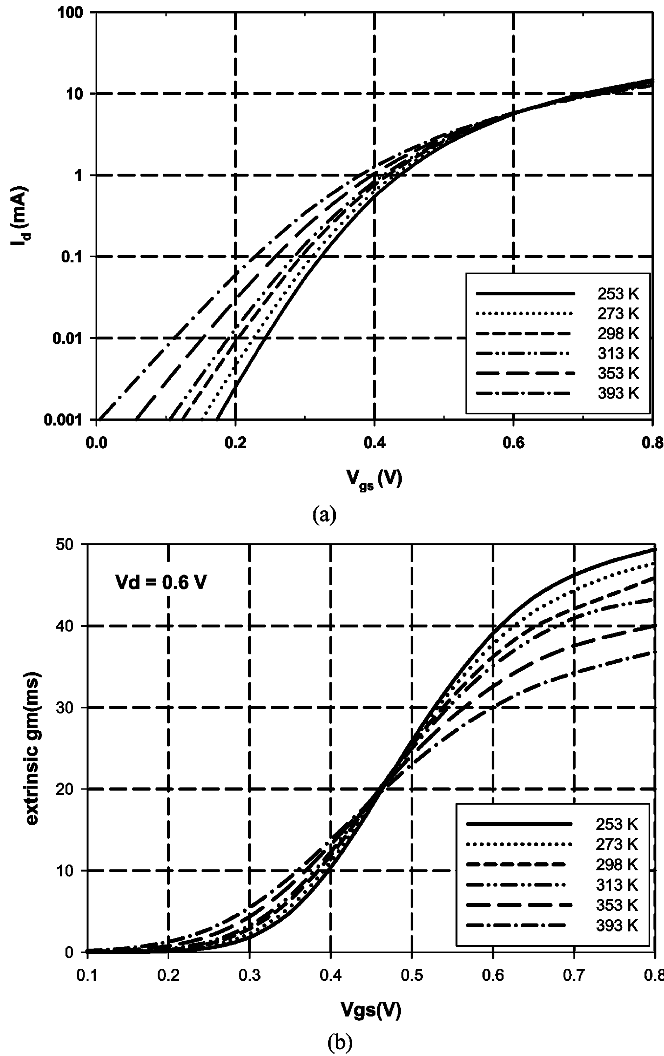


Fig. 2. Measured: (a) I_d–$V_{\rm gs}$ and (b) g_m–$V_{\rm gs}$ relationship in the temperature range from 253 to 393 K.

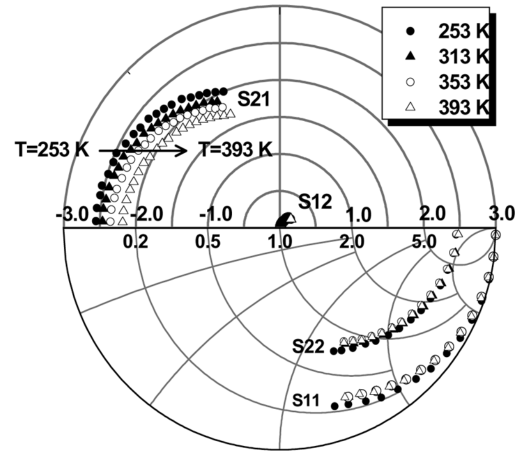


Fig. 3. Measured S-parameters of the NMOS transistor from 0.5 to 20 GHz.

becomes almost unchanged with temperature when $V_{\rm gs}$ equals 0.62 V. This bias condition is the zero temperature coefficient point of the drain current $({\rm ZTC}_{id})$. When the NMOS transistor is biased at ${\rm ZTC}_{id}$, the drain current exhibits negligible temperature variation.

By differentiating i_d with respect to $V_{\rm gs}$, the temperature dependence of the extrinsic transconductance is obtained, as indicated in Fig. 2(b). This shows that g_m variation with temperature nearly disappears at $V_{\rm gs} = 0.46$ V. This particular bias point is called the zero-temperature-coefficient point of transconductance $({\rm ZTC}_{gm})$.

To compromise between the temperature variation of drain current and transconductance, the bias condition of an NMOS transistor is generally chosen between ${\rm ZTC}_{id}$ and ${\rm ZTC}_{gm}$. This paper selects a gate bias of $V_{\rm gs} = 0.5$ V, which leads to $\Delta g_m =$ 3 mS and $\Delta i_d = 0.9$ mA over 253–393 K.

2) Element Extraction: The authors of [5]–[7] used element extraction methods to extract the small-signal elements based on the measured scattering parameters. First, the on-wafer measurement of the NMOS transistor biased at $V_{\rm gs} = 0.5$ V and $V_{\rm ds} = 0.6$ V was performed at various temperatures from 253 to 393 K to obtain the scattering parameters from 0.5 to 20 GHz, as shown in Fig. 3. Based on these results, the extraction procedure was performed to obtain the extrinsic and substrate parasitic elements and then the intrinsic elements. This procedure was repeatedly performed at each temperature of 253, 313, 353, and 393 K.

The extrinsic and substrate parasitic elements are $R_g = 2.6\ \Omega$, $L_g = 15.3$ pH, $R_s = 1.2\ \Omega$, $L_s = 45.2$ pH, $R_d = 1.5\ \Omega$, $L_d = 75$ pH, $C_{jd} = 27$ fF, $C_{bk} = 11.6$ fF, and $R_{bk} = 1.25$ kΩ at ambient temperature. Fig. 4 shows that intrinsic capacitors also vary slightly with temperature, which are $C_{\rm ds} \approx 20$ fF, $C_{\rm gs} \approx 55$ fF, and $C_{\rm gd} \approx 24$ fF. Compared to the above weakly temperature-varying elements, the intrinsic g_m and r_o have relatively greater temperature variation, where the intrinsic g_m varies from 29.2 to 25.3 mS (-13.7% variation) and r_o increases from 316 to 336 Ω ($+6.3\%$ variation) from 253 to 393 K.

B. Spiral Inductor

In addition to the NMOS transistor device, the passive spiral inductor is also affected by temperature [1]. Fig. 5 shows the variation of the quality factor with temperature for 2.5- and 1.68-nH spiral inductors in 0.13-μm CMOS technology. These inductors are laid out on an M8 layer with 3.5/2.5 turns of the metal line, having a 2-μm thickness, 6-μm linewidth, and 2-μm line spacing. The measurement results in Fig. 5 indicate that the quality factor decreases when temperature increases. At 15 GHz, the quality factor of the 2.5-nH inductor decreases from 17.2 to 9.3 and the 1.68-nH inductor decreases from 16.7 to 10.7 over 253–393 K. These experiment results shows that there is no apparent inductance change over the temperature range. This implies that the quality factor is primarily degraded by increasing parasitical resistance.

III. Design of Current-Reused CG-LNA

Fig. 6(a) shows that a CG-LNA is composed of two common-gate NMOS transistors, which are stacked together for sharing

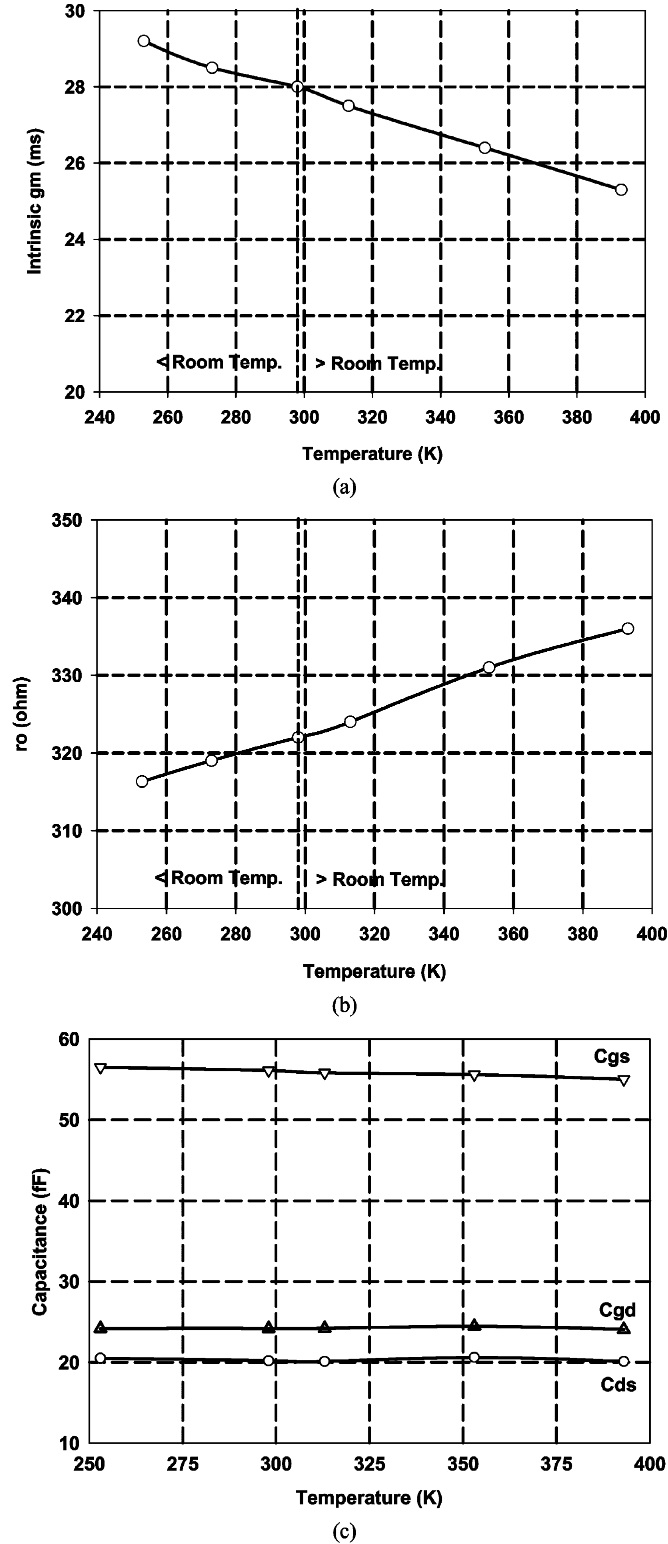


Fig. 4. Temperature dependence of the intrinsic elements: transconductance, output resistance, and parasitic capacitances ($V\text{gs} = 0.5$ and $V\text{ds} = 0.6$ V).

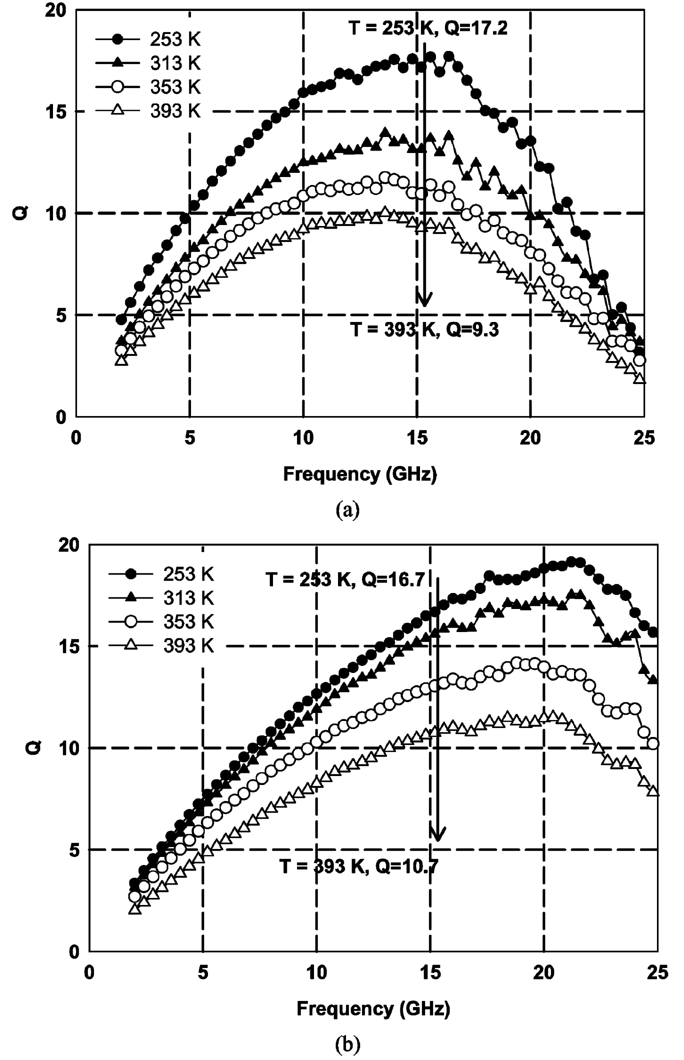


Fig. 5. Measured quality factor of the spiral inductor. (a) 2.5 nH. (b) 1.68 nH.

the same dc current to reduce the dc power consumption. As in Section II, the intrinsic capacitances C_{ds} and C_{gd} are small enough that the small-signal model of the CG-LNA can be simplified to Fig. 6(b).

A. Circuit Design

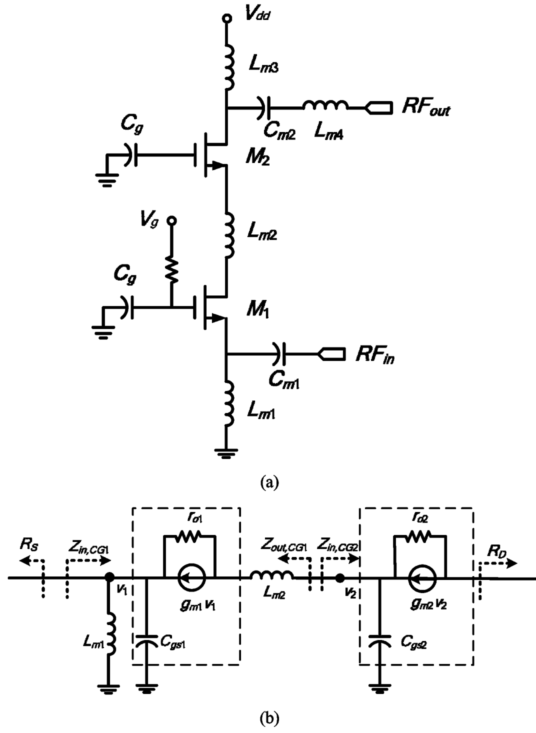
As in Section II, the gate bias voltage is set at $V_{\text{gs}} = 0.5$ V for minimal temperature variation of the transconductance and the drain current. As pointed out in [3], the coupling effect between the channel and gate becomes important at high frequencies, and may deteriorate the gain and noise performance. This effect is included in the gate conductance g_g [3] as follows:

$$g_g = \frac{\omega^2 C_{\text{gs}}^2}{5 g_{d0}} \tag{1}$$

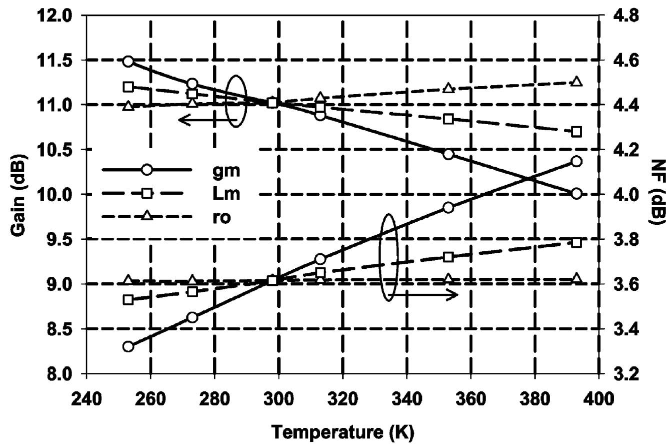
where g_{d0} is the channel conductance at zero drain-to-source voltage. Define $\eta(\omega)$ as the ratio of g_g to the transconductance g_m, i.e., $\eta(\omega) \equiv g_g / g_m$, and it approximates to

$$\eta(\omega) \approx \frac{\alpha}{5} \left(\frac{\omega}{\omega_T} \right)^2. \tag{2}$$

In the equation above, α is the ratio of the transconductance g_m to the channel conductance g_{d0} at zero drain-to-source voltage, and $\omega_T = g_m/(C_{\text{gs}} + C_{\text{gd}})$ is the unity current gain frequency. For the NMOS in question, $\alpha = 0.49$ and



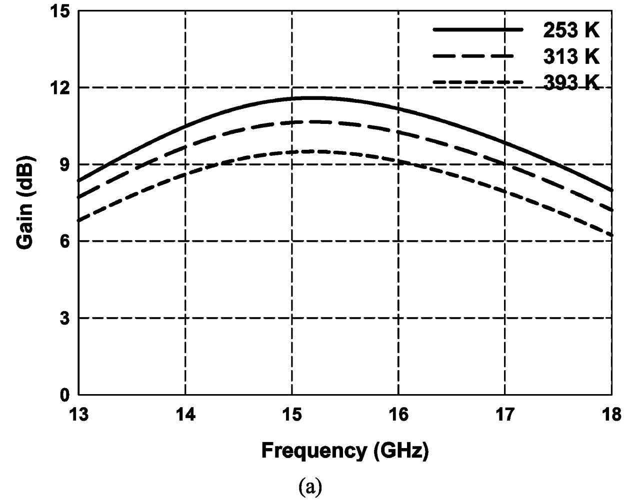
(a)



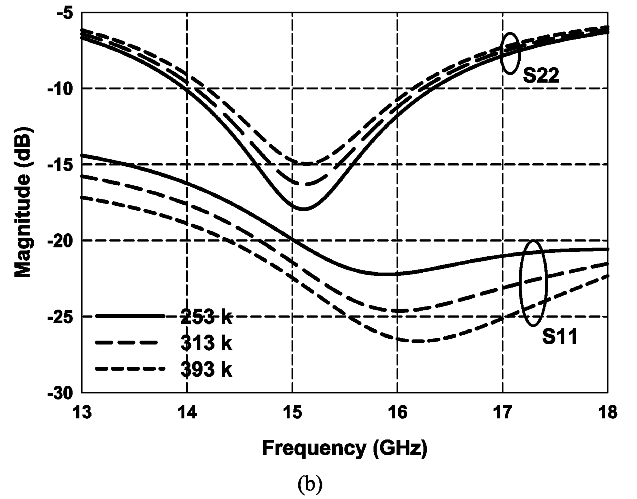
(b)

Fig. 6. Proposed current-reused stacked CG-LNA. (a) Schematic. (b) Small-signal equivalent circuit.

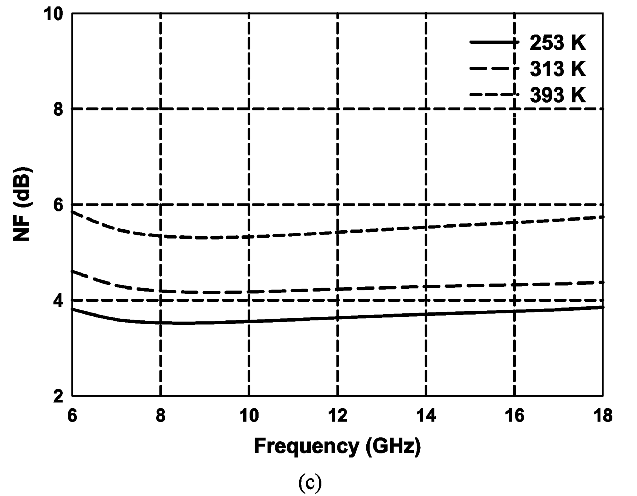
Fig. 7. Effects of the transconductance, output resistance, and matching inductors on gain and NF of the CG-LNA at 15.2 GHz.



(a)



(b)



(c)

Fig. 8. Simulated results of the designed CG-LNA over 253–393 K. (a) Power gain. (b) Return losses. (c) NF.

$f_T = 72$ GHz. Hence, $\eta = 0.0035$ at 15 GHz, implying a negligible channel-gate coupling effect in this case.

By taking into account the gate–source capacitance $C_{\rm gs2}$, the input impedance $Z_{\rm in,CG2}$ of M_2 becomes

$$\begin{aligned} Z_{\rm in,CG2} &= \left[\frac{(r_{o2}+R_D)\,j\omega C_{\rm gs2}+1+g_{m2}r_{o2}}{r_{o2}+R_D}+\eta_2(\omega)g_{m2}\right]^{-1} \\ &\approx \frac{r_{o2}+R_D}{(r_{o2}+R_D)\,j\omega C_{\rm gs2}+1+g_{m2}r_{o2}} \end{aligned} \quad (3)$$

where R_D denotes the impedance at the M_2 drain node. If $(r_{o2}+R_D/1+g_{m2}r_{o2})\omega C_{\rm gs2} \ll 1$, $Z_{\rm in,CG2}$ can be simplified as

$$Z_{\rm in,CG2} \approx \frac{r_{o2}+R_D}{1+g_{m2}r_{o2}} - j\left(\frac{r_{o2}+R_D}{1+g_{m2}r_{o2}}\right)^2 \omega C_{\rm gs2}. \quad (4)$$

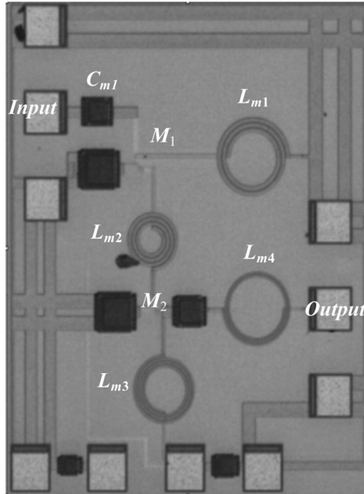


Fig. 9. Microphotograph of the proposed current-reused CG-LNA.

The inductor L_{m1} is added at the M_1 source node to resonate $C_{\rm gs1}$ so that $L_{m1}C_{\rm gs1} = 1/\omega_o^2$. The input impedance of M_1 at ω_o can then be expressed as

$$\begin{aligned} Z_{\rm in,CG1} &= \frac{r_{o1} + \mathrm{Re}\{Z_{\rm in,CG2}\}}{1 + g_{m1}r_{o1}} \\ &\quad + j\frac{\omega_o L_{m2} + \mathrm{Im}\{Z_{\rm in,CG2}\}}{1 + g_{m1}r_{o1}} \\ &= \frac{r_{o1}}{1 + g_{m1}r_{o1}} + \frac{r_{o2} + R_D}{(1 + g_{m1}r_{o1})(1 + g_{m2}r_{o2})} \\ &\quad + j\frac{1}{1 + g_{m1}r_{o1}} \\ &\quad \times \left[\omega_o L_{m2} - \left(\frac{r_{o2} + R_D}{1 + g_{m2}r_{o2}}\right)^2 \omega_o C_{\rm gs2}\right]. \end{aligned} \quad (5)$$

To match $Z_{\rm in,CG1}$ to R_s, L_{m2} must satisfy the following equation:

$$L_{m2} = \left(\frac{r_{o2} + R_D}{1 + g_{m2}r_{o2}}\right)^2 C_{\rm gs2}. \quad (6)$$

Section II shows that $C_{\rm gs}$ is nearly temperature independent and g_m and r_o have the opposite temperature coefficients. Therefore, the determination of inter-stage matching inductance L_{m2} based on (6) is valid for a wide temperature range. In other words, a good return loss can be maintained over 253–393 K.

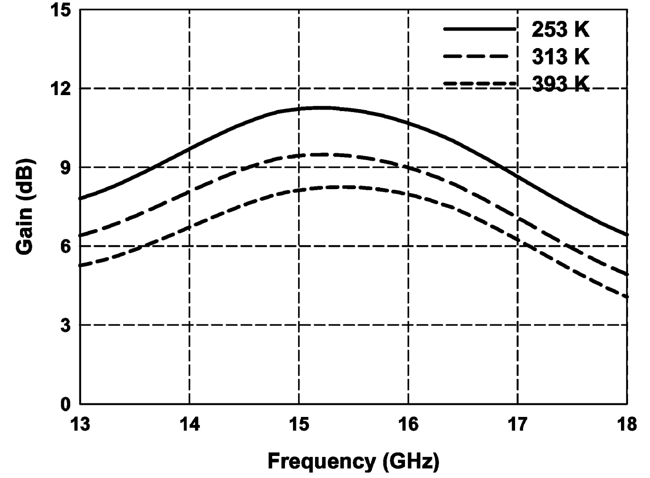
If input is matched, the effective transconductance becomes

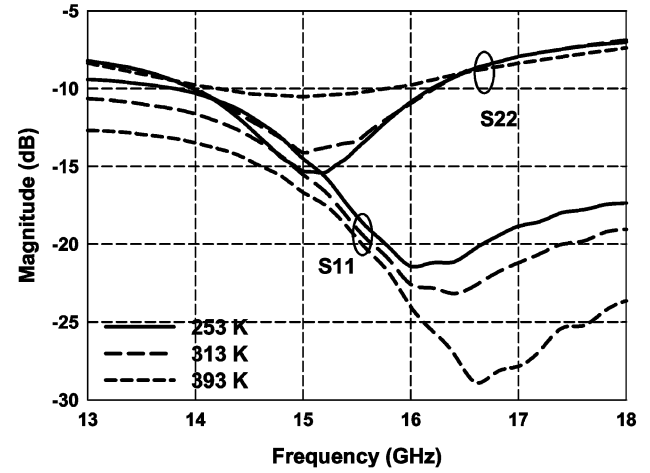
$$g_{m,\rm CG} = \frac{1}{2R_s}\left[1 - g_{m1}R_s\eta_1(\omega_o)\right]. \quad (7)$$

Equation (7) indicates that the temperature variation of LNA gain is dominated by the temperature dependence of g_{m1}. The temperature variation of power gain can be minimized if the bias is carefully designed at the zero-temperature-coefficient point, as discussed in Section II-A.

Regarding noise performance, the noise factor is given by

$$F_{\rm CG} \approx 1 + \frac{\gamma_1}{\alpha_1}\left[\frac{1}{g_{m1}R_s} + \eta_1^2(\omega_o)g_{m1}R_s + 2\eta_1(\omega_o)\right] + \delta_1\eta_1(\omega_o)g_{m1}R_s \quad (8)$$





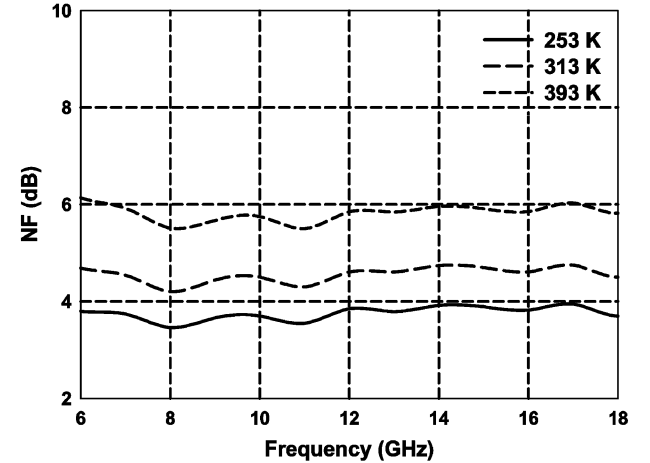


Fig. 10. Measured results of the designed CG-LNA over 253–393 K. (a) Power gain. (b) Return losses. (c) NF.

where γ_1 is the channel thermal noise coefficient and $\gamma_1 \approx 1.2$ from [7]. The bias-dependent coefficients α, γ, and δ are nearly unchanged with temperature because the bias has been properly selected close to the zero-temperature-coefficient point. This also minimizes the temperature effect on the NF.

TABLE I
COMPARISON OF CMOS LNAs

Ref.	Topology/ Tech.	RF frequency (GHz)	Power Gain (dB)	Power Gain Variation (dB) (temp. range)	NF (dB)	NF Variation (dB) (temp. var. range)	DC Consump. (mW)	DC Consum. Variation (mW) (temp. var. range)
[1]	CS/CMOS SOI	2.4	10	9.1 – 10 (298-473 K)	3.4	3.4 - 5.7 (298-473 K)	2.3	2.2 - 3.7 (298-473 K)
[2]	CS/SiGe BiCMOS	5.5	14.1	13.7 - 14.1 (273-373 K)	2.4	2.4 - 2.9 (273-373 K)	11.8	11.8 - 15.8 (273-373 K)
[8]	CS/0.18μm CMOS	13	4.9	-	4.7	-	9.7	-
[9]	CS/0.18μm CMOS	14	10.7	-	3.2	-	28.6	-
[10]	CS/0.09μm CMOS	14.5	12.3	-	2.1	-	11.2	-
This work	CG/0.13μm CMOS	15.2	10.3	8.5-11.6 (253-393 K)	4.3	3.9 - 5.9 (253-393 K)	5.9	5.5 - 6.5 (253-393 K)

B. Simulation

By using the measured temperature coefficients of the NMOS transistor and spiral inductors in Section II, the temperature dependence of the CG-LNA is simulated. First, the contribution from the respective temperature coefficient of the transconductance g_m, the output resistance r_o, and the spiral inductor L_m is simulated. Fig. 7 shows that the power gain decreases by 1.5 dB and the NF increases by 0.9 dB at 15.2 GHz when g_m decreases from 29.2 to 25.3 mS. When r_o increases from 316 to 336 Ω, the power gain changes slightly by 0.25 dB and the NF remains nearly unchanged. The spiral inductors induce 0.5-dB gain reduction and 0.3-dB NF increments. These simulation results show that the temperature coefficient of g_m dominates the power gain and NF temperature performance of the CG-LNA.

Next, the total effect from the temperature property of g_m, r_o, and L_m on the CG-LNA performance is simulated. Fig. 8 shows the simulated frequency response 253, 313, and 393 K, respectively. The power gain reduction from 253 to 393 K is around 2.1 dB at 15.2 GHz. This gain reduction is about the same at other frequencies in the 13–18-GHz range. Over the temperature range of 253–393 K, the input return loss is better than 17 dB and the output return loss is better than 10 dB from 14.2 to 16.2 GHz. The NF has an increment of 1.9 dB from 253 to 393 K at 15.2 GHz, and this increment is about the same at other frequencies in 6–18 GHz.

C. CMOS Layout

The proposed current-reused CG-LNA was implemented in 0.13-μm CMOS technology. The inductors L_{m1} (1.1 nH), L_{m2} (0.9 nH), L_{m3} (1.7 nH), and L_{m4} (1.4 nH) were realized with a spiral structure, and the RF-bypassing gate capacitance C_g was implemented with a 2.5-pF metal–insulator–metal capacitor. All gate bias resistors of 10 kΩ were realized using n^+ poly resistors. Fig. 9 shows a chip photograph, which covers an area of 0.6 mm^2 including the input and output pads.

IV. MEASUREMENT RESULTS OF CURRENT-REUSED CG-LNA

The implemented NMOS LNA was on-wafer measured with HP8510 vector network analyzer and NP5 noise measurement systems. Fig. 10 depicts the measured frequency performance at various temperatures (253, 313, and 393 K). At 313 K, the power gain is 10.3 dB and the input and output return losses are better than 15.6 dB at 15.2 GHz, respectively.

The input $P_{1\ \mathrm{dB}}$ is -14.8 dBm and the input IP3 is -5 dBm. The NF is 4.3±0.2 dB over a broad frequency range of 6–18 GHz, presenting a wideband noise characteristic. The implemented CG-LNA consumes 4.5 mA from a 1.3-V power supply. When the temperature increases from 253 to 393 K, the power gain at 15.2 GHz monotonically decreases by 3 dB and the NF increases from 3.9 to 5.9 dB over the 140-K variation range. The similar power gain reduction of 3 dB and the NF increment of 2 dB are also seen at other frequencies in the 13–18 GHz. The drain current increases from 4.2 to 5 mA, corresponding to a 11.9% variation over the 140-K variation range. The input and output return losses are better than 10 dB in 14–16 GHz, which implies that the input and output match is less affected by temperature. The measurement results agree very well with the simulation ones in Fig. 8, except the moderate degradation in the output return loss.

Table I outlines the measured performance of the proposed CG-LNA and other CS-LNAs. In terms of temperature performance, only a few CS-LNA studies in [1] and [2] have conducted temperature performance measurements, and this paper is the first to report the temperature performance of the Ku-band CG-LNA topology. Among these chips in Table I, the 5.5-GHz SiGe CS-LNA [2] achieves the smallest power gain temperature variation (0.4 dB/100 K) and moderate NF variation (0.5 dB/100 K) over the 273–373-K range. This outstanding temperature variation performance is attributed to the incorporation of a proportional-to-absolute temperature compensation circuit. However, the dc power consumption variation (34%/100 K) is relatively large. For the 2.4-GHz CS-LNA in SOI technology [1], it also has a large dc power consumption variation of 68%/175 K, while it has excellent gain temperature

variation of 0.9 dB/175 K. Compared to these two chips [1], [2], the proposed 15-GHz CG-LNA chip has the least dc power consumption variation (12%/140 K), but relatively poor gain variation. This is because the NMOS transistor bias point of the proposed chip is selected between ZTC_{id} and ZTC_{gm} to compromise the bias current and gm temperature variations.

V. Conclusion

This paper presents the first experimental measurement of the effect of temperature on Ku-band NMOS CG-LNAs. The device characteristics of the MOS transistor and the spiral inductor are experimentally obtained in a range from 253 to 393 K. First, the zero temperature coefficient points of the drain current and transconductance are obtained such that the dc-bias condition of the NMOS transistor can be determined. This, in turn, makes it possible to minimize the drain current and transconductance variation with temperature. This paper also extracts the temperature variation of intrinsic and extrinsic elements of the NMOS small-signal model from the measured scattering parameters. Based on these results, this paper designs a current-reused CG-LNA in 0.13-μm CMOS technology. At room temperature, the implemented CG-LNA has a measured power gain of 10.3 dB and NF of 4.3 dB at 15.2 GHz, while consuming 4.5 mA from a 1.3-V power supply. When the temperature changes from 253 to 393 K, the CG-LNA has a power gain variation of 3 dB, NF variation of 2 dB, and a dc power consumption variation of $+11.9\%$. This paper demonstrates that the temperature performance of the NMOS CG-LNA in the Ku-band can be optimized simply by selecting the proper transistor bias, which provides a simple, but effective method of minimizing the temperature effect.

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