國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

具有 SSTL_2 規格之

高速輸入/輸出電路設計及分析

Design and Analysis of

SSTL_2 I/O Buffer for DDR Applications

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指導教授　：　柯明道　教授

中華民國九十四年九月

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摘要

隨著 CPU 運算頻率的增加，我們所要處理的資料量也相對的增加，所以我們也需要速度更快的記憶體來處理這些傳輸的資料，不過因為 MOS 製程的特性有所極限，所以我們的記憶體就必須改變其架構或存取方法使能夠達到我們所需要的速度，所以記憶體由原本只有在時脈上升的時候存取資料，改由在時脈上升及下降的時候各存取一次資料，也就是由每一個週期只存取一次資料改為每個週期存取兩次資料，進而來使得記憶體存取的速度能增快，而這樣的架構就是我們所說的 DDR (Double Data Rate) SDRAM，可是這樣的架構下，我們必須要其他的輸入輸出介面，或者一些限制來避免資料傳輸的錯誤。而這篇論文則主要是設計能使用在 DDR SDRAM 之輸入輸出介面，還有在 DDR SDRAM 中能準確鎖住時脈相位以避免資料傳輸錯誤之延遲鎖定迴路。

在輸入輸出介面這方面的設計為使用 0.13 μm 1P8M CMOS 製程所實現的具有 SSTL_2 規格的輸入輸出介面，此設計包括兩個版本，兩個版本皆使用兩個電壓源，一個即是內部電路所要傳送或接收之電壓，其值為 1.2 V，另一個則是在輸出端所需要使用之電壓，其值為 2.5 V，要能使用在 DDR SDRAM 電路所需要之頻率為 400Mbps，而我設計之目標希望能達到 600Mbps。此兩種版本的差別

主要在是否具有迴轉率控制 (Slew Rate Control) 電路。

而另一項設計就是使用 0.13-μm 1P8M CMOS 製程所實驗之延遲鎖定迴路，其所使用之電壓源為 1.2 V，輸出之時脈頻率為 66MHz 到 250MHz，而 duty cycle 能在 45%到 55%之間。

Design and Analysis of

SSTL_2 I/O Buffer for DDR Applications

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ABSTRACT

For the higher CPU operation frequency, the amount of data transfer must be dealt with. So we need the memory which equips higher operation speed to speed up the data transfer. Because of the limitation of the MOS characteristics, the memory has to change the architecture or access method to achieve the desired operation frequency. So the memory architecture accesses data at the rising edge which means to access data once every clock cycle is improved to access data at both rising and falling edges that is accessing data twice every clock cycle. This can make the memory access data at higher speed. This architecture is called DDR (Double Data Rate) SDRAM. DDR SDRAM needs specific I/O interface or limitation to prevent transferring wrong data. This thesis discusses the I/O circuits design for the DDR SDRAM applications. It also discusses delay-locked loop (DLL) which can lock the internal clock accurately to prevent transferring wrong data.

The I/O interface is realized according to the SSTL_2 standard fabricated by

0.13 μm 1P8M CMOS process. There are two versions realizing the SSTL_2 I/O circuit. They both apply two pairs of power supply. One of them supplies to transfer or receive data from internal circuit, and its value is 1.2 V. Another one supplies the main circuits for transferring or receiving data by the I/O circuits, and its value is 2.5 V. The operation frequency for DDR SDRAM applications is 400 Mbps, and the goal of this design is to be able to achieve 600 Mbps. The differential part of these versions is whether the SSTL_2 I/O circuit equips the slew rate control circuit or not.

Another topic discussed in this thesis is the delay-locked loop (DLL) circuit fabricated by 0.13 μm 1P8M CMOS process. The power supply is 1.2 V, and the range of operation frequency is from 66 MHz to 250 MHz. The duty cycle of DLL architecture should be kept between 45% and 55%.

誌謝

回顧快兩年的碩士求學生涯，這過程真可以酸甜苦辣、五味雜陳來形容。這其中最苦的時期在於碩一剛入學時，由於當時心態尚未調適過來以至於在修課方面充滿著極大的挫折感與無力感。幸而在實驗室陳世倫學長適時的教導還有鄧志剛學長及陳榮昇學長的鼓勵讓我能咬緊牙根撐過最苦的日子，這不但讓我對日後的修課不再畏懼也對未來所面臨到更困難的挑戰具有更高的抗壓性。回顧這段往事真使我覺得自己何其幸運，能在最無助的時候得到實驗室師長最正面的幫助，這也使我懷著最真誠的心，深深感謝生活中每一個貴人。

首先要感謝的是我的指導教授柯明道博士。老師以其本身嚴謹的研究態度以及超乎常人的研究熱情，讓我於這兩年中獲得最珍貴的研究心態與方法。而在老師開明的指導以及豐沛的研究資源下，我不但能盡情將研究的電路下線驗證，也由於所從事的論文研究具實用性。除此之外，老師亦提供相當充裕的研究經費使我在這兩年中不至於生活匱乏而能更努力的從事我的碩士論文研究。畢業之後無論從事任何研究我都將會僅記老師的至理名言：Smart = 做事要有效率，成果要有水準。

接著要感謝的是一起打拼的同學們，宗信、弼嘉、建樺、鍵樺、啟祐、吳諭、家熒、煒明、志朋、峻帆、傑忠、岱原、宗熙、台祐、建文、進元，大家一起做研究、出遊、唱歌，讓我在苦悶的研究生活中增添不少樂趣。我也要感謝實驗室陳世倫學長、陳榮昇學長、張瑋仁學長、徐新智學長、陳世宏學長、林昆賢學長、黃彥霖學長、鄧至剛學長、顏承正學長、許勝福學長、王文泰學長。他們無論是在論文研究的瓶頸或是晶片量測的疑難雜症上都給了我很多的方向及幫助，使我能更順利的完成我的碩士論文。

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黃靖驊

九十四年九月

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Chapter 1
Introduction

1.1 MOTIVATION

Along with the electric technology improves rapidly, the process scale is also decreased quickly. Therefore, the value of power can be reduced so as to reduce the swing range. The algorithm develops much smarter than before. So the microprocessors can be designed to achieve higher speed. The increasing operation frequency would need higher speed memory to deal with the increasing amount of data that is created in the period of the operation time. Because the internal clock frequency in microprocessors is up to gigabits-per-second range, memory must support this speed of data transfer. But the speed of conventional SDR SDRAM would be limited by process or architecture. So DDR SDRAM was developed to replace conventional SDR SDRAM to support such high speed. DDR SDRAM needs the I/O circuits named stub series terminated logic for 2.5 V (SSTL_2) to support such high speed. Also DDR SDRAM needs delay-locked loop (DLL) to lock the internal clock referring to the external clock. DLL can avoid timing error when data are transferred at such high speed. This I/O circuit of SSTL_2 and DLL are the two main subjects discussed in this thesis.

1.2 DDR SDRAM CONCEPT

Before introducing SSTL_2 and DLL, simply understanding DDR SDRAM architecture is necessary. The DDR SDRAM transfers data at the rate of 200, 266, 333,

and 400 Mbps. Its clock speed is 100, 133, 166, 200 MHz. DDR SDRAM transfer data at both rising and falling edge of clock. The conventional SDR SDRAM only fetches data at rising edge of clock. But DDR SDRAM spends one cycle in employing 2-bit prefetch architecture. DDR SDRAM transfers data twice in a period of clock cycle, and SDR SDRAM only transfers one time in a period of clock cycle. DDR SDRAM transfers data twice than SDR SDRAM when they are operated in the same frequency so that DDR SDRAM can have higher data rate without increasing clock frequency. But it is difficult to accurately control the data input/output timing based on the conventional single clock. Therefore, DDR SDRAM adopts a differential clock scheme that enables accurate memory control. The duty cycle of clock has to keep about 50% to prevent timing error. This is not the same as SDR SDRAM. Because SDR SDRAM can make the high state a little less than the low state. This can prevent next data transferred earlier than expected. But DDR SDRAM should keep the duty cycle about 50% as accurately as possible. The internal clock is generated by the external clock across long wire line or clock tree. This may influence the accuracy of timing. So DLL is used here to lock the internal clock referred to the external clock. DLL would generate the internal clock that has duty cycle about 50%. The detail about DLL will be discussed in chapter 4. DDR SDRAM employs SSTL_2 interface to eliminate the signal degradation caused by noise and reflection produced as a result of a high operating frequency. SSTL_2 is a low-voltage (2.5 V), amplitude and high-speed interface that reduce the effect of reflection by connecting series resistance between the signal branch point from the bus and the memory. There are another technologies used in DDR SDRAM architecture in [1] - [3]. The comparisons of DDR and SDR SDRAM are listed in Table 1.1.

1.3 SSLT_2 I/O CIRCUIT ARCHITECTURE

Fig. 1.1 shows the concept of SSTL_2 architecture. The output of SSTL_2 transmitter is CMOS buffer. The CMOS buffer should provide 8.1mA output current for Class_I, and 16.2 mA output current for Class_II. The receiver of SSTL_2 is a differential pair. One input of this differential pair is connected to reference voltage which value is $0.5xV_{DDQ}$. Another is connected to the input pin of the receiver. When receiver receives data, the input pin of the receiver compares with reference voltage. The data is judged to be '1' when the voltage of input pin is larger than reference voltage, and to be '0' when the voltage of input pin is smaller than reference voltage. RS is called stub resistance. It is connected in series to the output pin (Vout) that provides impedance matching between the transmission line and device output. The termination voltage (V_{TT}) is terminated with RT. The value of termination voltage is the same as reference voltage. The value of RT in Class_I is different to in Class_II. It will be explained in following chapter. And SSTL_2 uses terminal resistance (RT) connected to termination voltage to reduce the swing range to increase the speed. Otherwise, this termination suppresses signal reflection in the transmission line and also reduces voltage spikes, enabling high-speed data transmission.

1.4 DLL ARCHITECTURE

DLL applied in DDR SDRAM is designed to realize a fast access time and high operation frequencies by controlling and adjusting the time lag between the external clock and internal clock. The block diagram of conventional DLL architecture is shown in Fig. 1.2. The comparator compares the external clock and feedback of internal clock. Then the arbiter and finite state machine (FSM) receive the result of

comparator and sends up or down signal to up/down counter. And decoder will decode the signal of up/down counter to control the delay line to lock the internal clock referring to external clock. There are many methods to realize DLL architecture such as digital DLL, analog DLL, and mixed-mode DLL. These different types of DLL architecture have their individual advantages and disadvantage. Judging whether they are significant or not is important in designing DLL architecture applied in DDR SDRAM.

1.5 THESIS ORGANIZATION

Chapter 2 of this thesis discusses the SSTL_2 standard. The detail DC and AC specifications and some features of DLL will be presented in this chapter. Chapter 3, two version design of SSTL_2 I/O circuit are presented and the measurement results are shown in the last section of this chapter. Chapter 4 discusses DLL architecture design more detail. We will discuss all blocks of this DLL architecture design, and explain how these blocks operate. Summarizing this thesis and making some conclusions are described in the last chapter.

Table 1.1

Difference in functions and specifications between DDR and SDR SDRAM.

Item	DDR SDRAM	SDR SDRAM
Data Transfer Frequency	Twice the Operation Frequency	Same as the Operation Frequency
Data Rate	$2/t_{clock}$	$1/t_{clock}$
Clock Input	Differential Clock	Single Clock
Data Strobe Signal(DQS)	Essential	Not Support
Interface	SSTL_2	LVTTL
Supply Voltage	2.5 V	3.3 V
CAS Read Latency	2, 2.5	2, 3
CAS Write Latency	1	0
Burst Length	2, 4, 8	1, 2, 4, 8 Full-Page(256)*
Burst Sequence	Sequential/Interleave	Sequential/Interleave
Use of DLL	Essential	Optional
Data Mask	Write Mask Only	Write Mask/Read Mask

* Full-Page(256) burst of SDR SDRAM is an option.

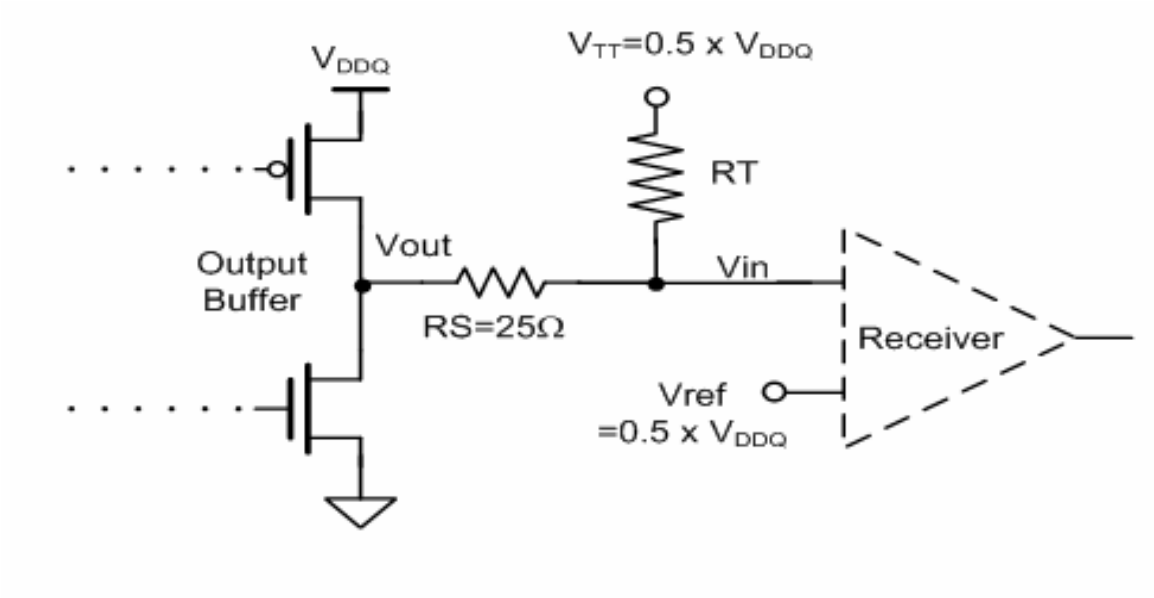

Fig. 1.1 Concept of SSTL_2 Architecture

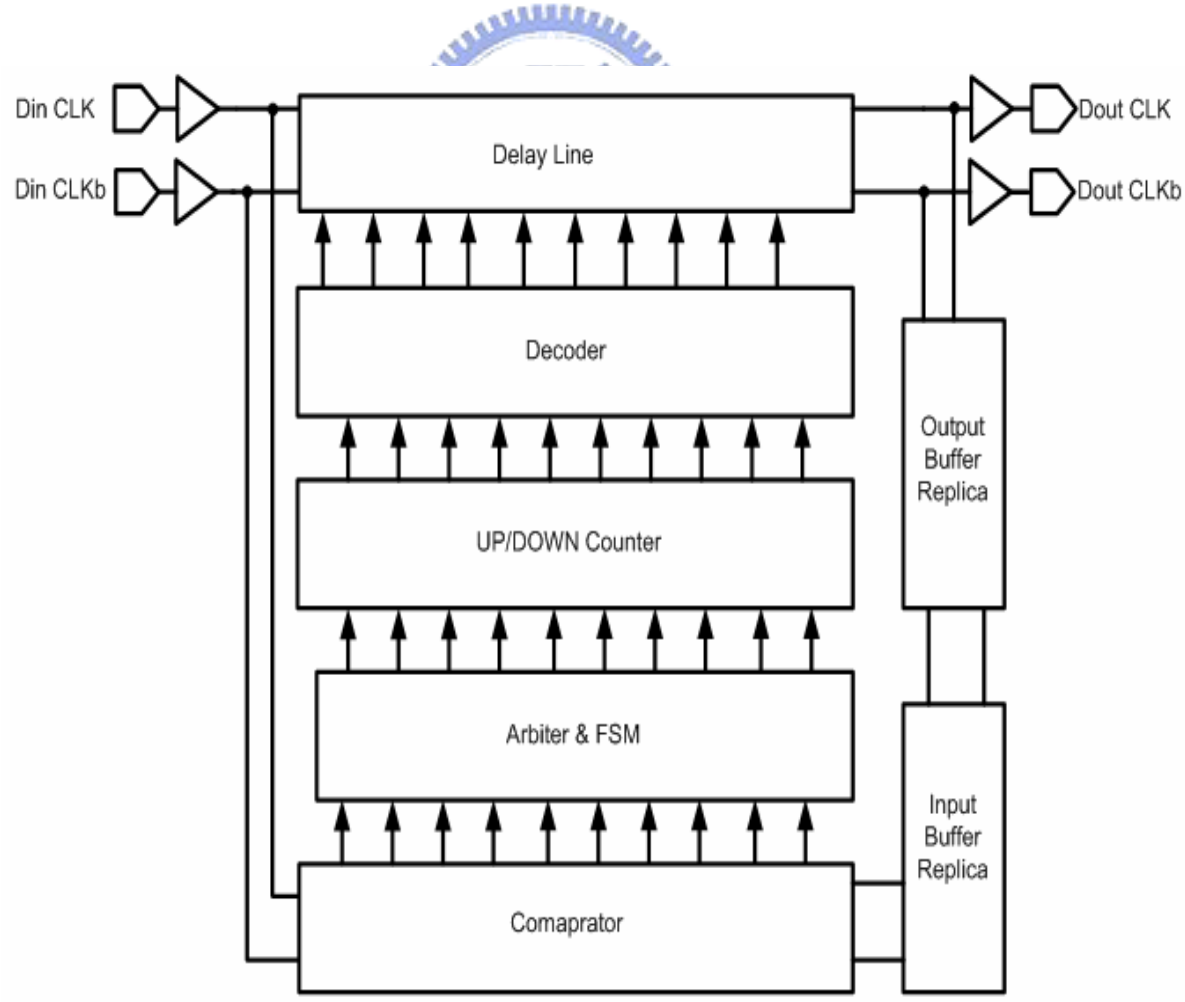

Fig. 1.2 Block Diagram of DLL Architecture

Chapter 2

Specifications of Stub Series Terminated Logic for 2.5 V (SSTL_2) Standard and Delay-Locked Loop (DLL) Standard

2.1 BACKGROUND

For high frequency memory application, the data transfer must resist the noise or signal reflection through the transmission line. Although internal circuits may achieve hundreds megabits-per-second even gigabits-per-second range, the I/O circuits may not support such high frequency. So even the memory uses the newest process, algorithm, and architecture to satisfy the speed what we want to achieve, it can still not output the signal at this operational frequency. In SDR SDRAM, LVTTL is applied as the I/O interface. But in DDR SDRAM, the data rate would reach to 400 Mbps. The LVTTL may not be suitable for DDR SDRAM interface at this frequency because LVTTL didn't have enough noise margins and operation frequency. In such high speed, to enable data transmission and to suppress noise influences are the main factors in interface determinant. SSTL_2 uses termination resistance connected to termination voltage to suppress signal reflection in the transmission line, to reduce voltage spikes, and to enable high-speed data transmission. So SSTL_2 is suitable to the DDR SDRAM interface. Otherwise, high-speed data transmission should emphasis the subject of timing. Providing accurate clock is significant to data transmission. DLL can realize a fast access time and high operation frequencies so that it is often applied in the DDR SDRAM architecture. DLL provide a differential

pair of clock locked as the external clock to be sure that the data transmission can meet the accurate timing.

2.2 STANDARD OF SSTL_2

The interface applied in DDR SDRAM is defined by the document, Stub Series Terminated Logic for 2.5 V (SSTL_2) JESD8-9B [4]. This JEDEC standard document defines the AC voltage level, DC voltage level, minimum output current, and all voltage sources needed in the SSTL_2 circuit. Also it shows the concept of two types SSTL_2 I/O circuits, Class_I I/O circuit and Class_II I/O circuit, and roughly compares the differences between Class_I and Class_II I/O circuit.

2.2.1 Concepts of Two Types SSTL_2 I/O Circuits

SSTL_2 output buffer is mainly compartmentalized Class_I and Class_II I/O circuit. Fig. 2.1 shows the SSTL_2 architecture. RS is the stub resistance, whose value is 25 Ω, connected in series to output pin. The stub resistance provides impedance matching between the device output and transmission line. RT has different value in Class_I and Class_II application. In Class_I architecture RT is 50 Ω, and RT is 25 Ω in Class_II architecture. In actual application, there is transmission line connecting RS and RT. So RT is a concept of equivalent impedance looking from the end of RS. The detail description of SSTL_2 output connection will be discussed in the next chapter. Otherwise, Class_I and Class_II are also different in the aspect of electric characteristics. It will be shown in section 2.2.4, output buffer electric characteristic.

Otherwise, the receiver of SSTL_2 has two ways to receive data. This thesis emphasizes discussing single-ended signal. The single-ended signal receiver has input

pin of reference voltage, Vref. At the mention of receiver before, the receiver has a differential pair to receive data. One input pin of this differential pair has the function of the receiver input pin. Another is connected to the reference voltage, Vref. In the later chapter, the single-ended signal receiver will be emphasis. The different part between single-ended and differential signals receiver is that the pin which is connected to reference voltage is changed to be connected to the inverse phase of the output data. Tables 2.1 and 2.2 list the DC and AC logic levels and AC test conditions about differential input, and Fig. 2.2 shows the waveform of SSTL_2 differential input levels simply. In Fig. 2.2, V_{TR} means the "true" input level, and V_{CP} means the "complementary" input level. $V_{IN(DC)}$ is defined the allowable DC excursion of each differential input. $V_{Swing(DC)}$ / $V_{Swing(AC)}$is the absolute value of the DC/AC value difference between the "true" input level and the "complementary" input level. $V_{X(AC)}$ is the crossing point of V_{TR} and V_{CP}. The typical value of $V_{X(AC)}$ is expected to be about 0.5x V_{DDQ} of the transmission device and $V_{X(AC)}$ is expected to track variations in V_{DDQ}. $V_{X(AC)}$ indicates the voltage at which differential input signals must be crossing. Table 2.2 lists the differential input AC test conditions. Fig. 2.3 and Fig. 2.4 are two examples of SSTL_2 Class_I differential signals AC test conditions. Those figures can simply explain the different part between single-ended and differential signals I/O circuits. In later chapter, the single-ended signal I/O circuit will be discussed mainly.

2.2.2 Supply Voltage Levels

All circuits have to need power to make them work normally. First, supply voltage levels must be defined. Table 2.3 lists the supply voltage levels. For explaining SSTL_2 circuits more clearly, Fig. 1.1 is repeated here again as Fig 2.5.

V_{DDQ} is the output supply voltage. It provide the output buffer a pair of separate power lines, because the output buffer must source and sink large amount of current. It would make the control circuits influenced by the ground bounce and power bounce which is induced by the large amount of output current. So the control circuit power line can be separated from the output buffer power line. Table 2.3 defines the relationship between V_{DD} and V_{DDQ}. There is no specific device V_{DD} supply voltage requirement for SSTL_2 compliance. However, under all conditions V_{DDQ} must be less than or equal to V_{DD}. Otherwise, the input reference voltage, Vref, may be selected by the user to provide optimum noise margin in the system. Typically the value of Vref is expected to be (0.49~0.51)xV_{DDQ} of the transmitting device and Vref is expected to track variations in V_{DDQ}. And peak to peak AC noise on Vref may not exceed +/-2% of $Vref_{(DC)}$. The terminated voltage also has relationship to Vref. V_{TT} of transmitting device must track Vref of receiving device. Because the SSTL_2 I/O circuits receive data from internal circuits and transmit data to internal circuits, they need a pair of low voltage, 1.2 V, to supply the circuits be able to transfer data with internal circuits correctly. In the aspect of low voltage power line is not defined accurately.

2.2.3 Input Logic Electric Characteristics

Input logic levels are shown in Table 2.4. We can reference Fig. 2.6 to understand the relationship of the input logic levels more clearly. Within this standard, it is the relationship of the V_{DDQ} of the driving and the Vref of the receiving device that determines noise margins. However, in the case if $V_{IH(MAX)}$ (i.e. input overdrive) it is the V_{DD} of the receiving device that is referenced. In the case where a device is implemented that supports SSTL_2 inputs but has no SSTL_2 outputs, and therefore

no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ}+300mV). Otherwise, V_{IH} and V_{IL} both have AC and DC value definition. The DC value is defined smaller than AC value. It means that the hysteresis zone of the AC value is larger than the DC value's. Since the AC value is less stable than DC value, AC value must need larger noise margins than DC value. When receiver receives continual low or high signals, the signals can be treated as the DC values. The AC value of V_{IH} and V_{IL} must have larger noise margins than DC value of V_{IH} and V_{IL} to defend the noise affecting. Then, Table 2.5 shows the AC input test conditions. The AC input test conditions are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise environment makes it difficult to create clean signals with limited swing. The AC test conditions may be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis that the device will meet its timing specifications under all supported voltage conditions. For $V_{Swingmax}$, the input signal maximum peak to peak swing, compliant devices must still meet the $V_{IH(AC)}$ and $V_{IL(AC)}$ specifications under actual use conditions. The 1 V/ns input signal minimum slew rate is to be maintained in the $V_{ILmax(AC)}$ to $V_{IHmin(AC)}$ rage of the input signal swing. Fig 2.7 shows the AC input signal wave form of Table 2.5.

2.2.4 Output Buffer Electric Characteristics

The output part of SSTL_2 is composed of CMOS buffer. The specifications of output buffer electric characteristics sets minimum requirements for output buffers in such a way that when they are applied within the range of power supply voltage specified in SSTL_2 and are used in conjunction with SSTL_2 input receivers then the input receiver specifications can be met or exceeded. The specifications are quite

different from traditional specifications, where minimum values for V_{OH} and maximum values for V_{OL} are set that apply to the entire supply range. In SSTL_2, the input voltage provided to the receiver depends on the driver as well as on the termination voltage and termination resistors. Of particular interest here are the values V_{OUT} and V_{IN}. These values depend not only on the current drive capabilities of the buffer, but also on the values of V_{DDQ} and V_{TT} (Vref is equal to V_{TT}). The important condition is that V_{IN} be at least 405 mV above or below V_{TT} as a result of V_{OUT} attaining its maximum low or its minimum high value. As will be seen later, the two cases of interest for SSTL_2 are where the series resistor RS equals 25 Ω and the termination resistor RT equals 50 Ω (for Class_I) or 25 Ω (for Class_II). V_{TT} is specified as being equal to 0.5x V_{DDQ}.

In order to meet the 405 mV minimum requirement for V_{IN}, a minimum of 8.1 mA must be developed across RT if RT equals 50 Ω (Class_I) or 16.2 mA in case RT equals 25 Ω (Class_II). The driver specification now must guarantee that these values of V_{IN} are obtained in the worst case conditions specified by this standard. Table 2.6 and Table 2.7 codify Class_I output buffer DC current drives and AC test conditions. Table 2.8 and Table 2.9 codify Class_II output buffer DC current drives and AC Test conditions. Table 2.10 is the spread sheet showing how the limits of SSTL_2 circuit voltage depend on V_{DDQ}. It shows some cases about the influence of the variation of Vref and V_{TT}. In Table 2.10 the “on resistance” equals V_{TT}/I - (RS+RT). The worst case assumption for V_{TT} results from the fact that for V_{TT}=$V_{TT(MIN)}$ the input at the receiver is already biased towards the low state and less current will be required to develop 345 mV ΔV_{IN}. If the driver maintains a resistance lower than the “Maximum On Resistance”, more than the 345 mV will be presented to the receiver.

These specifications are defined in the above sections. The SSTL_2 I/O circuits should obey these specifications to be designed to transfer data correctly. The more

detail aspect about the SSTL_2 I/O circuits will be discussed in next chapter.

2.3 STANDARD OF DLL

In DDR SDRAM, the DLL circuit, shown in Fig. 2.8, is designed to realize a fast access time and high operation frequency by controlling and adjusting the time lag between the external clock and internal clock. There are many ways to realize the DLL circuits, such as digital DLL architectures [5] - [8], analog DLL architectures [9], and mixed-mode DLL architectures [10]. The digital DLL architectures have the advantage of low power consumption and high operation frequency, and they have the disadvantage of more complex control circuits. The analog DLL architectures have the advantage of locking more precisely, and they have the disadvantage of high power consumption. The mixed-mode DLL architectures have the advantage of both digital and analog DLL architectures, and they have the disadvantage of large chip area and complex timing control. These types of DLL architectures have different advantages and disadvantages. Determining whether they are significant or not helps designer to decide which DLL architecture can be applied in the DDR SDRAM.

DLLs are now often used in the DDR SDRAM architecture in order to hide clock distribution delays and to improve overall system timing. In these applications, DLLs must closely track the input clock. However, the rising demand for the DDR SDRAM I/O interfaces has created an increasingly noisy environment in which DLLs must function. This noise, typically in the form of supply and substrate noise, tends to cause the output clock of DLLs to jitter from their ideal timing. Otherwise, for the demand of the duty cycle, the DLLs must output the internal clock with 50% duty cycle. So, with a shrinking tolerance for jitter in the decreasing period of the output clock, the design of low jitter DLLs has become very challenging. Here the

specification of the DLL which operation range is 66 MHz to 250 MHz reference clock frequency in DDR SDRAM application is defined. The delay adjustment range is 0% to 100% of input clock cycle in the range of operation frequency. The locking time is 150 input clock cycles. It means that no matter the reference input clock frequency is the output clock must be locked within 150 input clock cycles, and the range of the output clock duty cycle is 45% to 55%. The DLL current consumption is 10 mA. Table 2.11 codifies these specifications of the DLL architecture.

Table 2.1

Differential Input Logic Levels.

Symbol	Parameter	Minimum	Maximum
$V_{IN(DC)}$	DC Input Signal Voltage	-0.3 V	V_{DDQ}+0.3 V
$V_{Swing(DC)}$	DC Differential Input Voltage	0.3 V	V_{DDQ}+0.6 V
$V_{Swing(AC)}$	AC Differential Input Voltage	0.62 V	V_{DDQ}+0.6 V
$V_{X(AC)}$	AC Differential Cross Point Voltage	0.5xV_{DDQ}-0.2 V	0.5xV_{DDQ}+0.2 V

Table 2.2

Differential Input AC Test Conditions.

Symbol	Parameter	Minimum	Maximum
V_r	Input Timing Measurement Reference Level	V_x (Cross Point)	
V_{Swing}	Input Signal Peak To Peak Swing Voltage	------	1.5 V
SLEW	Input Signal Slew Rate	1.0 V/ns	------
t_{CKD}	Clock Duty Cycle	45%	55%

Table 2.3

Supply Voltage Levels.

Symbol	Parameter	Minimum	Normal	Maximum
V_{DD}	Device Supply Voltage	V_{DDQ}	------	n/a
V_{DDQ}	Output Supply Voltage	2.3 V	2.5 V	2.7 V
Vref	Input Reference Voltage	1.13 V	1.25 V	1.38 V
V_{TT}	Termination Voltage	Vref-0.04 V	Vref	Vref+0.04 V

Table 2.4

Input Logic Levels.

Symbol	Parameter	Minimum	Maximum
$V_{IH(DC)}$	DC Input Logic High	Vref+0.15 V	V_{DDQ}+0.3 V
$V_{IL(DC)}$	DC Input Logic Low	-0.3 V	Vref-0.15 V
$V_{IH(AC)}$	AC Input Logic High	Vref+0.31 V	------
$V_{IL(AC)}$	AC Input Logic Low	------	Vref-0.31 V

Table 2.5

AC Input Test Conditions.

Symbol	Parameter	Value
Vref	Input Reference Voltage	0.5 x V_{DDQ} V
$V_{Swingmax}$	Input Signal Max Peak to peak Swing	1.5 V
Slew	Input Signal Minimum Slew Rate	1.0 V/ns

Table 2.6

Class_I Output Buffer DC Current Drives.

Symbol	Parameter	Minimum	Maximum
$I_{OH(DC)}$	Output Minimum Source DC Current	-8.1 mA	------
$I_{OL(DC)}$	Output Minimum Sink DC Current	8.1 mA	------

Table 2.7

Class_I Output Buffer AC Test Conditions.

Symbol	Parameter	Value
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.608 V
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} - 0.608 V

Table 2.8

Class_II Output Buffer DC Current Drives.

Symbol	Parameter	Minimum	Maximum
$I_{OH(DC)}$	Output Minimum Source DC Current	-16.2 mA	------
$I_{OL(DC)}$	Output Minimum Sink DC Current	16.2 mA	------

Table 2.9

Class_II Output Buffer AC Test Conditions.

Symbol	Parameter	Value
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.81 V
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} - 0.81 V

Table 2.10

Spread Sheet Showing how the Limits of SSTL_2 Circuit Voltage Depend on V_{DDQ}.

Condition	**Class_I**	**Class_I**	**Class_I**	**Class_II**	**Class_II**	**Class_II**	**Class_II normal**
V_{DDQ}	2.3 V	2.5 V	2.7 V	2.3 V	2.5 V	2.7 V	2.5 V
$Vref_{(MIN)}=V_{DDQ}$ *0.49	1.13 V	1.23 V	1.32 V	1.13 V	1.23 V	1.32 V	1.25 V
$Vref_{(MAX)}=V_{DDQ}$ *0.51	1.17 V	1.28 V	1.38 V	1.17 V	1.28 V	1.38 V	1.25V
$V_{TT(MIN)}=Vref_{(MIN)}$ -0.04V	1.09 V	1.19 V	1.28 V	1.09 V	1.19 V	1.28 V	1.25 V
$V_{TT(MAX)}=Vref_{(MAX)}$ +0.04V	1.21V	1.32 V	1.42 V	1.21V	1.32 V	1.42 V	1.25V
RS	25 Ω	25 Ω	25 Ω	25 Ω	25 Ω	25 Ω	25 Ω
RT	50 Ω	50 Ω	50 Ω	25 Ω	25 Ω	25 Ω	25 Ω

Output High Drive							
Minimum Output Current	-8.1mA	-8.1mA	-8.1mA	-16.2mA	-16.2mA	-16.2mA	-16.2mA
$V_{TT(WC)}=Vref_{(MAX)}$ -0.04V	1.13 V	1.24 V	1.34 V	1.13 V	1.24 V	1.34 V	1.25 V
Minimum Voltage at V_{IN}	1.54 V	1.64 V	1.74 V	1.54 V	1.64 V	1.74 V	1.66V
Minimum Voltage at V_{OUT}	1.74 V	1.84 V	1.94 V	1.94 V	2.05 V	2.15 V	2.06 V
Maximum On Resistance	69.1 Ω	81.2 Ω	93.3 Ω	22.0 Ω	28.1 Ω	34.1 Ω	27.2 Ω
$\Delta V_{IN(MIN)}= V_{IN}$-Vref	365 mV	365 mV	365 mV	365 mV	365 mV	365 mV	405 mV

Output Low Drive							
Minimum Output Current	8.1mA	8.1mA	8.1mA	16.2mA	16.2mA	16.2mA	16.2mA
$V_{TT(WC)}$=$Vref_{(MAX)}$ +0.04V	1.17 V	1.27 V	1.36 V	1.17 V	1.27 V	1.36 V	1.25 V
Maximum Voltage at V_{IN}	0.76 V	0.86 V	0.96 V	0.76 V	0.86 V	0.96 V	0.85V
Maximum Voltage at V_{OUT}	0.56 V	0.66 V	0.76 V	0.36 V	0.46 V	0.55 V	0.44 V
Maximum On Resistance	69.1 Ω	81.2 Ω	93.3 Ω	22.0 Ω	28.1 Ω	34.1 Ω	27.2 Ω
$\Delta V_{IN(MIN)}$= V_{IN}-Vref	-365mV	-365mV	-365mV	-365 mV	-365 mV	-365 mV	-405 mV

Table 2.11

Specifications of the DLL Architecture.

Parameter	**Specification**
Reference Input Clock Range	66 MHz ~ 250 MHz
Delay Adjustment Range	0% to 100% of Input Clock Cycle
Delay Adjustment Resolution	1.7% of Input Clock Cycle
Number of Adjustment Steps	60 (7 bits)
Locking Time	150 Input Clock Cycles
Current Consumption	10 mA
Duty Cycle	45% ~ 55%

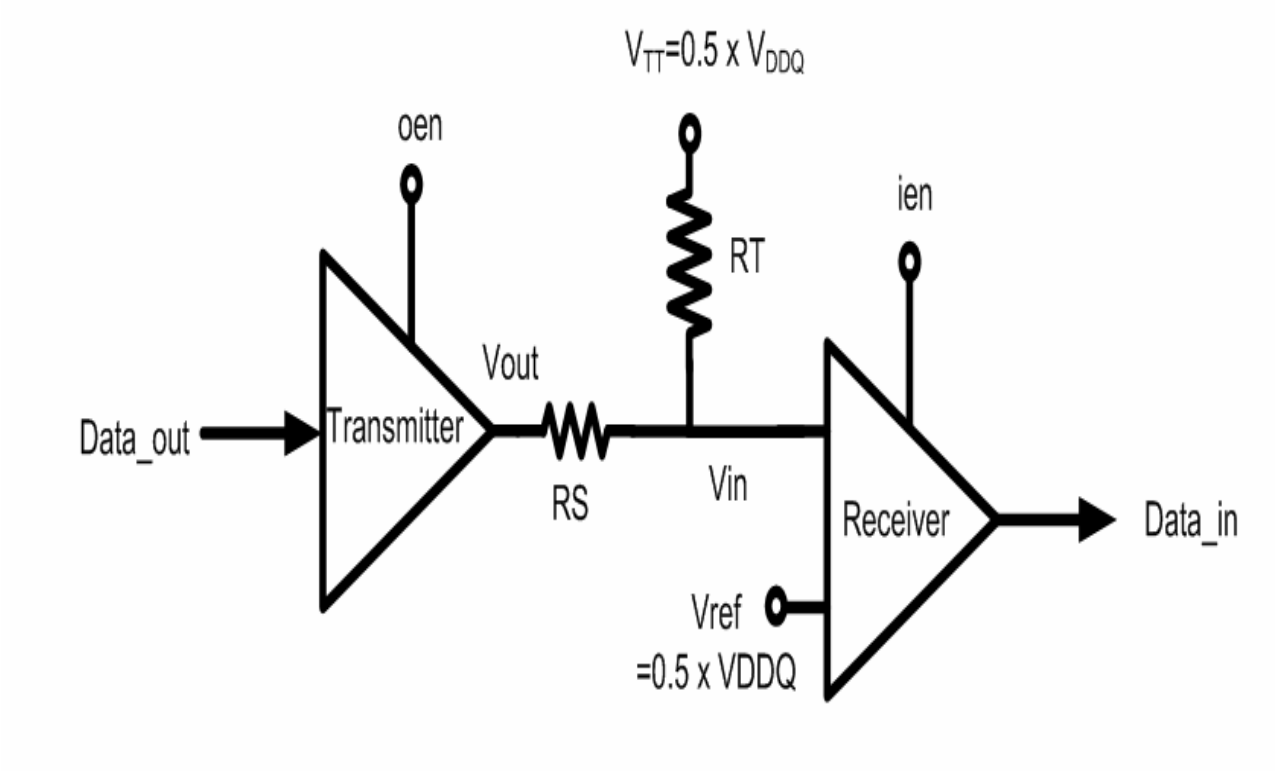

Fig. 2.1 SSTL_2 Architecture

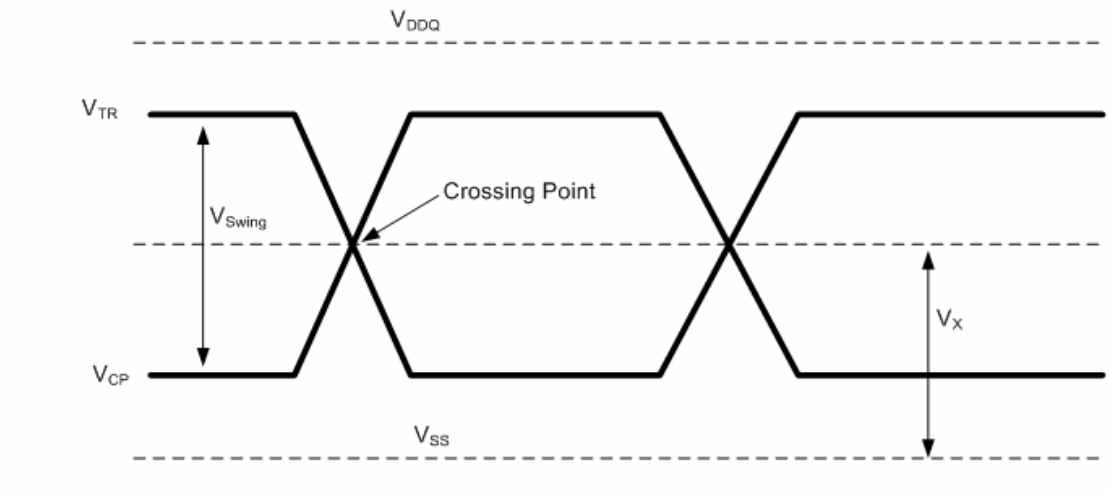

Fig. 2.2 SSTL_2 Differential Input Levels

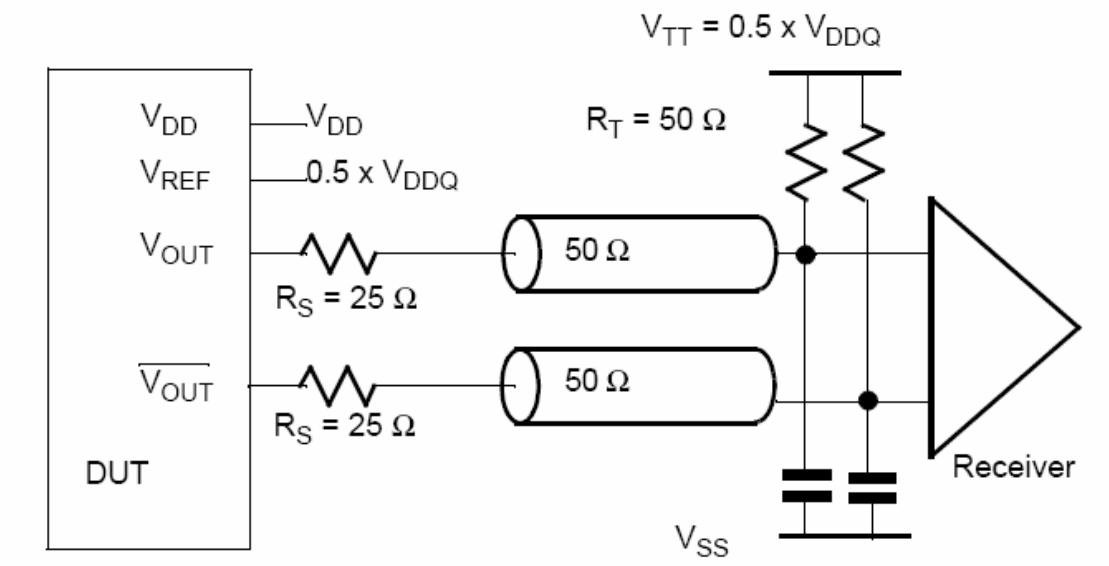

Fig. 2.3 Example of SSTL_2 Class_I Differential Signal

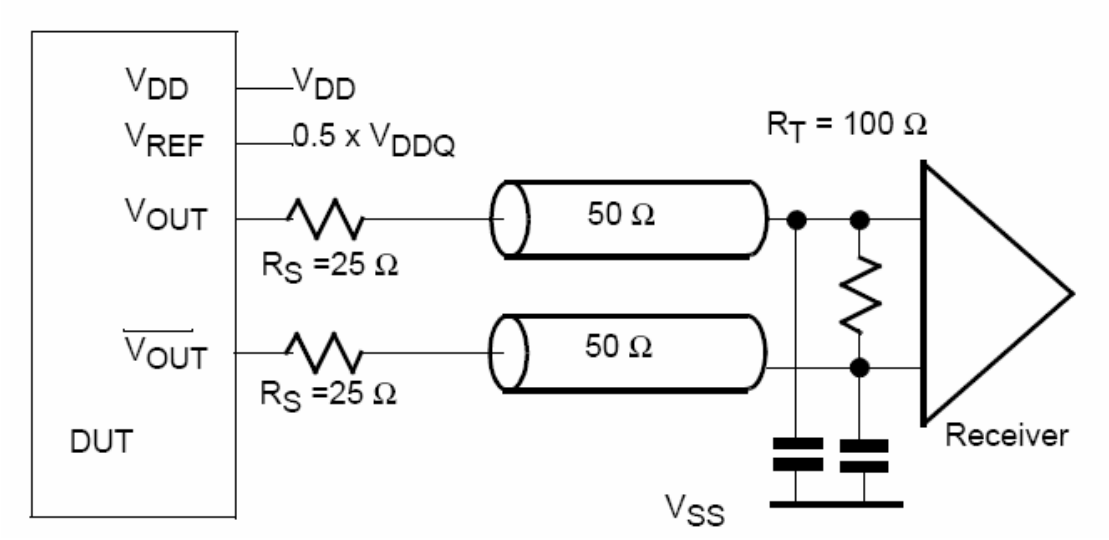

Fig. 2.4 Example of SSTL_2 Class_I Differential Signal

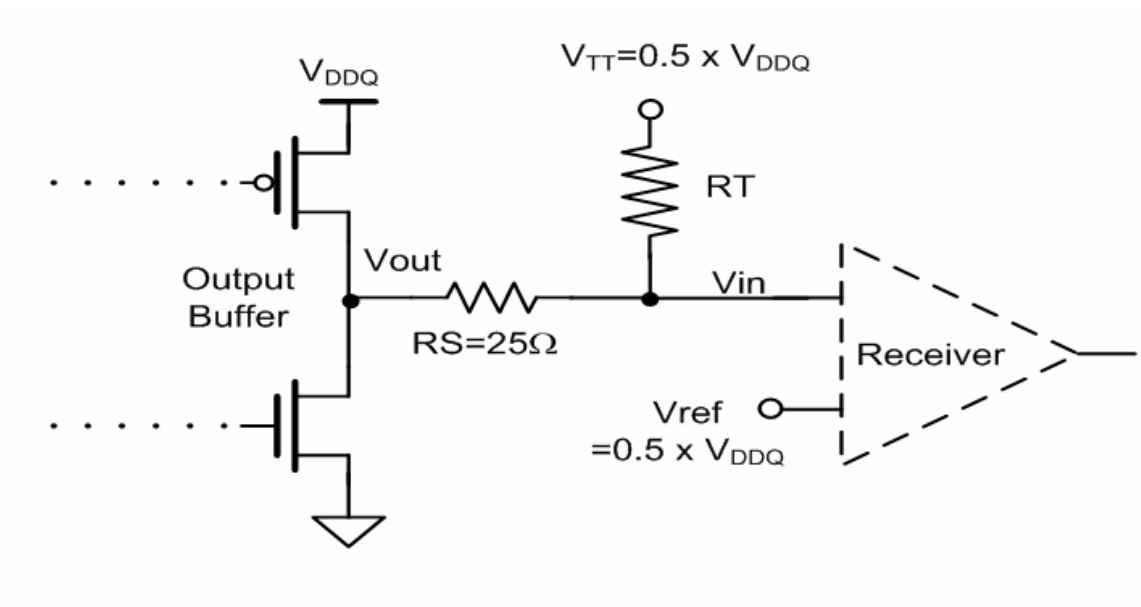

Fig. 2.5 Concept of SSTL_2 Architecture

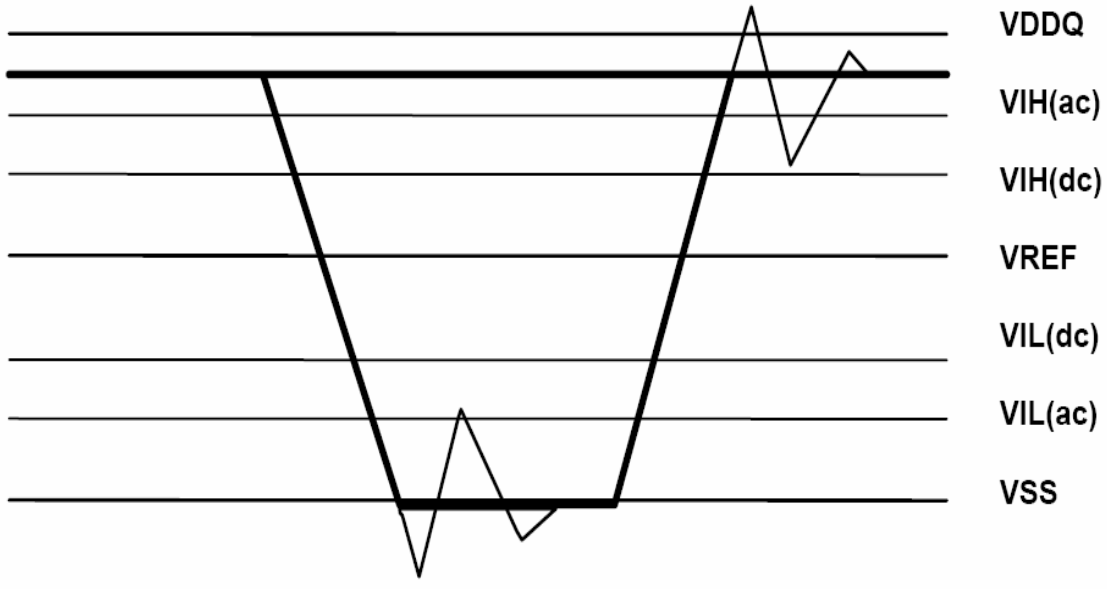

Fig. 2.6 SSTL_2 Input Voltage Levels

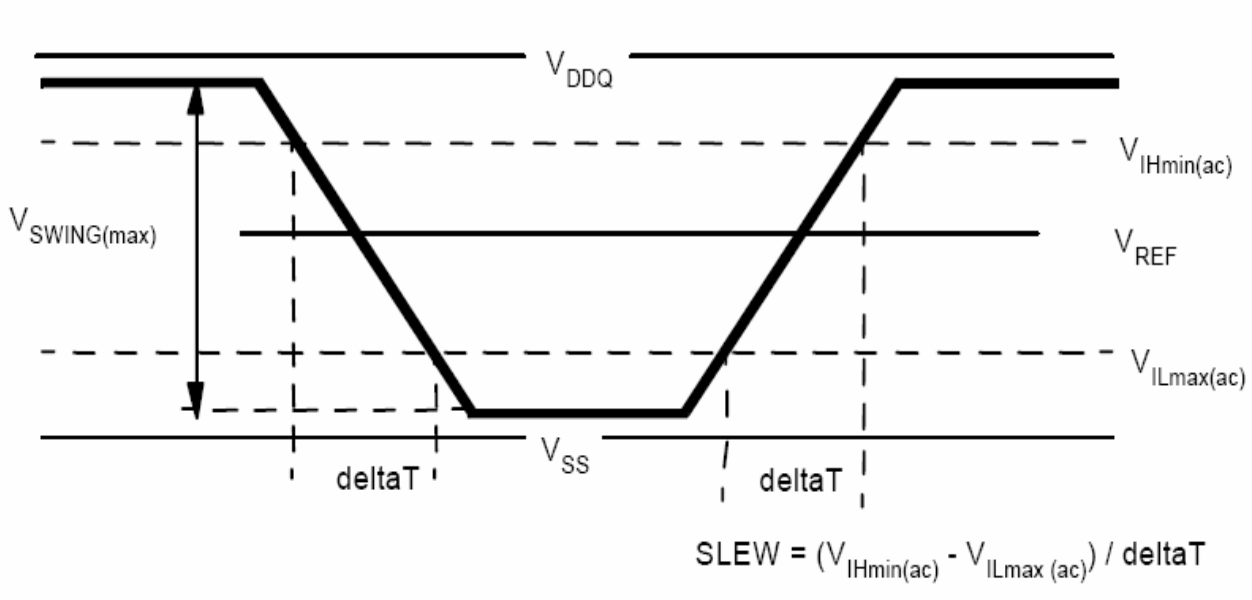

Fig. 2.7 AC Input Test Signal Wave Form

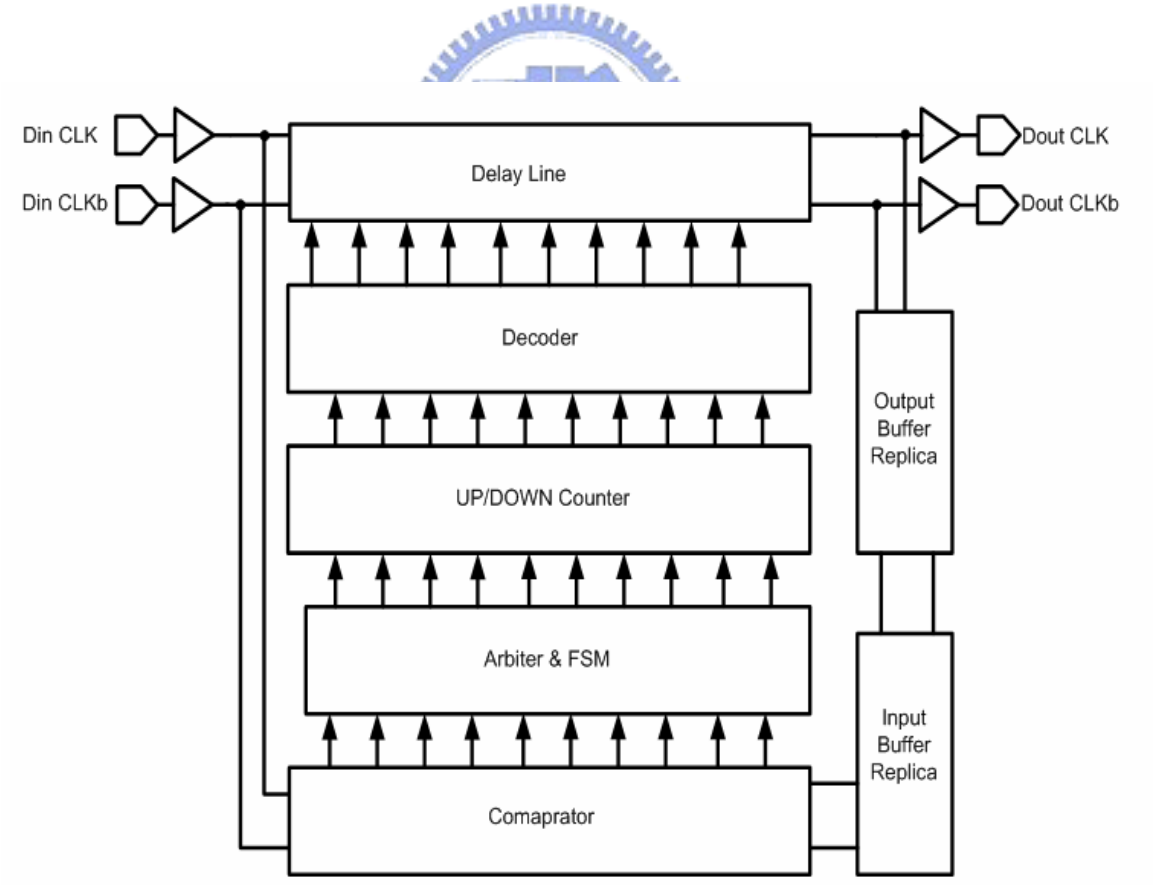

Fig. 2.8 Block Diagram of DLL Architecture

Chapter 3

SSTL_2 I/O Buffer

3.1 INTRODUCTION

The data rate of transceiver is highly dependent on the I/O interface circuit of transceiver and the cable length. For many digital systems, the major performance limiting factor is the interconnection bandwidth between chips to chips or chips to boards. Therefore, how to design high-speed I/O interface circuits is an important issue [11]. Besides, as the data rate of system is up to several gigabits-per-second range nowadays, the power consumption is another important issue. The design of high speed I/O interface circuits has led to concern on how to increase performance, decrease power consumption, reduce cost and mitigate noise or EMI/RFI. However, the above four factors are trade off to each other.

The I/O Circuit applied in the DDR SDRAM architecture is stub series terminated logic (SSLT_2). SSTL_2 operates at the frequency of 400Mbps which is 200 MHz clock rate for its maximum speed. When the signals transfer data at such operation frequency, the influences of the noise and signal reflection will make the data transfer bring the dirty data or wrong data. In conventional data transfer, the I/O circuits often use the method of full swing. The full swing data transfer has the better ability of noise disputing, but it can't achieve higher operation frequency. When the requirement of operation frequency increases, the swing range should be decreased making the circuit to achieve higher speed. But the decreased swing range would be sensitive to the noise. So the I/O circuits would require the noise disputing equipment. SSTL_2 uses the termination voltage to suppress the swing range to achieve the

improvement of operation frequency. SSTL_2 uses the termination resistance connecting to the termination voltage to suppress signal reflection in the transmission line and also reduces voltage spikes, enabling high-speed data transmission. The following section will discuss the I/O circuit with the specification of SSTL_2 that were developed to ensure that data signals can meet the higher data throughput speeds needed for newer memory systems.

3.2 SSTL_2 ARCHITECTURE

There are mainly two kinds of SSTL_2 architectures. One kind of SSTL_2 architecture is called Class_I, and another is called Class_II. The differences of these two types of SSTL_2 architecture is mainly in the parts of output current and terminated resistance. Figs. 3.1, 3.2, and 3.3 show the Class_I type and Class_II type of SSTL_2 architectures. Fig. 2.5 is repeated here again as Fig.3.4 and shows the concept of SSTL_2 architecture. As mentioned before, the Class_I and Class_II I/O circuits are different in the termination resistance, RT, and the output current. Actually, the termination resistance is the equivalent impedance. Figs. 3.1, 3.2, and 3.3 show the SSTL_2 data transfer with transmission line. They show the equivalent impedance of the termination resistance, RT, and the applications of the SSTL_2 test condition. Fig. 3.2 and Fig 3.3 show two ways of SSTL_2 Class_II type termination. In Fig. 3.2, the bus is terminated at both ends with a 50Ω resistance, for a combined series resistance of 25Ω. In Fig 3.3, the bus is terminated at the far end from the controller with a single 25Ω resistance. It is strongly recommended that the single resistance termination scheme in Fig. 3.3 be used for best performance. The benefits of this approach include reduced cost, simpler signal routing, reduced reflections, and better signal bandwidth and settling. The SSTL_2 Class_II type I/O circuit often

applied in the DIMM (Dual In-Line Memory Modules) architecture such as shown in Fig. 3.5. This architecture often transfers data through long transmission lines or long distance. So designers should simulate the SSTL_2 Class_II type I/O circuit with the strict way such as Fig. 3.2, the worse data transfer type. Otherwise, the best way of SSTL_2 data transfer is that transfers data to receiver without transmission line. In this way, shown in Fig 3.6, means that interconnections are short, and there is no need for and termination at all. This application can be served by a Class_I or Class_II type I/O circuit and an SSTL_2 type receiver. But sometimes SSTL_2 often use the transmission line and resistances to transfer data for a long distance. Here, SSTL_2 with transmission line is the emphasis of following discussion. It is because that if the circuits are designed and satisfying the worse case, the circuits will be applied in any case. The following section will discuss the transmitter and the receiver respectively.

3.2.1 Transmitter

Fig. 3.4 is the concept of the SSTL_2 architecture. It shows the output of SSTL_2 consisting of the CMOS output buffer. As mentioned before, SSTL_2 has two types I/O circuits. These two types SSTL_2 I/O circuits are different in the output current, so the CMOS output buffer of SSTL_2 has different size. Table 2.6 to Table 2.9 list the DC output current and AC test condition specification of Class_I type and Class_II type I/O circuits. They show that the DC current of Class_II type SSTL_2 circuit (16.2mA) is twice as much as the DC current of Class_I type SSTL_2 circuit (8.1mA). This condition influences the AC test condition specification. When the circuits satisfy the DC current levels, the connection method such as Fig. 3.1 to Fig. 3.3 will resolve the AC test condition level. So at first, the designer must determine the size of Class_I type or Class_II type output buffer to satisfy the claim of the

specification. Fig. 3.7 shows the block diagram of the SSTL_2 transmitter. The control circuits of SSTL_2 transmitter include state logic, level converter, and tapper buffer. The state logic receives the signal called output enable, “oen,” to control if the data, Data_out, will be transferred. When oen is high, the received data will be transferred. Oppositely, both PMOS and NMOS of the output buffer will be turned off, when oen is low. So the state logic, shown in Fig. 3.8, can clearly explain the function clearly.

Otherwise, due to the voltage of the transfer data is 0V to 1.2V, and the output buffer supply voltage is 2.5V, the control circuits should need a level converter to be sure the correctness of the data transfer. The level converter, shown in Fig. 3.9, consists of the 1.2V device, the inverter in Fig. 3.9, to create a pair of differential signal. Then the differential signal would make one of the NMOS turn on, and another is off. Next, the PMOS will extend the difference quickly to make one of output signal is 2.5V and another is 0V. But this level converter has the disadvantage of poor pull down ability. This causes that the falling time will be larger than rising time. In the DDR SDRAM application, it is significant to make rising time and falling time symmetrical to prevent the jitter depressing the performance. So if we want to get symmetric rising time and falling time, we should increase the NMOS size of the level converter. But this effect has limit. The next section, SSTL_2 architecture with slew rate control, will discuss the improvement of this level converter architecture.

Otherwise, due to PMOS and NMOS of the output buffer have large size, the level converter doesn’t have the ability to pull up or pull down the signal quickly. So the tapper buffer is applied here to drive the large size output buffer. Otherwise, the tapper buffer may not have to transfer data with full swing range. It just needs to transfer data with the correct voltage level, but this is passive. So if the operation frequency increases, the tapper buffer may not be able to work normally. When this

circuit operates at the frequency of 200MHz, the tapper buffer still can transfer data correctly with full swing range. So the circuit has no problem to work normally. This circuit can still work normally at the frequency of 300MHz (i.e. 600 Mbps). Although the tapper buffer may not work with full swing range.

3.2.2 Receiver

The SSTL_2 receiver judges the data as the high level when the data voltage is higher than 1.25V, and judges the data as the low level when the data voltage is lower than 1.25V. So the SSTL_2 receiver uses a differential pair to realize this architecture. Fig. 3.10 is the schematic of SSTL_2 receiver. One input of the differential pair is connected to the reference voltage, Vref, and another is connected to the input of the receiver, which is also the pad of the SSTL_2 I/O circuit. The differential pair often needs a current source to provide the circuit sufficient amount of current to make the circuit work normally. In analog circuit design, the current source must be provided accurately. It often uses current mirror to mirror the current, which the designers want to apply in the analog circuits, from the self-biased current source. But the differential pair only needs the current to make the circuit operated normally. It doesn't have to have accurate amount of current. So this circuit uses an NMOS to provide the operation current. The NMOS is controlled by the signal called input enable, "ien," which turns on the NMOS when its voltage level is high, and turns off the NMOS when its voltage level is low. Then, this circuit needs a high-to-low voltage converter to transfer the voltage level of 2.5 V to 1.2V when the logic level is high. And the voltage level still keeps at 0V when the logic level is low. In Fig 3.10, the output load capacitance is 250 fF considered the long distance metal line loading.

3.2.3 Layout Style

In the I/O circuit application, the designer should notice the layout style much more. Because the I/O circuits are often parallel arranged, it must be claimed about the cell hight and pitch strictly. Although the Class_I type and the Class_II type have different size in the output buffer, the two types I/O circuits must have the same cell hight and pitch. Because Class_II type SSTL_2 circuit has larger size in the output buffer and tapper buffers, the I/O circuits must be realized according to the size of Class_II type SSTL_2 circuit. And the control circuit and output buffer of Class_I type SSTL_2 circuit is smaller than Class_II type. So Class_I typre SSTL_2 circuit can use the decouple capacitance to fill the excess area. Comparing Fig. 3.11 and Fig. 3.13 clearly shows that the control circuit of Class_I type SSTL_2 has larger decouple capacitance than Class_II type. In this application Class_I type and Class_II type output buffer have different size, but the layout size of Class_I type and Class_II type output buffer are the same. The excess size of Class_I type output buffer should be turned off. In this way, the layout style of Class_I type, shown in Fig.3.12, and Class_II type, shown in Fig.3.14, have the same cell hight (143 μm) and pitch (60 μm). The layout style also influences the ESD protection level. The power pins of this I/O circuit architecture must equip the ESD protection circuit. The 2.5V power pin applies the RC inverter architecture, Fig. 3.15, as the ESD protection circuit, and the 1.2V power pin applies GGNMOS architecture, Fig.3.16. In Fig. 3.16, the gate of the NMOS doesn't connect to ground directly. It has a resistance connected between the gate and ground. The function of this resistance would make the gate voltage not decrease too fast so that the NMOS can't discharge the ESD current sufficiently. These ESD protection circuits must be noticed that every finger of the NMOS used to discharge ESD current must turn on at the same time as possible as they can. So if the

discharge path has a longer length, the metal line must be wider to sustain the large current and make the fingers be able to turn on at the same time. In this way, the ESD protection circuits can achieve its best efficiency.

3.3 SSTL_2 ARCHITECTURE WITH SLEW RATE CONTROL

Because SSTL_2 have large amount of current, the instant current will induce the ground bounce and power bounce. As the decreasing supply voltage, these reactions will make the circuit work normally. There are some methods to solve the ground bounce and power bounce influence such as reducing the power line length, double bound which means paralyzing the inductance of power line to reduce the value of inductance, putting the power pins in the middle of the chip, and applying the slew rate control circuit on the output buffer. Applying the slew rate control circuit on the output buffer is the main method reducing the ground bounce and power bounce when the designer simulates the circuits. If the I/O circuit can depress the influence of ground bounce and power bounce, the power line can sustain more I/O circuit swing simultaneously without transferring the wrong data. The SSTL_2 architecture with slew rate control, shown in Fig. 3.17, will be discussed in the following sections. This design also improves the disadvantage of the level converter, and modifies the receiver slightly.

3.3.1 Level Converter

In the previous design, the level converter has the disadvantage of rising time and falling time asymmetric. The reason why the rising time and falling time is asymmetric is that the NMOS devices of the conventional level converter, Fig. 3.9,

are driven by the 1.2V power supply. But these NMOS are realized by the process of 2.5V. When the PMOS pull up the voltage, the gate of PMOS will be at the voltage of 0V. But when the NMOS devices pull down the voltage, the gate of NMOS is operated only at the voltage of 1.2V. So this conventional level converter has poor ability of pull-down. The modified level converter, Fig. 3.18, uses the always on NMOS, MN3 and MN4, to improve the pull-down ability. Be attentive that MN3 and MN4 are realized by the process of 1.2 V same as the inverter. Fig. 3.19 shows the simulation result of comparing these two kinds of level converter waveform. The conventional level converter has more gradual waveform, the original waveform in the figure, than the modified level converter when it is pull down. This makes the modified level converter equip the characteristic of symmetrical rising time and falling time to reduce the influence of asymmetric jitter.

3.3.2 Receiver

The modified design, shown in Fig. 3.20, includes the receiver, high-to-low level converter, and a NAND gate which is the major different from previous design, shown in Fig.3.10. In Fig. 3.10, the receiver uses the signal “ien” to control if the circuit turn on or not. But if the ground bounce makes the NMOS that applied as the currant source turn on, the circuit maybe transfers the data that we do not want if the disable time is not short enough. Because the ground bounce may cause the voltage between the gate and the source of the NMOS that is applied as the current source of the receiver exceeding the threshold voltage to turn on the receiver when the receiver should be turned off. The modified receiver adds the NAND gate that is applied to control the receiver enabling or disabling the receiver. Because the signal “ien” can turn off the NAND gate directly when “ien” is at the level of logic “0”, this can

prevent that the current source is turned on by ground bounce or noise.

3.3.3 Slew Rate Control Circuits

When current passes through the bonding wire, it will induce the voltage drop such as equation 3-1:

$$V = L\frac{di}{dt} \qquad (3\text{-}1)$$

When the output buffer transfers data, the large amount of current would be created in a short period of time to pull up or pull down the output node. Otherwise, the power line is realized by metal which will induce the conductance effect according to the length of metal line. So the designers often put the power pad at the middle of the chip to reduce the length of metal line between the pad and the package pin so that the conductance effect can be reduced to ease the power bounce and ground bounce. Besides, the slew rate control circuits also applied to achieve this goal of easing the ground bounce and power bounce. The function of slew rate control circuit is reducing the slope of the transion curve. But slew rate control circuit will reduce the operation frequency. To sacrifice the operation frequency is sometimes necessary for satisfying the specification. The conventional slew rate control circuit is shown as Fig. 3.21. This is a three-step slew rate control circuit. The numbers of steps should be considered by the requirement of applying system. In Fig. 3.21, the output buffer is divided to three parts. The theory of this slew rate control circuit is to reduce the instant current in a short period of time. It uses the resistances to turn on these parts of output buffer step-by-step. The function of resistances is to delay the input signal to turn on or turn off the divided output buffer step-by-step. This can reduce the current variation in a period of time caused by the output buffer to suppress the ground

bounce and power bounce. But this has disadvantage of turning off PMOS or NMOS slowly as it turns on PMOS or NMOS. It consumes more power for turning off the MOS slowly to reduce the current supplied by the power. So the modified slew rate control circuit is designed to solve this disadvantage. Because in conventional slew rate control circuit the input signal is transferred step-by-step whether the MOS should be turned on or turned off. The modified slew rate control circuit must achieve the goal of turning on MOS step-by-step and turning off MOS as soon as possible. For example, the PMOS of output buffer is turned on when the gate is pulled down to the logic low by the NMOS N4. The signal of pull-down will be transferred through the transmission gates for the function of delaying the signal to turn on PMOS step-by-step. For turning off PMOS, the PMOS, P1, P2, and P3, will turn off the PMOS of output buffer at the same time preventing from consuming the unnecessary current to reduce the power consumption. This slew rate control circuit is applied in the second version SSTL_2 I/O circuit.

3.4 MEASUREMENT RESULTS

There are two kinds for the test of SSTL_2 I/O circuit design. The measurement environment setup is shown in Fig. 3.23, and it uses a pulse generator to create the input signal of the transmitter. The transmitter transfers data through the transmission line to the receiver. When testing the Class_I type transmitters, the Class_II type I/O circuits are applied as the receivers. Oppositely, the Class_I type I/O circuits are applied as receivers for testing Class_II type transmitters. Figs. 3.24 and 3.25 are these test circuits for Class_I and Class_II as transmitter respectively. Fig. 3.26 is the die photo and layout for first tap-out. Because the numbers of pad is not enough to support the requirement of testing circuits, the input pins of Class_I I/O circuits are

connected together. Due to this connecting way, the SSTL_2 I/O circuits can only test the worse case that three bits transfer data at the same time. Fig. 3.27 is the PCB board of Class_I test circuit for the first tap-out. The maximum operation frequency for SSTL_2 applied in DDR SDRAM is 400 Mbps (200 MHz clock rate). Fig. 3.28 is the measurement result for the maximum frequency for Class_I type SSTL_2 I/O circuits applications, and Fig. 3.29 is the utmost operation frequency for the first version of Class_I type SSTL_2 I/O circuits. Fig. 3.30 is the PCB board for testing the first version Class_II type SSTL_2 I/O circuits. Fig. 3.31 and Fig. 3.32 are the measurement results for the Class_II type SSTL_2 I/O circuits operated at the speed of 400 Mbps and 500 Mbps respectively. The second tap-out die photo and layout is shown in Fig. 3.33. The internal circuits are the first version SSTL_2 I/O circuits, and the external circuits are the SSTL_2 I/O circuits with slew rate control circuit. The internal circuits test two bits of the first version SSTL_2 I/O circuits operated at the same time. The external circuits can test the SSTL_2 I/O circuits with slew rate control circuit for one bit or eight bits operated at the same time. Fig. 3.34 is the PCB board for testing the internal circuits. Fig. 3.35, Fig. 3.36, and Fig. 3.37 are the measurement results of two bits first version Class_I type SSTL_2 I/O circuit operated at the same time for different operation frequency. Figs. 3.38, 3.39, and 3.40 are the measurement results for two bits first version Class_II type SSTL_2 I/O circuit operated at the same environment as Class_I type. The SSTL_2 I/O circuit with slew rate control circuit testing PCB board is shown in Fig. 3.41. This PCB board can test the SSTL_2 I/O circuit with slew rate control circuit only one bit or eight bits operated at the same time. Fig. 3.42 to Fig. 3.47 are the measurement results of two types SSTL_2 I/O circuit with slew rate control circuit operated only one bit at the same time, and Figs. 3.48 to 3.54 are the measurement results for this circuit operating eight bits at the same time.

3.5 CONCLUSION

For these measurement results, the SSTL_2 I/O circuit with slew rate control circuit equips better performance than the first version SSTL_2 I/O circuit. It can be operated at the speed of 600 Mbps for eight bits SSTL_2 I/O circuit with slew rate control circuits operated at the same time without transferring wrong data. But at this operation frequency for two bits or three bits of the first version SSTL_2 I/O circuits, the duty cycle of this I/O circuit does no longer maintain at 50%. The SSTL_2 I/O circuit with slew rate control circuit may be able to be operated higher frequency, but the output signals are transferred by tapper buffers which limit the maximum operation frequency. Otherwise, for the DDR SDRAM application these two versions SSTL_2 I/O circuit can be operated normally (operating at the speed of 400Mbps). Table 3.1 shows the electrical characteristics of these kinds of SSTL_2 I/O circuits. The output enable time is defined the reaction time of the output node, Vout, after "oen" is high. The current consumption of 2nd version Class_II type SSTL_2 I/O circuit is larger than the reference. This is because the size of output buffer may be larger than the reference due to the most current consumption produced by the output buffer of Class_II type SSTL_2 I/O circuit. Table 3.2 shows the HBM ESD testing of the I/O circuit. The ESD level of the I/O circuit is more than 5 kV. The HBM ESD testing for VDD-to-VSS Stress Positive-mode is 6kV.

Table 3.1

Comparison of SSTL_2 Electrical Characteristics

	Reference[12]		**1st Version SSTL_2**		**SSTL_2 with Slew Rate Control**	
	Class_I	**Class_II**	**Class_I**	**Class_II**	**Class_I**	**Class_II**
Output Enable Time	2 ns	2 ns	1.2 ns	1.3 ns	1.8 ns	1.8 ns
Output Disable Time	2 ns	2 ns	1.9 ns	2.1 ns	1.5 ns	1.6 ns
Input Enable Time	0.5 ns	0.5 ns	0.9 ns	0.9 ns	1.1 ns	1.1 ns
Input Disable Time	1 ns	1 ns	0.6 ns	0.6 ns	0.9 ns	0.9 ns
Current Consumption	10 mA	14 mA	9.5 mA	17.3 mA	9 mA	17 mA

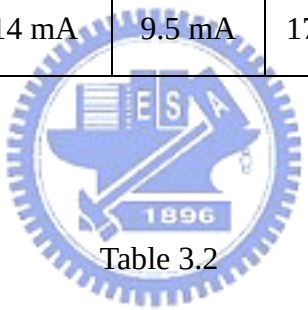

Table 3.2

HBM ESD Testing

	PS-mode	NS-mode	PD-mode	ND-mode
Class_I PAD	5 kV	> 8 kV	> 8 kV	5.5 kV
Class_II PAD	5.5 kV	> 8kV	> 8kV	7 kV

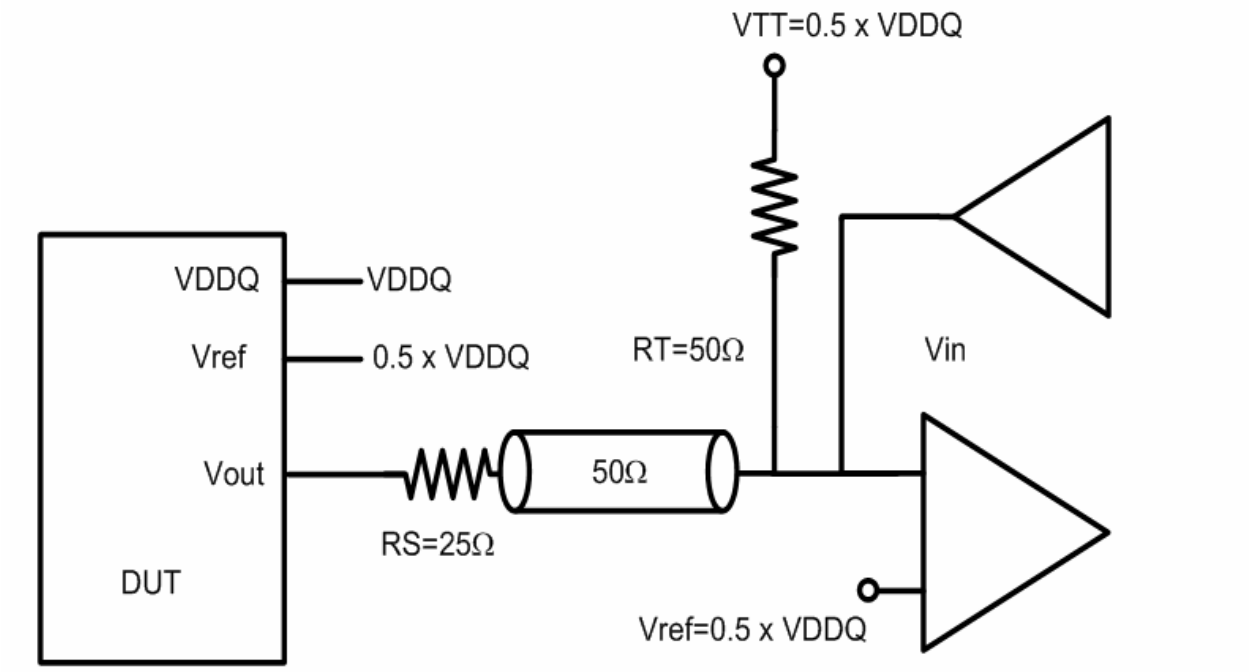

Fig. 3.1 Class_I type of SSTL_2 Architecture

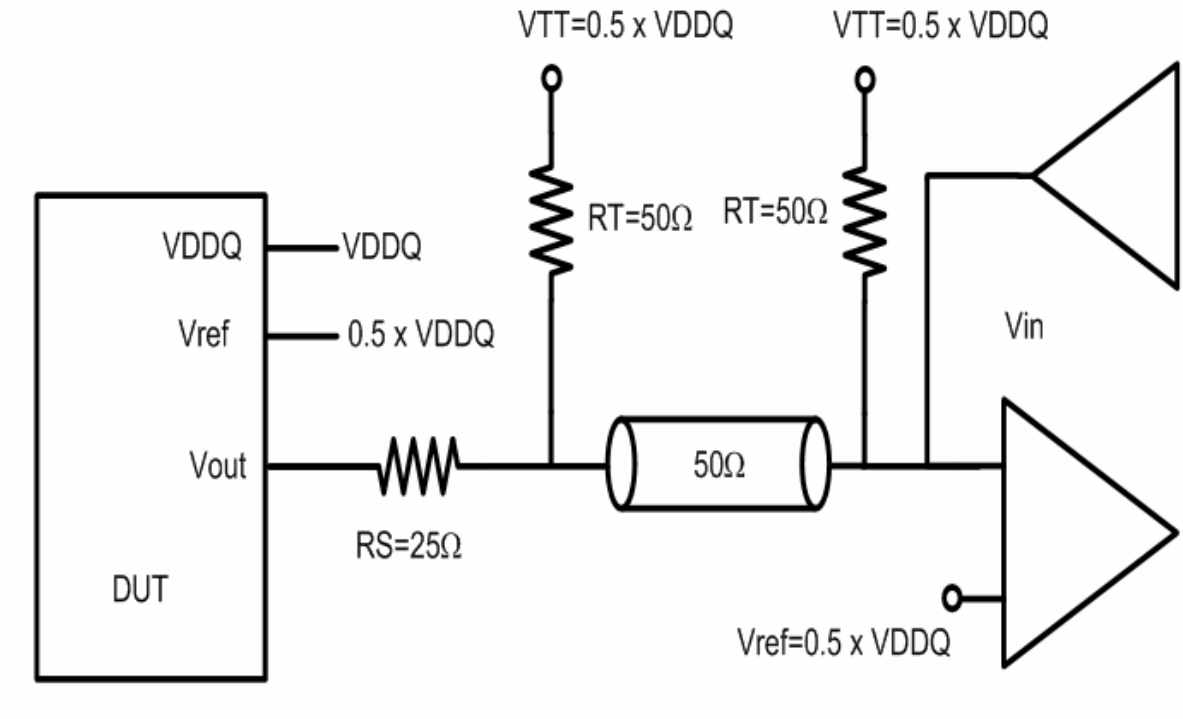

Fig. 3.2 Class_II type of SSTL_2 Architecture (double-terminated output)

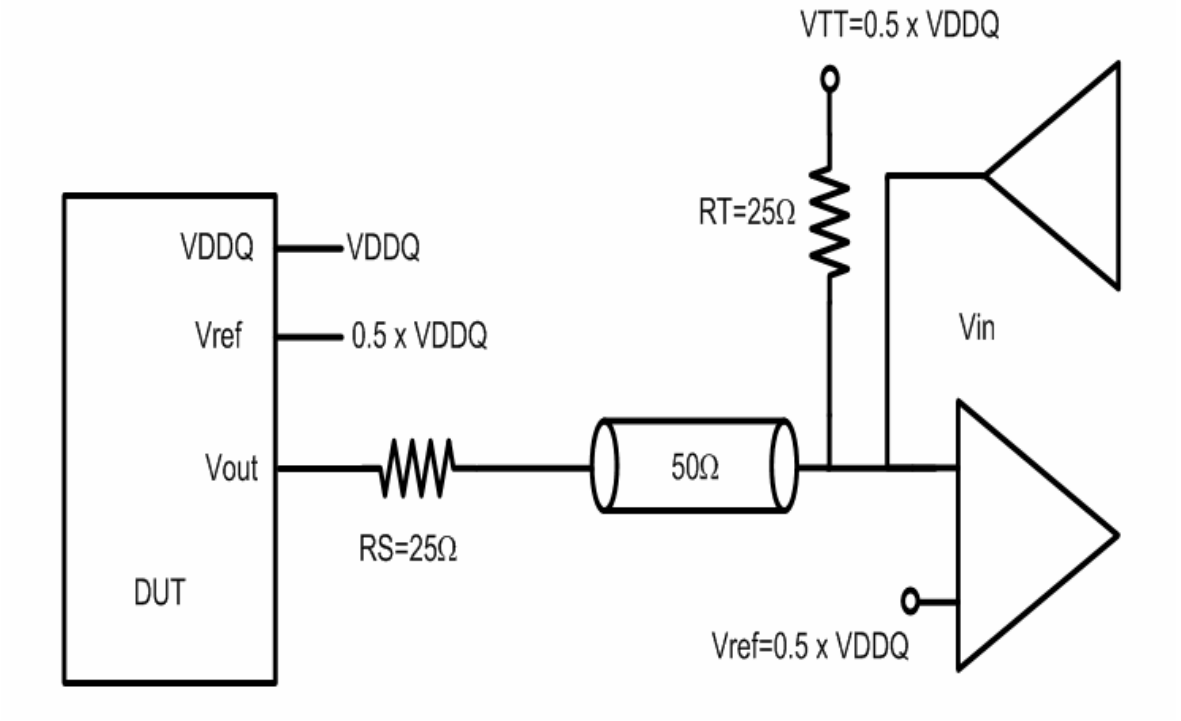

Fig. 3.3 Class_II type of SSTL_2 Architecture (single-terminated output)

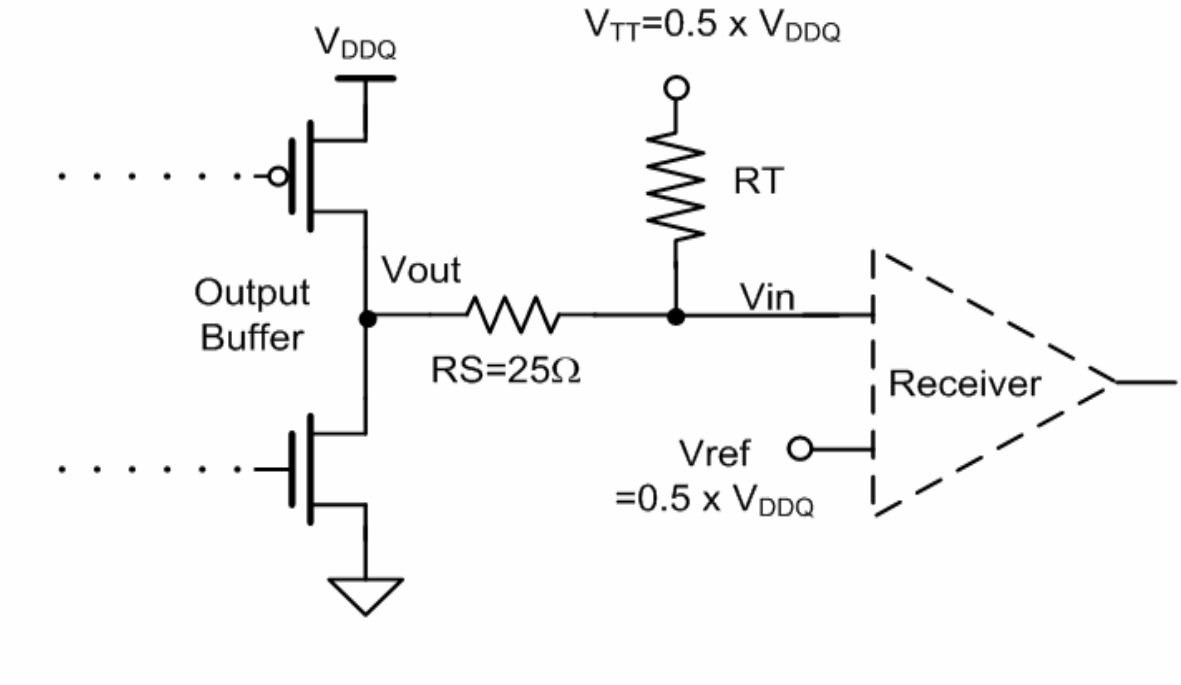

Fig. 3.4 Concept of SSTL_2 Architecture

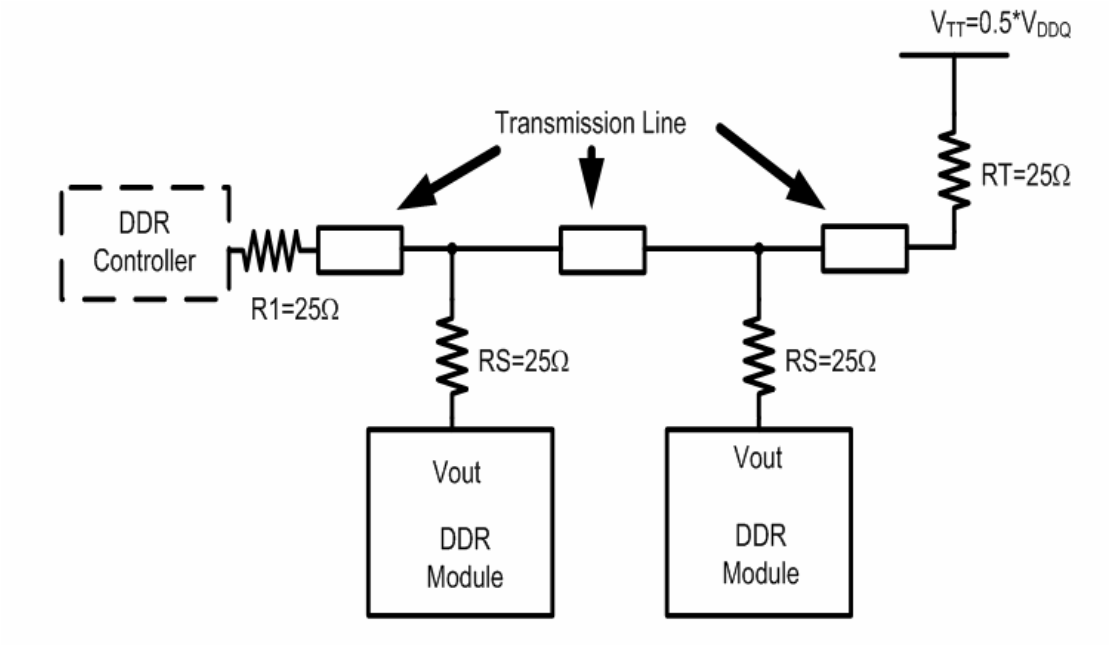

Fig. 3.5 SSTL_2 Applied in DIMM Architecture

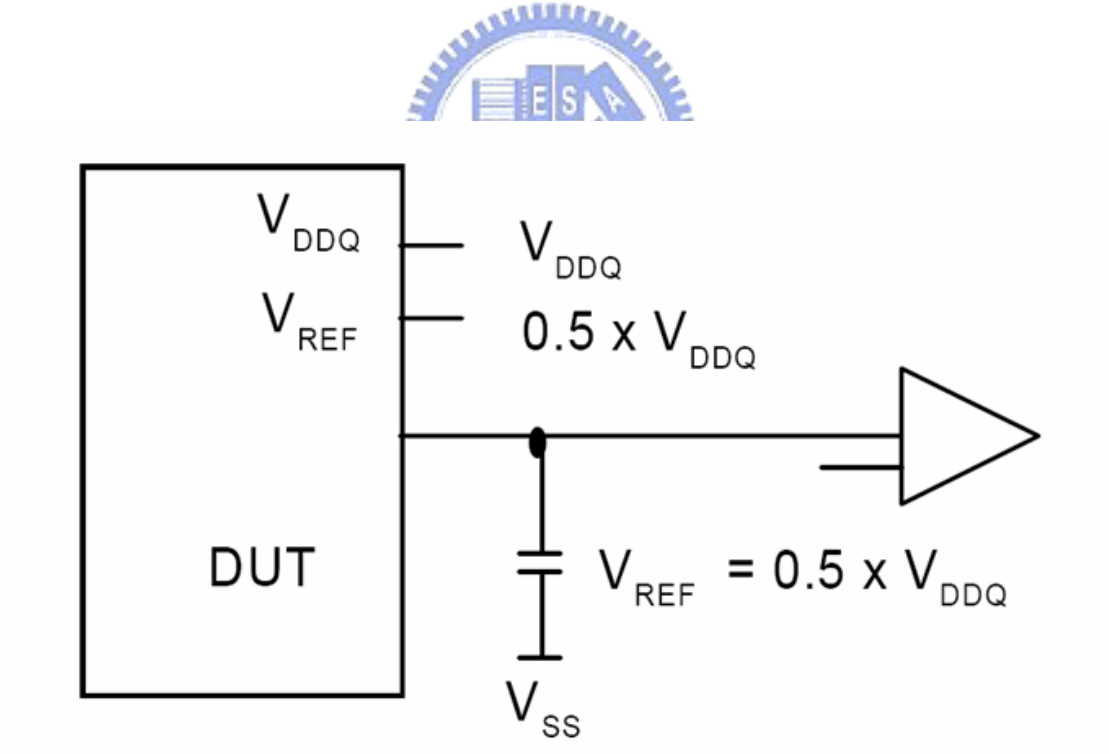

Fig. 3.6 SSTL_2 Unterminated Output Load

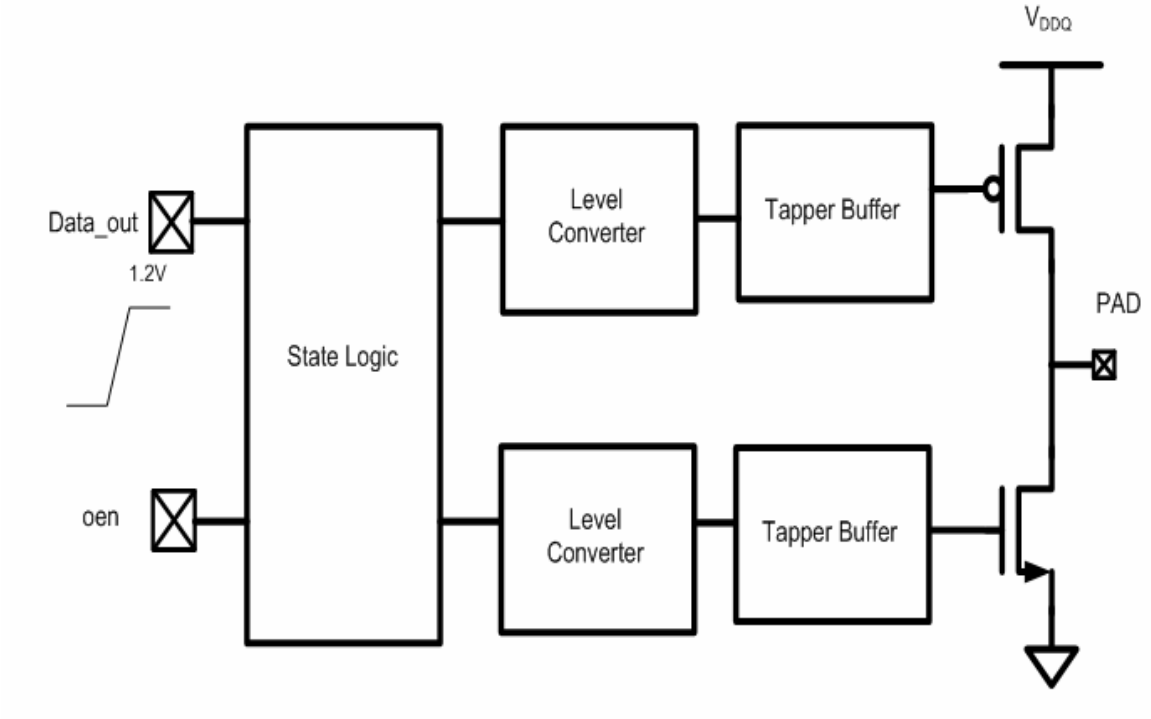

Fig. 3.7 Block Diagram of SSTL_2 Transmitter

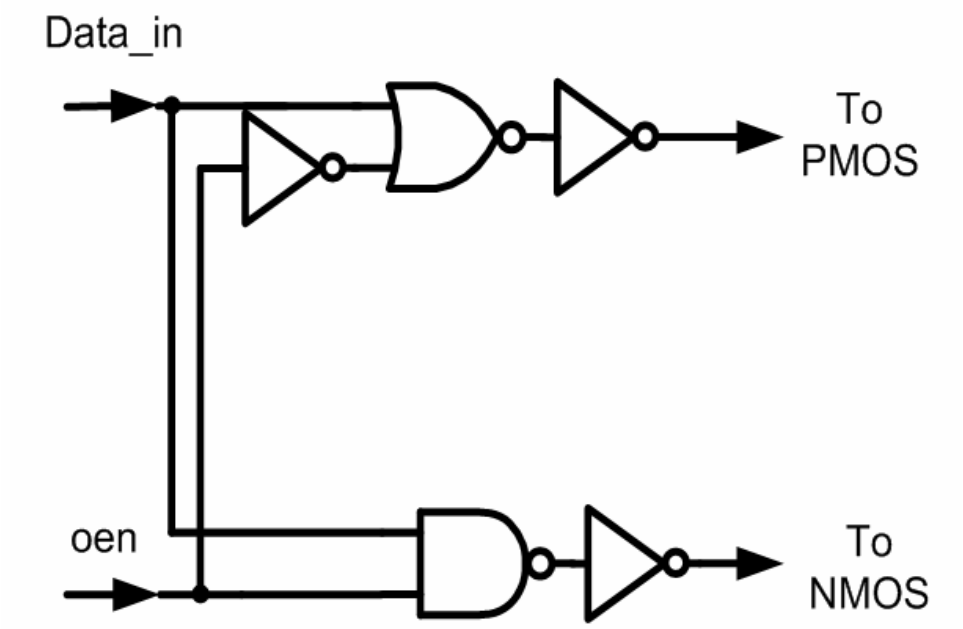

Fig. 3.8 Schematic of State Logic

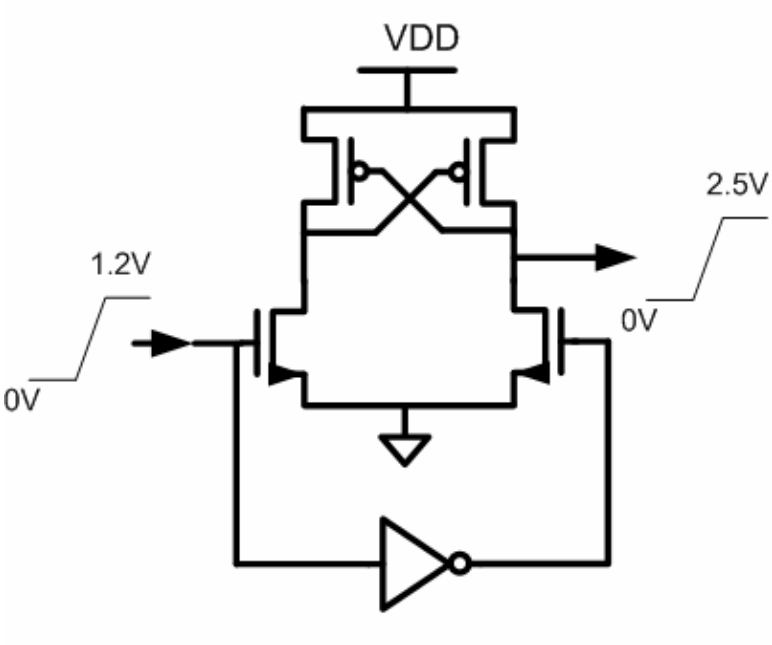

Fig. 3.9 Schematic of Level Converter

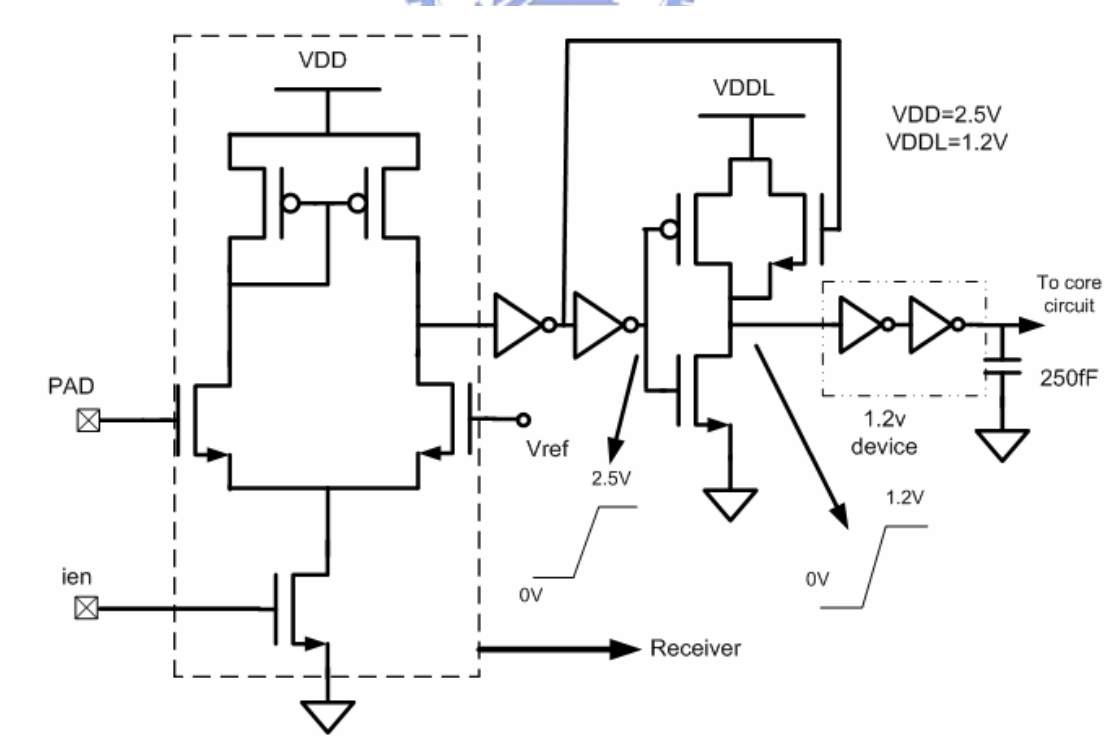

Fig. 3.10 Schematic of SSTL_2 Receiver

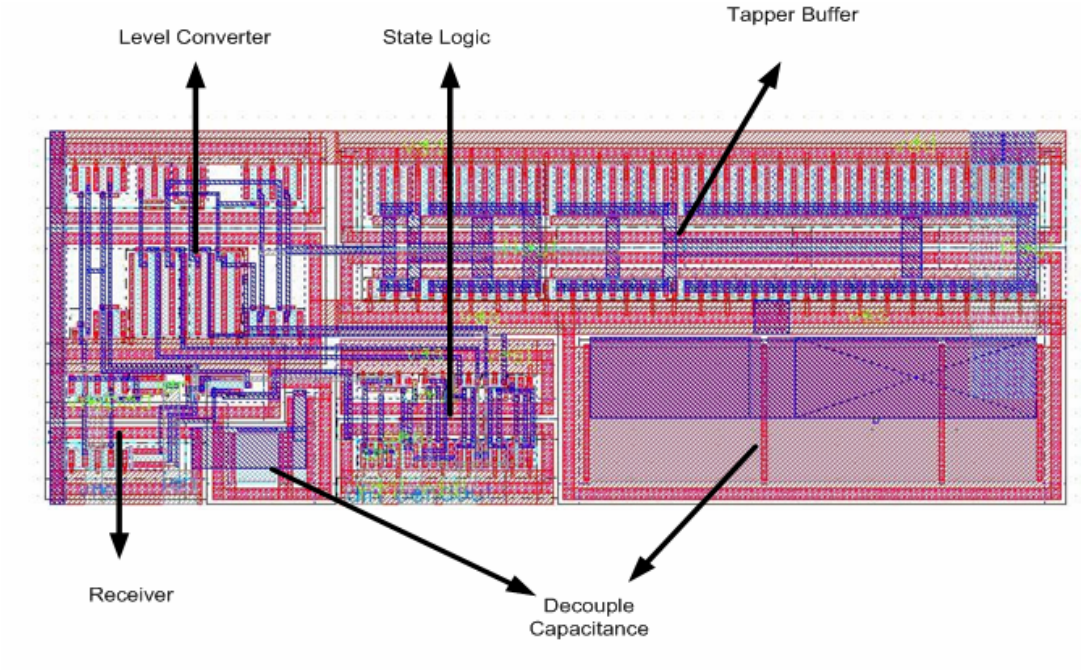

Fig. 3.11 Control Circuit of SSTL_2 Class_I type

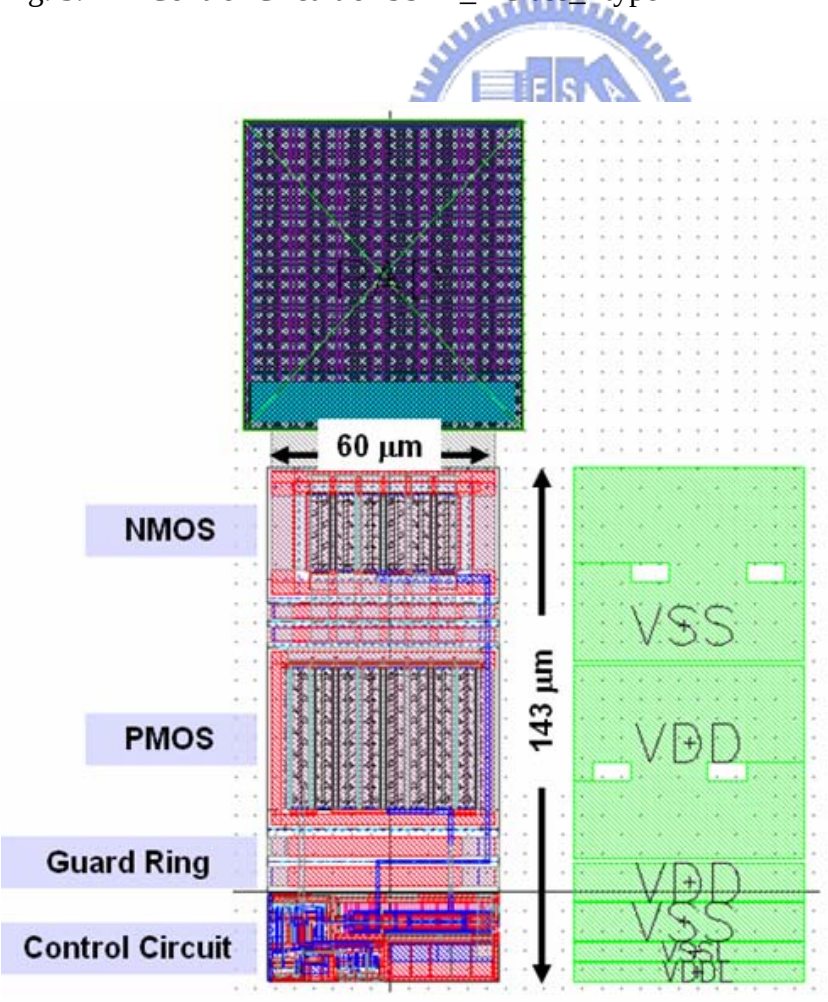

Fig. 3.12 SSTL_2 Class_I type I/O Circuit

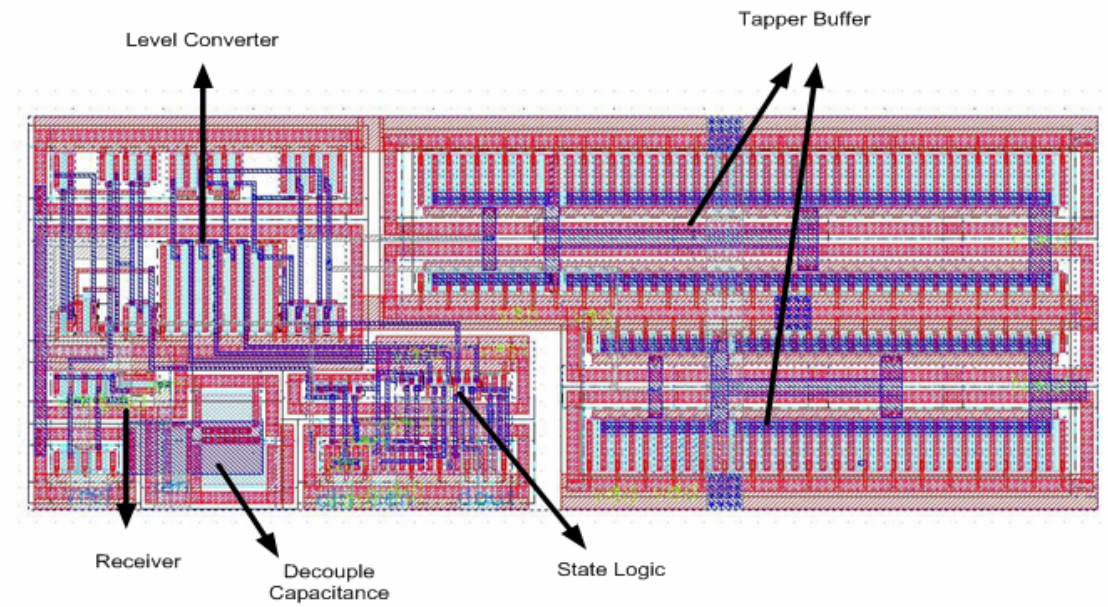

Fig. 3.13 Control Circuit of SSTL_2 Class_II type

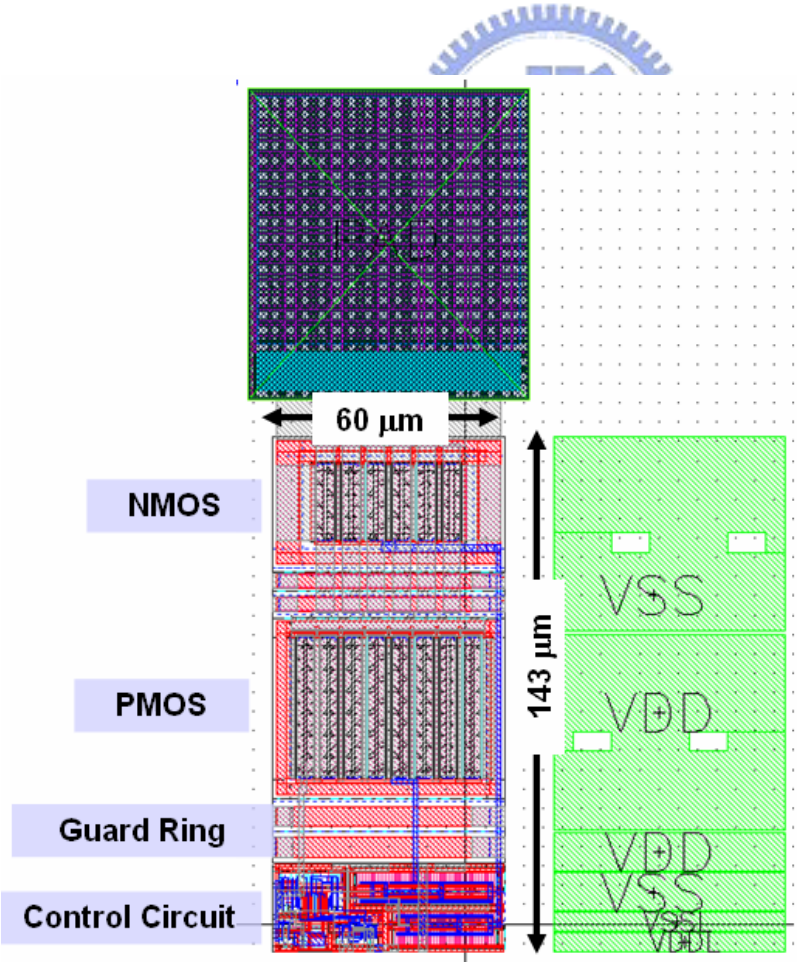

Fig. 3.14 SSTL_2 Class_II type I/O Circuit

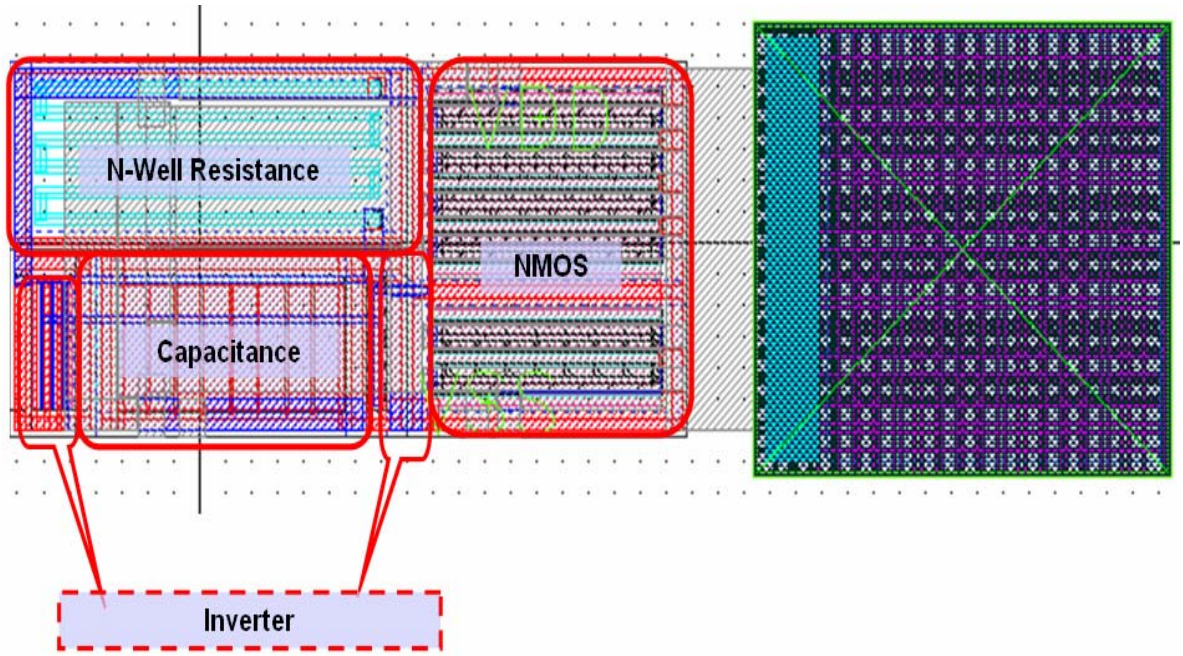

Fig. 3.15 2.5V ESD Protection Circuit

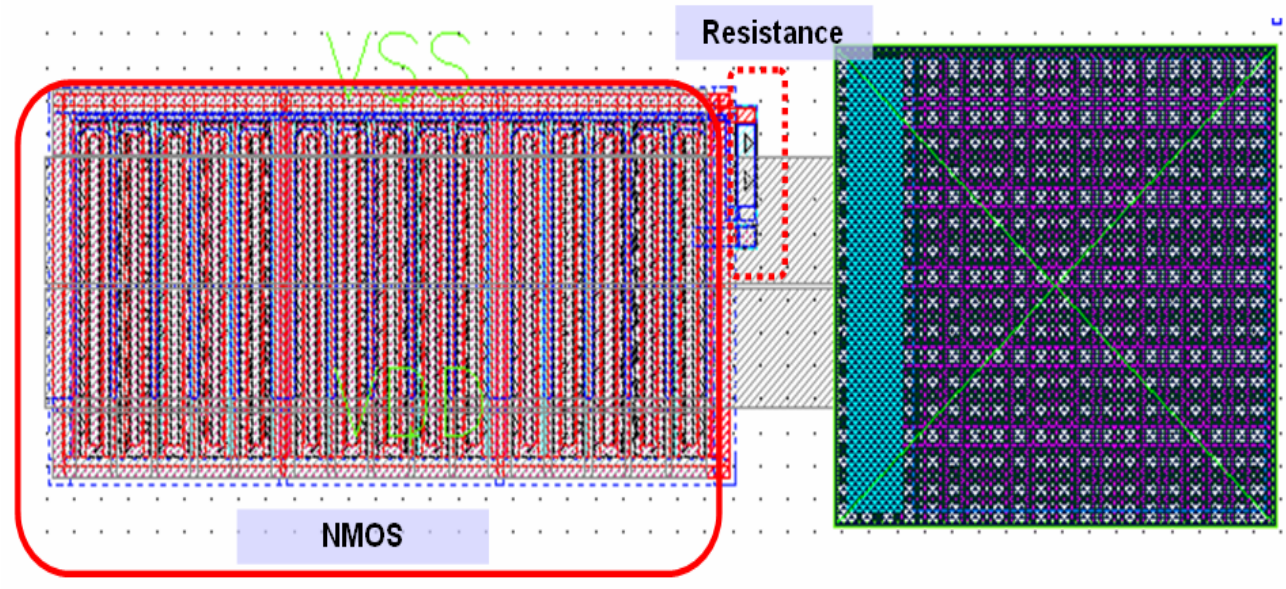

Fig. 3.16 1.2V ESD Protection Circuit

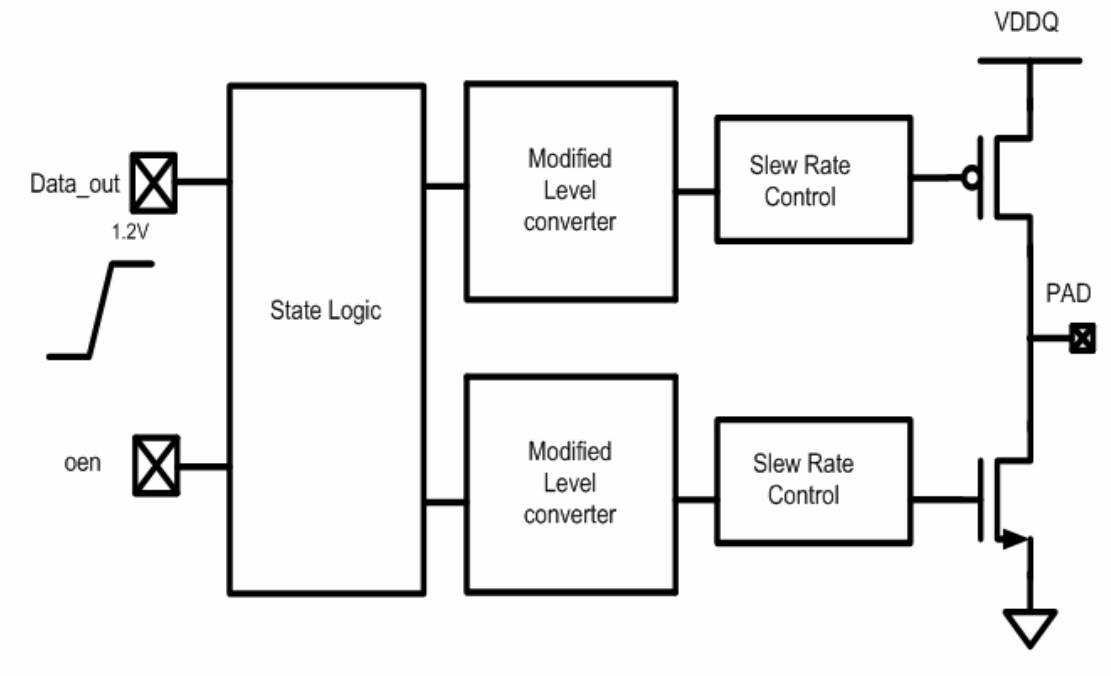

Fig. 3.17 Block Diagram of SSTL_2 with Slew Rate Control

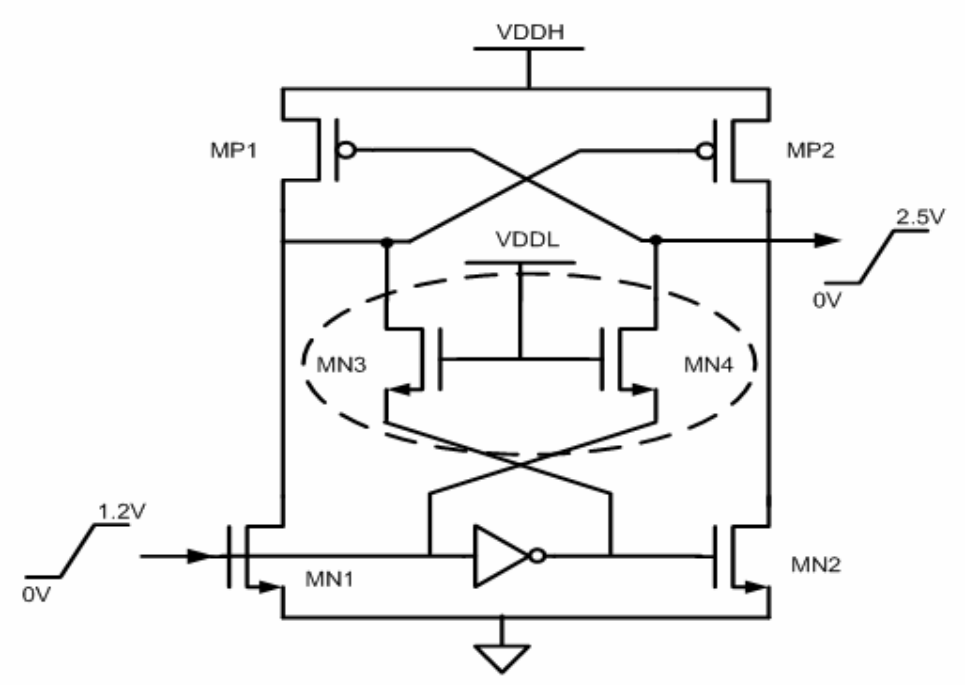

Fig. 3.18 Modified Level Converter

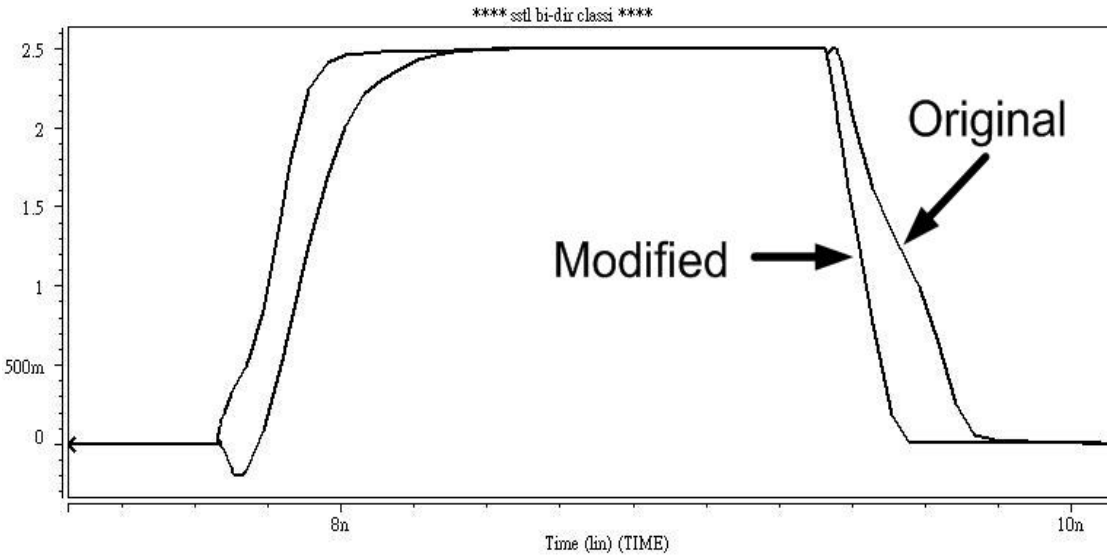

Fig. 3.19 Comparison of the Level Converter Simulation Result

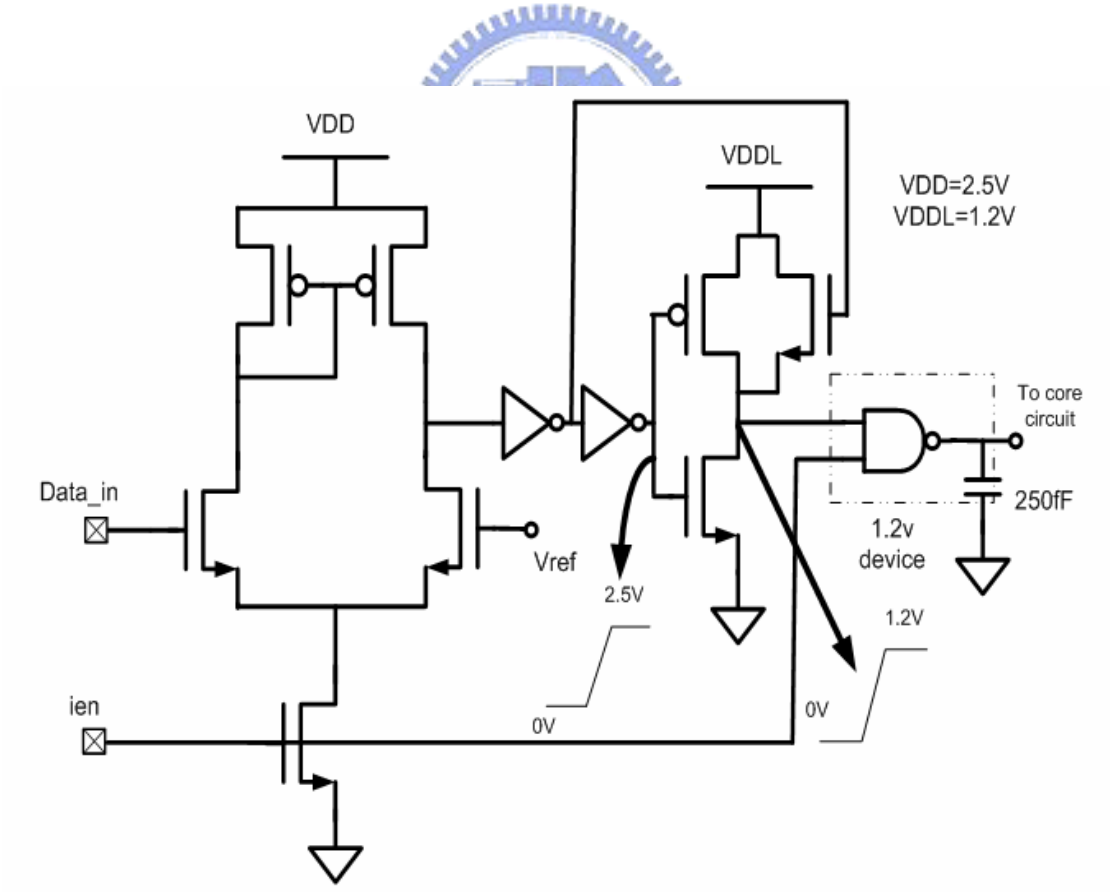

Fig. 3.20 Modified Receiver

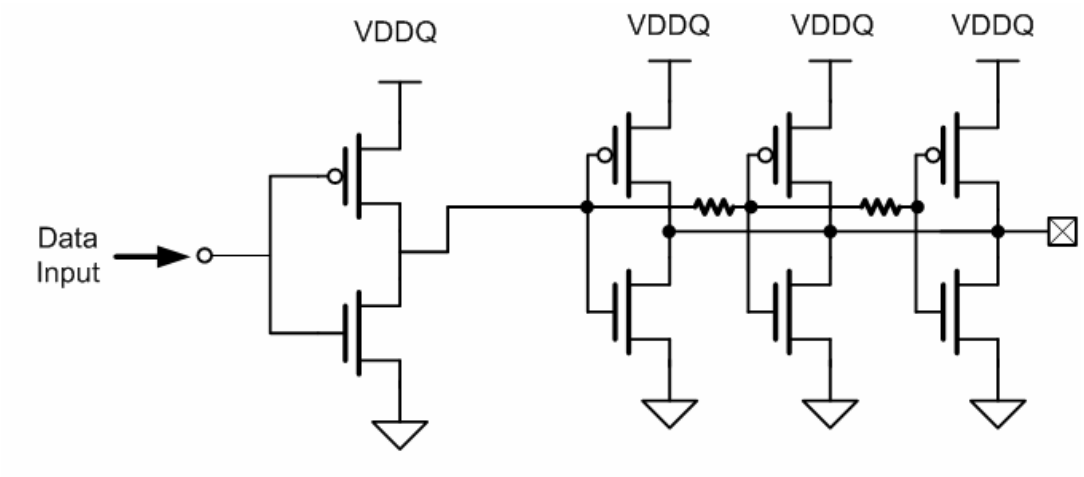

Fig. 3.21 Conventional Slew Rate Control Circuit of Output Buffer

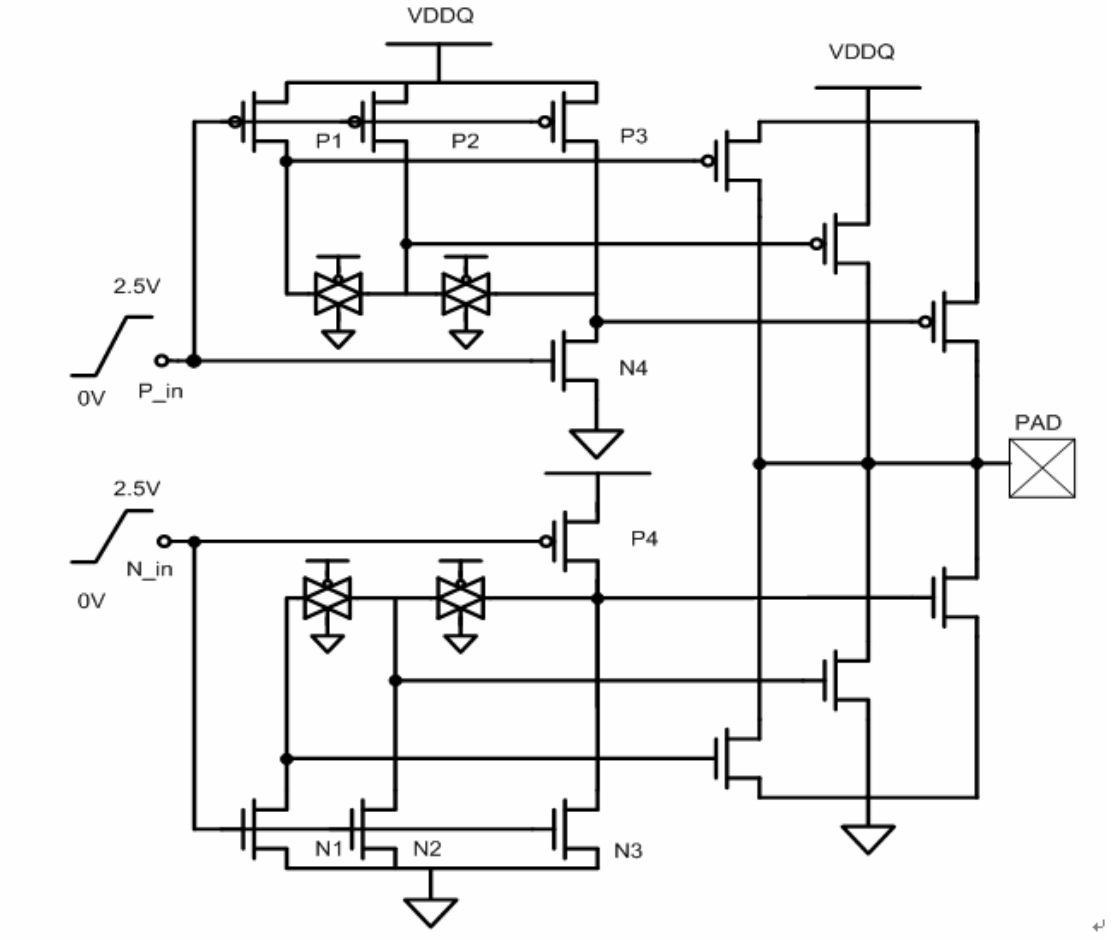

Fig. 3.22 Modified Slew Rate Control Circuit of Output Buffer

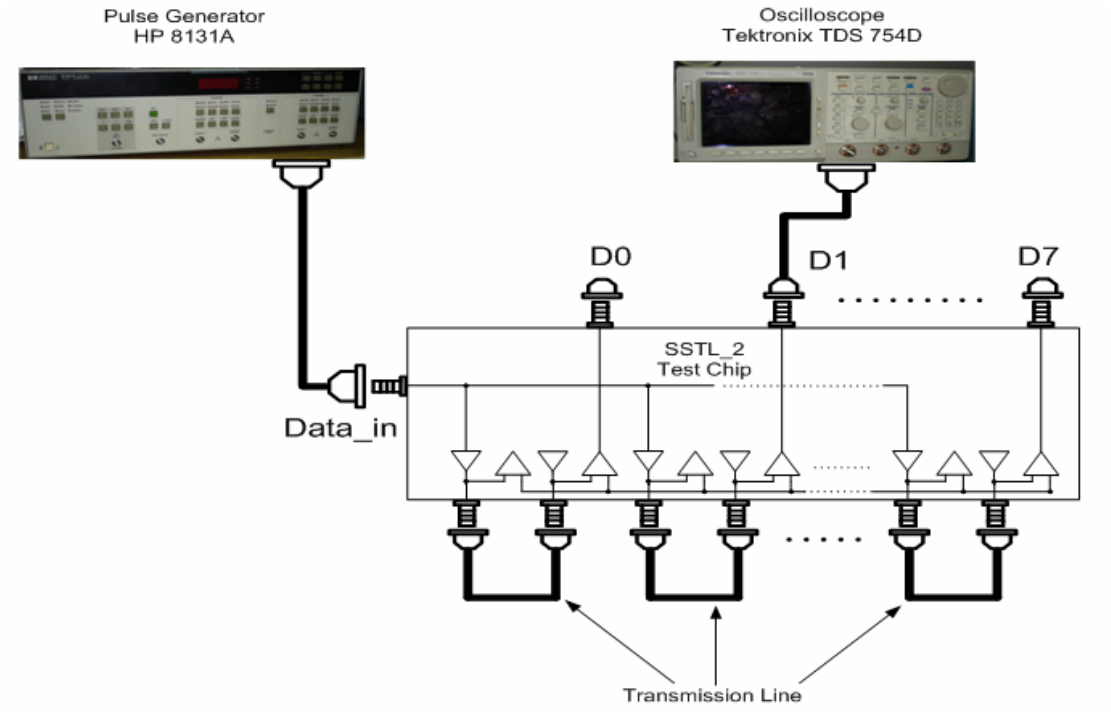

Fig. 3.23 Measurement Environment Setup

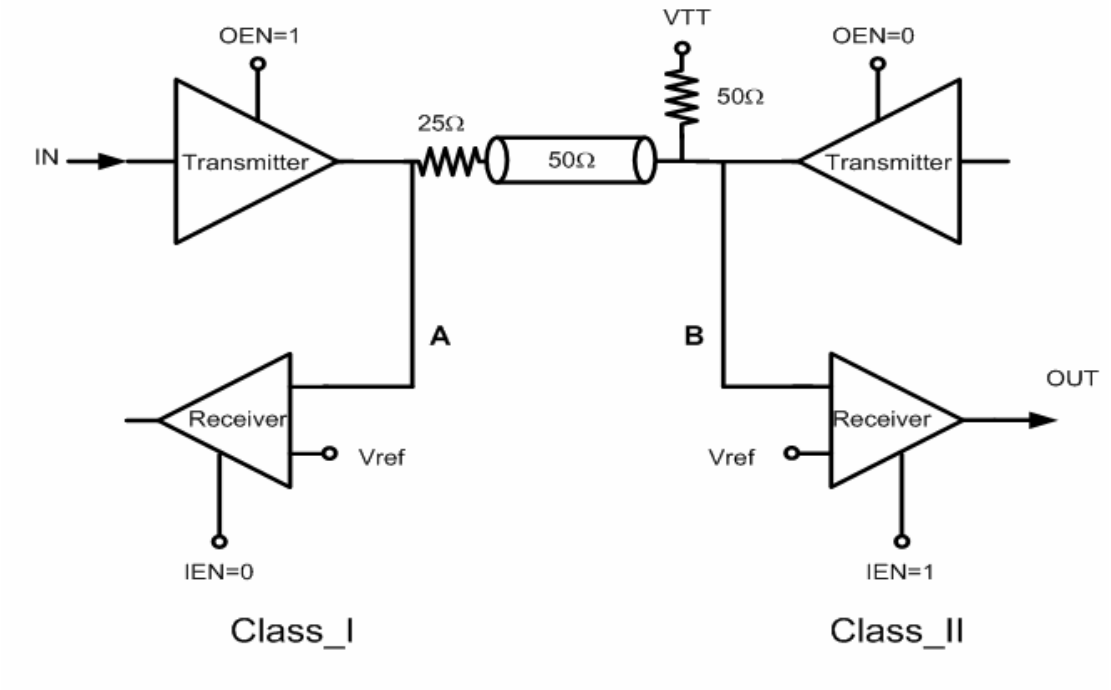

Fig. 3.24 Class_I Test Circuit

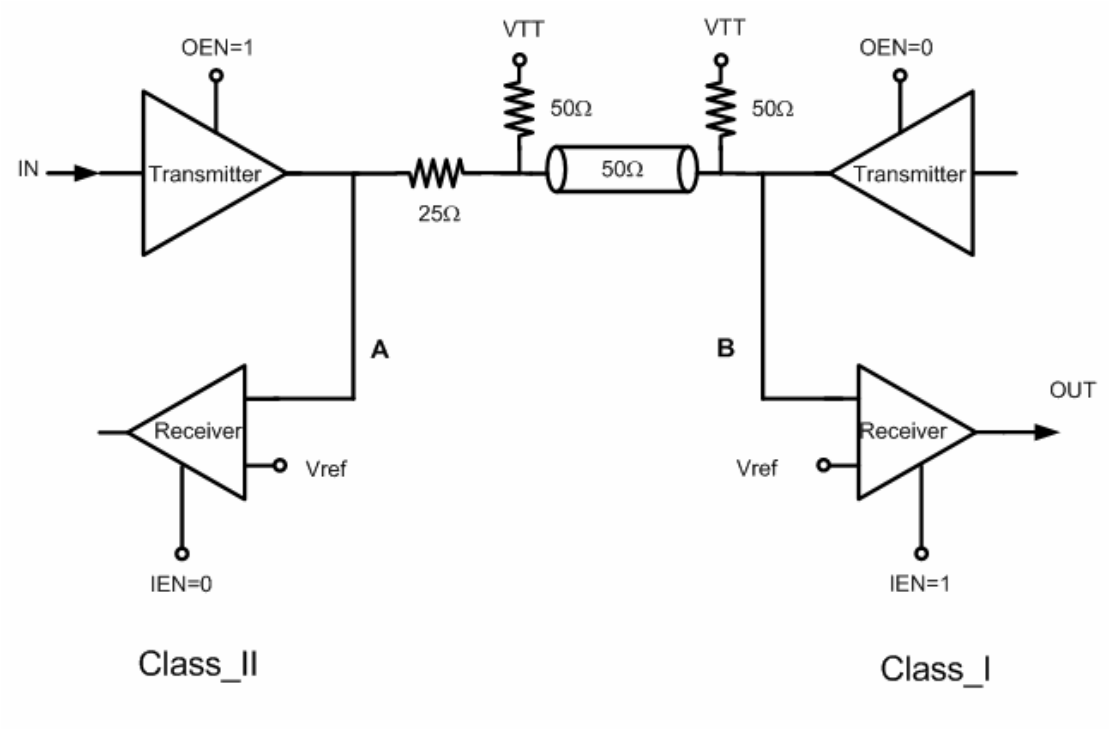

Fig. 3.25 Class_II Test Circuit

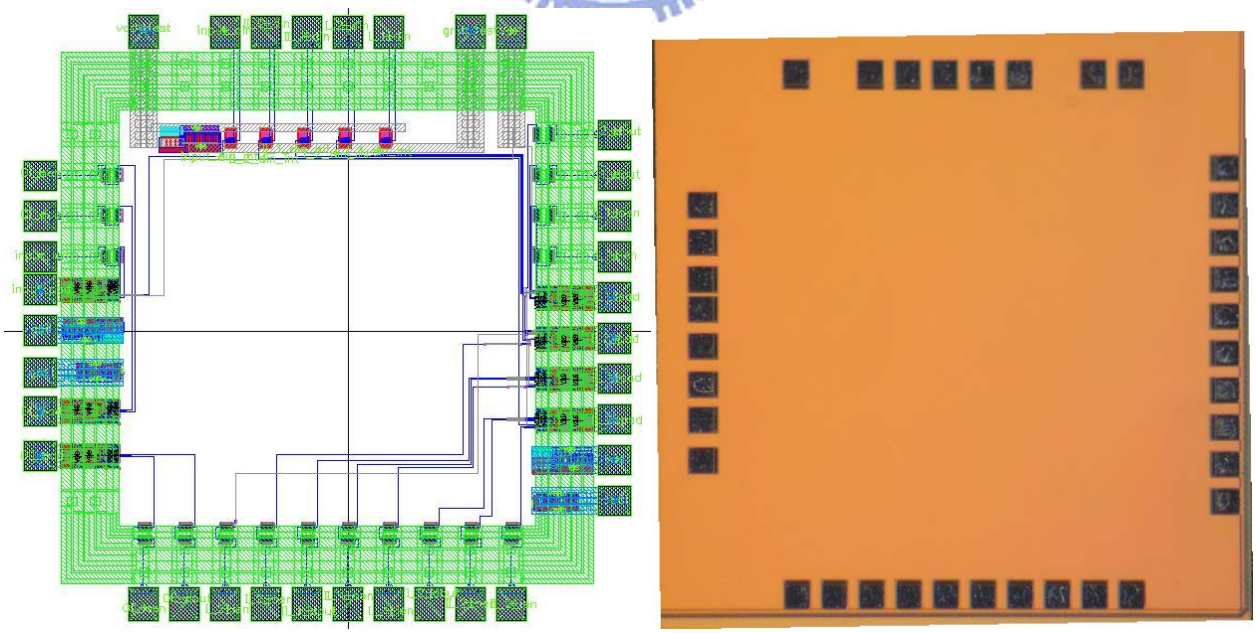

Fig. 3.26 The Die Photo and Layout of 1st tap-out

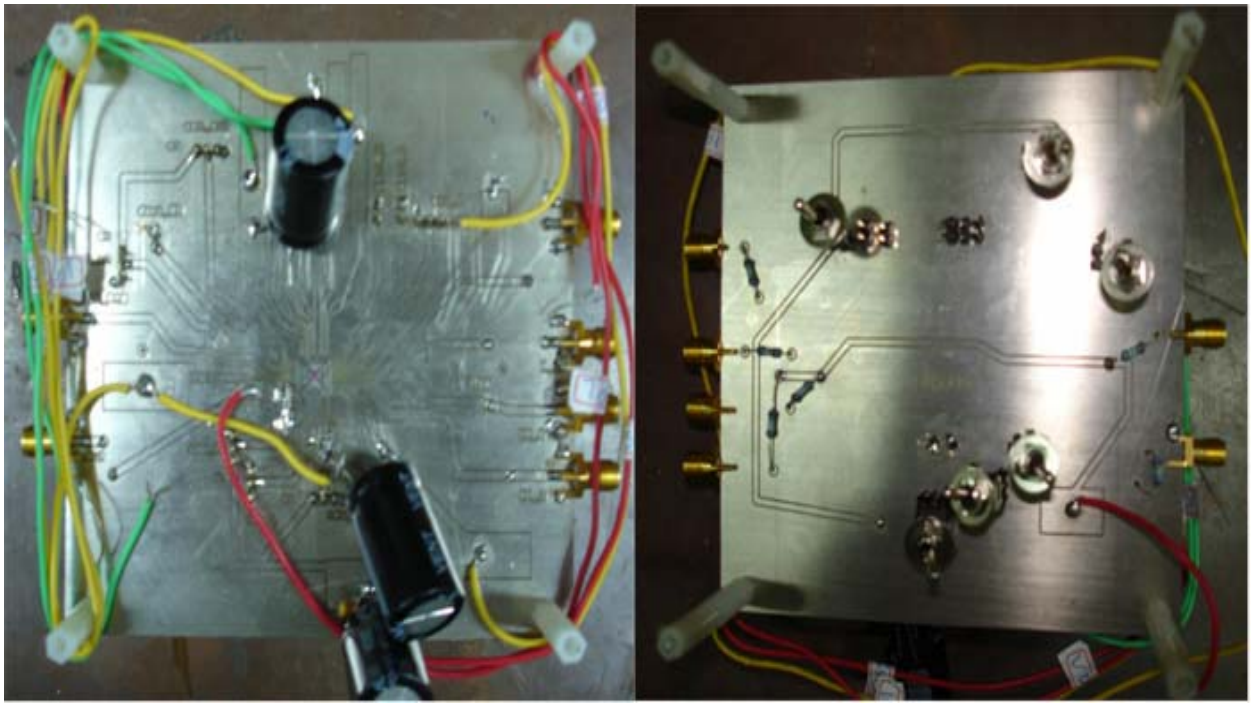

Fig. 3.27 PCB Board of 1st tap-out Class_I Test Circuit

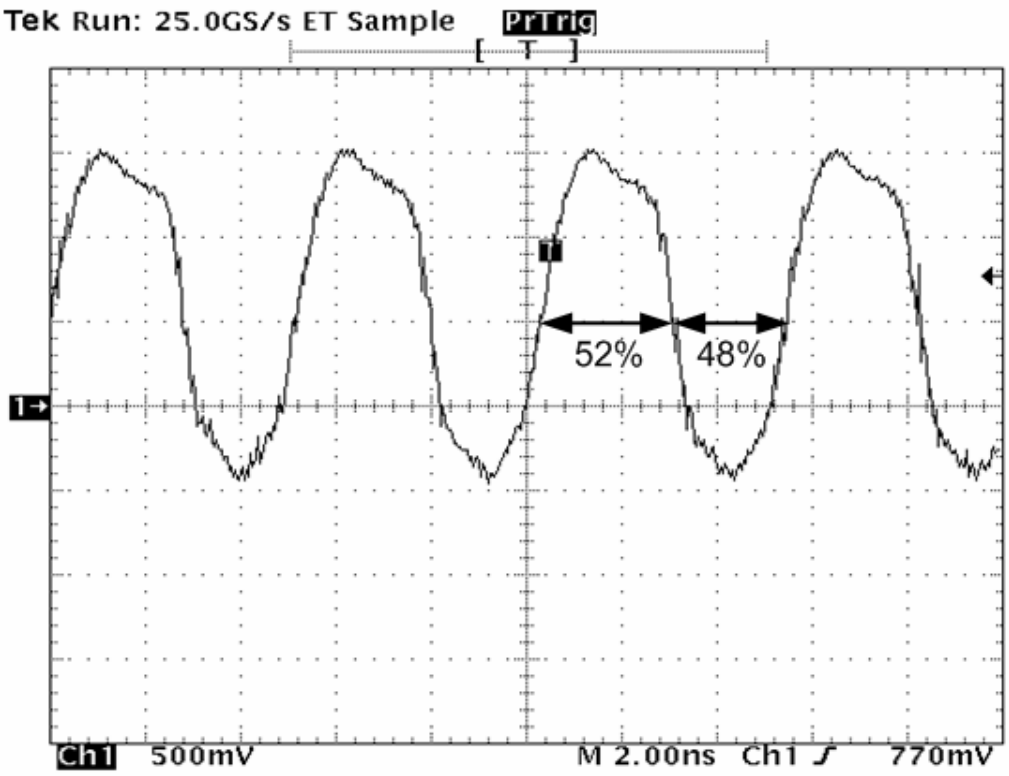

Fig. 3.28 Class_I Test Circuit Operated at 400 Mbps (200MHz)

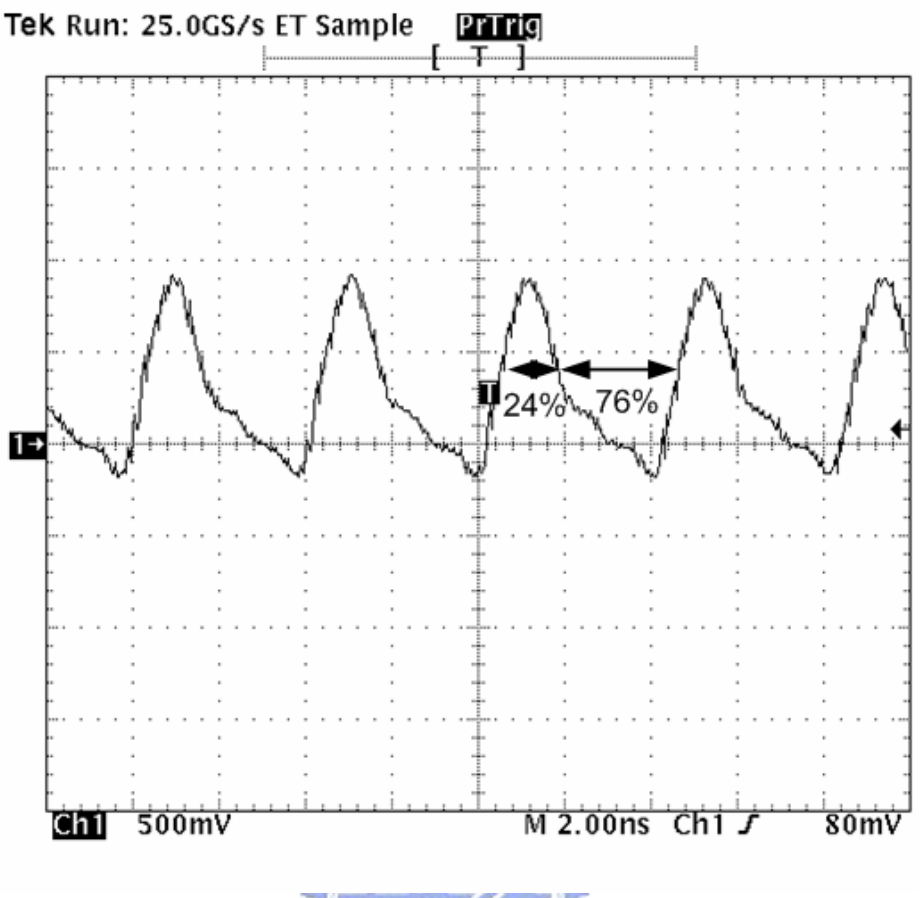

Fig. 3.29 Class_I Test Circuit Operated at 500 Mbps (250MHz)

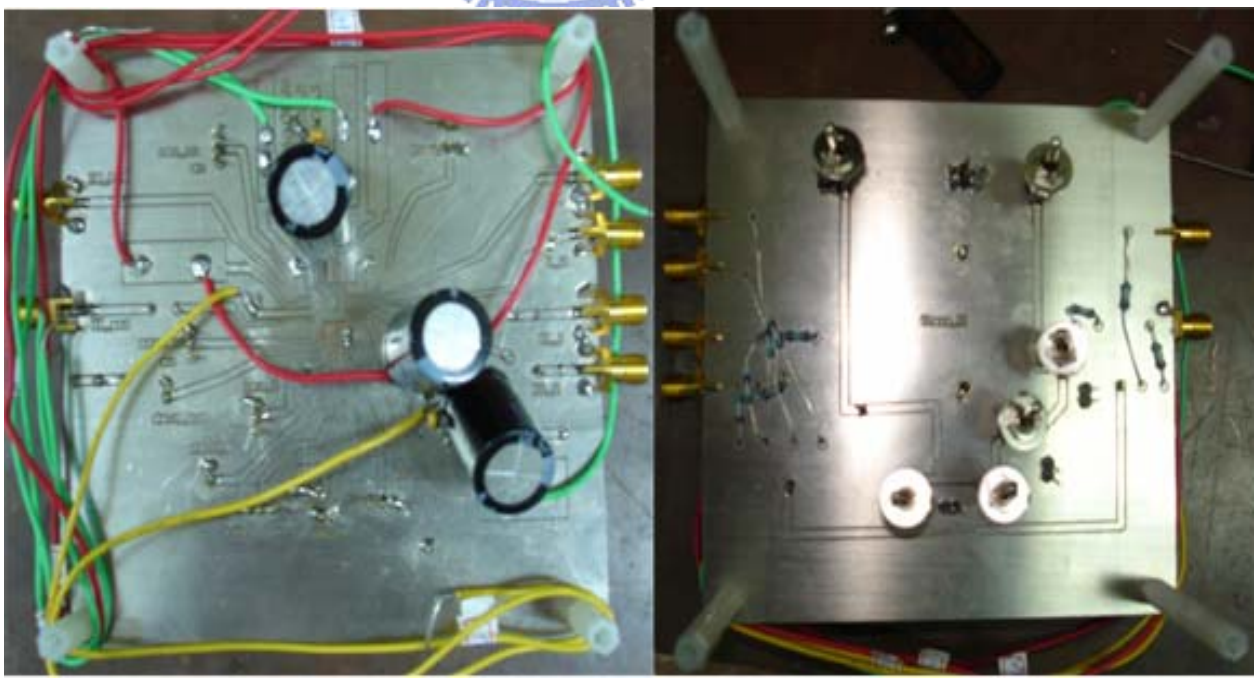

Fig. 3.30 PCB Board of 1st tap-out Class_II Test Circuit

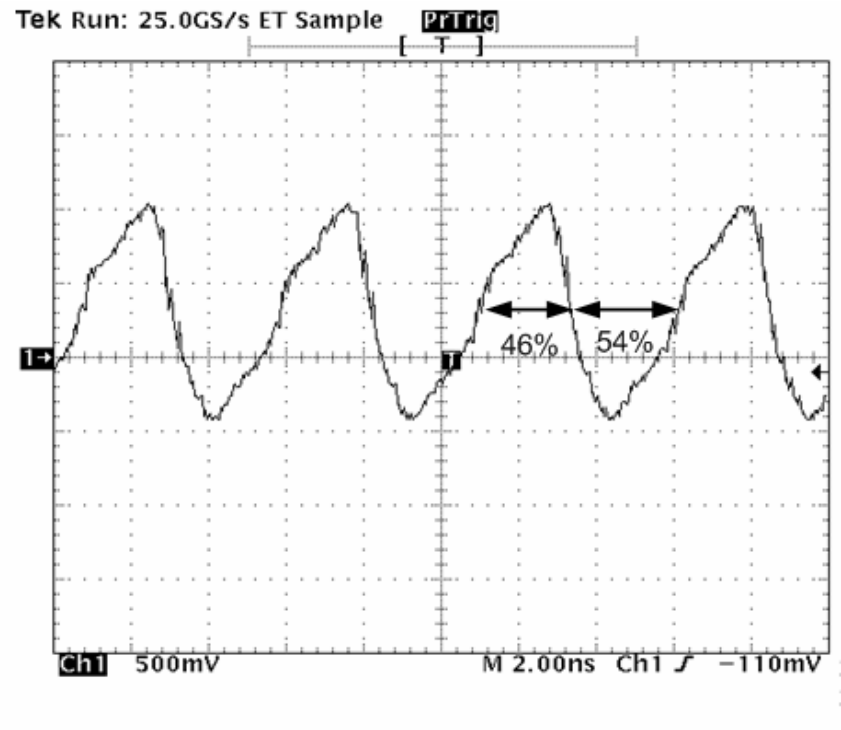

Fig. 3.31 Class_II Test Circuit Operated at 400 Mbps (200MHz)

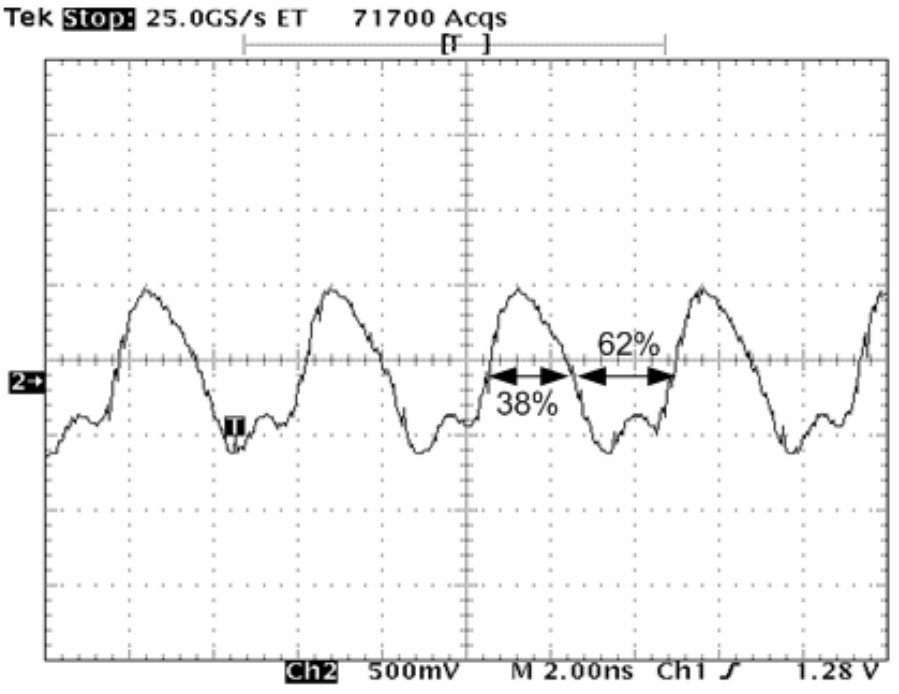

Fig. 3.32 Class_II Test Circuit Operated at 500 Mbps (250MHz)

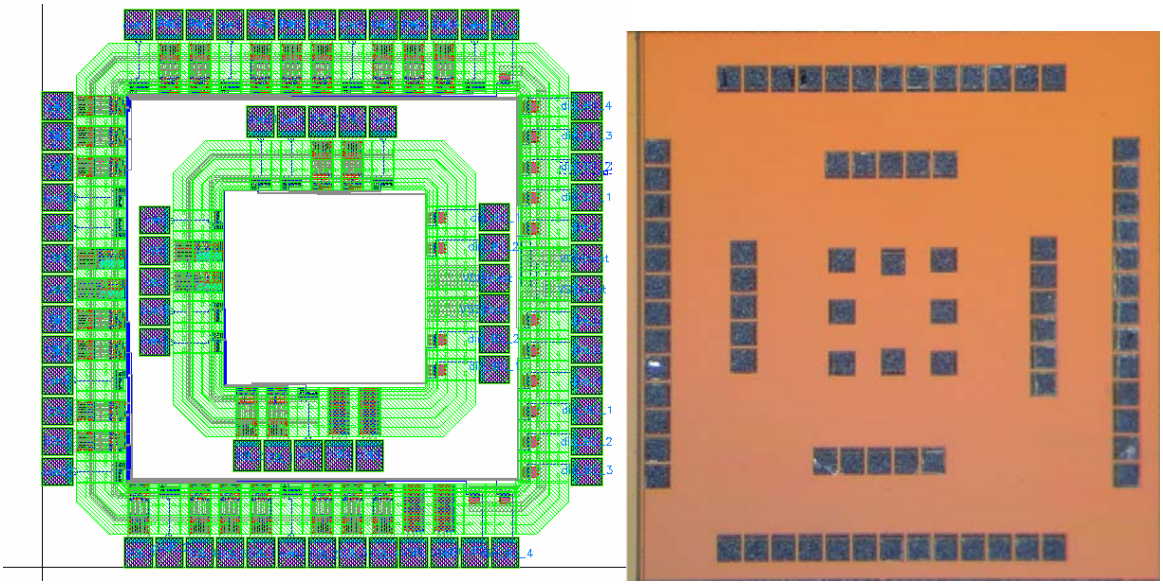

Fig. 3.33 The Die Photo and Layout of 2nd tap-out

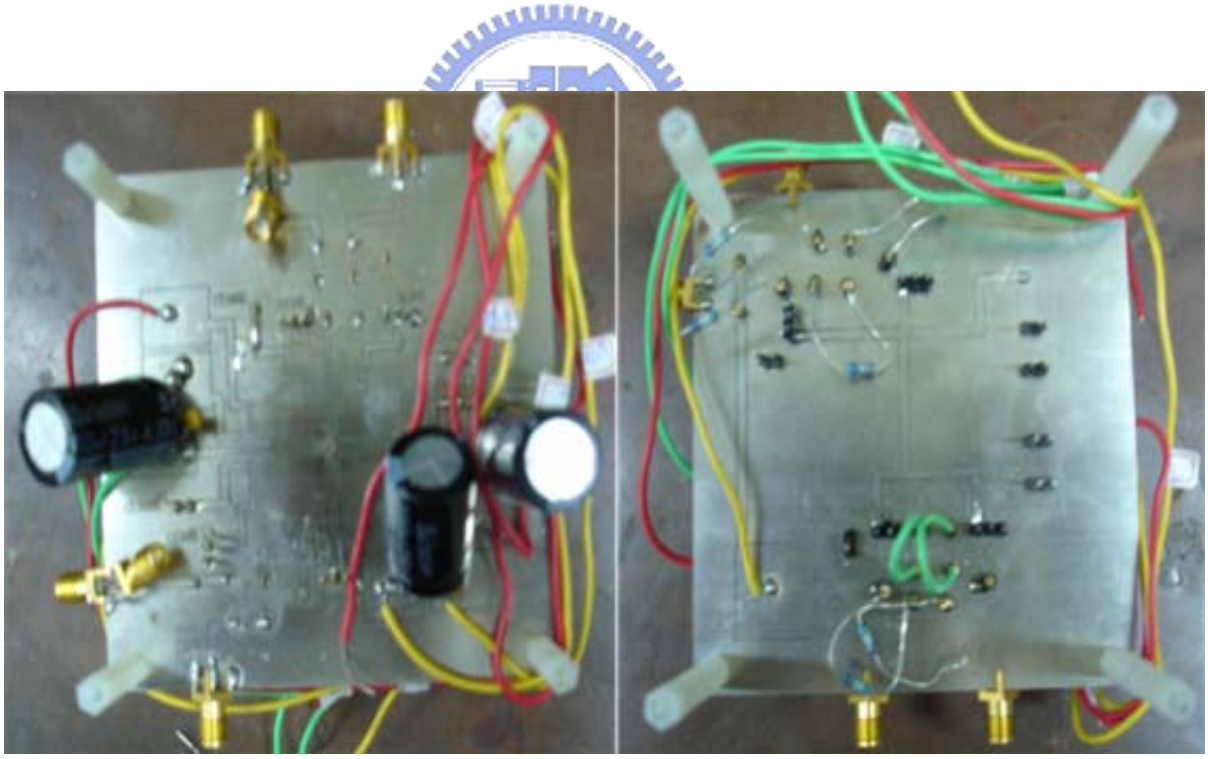

Fig. 3.34 PCB Board of 2nd tap-out Internal Circuit

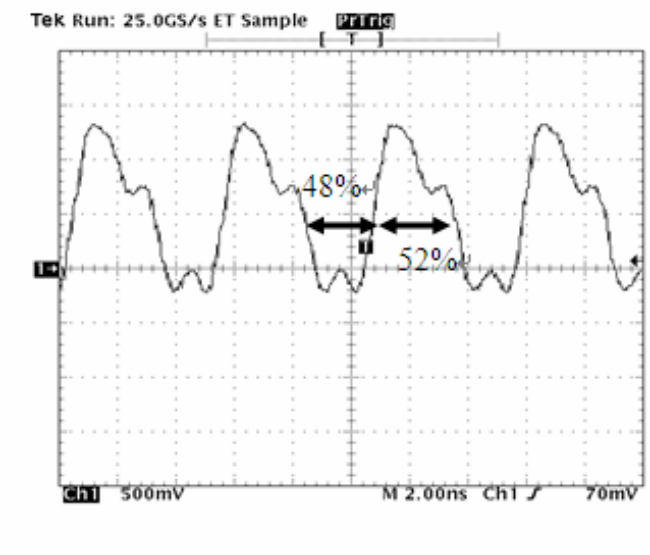

Fig. 3.35 Class_I Test Circuit Operated at 400 Mbps (200MHz)

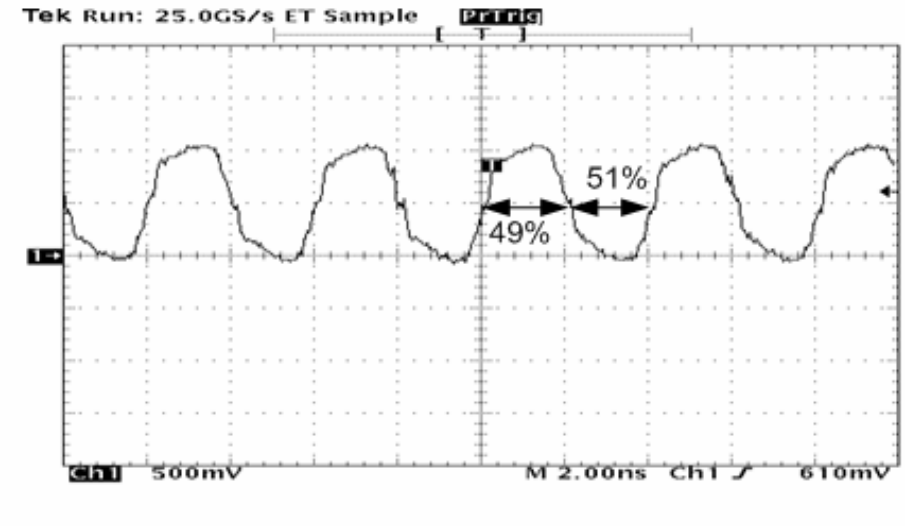

Fig. 3.36 Class_I Test Circuit Operated at 500 Mbps (250MHz)

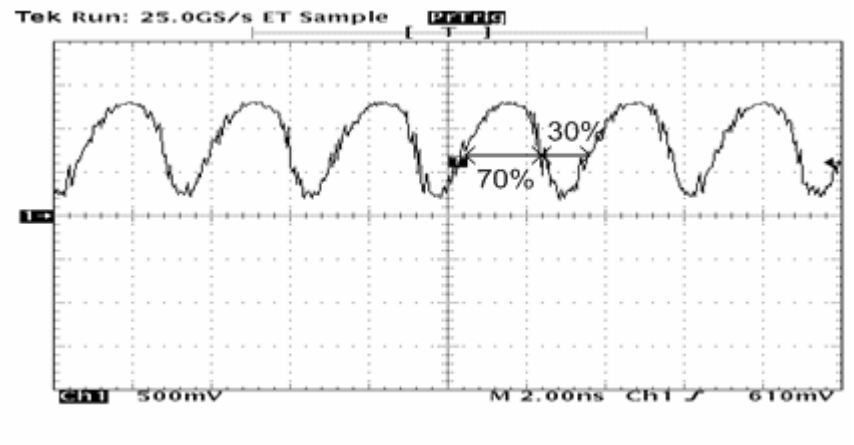

Fig. 3.37 Class_I Test Circuit Operated at 600 Mbps (300MHz)

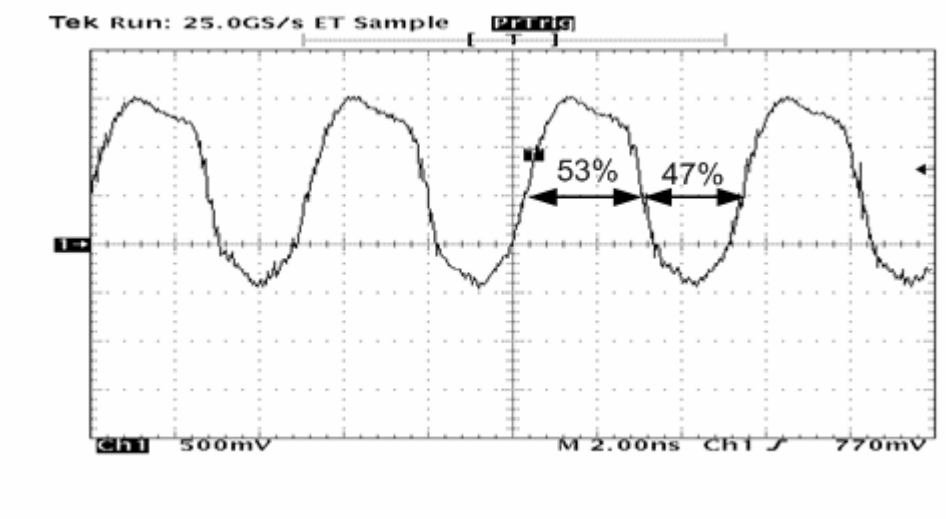

Fig. 3.38 Class_II Test Circuit Operated at 400 Mbps (200MHz)

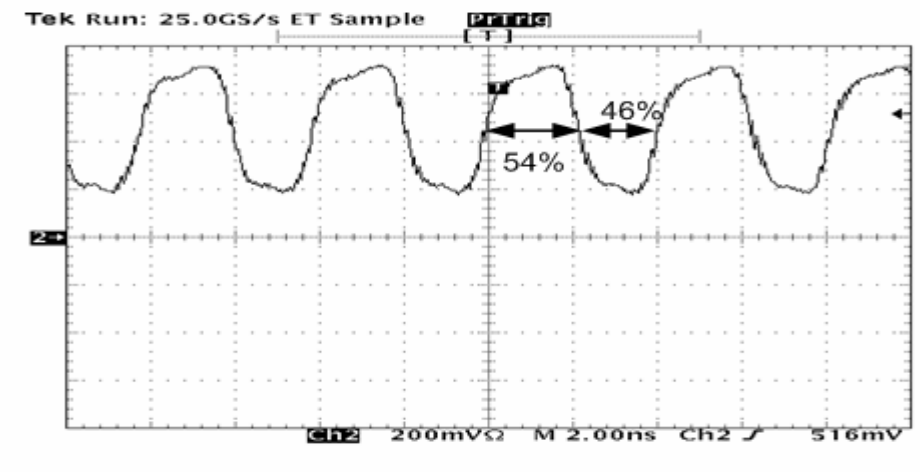

Fig. 3.39 Class_II Test Circuit Operated at 500 Mbps (250MHz)

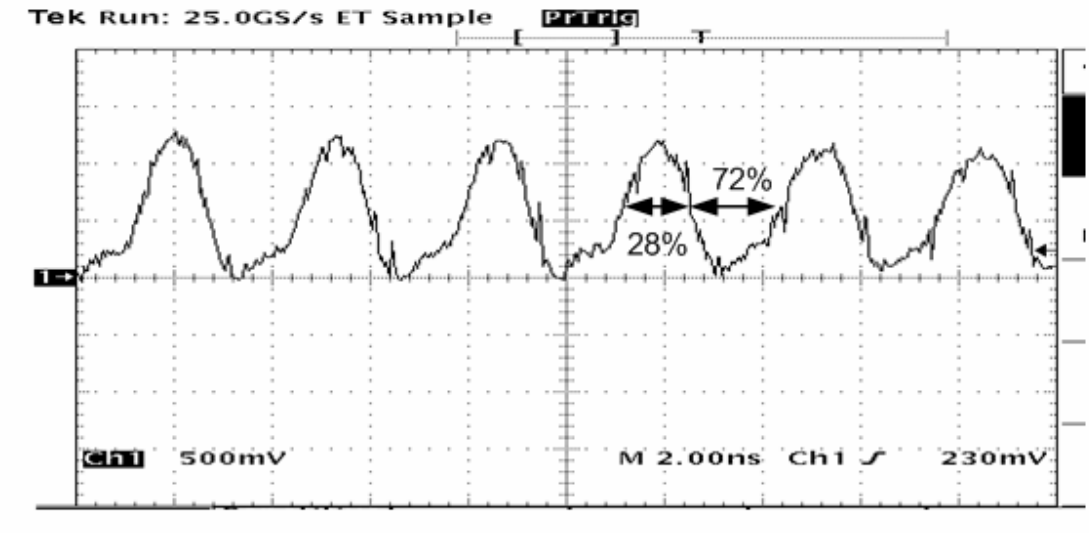

Fig. 3.40 Class_II Test Circuit Operated at 600 Mbps (300MHz)

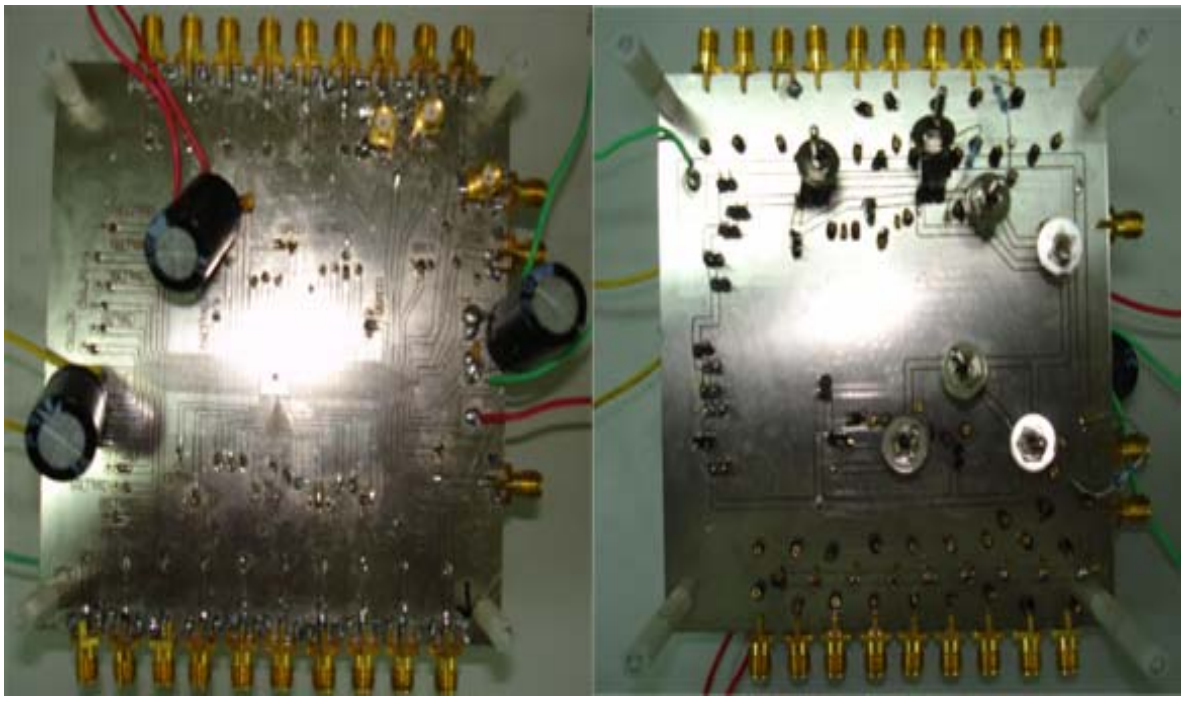

Fig. 3.41 PCB Board of 2nd tap-out Internal Circuit

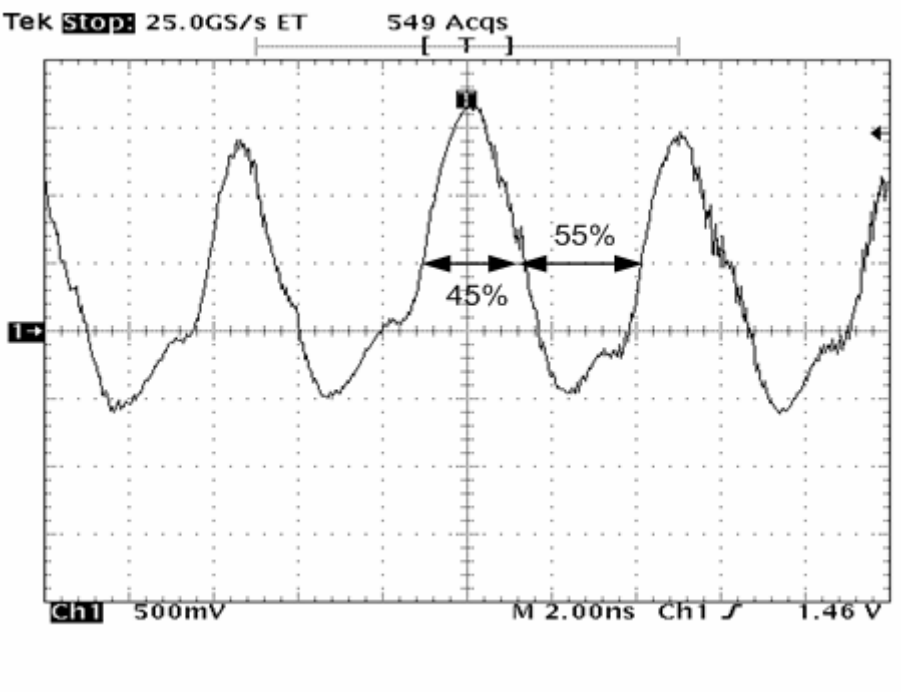

Fig. 3.42 1 bit Class_I Test Circuit Operated at 400 Mbps (200MHz)

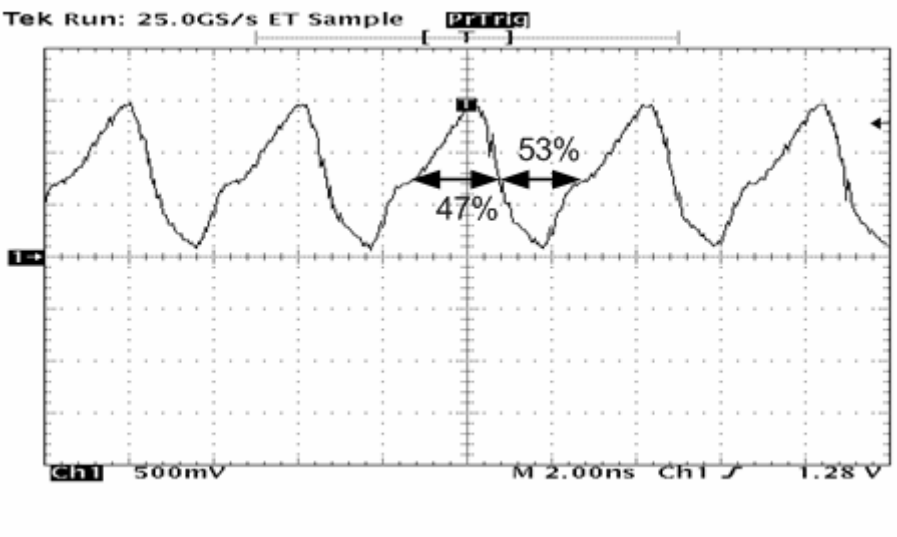

Fig. 3.43 1 bit Class_I Test Circuit Operated at 500 Mbps (250MHz)

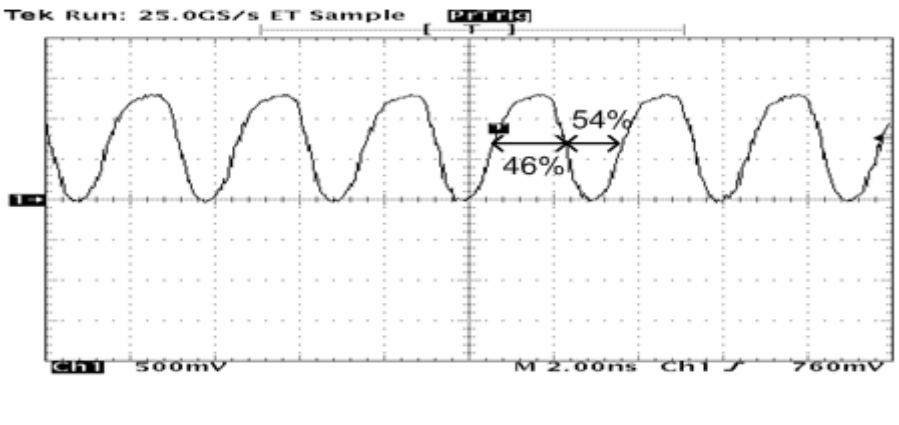

Fig. 3.44 1 bit Class_I Test Circuit Operated at 600 Mbps (300MHz)

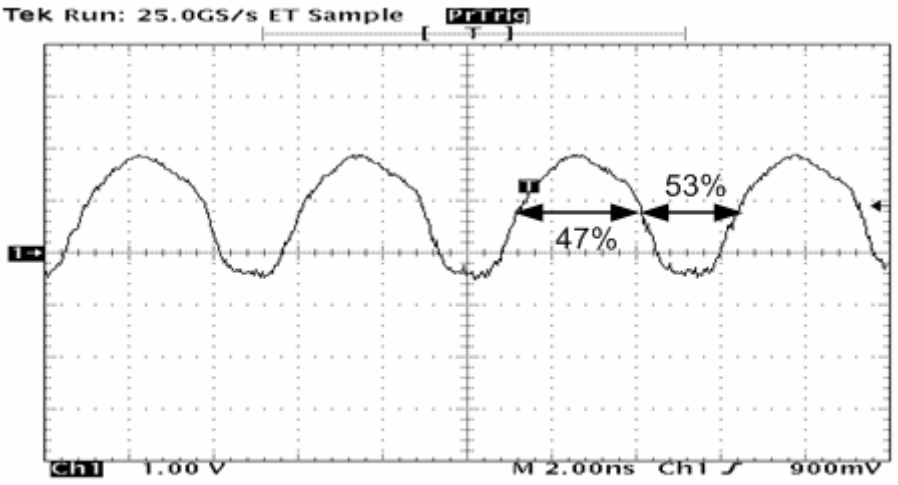

Fig. 3.45 1 bit Class_II Test Circuit Operated at 400 Mbps (200MHz)

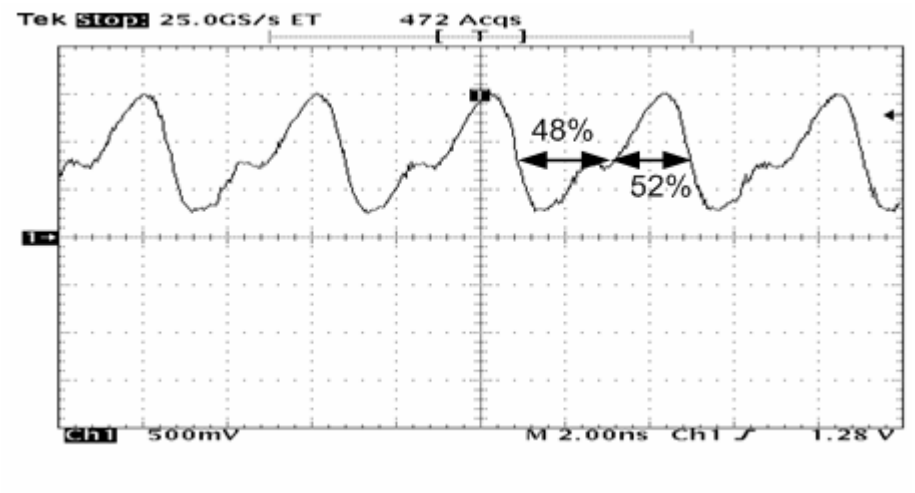

Fig. 3.46 1 bit Class_II Test Circuit Operated at 500 Mbps (250MHz)

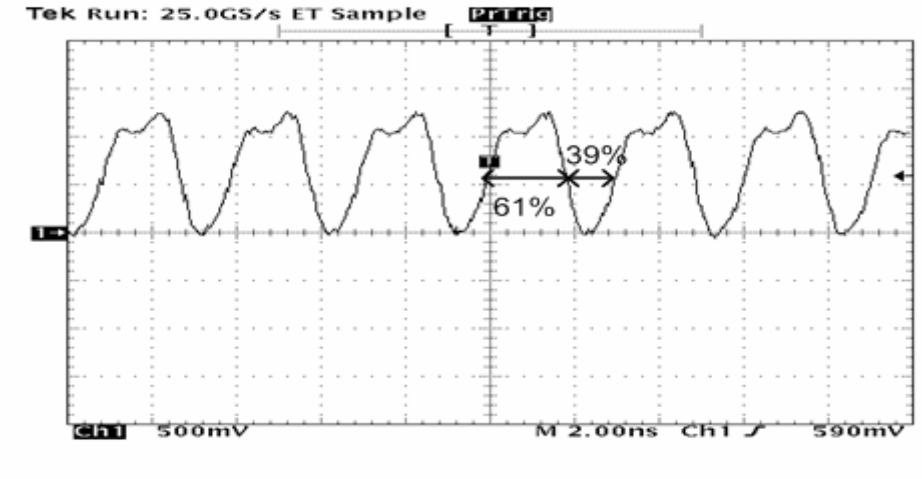

Fig. 3.47 1 bit Class_II Test Circuit Operated at 600 Mbps (300MHz)

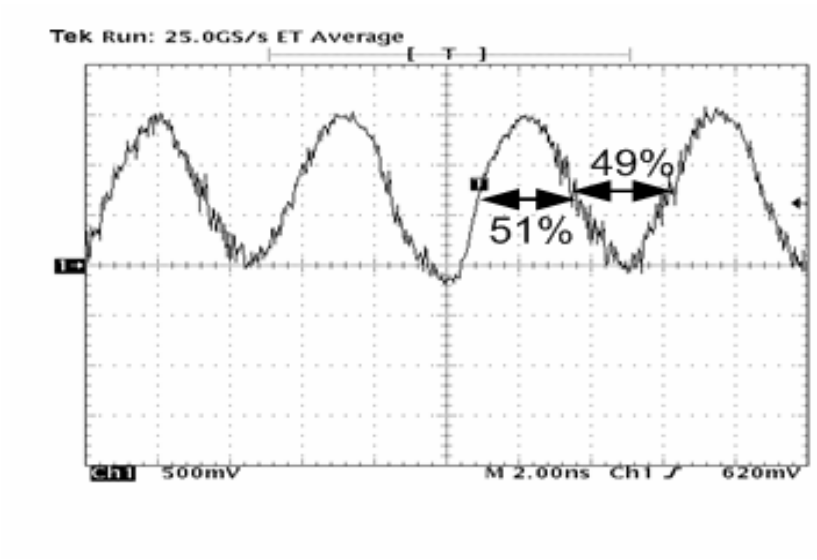

Fig. 3.48 8 bits Class_I Test Circuit Operated at 400 Mbps (200MHz)

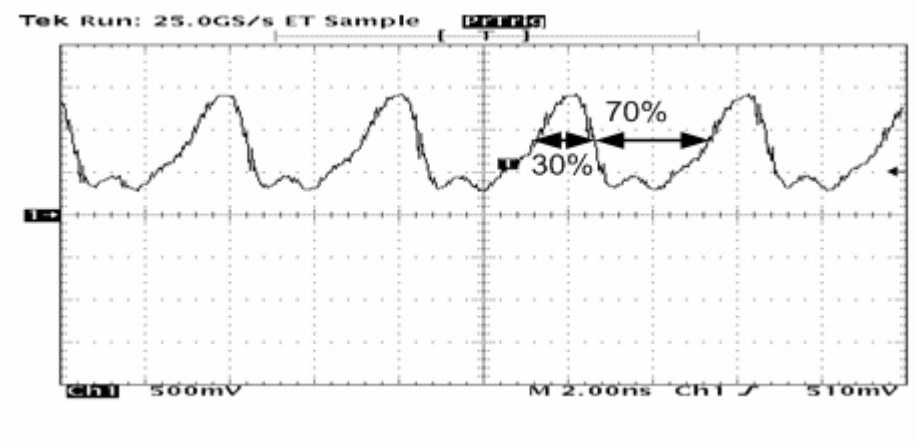

Fig. 3.49 8 bits Class_I Test Circuit Operated at 500 Mbps (250MHz)

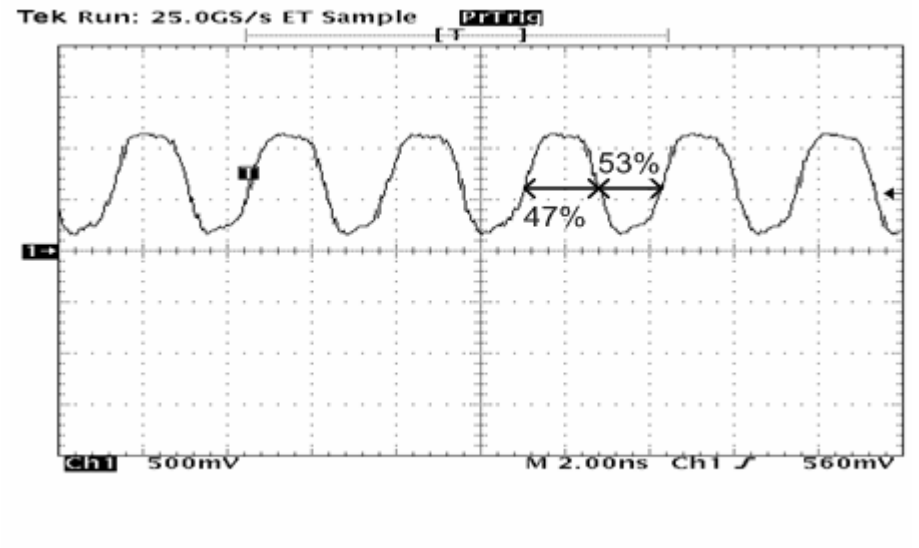

Fig. 3.50 8 bits Class_I Test Circuit Operated at 600 Mbps (300MHz)

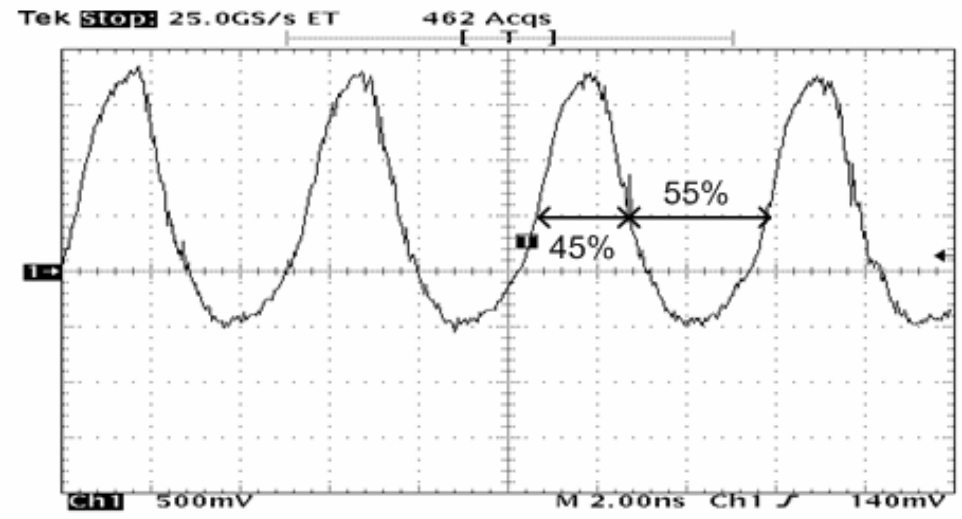

Fig. 3.51 8 bits Class_II Test Circuit Operated at 400 Mbps (200MHz)

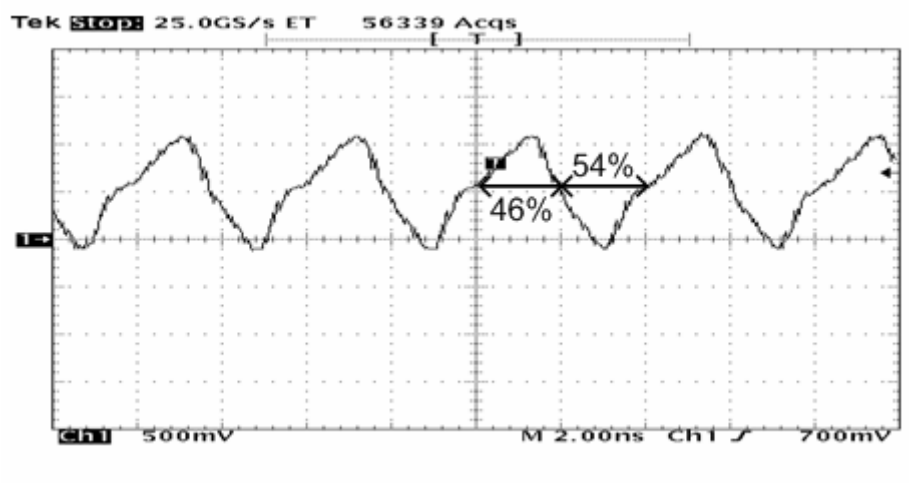

Fig. 3.52 8 bits Class_II Test Circuit Operated at 500 Mbps (250MHz)

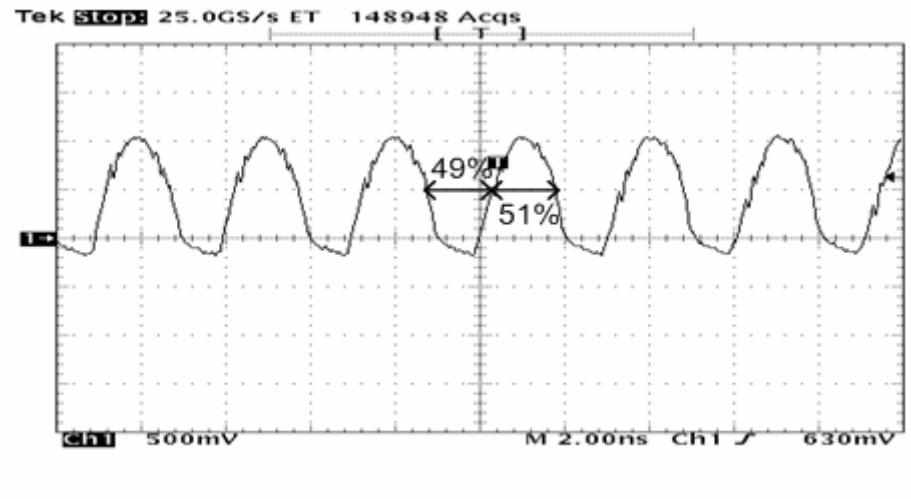

Fig. 3.53 8 bits Class_II Test Circuit Operated at 600 Mbps (300MHz)

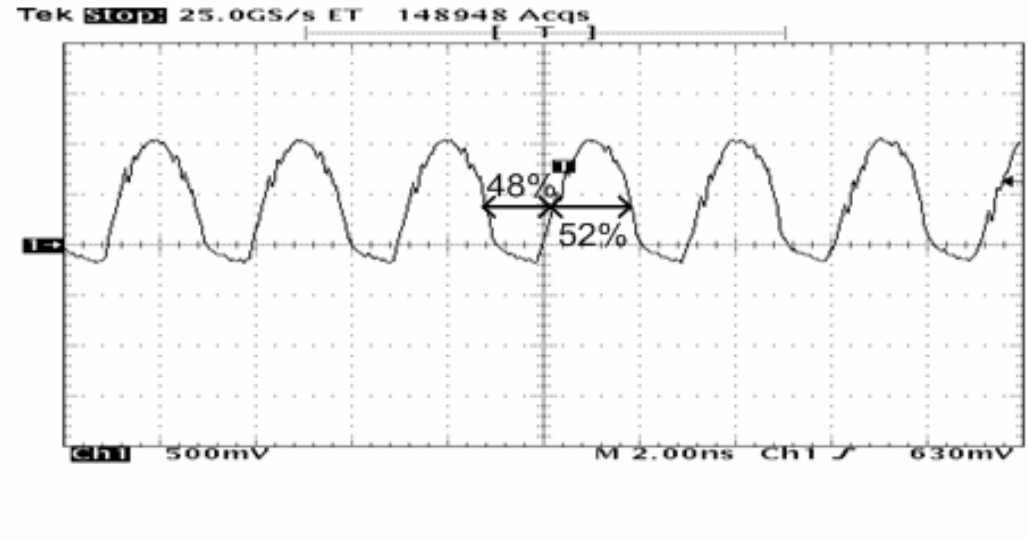

Fig. 3.54 8 bits Class_II Test Circuit Operated at 666 Mbps (333MHz)

Chapter 4

Delay-Locked Loop

4.1 INTRODUCTION

DDR SDRAM is required a DLL (Delay-Locked Loop) circuits. The DLL circuit is designed to realize a fast access time and high operation frequencies by controlling and adjusting the time lag between the external clock and internal clock. As mentioned in previous chapter, the DLL is divided in three types architecture, digital, analog, and mixed-mode DLL architectures. The digital DLL architectures have the advantage of low power consumption and high operation frequency, and they have the disadvantage of more complex control circuits. The analog DLL architectures have the advantage of locking more precisely, and they have the disadvantage of high power consumption. The mixed-mode DLL architectures have the advantage of both digital and analog DLL architectures, and they have the disadvantage of large chip area and complex timing control. These types of DLL architectures have different advantages and disadvantages. Determining whether they are significant or not helps designer to decide which DLL architecture can be applied in the DDR SDRAM. Here, the digital DLL architectures applied in DDR SDRAM will be designed in this chapter.

4.2 BASIC DLL ARCHITECTURE

The conventional DLL architectures include delay line, decoder, up/down counter, arbiter, finite state machine (FSM), and comparator. The block diagram of

conventional DLL architecture is shown in Fig. 4.1. DLL applies the comparator to compare the feedback clock. There are many methods to fetch the feedback clock for comparison so that there are different ways to realize the comparator. Then, the arbiter will judge and send the command to the FSM. The FSM will decide whether the up/down counter should be increased or decreased. The decoder decodes the up/down counter data to control the delay line to adjust the internal clock to deduce the difference between external clock and internal clock. In next section the modified DLL architecture.

4.3 DLL CIRCUIT IMPLEMENTATION

This section discusses the modified DLL architecture, shown in Fig. 4.2. This DLL architecture compares the external clock and the internal clock every two clock cycles by applying the divider. The divider, shown in Fig. 4.3, is composed of a D Flip-Flop and an inverter. The output of the D Flip-Flop switches every two clock cycle by using the feedback inverter. The character of this DLL architecture is the hierarchical delay line. So the comparator must be divided to coarse delay comparator and fine delay comparator, respectively. In next sections, the functions of every block will be explained.

4.3.1 Delay Line

The delay line of modified DLL architecture includes coarse delay and fine delay for the hierarchical architecture. The delay line of fine delay will be discussed in section 4.3.4 for explaining more clearly. In this section, the delay line of coarse delay is the main subject. The coarse delay line receives the signal from fine delay line. The

basic stage of coarse delay is combined by inverter chains and capacitance. The schematic of the basic stage of coarse delay is shown in Fig. 4.4. The delay time of every stage is 900 ps, and every stage is divided to 6 minor stages. It is because that the largest delay time of fine delay is 150ps. For hierarchical delay line, it is significant that the difference between the largest fine delay time and the smallest coarse delay time must be reduced for decreasing the jitter cased by the discontinuous delay. The capacitances are applied to fit the delay time. For power consumption consideration, every stage applies a NAND gate to control whether the stage should be operated or not. If there is no NAND gate in the coarse delay line, the whole coarse delay line will always be operated. The long coarse delay line will have large power consumption. So the NAND gate can turn off the unnecessary coarse delay line to reduce the power consumption.

4.3.2 Shifter

In conventional DLL architecture, the up/down counter often applies adder to realize the function. But the delay lines are often controlled by thermal meter code. The decoder is required to decode the signal of up/down counter. To spare the complexity of the control circuit, the modified DLL architecture applies the shifter, shown in Fig. 4.5, to replace the up/down counter and decoder. Every bit of the shifter has the functions of shift left, shift right, and not shift. The command of shift left means increasing delay time, and the input is connected to the lower bit. Contrarily, shift right means decreasing delay time, and the input is connected to the higher bit. So the input of the LSB shift left is connected to Vdd. The input of the MSB shift right is connected to GND. This shifter can created the thermal meter code directly, and the code can be applied to control the delay line by using simple logic gates

transforming the code. This method can reduce the chip area efficiently.

4.3.3 Coarse Delay Comparator

The coarse delay comparator compares the value of divided internal clock, divided internal clock with 150ps delay, and divided internal clock with 900ps delay at the rising edge of the divided external clock. These delay times are decided by the one coarse delay stage delay time and the minor coarse delay stage delay time. All cases of the coarse delay comparator state are shown in Fig. 4.6. There are three bits signal that should be judged at the rising edge of the divided external clock. This can be realized by a D Flip-Flop that the control clock is connected to divided external clock. These cases can mainly be codified four parts, so the decoder is applied to decode these cases into two bits signal, reference the Table 4.1. The relationship between the function and the decoded signal is shown in this table clearly. It is simpler that codifying these cases into two bits signal. This can reduce the complexity of realizing the finite state machine (FSM) of the coarse delay control circuit. The operation theory of this FSM will be discussed in section 4.3.5 more detail.

4.3.4 Fine Delay Comparator and Fine Delay Operation Theory

The fine delay architecture is referenced [8]. This architecture adjusts the internal clock every two clock cycles. The block diagram is shown in Fig 4.7. The architecture equips two suites of the same adjusting equipment. Because each of the adjusting equipment adjusts one clock cycle of internal clock every two clock cycle. The comparator, shown in Fig 4.8, compares the crossing point of external clock and feedback clock. When feedback clock, ret. CLK-F, is at low logic level, the nodes, N1

and N2, are pulled up to the supply voltage that makes the signals, Up-F and Down-F, are at low logic level. When feedback clock, ret. CLK-F, is at high logic level, the comparator applies the inverter chain to make a short window that both ret. CLK-F and ret. CLK-Db are at high logic level. In this period of short window, the comparator compares the crossing point of the external clock, ext. CLK and ext. CLKb. If the crossing point of external clock is faster than the feedback clock, the nodes N1 is higher than N2. The cross-coupled architecture, T4 and T5, will amplify the voltage difference between N1 and N2. The Up-F will be at the high logic level to create the delay time of the fine delay, and Down-F will be at the low logic level.

Also this architecture applies the dummy unit coarse delay (UCD) and replica unit coarse delay (UCD) to keep the continuation between fine delay time and coarse delay time. The signals, φmf and φmd, control the delay line of fine delay, in Fig. 4.9, whether it should be turned on or not. Fig. 4.9 shows the timing diagram of this fine delay operation. In cycle-1 and cycle-2 one of these two suites adjusting equipments is operated respectively. During cycle-1, the signal, φmf, turns on the fingers which are determined by the decoder to discharge the voltage of the node φmix. After unit coarse delay time, the signal, φmd, will turn on all fingers of the fine delay circuit until t_m the beginning of the hold time, t_{hold}. Due to the different speed of discharging the node φmix, the node φmix has different hold voltage. At t_{in}, all fingers are turned on to discharge the node φmix. Due to the different hold voltage, the node φout1 has different delay time during cycle-2. In this moment, another suite of fine delay control circuit is operated to discharge another suite of fine delay circuit. The output of the fine delay line connected to the input of the coarse delay line is applied the OR gate combining φout1 and φout2 which is the output of these two suites of fine delay circuit.

4.3.5 Finite State Machine

The finite state machine (FSM) controls the operation of coarse delay. It is mainly divided into two parts which control different delay time of the coarse delay. The input of these finite state machines is made by decoding three signals, divided feedback clock, divided feedback clock with 150 ps delay, and divided feedback clock with 900 ps delay. This is explained in section 4.3.3, and the decoded signals are shown in Table 4.1. The finite state machine called FSM1 that controls 900 ps delay is shown in Fig. 4.10. When starting the DLL architecture the architecture adjusts internal clock by the order of 900 ps. After resetting or starting the circuit, FSM1 is at the state S0. In this state the delay time is the shortest, so if it receives “00”, the delay line should delay 900 ps not forward 900 ps. The output signals of FSM1 control the shifter. When the left bit is “1”, the shifter doesn’t shift whether the right bit is “1” or not. When the left bit is “0”, the shifter will shift left which means increasing delay time when the right bit is “1” and shift right oppositely.

Before FSM1 is at the state S2 that means the difference between internal clock and external clock is less than 900 ps, the finite state machine called FSM2 that controls 150 ps delay is at the state S0 in Fig. 4.11. Before FSM1 finishes its operation, the right bit of output signals is “1” to reset the data of FSM2 preventing the controlling error. The left and middle bit of output signals are the same as the output signals of FSM1. When FSM2 is at state S2, the locking signal becomes “1” to hold the data of these shifters and transfers the signal to the fine delay control circuits to start these fine delay control circuits. In this moment, the difference between external clock and internal clock is less than 150 ps.

4.4 DLL SIMULATION RESULT

Fig. 4.12 and Fig. 4.13 show the timing diagrams of DLL operating at 250 MHz and 66 MHz respectively. This DLL architecture equips signals to detect the delay adjustment. Also the DLL has a lock signal to announce the internal clock locked. Figs. 4.14, 4.15, and 4.16 show the jitter histogram of DLL operated at 250 MHz with different corner and temperature, and the jitter are 33 ps, 42 ps, and 50 ps respectively. Figs. 4.17, 4.18, and 4.19 show the jitter histogram of DLL operated at 66 MHz with different corner and temperature, and the jitter are 68 ps, 70 ps, and 80 ps respectively. These figures show the jitter simulation influenced by different situation. The jitter of DLL operated at 66MHz is larger than at 250 MHz. This is because that the capacitances applied in this architecture are MOS capacitances. MOS capacitance is sensitive to operation voltage. The clock of DLL operated at 66 MHz passes through longer delay line so that it applies more MOS capacitances for delaying longer. Fig. 4.20 is the jitter histogram of DLL operated at 66 MHz with ideal capacitances, and the value of jitter is 50 ps.

4.5 CONCLUSION

Table 4.2 is the electric characteristics of this DLL architecture operated at different frequency. This DLL architecture has advantages of low current consumption and fast locking the internal clock. It can be operated at the frequency of 66 MHz to 250 MHz. But the coarse delay line of this architecture can be improved for decrease the jitter. If this architecture can overcome this disadvantage, it can be realized better performance in DDR SDRAM applications.

Table 4.1

Function and Decode of Coarse Delay State

State	Function	Decode
111	Delay 900ps	11
001	Delay 900ps	11
011	Delay 900ps	11
110	Delay 150ps	10
100	Coarse Delay Locked	01
000	Delay -900ps	00

Table 4.2

Electrical Characteristics of DLL

Parameter	Specification	Operation at 66 MHz	Operation at 250 MHz
Reference Input Clock Range	66 MHz ~ 250 MHz	66 MHz	250 MHz
Locking Time	150 Input Clock Cycles	87 cycles	28 cycles
Current Consumption	10 mA	4.62 mA	5.37 mA
Duty Cycle	45% ~ 55%	53.3%	51%

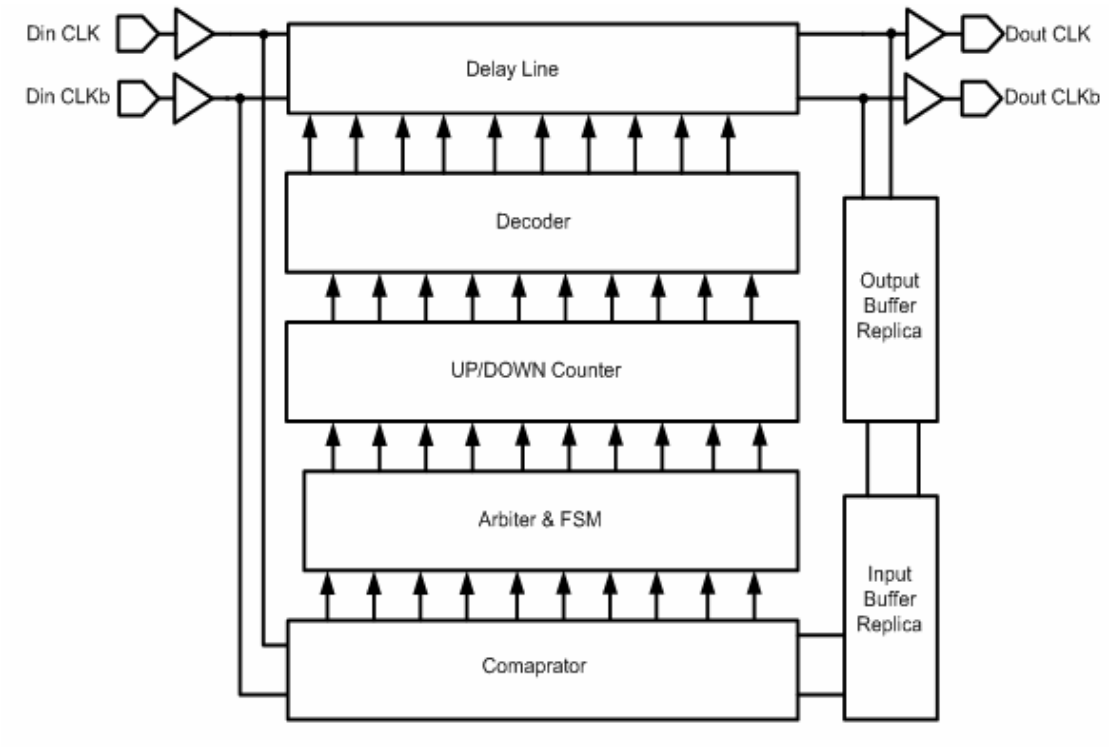

Fig. 4.1 Block Diagram of DLL Architecture

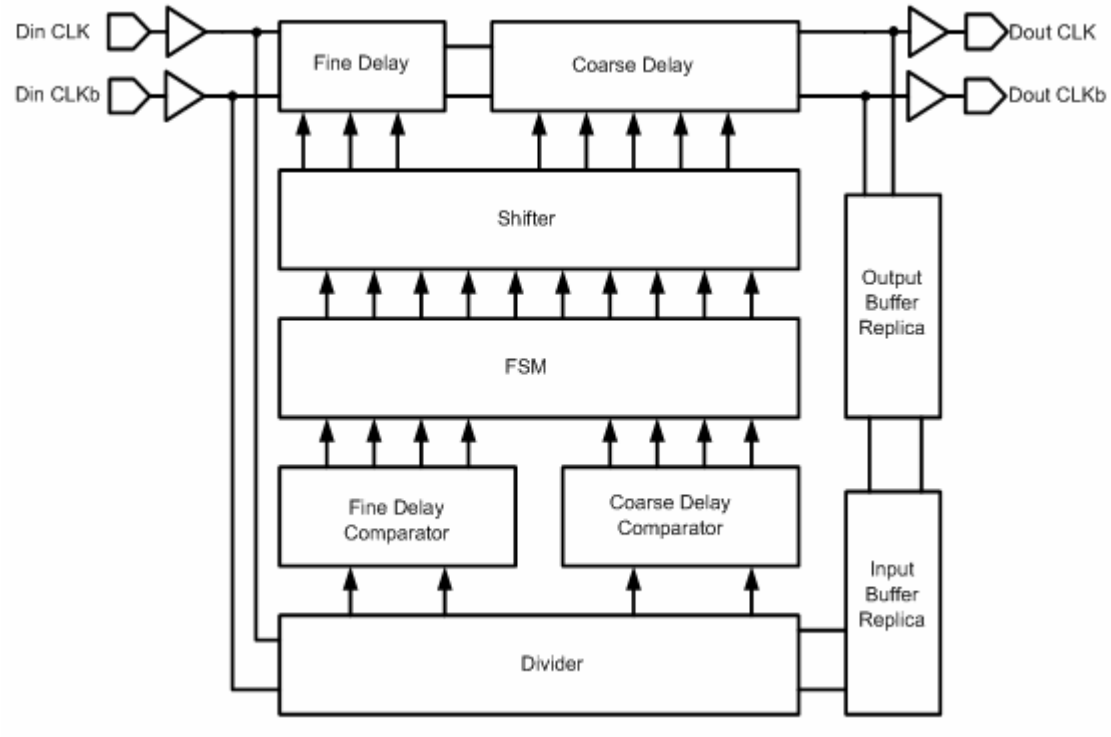

Fig. 4.2 Block Diagram of Modified DLL Architecture

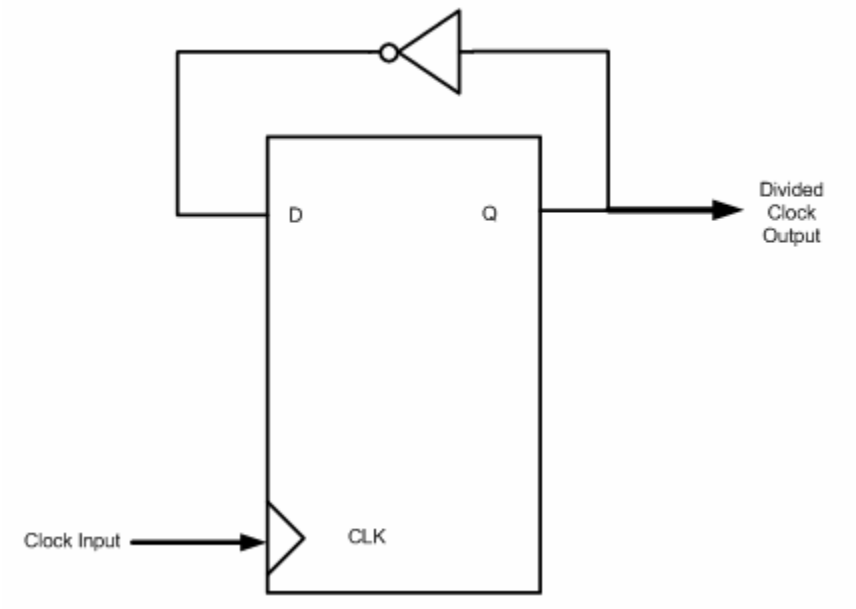

Fig. 4.3 Schematic of Divider

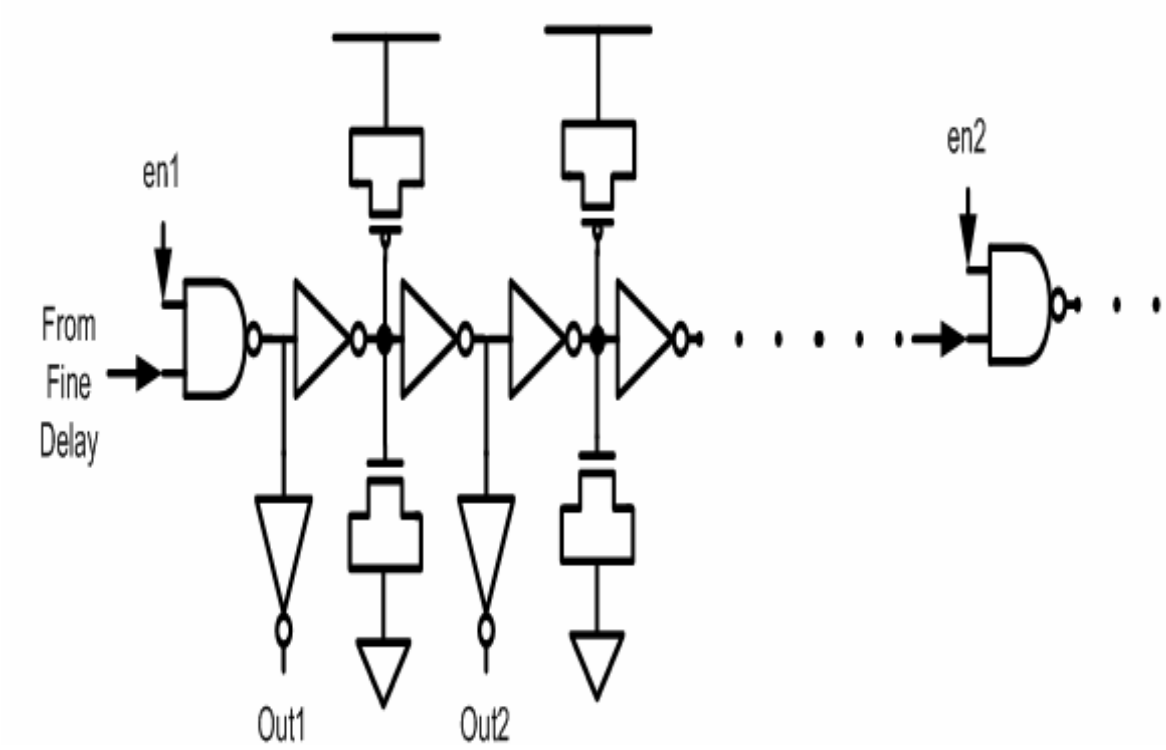

Fig. 4.4 Basic Stage of Coarse Delay

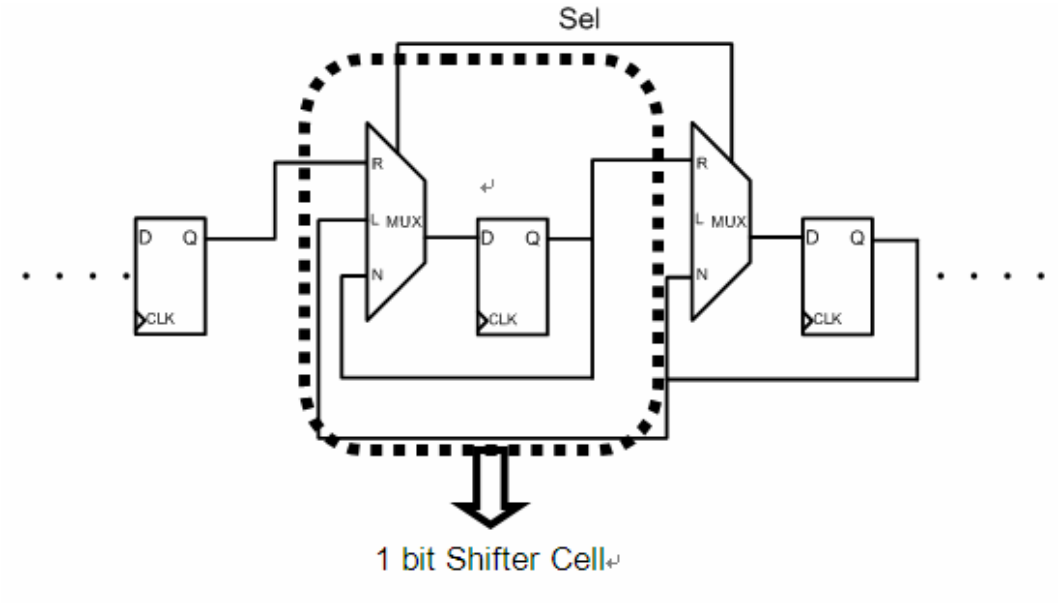

Fig. 4.5 Schematic of Shifter

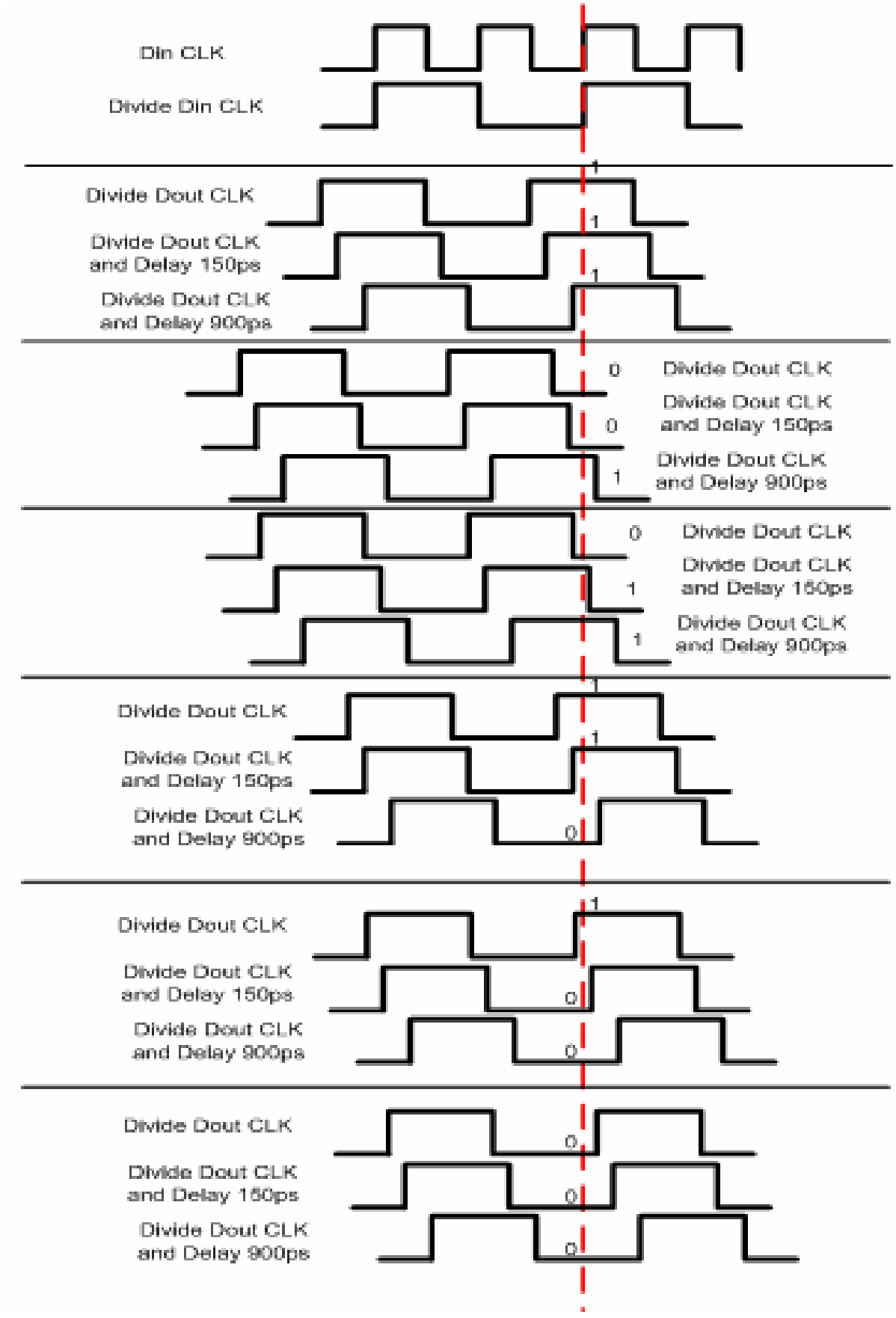

Fig. 4.6 Waveform of Coarse Delay Cases

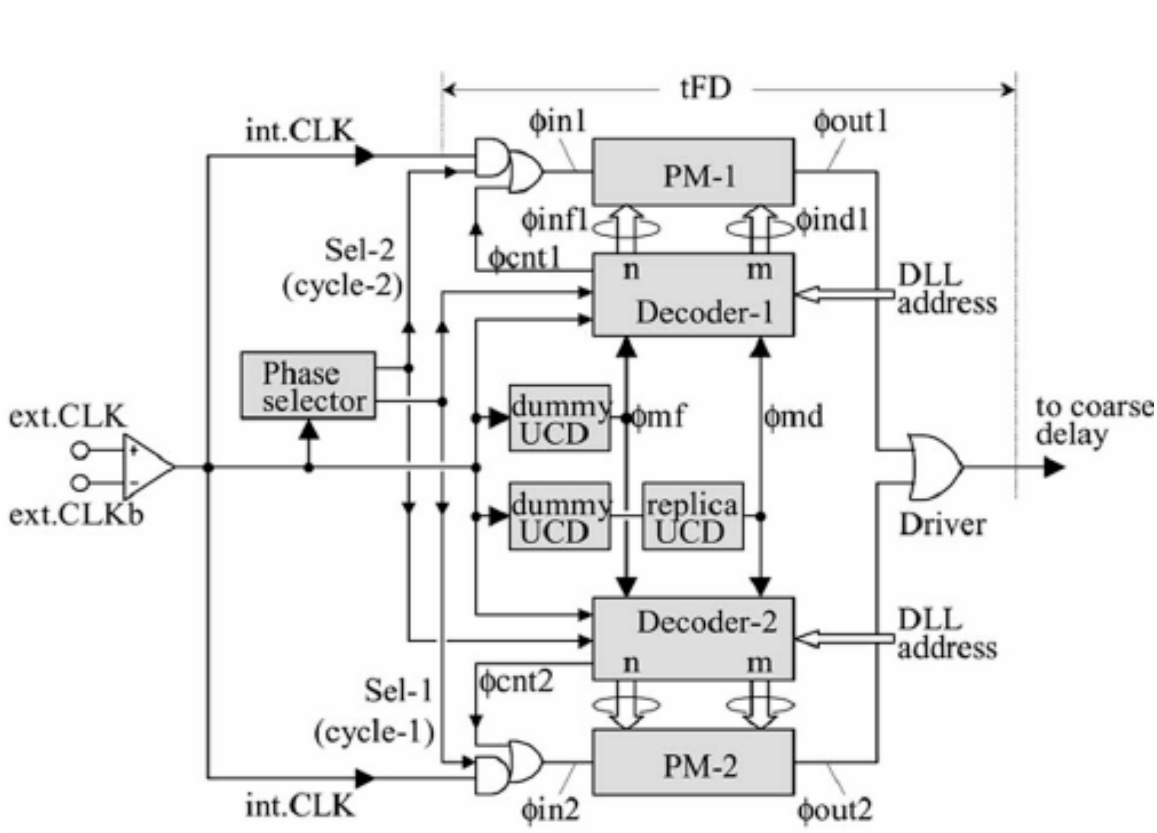

Fig. 4.7 Block Diagram of Fine Delay Control Circuit

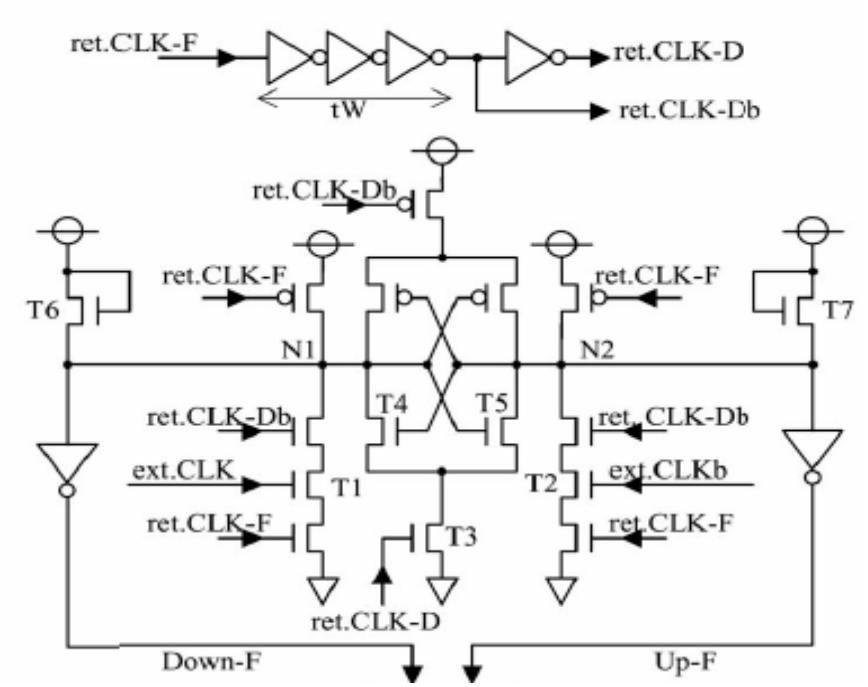

Fig. 4.8 Schematic of Fine Delay Comparator

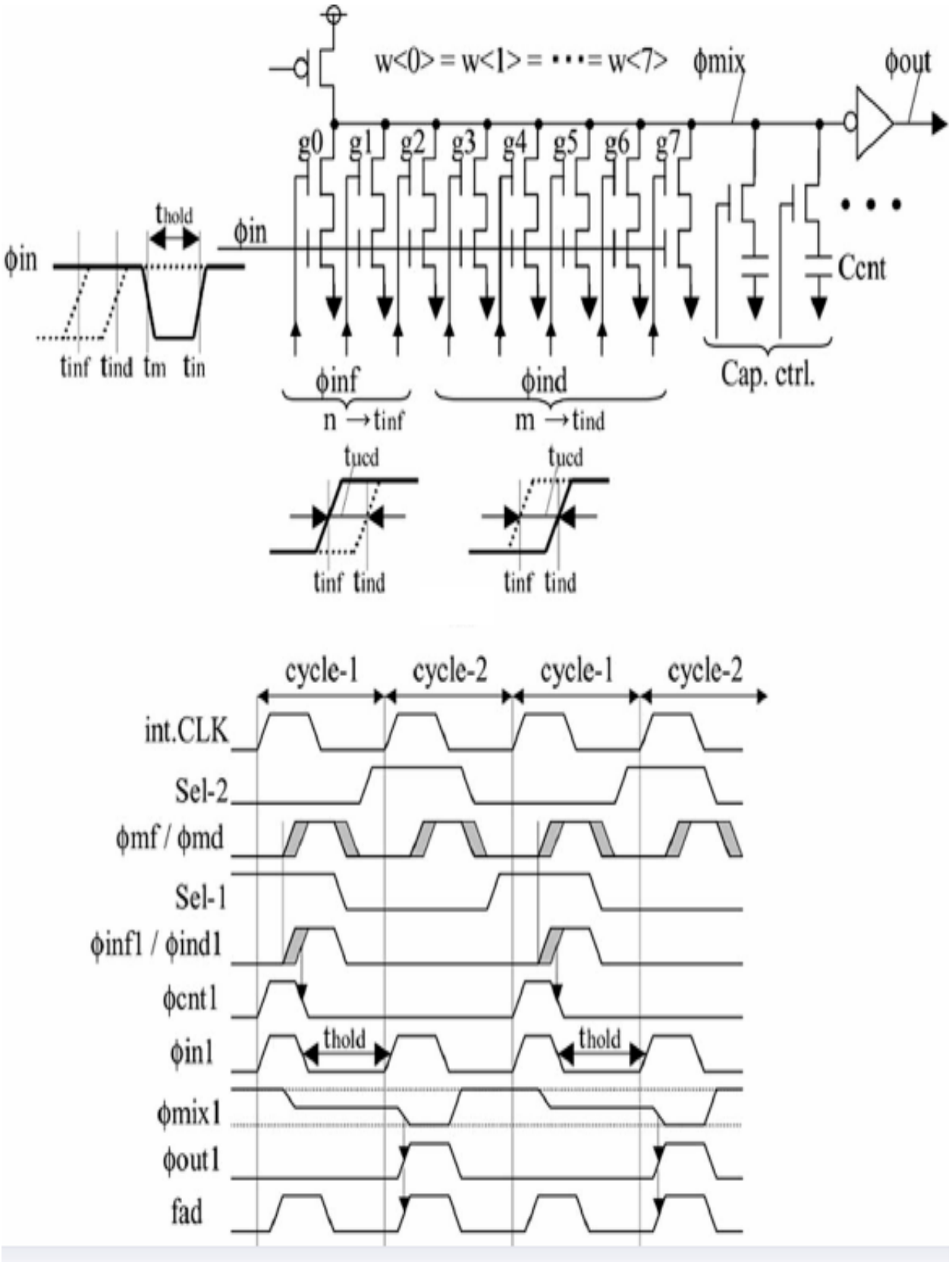

Fig. 4.9 Schematic and Timing Diagram of Fine Delay

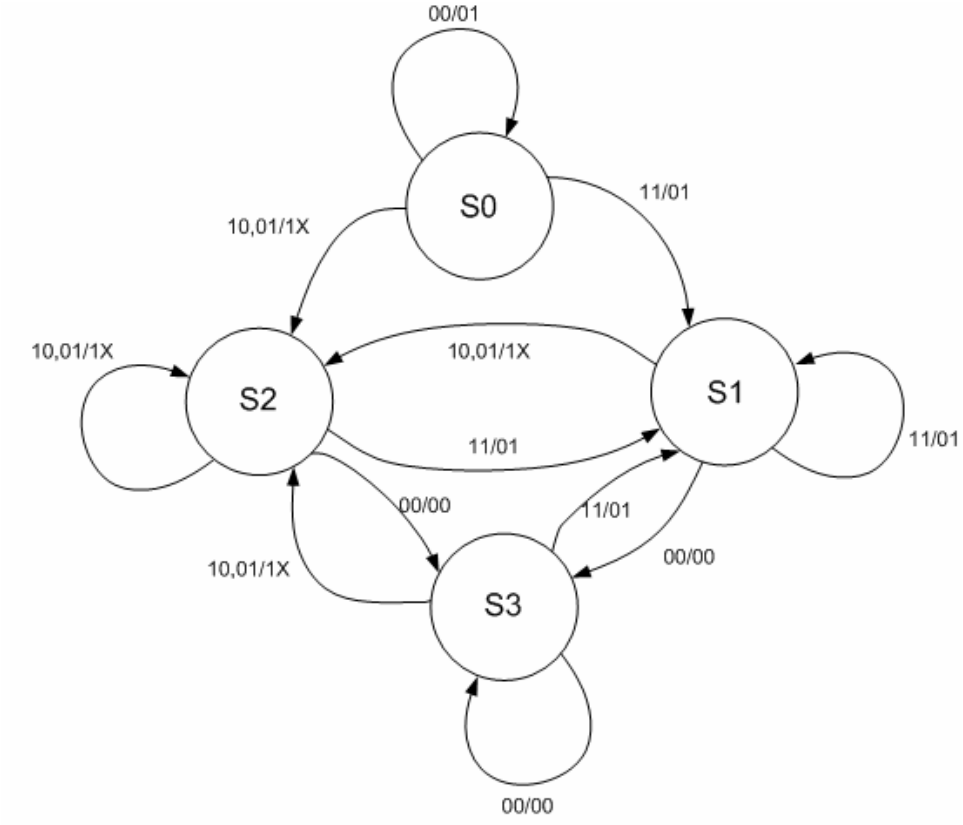

Fig. 4.10 Finite State Machine of 900 ps Adjustment

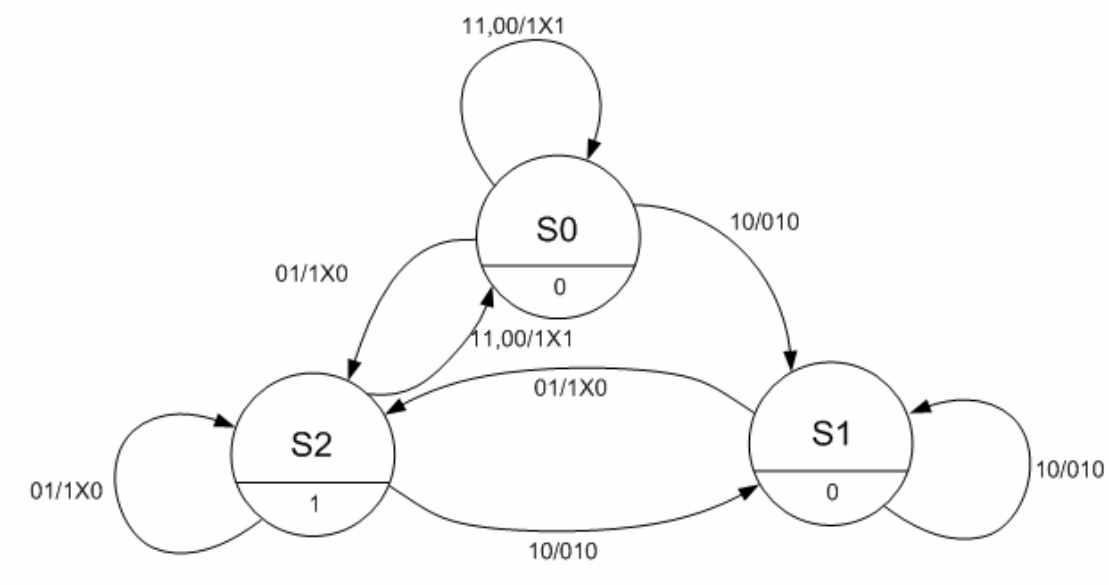

Fig. 4.11 Finite State Machine of 150 ps Adjustment

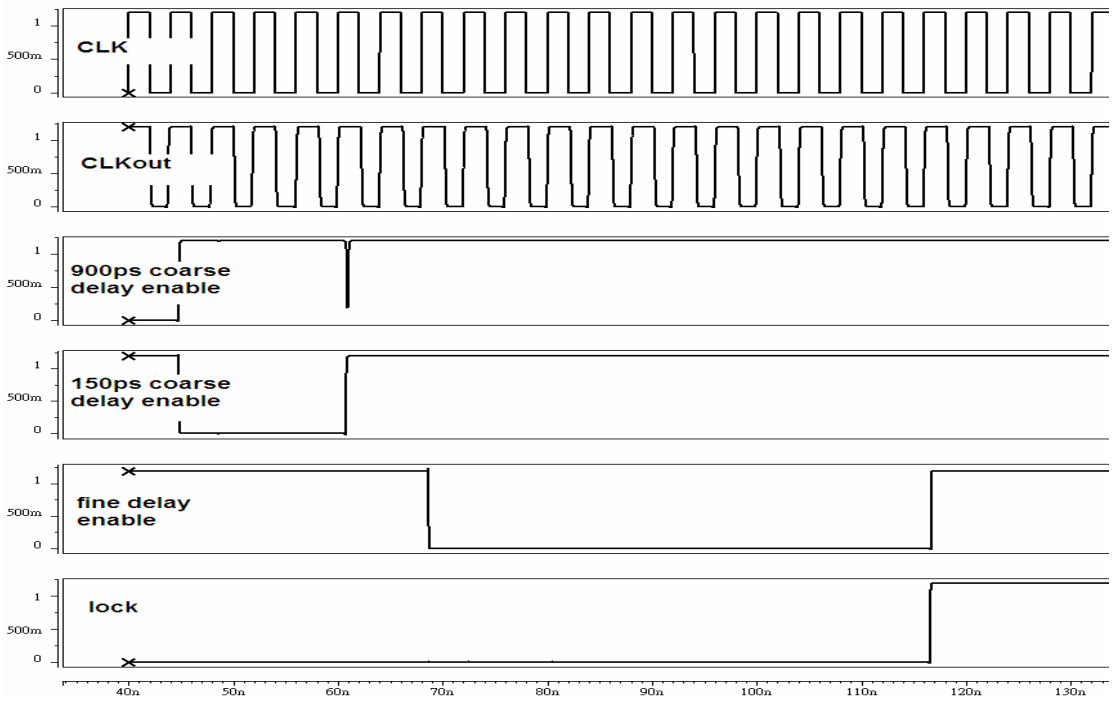

Fig. 4.12 Timing Diagram of DLL at 250 MHz

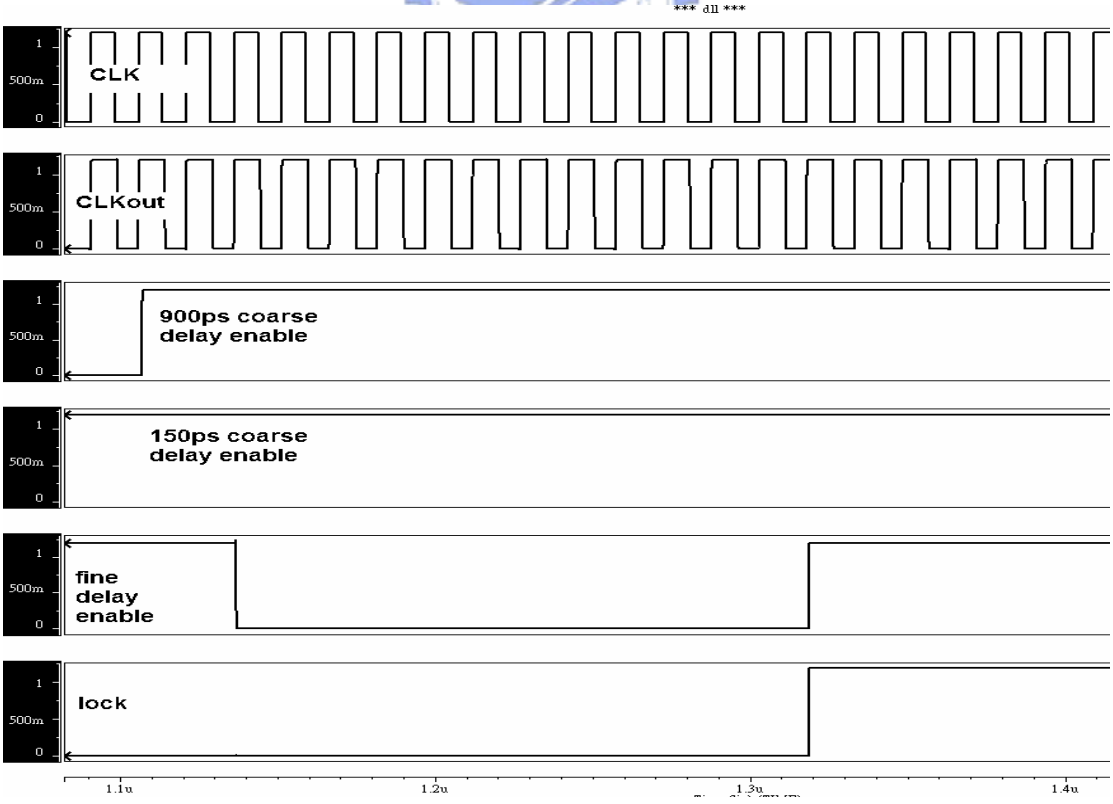

Fig. 4.13 Timing Diagram of DLL at 66 MHz

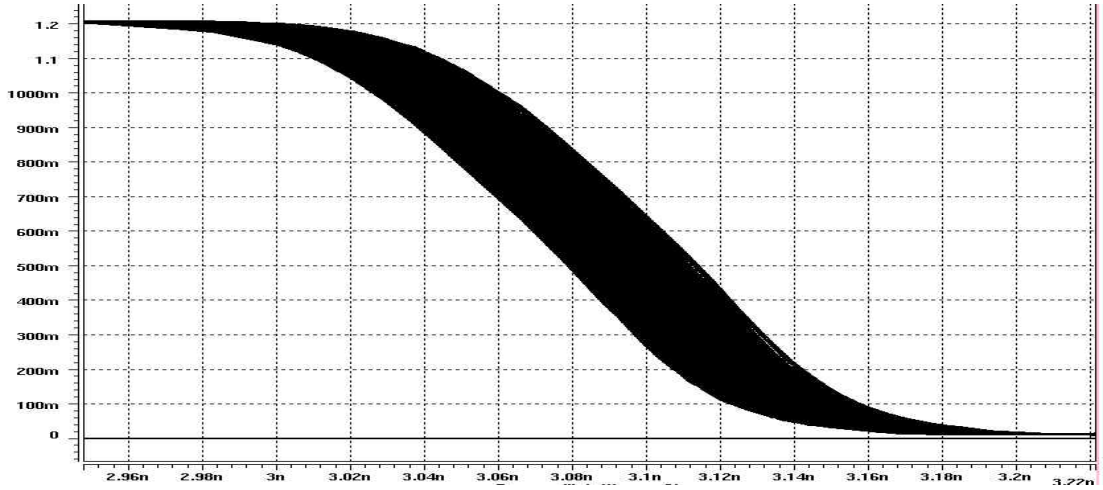

Fig. 4.14 Jitter Simulation of DLL at 250 MHz in TT Corner 25℃

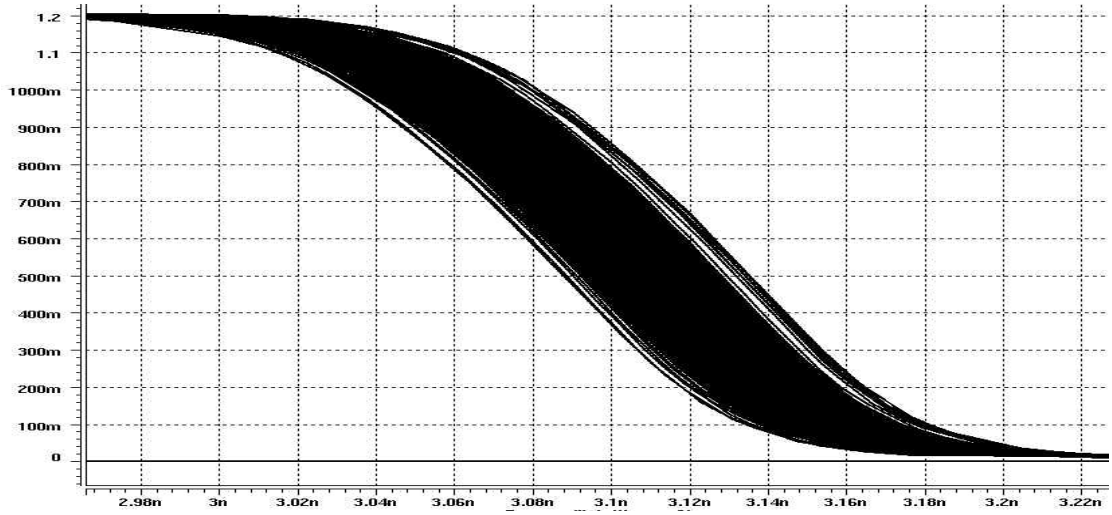

Fig. 4.15 Jitter Simulation of DLL at 250 MHz in FF Corner 85℃

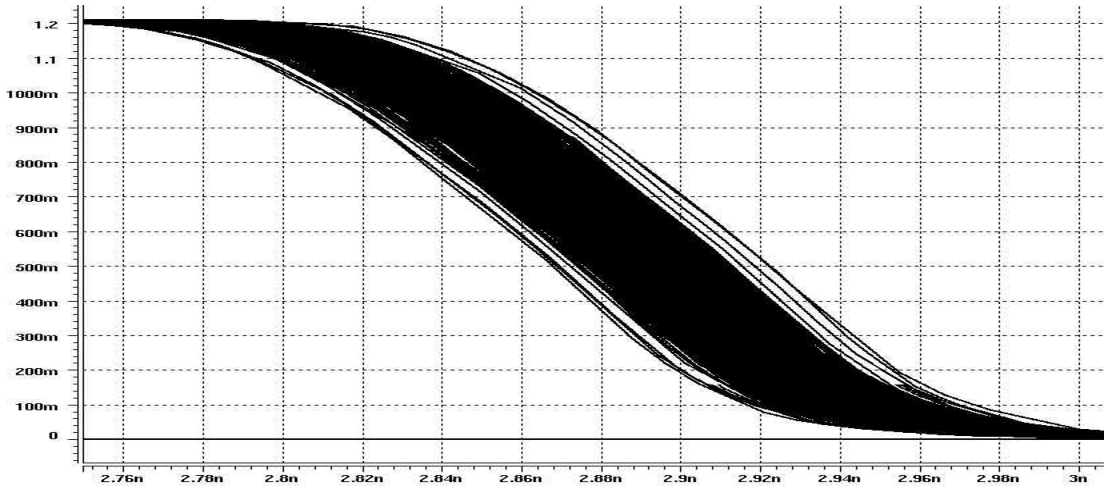

Fig. 4.16 Jitter Simulation of DLL at 250 MHz in SS Corner 0℃

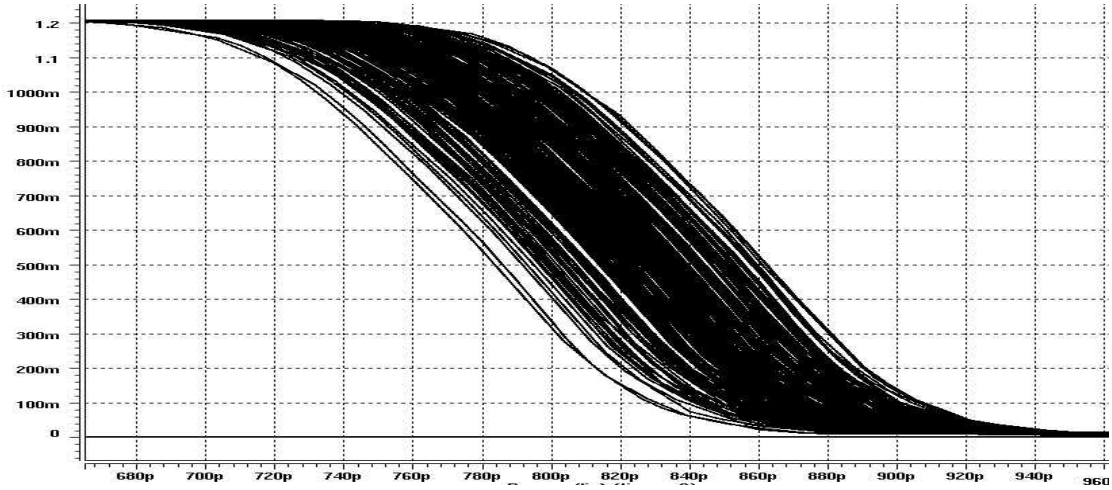

Fig. 4.17 Jitter Simulation of DLL at 66 MHz in TT Corner 25℃

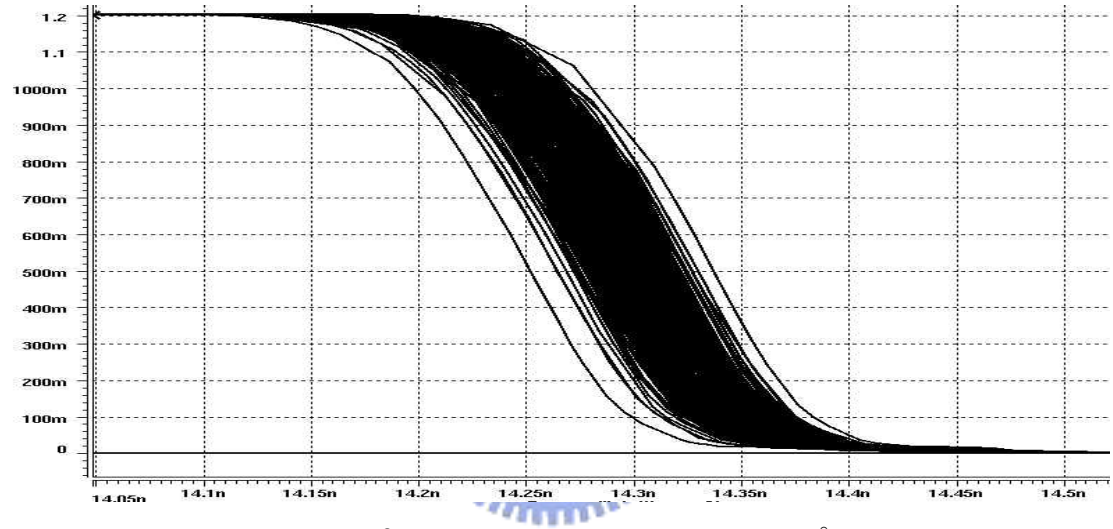

Fig. 4.18 Jitter Simulation of DLL at 66 MHz in FF Corner 85℃

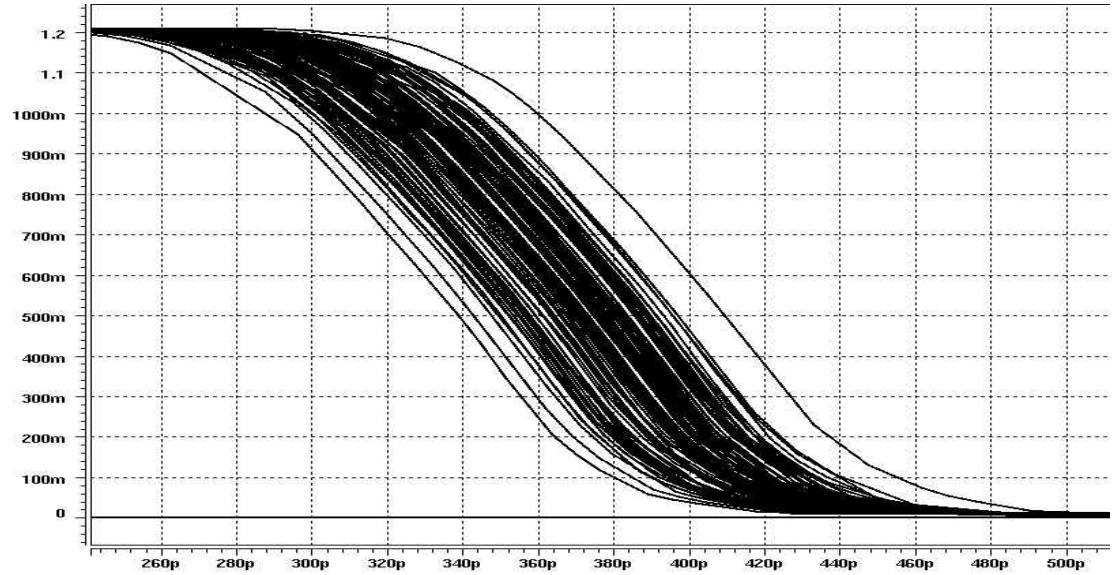

Fig. 4.19 Jitter Simulation of DLL at 66 MHz in SS Corner 0℃

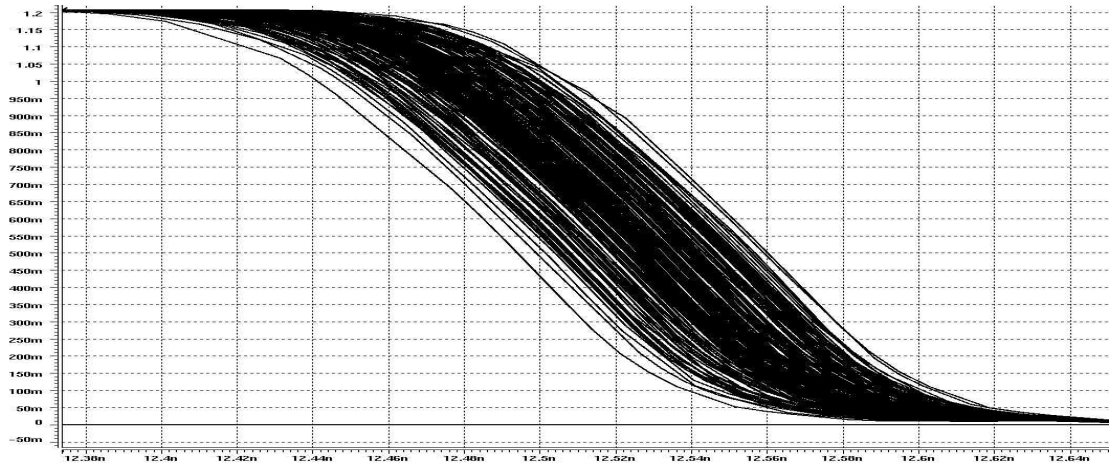

Fig. 4.20　Jitter Simulation of DLL at 66 MHz in TT Corner 25℃　Font Type

Chapter 5

Summary and Future Works

5.1 SUMMARY

Chapter 2 introduces the specifications of SSTL_2 I/O circuit and DLL. This chapter clearly discusses AC and DC specifications of the SSTL_2 standard. It also simply introduces the background for the SSTL_2 and DLL architecture in DDR SDRAM applications.

Chapter 3 presents the SSTL_2 architecture in different methods. SSTL_2 I/O circuits are fabricated in 0.13 μm 1P8M CMOS process and the power supplies are 2.5 V and 1.2 V. The maximum operation frequency of SSTL_2 without slew rate control circuit is 500 Mbps (250 MHz clock rate) for operating 3 bits applied on the same power line. SSTL_2 with slew rate control circuit improves the disadvantage of the first version. It can be operated at the speed of 600 Mbps for 8 bits on the same power line. Although the maximum operation frequency of SSTL_2 is 400 Mbps, the higher operation speed SSTL_2 architecture can achieve the more margin it can sustain.

Chapter 4 discusses the DLL architecture design. This DLL architecture can be operated at the range of 66 MHz to 250 MHz. This DLL architecture applies hierarchical delay line architecture to adjust the internal clock. The hierarchical delay line architecture must notice the continuance between fine delay time and coarse delay time. The maximum jitter is 80 ps which arise in the case of operating the DLL architecture at the operation frequency of 250 MHz in 0℃.

5.2 FUTURE WORKS

Although SSTL_2 is verified to be operated normally in the DDR SDRAM applications, it can be improved to get better performance. It can be applied more I/O circuits operating on the same power line to reduce power lines routing in the chip. The DLL architecture can improve the disadvantage of coarse delay line to reduce the jitter. To improve these disadvantages can increase the reliability for these architecture applications.

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