國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

低電壓差動訊號傳輸標準之
平面顯示器高速資料接收器設計

Design on 1.225 Gb/s LVDS Receiver for UXGA Flat Panel Display Applications

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指導教授　：　柯明道　教授

中華民國九十四年九月

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碩士論文

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摘要

隨著平面顯示器尺寸不斷地增加，顯示器所提供的色彩濃度與解析度也不斷地提升。解析度 SVGA (800×600 像素) 和 XGA (1024×768 像素) 已是平面顯示器最基本的要求。解析度不斷地提升，同時也意味著資料傳輸量與資料傳送速度的提升。尤其以位於平面顯示系統裡，直接連接顯示卡到液晶顯示時脈控制器之間的資料傳送遇到的瓶頸最為明顯。在高速的資料傳送速度下，如何正確地傳送資料成為一個值得研究的課題。本論文將提出一個應用於平面顯示系統低電壓差動訊號接收器的新架構，提升資料接受器對訊號偏移量的忍受度，同時降低整個電路的複雜度，達到提高資料接收效率並節省成本的效果。本文提出的新架構主要分成兩個部份，第一部份中提出三倍四分之一步距取樣 (Three quarter steps oversampling) 架構來提升接收器對輸入訊號眼圖 (eye diagram) 的忍受度。第二部份提出延遲選擇 (Delay selecting) 架構來降低整個接收器佈局的複雜度。

傳統接收器架構中，大多使用三倍取樣 (Three times oversampling) 架構來恢復輸入訊號。當輸入資料偏移量接近二分之一步距時，三倍取樣架構將無法分辨出偏移量是領先還是落後取樣時脈，因此可能造成恢復資料的出錯。本文提出的三倍四分之一步距取樣中，因為存在一個取樣點落在取樣步距二分之一處，所以在資料偏移量小

於二分之一步距下，三倍四分之一步距取樣架構皆能判斷出資料偏移的方向，達到提升對眼圖的容忍度。第二部份的延遲選擇架構取代傳統電路中的相位選擇（phase selecting）架構。傳統的相位選擇架構搭配三倍取樣架構，在平面顯示系統低電壓差動訊號接收器的應用中，需要使用 21 個不同相位的取樣時脈，如此一來將增加電路佈局的複雜度，連帶造成佈局面積的膨脹。新架構中因為使用延遲選擇架構取代相位選擇架構，整個電路中只需要使用到 7 個不同相位的取樣時脈，大幅減低佈局的複雜度，同時縮小整個佈局面積達到降低成本的目的。

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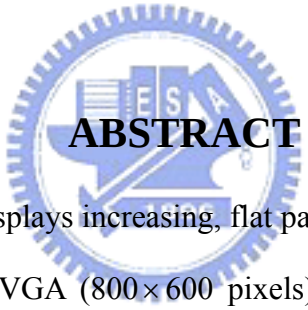

ABSTRACT

As the size of flat panel displays increasing, flat panel displays offer higher color depth and resolution. Offering the SVGA (800×600 pixels) and the XGA (1024×768 pixels) resolutions becomes a basic requirement of flat panel displays. The increase of display resolution also means the increase of data rate. Especially at the interfaces that directly connect a graphics card to a liquid crystal display's (LCD's) timing controller in FPD systems, the high-speed data rate becomes a serious bottle net. When the resolution is up to SXGA (1280×1024 pixels) and UXGA (1600×1200 pixels), the data rate is up to 784 Mbps and 1155 Mbps. How to recover data correctly in the high-speed data rate becomes a significant topic. This thesis is going to present a new architecture of receiver with the LVDS standard for FPD application, which increases the tolerance of the skew between signals and reduces the complexity of the layout. The new architecture not only increases the performance but also reduces the cost. There are tow parts of the new architecture

presented in this thesis. First part presents the “three quarter steps oversampling” system, which increases the tolerance of the eye diagram of input data. Second part presents the “delay selecting,” which reduces the complexity of the layout.

In traditional architecture, most receivers use the “three times oversampling” system to recover input data. However, when the skew between input data and the input clock is close to half step time, the “three times oversampling” system can not detect whether the skew leads or lags, and may induce errors in recovered data. Because there exists a sampling clock phase at the center of data step in the “three quarter steps oversampling” presented in this thesis, the “three quarter steps oversampling” system can detect whether the skew leads or lags when the skew between input data and the input clock is close to half step time. Thus, by using the new system the receiver can increase the tolerance of the eye diagram of input data. The “delay selecting” presented in the second part is used in the receiver instead of the “phase selecting,” which is usually used in traditional architecture. Using the traditional “delay selecting” and “three times oversampling” system in the receiver for FPD applications, it needs 21 differential sampling clock phases to sample input data, and that will increase the complexity of layout and induce the expansion of the layout area. Because the new architecture uses the “delay selecting” instead of the “phase selecting”, it only needs 7 differential sampling clock phases during recovering input data, and that actually reduces the complexity and the area of the layout and reduces the coast of the receiver.

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吳建樺

九十四年九月

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TABLE CAPTIONS

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Chapter 1
Introduction

1.1 MOTIVATION

As process technologies continue to scale down, the on-chip data rate moves faster than the off-chip data rate. The interface between chips will become a significant bottleneck in high-speed data communication. Thus, how to speed up transmitting data rate over several inches, or even meters between computers or information electrical machines is more and more important.

A typical link (Fig. 1.1) between chips is comprised of three primary components, a transmitter, a channel, and a receiver. In the channel, when the distance between chips is longer, the parasitic effects will become more serious. Under these serious parasitic effects, the frequency of a full swing signal will be limited. Besides, when the data rate of system is up to gigabits-per-second, using a full swing signal to transmit data will induce large power consumption. Therefore, in a high speed and long distance communication how to transmit data is important.

LVDS, low-voltage differential signaling, is one of I/O interfaces usually used in application cases, especially in the data transmission from graphics controller to LCD panels. Due to the specificity of low-voltage swinging, using LVDS I/O interface can not only speed up the data rate, but also reduce the power consumption of I/O interface circuits.

To transmit the internal data into the signal form satisfying the interface specification like LVDS, transmitters in the data communication are needed. Besides, to reduce the number of channels off-chips, each transmitter usually serializes several data from different internal channels into one of these channels off-chips. In some application cases,

transmitters will translate 21 or 28 bits wide TTL data into LVDS data 3 or 4 bits wide and 7 bits deep.

However, how do receivers recover the 3 or 4 bits wide and 7 bits deep LVDS data into 21 or 28 bits wide full swing data correctly, especially when the data rate is up to gigabits-per-second? The parasitic effects in these off-chips channels will induce serious skews and jitters under the high-speed data rate. These receivers need a detecting system to detect these skews and jitters induced by parasitic effects and recover data correctly. In this thesis, a new architecture of the data receiver used in the link with LVDS standard for flap panel display applications is going to be presented.

Table 1.1 lists the resolutions to cope with in this thesis. In this thesis the high resolutions is our main concerns. The receiver presented in this thesis is designed to satisfy the UXGA (1600 × 1200 pixels) resolution, which requires a data rate up to 1155 Mbps and a PLL offering 165MHz clocks.

1.2 THE FPD LINK

Fig. 1.2 shows a typical FPD Link (Flat panel Display Link) application. The FPD Link chipset is a family of interface devices specifically configured to support data transmission from graphics controller to LCD panels. The employed technology, LVDS (Low Voltage Differential Signaling), is ideal for high speed and low power data transfer. This enables the implementation of high-end displays.

The FPD Link chipset is composed of a transmitter chip and a receiver chip. The transmitter chip is used to convert the internal data, the output data of graphic card, into LVDS data. After LVDS data are transmitted through the transmission line, the receiver reconverts the LVDS data into internal digital data as the input data of the timing controller.

In the FPD Link application, decreasing the number of channels could reduce the cost.

To decrease the number of channels, in application cases, each transmitter would serialize seven different data source into one channel. Therefore, input signal of the receiver is a seven deep LVDS signal. On the other hand, the data rate in each channel is seven times the clock frequency, as shown in Fig. 1.3.

Because of parasitic effects in channels, skews between signals passing channels may occur. Fig. 1.4 shows the timing between input data and the input clock when the skews happen. The receiver must detect the skew between data and the input clock and recover data correctly. In a traditional receiver, three times oversampling is a popular system used to help the receiver detect the skew between data and the input clock. However, in application cases which uses a seven deep serial data as input data, the three times oversampling system needs 21 different sampling clock phases, and that would induce the expansion of the layout area of the PLL (phase lock loop), which provides the receiver 21 different sampling clock phases. To solve this problem, this thesis will present a new detect system using “three quarter steps oversampling” and “delay selecting” instead of “three times oversampling” and “phase selecting” used in the traditional system.

1.3 THESIS ORGANIZATION

The chapter 2 of the thesis would discuss the low-voltage differential signaling (LVDS) standard. The detail DC specifications, signal level and applications of LVDS standard are presented. In the chapter 3, the architecture and implementation of a CDR are discussed. A modified architecture of CDR would be presented and compared with the traditional architecture. The chapter 4 would discuss each building block of the modified architecture presented in chapter 3. How each block is implemented would be presented in this chapter. In chapter 5, the measurement results of the LVDS receiver fabricated in 0.13-μm CMOS process would be present. In chapter 6 are conclusion and future works.

Table 1.1 The video resolutions and the corresponding specificity

Resolutions	SVGA	XGA	SXGA	UXGA
Pixels	800×600	1024×768	1280×1024	1600×1200
PLL Frequency	40 MHz	65 MHz	112 MHz	165 MHz
Data Rate	280 Mbps	455 Mbps	784 Mbps	1155 Mbps

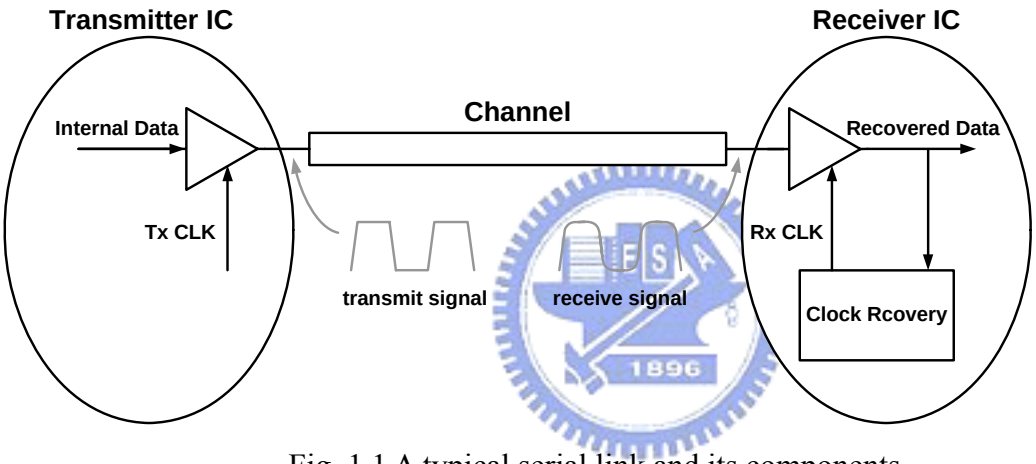


Fig. 1.1 A typical serial link and its components

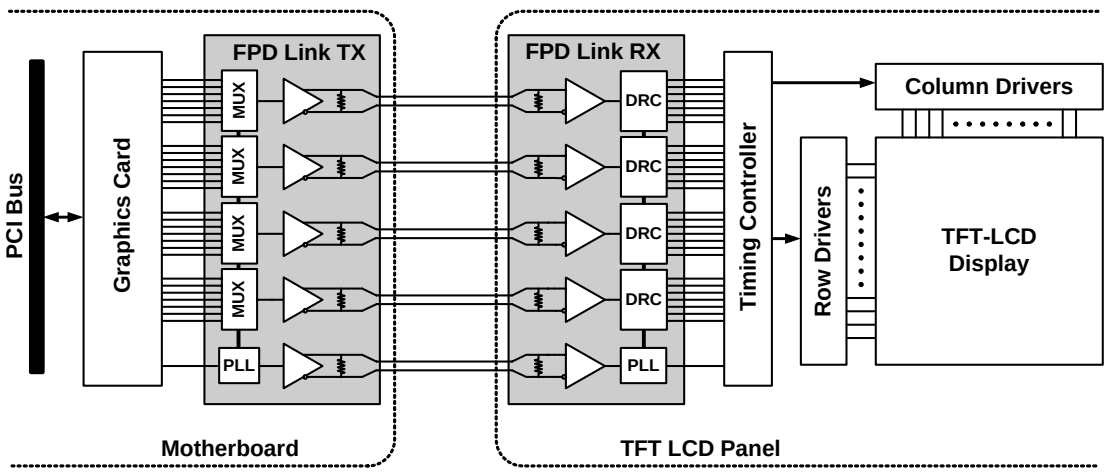


Fig. 1.2 A typical FPD Link application

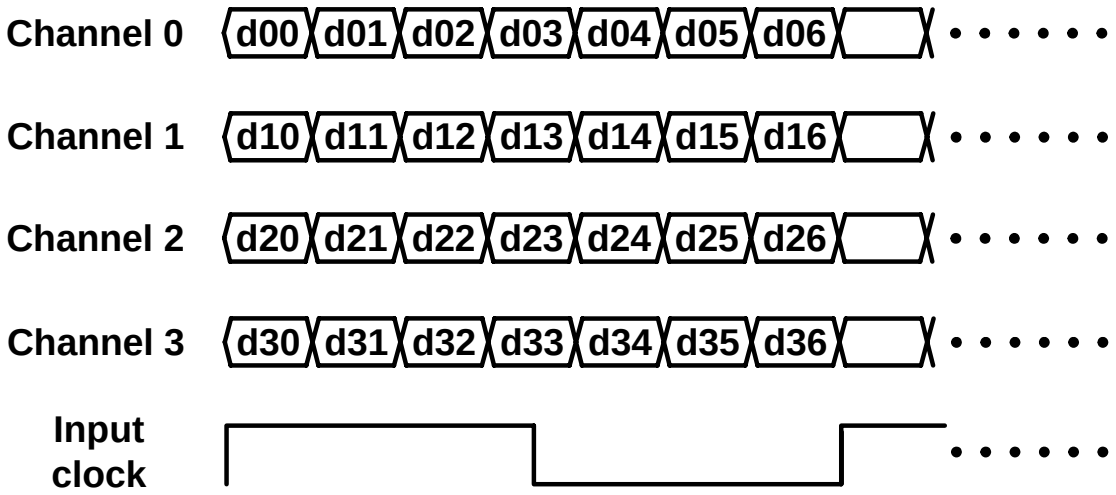


Fig. 1.3 The timing relation between input data and input clock in channels

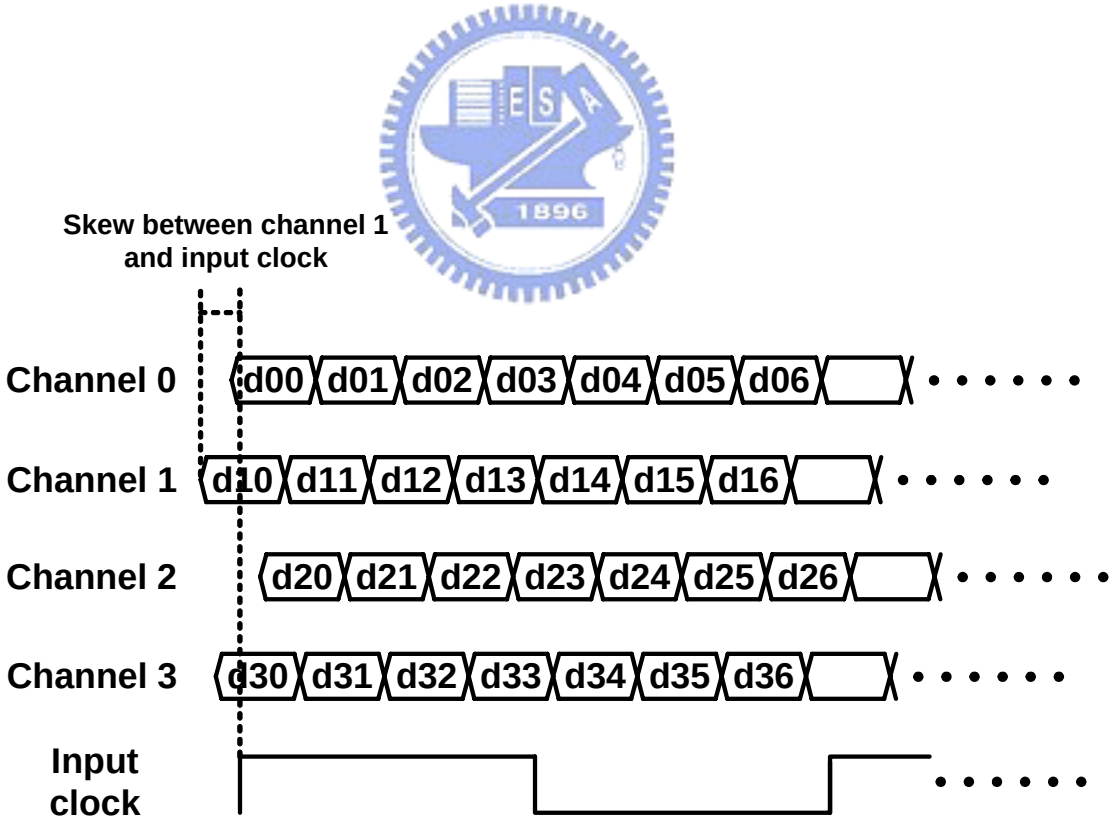


Fig. 1.4 The timing relation between data and clock when skews happen

Chapter 2

Specifications of Low-Voltage Differential Signaling (LVDS)

2.1 STANDARDS OF LVDS

There are two industry standards that define LVDS [1]. One of the two standards is the generic electrical layer standard defined by the TIA (Telecommunications Industry Association) [2]. This standard is known as ANSI/TIA/EIA-644. The other application specific standard is the standard defined by the IEEE (Institute for Electrical and Electronics Engineering), which is titled SCI (Scalable Coherent Interface) [3]. In this thesis, the receiver is designed following the IEEE standard, SCI.

The original SCI is specified in IEEE standard 1596-1992. The original standard provides computer-bus-like services but uses a collection of fast point-to-point links instead of a physical bus in order to reach far higher speeds. This basic specification defines differential ECL (Emitter Coupled Logic) signals, which provide a high transfer rate (16 bits are transferred every 2 ns). However, because this specification only addressed the high data rates required and didn't address the low power concerns, this original specification is inconvenient for some applications. Thus, SCI-LVDS specified in IEEE 1596.3 was defined as a subset of SCI. SCI-LVDS specifies signaling levels (electrical specifications) for not only the high-speed but also the low-power physical layer interface. Besides, SCI-LVDS also defines the encoding for packet switching used in SCI data transfers.

2.2 INTRODUCTION OF LVDS

The primary goal of IEEE standard for LVDS is to create a physical layer specification for drivers and receivers and signal encoding suitable for use with the SCI as specified by IEEE standard 1596-1992 in low-cost workstation and personal computer applications. In this thesis, because our research focuses on the receiver, following introduction of LVDS will focus on the specification for receivers.

2.2.1 Configuration

Fig. 2.1 shows a typical LVDS interface, which is connected point-to-point. In the LVDS interface, the driver sends a low-voltage swing (400 mV single-ended maximum) differential signal to the receiver with a very high data rate (in IEEE standard for LVDS the data rate is reach 500 Mbits per second per signal pair), and low power dissipation. The power consumption is low because signal swings are small. The LVDS driver drives a minimum 2.5 mA current through a 100-ohm termination resister and switches the direction of current to change the value of data carried by the differential signal. Because the driver load is an uncomplicated point-to-point 100-ohm transmission line environment, the driver can switch the direction of the current through the termination resister in a high speed.

LVDS is independent of the physical layer transmission media. As long as the media deliver the signals to receiver with adequate noise margin and within the skew tolerance range, the interface will be reliable. This is a great advantage when using cables to carry LVDS signals. Sine all connections are point-to-point connected, physical links between nodes are independent of other node connections in the same system. This allows for freedom in developing a useful interconnection that fits the needs of application cases.

In IEEE LVDS standard, the physical environment of point-to-point connections between circuit boards is divided into two cases. First case is for the connections used

between two or more different circuit boards, which must operate with tolerance for V_{gpd} (approximately ± 1 V for 2.5 V powered system). Second case is for the connections used on a PCB or similar environment that will guarantee V_{gpd} is less than 50 mV. In each of these two different cases, the IEEE LVDS standard has different specification. IEEE LVDS standard calls the first as general purpose link and second case as reduced rang link. In this thesis, because the receiver is designed for a FPD Link, which is used between the motherboard and the TFT LCD panel, all the designs are follow the specification in the general purpose link case.

2.2.2 Driver Output Levels

The output signal of the driver is in a small-swing differential voltage when the driver is properly terminated. Fig. 2.2 shows the differential signal and the relation between the two single-ended outputs. The differential signal is composed of the two single-ended outputs. Because this two single-ended outputs switch alternately, the driver keeps the current constant. The load resistance determines the differential voltage level. In differential application cases the load resistance is different, but in most cases the load resistance is 100-ohm. Fig. 2.2 shows the case where a current source is providing a 4 mA current and the outputs are switching the current at a 50% duty cycle.

Fig. 2.2 also shows the receiver threshold limits in relation to the single-ended signals that arrive at the receiver inputs. When the magnitude of the differential signal is exceeds the threshold voltage, the receiver would determine the logic of input data is switched. In IEEE LVDS standard, a differential voltage grater than or equal to V_{idth}(max) is a logic high, and less than or equal to V_{idth}(min) is a logic low.

In ideal case, the amplitude and common-mode voltage of the steady-state differential signals would not change, but in application case, both of the amplitude and common-mode voltage would change. Thus, IEEE LVDS standard defines the acceptable range of these

changes on signal level. Fig. 2.3 defines the change range of the differential voltage (ΔV_{od}) and the driver offset voltage (ΔV_{os}) in IEEE LVDS standard. ΔV_{od} and ΔV_{os} can also be defined in a expression way. Equation (2-1) and equation (2-2) are the definitions of ΔV_{od} and ΔV_{os} respectively.

$$\Delta V_{od} = \left|V_{od}(high)\right| + \left|V_{od}\right|(low)\left| \right. \tag{2-1}$$

where $V_{od}(high) = V_{oph} - V_{onl}$, and $V_{od}(low) = V_{onh} - V_{opl}$

$$\Delta V_{os} = \left|V_{os}(high) + V_{os}(low)\right| \tag{2-2}$$

where $V_{os}(high) = (V_{oph} - V_{onl})/2$, and $V_{os}(low) = (V_{opl} - V_{onh})/2$

Table 2.1 shows the detail of the driver specification in general purpose link case in IEEE LVDS standard.

2.2.3 Receiver Input Level

Fig. 2.4 shows the receiver signal level. When the differential input signal is greater than $+V_{idth}$, the receiver would detect the input data as logic high. If the input signal were lower than $-V_{idth}$, the receiver would detect the input data as logic low. To eliminate the possibility of oscillating receiver output signal when the differential input signal is undefined, the threshold hysteresis is needed in receiver design. The undefined input signal may occur when the receiver inputs are unconnected, or when the connected driver is powered down. Fig. 2.5 shows the receiver hysteresis. When the input signal is changing between $+V_{idth}$ and $-V_{idth}$, the receiver would not change the output state.

When the link is operated between two different circuit boards, the different ground-potential may shift the common-mode voltage level. To avoid the error recovered data induced by the different common-mode level happen, the specificity defines an acceptable common-mode voltage range. Fig. 2.6 shows the V_{icm} waveform. V_{icm} defined as the average of V_{ia} and V_{ib} measured with respect to the receiver ground potential. Besides the different potential between driver ground and receiver ground, noise couple between channels would also induce the move of the common-mode level. IEEE standard limits the maximum shift value of common-mode level, and defines the $V_{icm}(max)$ and $V_{icm}(min)$ to limit the range of the input V_{icm} waveform.

A link system transmitting parallel signals must consider the effect of skews. Because the different channel environments or noise couples, the synchronous signals transmitted through different channels may arriver the receiver in different time. On the other hand, the synchronous signals become asynchronous after transmitted through different channels, and skews between signals must be considered when the receiver recovers these parallel signals. IEEE standard defines the range of skews, and in this rang the receiver must be able to recover data with skews correctly. Fig. 2.7 defined the t_{skew} for propose of IEEE standard. To set the specificity of signal level more completely IEEE standard defines another two kind of skews for generated differential signal beside t_{skew}. Skew 1 called t_{skew1} is the skew between the high-to-low and low-to-high transitions of complementary single-ended signal. Fig. 2.8 shows the definition of t_{skew1}, and equation (2-3) defines t_{skew1} in expression. Skew 2 called t_{skew2} is the skew between any differential signals measured at the output of driver. Fig. 2.9 shows the definition of t_{skew2}, and equation (2-4) defines t_{skew2} in expression.

$$t_{skew1} = \left|tp_{HLA} - tp_{LHB}\right| \quad or \quad \left|tp_{HLB} - tp_{LHA}\right| \tag{2-3}$$

Where $tp_{HLA/B}$ and $tp_{LHA/B}$ are the propagation delays on driver output A and B for high

to low and low to high.

$$t_{skew2} = \left| tp_{diff}[i] - tp_{diff}[j] \right| \tag{2-4}$$

Where i is any one of the parallel signals and j is any other signal.

Table 2.2 shows the detail of the receiver specification in general purpose link case in IEEE LVDS standard.

Table 2.1 LVDS driver specification in general purpose link case

Symbol	Parameter	Conditions	Min	Max	Units
V_{oh}	Output voltage high, V_{oa} or V_{ob}	R_{load} = 100 Ω ± 1%		1475	mV
V_{ol}	Output voltage low, V_{oa} or V_{ob}	R_{load} = 100 Ω ± 1%	925		mV
$\|V_{od}\|$	Output differential voltage	R_{load} = 100 Ω ± 1%	250	400	mV
V_{os}	Output offset voltage	R_{load} = 100 Ω ± 1%	1125	1275	mV
R_o	Output impedance, single ended	V_{cm} = 1.0 V and 1.4 V	40	140	Ω
ΔR_o	R_o mismatch between A & B	V_{cm} = 1.0 V and 1.4 V		10	%
$\|\Delta V_{od}\|$	Change in $\|V_{od}\|$ between “0” and “1”	R_{load} = 100 Ω ± 1%		25	mV
ΔV_{os}	Change in V_{os} between “0” and “1”	R_{load} = 100 Ω ± 1%		25	mV
I_{sa}, I_{sb}	Output current	Driver shorted to ground		40	mA
I_{sab}	Output current	Driver shorted to together		12	mA
$\|I_{xa}\|$, $\|I_{xb}\|$	Power-off output leakage	V_{cc} = 0 V		10	mA
Clock	Clock signal duty cycle	250 MHz	45	55	%
t_{fall}	V_{od} fall time, 20-80%	Z_{load} = 100 Ω ± 1%	300	500	ps
t_{rise}	V_{od} rise time, 20-80%	Z_{load} = 100 Ω ± 1%	300	500	ps
t_{skew1}	Differential skew	Any differential pair on package		50	ps
t_{skew2}	Channel-to-channel skew	Any two signals on package		100	ps

Table 2.2 LVDS receiver specification in general purpose link case

Symbol	Parameter	Conditions	Min	Max	Units
V_i	Input voltage range, V_{ia} or V_{ib}	$\|V_{gpd}\| < 925$ mV	0	2400	mV
V_{idth}	Input differential threshold	$\|V_{gpd}\| < 925$ mV	−100	+100	mV
V_{hyst}	Input differential hysteresis	$V_{idhh} - V_{idhl}$	25		mV
R_{in}	Receiver differential input impedance	———	90	110	mV
t_{skew}	Skew tolerable at receiver input to meet set-up and hold time requirements	Any two package inputs		600	Ω

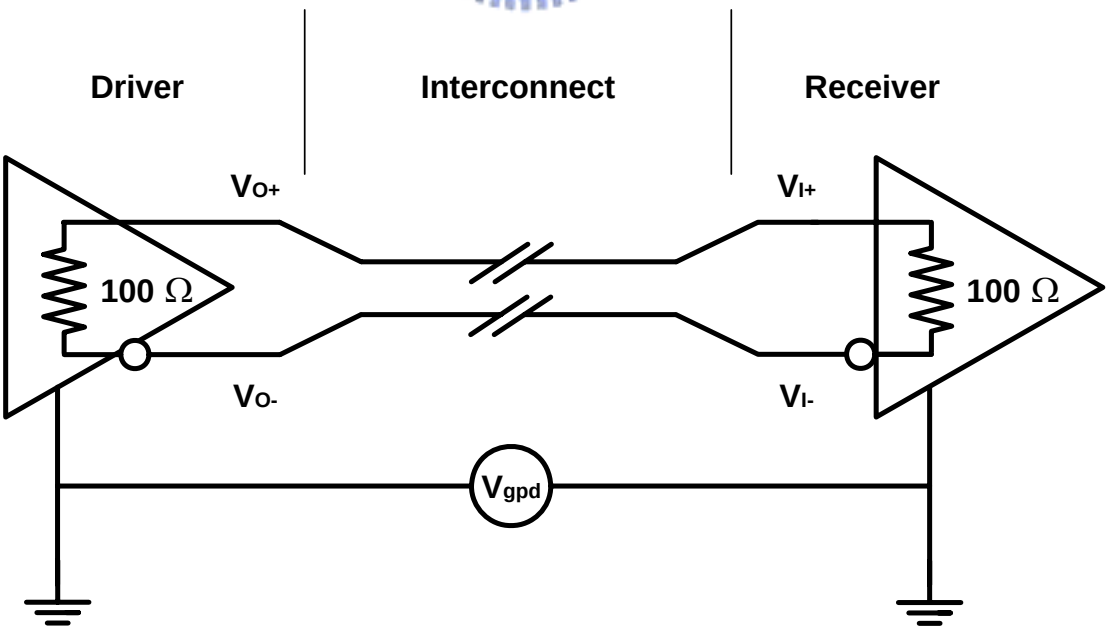


Fig. 2.1 Typical LVDS interface

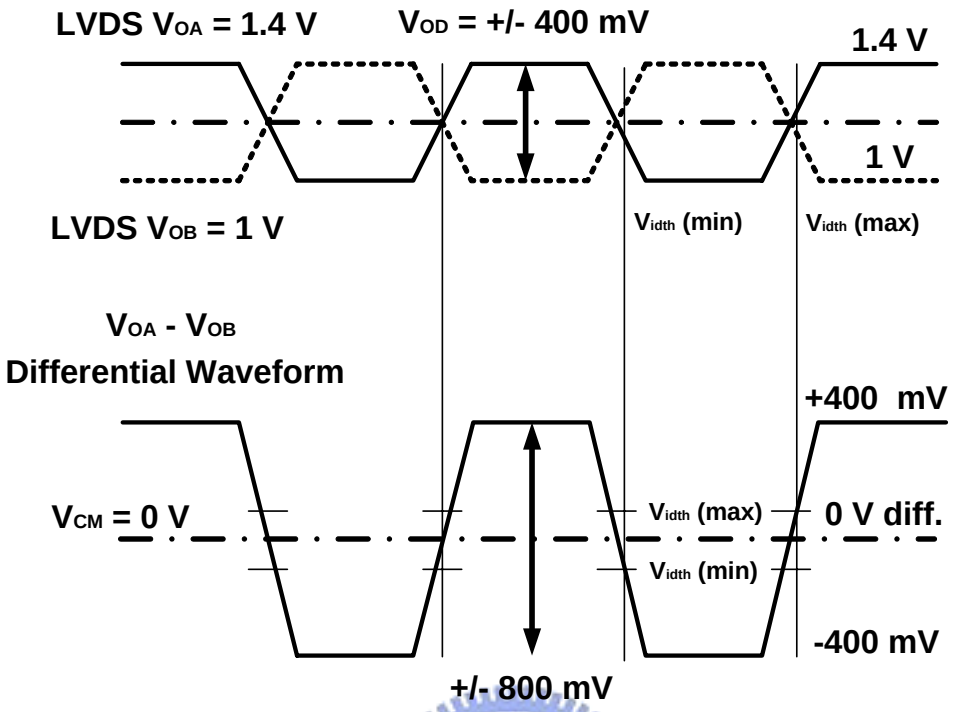


Fig. 2.2 The driver signal level of LVDS for 1.2V V_{OS}

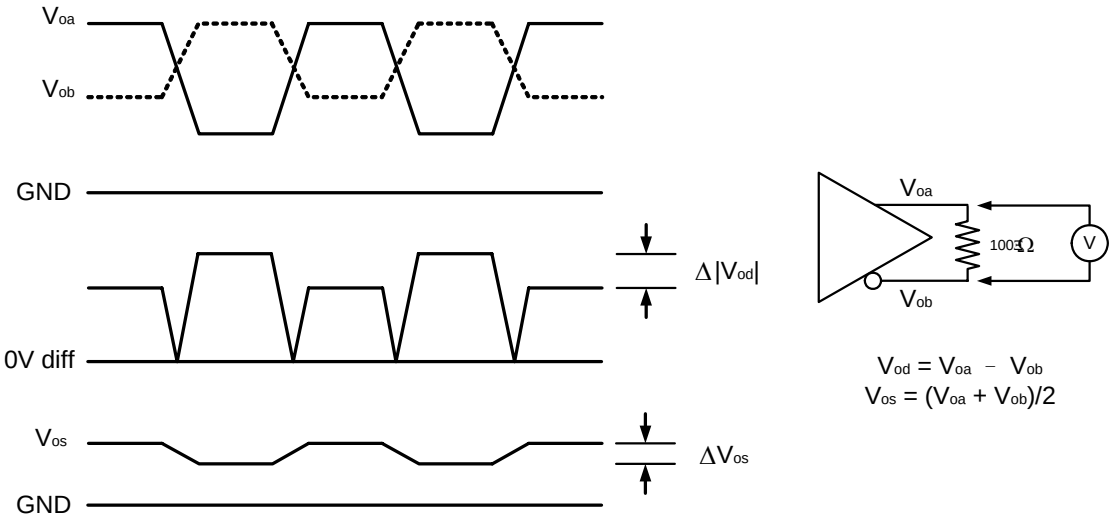


Fig. 2.3 The definition of ΔV_{od} and ΔV_{os}

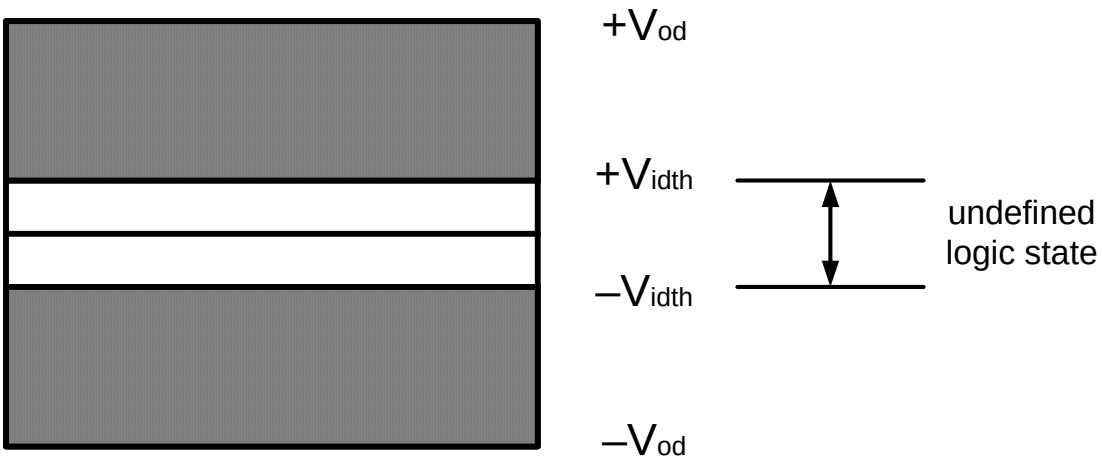


Fig. 2.4 Receiver input signal levels

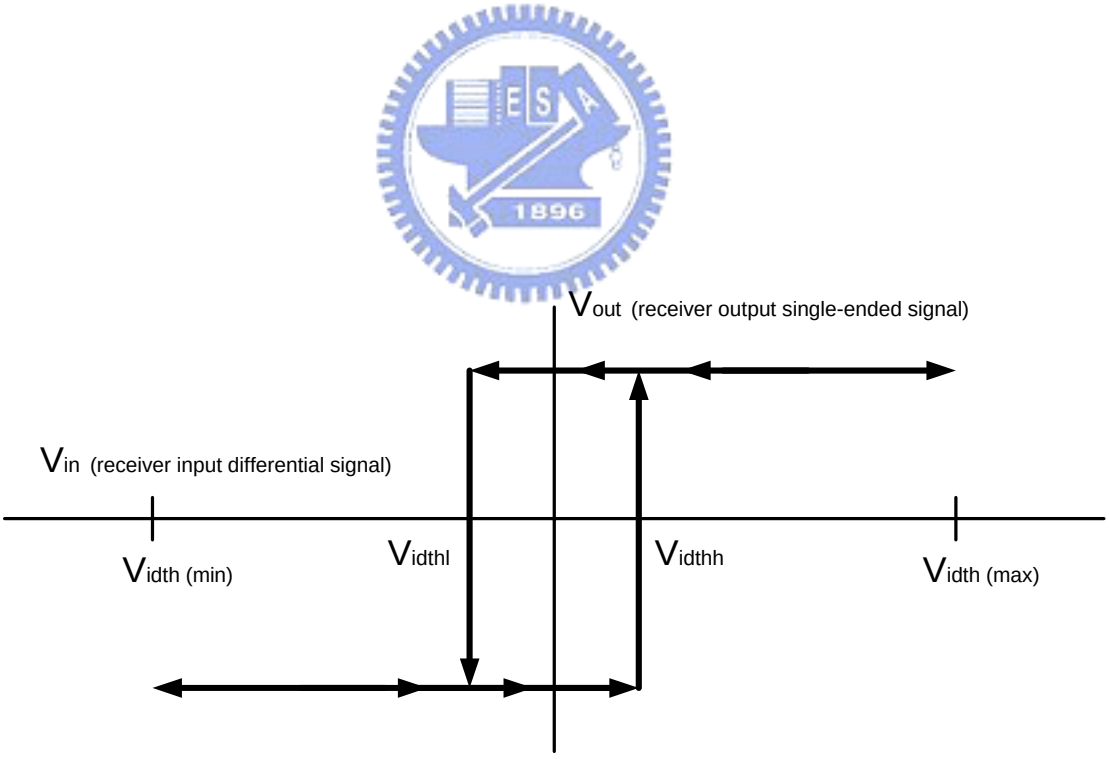


Fig. 2.5 Receiver hysteresis

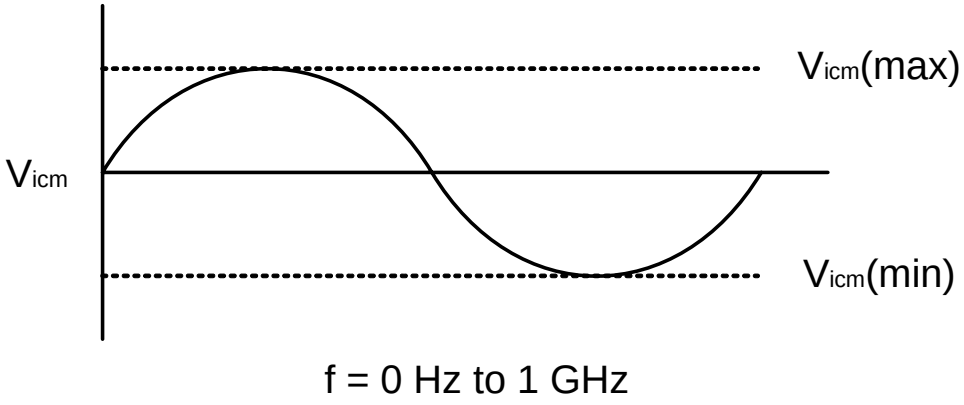


Fig. 2.6 V_{icm} input waveform

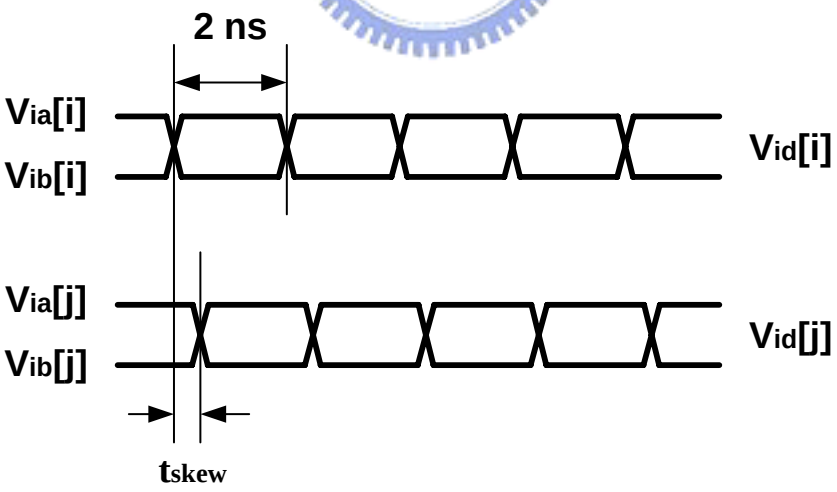


Fig. 2.7 t_{skew} between two receiver inputs

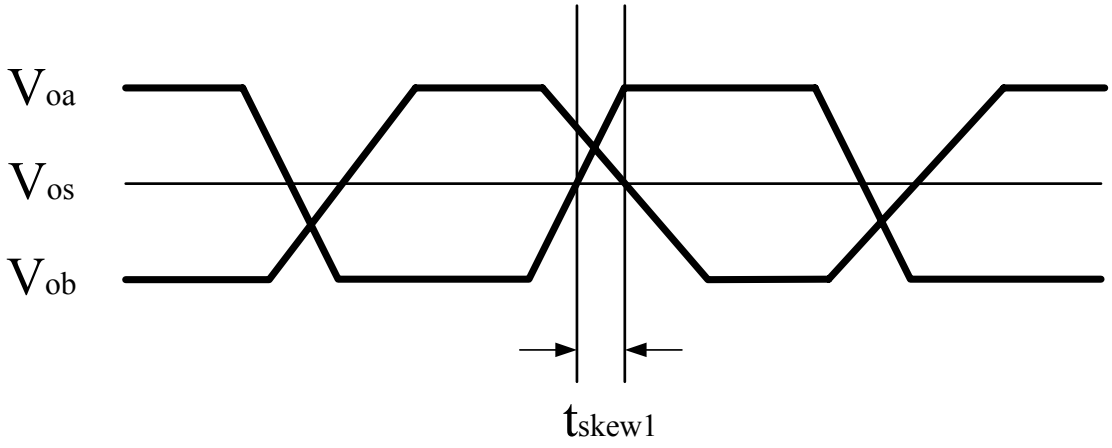


Fig. 2.8 t_{skew1} between complementary single-ended signals

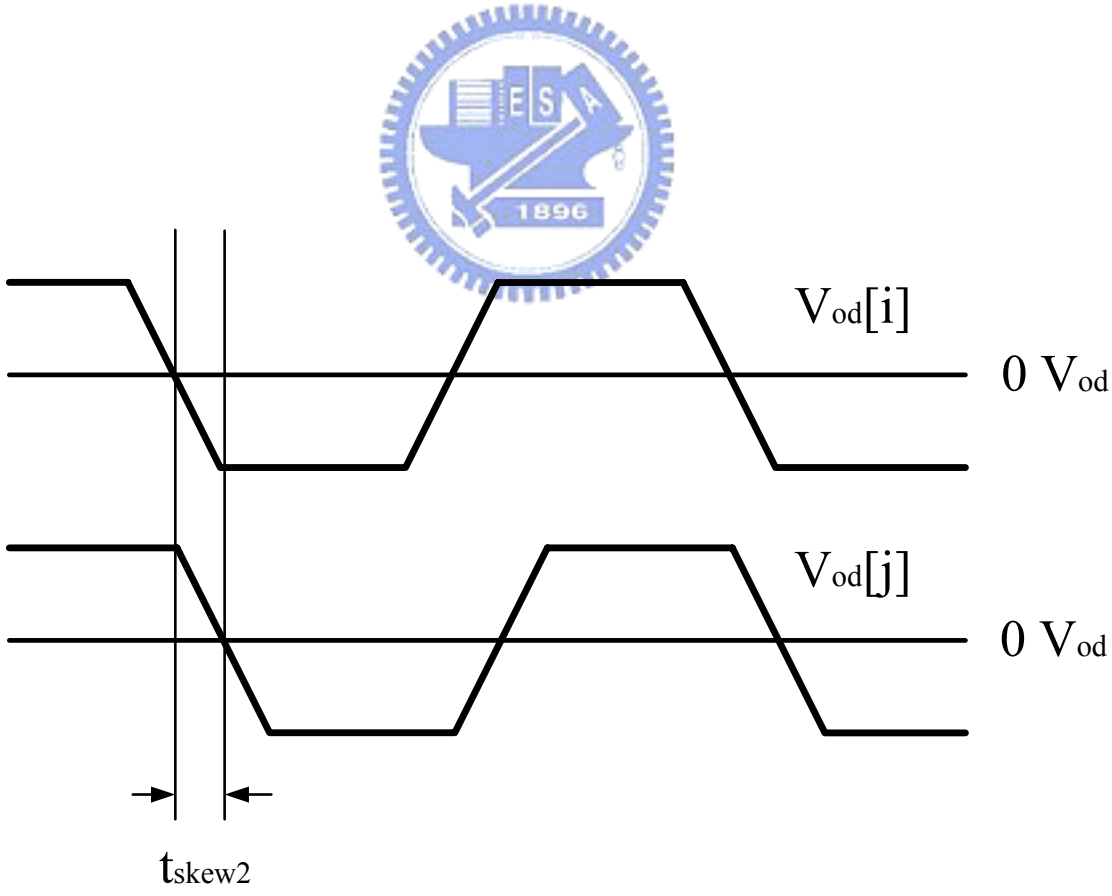


Fig. 2.9 t_{skew2} between any parallel signals

Chapter 3

Architecture of Data Recovery System

3.1 TRADITIONAL DESIGN

In a typical FPD Link, there are four data channels and one clock channel as shown in Fig 3.1. The driver serializes seven parallel data into one channel. Fig 3.2 shows the timing relation between clock and serialized data. The data rate of each serialized data is seven times the frequency of the clock. However, the different parasitic effect in each channel will induce different time delay and distortion on each transmitted data and clock. Because the different channel effect, these signals will become asynchronous after arrive the receiver. In ideal case, no skews happen after channel effect, the receiver needs only a PLL (phase lock loop) to lock the input clock and proffer seven different data-sampling clock phases and by using these different sampling clock phases the receiver can recover the serial data into seven parallel data with data rate the same as the clock frequency (in FPD Link there are seven different data are serialized in each channel in one clock period). Fig. 3.3 shows the operation timing in the idea case. In application cases, skews between any two signals are unavoidable and the seven different data-sampling clock phases may locate nearly transition edges of the serial data as shown in Fig. 3.4. If the sampling clock phase is near the transition edge, the changing data may be missed or double sampled as shown in Fig 3.5. Thus, to avoid these error data induced by skews happen the recovery system needs an extra mechanism to detect the happen of skews and shift the sampling clock phases away the transition edges of the each serial signal to make sure that these data can be sampled in stable state.

3.2.1 Three Times Oversampling

In traditional design, three times oversampling is usually used in recovery system [4] - [6]. In FPD Link using three times oversampling needs a PLL proffer 21 different sampling clock phases, three times the number of serial data in one clock period. By using these 21 different sampling clock phases, the recovery system can oversample each datum three times as shown in Fig. 3.6. However, when the skews between data and clock happen, the oversampled results of the same datum may be different as the logic state of serial data is changing. Fig. 3.7 shows the sampling timing relation when the skew between serial data and clock happens.

By detecting the different between sampled data sampling the same serial datum, three times oversampling system can detect whether the skew happens or not. Fig. 3.8 shows the timing relation between sampling clock phases and serial data when different skews happen. In Fig. 3.8 (a), as the sampling clock phases lag input serial data stream by a certain amount, data transition might appear between second and third sampled data value within data information set. In Fig. 3.8 (b), if the sampling clock phases lead the input serial data stream by a certain amount, data transition might appear between first and second data value within data information set. In case Fig. 3.8 (c), the input serial data stream is lock by the sampling clock phases, and the first, second and third data value within data information set are the same.

3.2.2 Phase Selecting

Fig. 3.9 shows the architecture of a traditional CDR (clock and data recovery circuit) [4]. It consists of two input buffer, a data sampler, a synchronizer, a phase detector, a voter, a DLPF (digital low pass filter), a phase selector, and a PLL (phase lock loop). One of these two input signal is serial input data in LVDS signal, and another one is input clock in LVDS signal too.

At first, these two input buffer transmit input signals from LVDS signals into full-swing signals. The PLL locks the full-swing input clock and provides the data sampler 21 different sampling clock phases. Because the data rate of input serial data stream is seven times the frequency of input clock, the data sampler uses these 21 different sampling clock phases provided by PLL to sample each serialized datum three times. After data sampler, the input data stream is divided into 21 bits data. However, because these 21 bits data are sampled by different sampling clock phase these 21 bits data translate in different time. On the other hand, the 21 bits data are asynchronous as shown in Fig 3.10. To reduce the complexity of the recovery system, the synchronizer is used to synchronize the 21 bits asynchronous data.

By comparing every three sampled data of each serial datum, the phase detector can detect if any serial datum is lagged or leaded. If one datum were detected lead or lag, the first sampled result is different from the second and third sampled results or the third result is different from the first and second results, the phase detector would send a signal “up” or “down” in a couple bits, one “up” bit and one “down” bit, as the phase detecting result of this datum. Thus, in each clock period the phase detector would send out seven couple bits as detecting result signals of these seven serial data respectively.

However, because the effect of jitters these seven detecting result signal would not always the same. For example, one “up” result and three “down” results appear in one clock period as shown in Fig. 3.11. After the phase detector is a voter. The voter would receive seven couple bits from the phase detector in every clock period. Each couple bits carry the detection information of one serial datum in this clock period. By comparing these “up” bits and “down” bits in these seven couple bits, the voter must determine whether the input serial data stream leads the input clock or lags. If the “up” signals is over tow bits more than the “down” bits, the voter would send out another “up” signal. On the other hand, if the “down” signals are over two bits more than the “up” bits, the voter would send out another

“down” signal.

In application cases, the effect of jitters is serious and that means the jitters disperse in a large rang. Thus the voter is not enough to avoid the wrong “up” or “down” signal induce by the effect of jitters. To increase the jitter tolerance of the CDR, after voter the “up” or “down” signal must pass the DLPF, that means the DLPF would not let the “up” or “down” signal pass unless the “up” or “down” bit must keep in high logic for three consecutive clock periods at least. If the “up” or “down” bit keeps in high logic over three consecutive clock periods the DLPF would send out anther real “up” or “down” signal.

The phase selector would receive a couple of bits, one real “up” bit and one real “down” bit, in every clock period. If the DLPF pass a real “up” signal to the phase selector, the phase selector would accept the detection that the input serial data stream leads these 21 sampling clock phases and shift up these 21 different sampling clock phases one phase let faster sampling clock phases sample the input serial data stream in next clock period. Similarly, if the DLPF pass a real “down” signal to the phase selector, the phase selector would accept the detection that the input serial data stream lags these 21 sampling clock phases and shift down these 21 different sampling clock phases one phase let slower sampling clock phases sample the input serial data stream in next clock period. Fig. 3.12 shows the operation of the phase selector.

These detecting system will keep shifting these data sampling clock phases up or down until there are no real “up” and real “down” signals are send into the phase selector and that mean the three times oversampling is in lock state. Fig. 3.13 shows the timing relation between the input serial data stream and the input clock in lock state. In lock state, when jitters happen the first sampled datum and third sampled datum may be an error datum that sampled in wrong datum but the second sampled datum would keep the same logic stat with the sampled datum because the second sampling clock phase would still be kept in the right datum. Thus, the CDR would select each second sampled result as the recovered datum of

each serial datum and send out these seven recovered data in parallel as the output of the CDR.

Besides, to differentiate the new architecture of CDR presented in following from the traditional design, the architecture of a traditional CDR is called “phase selecting”.

3.2 NEW DESIGN

3.2.1 Three Quarter Steps Oversampling

Fig. 3.14 shows a typical architecture of a PLL. The number of VCO cells in a PLL is determined by the number of phases the PLL must provide. Besides, in application cases, these VCO cells are usually designed in fully differential and that can increase the stability of the PLL. Because these VCO cells are fully differential, these inverted phases can be used as the output phases of the PLL when the number of phase the PLL must provide is an even number. Thus, if a PLL is required to provide n phases where n is an even number, the PLL can use only n/2 VCO cells to provide n different phases dispreading in one clock period uniformly. Fig. 3.15 shows the relation between output phases of the VCO cells and output phases of the PLL when the PLL must provide 8 different phases in one clock period. However, if the PLL must provide odd number phases, the PLL can’t use these inverted phases of VCD as output phases and a PLL providing n number phase where n is an odd number must use n VCO cells to provide these output phase the PLL must provide.

In application cases of FPD Link, because the input data stream is 7 bits deep signal serialized in one clock period, the PLL must provide 21 different sampling clock phases to implement three times oversampling. Because 21 is an odd number, the PLL can not use these inverted phases of VCO cells as a part of these 21 different sampling clock phases. Thus, in three times oversampling the PLL must use 21 VCO cells to provide 21 different sampling clock phases dispreading uniformly in one clock period and that would make the

layout area of the PLL expand. However, the VCD is the primary part in the layout area of the PLL. To reduce the problem this thesis presents a modified process, which is called “three quarter steps oversampling”, to recover data.

In “three quarter steps oversampling” the PLL provides 28 different sampling clock phases dispreading uniformly in one clock. Because there is seven data are serialized in one clock, there are four different sampling clock phases in ever data step and each distance between every two adjacent phases is equate to a quarter data step time. To detect the locations of skews between input data stream and input clock the “three quarter steps oversampling” would select three of these four phases in each data step to oversample each datum. Because each datum is oversampled three times and each distance between every two adjacent sampling clock phases is equate to a quarter step time, this modified process which is used to recover data is called “three quarter steps oversampling”. Because the PLL in “three quarter steps oversampling” provides 28 different sampling clocks phases where 28 is an even number, the PLL can use only 14 VCO cells to provide these sampling clock phases. Thus, the number of VCO cells used in “three quarter steps oversampling” is less than that used in “three times oversampling”. On the other hand, the layout area of the PLL used in “three quarter steps oversampling” will be smaller than the PLL used in “three times oversampling”. Fig. 3.16 shows the VCO cells of the PLL used in “three quarter steps oversampling” and “three times oversampling” respectively.

Fig 3.17 shows the operation of the “three quarter steps oversampling”. By using 21 of these 28 different sampling clock phases provided by the PLL, the CDR could detect whether the sampling clock phases lag input data stream or lead. If the sampling clock phases lag the input data stream as shown in Fig. 3.17 (a), the CDR would shift up these sampling clock phases one phase. If the sampling clock phases lead the input data stream as shown in Fig. 3.17(b), the CDR would shift down these sampling clock phases one phase. The CDR would keep shifting these sampling clock phases until the input data stream is

locked by these sampling clock phases as shown in Fig. 3.17 (c).

Besides the improvement of reducing the layout area of PLL, the “three quarter steps oversampling” also has higher tolerance of input data eye diagram. Fig. 3.18 shows the timing relation between the eye diagram of the input data stream and the sampling clock phases in the “three quarter steps oversampling” case and the “three times oversampling” case respectively. In “three quarter steps oversampling” the CDR can keep in lock state when the eye diagram of the input data stream closes nearly 50%, but in “three times oversampling” the eye diagram of the input data stream must open over 60% to keep the CDR in lock state.

3.2.2 Delay Selecting

Three quarter steps oversampling does reduce the size of PLL, but it also has another problem. There are only 21 phases used to sample data when three times oversampling is used, but there will be 28 phases used to sample data when three quarter steps oversampling is used. Using more different phases to sample data will make the layout of CDR more complex. Besides, because the sampling clock phases used in three quarter steps oversampling is more than that used in three times oversampling, the three quarter steps oversampling CDR need more MUXs to implement the motion of selecting sampling clock phases.

To overcome this problem, a new architecture of a CDR is presented in following. Besides using three different sampling clock phase oversample data stream, using the same sampling clock phase sample three different delayed data can also detect the happen of skews too [9]. By using VCO cells as delay cell, the CDR can delay input data stream one phase, two phases, and three phases respectively. Using these three the same data streams delayed one phase, two phases, and three phases as a detection window, the CDR can use one sampling clock detect whither the edge happens in this windows as shown in Fig. 3.18.

If there is any edge happens in the detection window, the CDR will change the delayed time up or down one phase in next clock period.

Fig. 3.19 shows the operation of delay selecting. If the edge happens between the data delayed one phase and the data delayed two phases, the delay time of input data stream would be decrease one phase in next clock period. If the edge happens between the data delayed two phases and the data delayed three phases, the delay time of input data stream would be increase one phase in next clock period. The delay time would be changed until there no edge happens in the detection window.

Fig. 3.20 shows the architecture of the delay selecting CDR. To implement the operation of delay selecting, the CDR use VCD cells as delay cells create three data stream delayed in different phased. One of these three delayed data streams would be selected and the selected stat stream would be sent into the detection window. In the detection window the selected data stream is delayed into three different delayed data streams again. In detection window the CDR can use only seven different sampling clock phases to sample these three data stream and detects whether any edge happen. The detection window would send out “up” and “down” signals in every clock period. The same as the phase selecting CDR, these “up” and “down” signal must pass a voter and a DLPF. After passing the voter and the DLPF, if a real “up” or “down” signal is send out, the delay selector would change the selected data stream up or down as shown in Fig. 3.21. If the skew is over a data step time the information between input signals is not enough to detect whither the skew is a lead skew or a lag one. To avoid this undetected skew, LVDS specificity would limit the skew range between every two different channel. Because the skew range between every two different channel is limited in one data step time, the delay selector only need three different delay timing, one phase delay, two phases delay, and three phases delay, to be selected to cancel the skew.

By using delay selecting to implement three quarter steps oversampling the CDR can

reduce the number of sampling clock phases from 28 to 7 and also reduce the number of MUXs. On the other hand, the layout area is reduced and simplified.

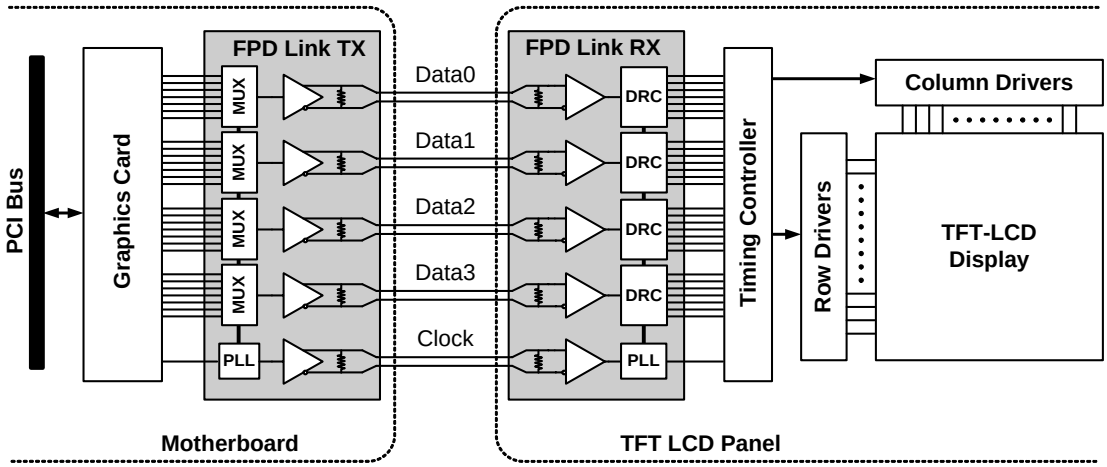


Fig. 3.1 Typical FPD Link

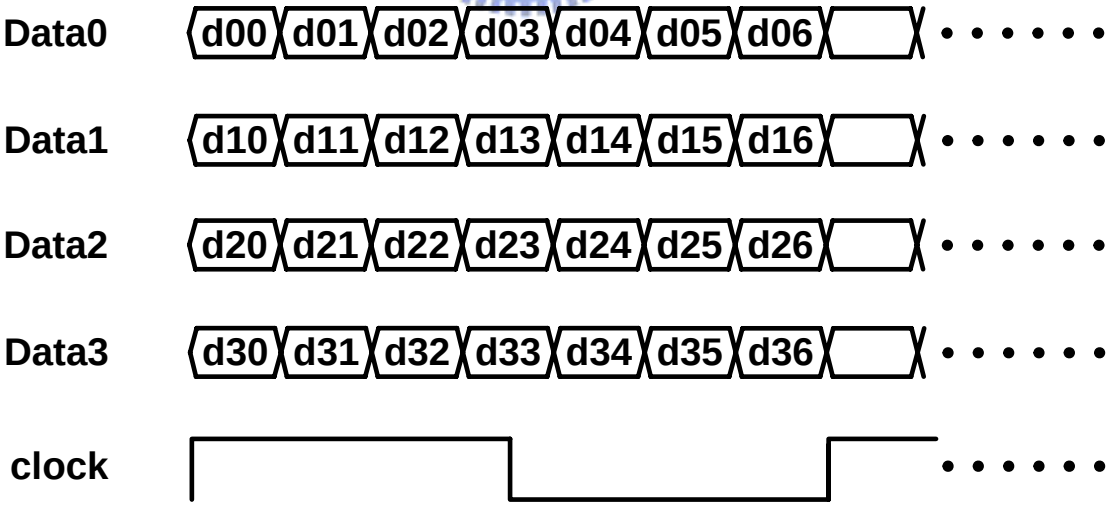


Fig. 3.2 Timing relation between clock and serial data streams

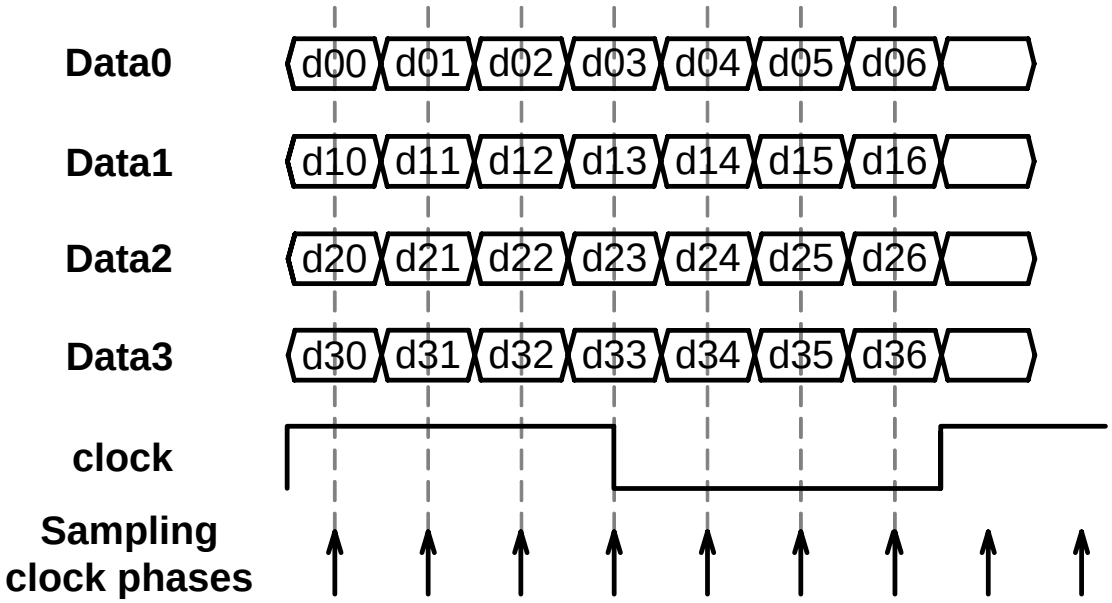


Fig. 3.3 Operation timing in ideal case

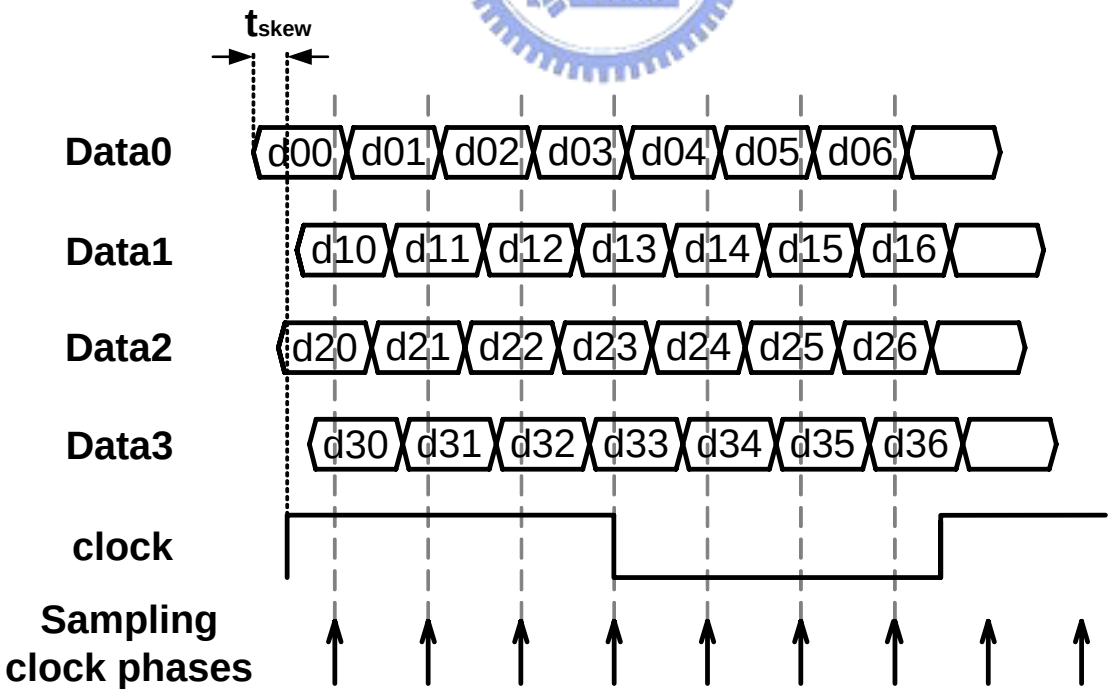


Fig. 3.4 Operation timing in real cases

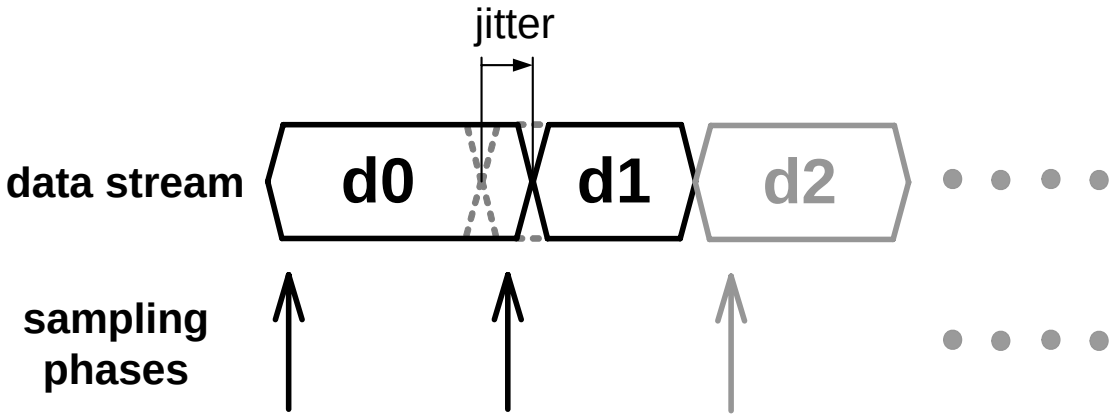


Fig. 3.5 Operation timing when jitters happen, d0 is double sampled and d1 is missed

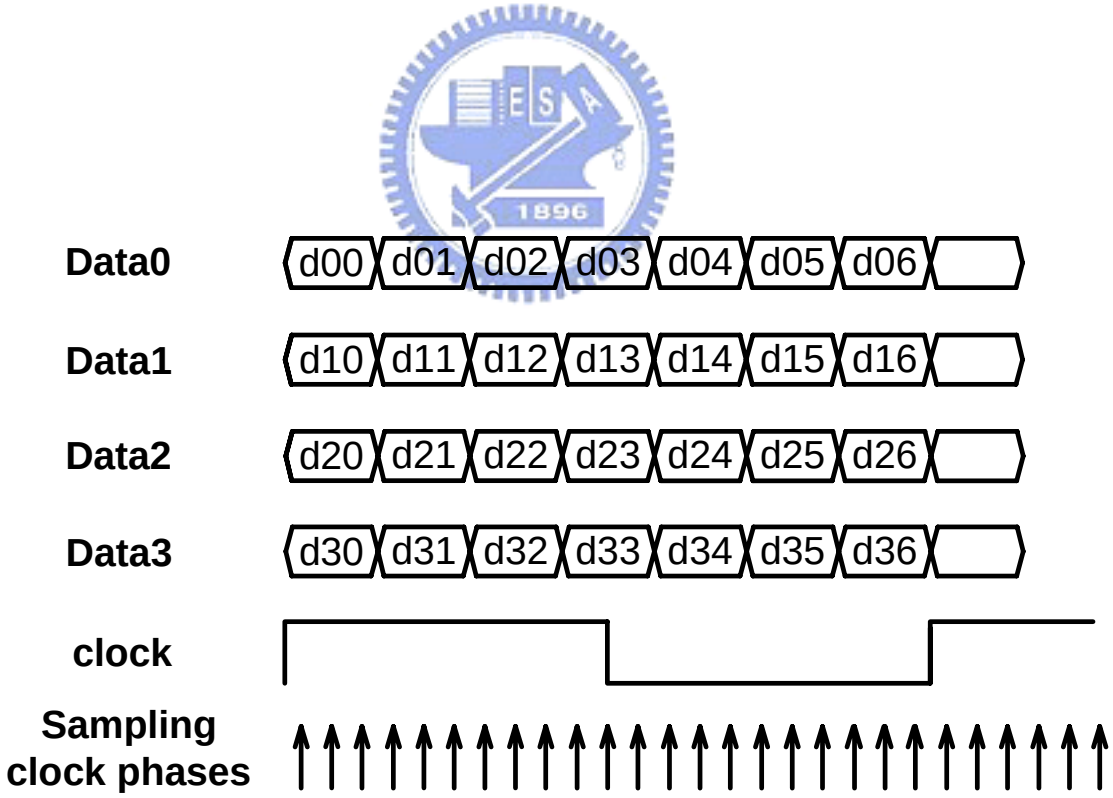


Fig. 3.6 Operation timing of three times oversampling

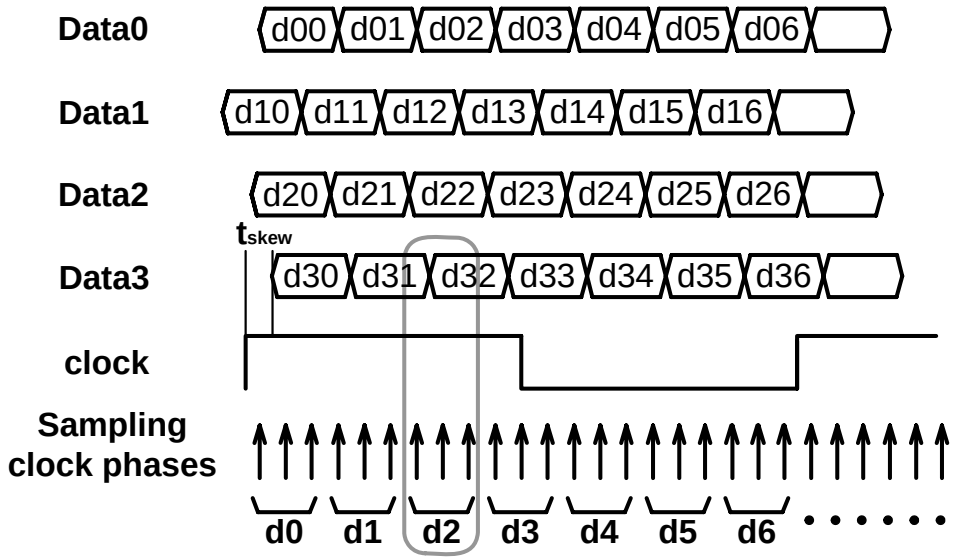


Fig. 3.7 Operation timing of three times oversampling when skews happen

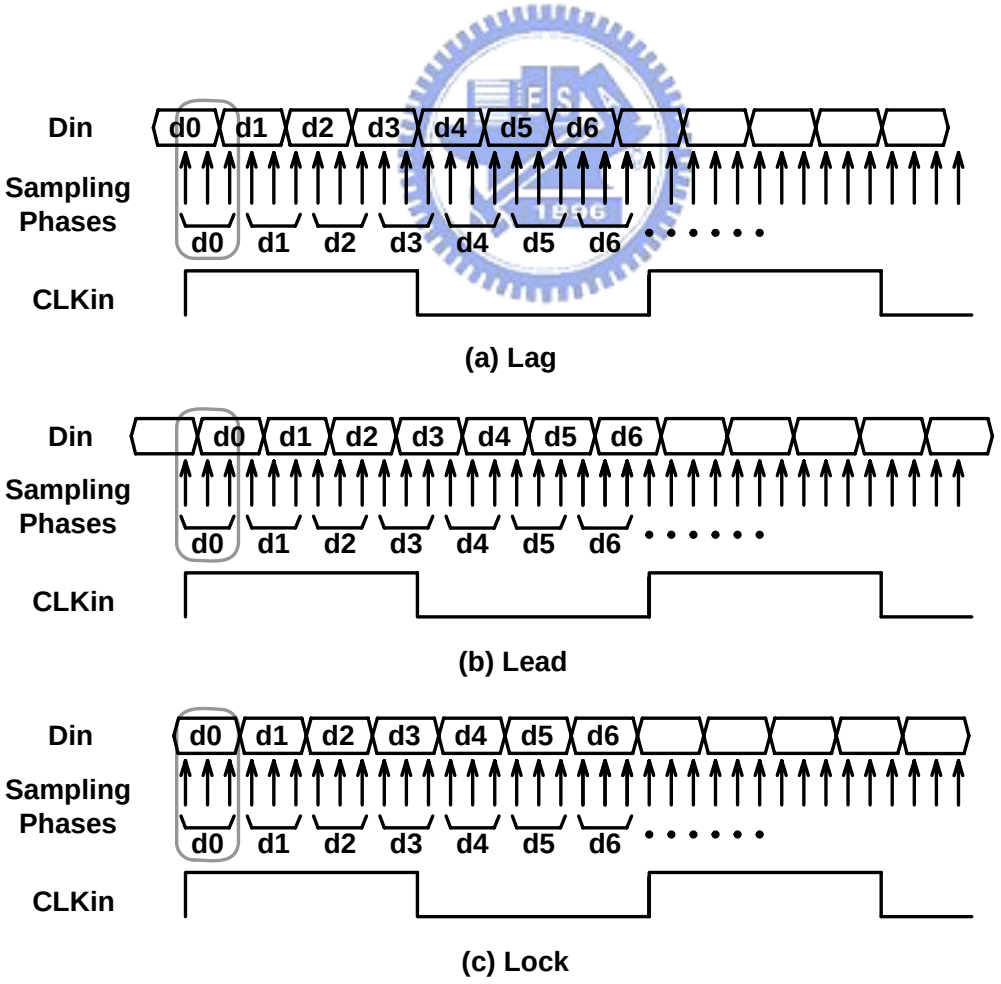


Fig. 3.8 (a) Lag, (b) lead and (c) lock states of three times oversampling

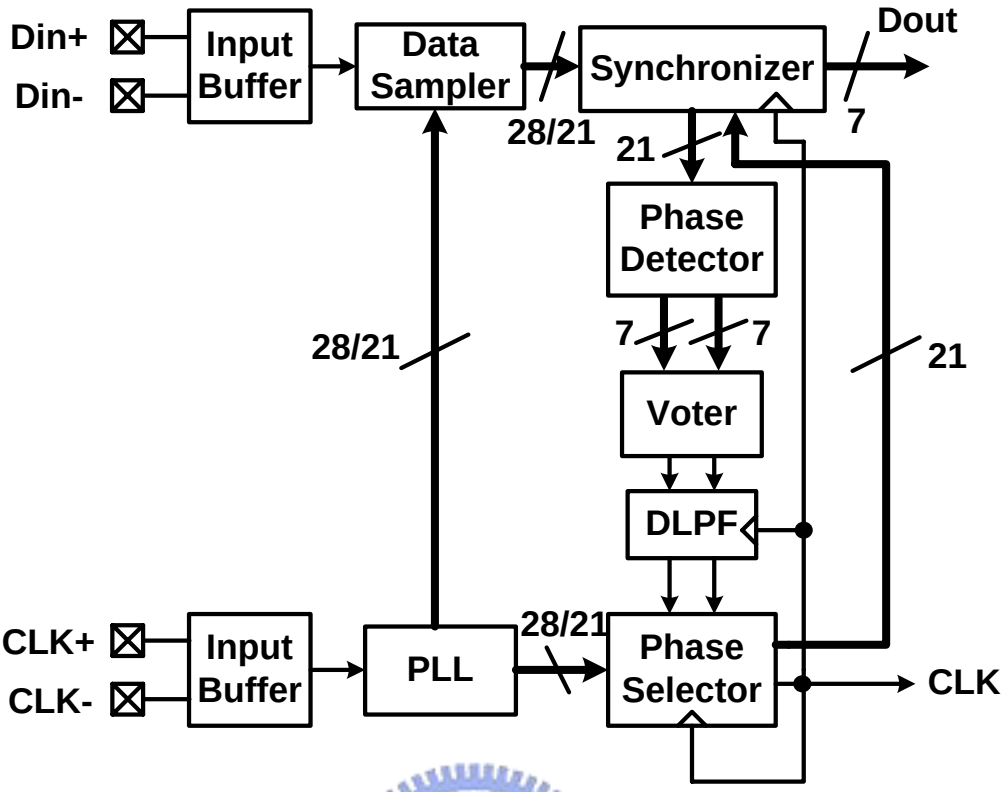


Fig. 3.9 Architecture of a traditional CDR

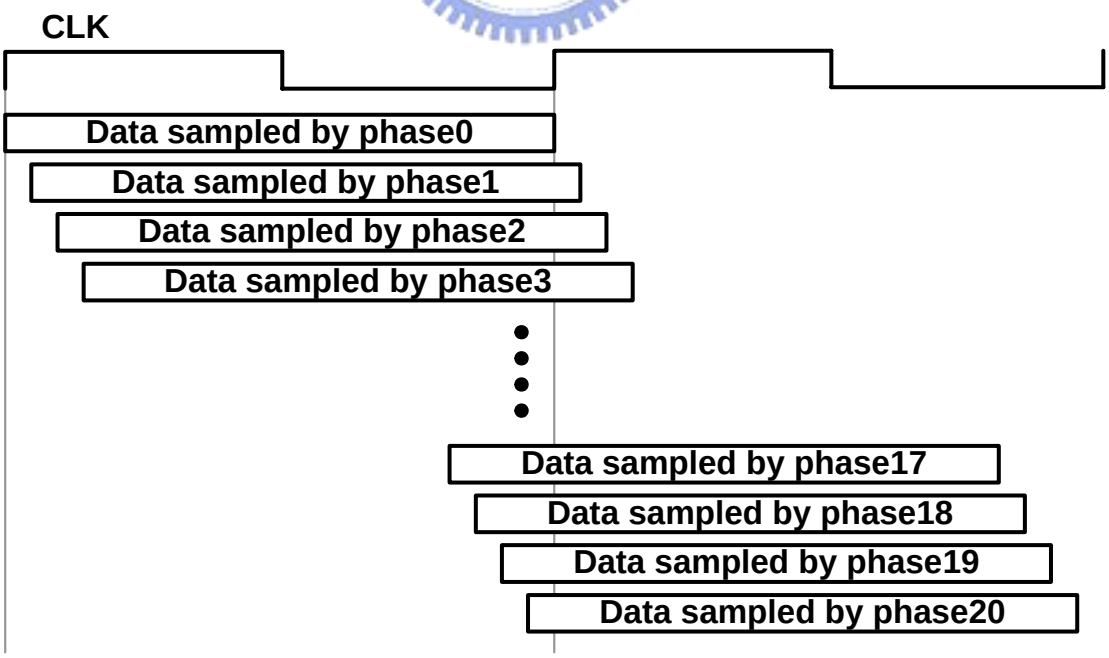


Fig. 3.10 Timing relation between sampled data

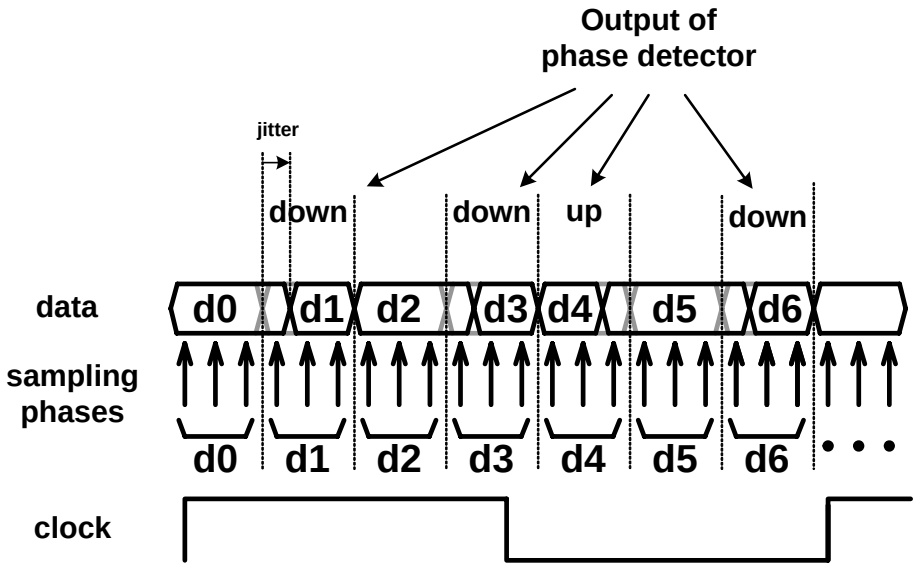


Fig. 3.11 Operation of phase detector when jitters happen

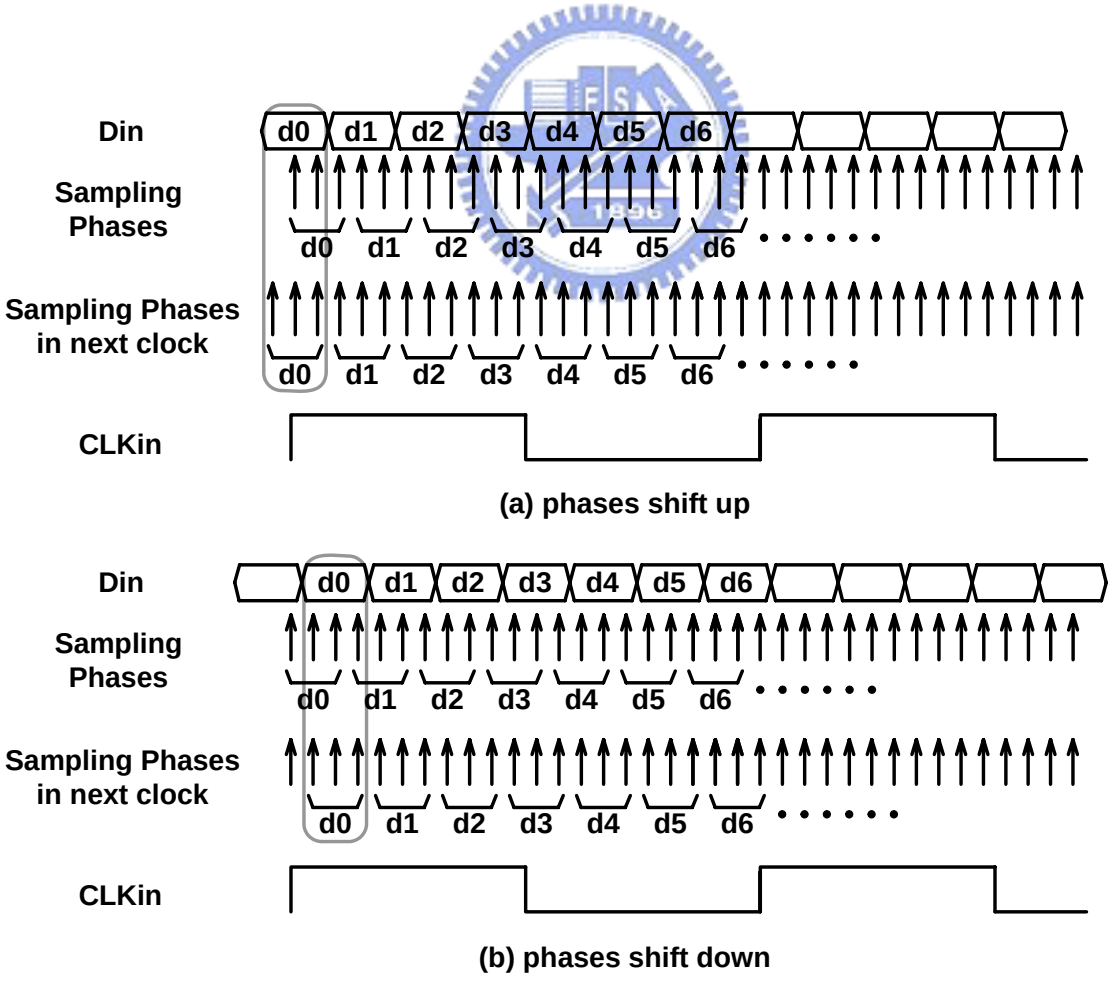


Fig. 3.12 Operation of phase selector

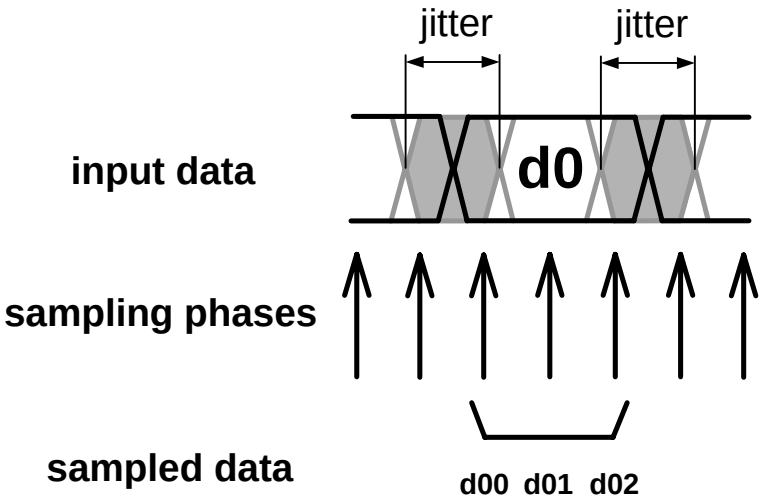


Fig. 3.13 Data sampling timing when jitters happen

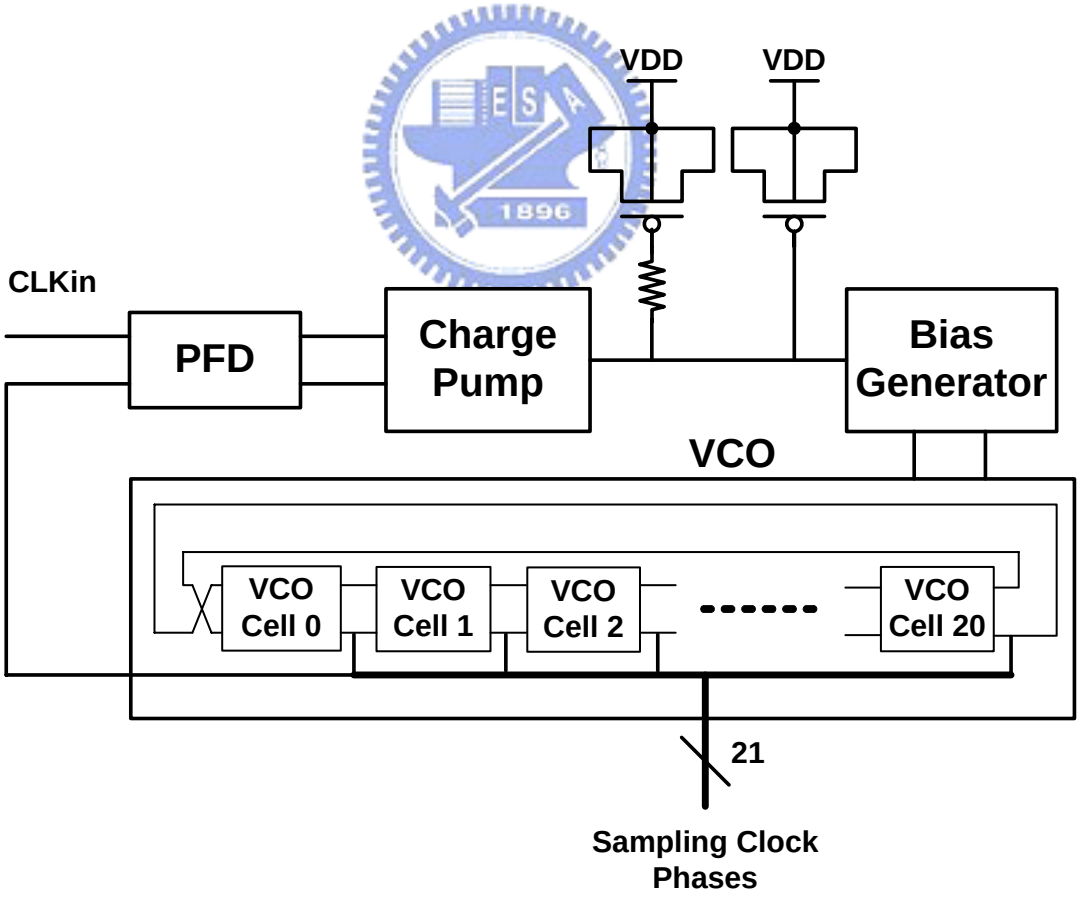


Fig. 3.14 Typical architecture of a PLL

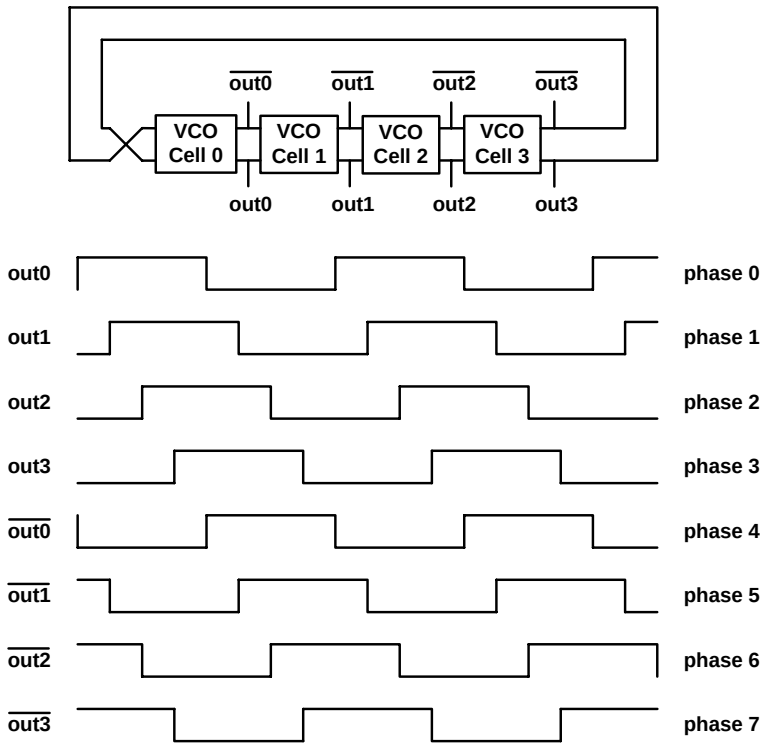


Fig. 3.15 Timing relation between VCO cells outputs

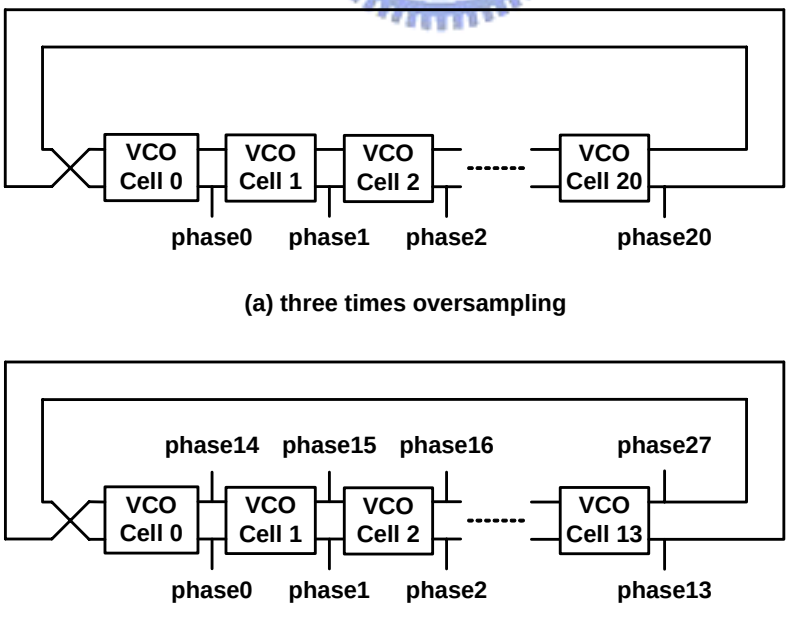


Fig. 3.16 Comparison of VCO cells number

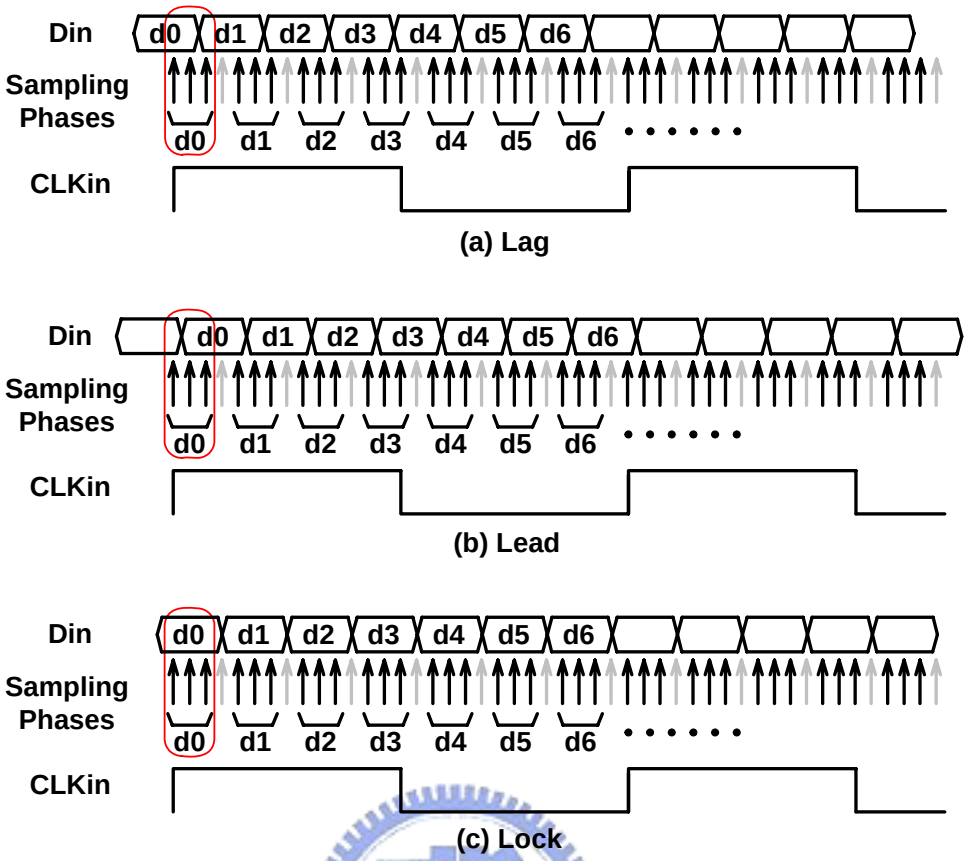


Fig. 3.17 Operation of "three quarter steps oversampling"

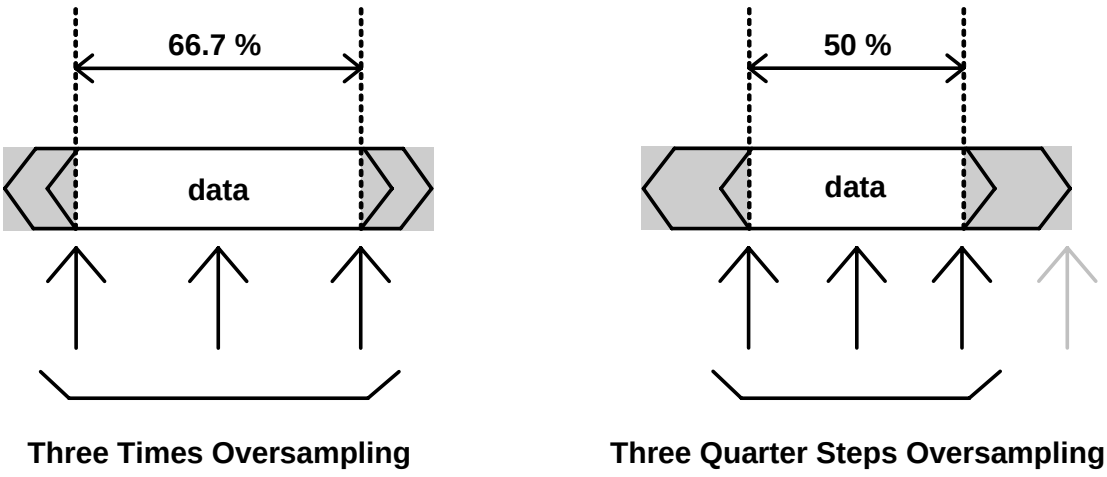


Fig. 3.18 Comparison of eye diagram tolerance in lock state

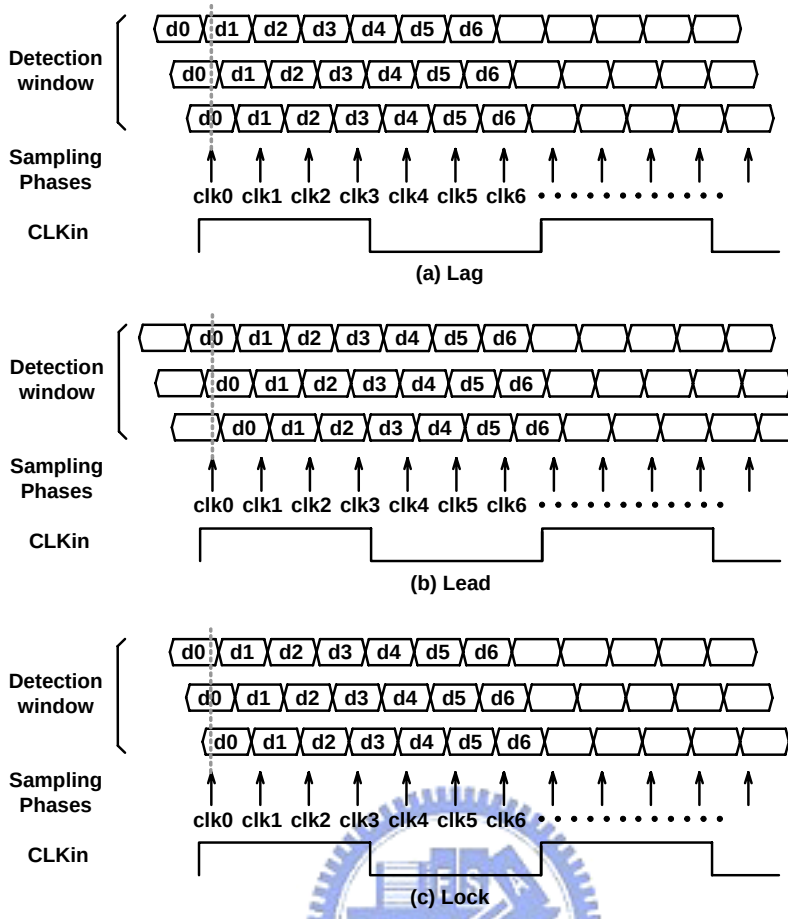


Fig. 3.19 Operation of the detection window

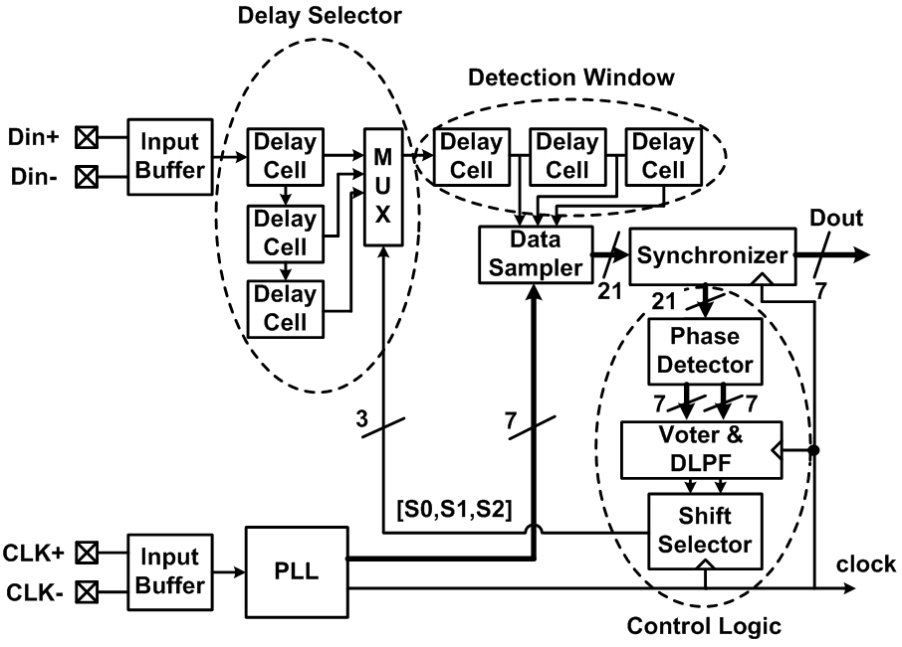


Fig. 3.20 Architecture of a “delay selecting” CDR

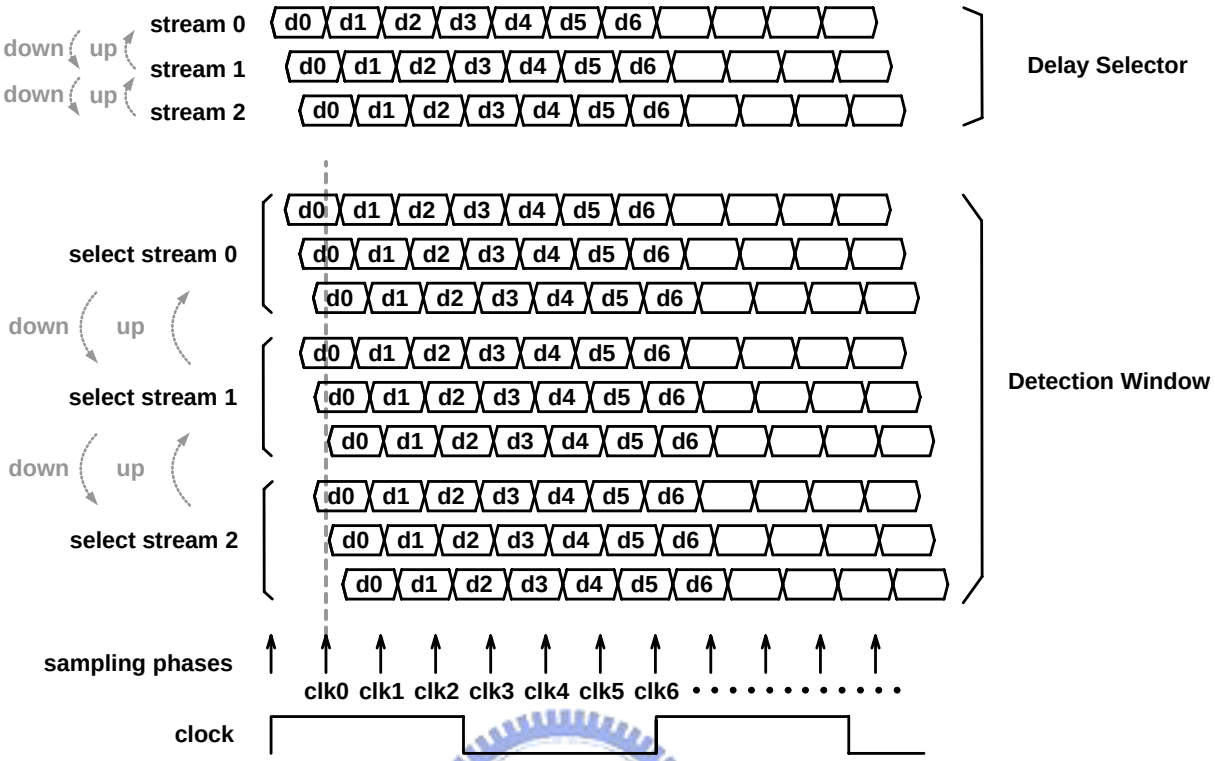


Fig. 3.21 Operation of the “delay selecting” CDR

Chapter 4

Building Blocks of Delay Selecting CDR

Fig. 3.20 shows the architecture of the delay selecting CDR. These building blocks of the delay selecting CDR would be presented in this chapter.

4.1 LVDS INPUT BUFFER

Fig. 4.1 shows a traditional design of a LVDS receiver buffer. The differential input signal is detected by the Schmitt trigger (M1 ~ M6 and M7 ~ M10), which translates the detected signal into the full swing output V_{out}. However, in this receiver buffer the lower bound of input signal common mode range is limited by M3 and M4. In IEEE LVDS standard the specificity of the LVDS levels at the receiver input are (4-1) and (4-2).

$$|V_{idth}| \geq 100mV \tag{4-1}$$

$$0mV \leq V_i \leq 2400mV \tag{4-2}$$

Thus, when the common mode voltage of input signal is close to 0mV, M1 and M2 in Fig. 4.1 would enter into the triode region to keep the V_{gs} of M4 and M5 over V_{th}. Because M1 and M2 operate in triode region, the voltage gain of this design in Fig. 4.1 would be significantly reduced.

To overcome this problem of input common mode range in Fig. 4.1, a new LVDS receiver buffer is reported [10]. Fig. 4.2 shows the new design. To solute the problem in traditional design, the new design is cascoded another buffer, first stage buffer, before the Schmitt trigger. The voltage gain of the first stage buffer is almost insensitive to the input

signal common mode voltage. Because the differential signal after the first stage is almost irrelevant to the input common mode voltage, the Schmitt trigger can be implemented in NMOS type, which has better frequency response the PMOS type. However, in reference [10] the new designed receiver input buffer is implemented in 3.3V devices. In the thesis the LVDS CDR is implemented in 0.13 μm 1.2V / 3.3V CMOS process. In order to translate the input signal from the 3.3V LVDS signal into a 1.2V full swing signal, the receiver input buffer in this thesis is implemented in 1.2V, Vddl, beside the current source supporting current to M1 and M2 is connect to 3.3V, Vddh, as shown in Fig. 4.3. Concerning in the problem of gate oxide reliability the first stage buffer M1 ~ M6 must designed in 3.3V device.

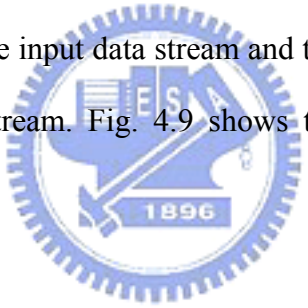
To receive a high speed input signal the frequency response of the receiver input buffer is important. If the receiver must receive a signal in 1.25 Gb/s, the frequency response bandwidth of the input buffer must higher than 625 MHz. To make sure the frequency response bandwidth is higher enough, the bias voltages V_{b1}, V_{b2} and impedance value of R_1 and R_2 is important. Fig. 4.4 shows the frequency response simulation result of the LVED receiver input buffer designed in this thesis.

4.2 DELAY SELECTOR

After input buffer input data signal is translated from 3.3V LVDS signal into full swing 1.2V digital serial data stream. This serial data stream would be send into the delay selector. Fig. 4.5 shows the architecture of delay selector. Delay selector is composed of three delay cells and one three to one MUX. By using these three delay cells the input serial data stream is delayed into three different time delayed data streams. One of these three different time delayed data streams would be selected according to the operational code send from the shift selector. Fig. 4.6 shows the circuit of the delay cell. Controlling bias voltage at V_{bp} and

V_{bn}, the pull up and pull down current of the delay cell would be changed. According to different pull current, the delay cell can make the input signal delayed in different time. To make sure each delay time is equal to a quarter data step, the delay cell is design in the same scale with the VCO cell in the PLL and the bias voltages V_{bp} and V_{bn} is also provide by the PLL.

The signals after delay cells are differential and not a full swing signal. To pull these signals into full swing single ended signal, a different to single ended converter is needed. Fig. 4.7 shows the different to single ended converter. Fig. 4.8 shows the simulation result of the delay cells and differential to single end converters. After delay cells and differential to single end converters, the send out signals, D0 ~ D2, are full swing data streams delayed in different phases respectively. The delay selector would select one of these three data stream to cancel the skew between the input data stream and the clock. A three to one MUX is used to select the correct data stream. Fig. 4.9 shows the schematic diagram of the three-to-one MUX.



4.3 DETECTION WINDOW AND DATA SAMPLER

After the delay selector the selected data stream would be send into the detection window. The detection window is composed of three delay cells, which is the same as that used in the delay selector. In the detection window the selected data stream would be delayed in different phases. After detection window these data stream delayed in different phases would be sampled by different sampling clock phases in data sampler as shown in Fig. 4.10. By sampling these delayed data streams the CDR can get the logic state of the input data stream at different moment. Fig. 4.11 shows the timing relation between sampled data streams, sampling clock phases, and sampling results.

4.4 SYNCHRONIZER AND CONTROL LOGIC

As shown in Fig. 4.11 the sampling results, D0 ~ D20, are asynchronous. To simplify the circuit after the sampler in this CDR a synchronizer is used to synchronize these sampling results. These synchronized data stream would be send into control logic. In control logic a phase detector is used to detect whether a skew happen in the detection window. Fig. 4.12 shows the schematic diagram of the phase detector and the truth table of the phase detector. If the input signal of the phase detector is “001” or “110” the phase detector would assume that in this detection window a translation edge happens in the data stream behind the center sampling clock phase and sends out a “down” signal to ask the delay time of the selected data stream lag a quarter step time in next clock period. On the contrary, if the input signal of the phase detector is “100” or “011” the phase detector would assume that in this detection window a translation edge happens in the data stream before the center sampling clock phase and sends out a “up” signal to ask the delay time of the selected data stream lead a quarter step time in next clock period.

Besides the skews between data stream and the clock signal the jitter in data stream would make the phase detector send out “up” or “down” signal too. As the result, this requirement sent out by the phase detector would not be accepted immediately and a voter and a DLPF (digital low pass filter) are used to analysis these “up” and “down” signals and verify that a skew between the data stream and the clock signal really happens.

Because there are seven data be serialized into the input data stream during each clock period, the CDR need seven phase detectors to detect whether any translation edge happen in each data step. In another word, there would be seven detection results sent out in each clock period. If a skew really happen between the data stream and the clock these seven detection results should be the same or no detection result, no edge happen in this data step. However, the fitter in the data stream would make some wrong detection result as shown in

Fig. 4.13. To avoid the wrong shifting on delay time the voter is designed to make sure the requiring signals “up” or “down” are two more than the opposite requiring signals “down” or “up”. Fig. 4.14 shows the schematic diagram of the voter for “up” signals. When up requiring signals are more than down requiring signals, turn on NMOSs are more than turn on PMOSs and the bias voltage at node N1 would be lower than the threshold voltage of the inverter and the output “up” signal would be pulled high. On the other hand, when up requiring signals are less than down requiring signals, turn on NMOSs are less than turn on PMOSs and the bias voltage at node N1 would be higher than the threshold voltage of the inverter and the output “up” signal would be pulled low. An extra PMOS, M_{pex}, is added before the inverter. The M_{pex} is always turned on to make sure the output “up” signal wouldn’t be pulled high when up requiring signals are just one more than down requiring signals.

After the “up” or “down” requirement passes the voter the shifting requirement would still not be accepted immediately. To avoid the wrong requirement induce by jitters more completely the “up” or “down” requirement must pass another test circuit, a DLPF (digital low pass filter). DLPF is a finite state machine. Fig. 4.15 shows the state diagram of the DLPF. The output “UP” would be pulled high only when the up requiring keeps in high over three clock periods.

The shifting requirement “UP” or “DOWN” from the DLPF would be sent into the shift selector. Fig. 4.16 shows the schematic diagram of the shift selector. When the “UP” signal is high, in next clock period the value of S_n would become the value of the S_{n-1} in this clock period. When the “DOWN” signal is high, in next clock period the value of S_n would become the value of the S_{n+1} in this clock period. Fig. 4.17 shows the shift selector and the delay selector. “S_0, S_1, and S_2” are the output selecting signals of the shift selector, and “S_0, S_1, and S_2” would always be reset as “1, 0, and 0 ” as the beginning. Thus, there are always only one “1” signal in these selecting signals “S_0, S_1, and S_2”. According to the shift

requirement signal “UP” or “DOWN” the “1” signal would shift up or down in “S_0, S_1, and S_2”. The location of the “1” signal in “S_0, S_1, and S_2” decides which delayed data stream in the delay selector is selected to be sampled. If a “UP” requirement were accepted the delayed time of the selected data stream would be increase one phase time in next clock period. If a “DOWN” requirement were accepted the delayed time of the selected data stream would be decrease one phase time in next clock period. The motion of shifting delay time would occur until the sampling edge locates away the data translating edge and no more shift requirement signal “UP” or “DOWN” happens.

4.5 PHASE LOCK LOOP (PLL)

Fig. 4.18 shows the architecture of the designed PLL [12]. A PLL is basically an oscillator, which can provide clocks in different phase. As the name, phase lock loop, one of these clocks provided by PLL can be locked to the input clock with the same phase and frequency. A negative feedback loop is used in PLL as shown in Fig. 4.18. The PLL is composed of a PFD (phase frequency detector), a charge pump, a loop filter, a VCO (voltage-controlled oscillator), and a differential-to-single-ended conversion circuit. The PFD is used to detect the phase/frequency different between the input clock and the output clock. The charge pump is used to charge or discharge the capacitance of the loop filter according to the output signal of the PFD. The bias generator provides two property bias voltages, V_{bp} and V_{bn}, which is depend on the output voltage of the loop filter, V_{ctrl}. V_{bp} and V_{bn} would be sent into the VCO, and these output clocks of the VCO would change their phase/frequency according to the voltage of V_{bp} and V_{bn} until there is no phase delay between the input clock and the output clock of the VCO. Following is the detail description of each circuit block in the designed PLL.

4.5.1 Phase Frequency Detector

Fig. 4.19 shows the schematic diagram of the phase frequency detector. PFD is used to detect the phase error between the input clock and the feedback clock. The TSPC-DFF would pull output signal high when the rise edge happen in the input signal. If the rise edge in the input clock happens before the rise edge in the feedback clock, the "up" signal would be pulled high until the rise edge in the feedback clock happens and trigger the reset signal reset these two TSPC-DFF. On the other hand, if the rise edge in the feedback clock happens before the rise edge in the input clock, the "down" signal would be pulled high until the rise edge in the input clock happens and trigger the reset signal reset these two TSPC-DFF. Thus, when the phase error between the input clock and feedback clock happens, the PFD would send out a pulse signal "up" or "down" and the length of the pulse signal is depend on the distance of the phase difference between the input clock and feedback clock. Ideally, the PFD should have the ability to distinguish any phase error between the input clock and the feedback clock. In practical, when the phase error is too small, the reset signal is so fast that the following charge pump circuit will not be activated and that will result in dead zone, undetectable phase difference range. To eliminate the dead zone a delay buffer is added in the reset path.

4.5.2 Charge Pump and Loop Filter

Fig. 4.20 shows the schematic diagram of the charge pump [12]. The charge pump is used to charge or discharge the loop filter to control the center frequency of the VCO according to the "up" and "down" signals from the PFD. A second-order on-chip loop filter is designed to suppress the reference [13]. As shown in Fig. 4.21 the loop filter is composed of a resistor R_1, a capacitor C_1 and a capacitor C_2. The loop filter provides a pole in the original to provide an infinite DC gain to get the zero static phase error, and a zero in the open loop response in order to improve the phase margin to ensure overall stability of the

loop. C_2 is used to provide higher-order roll off for reducing the ripple noise to mitigate frequency jump. However, C_2 would also make the overall PLL system become third-order one and affect the stability of the loop. In general case, the loop filter would be set as $C_1 > 20 \times C_2$ and the third-order loop can be approximated to second-order loop. The total transfer function of the loop filter can be expressed as the equation (4-1).

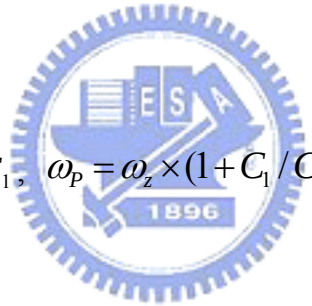
$$F(s) = \frac{1}{C_1 + C_2} \frac{sR_1C_1 + 1}{s\left[(sR_1C_1C_2 / C_1 + C_2) + 1\right]} \tag{4-1}$$

and hence

$$F(s) = \frac{K \times (s + \omega_z)}{s \times (1 + s / \omega_p)}$$

where

$$\omega_z = 1 / R_1C_1,\ \omega_P = \omega_z \times (1 + C_1 / C_2),\ K = \frac{R_1 \times C_1}{C_1 + C_2}$$



4.5.3 Bias Generator

Fig. 4.22 shows the schematic diagram of the bias generator [12]. The bias generator provides two output bias voltages, V_{bn} and V_{bp}, according to the input voltage V_{ctrl}. These two output bias voltages, V_{bn} and V_{bp}, are used to adjust the bias current of the VCD delay cells and control the frequency of the feed back clock generated by the VCO. The bias generator is composed of a differential amplifier, a half-buffer replica and a control voltage buffer. The differential amplifier is a unity-gain buffer, which is used to force the voltage of nod n1 in Fig. 4.22 equal to V_{ctrl}. Besides, the bias voltage V_{bn} is also dynamically adjusted by the differential amplifier to increase the supply noise immunity. When the supply voltage

changes the differential amplifier would adjust these two bias voltages and keep the bias current in the VCO constant. Because the differential amplifier is self-biased, the star-up circuit is needed.

Because the differential amplifier and the half-buffer replica form a negative feedback loop, the frequency response issue of the feedback loop must be considered. In general cases, in order to track the supply and substrate noise, which would affect the VCO jitter performance, the bandwidth of the feedback loop circuit would usually be set the same as the operation frequency of the VCO. The control voltage buffer is used to isolate the control voltage, V_{ctrl}, from capacitive coupling in the VCO delay cells.

4.5.4 VCO and Differential-to-Single-Ended Converter

Fig. 4.23 shows the schematic diagram of the VCO. The designed VCO is a 14 stages oscillator, which can provide 28 different clock phases. Seven of these 28 different clock phases would be sent out for the data sampler to sample the input data stream. The designed VCO cells, which were presented in reference [12], have low sensitivity and high noise rejection capability of the supply and substrate voltage. As the result, the output clocks of the VCO composed of these VCO cells has low jitter characteristic. However the output signal of the VCO cell is a low swing and differential signal, which can't be used in the data sampler. To solute this problem, a differential-to-single-ended converter is needed. Fig. 4.24 shows the schematic diagram of the differential-to-single-ended converter. It is composed of two opposite phase NMOS differential amplifiers driving two PMOS common-source amplifiers connected by an NMOS current mirror. Because the two NMOS differential amplifiers use a NMOS current source the same as that used in the VCO cells, the converter can receive the correct common-mode input voltage level. These output signals of the differential-to-single-ended converter is full swing digital signals and can be used to sample the input data stream in the data sampler.

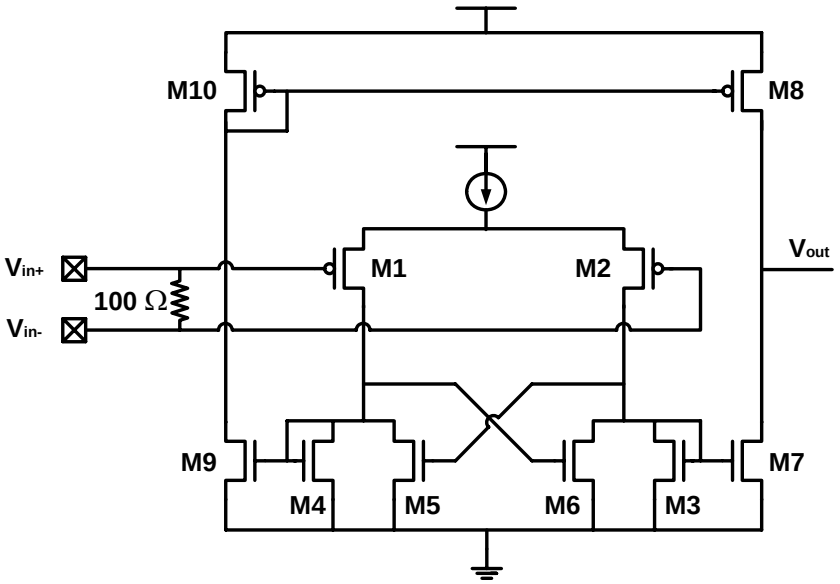


Fig. 4.1 Traditional LVDS input buffer

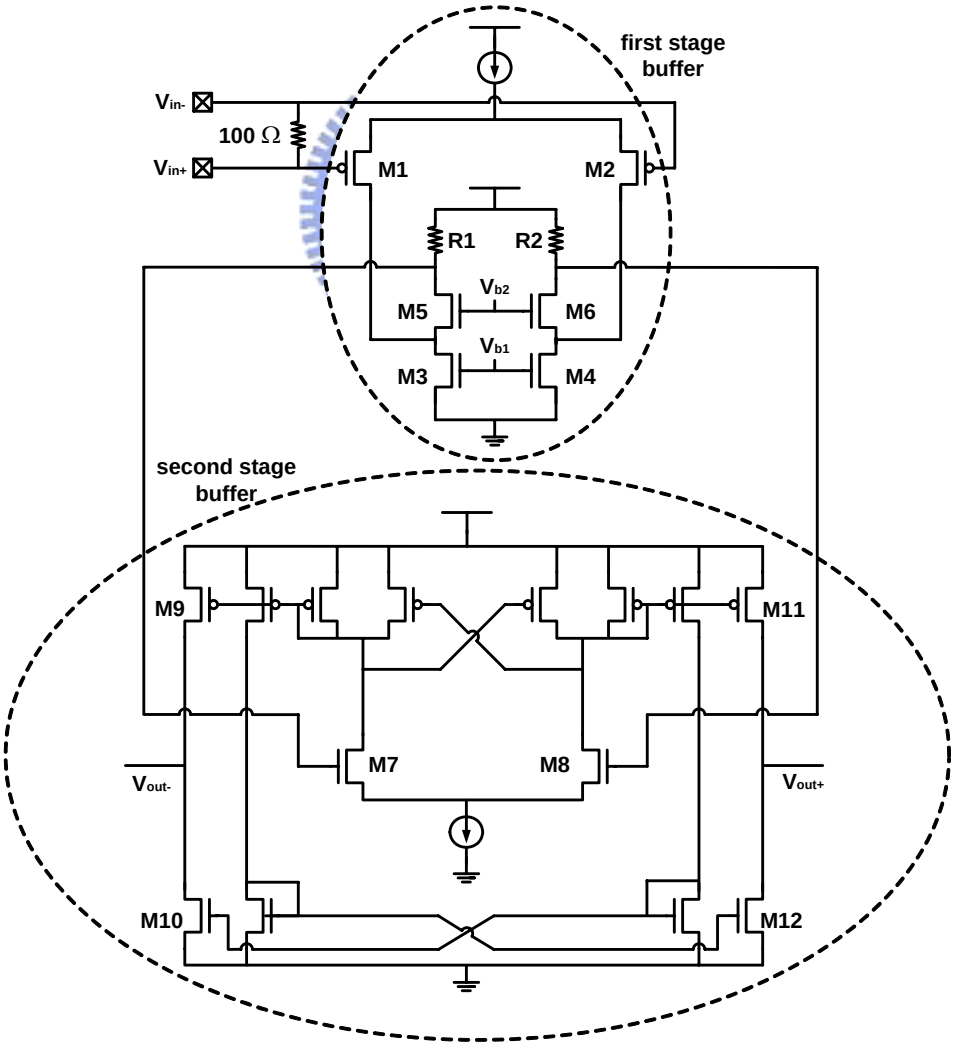


Fig. 4.2 New design of LVDS receiver input buffer

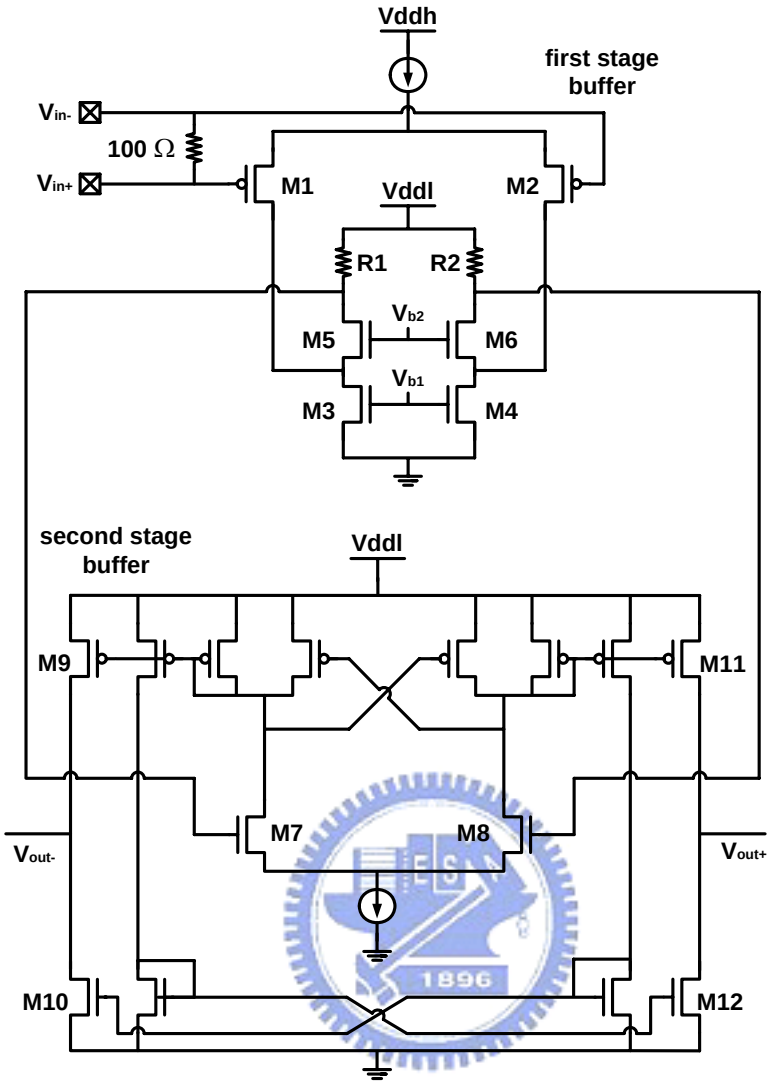


Fig. 4.3 LVDS receiver input buffer in this thesis

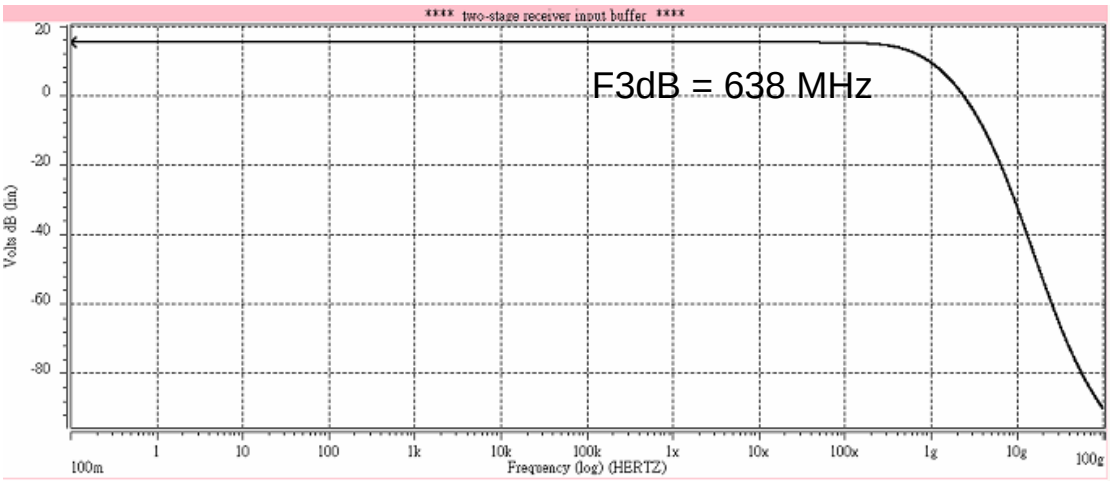


Fig. 4.4 Simulated frequency response of the LVDS receiver input buffer (Fig. 4.3)

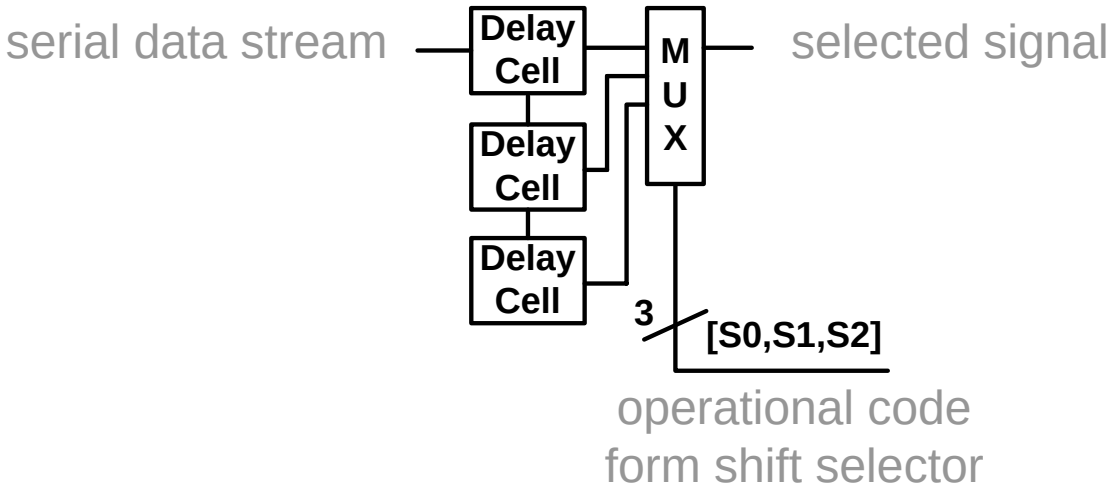


Fig. 4.5 Architecture of the delay selector

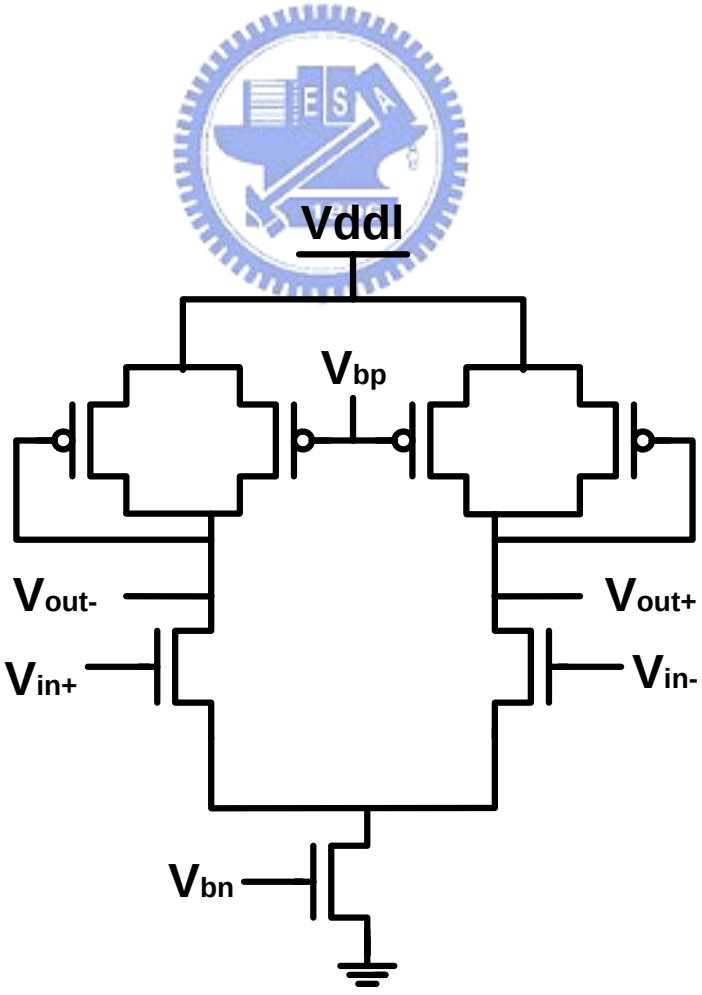


Fig. 4.6 Schematic diagram of the delay cell

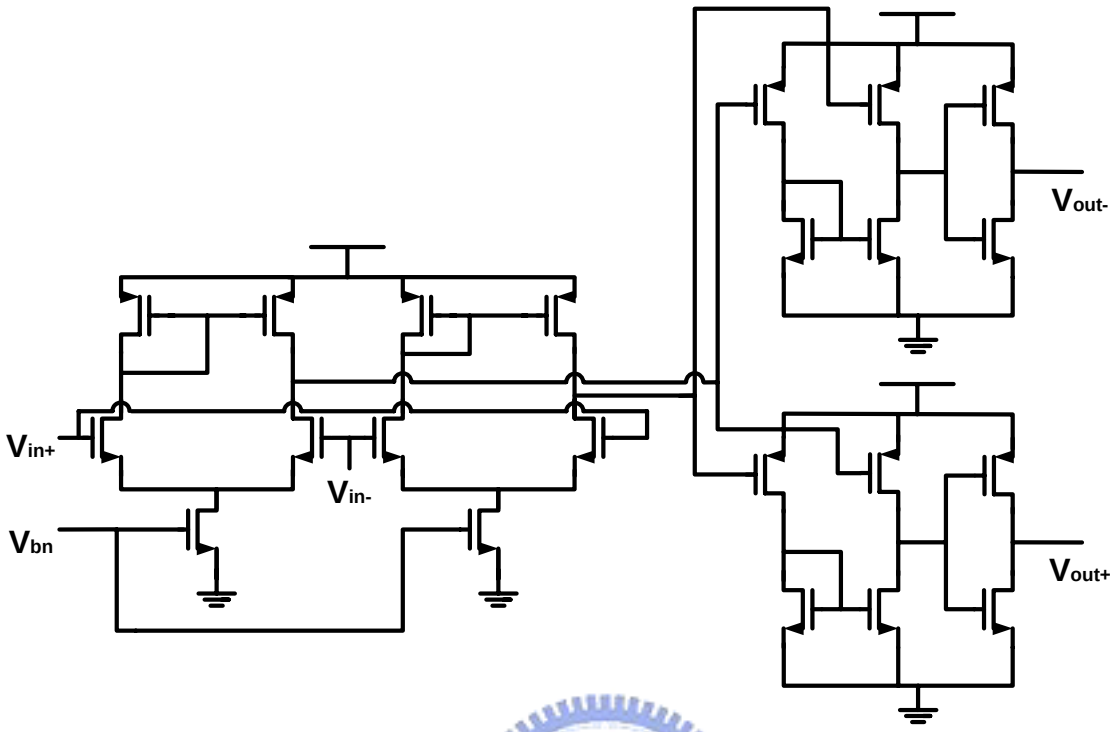


Fig. 4.7 Schematic diagram of the differential to single ended converter

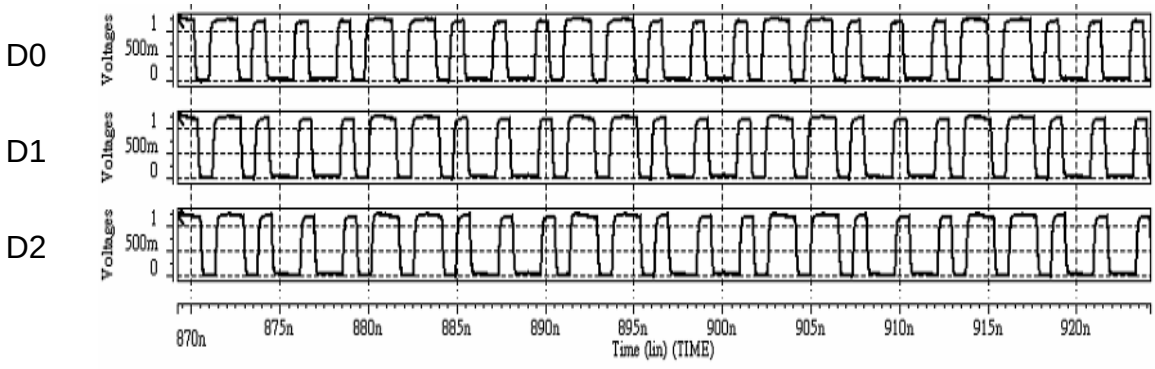


Fig. 4.8 Simulation result of the delay cells and

differential to the single ended converters

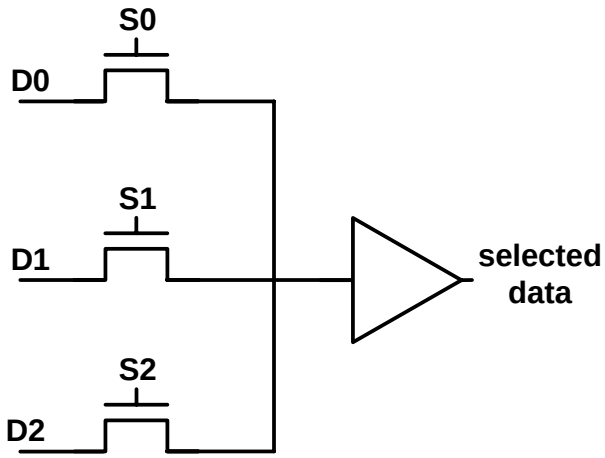


Fig. 4.9 Schematic diagram of the three to one MUX

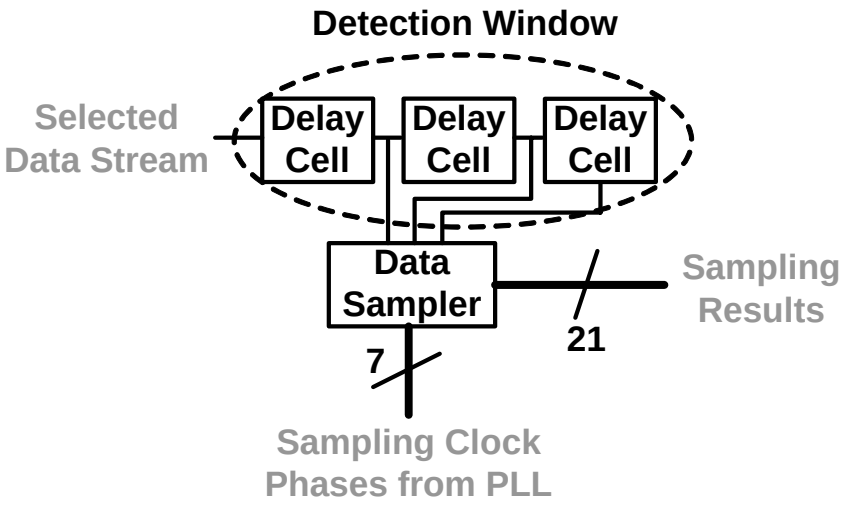


Fig. 4.10 Detection window and data sampler

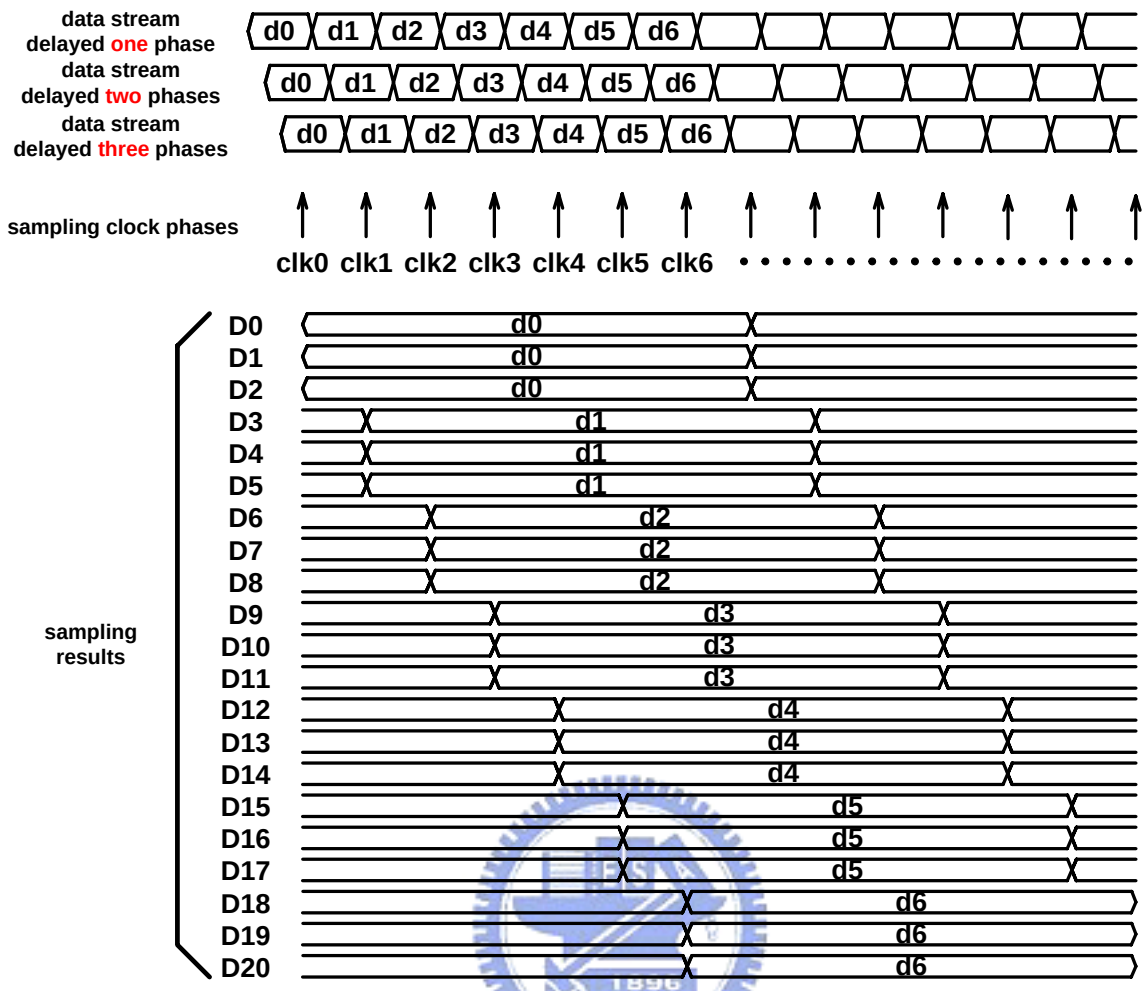
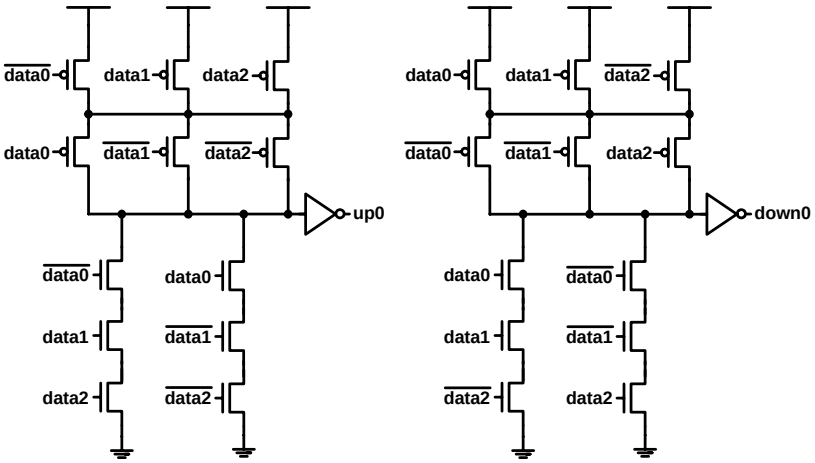


Fig. 4.11 Operation timing of the data sampler



data0	data1	data2	up0	down0
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	0	0

Fig. 4.12 Schematic diagram and truth table of the phase detector

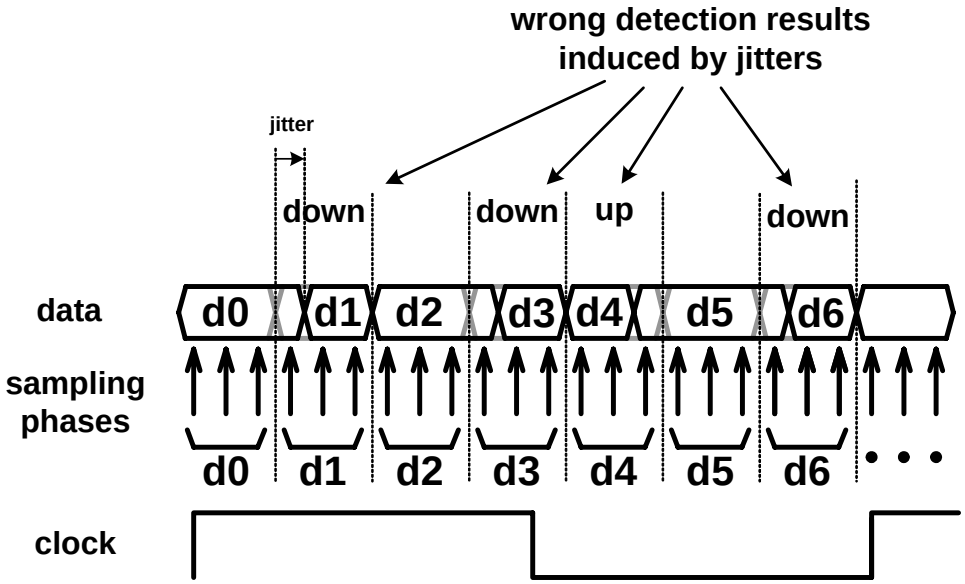


Fig. 4.13 Wrong detection results induced by jitters

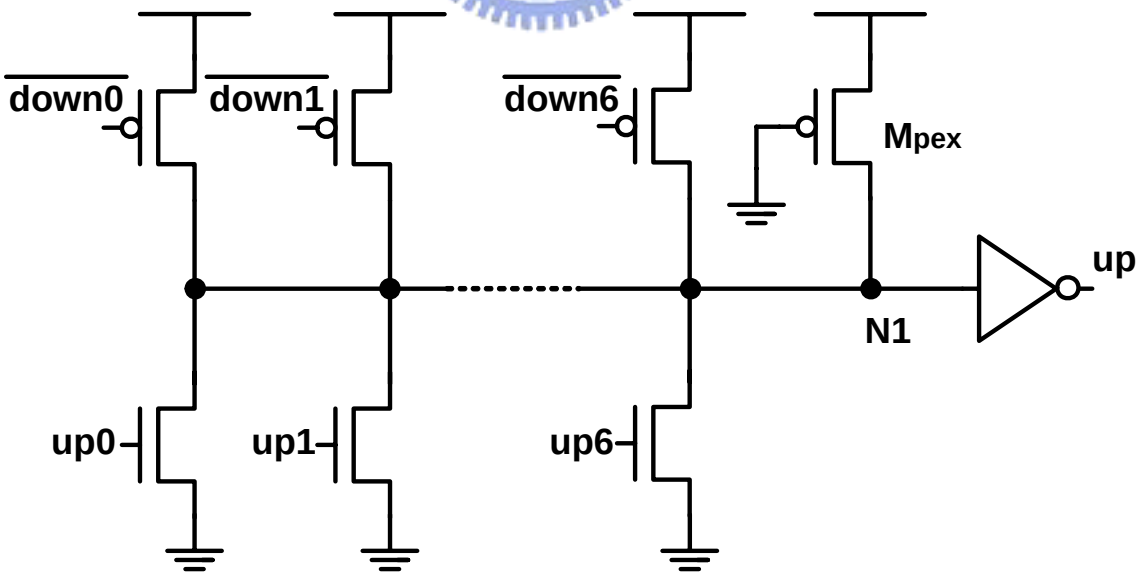


Fig. 4.14 Schematic diagram of the voter

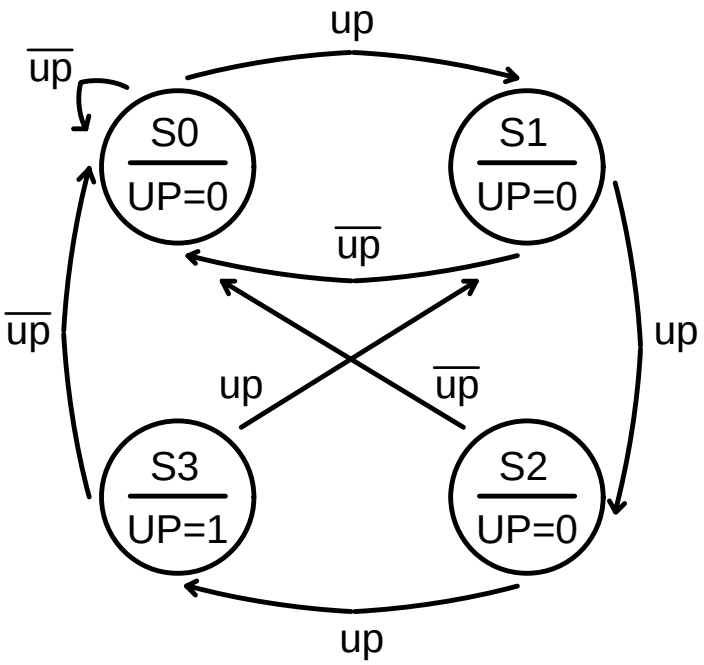


Fig. 4.15 State diagram of DLPF

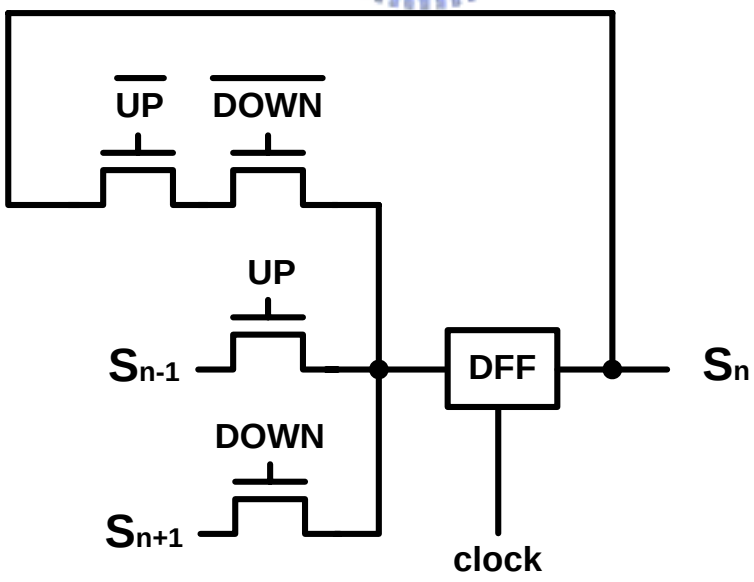


Fig. 4.16 Schematic diagram of the shift selector

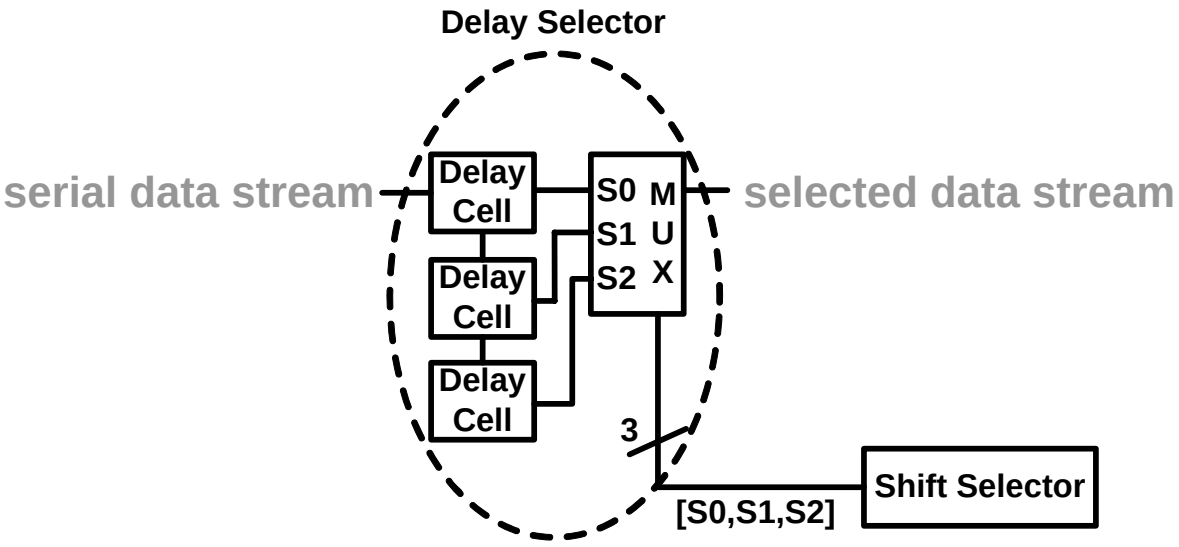


Fig. 4.17 Sifter selector and delay selector

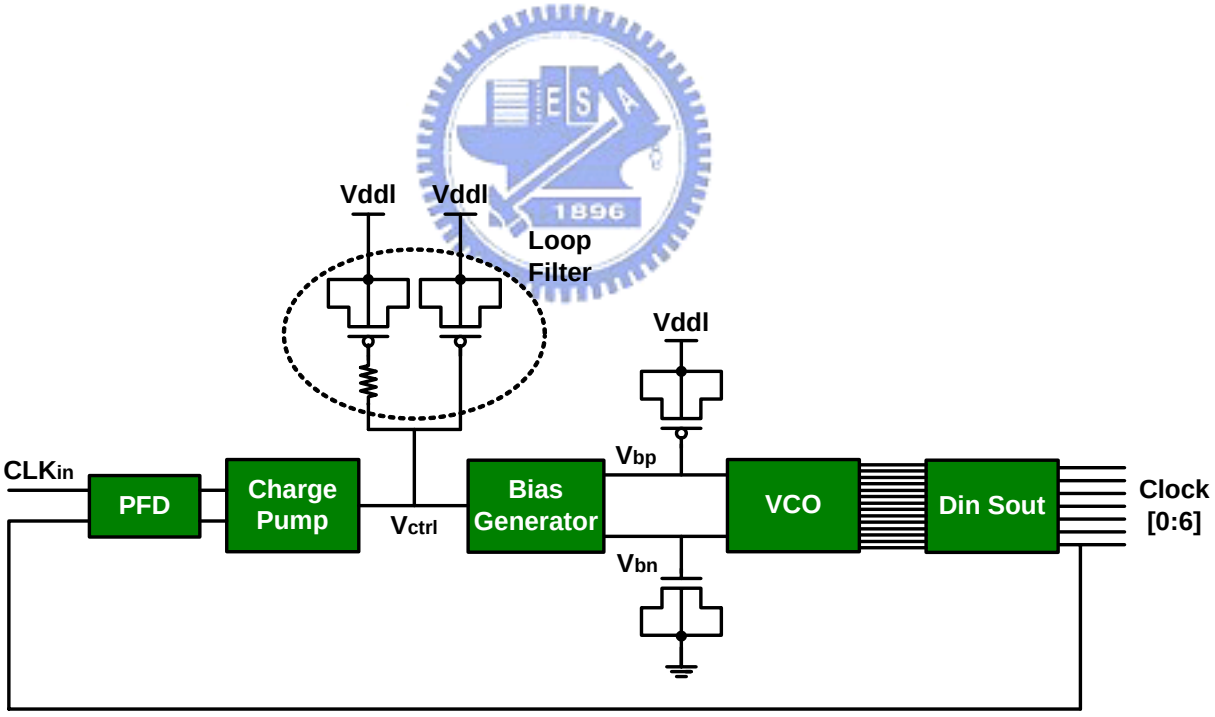


Fig. 4.18 Architecture of the designed PLL

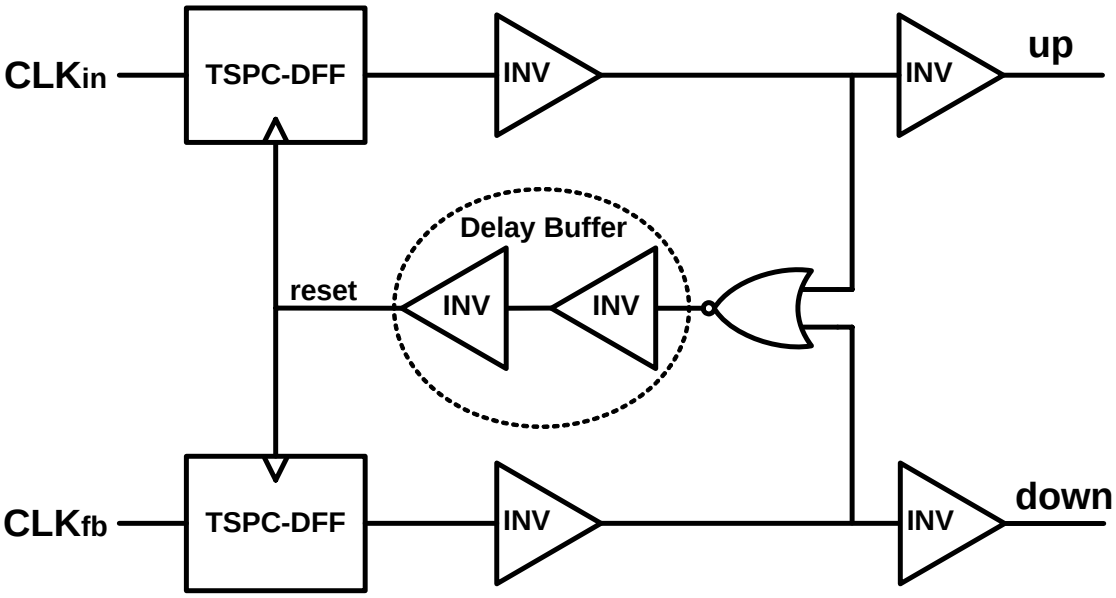


Fig. 4.19 Schematic diagram of the PFD

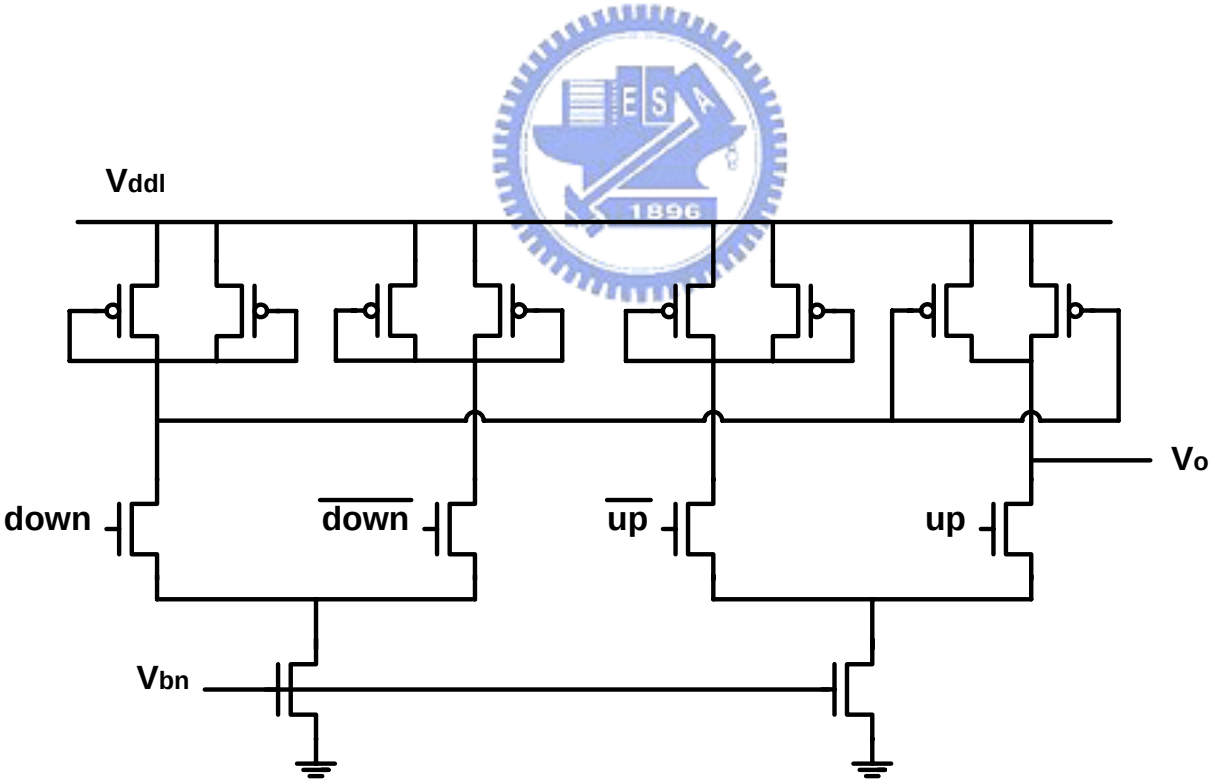


Fig. 4.20 Schematic diagram of the charge pump

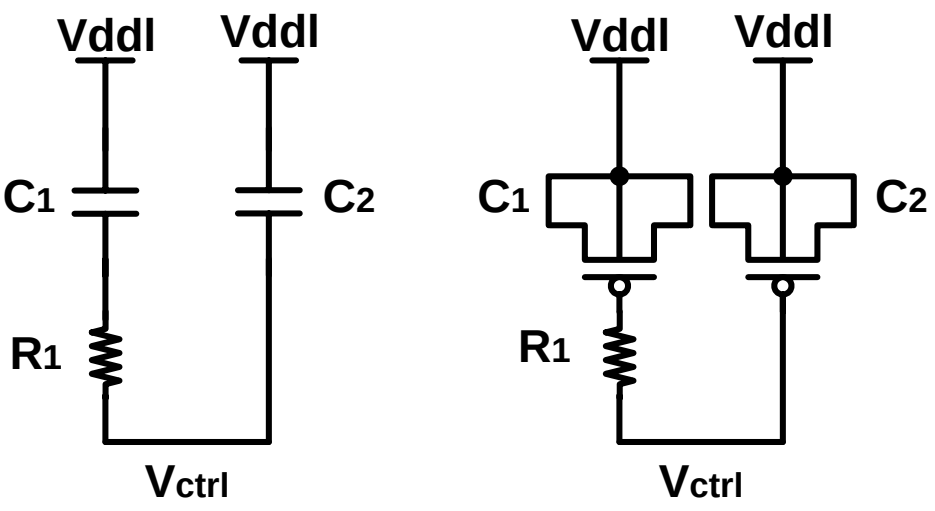


Fig. 4.21 Schematic diagram of the loop filter

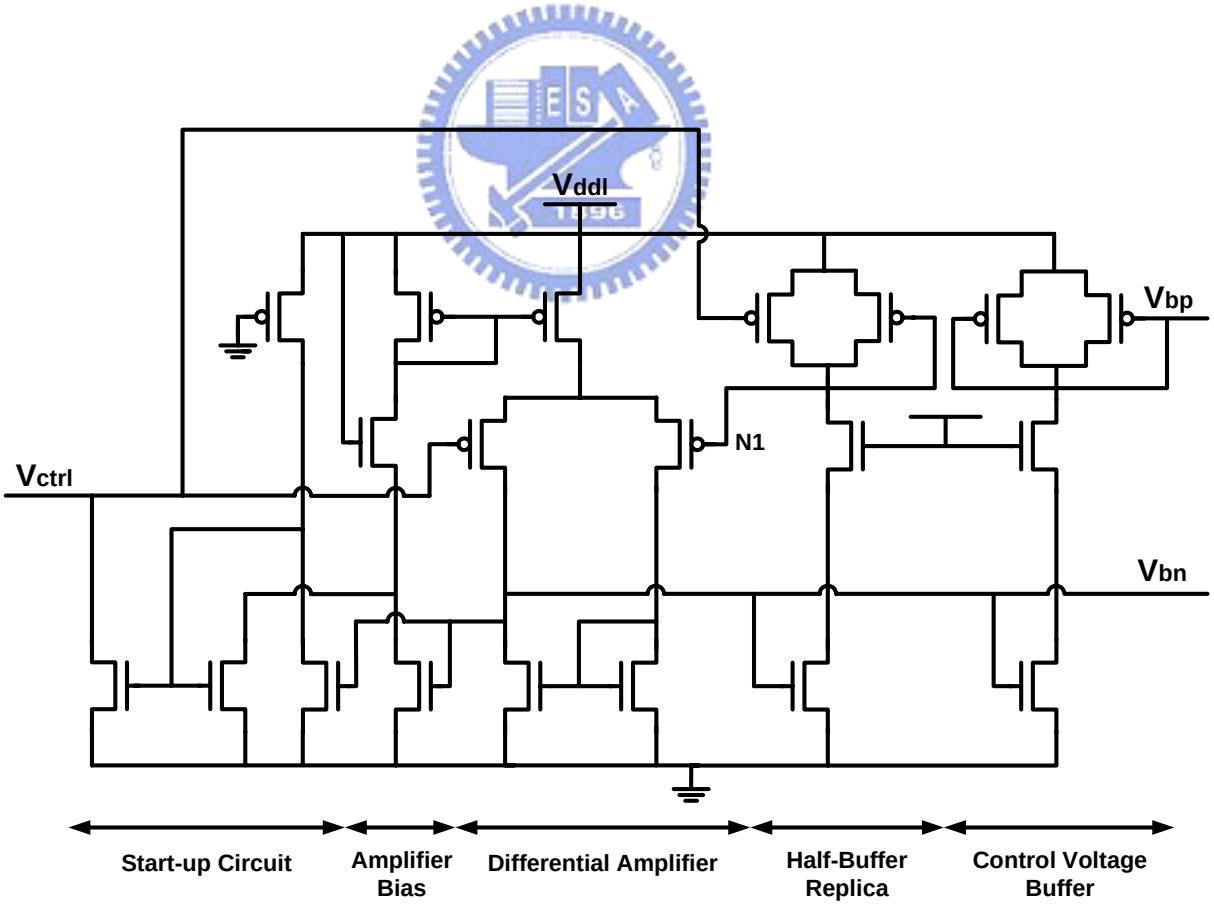


Fig. 4.22 Schematic diagram of the bias generator

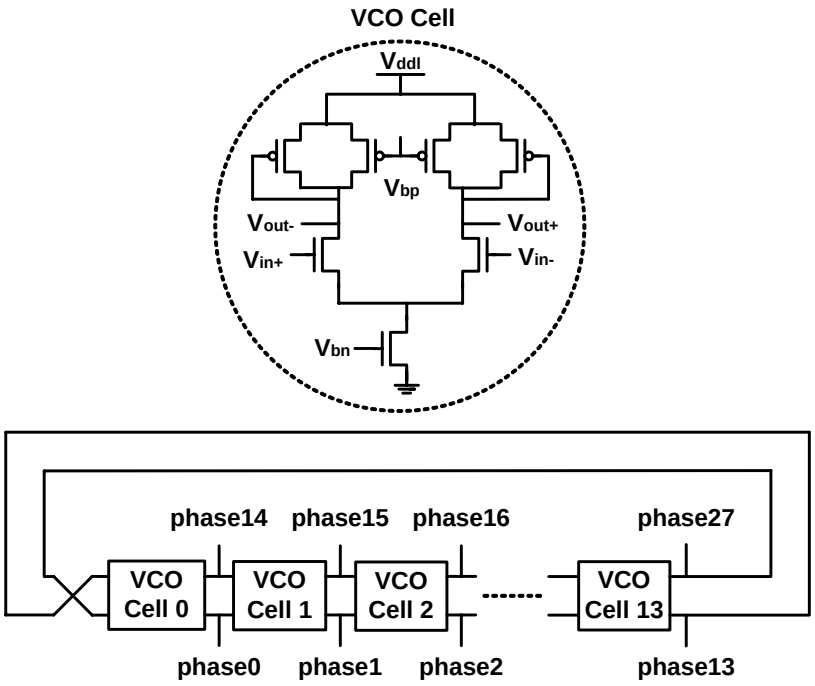


Fig. 4.23 Schematic diagram of the VCO

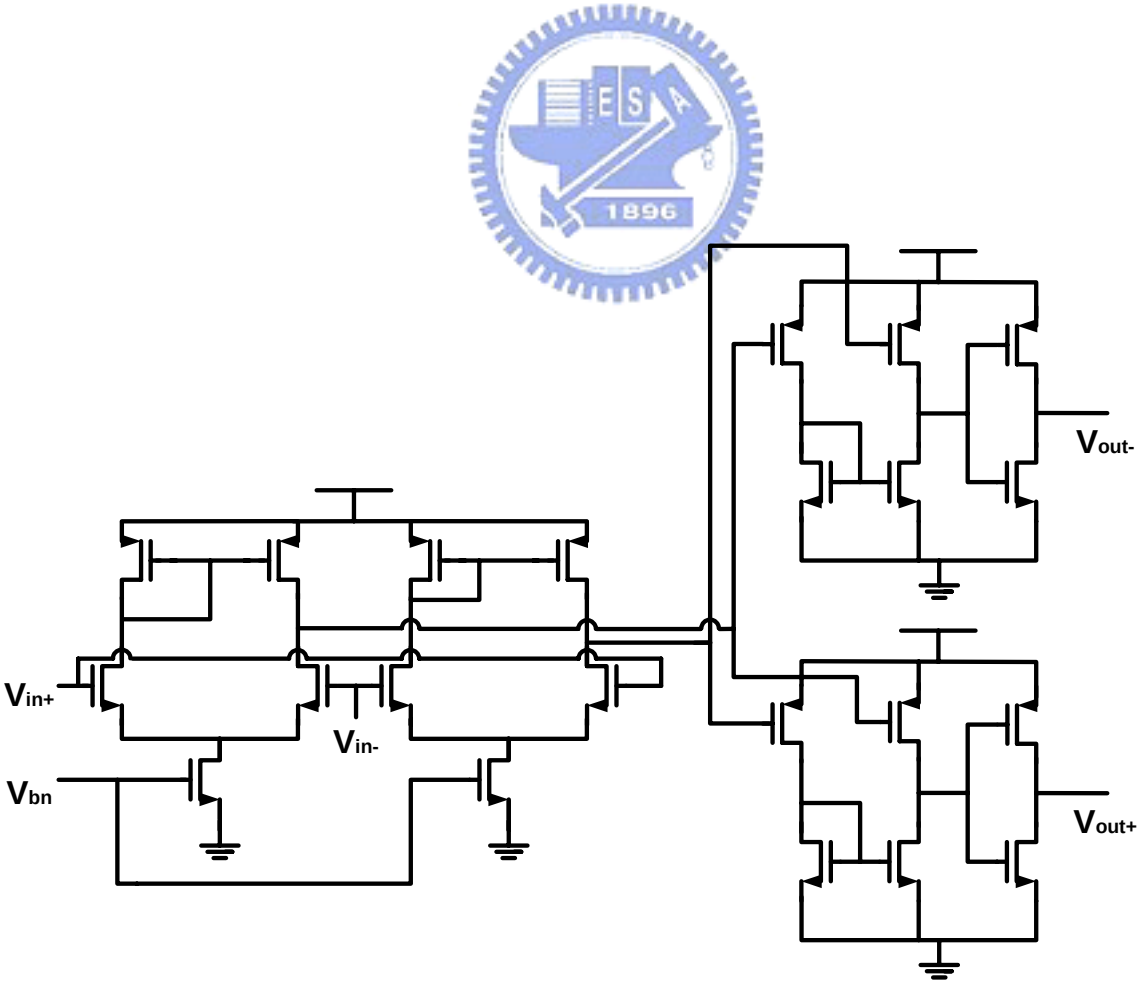


Fig. 4.24 Schematic diagram of the differential-to-single-ended converter

Chapter 5

Experiment Results

Fig. 5.1 shows the layout and the die photo of the LVDS data recovery receiver fabricated in a 0.13-μm 1P8M CMOS process with 3.3V and 1.2V power supply. In the die photo Fig. 5.1(b) because the polymer layer can't see the circuit under the polymer layer. In the tap out test chip there are two test circuits, serial output test circuit and parallel output test circuit. Fig. 5.2 shows the block diagram of the serial output test circuit in the tap out test chip. To simplify the process of testing whether the LVDS receiver recovers input data stream correctly or not, some test circuits are added in the test circuit. To reduce the channels must be observed, a serializer is used to serialize these recovered parallel data. Because the serial recovered data is a high data rate data stream, a LVDS output buffer is needed to drive this high-speed data stream.

In the test process a known pattern is sent into the test chip and by observe the output data of the test circuit it can be verify that whether the LVDS receiver recovers input data stream correctly or not. If the LVDS receiver can actually recover the input data correctly the output data stream would be the same as the input pattern, or the output data stream would be different from the input pattern. Fig. 5.3 shows the measurement environment setting of the test for the serial output test circuit. The known differential data pattern and differential clock signals generated by the pulse pattern generator are sent into the test chip, and the output data stream is observed from the infiniium oscilloscope. Fig. 5.4 shows the top view of the serial output testing PCB photo and Fig. 5.5 shows the bottom view. In the testing of the serial output test circuit, besides a cyclic "010101" pattern, in this thesis a cyclic "1001001 0110110" pattern is also used to test the function of the test chip too. Fig. 5.6 ~ Fig. 5.9 show the test result when the cyclic "010101" pattern is sent into the test chip

at a data rate up to 1.1 Gb/s, 1.25 Gb/s, 1.8 Gb/s and 2 Gb/s respectively. When the data rate is 1.1 Gb/s, 1.25 Gb/s and 1.8 Gb/s the output data are all the same as the input pattern but when the data rate is up to 2 Gb/s there are some errors happen in the output data stream as shown in Fig. 5.9. Fig. 5.10 ~ Fig. 5.13 show the test result when the cyclic "1001001 0110110" pattern is sent into the test chip at a data rate up to 1.1 Gb/s, 1.25 Gb/s, 1.8 Gb/s and 2 Gb/s respectively. The same as the cyclic "010101" pattern, when the data rate is up to 1.1 Gb/s, 1.25 Gb/s and 1.8 Gb/s the output data are all the same as the input pattern but when the data rate is up to 2 Gb/s there are some errors happen in the output data stream as shown in Fig. 5.13. As the result, the upper boundary of the data rate that the LVDS receiver can recovers the input data correctly is 2 Gb/s and the lower boundary is 1.1 Gb/s.

Fig. 5.14 shows the block diagram of the parallel output test circuit in the tap out test chip. Because the data rate of the recovered parallel data is the same as the clock frequency, taper buffers are able to drive these recovered parallel data streams. Fig. 5.15 shows the measurement environment setting of the test for the parallel output test circuit. Fig. 5.16 shows the top view of the parallel output testing PCB photo and Fig. 5.17 shows the bottom view. In the testing, set a pattern lets the recovered data stream D0 is a cyclic "01" signal, and lets recovered data streams D1 and D6 are cyclic "0011" signals as shown in Fig. 5.18. By observing recovered data streams D0, D1, D6 and recovered clock from the infiniium oscilloscope, it can be tested whether the LVDS receiver recovers input data streams correctly or not. By setting different delay time between data and clock, the skew tolerance of the LVDS receiver can be verified. If the positive or negative delay time is over the skew tolerance, the LVDS receiver would fail to recover data. As shown in Fig. 5.19(a), if the positive delay time is over the skew tolerance the recovered D0 would become a cyclic "0011" signal and the D1 would become a cyclic "01" signal. If the negative delay time is over the skew tolerance the recovered D0 would become a cyclic "0011" signal and the D6 would become a cyclic "01" signal as shown in Fig. 5.19(b). Fig. 5.20 ~ Fig. 5.24 show the

testing result when setting the pulse pattern generator make a 0 ps, 100 ps, 150 ps, –600 ps and –650 ps skew between the input data and input clock respectively at 1.25 Gb/s data rate. When the skew is between –600 ps and 100 ps the recovered data is correct D0 is a cyclic "0101" signal and D1 and D6 are cyclic "00110011" signals. When the skew is –650 ps and 150 ps the recovered data is wrong. A reasonable assuming that a 200 ps skew between the input data and input clock on chip already exists when the pulse pattern generator set no skew happen. As the result, it is accepted that the skew tolerance of this LVDS receiver is more than ± 300 ps which is ± 37.5 % of the data step, 800 ps.

Fig. 5.25 shows the measurement environment setup of the LVDS Link test. Using the pulse generator provide a reference clock for the LVDS transmitter, the LVDS transmitter can serialize the on chip PRBS signals and send out the serial data stream in LVDS level. The LVDS receiver receives the serial LVDS data stream and recovers these data into parallel full swing signals. Fig. 5.26 ~ Fig. 5.28 show the measurement result observing recovered clock and recovered data stream, D6, from the oscilloscope when the input data rate is 1.15 Gb/s, 1.4 Gb/s and 1.75 Gb/s respectively. Table 5.1 is the summary of the measurement result.

Table 5.1 Measurement result summary

Symbol	Parameter	Conditions	Min	Max	Units
V_{cm}	Input common mode voltage	V_d = 400 mV	0	1270	mV
V_d	Input differential voltage	V_{cm} = 1 V	150	—	mV
f_{clk}	Input clock frequency	V_{cm} = 1 V and V_d = 400 mV	165	250	MHz
DR	Input data rate	V_{cm} = 1 V and V_d = 400 mV	1.11	1.8	Gb/s
t_{skew}	Skew tolerance between input signals	DR = 1.25 Gb/s	–350	350	ps
P	Power consumption	DR = 1.25 Gb/s	—	39.7	mW

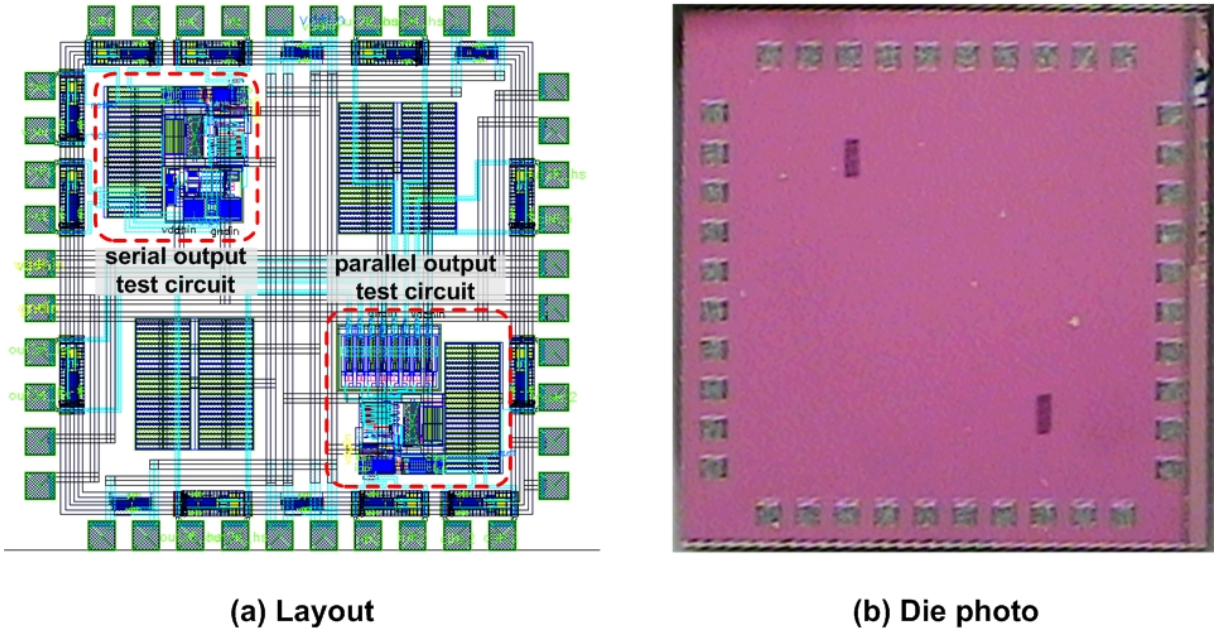


Fig. 5.1 Layout and die photo of the tap out test chip

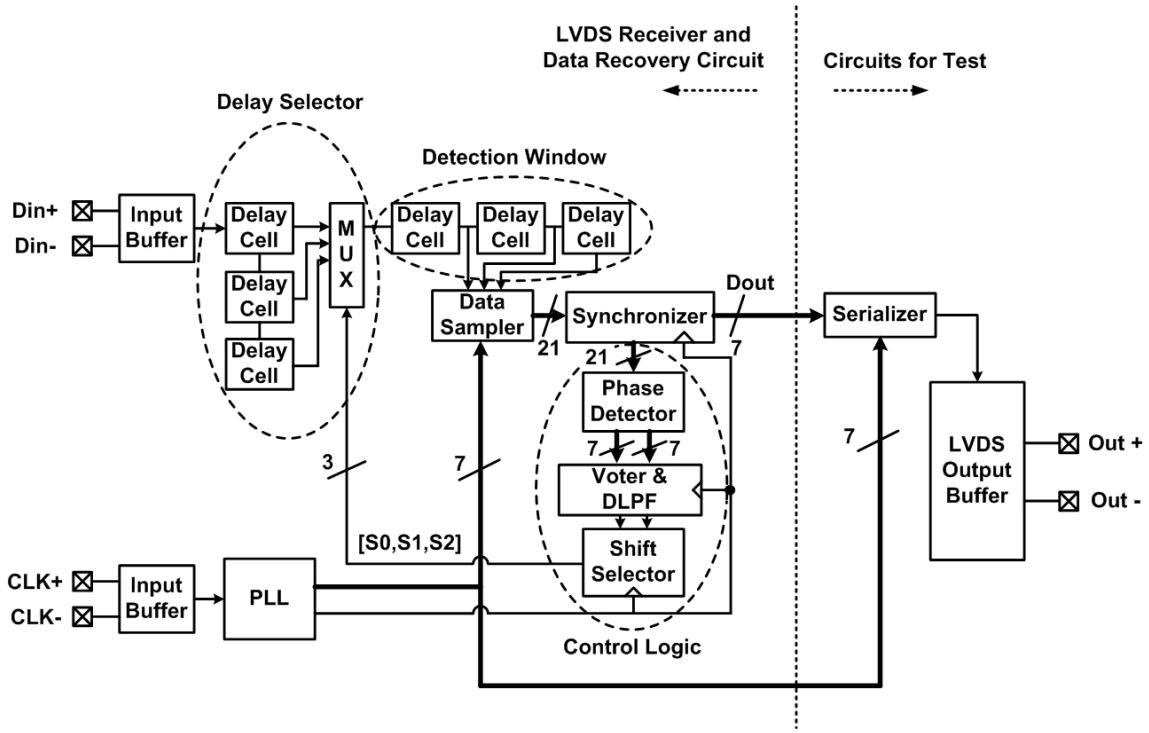


Fig. 5.2 Block diagrams of the serial output test circuit in the tap out test chip

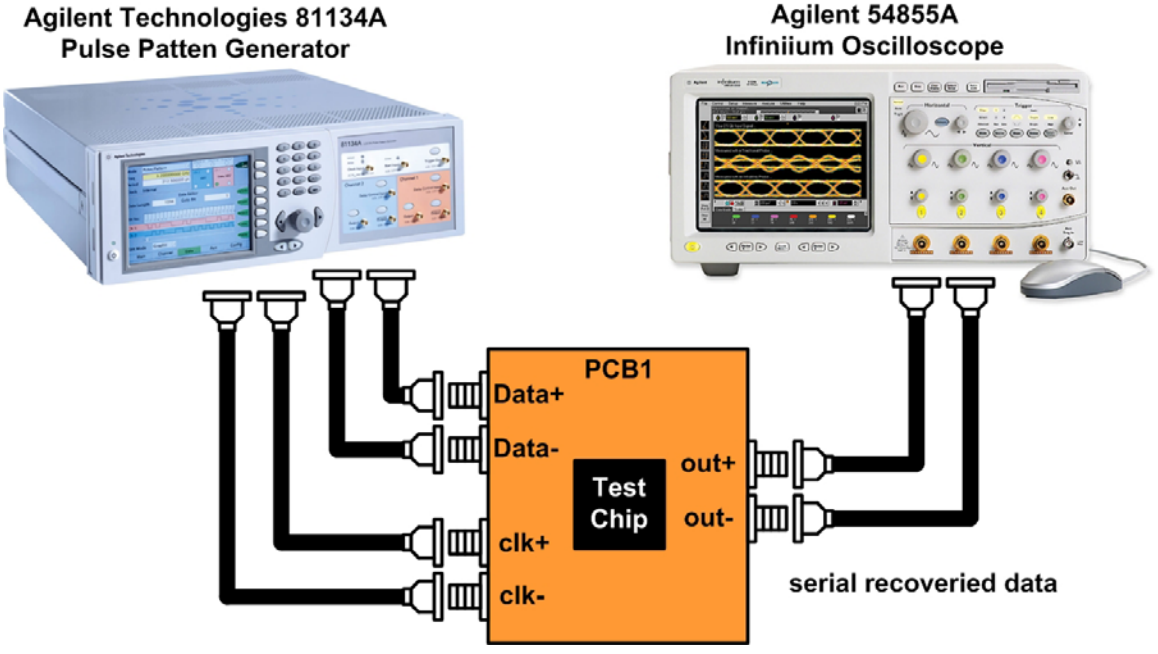


Fig. 5.3 Measurement environment setting of the serial output test

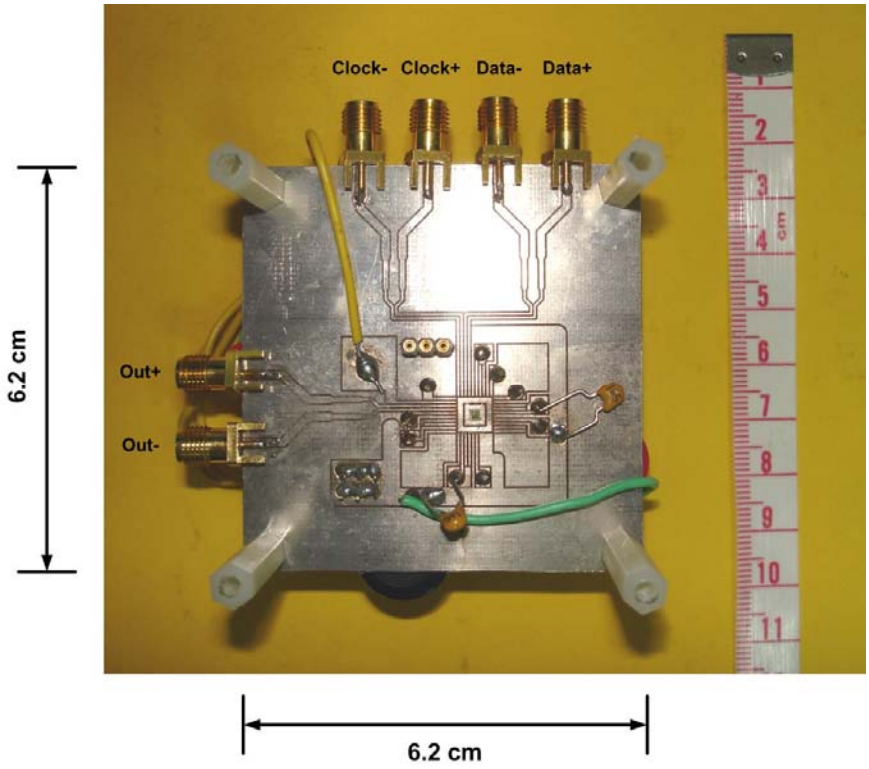


Fig. 5.4 Top view of the serial output testing PCB photo

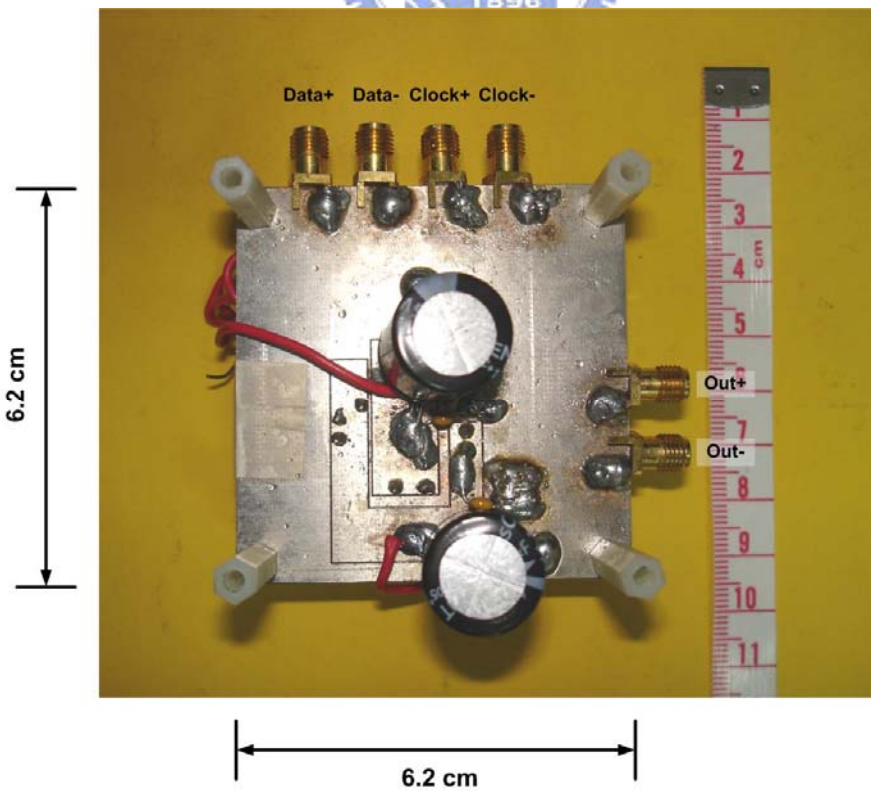


Fig. 5.5 Bottom view of the serial output testing PCB photo

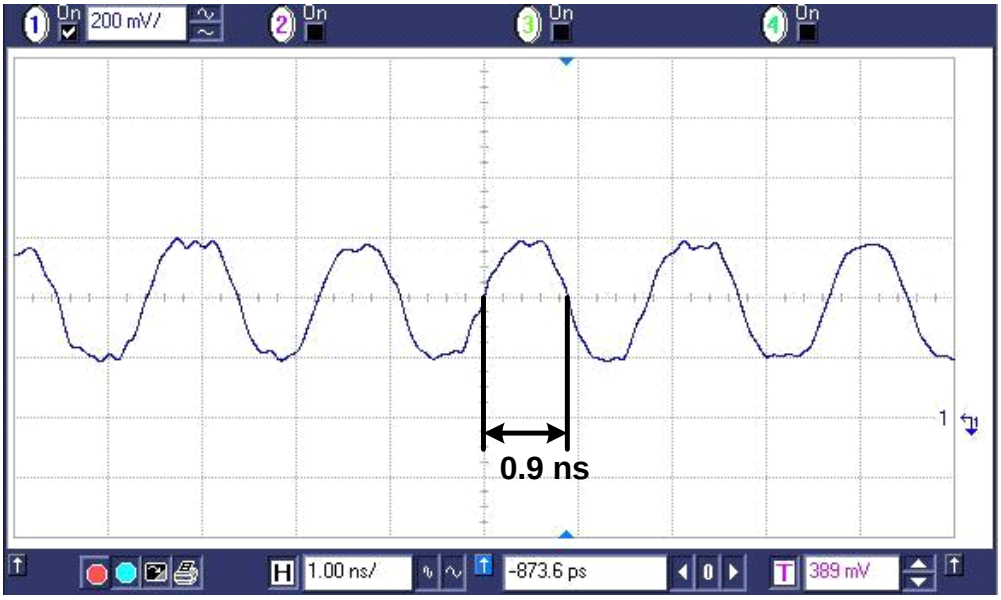


Fig. 5.6 Cyclic “010101” pattern test result at data rate up to 1.1 Gb/s

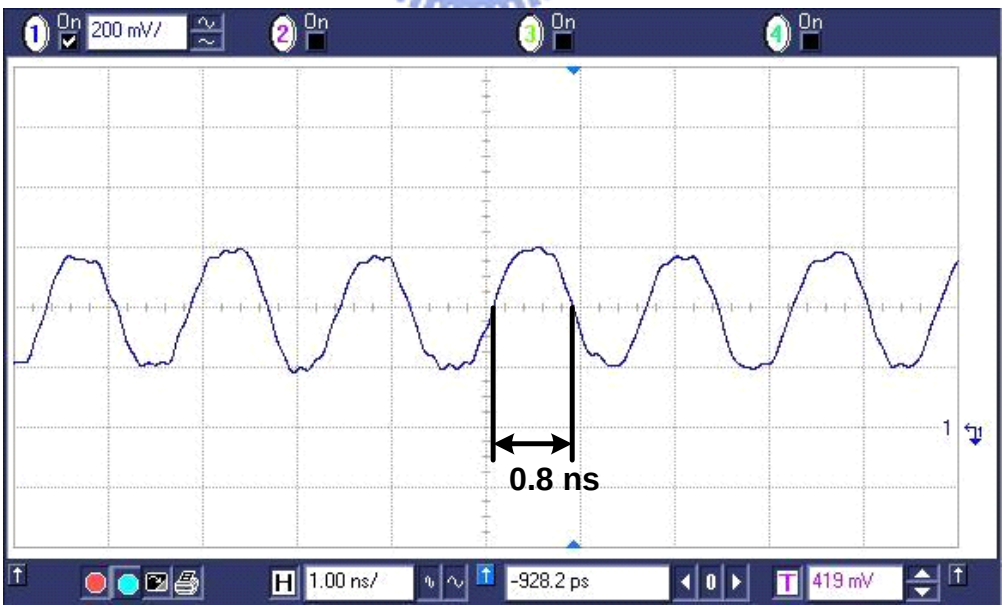


Fig. 5.7 Cyclic “010101” pattern test result at data rate up to 1.25 Gb/s

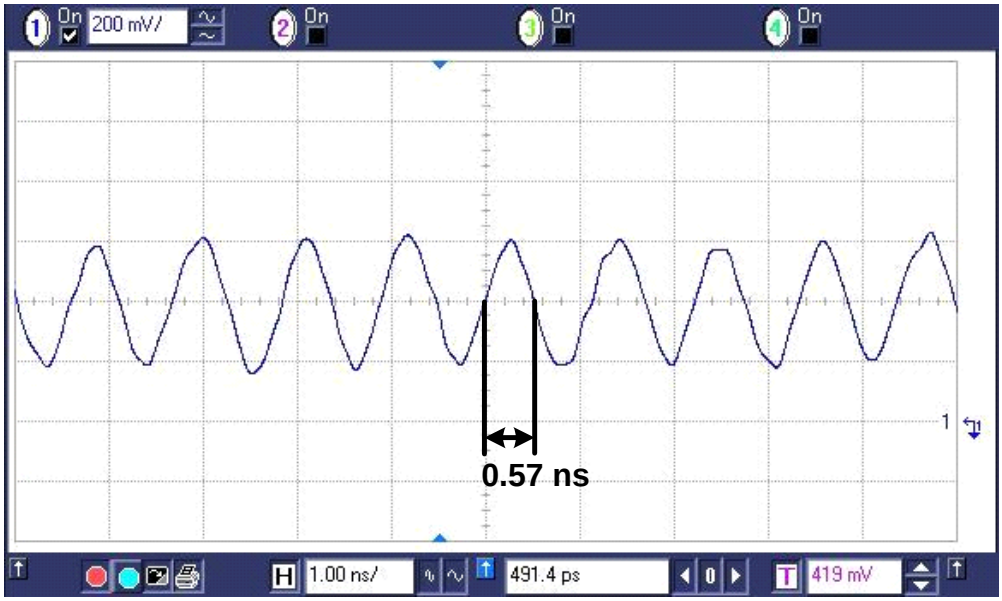


Fig. 5.8 Cyclic “010101” pattern test result at data rate up to 1.8 Gb/s

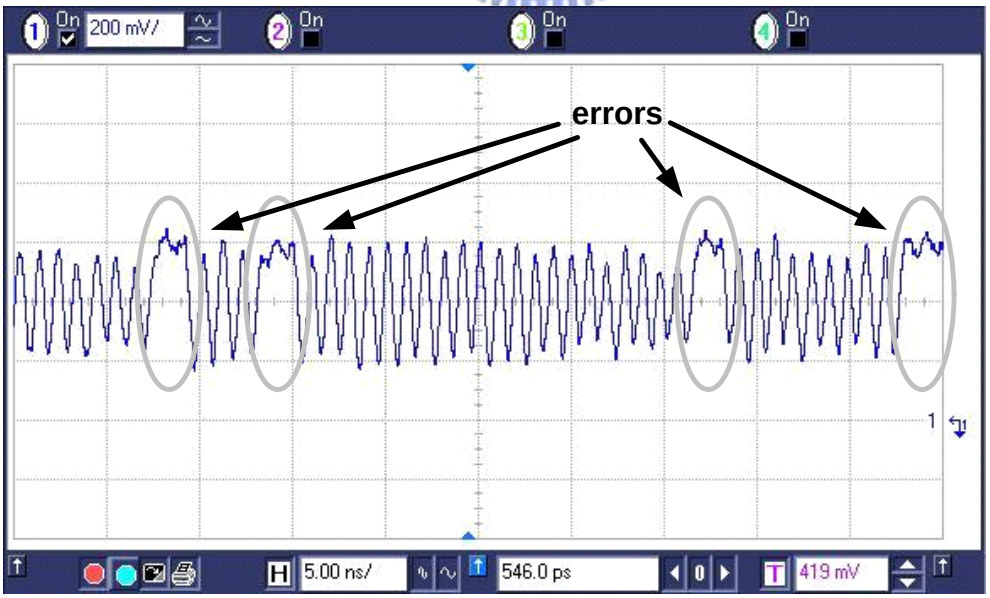


Fig. 5.9 Cyclic “010101” pattern test result at data rate up to 2 Gb/s

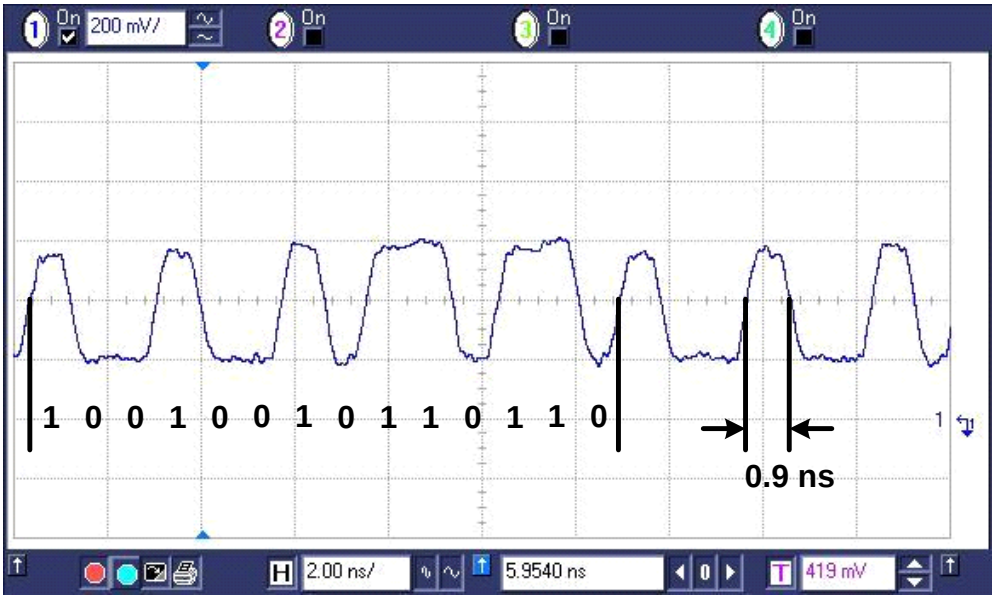


Fig. 5.10 Cyclic “1001001 0110110” pattern test result at data rate up to 1.1 Gb/s

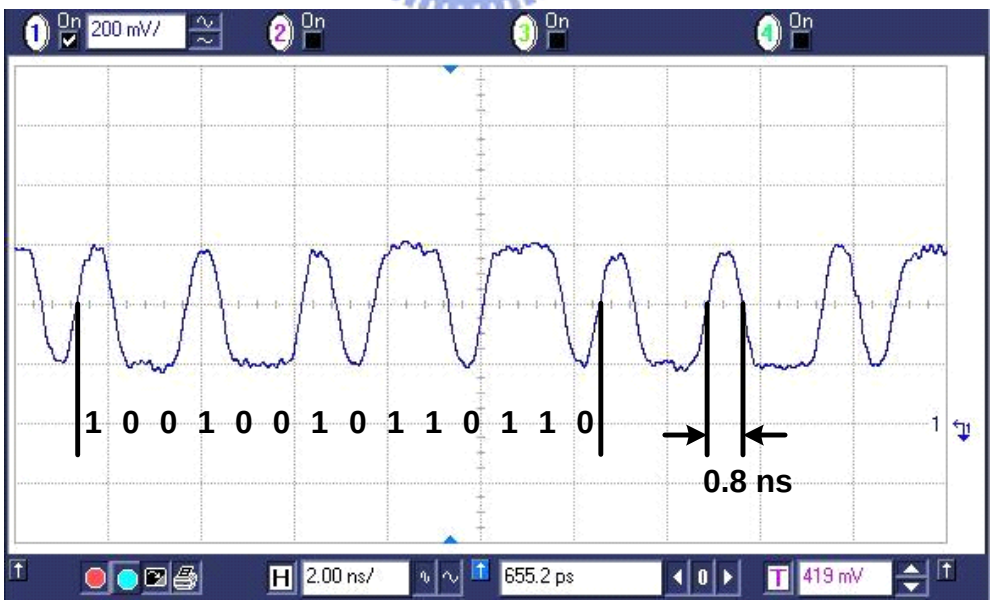


Fig. 5.11 Cyclic “1001001 0110110” pattern test result at data rate up to 1.25 Gb/s

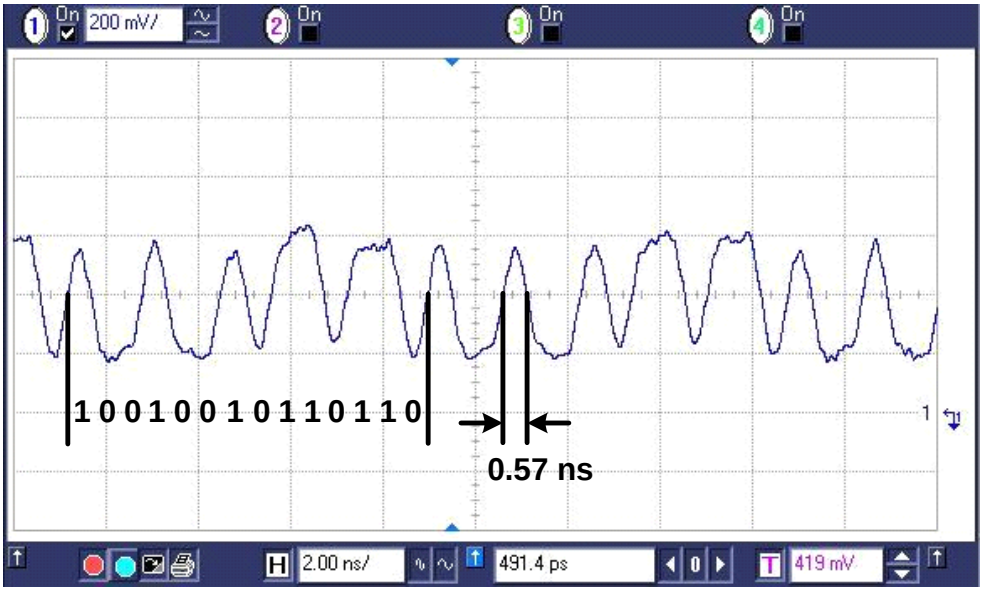


Fig. 5.12 Cyclic “1001001 0110110” pattern test result at data rate up to 1.8 Gb/s

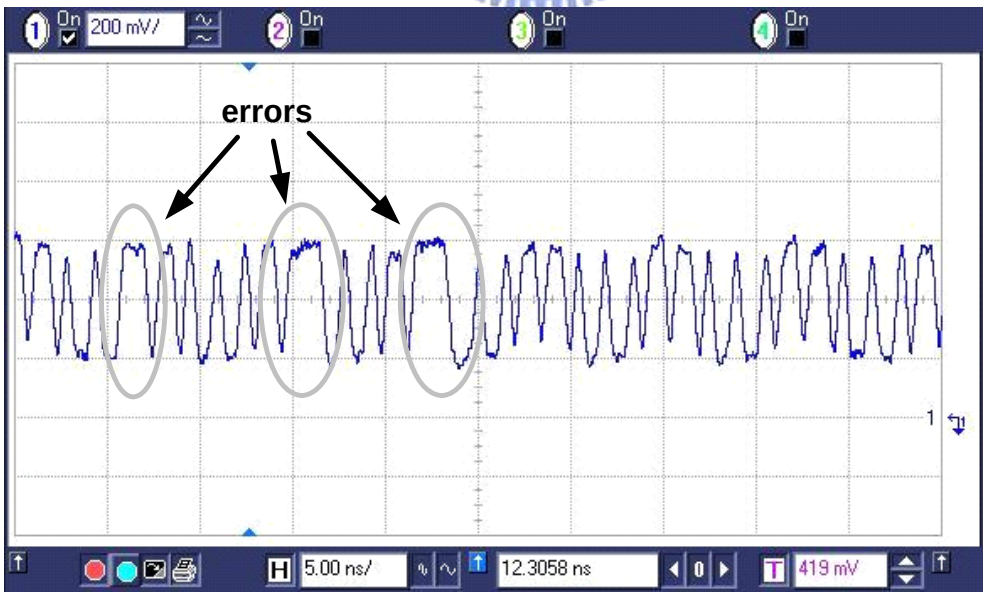


Fig. 5.13 Cyclic “1001001 0110110” pattern test result at data rate up to 2 Gb/s

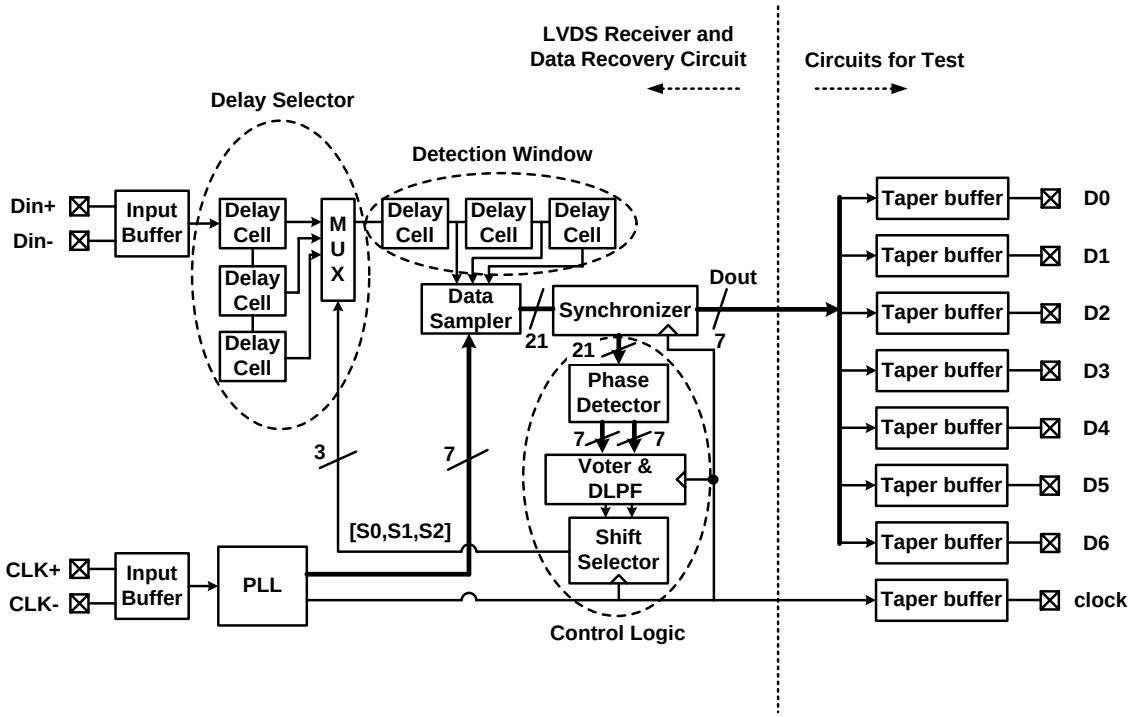


Fig. 5.14 Block diagrams of the parallel output test circuit in the tap out test chip

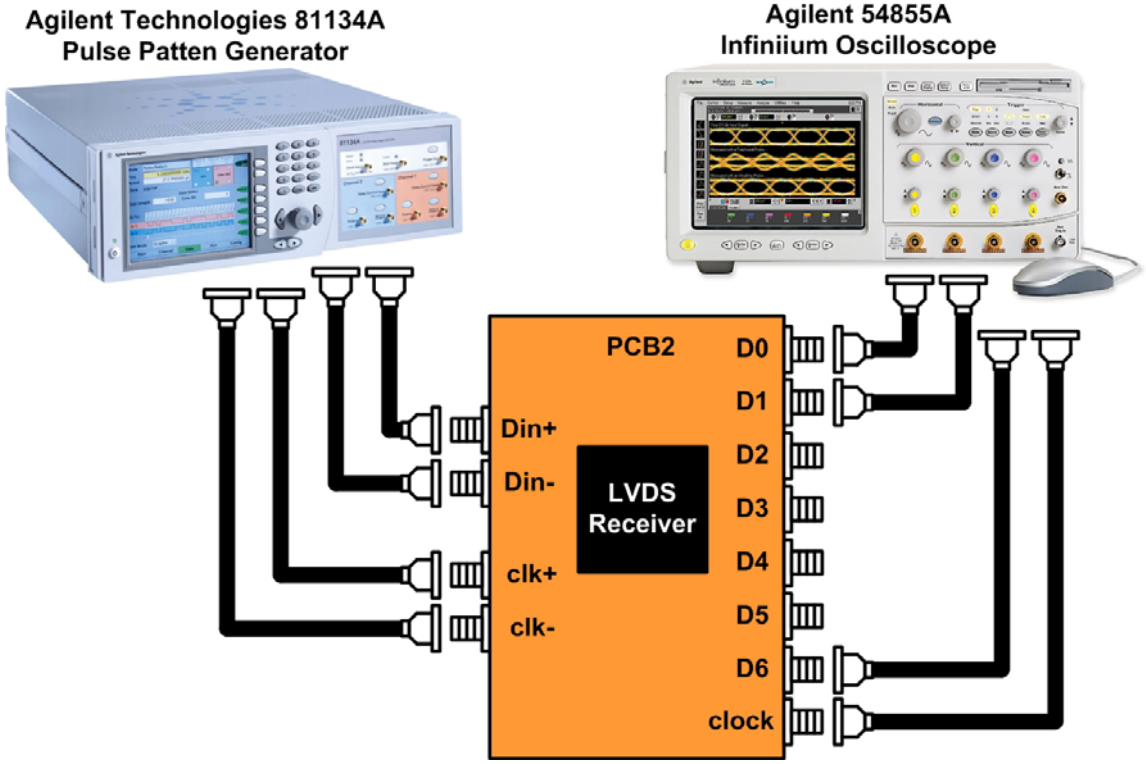


Fig. 5.15 Measurement environment setting of the parallel output test

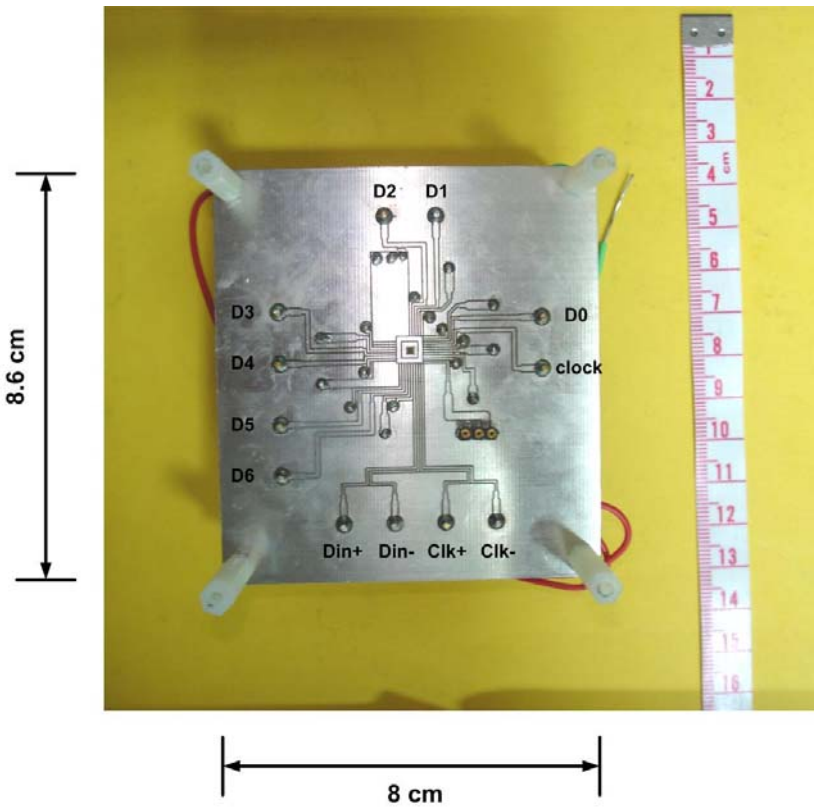


Fig. 5.16 Top view of the parallel output testing PCB photo

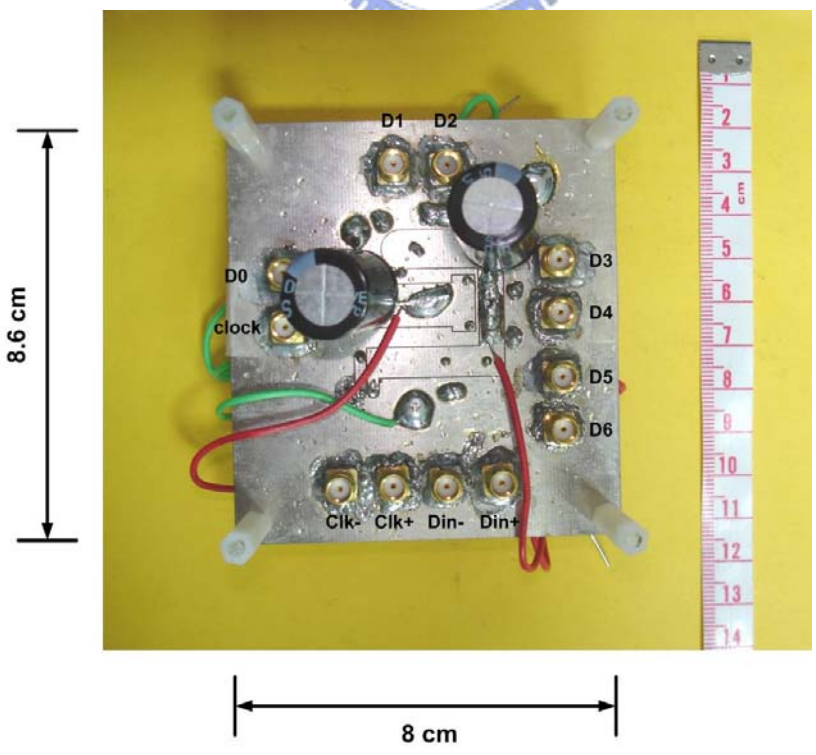


Fig. 5.17 Bottom view of the parallel output testing PCB photo

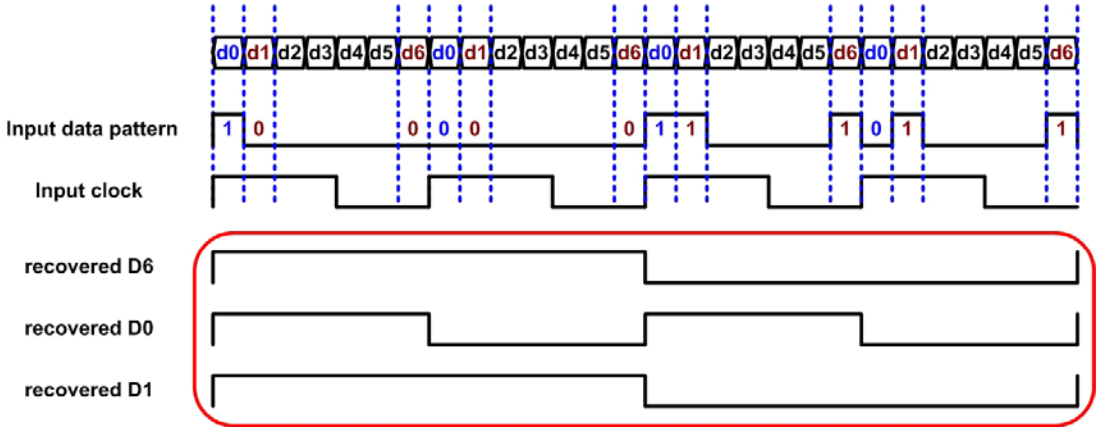


Fig. 5.18 Test pattern for skew tolerance test

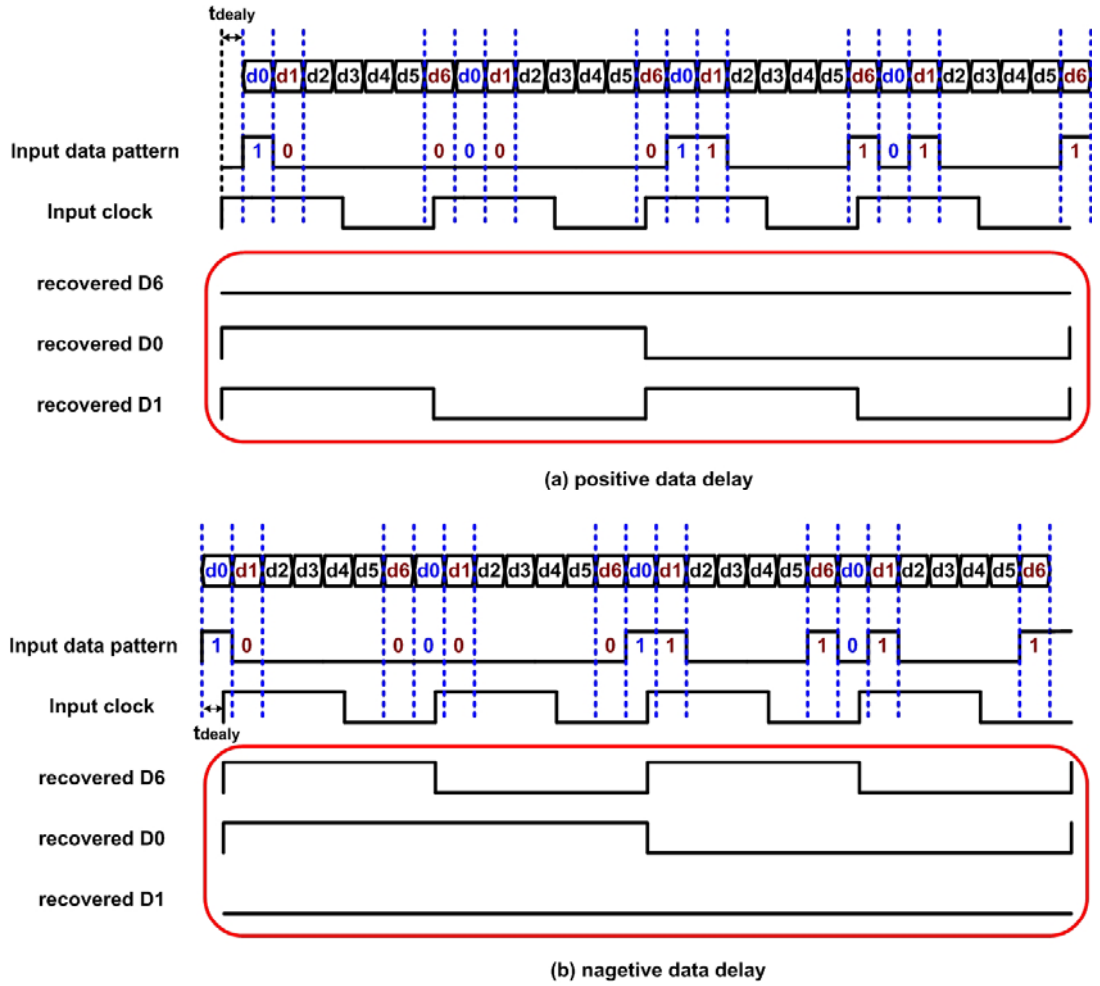


Fig. 5.19 Error recovered data streams when data delay is over skew tolerance

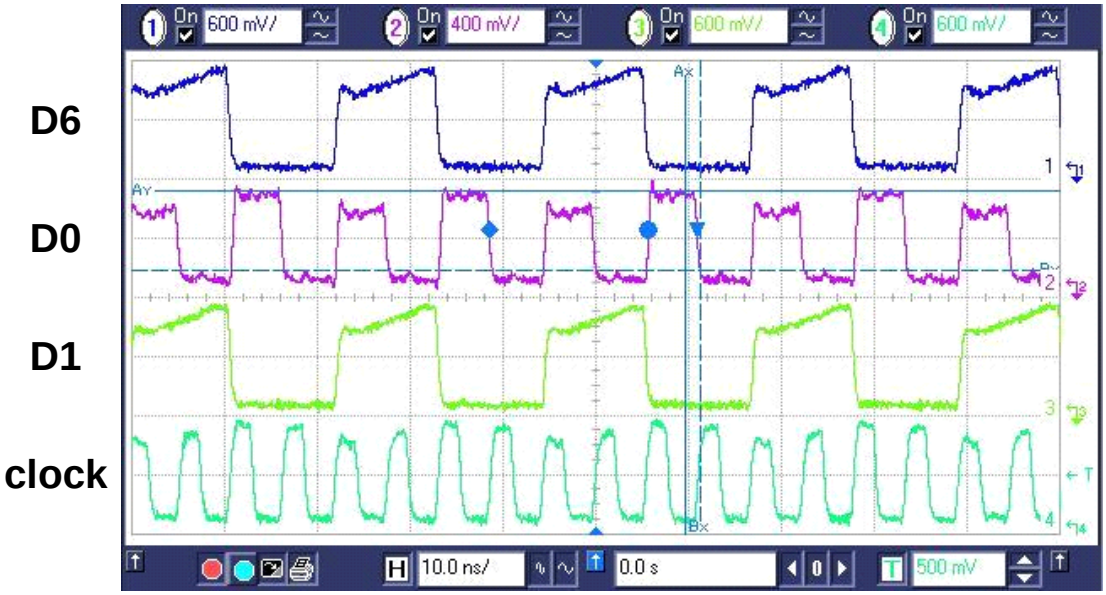


Fig. 5.20 Parallel output testing result when no skew is set in pattern generator

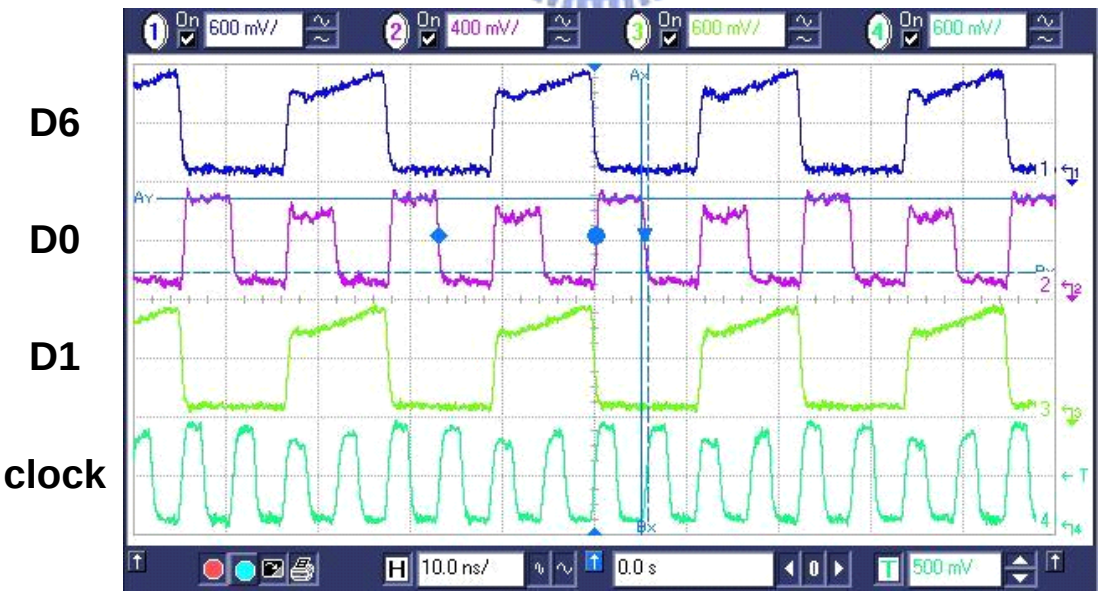


Fig. 5.21 Parallel output testing result when set a 100ps skew in pattern generator

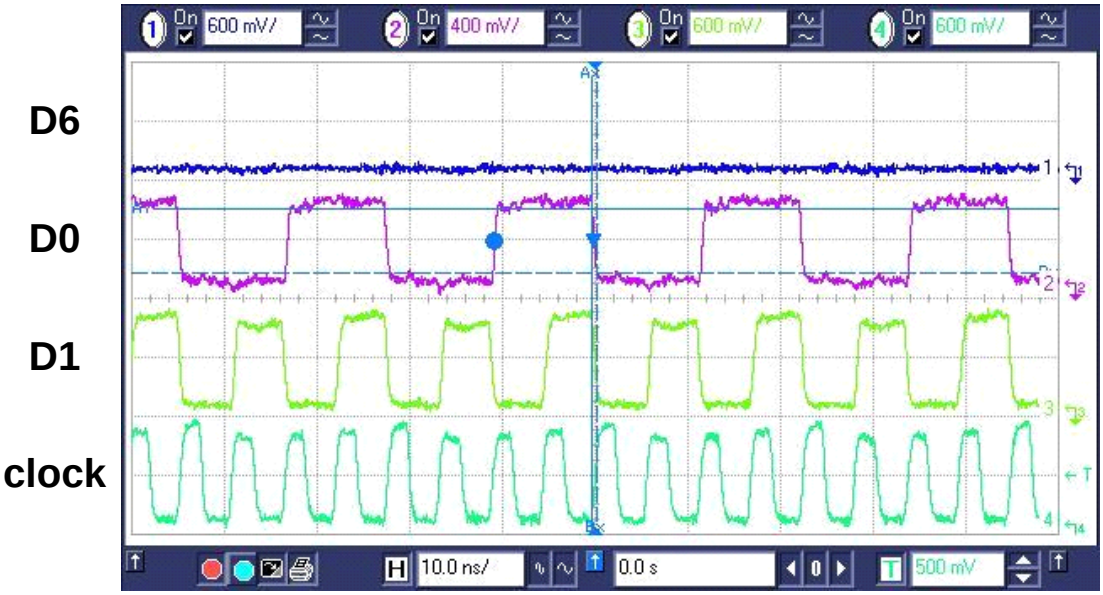


Fig. 5.22 Parallel output testing result when set a 150ps skew in pattern generator

Fig. 5.23 Parallel output testing result when set a –600ps skew in pattern generator

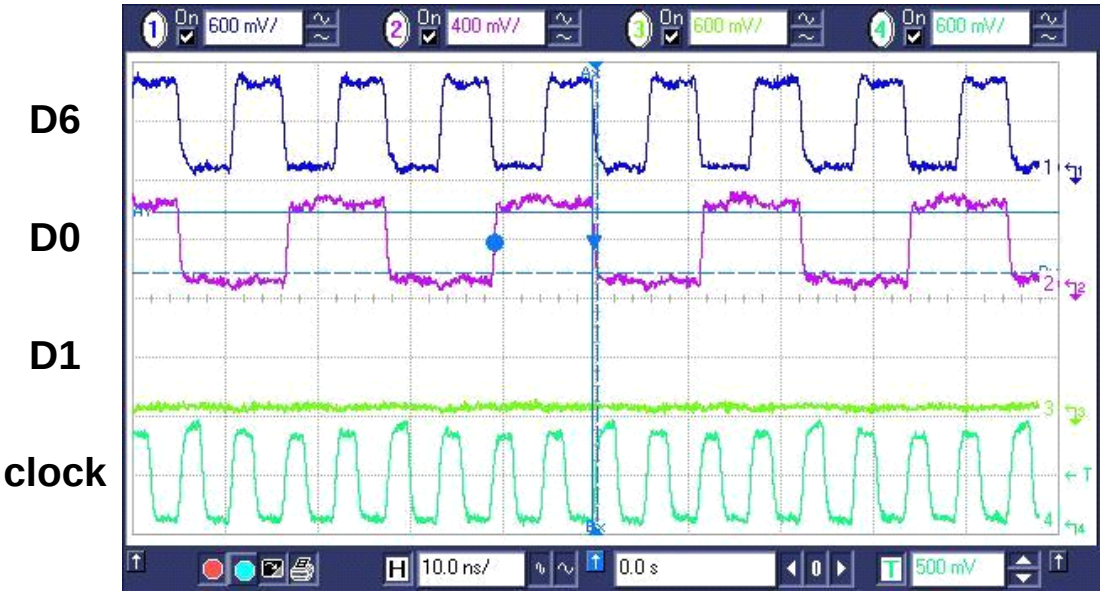


Fig. 5.24 Parallel output testing result when set a –650ps skew in pattern generator

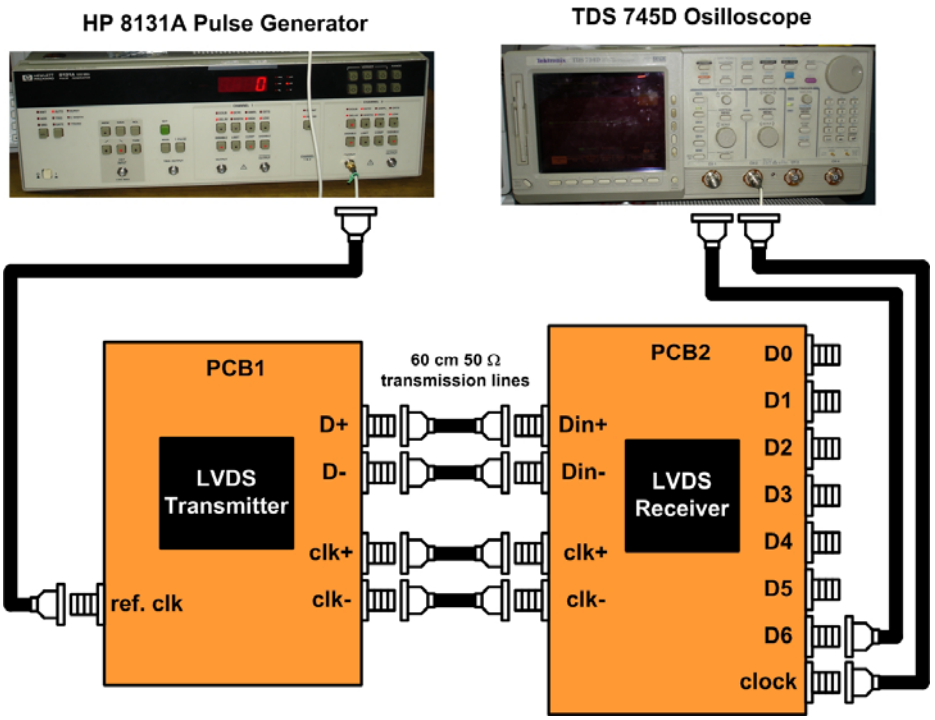


Fig. 5.25 Measurement environment setup of the LVDS Link test

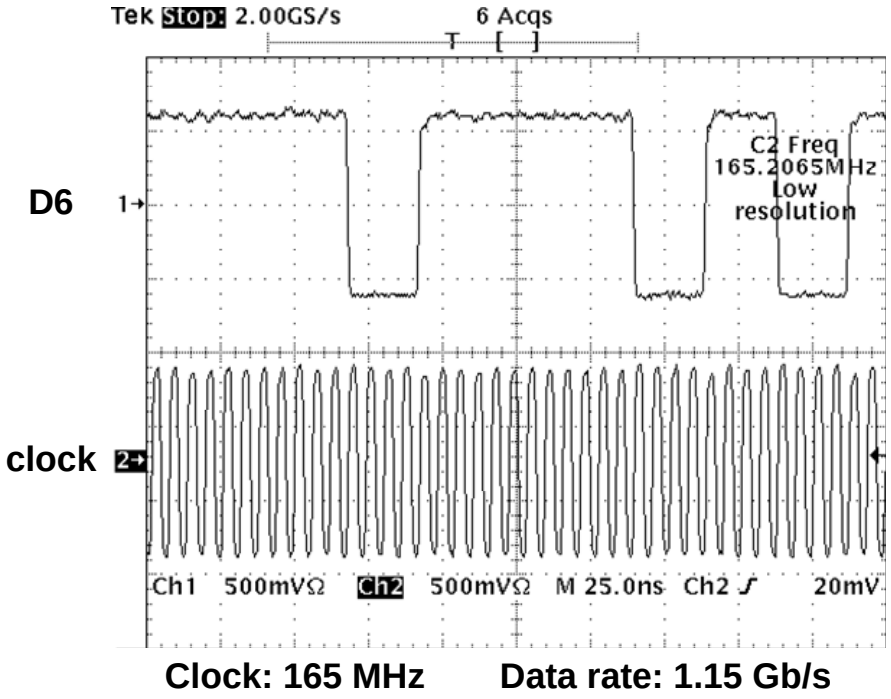


Fig. 5.26 LVDS Link measurement result at data rate up to 1.15 Gb/s

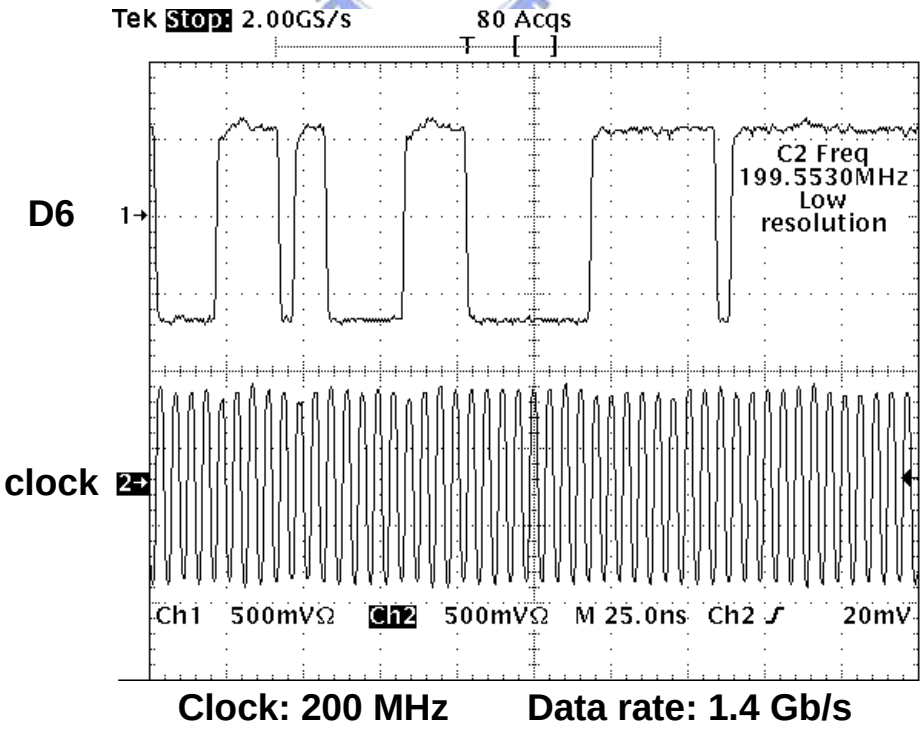


Fig. 5.27 LVDS Link measurement result at data rate up to 1.4 Gb/s

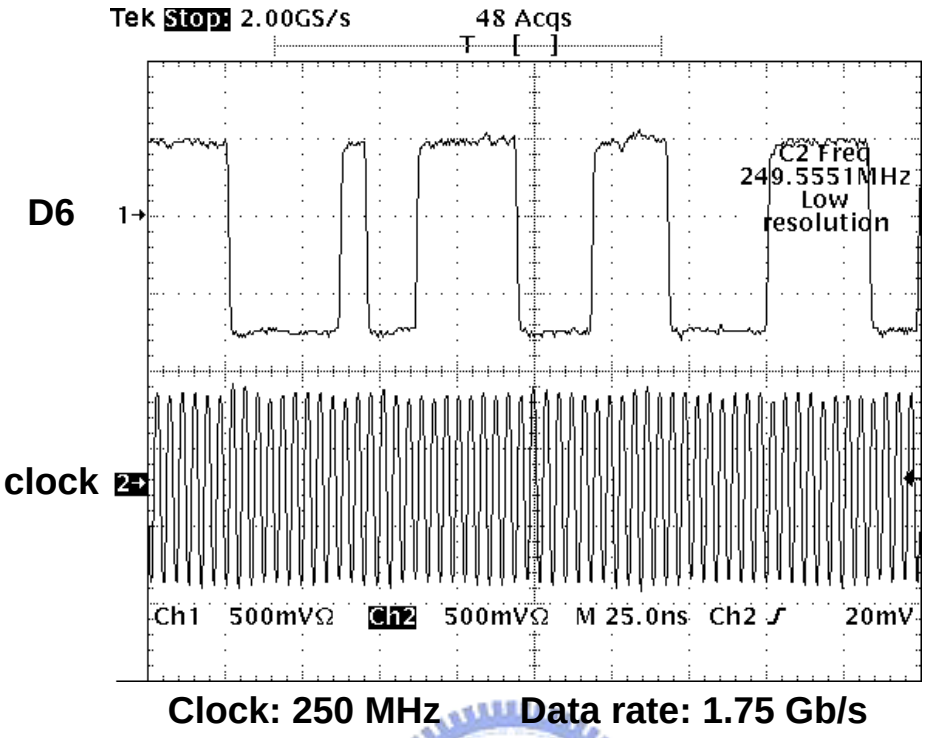


Fig. 5.28 LVDS Link measurement result at data rate up to 1.75 Gb/s

Chapter 6

Conclusion and Future Works

6.1 Conclusion

In this thesis a LVDS CDR receiver is present and the function of LVDS receiver is all verified. The LVDS receiver is implemented in 0.13-μm 1P8M COMS process with 3.3 V and 1.2 V power supply. The LVDS receiver can recover the seven deep LVDS serial input data at data rate from 1.11 Gb/s to 1.8 Gb/s, which can suppose the FPD Link application for UXGA resolution. The skew tolerance of the implemented LVDS receiver is +350 ps ~ –350 ps when the input data rate is 1.25 Gb/s. The power consumption of the LVDS DCR receiver is less than 40 mW when the operation data rate is 1.25 Gb/s.

6.2 Future Works

Although the LVDS CDR receiver is already presented in the thesis and the function of the implement receiver is verified, there are still some tasks can be improved. DLL, delay lock loop, is a circuit similar to the PLL. DLL can lock a reference clock the same as a PLL. And the DLL can implement that with a layout area much smaller than PLL. It is an interesting topic to implement the LVDS DCR receiver with a DLL instead of the PLL.

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