# 國 立 交 通 大 學

## 電子工程學系　電子研究所碩士班

## 碩　士　論　文

低壓差動訊號標準(LVDS)之
平面顯示器高速傳輸器設計

# Design on 1.225 Gb/s LVDS Transmitter for UXGA Flat Panel Display Applications

研 究 生 　:　周宗信

指導教授 　:　柯明道　教授

中華民國九十四年九月

# 低壓差動訊號標準(LVDS)之
# 平面顯示器高速傳輸器設計

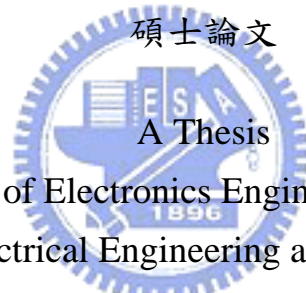# Design on 1.225 Gb/s LVDS Transmitter for UXGA Flat Panel Display Applications

研 究 生： 周宗信        Student  : Tsung-Hsin Chou

指導教授： 柯明道 教授        Advisor  : Prof. Ming-Dou Ker

國立交通大學

電子工程學系　電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronics Engineering

Sep. 2005

Hsin-Chu, Taiwan, Republic of China

中華民國九十四年九月

# 低壓差動訊號標準(LVDS)之
# 平面顯示器高速傳送器設計

學生: 周 宗 信　　　　　　指導教授: 柯 明 道 教授

國立交通大學

電子工程學系　電子研究所碩士班

## 摘要

隨著製程的進步，不僅是積體電路上的電路複雜度更高且速度也隨之提升。因此對於一個高效能的系統，高頻寬、低功率的傳輸介面也就更加需要。而在今日的平面顯示器，其色彩及解析度的要求越來越高。而對一個 UXGA (1600 × 1200) 解析度的顯示器來說，其所需要的資料傳輸速度至少必須在 1.155 Gb/s 以上。在此篇論文，包含兩個設計子項，並經由兩個獨立晶片來驗証。

第一個設計是 PLL。使用的製程是 0.13-μm 1P8M CMOS。使用的電壓是 3.3V，而並沒有除頻。

第二個設計則傳送器的設計包含一個可把 7 位元轉換成一個低壓差動訊號的資料外，並且也提供了一個時序信號。同樣是在 0.13-μm 1P7M CMOS 包含 PRBS 作為內部測試的訊號源。傳送器能正常傳送出 1.4 Gb/s 的串列資料。在電壓電源為 3.3V 時，總消耗功率為 125mW。

# Design on 1.225 Gbps LVDS Transmitter for UXGA Flat Panel Display Applications

Student: Tsung-Hsin Chou          Advisor: Prof. Ming-Dou Ker

*Department of Electronics Engineering & Institute of Electronics*
*National Chiao-Tung University*

## ABSTRACT

With the advanced process technology, the complexity and the operating speed of the circuit are increasing. Therefore, for a system with high performance, a high data-bandwidth and low power transmission interface is very important nowadays. Flat panel displays (FPDs) continue to offer an increase in color depth and resolution, today. For UXGA (1600 × 1200) resolution required by flat panel display system, the data transmission rate must be higher than 1.155 Gb/s. This thesis includes two topics, which were verified through two individual chips.

The first design is the PLL, implemented on the process of 0.13-μm 1P8M CMOS. The operating voltage is 3.3V and the frequency division is not included.

The second design is the transmitter, which includes one data channel, converting seven bits into one data stream, and one clock channel. The circuit is implemented with the process of 0.13-μm 1P8M CMOS. It also includes a PRBS as a self-test signal source. The transmitter can transmit 1.4 GB/s serial data stream properly. The power consumption is about 125mW at 3.3V.

# 誌 謝

　　回顧快兩年的碩士求學生涯，這過程真可以酸甜苦辣、五味雜陳來形容。這其中最苦的時期在於碩一剛入學時，由於當時心態尚未調適過來以至於在修課方面充滿著極大的挫折感與無力感。幸而在實驗室陳世倫學長適時的教導還有鄧志剛學長及陳榮昇學長的鼓勵讓我能咬緊牙根撐過最苦的日子，這不但讓我對日後的修課不再畏懼也對未來所面臨到更困難的挑戰具有更高的抗壓性。回顧這段往事真使我覺得自己何其幸運，能在最無助的時候得到實驗室師長最正面的幫助，這也使我懷著最真誠的心，深深感謝生活中每一個貴人。

　　首先要感謝的是我的指導教授柯明道博士。老師以其本身嚴謹的研究態度以及超乎常人的研究熱情，讓我於這兩年中獲得最珍貴的研究心態與方法。而在老師開明的指導以及豐沛的研究資源下，我不但能盡情將研究的電路下線驗證，也由於所從事的論文研究具實用性。除此之外，老師亦提供相當充裕的研究經費使我在這兩年中不至於生活匱乏而能更努力的從事我的碩士論文研究。畢業之後無論從事任何研究我都將會僅記老師的至理名言：Smart＝ 做事要有效率，成果要有水準。

　　接著要感謝的是一起打拼的同學們，靖驊、弼嘉、建樺、鍵樺、啟祐、諭哥、家燊、煒明、志朋、峻帆、傑忠、岱原、宗熙、台祐、建文、進元，大家一起做研究、出遊、唱歌，讓我在苦悶的研究生活中增添不少樂趣。我也要感謝實驗室陳世倫學長、陳榮昇學長、張瑋仁學長、徐新智學長、陳世宏學長、林昆賢學長、黃彥霖學長、鄧至剛學長、顏承正學長、許勝福學長、王文泰學長。他們無論是在論文研究的瓶頸或是晶片量測的疑難雜症上都給了我很多的方向及幫助，使我能更順利的完成我的碩士論文。

　　最後要感謝我的父母及女友于采加。感謝他們多年來默默的關心與支持，在我最需要的時候給予最大的幫助，使我能勇往向前，一路走來直至今日。生命中的貴人甚多，不可勝數，我將秉持著感恩的心，盡最大的能力幫助也即將展開論文研究的學弟妹們。

<div align="right">

周宗信

九十四年九月

</div>

# CONTENTS

# TABLE CAPTIONS

# FIGURE CAPTIONS

# Chapter 1

# Introduction

## 1.1 MOTIVATION

With advance in IC technology scaling and aggressive circuit design, the operating speed of the system has been pushed to the gigabits-per-second. Besides, the area efficiency has been grown with an exponential rate. However, advantage from those improvements can not increase the overall system performance unless the electric signaling has been taken into consideration. For example, the chip-to-chip, intelligent hub and routers or the optical communication system requires very high speed data transfer. However, the main bottleneck is the board bandwidth is relatively constant, compared with the progress inside the chip.

The traditional technique utilized during the past decades is heavily parallelism. However, this solution can no longer be an optimal one. The increasing date-rate demands increasing complexity, higher cost of the IC package and even the design effort of the printed circuit board (PCB). Moreover, the technique also induces unavoidable huge power consumption and large electric-magnetic-interference (EMI) during signal transmission [1]. Therefore, lots of researches have been proposed and the circuit topology is deviated from parallel-based technology to the serial-based technology. The figure 1.1 is shown to address the basic difference between the parallel-based technology and the serial-based technology.

The design target is to design a LVDS transmitter for the flat panel display system. The required data rate should be able to support the UXGA resolution. As shown in figure 1.2, the data rate required is 1.155 Gb/s.

## 1.2 GENERAL ARCHITECTURE OF THE SERIAL-LINK

The serial-based links can easily provide data rate up to gigabits-per-second, with the advantage of lower power consumption, smaller chip area, less EMI and lower cost than the parallel-based one. The basic topology of the serial-based technology is shown in the figure 1.2. At first, the serial-based technology is achieved by transforming the clock-timed digital signals into the phase-timed digital/analog signals, which is shown in the figure 1.3. Therefore, a multiple phase generator, such as a general phase-lock-loop (PLL), is required and the parallel-to-serial-converter should be utilized. The driver then signals the high-speed digital signal in analog form on the channel. Sometimes, differential signaling is preferred for noise consideration, demonstrated in the figure 1.2. The common noise, like power line noise, can be rejected. Therefore, the signal-to-noise -ratio (SNR) can be increased by the cost of extra pins. The termination resistance is utilized for the sake of reducing signal reflection, which is often the problem of high frequency signaling. The receiver is composed by input-buffers, data-recovery circuits, and serial-to-parallel-converters. The input-buffers will amplify the received signal and sometimes reduce the noise, which is introduced during the transmission period. Then, the amplified signal must be determined by the data-recovery circuits. Yet every so often, the signal timing is not ideally conveyed. Therefore, the data-recovery circuits should sample the signal in the optimal position to reduce the impacts caused by ambiguity of data boundaries. Also, the data required by the other data processing parts will be achieved by the serial-to-parallel-converters, which transform the phase-timed, optimally-sampled signals to clock-timed digital signals.

The population applications are optical communication, USB, IEEE-1394,

TMDS, PECL, LVDS and RSDS, etc [2]. Some industrial standards of high-speed serial links are listed in figure 1.4

## 1.3 THESIS ORGANIZATION

The chapter 2 of this thesis will be the introduction of the LVDS standard. The specification is presented in detail and the applications for the standard are shown. The chapter 3 is devoted to the PLL. The design of PLL should be the most critical part in the transmitter. Therefore, the design and verification by the simulation is described in this chapter. In the chapter 4, discussions of the serial-links are presented and the design of the transmitter is presented. The measurement results are shown in chapter 5 and the conclusion and future work are given in chapter 6.

Parallel-based technology



Serial-based technology
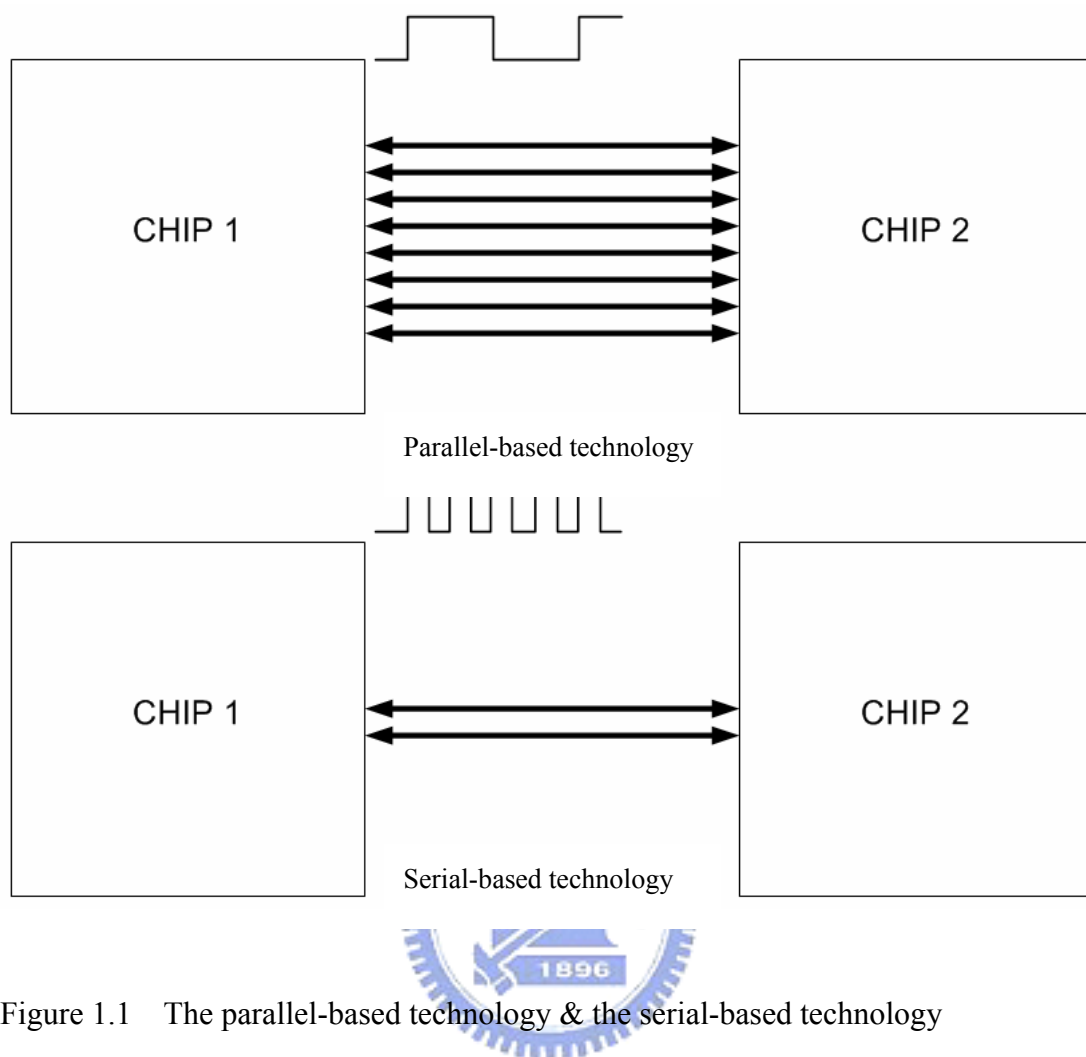
Figure 1.1    The parallel-based technology & the serial-based technology

| Resolution | PLL Frequency | Data Rate |
|---|---|---|
| VGA (640 × 480 pixels) | 25 MHz | 175 Mbps |
| SVGA (800 × 600 pixels) | 40 MHz | 280 Mbps |
| XGA (1024 × 768 pixels) | 65 MHz | 455 Mbps |
| SXGA (1280 × 1024 pixels) | 112 MHz | 784 Mbps |
| UXGA (1600 × 1200 pixels) | 165 MHz | 1155 Mbps |

Figure 1.2    The data rate required for the flat panel display systems
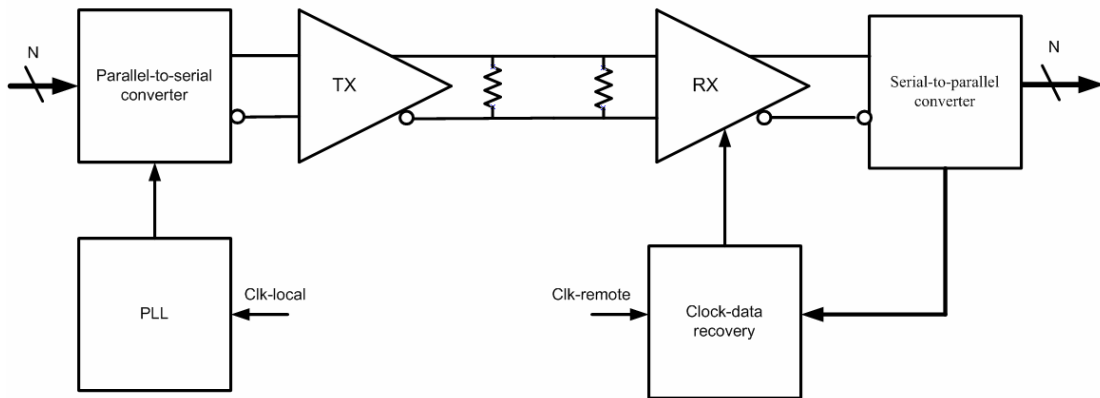
Figure 1.3　The architecture utilizing the differential mode to reduce the EMI
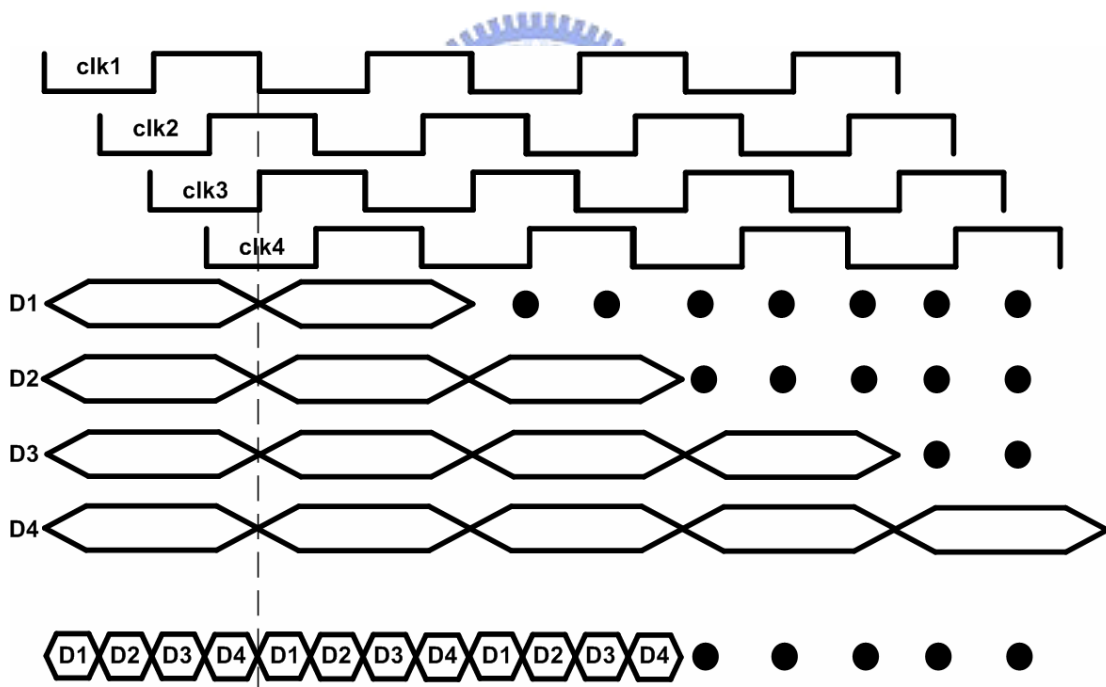


Figure 1.4　The clock-timed signals (upper part) and the phase-timed signals (lower part)

| Standard | Speed |
|----------|-------|
| IEEE 1394 | 400Mbps |
| USB 2.0 (High Speed) | 480Mbps |
| RAM BUS | 800Mbps |
| IEEE 802.3 | 1Gbps |
| TMDS (For UXGA) | 1.65Gbps |
| SONET OC-48 | 2.4883Gbps |

Figure 1.5    Industrial standards for high-speed serial link.

# Chapter 2

# Specifications of Low Voltage Differential Signaling (LVDS)

## 2.1 INTRODUCTION

For the advance in the process technology, the application is more powerful and less expansive. At present, not only the concept of user-friendly-interface but also the application of multimedia demands increasingly data transfer. Because they give users better experience and more entertainment, this trend will not stop in the near future. Besides, since the operating speed of the chip approaches several giga-hertz, the data transfer between the chips also requires very high speed I/O interface, otherwise the system performance degrades importantly.

However, the standards, serviceable in the past decades, such as RS-422, RS-485, SCSI and so forth, can not do the job. These standards all have their own notable degradation while transferring raw data across a medium. Challenges, such as power consumption, fast data transfer and economical solution, remain to be solved. However, these factors often have relations of trade-off. Fast data transfer always requires higher power consumption. Lower power consumption always implies higher circuit complexity, therefore higher cost. Also these challenges should be solved under the requirement of lower voltage level, which is a severe terms.

Therefore, some standards have been proposed. The Low-Voltage-Differential-signaling (LVDS) is one of them. It has lower voltage swing (about 400 mV), higher data rate (above 400Mb/s) and lower power

consumptions. It can solve the bottleneck problems while serving as the high speed I/O interface in a wide range of application areas.

There are two industry standards that define LVDS [3]. The more common of the two is the generic electrical layer standard defined by the TIA (Telecommunications Industry Association) [4], which is known as ANSI/TIA/EIA-644, and the other is the IEEE (Institute for Electrical and Electronics Engineering) standard which is titled SCI (Scalable Coherent Interface).

### 2.1.1 ANSI/TIA/EIA-644

The editor position of this specification is held by the National Semiconductor Corporation. The electric characteristic of the driver output and the receiver input is defined. The functional specifications and the protocols are not defined. Therefore it is the more generic of the two standards and is intended for multiple applications. The electrical-only ANSI/TIA/EIA-644 standard is shown in Table 2.1, and it is intended to be referenced by other standards that specify the complete interface (connectors, protocol, etc.). The standard implies a recommended maximum data rate of 655 Mb/s and a theoretical limitation of 1.923 Gb/s. However, the speed achievable is not definite as its recommendation. It is application (desired signal quality, such as SNR) and device (such as transition time) specific. At present, the LVDS standard is feasible under the operating speed ranging from 500 Mb/s to 1.5 Gb/s above. Also the media specification is supplied in this standard and the failsafe operations of the receiver under fault conditions are given. Besides, other configurations are discussed, such as multi-drop or bidirectional half-duplex configurations, as shown in the figure 2.1.

*2.1.2 IEEE 1596.3 SCI-LVDS*

This standard, SCI-LVDS, is defined as a subset of SCI and is specified in the IEEE 1596.3 standard, which is approved in Mar. 1994. Originally, the SCI standard referenced a differential ECL (Emitter-Couple-Logic) within the SCI 1596-1992 IEEE standard [5]. However, the ECL standard is although high-speed with the disadvantage of massive power consumptions. Besides, ECL and PECL require more complex termination than the one-resistor solution for LVDS [6]. PECL drivers commonly require 220Ω pull down resistors from each driver output, along with 100Ω resistor across the receiver input. Therefore, this SCI standard only addressed the high-speed aspect but ignore the low-power requirement. Thus, the SCI-LVDS is introduced to include the power consumption issues.

The SCI-LVDS standard specified the electric signaling levels for the purpose of high-speed data transfer and low-power requirement. The electric characteristic is similar to the TIA version, but differs in some electric requirements and load conditions. Both standards feature similar driver output levels, receiver thresholds and data rates. However, the SCI-LVDS also defines the encoding for packet switching used in SCI data transfer, which is not within the scope of TIA version. Packets are constructed from 2-byte (doublet) symbols, which is the fundamental 16-bit symbol size. The media specification is not given. Also the data transfer speed is not noted as the former one. It is in the order of 500 Mb/s based on serial or parallel transmission of 1, 4, 8, 16, 32 and 64 … bits.

In the interest of promoting a wider standard, no specific process technology, medium, or power supply voltages are defined by either standard. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies, migrate from 5V to 3.3V to sub-3V supplies, and transmit over PCB traces or cable, thereby serving a broad range of applications in many industry segments.

National Semiconductor Corporation held the chairperson position for this standard. As discussed, the generic property of ANSI/TIA/EIA-644 makes it more popular than the IEEE 1596.3 SCI-LVDS standard. Therefore, this design is based on the ANSI/TIA/EIA-644 standard.

## 2.2 SPECIFICATION OF LVDS

The basic principle and characteristic of the Low-Voltage Differential Signaling (LVDS) is discussed as following.

### 2.2.1 Basic Concepts of LVDS standard

The basic topology of LVDS is shown in figure 2.2, which shows a simplified driver and receiver connected via 100Ω differential impedance media. As shown in figure 2.3, it has four switches, constructed by MOS here, and two current sources. The signaling is operating on a differential pair line, such as two balance PCB traces or balance cable lines. Based on the transmitted data, these four switches will change the current path to induce the voltage polarity change. The receiver has a DC impedance of 100Ω and the switched-current across the impedance will generating the essential part of the voltage sensed by receiver, which is about 350 mV.

For the method of differential signaling, LVDS is less susceptible to common-mode noise than single-ended schemes. Therefore the electromagnetic emission will have less impact on the signal quality. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receiver which detects only

the voltage difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. The current-mode driver is not prone to ringing and switching spikes, further reducing noise. Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current-mode, very low almost flat power consumption across frequency is obtained. Switching spikes in the driver are very small, so that total current consumption does not increase exponentially as switching frequency is increased. Also, the power consumed by the load (3.5 mA × 350 mV = 1.225 mW) is very small in magnitude.

The differential data transmission method although has lots of advantages, but the cost of extra cable lines or PCB traces seems to be a disadvantage, compared with the single-ended scheme. However, the single-ended scheme always consumes massive power, and a great deal of ground pins are demanded for acceptable signal quality. Since the ground of such scheme is not always clear, the number of ground pins demanded is large. Therefore, extra pins required by the differential data transmission method should not be a major problem. At the same time, the PCB design is a challenge of both scheme, which is out of the scope of this paper.

Dedicated point-to-point links provide the best signal quality due to the clear paths they provide. LVDS has many advantages that make it likely to become the next famous data transmission standard rates from hundreds to thousands of megabits per second and short haul distances in the tens of meters. In this role, LVDS far exceeds the 20 Kb/s to 30 Mb/s rates of the common RS-232, RS-422, and RS-485 standards.

*2.2.2 Several Configurations*

As shown in Fig. 2.2, the point-to-point configuration is the most general and basic scheme used for LVDS standard [3]. However, other topologies/configurations are also possible.

The configuration, as shown in the upper part of Fig. 2.1, allows bi-directional communication over a single twisted pair cable. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (< 10 m).

In the lower part of Fig. 2.5, a multi-drop configuration connects multiple receivers to a driver. These are useful in data distribution applications. They can also be used if the stub lengths are as short as possible (less than 12 mm, which is application dependent). Use receivers with power-off high impedance if the network needs to remain active when one or more nodes are powered down. This application is good when the same set of data needs to be distributed to multiple locations.

Also, multi-point configuration supports multiple drivers, but only one is allowed to be active at any given time. With such scheme, double terminated busses can be used without trading off signal swing and noise margin. Termination should be located at both ends of the bus. Besides, failsafe operation should be considered. When all drivers, constructed in tri-state type, are in the high impedance state, a known state on the bus is required. As with the multi-drop bus, stubs off the mainline should be kept as short as possible to minimize transmission line problems, such as reflection or decay.


*2.2.3 Discussion of the termination, connecter and cables*

The distance and the speed requirements seem to be a simple question at first.

However, after some study, the question is rather a system level one than a device level one. A number of other parameters besides the switching characteristics of the drivers and receivers must be known. The cables, connectors and PCB used are application dependant and have essential effects on the system performance. Also, the performance criteria for the system should be identified. Therefore, discussion for termination, cables and connectors are given as below and the signal quality criteria is discussion in the next subsection.

It is very common for designers to automatically use any off-the-shelf cables and connectors and 50 Ω auto-routing when doing new designs. While this may work for some LVDS designs, it can lead to noise problems. Remember that LVDS is differential and does have low swing, current-mode outputs to reduce noise, but that its transition times are quite fast. This means impedance matching (especially differential impedance matching) is very important. Those off-the-shelf connectors and that cheap blue ribbon cable are not meant for high-speed signals (especially differential signals) and do not always have controlled impedance.

As discussed above, the termination is an important issue considering high frequency signaling. The signal quality will be impacted severely with bad termination, because of the electromagnetic effect. The signal will reflect from the far terminal and corrupt the signal characteristic. Whether the LVDS transmission medium consists of cables or controlled impedance traces on a printed circuit board, the transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate the high-speed signals. If the medium is not properly terminated, signals reflect from the end of the cables or traces and may interfere with succeeding signals.

Proper termination also reduces unwanted electro-magnetic emissions and provides the optimum signal quality. To prevent reflections, LVDS requires a

terminating resistor that is matched to the actual cables or PCB traces differential impedance. Commonly a 100 Ω termination is employed. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input. Also, Center tap capacitance termination may also be used in conjunction with two 50Ω resistors to filter common-mode noise at the expense of extra components if desired. This is shown in the figure 2.5. This termination is not commonly used or required.

The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL (Positive Emitter Coupled Logic) require more complex termination than the one-resistor solution for LVDS [6]. PECL drivers commonly require 220 Ω pull down resistors from each driver output, along with 100 Ω resistor across the receiver input. For more stringent specification, impedance control should be employed or the signal quality will be corrupted by signal reflection.

As shown above, the LVDS standard is intended to be referenced by other standard [7], [8]. It does not define the functional properties or system protocols. Also, the media is not given, for the generic purpose. The referencing standard should include the media, data rate, length, connectors, function, and pin assignments, etc. The connectors and cables required are application specific.

For high-speed operation, it suggests that to use differential cables is better choice for LVDS standards, such as twisted pair cables (shown in figure 2.6), twin-ax cables (shown in figure 2.7) or flex circuits (shown in figure 2.8) with closely coupled differential traces. CAT 3, suitable for distance about 10 m, and CAT 5, for longer distance, is readily available.

Twisted pair cables are a relatively low cost solution with good balance. It is flexible and an appropriate medium for long distance transmission, based on the

application.

Twin-ax cables are also flexible and have low skew compared with the twisted pair cables. This type of cable shields around each pair for isolation. For being not twisted, they tend to have very low skew within a pair and between pairs. These cables are for the purpose of long distance. Twin-ax cables have been commonly utilized in Channel Link and FPD-Link applications.

Flex circuits is a good choice for very short runs. However, as shown in figure 2.7, it is difficult to be shielded. It is often used as interconnects between boards within systems. The members of differential pairs should be closely coupled (S < W) and use ground shield traces between the different differential pairs.

Since the system always deviates from one to the other, the connectors are also application dependent. The connectors depend upon the cable system being used, the number of pins, the need for shielding and other mechanical footprint concerns. Depending on the data rate, the standard connectors, for medium speed, and the optimized, low skew connectors, for higher speed, are readily available and less expansive.

*2.2.4 The criteria for Signal Quality*

As mentioned yet, signal quality may be measured by a variety of means, such as rise time at the load, jitter at the eye pattern and bit error rate test, etc [9]. The eye pattern and bit error rate test is the most common methods in design the high speed I/O interface. They are described as following.

Eye pattern measurements are useful in measuring the amount of jitter versus the unit internal, to establish the data rate versus cable length curves. Therefore the method is a very accurate way to measure the expected signal quality and severed as system level performance criteria.

The eye pattern is used to measure the effects of inter-symbol interference (ISI) on random data transmitted through a particular medium. The signal transition time is data dependant. For example, in the most general NRZ encoding scheme, a transition high after a long series of low will have a sharper edge. And a fast transition will have softer edge. Overlaid the signal, the so-called eye pattern is shown. The effect is shown in the figure 2.9. The left side is the ideal eye pattern and the right side is the practical eye pattern at the end of cables. As it shows, the practical one has not only slower transition edge but also wider width of the crossing points. Besides, for the receiver end, the appropriate eye pattern should be identified. The figure 2.10 is an simplified example. It describes the sampling locations for minimum jitter. Peak-to-peak jitter is defined as the width of the signal crossing the optimal receiver thresholds. However, the receiver is specified to switch between + 100 mV and − 100 mV. Therefore for a worse case jitter criterion, a box should be drawn between ± 100 mV and the jitter is measured between the first and last crossing at ± 100 mV. If the vertical axis units in Fig. 2.10 were 100mV/division, the worse case jitter is at ± 100 mV levels.

Eye patterns can show the effects of a random data pattern after transmitting through medium. Therefore, they provide a useful tool to analyze jitter and the resulting signal quality. They served as a criterion to determine the maximum cable length for a given data rate or vice versa. The acceptable amount of jitter is different from system to system. Commonly 5 %, 10 %, or 20 % is acceptable, with 20 % jitter usually being an upper practical limit. It will be difficult to make error-free recovery of NRZ data, with more than 20% jitter, which is usually close down the eye opening.

The other popular method is the bit error rate test. Bit error rate testing is one way to measure of the performance of a communications system. The standard equation for a bit error rate measurement is:

Bit Error Rate = (Number of Bit errors)/(Total Number of Bits)

Common measurement points are bit error rates of:

≤ 1 x 10-12 => One or less errors in 1 trillion bits sent

≤ 1 x 10-14 => One or less errors in 100 trillion bits sent

Note that BER testing is time intensive. The time length of the test is determined by the data rate and also the desired performance benchmark. For example, if the data rate is 50Mbps, and the benchmark is an error rate of 1 x 10-14 or better, a run time of 2,000,000 seconds is required for a serial channel. 2,000,000 seconds equates to 555.6 hours or 23.15 days!

For both performance measurements, a PRBS (pseudo-random bit sequence) is often severed as an random transmitting data generator. Depending on the specification required, the period of PRBS can be determined.

### 2.2.5 The signal level of the LVDS standard

An LVDS receiver can tolerate a maximum of ± 1 V ground shift between the driver's ground and the receiver's ground. Note that LVDS has a typical output offset voltage of + 1.2 V, and the summation of ground shifting, output offset voltage and any longitudinally coupled noise is the common mode voltage seen on the receiver input pins with respect to the receiver ground. The common mode range of the receiver is + 0.2 V to + 2.2 V, and the recommended receiver input voltage range is from ground to + 2.4 V. For example, if a driver has a $V_{OH}$ of 1.4 V and a $V_{OL}$ of 1.0 V (with respect to the driver ground), and a + 1 V ground shift is present (driver ground + 1 V higher than receiver ground), this will become + 2.4 V (1.4 + 1.0) as $V_{IH}$ and + 2.0 V (1.0 + 1.0) as $V_{IL}$ on the receiver inputs referenced to the receiver ground. On the contrary, with a − 1 V ground shift and the same driver levels results as 0.4 V (1.4 − 1.0) $V_{IH}$ and 0.0 V (1.0 − 1.0) $V_{IL}$ on the receiver inputs. This is

shown in Fig. 2.11.

*2.2.6 Advantages and Applications*

The LVDS solutions are less expensive CMOS implementations as compared to specific solutions on elaborate and complex processes, such as GaAs or bipolar. Besides, by using low cost, off-the-shelf CAT3 cables and connectors, or FR4 materials, high performance can be achieved easily. The power consumptions are very little, so power supplies, fans, etc., can be reduced or eliminated and the total cost of LVDS interface can be lower. Since the utilizing of differential data transmission method, LVDS is a low noise producing, noise tolerant technology − power supply and EMI noise are greatly minimized. Compared with other standards, LVDS transceivers are relatively inexpensive and can also be integrated around digital cores, providing a higher level of integration. It can move data so much faster than TTL (Transistor-Transistor Logic), so multiple TTL signals can be serialized into a single LVDS channel, reducing board, connector, and cable costs.

The high-speed and low-power/noise/cost benefits of LVDS broaden the scope of LVDS applications far beyond those for traditional technologies. The applications of LVDS in several aspects are summarized in figure 2.12.

*2.2.7 Conclusion of the LVDS standard*

Consumers are demanding more realistic, visual information in the office and in the home. This is driving the need to move video, 3-D graphics and photo-realistic image data from camera to PCs and printers through LAN, phone, and satellite systems to home set top boxes and digital VCRs. Solutions exist today to move this high-speed digital data both very short and very long distances: on a printed circuit board (PCB) and across fiber or satellite networks. Moving this data from

board-to-board or box-to-box, however, requires an extremely high-performance solution that consumes a minimum of power, generates little noise (must meet increasingly stringent FCC/CISPR EMI requirements), is relatively immune to noise and is inexpensive. Many kinds of specifications are purposed for these requirements, such as ECL, PECL, LVDS and RSDS [10].

As shown above, the LVDS standard can solve these problems and severed as a high performance I/O interface. The high speed signaling is achieved by the differential signaling with lower swing. The differential signaling also provides the advantage of reducing EMI, power, complexity and better noise immunity. Besides, since the high speed achievable by the LVDS standard, it allows designers to implement a simple point-to-point link without complex termination issues. Also, the low power and differential signaling makes the integration with the digital core and PLL a reliable solution. Therefore, a compact, low cost high speed interface is achievable. When gigabits at mW are required, the LVDS solution can be a simple and high-performance choice. Merits and drawbacks of different I/O interface technologies are summarized in table 2.2 and table 2.3.

Table 2.1    The electrical-only ANSI/TIA/EIA-644 (LVDS) standard of LVDS.

| Parameter | Description | Min | Max |
|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | 247 mV | 454 mV |
| $V_{OS}$ | Output Offset Voltage | 1.125 V | 1.375 V |
| $\Delta V_{OD}$ | \|Change to $V_{OD}$\| | | 50 mV |
| $\Delta V_{OS}$ | \|Change to $V_{OS}$\| | | 50 mV |
| $I_{SA}, I_{SB}$ | Short Circuit Current | | 24 mA |
| $t_r / t_f$ | Output Rise/Fall Times ($\geq$ 200 Mb/s) | 0.26 ns | 1.5 ns |
| | Output Rise/Fall Times ($\leq$ 199 Mb/s) | 0.26 ns | 30 % of $t_{ui}$ |
| $I_{IN}$ | Input Current | | 20$\mu$A |
| $V_{TH}$ | \|Threshold Voltage\| | | $\pm$ 100 mV |
| $V_{IN}$ | Input Voltage Range | 0 V | 2.4 V |

$t_{ui}$ is unit interval (i.e. bit width).

Table 2.2    Merits and drawbacks of different I/O interface technologies.

| Advantages | LVDS | PECL | Optics | RS-422 | GTL | TTL |
|---|---|---|---|---|---|---|
| Data rate up to 1 Gb/s | + | + | + | – | – | – |
| Very low skew | + | + | + | – | + | – |
| Low dynamic power | + | – | + | – | – | – |
| Cost effective | + | – | – | + | + | + |
| Low noise/EMI | + | + | + | – | – | – |
| Single power supply/reference | + | – | + | + | – | + |
| Migration path to low voltage | + | – | + | – | + | + |
| Simple termination | + | – | – | + | – | + |
| Wide common-mode range | – | + | + | + | – | – |
| Process independent | + | – | + | + | + | + |
| integration with digital circuits | + | – | – | – | + | + |
| Cable breakage/splicing issues | + | + | – | + | + | + |
| Long distance transmission | – | + | + | + | – | – |
| Industrial temp/voltage range | + | + | + | + | + | + |

Table 2.3　Quick comparison of the differential signaling standards

| parameter | LVDS | PECL | RS-422 |
|---|---|---|---|
| Differential output voltage | ±250~450 mV | ±600~1000 mV | ±2~±5 |
| Receiver input threshold | ±100 mV | ±200~300 mV | ±200 mV |
| Data rate | >400 Mb/s | >400 Mb/s | <30 Mb/s |
| Supply current quad driver* | 8 mA (max) | 32~65 mA (max) | 60 mA (max) |
| Supply current quad receiver* | 15 mA (max) | 40 mA (max) | 23 mA (max) |
| Propagation delay of driver | 1.7 ns (max) | 4.5 ns (max) | 11 ns (max) |
| Propagation delay of receiver | 2.4 ns (max) | 7.0 ns (max) | 30 ns (max) |
| Pulse skew (driver or receiver) | 400 ps (max) | 500ps (max) | N/A |
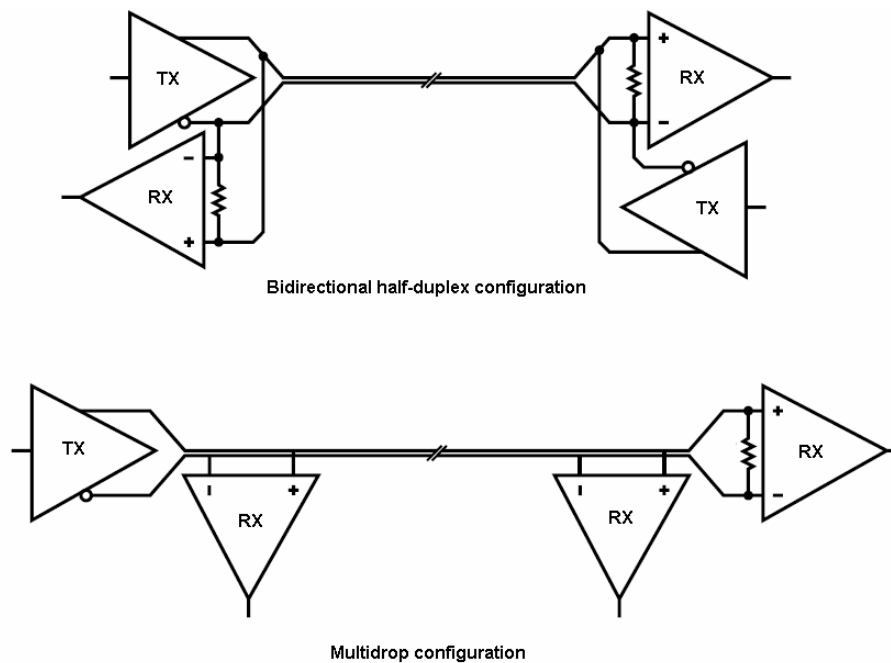


Figure 2.1　Bidirectional half-duplex and multi-drop configurations
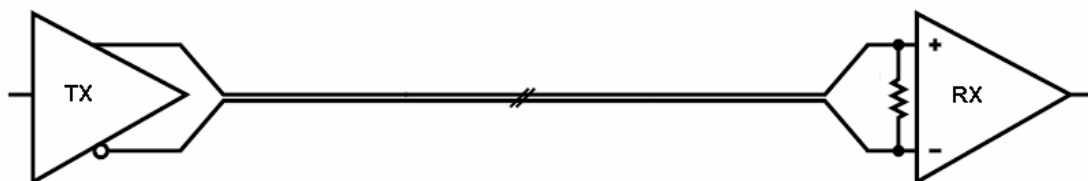


Figure 2.2　Basic point-to-point configuration
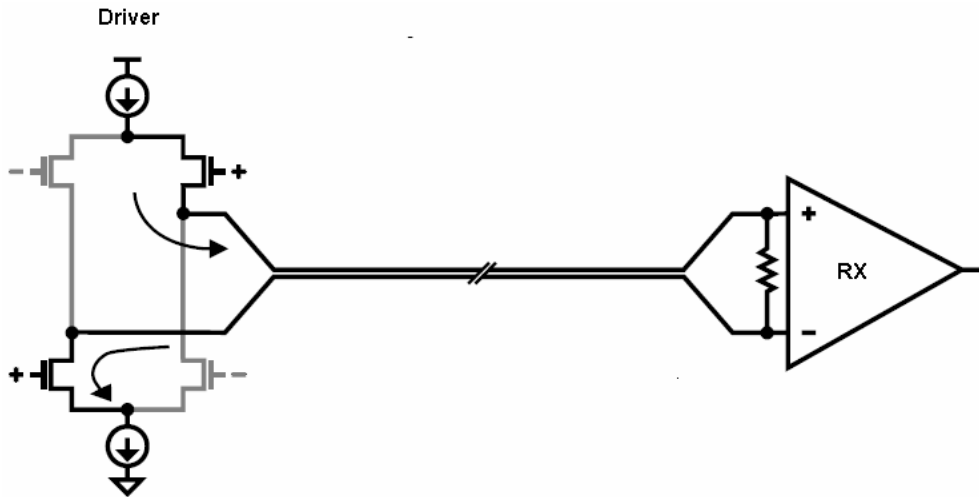
Figure 2.3 Basic topology of LVDS standard
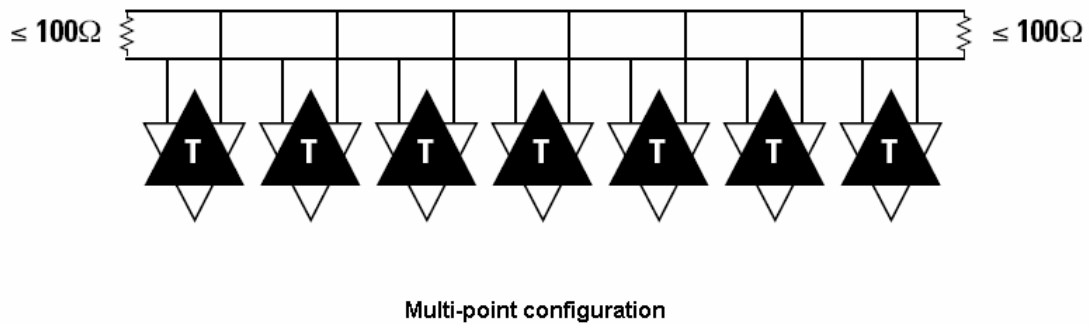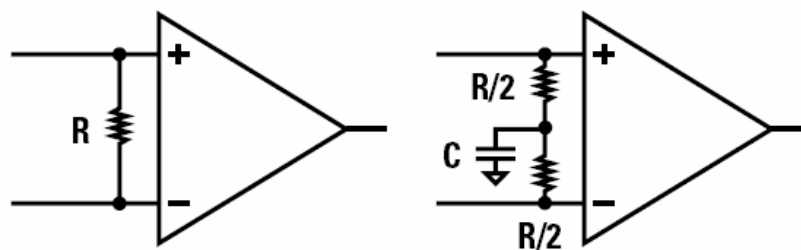


Multi-point configuration

Figure 2.4 Multi-point configuration



Common Differential Termination Schemes
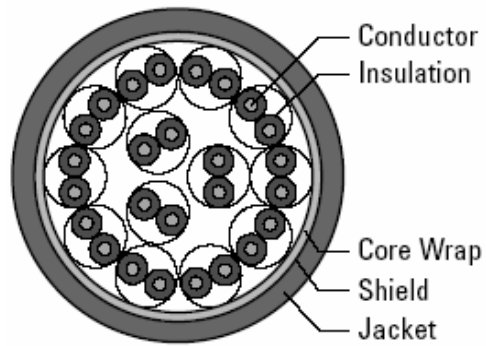
Figure 2.5 Termination configuration

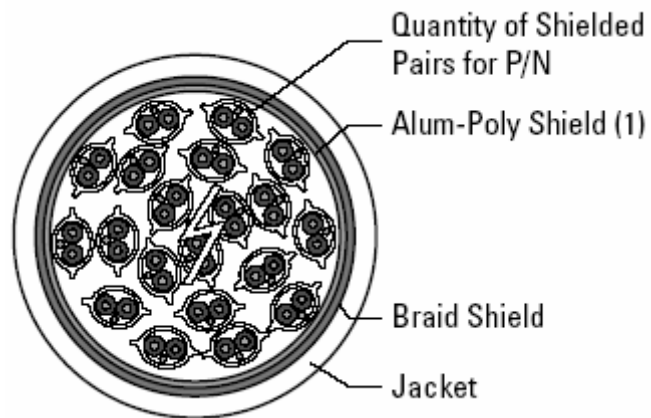Figure 2.6    Cross section drawing of a twisted pair cable



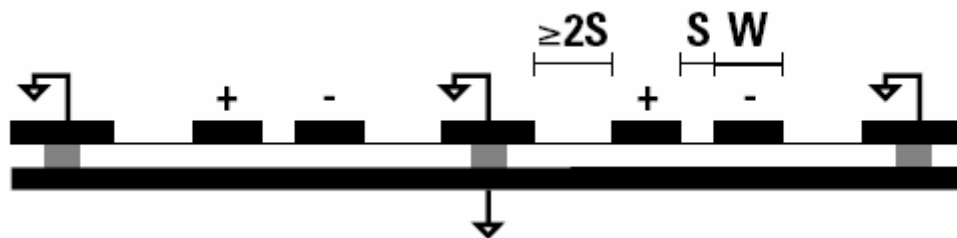Figure 2.7    Cross section drawing of a twin-ax cable



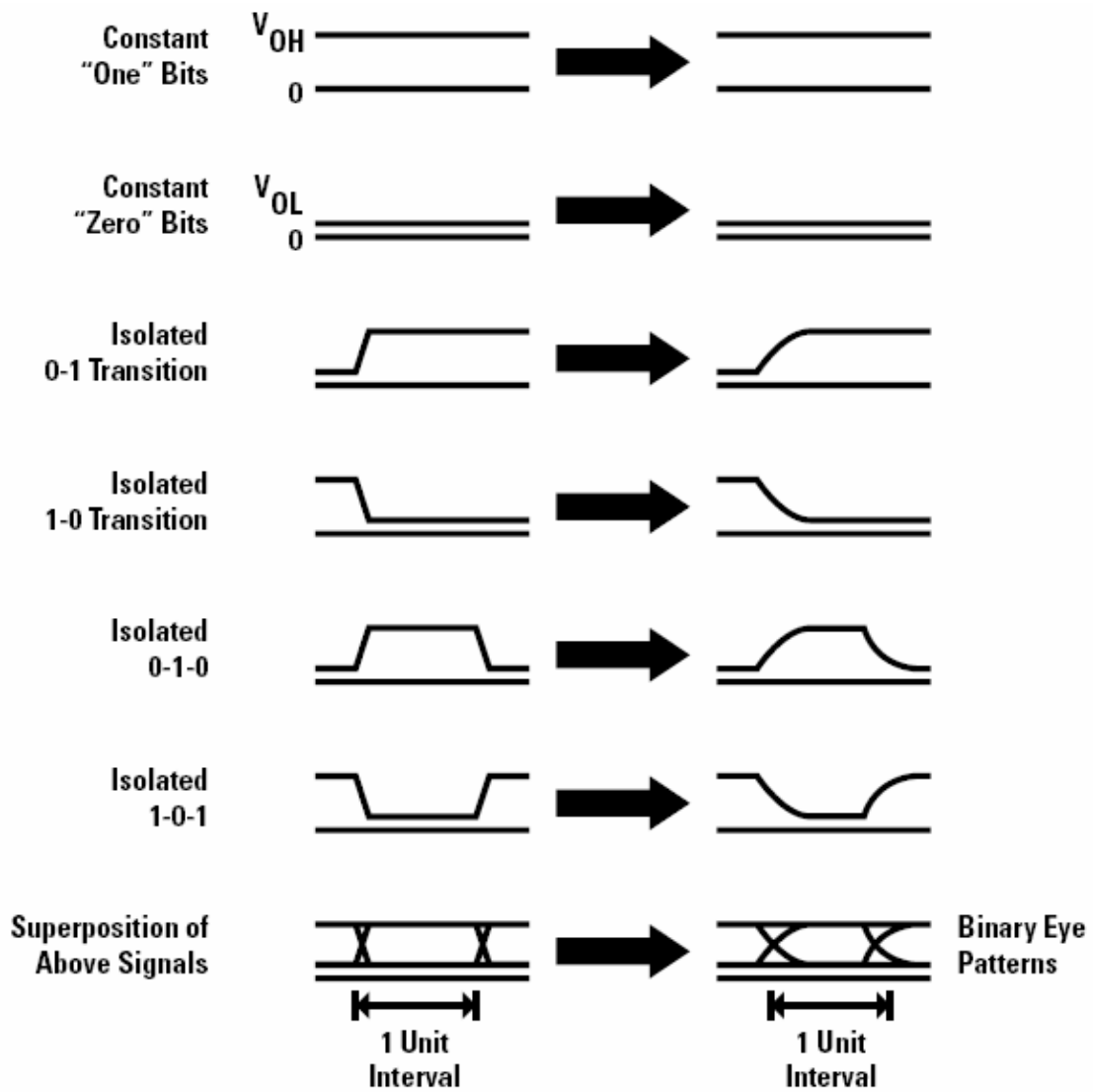Figure 2.8    Cross section drawing of a flex circuit
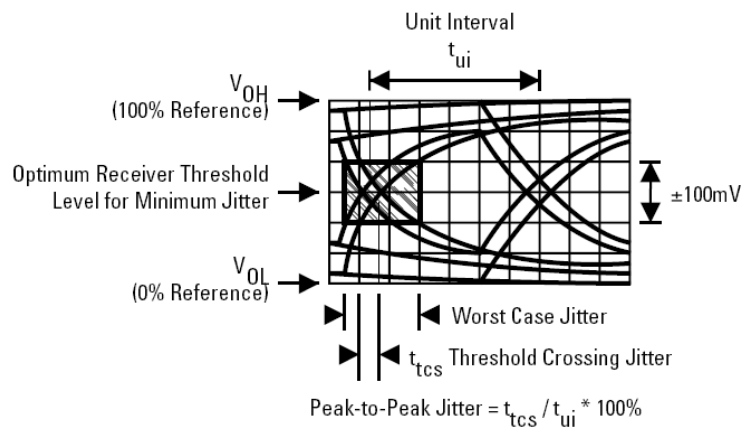
Figure 2.9　Cause of the eye pattern



Figure 2.10　Eye pattern of the NRZ

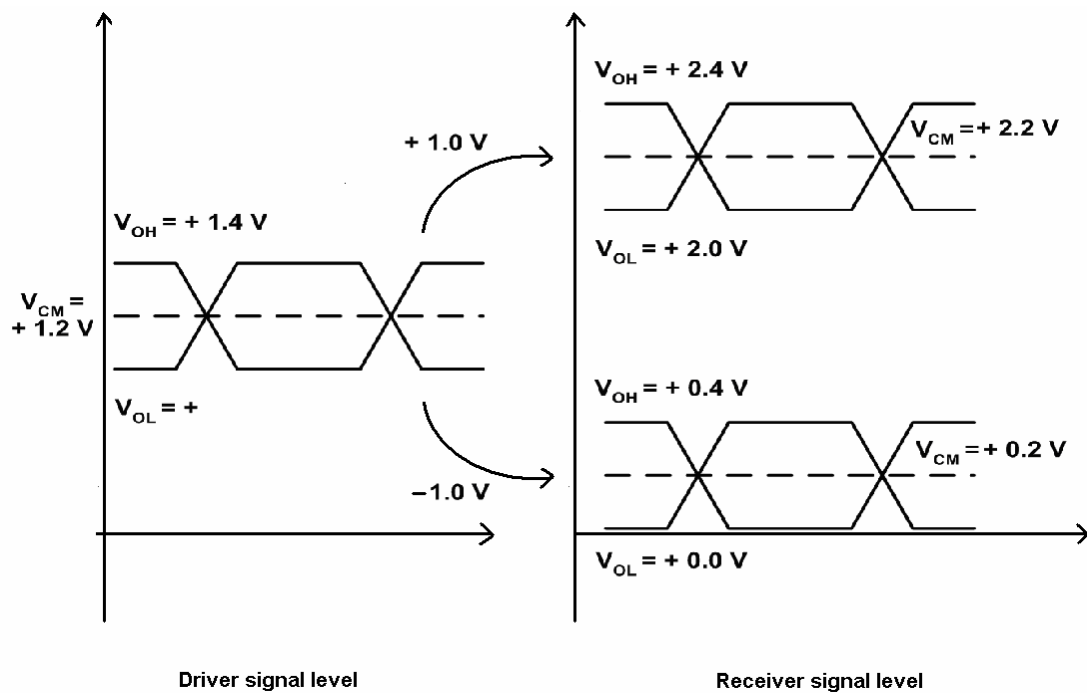Driver signal level     Receiver signal level

Figure 2.11  The signal level of LVDS standard

| PC/Computing | Telecom/Datacom | Consumer/Commercial |
| --- | --- | --- |
| Flat panel displays | Switches | Home/commercial video links |
| Monitor link | Add/drop multiplexers | Set top boxes |
| SCI processor interconnect | Hubs | In-flight entertainment |
| Printer engine links | Routers | Game displays/controls |
| Digital Copiers | | |
| System clustering | (Box-to-box & rack-to-rack) | |
| Multimedia peripheral links | | |

Figure 2.12  The scope of the LVDS applications

25

# Chapter 3

# Design of PLL

## 3.1 INTRODUCTION

Monolithic phase-locked loops, ever since their introduction, have found wide use in a number of applications. The commercial success of local area networks and the demand for higher data rates have recently increased the need for inexpensive high-frequency phase-locked loops. Data storage and RF data communications applications have also added to this need. Silicon CMOS is a natural technology for these circuits because the high production volume of digital CMOS circuits has significantly reduced the unit cost. Also, with advance of technology, the system operating speed is increasing. The high speed data transmission is transmitted between chips or even inside the chip. Therefore, the timing accuracy is an important issue in the high performance digital system. The PLL or DLL (delay-locked loop) is often utilized to reduce the timing skew. In addition, phase-locked loop is developed in such a delicate way that the integration with the digital block is possible. Therefore, the PLL is often one of the important blocks of a high performance system.

The serial-based data transmission is one of the solutions to the increasing demand of high speed data transfer. The clock-timed data signals are transformed to the phase-timed data signals and the better termination schemes are introduced to achieve better signal quality. The phase-locked loop is a traditional method to this transform. The multiple data bits are retimed to the phase edge and transmitted in a single clock cycle. Therefore, higher data rate is available in an inexpensive way.

However, DLL is sometimes a better choice in some application, for its

26

simplicity and better jitter performance. However, the lack of ability to frequency synthesis is major drawback of DLL. Therefore, PLL is more popular than DLL in many high performance systems.

Therefore, the PLL is the core of the design of serial-based data transmission. This chapter is devoted to this important circuit block.

## 3.2 DESIGN GOAL OF PLL

At first, because PLL is utilized in a variety of applications, the design of PLL is application specific. For example, requirement of PLL is very different in the purpose of de-skew and of frequency synthesis. The former is achievable even by DLL, a less complicate method. However, the latter is impacted by lots of factors, such as switching speed, frequency range, accuracy, etc.

Therefore, the topology of this transmitter is shown as figure 3.1. The seven parallel data signals are retimed to a single data signal by parallel-to-serial converter. The driver then signals the serial-based data through the channel, like PCB traces or cable lines. Because the targeted data rate is about 1.2 Gb/s, the PLL required is a relative simple and relax. The operating frequency is around 200 MHz. Therefore, a simpler circuit implementation can be chose.

## 3.3 THE BASIC ARCHITECHURE OF PLL

The basic architecture of PLL is shown in figure 3.2 [11]. This is a conceptual plot of this so-called "Charge-pump PLL", which is a popular configuration of PLL. However, the PLL will not work properly under the PVT deviation conditions. Therefore, the self-bias technique is employed to combat with this difficulty [12].

The technique of self-bias is employed in this PLL. It can provide a bandwidth

that tracks operating frequency. This tracking bandwidth can in turn provide a very broad frequency range, minimizing the supply and substrate noise induced jitter with a high input tracking bandwidth. Besides, fixed damping factor and input offset phase error cancellation are also advantage of this architecture.

At first, the phase-frequency detector (PFD) senses the phase difference between CLK_ref and the feedback signal, and then produces signals to determine whether the current source or the current sink is on. The loop filter transforms this current into voltage, which is used to control the voltage control oscillator (VCO). The loop filter is $2^{nd}$ order here, the $C_2$ is utilized for the purpose of filtering the high frequency signals, which will disturb the VCO and corrupt the timing accuracy. Then the output of VCO is feedback to the PFD through a frequency divider. This divider is included to achieve the important characteristic of PLL, frequency synthesis.
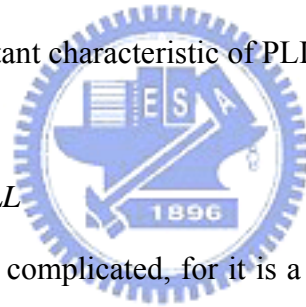
### 3.3.1 The basic analysis of PLL

Analysis of PLL is often complicated, for it is a mixed-signal system. The input signal is sampled at PFD, and transform to analog signal through loop filter and VCO. Besides, the frequency divider is usually constructed as a simple digital counter. Therefore, discrete and continuous analysis is required to accurately predict the behavior of PLL. Which makes the problem even more complicated is that PLL is a system focus on the timing information not a normal voltage or current signal. Consequently, there exists some approximate analysis of PLL, which may help designer to achieve the basic property of PLL, such as stability, settling, noise property, etc.

The classic analysis is shown in figure 3.3, which is a continuous, phase space conceptual plot. This model will be reasonable, for the loop bandwidth of PLL is generally lower than the operating frequency about 10 times, which is often true for

most cases.

As shown in figure 3.3, after some algebraic manipulation, the equation is as below:

$$\frac{\varphi_{out}}{\varphi_{in}} = H_s(s) = \frac{2\zeta\omega_n S + \omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2} \tag{3.1}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{vco} C_1}{N}} = \frac{1}{2}\sqrt{K\tau_1} \tag{3.2}$$

$$\omega_n = \sqrt{\frac{I_p K_{vco}}{NC_1}} = \sqrt{\frac{K}{\tau_1}} \tag{3.3}$$

$$K = \frac{I_p K_{vco} R_1}{N} \tag{3.4}$$

$$\tau_1 = C_1 R_1 \tag{3.5}$$

The Eq. (3.4) is approximately the unit-gain frequency of the open loop frequency response.

$$\text{Open loop frequency response} = I_p K_{vco}\left(\left(R_1 + \frac{1}{SC_1}\right) // \frac{1}{SC_2}\right)\frac{1}{NS}$$

$$\approx I_p K_{vco}\left(\left(R_1 + \frac{1}{SC_1}\right)\right)\frac{1}{NS}$$

$$\approx \frac{I_p K_{vco} R_1}{N}\frac{SC_1 + \frac{1}{R_1}}{S^2 C_1} \tag{3.6}$$

As we will see later, for the consideration of stability, the value of $C_2$ and $R_1$ can not be too large. Therefore, the approximate in Eq. (3.6) should be reasonable for general cases. This relation between the close loop response and the open loop response can be shown in figure 3.4. The $\omega_n$ is the geometric mean of the zero and the unit-gain frequency of the open loop frequency response. Therefore, in log scale, this plot shows $\omega_n$ is at the middle of zero and the unit-gain frequency.

Besides, the damping factor $\zeta$ is important in the settling property of PLL. The

small $\zeta$ means the change in input phase error will induce a large peaking in the output phase, which is always not desired for most application. The clock and data recovery circuit (CDR) which utilizes PLL as a timing regenerator will suffer from this characteristic. Besides, because the data transmission may through a long distance, like optical system, sometimes circuits as repeaters will be introduced to lessen the impact of channel loss. The amount of peaking in the phase domain must be well controlled, or the error-less data recovery will become very difficult in such case. In most cases, the $\zeta$ is often chosen to be larger than one. Sometimes, the value will be vary large, which makes the loop filter inside the chips is not acceptable.

### 3.3.2 The stability of PLL

However, as a general problem in all kinds of feedback system, the stability problem should deserve some attention. Figure 3.4 also shows the phase response of the open loop PLL. The zero is introduced to offer larger noise margin and improve the stability property. However, the loop filter is $2^{nd}$ order, which makes stabilizing the total feedback system a more complicated problem. Since PLL may require a as wide operating bandwidth as possible, the $K_{vco}$ value is sometimes vary larges, such as several hundred MHz per volt. The zero created by the $C_1$ and $R_1$ pair improves the stability, but every time the charge pump turns on, the voltage jump on $R_1$ is unavoidable. Hence, a second capacitor, $C_2$ is introduced. The value of $C_2$ should suffer from the tradeoff relation between stability and timing accuracy. The impact of $C_2$ can be seen as below:

$$PM = \tan^{-1}\frac{\omega_t}{\omega_z} - \tan^{-1}\frac{\omega_t}{\omega_{p2}}$$
$$\frac{d(PM)}{d\omega} = 0$$
$$\omega_t = \sqrt{\omega_z\,\omega_{p2}} \approx \frac{I_p K_{vco} R_1}{N}\frac{C_1}{C_1+C_2}$$

(3.7)

30

The Eq. (3.7) also shows that the not only the phase response is changed but also the amplitude response is changed. The unit-gain frequency is smaller than Eq. (3.4). In general practice, the position of $\omega_z$, $\omega_t$, $\omega_{p2}$ is often chosen to be four times apart. In such case, the phase margin is about 60° and the damping factor is one. The phase margin is enough for most application, and it is suitable for the design of LVDS transmitter. Also, the damping factor of one indicates the settling behavior of PLL will not be a severe problem.

Based on the equation given above, the parameter of PLL can be chosen. At first, the PLL specification is examined, and the operating frequency range will determine the rough value of $K_{vco}$. The value of $I_p$ is chosen to be around 100μA to 1mA for an off-chip loop filter. If an on-chip filter is employed, decrease the value of $I_p$ so that the reasonable trade off between chip area and charge pump current could be reached. Depending on the application, the reasonable value of N can be chosen. The frequency synthesis property of PLL may introduce few problems. However, for the LVDS driver, the frequency switching is not a necessary function. The unit-gain frequency of open loop should be about 1/10 of the operating frequency; the reason will be seen latter.

Now, the basic parameter is ready. The loop filter is the major problem of the design. As shown above, the value of $R_1$, $C_1$, $C_2$ can be determined after some algebraic manipulation. This is shown as below:

$$R_1 = \frac{N}{I_p K_{vco}} \omega_t$$

$$C_1 = \frac{4 I_p K_{vco}}{N \omega_t^2}$$

$$C_2 = \frac{I_p K_{vco}}{4 N \omega_t^2} \tag{3.8}$$

The value of $C_2$ above is an upper limit. In general, the $C_2$ will be less than 1/20 of $C_1$. Therefore, the PLL analysis can be simplified.

*3.3.3 The discrete property of PLL*

However, as described at first, the PLL can not be analyzed without assumptions of small phase error, limited operating frequency range. The continuous linear analysis is a simplified model for intuitively understanding. However, in this model, the operating frequency has no effect, which is not practically true. The ratio between operating frequency and the loop bandwidth can not be too large, or the phase error will not be eliminated as expected from the PLL. The reason is mainly from the ignorance of the mixed-signal property of PLL [13], [14]. The digital sampling property of PFD and charge pump will introduce extra phase shift. Besides, the digital frequency divider will also degrade the phase margin of the total feedback system. Therefore, by this approximated model, the parameter can be chosen, but extra verification is needed.

However, in order to determine the optimal parameter of PLL, the device level simulation will be a time-consuming work. Therefore, a behavior model for such mixed-signal PLL is built. This model can be seen in figure 3.5. The sampling property of PFD is modeled by multiplying the phase error with a narrow width, unity height pulse. And this signal will control the current source to drive approximately equal charge into the loop filter. The voltage on the loop filter controls VCO and the output of VCO is feedback to the PFD trough the divider. This model can help us to determine the rough parameter to reduce the time required for simulation.

The z-domain stability problem can be shown in the figure 3.6. Besides, the limit of operating frequency for a specific PLL can be shown as below:

$$K\tau_1 < \cfrac{1}{\cfrac{\pi}{\omega_{in}\tau_1}\left(1+\cfrac{\pi}{\omega_{in}\tau_1}\right)}$$

$$\frac{\omega_{in}}{K} > \frac{\pi}{2}\left(1+\sqrt{1+\frac{1}{\zeta^2}}\right)$$

(3.9)

These equations give us a simple relation to consider the limit of PLL. Besides, the loop delay induced extra phase shift can be added to the design procedure easily.

### 3.3.4 The noise property of PLL

The noise property of PLL has been surveyed for many years and it is not fully solved for the progress of technology and the complexity of applications. More and more applications demands better PLL for its property of easy integration with the digital core and varieties of functionality. However, since PLL is such a complicate system, a fully predictable model is not available. Compared with the power noise or ground noise, the electric noise of the device, which is often ignored in traditional analysis, is no longer ignorable.

The noise in the PLL can be analyzed in figure 3.7. For practical reasons, all the building blocks like PFD, LPF, VCO and frequency divider is made by the transistor. Therefore, the electric noise always intrudes some error, deviating from ideal case. The noise contributing from each block can be shown as below:

$$\frac{\varphi_{out}}{\varphi_{in}} = H_s(s) = \frac{2\zeta\omega_n S + \omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2} \tag{3.10}$$

$$\frac{\varphi_{out}}{\varphi_{n-pfd}} = \frac{2\pi}{I_p} \frac{2\zeta\omega_n S + \omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2} \tag{3.11}$$

$$\frac{\varphi_{out}}{\varphi_{n-lpf}} = K \frac{S}{S^2 + 2\zeta\omega_n S + \omega_n^2} \tag{3.12}$$

$$\frac{\varphi_{out}}{\varphi_{n-vco}} = \frac{S^2}{S^2 + 2\zeta\omega_n S + \omega_n^2} \tag{3.13}$$

$$\frac{\varphi_{out}}{\varphi_{n-div}} = -\frac{2\zeta\omega_n S + \omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2} \tag{3.14}$$

From the equations above, equations (3.10), (3.11), (3.14) imply a low-pass

property of the noise source at input, PFD and frequency divider. (3.12) and (3.14) suggests that noise at VCO is filtered with high-pass property and noise at LPF is filtered with band-pass property. Those noise characteristic will set different conditions for different applications. Besides, the periodic reset property of the digital PFD can reduce the impact caused by the 1/f noise.

The noise analysis can be done by summing all the power spectrums induced by those building blocks. However, the noise source at input and the VCO is generally more important than others. Thus, (3.10) and (3.14) is generally the basic equation for the PLL noise analysis. Due to these two equations, a trade-off relation is suggested. The higher loop bandwidth will filter the noise at VCO severely and the input noise will be passed to the output. However, for general cases, the input source is often a crystal oscillator, which is a relatively clearer source than VCO. Therefore, higher loop bandwidth is preferred. The noise at output is mainly affected by the noise at VCO. However, the loop bandwidth is limited by the stability problem, which is addressed in the sector 3.3.2.

## 3.4 THE BUILDING BLOCKS OF PLL

### 3.4.1 The phase-frequency detector (PFD)

For some application, the phase detector (PD) and the frequency detector (FD) are utilizing separately. The PD can adjust the phase difference but the frequency error can not be distinguished from the phase difference for the PD. Therefore, a FD is required for such case. Besides, the PD sometimes requires 50% duty-cycle inputs, or a steady phase offset will be introduced. However, for our application, the digital PFD is appropriate for its simplicity.

The PFD is a circuit block which senses the phase and frequency difference

between its two inputs, $\varphi_{in}$ and $\varphi_{feedback}$. A linear PFD is capable of generating a voltage level proportional to the phase difference and frequency error. The basic block diagram of PFD is shown in figure 3.8. As shown in the figure 3.8, the rising edge of the inputs will define the phase error. At first, the $F_{in}$ is form low to high and the UP signal is pulled high. Then, as long as the $F_{feedback}$ goes high, the down signal will be pulled high and reset UP and DOWN signals at the same time. The functionality can be shown as state diagram in figure 3.9. The rising edge of input will change the state. Also, the general characteristic of the PFD can be shown in the figure 3.10, which shows the characteristic curve of the PFD, combined with charge pump (CP) and the low-pass filter (LPF). Form figure 3.10, we can see the reason that PFD can be the PD and FD at the same time. Since the frequency error will constantly increase the phase error, which will be sensed by the PFD. Therefore, a positive area at the figure 3.10, means a increasing voltage level is resulted. The control voltage of VCO is higher and the frequency of the output steps up. Hence, the PFD can generate a voltage level proportional to the phase error and frequency error.

Ideally the linear PFD should generate any voltage level for any phase difference. However, for a small phase error, the PFD can't work properly, which results in the dead zone region in the characteristic curve. The dead zone region is an undetectable phase error for the PFD, which is highly undesirable for the PLL for accumulating timing error. However, the reason of dead zone is that a small phase error will change the state quickly, which equivalently requires fast switching of the CP. The CP can not be activated unless enough turn on time is provided. Hence, a general solution to this problem is to insert the delay cell to increase the turn on time for the CP. The delay cell may increase the sensibility of the PFD but narrower operating frequency will be the disadvantage. This drawback is mainly because the extra delay will result in a longer recovery time for the PFD to sense the next event. The maximum operating

frequency can be shown as below:

$$F_{op\text{-}max} = \frac{1}{2T_d}$$ 
(3.15)

where $T_d$ is the delay time of the delay cell.

The circuit implementation is shown in the figure 3.12, which is based on the TSPC DFF. Figure 3.11 is the basic TSPC DFF. The modified DFF is utilized. The D-input is replaced by the reset-pin and extra delay cell for the dead zone is not required, for its internal delay. The characteristic of the PFD can be shown in the figure 3.13. Therefore, the dead zone is not a severe drawback of the PLL.

*3.4.2 The charge pump (CP)*

The PFD generate two signals, UP and DOWN, which switches the CP. The current pump into the LPF is controlled by this mechanism. If the UP signal is longer, the net current flowed into the LPF is positive, which results in a higher control voltage for the VCO.

A simple differential type CP is used. The circuit can be shown in figure 3.13. This CP has two bias currents. One is a dynamic bias current, which is control by the bias-generate circuit. The other is a small constant bias current, generated by a self-bias circuit.

The purpose of the dynamic current is based on the technique of self-biasing. The self-biasing can be a powerful technique under the consideration of process, temperature and supply voltage. Self-biasing is basically capable of removing process deviation and environmental interfere and it is very important for the design of PLL, since timing accuracy is too critical to suffer any disturbances. Besides, this technique also provides the capability of bandwidth tracking. The self-biasing virtually make the PLL choose the best conditions for its operation under variation of environment and parameter. The self-biasing technique can be effective in competing with the power

supply noise and substrate noise. Also, fixed damping factor and bandwidth tracking can be a important advantage for higher input frequency tracking range. Therefore, a dynamic current is generated from the bias-generate circuit, which should be proportional to the control voltage of VCO. This process includes the input frequency as an important parameter in the design of PLL. Therefore, extra validation for the determination of PLL parameter is required.

However, as we can see later, the start up circuit for the self-biasing technique is required. Since low control voltage level will not activate the VCO to oscillate, and the dynamic current of CP can not effectively pump the voltage on LPF. Hence, the self-biasing technique will not work properly for initial condition. The general method is including the start up circuit in the bias-generate circuit. Here, a small constant current in the CP will help the self-biasing mechanism start up. Also, this small current may be helpful when low control voltage generates small dynamic current. It can help PLL to track the phase and frequency more quickly.
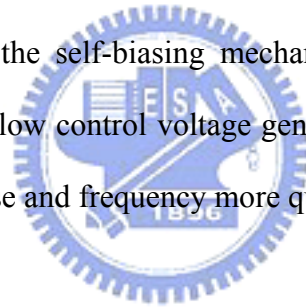
### 3.4.3 The low pass filter (LPF)

The LPF have two important properties. One is to extract the average value for the output of PFD, and the other is to stabilize the close loop PLL response [15]. As shown in the figure 3.15, the output of the PFD is not a smooth curve. Hence, the high frequency terms of the output will disturb the VCO severely. The low-pass characteristic of the loop filter is utilized to suppress the reference spurs. In addition to this property, the loop filter is an important and critical part of the design of PLL. The loop filter should introduce a zero for the problem of loop stability. However, because of the extra zero, high frequency terms can not be filtered by loop filter. It will cause the noise in the PFD and VCO to appear in the output. Therefore a second order loop filter is utilized to insert another pole for the high frequency attenuation.

This is shown in the figure 3.16.

However, the insertion of the second pole will complicate the analysis of PLL. Therefore, by setting $C_1 > 20 \times C_2$, the PLL can be analyzed as a second order loop not a third order loop.

The characteristic of the second order loop filter can be derived as below:

$$LPF(s) = \frac{K_{lpf}(s + \omega_z)}{s(1 + s/\omega_p)} \tag{3.16}$$

$$\omega_z = 1/R_1 C_1 \quad \omega_p = \omega_z(1 + C_2/C_1)$$
$$K_{lpf} = \frac{R_1 C_1}{C_2 + C_1} \tag{3.17}$$

### 3.4.4 The bias-generate circuit

The bias-generate circuit is the circuit block which dynamically adjusts the bias condition of the CP and VCO. With different operating frequency, different bias condition should be set. The control voltage of the VCO is the parameter to set the bias condition. Since PFD can adjust the frequency error, the charge pump will pump proper amount of charge into the LPF. Therefore, the control voltage through LPF should be proportional to the operating frequency. This bias generator circuit is not a process independent circuit. The purpose of bias-gen. is to generate appropriate bias condition for PLL. The performance of the PLL will be stabilized by the self-bias technique. This technique will provide a proper condition for operation.

The bias-generate circuit is shown at figure 3.17. The circuit is a simplified version. As shown in figure 3.18, the complex bias-generate circuit should have better performance. However, its complexity is relatively higher and the feedback loop inside the bias-generate circuit also require extra care. The stabilization of the circuit sometimes requires additional capacitance to insert zero. Therefore, the area may be

38

larger. Also, with stabilization of the loop, the bandwidth of the loop may not enough to track the high frequency supply noise. However, the simplified bias-generate circuit can be a simple and low-cost solution for our simple PLL. The noise from the supply voltage can be tracking roughly. Also, the complexity of the circuit is relatively simple, and the stabilization is not required inside the circuit block. Therefore, the extra capacitance required in figure 3.18 is not necessary. The area should be smaller, which results in low-cost solution.

### 3.4.5 The voltage controlled oscillator (VCO)

In this PLL, a voltage controlled ring oscillator is employed. The oscillator frequency is proportional to the bias voltage. The fundamental building block is shown in the figure 3.19. The voltage controlled delay cell contains a source-coupled pair with symmetric load, which consists of diode-connected NMOS devices. Since low jitter design for PLL is preferred, delay cell, which has low sensitivity of supply noise and substrate interfere, is preferred. The delay cell utilized here can improve the performance under noisy condition.

Also, the noise characteristic of VCO has been studied. For a differential type delay cell, the impact induced by the device electric noise is not necessarily better than single-ended delay cell. Since the device electric noise is not ignorable, the noise in the differential type delay cell may be independent for each half circuit. Hence, larger noise may be appeared.

Besides, the noise in the VCO can not be analyzed accurately as a simple linear-time-invariant system. It has been shown that the noise property in the VCO is a liner-time-variant system. This property can be shown as figure 3.20. The device electric noise is model as a simple impulse. For typical delay cell, the amplitude limiting mechanism will be an important property of the VCO. As shown in the figure

3.20, the noise impulse interferences the VCO at different time. If the noise corrupts the signal at the zero-crossing point, the maximum phase error was introduced in the output signal. However, if the noise interferences the signal at the highest point, the amplitude limiting mechanism will reduce the impact heavily. Hence, the phase error caused by this case will be minimized. Therefore, the time-variant property of VCO is shown clearly. Also, the linear property is proved a valid model even with time-variant characteristic. Besides, from the discussion, the VCO delay cell should be designed to have good symmetric characteristic. The diode connected NMOS device can improve the linearity of the delay cell. Hence the symmetric load utilized here can improve the jitter performance of the VCO.

As we can see, in order to minimize the jitter of the PLL, the VCO delay cell should be well designed. The PMOS source-coupled pair is employed for the consideration of the body effect. The removal of the body effect will reduce the uncertainty from the differential pair. A seven stage VCO is utilized in the PLL. The characteristic of the VCO is shown in figure 3.21. The $K_{vco}$ is about 250 MHz/V.

The output of the VCO is not full swing and an extra circuit is included. The differential-to-single-ended converter is shown in figure 3.22. The converter is composed by two differential amplifiers, which will amplify the small swing signal at VCO output. Then a inverter is employed to ensure full swing signal. A 50% duty cycle waveform is generated. The differential pair is biased by a simple self-bias circuit, which is shared all over the chip.
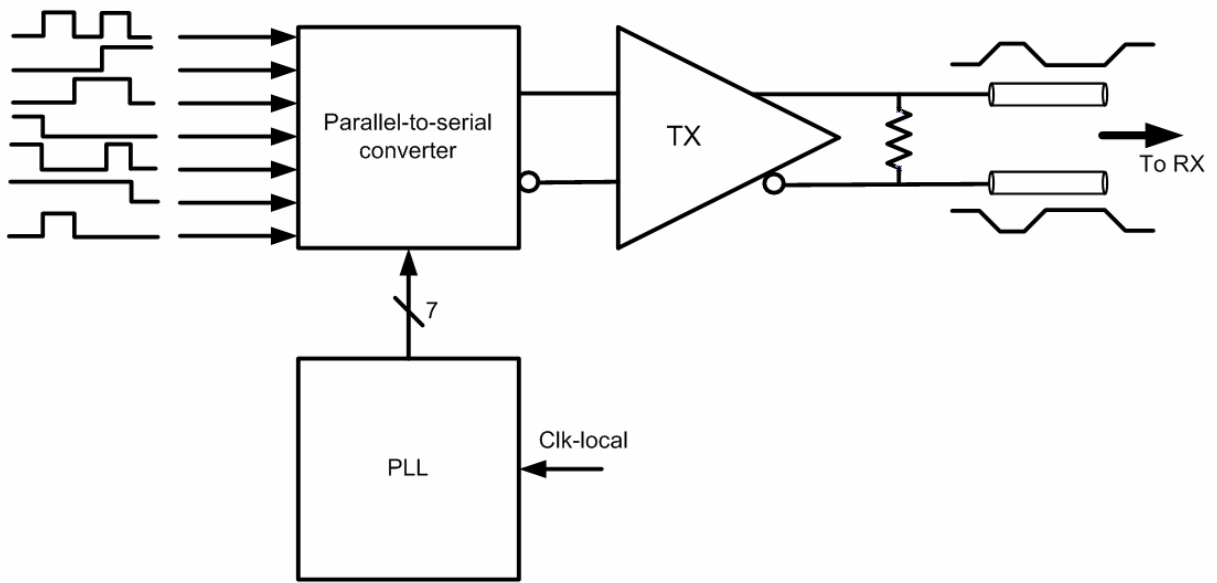
Figure 3.1    The topology of this transmitter
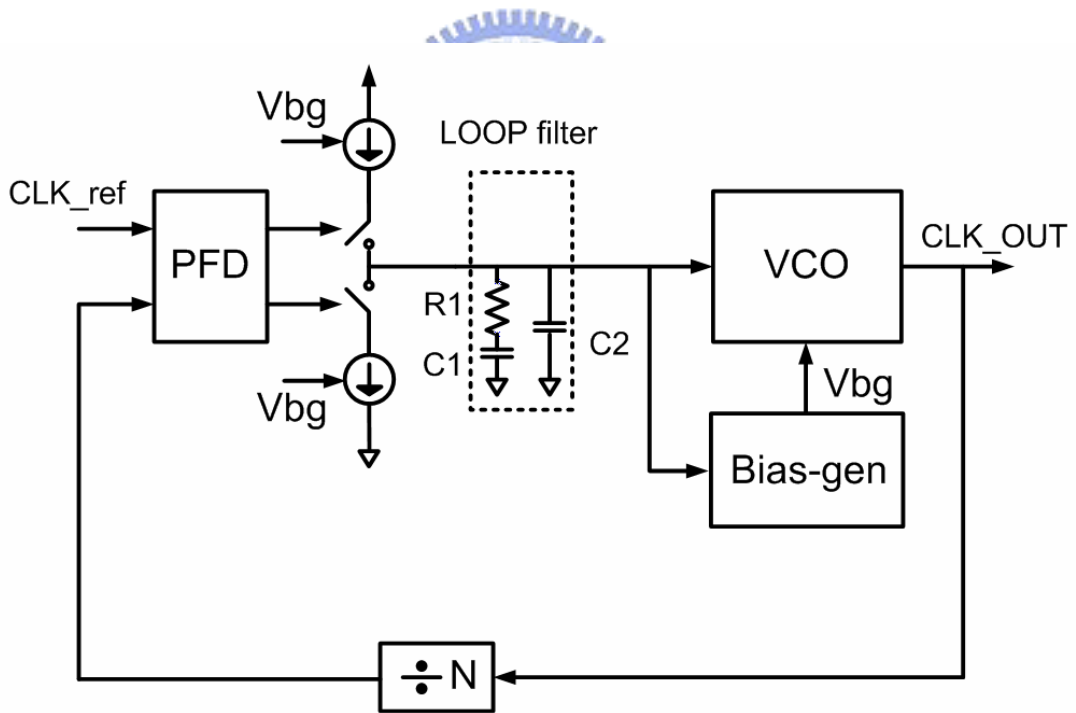


Figure 3.2    The basic architecture of PLL with self-bias technique
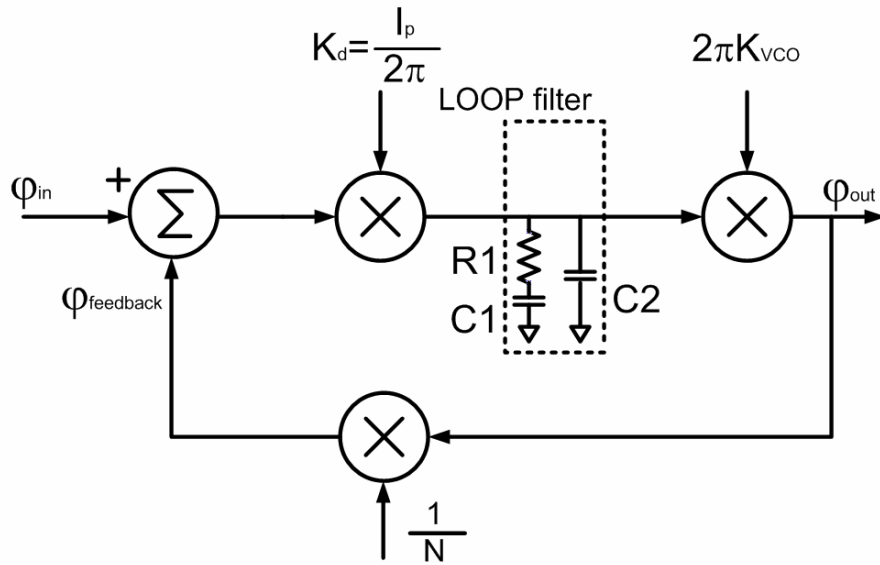
Figure 3.3    The simplified continuous approximate plot of PLL
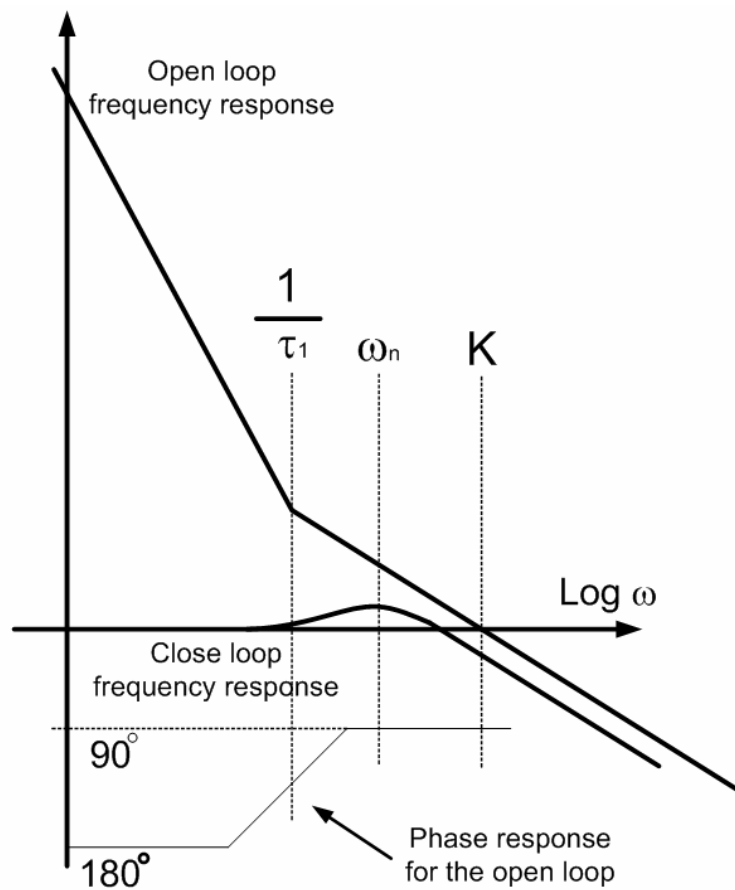


Figure 3.4    The relation between open loop frequency and close loop response
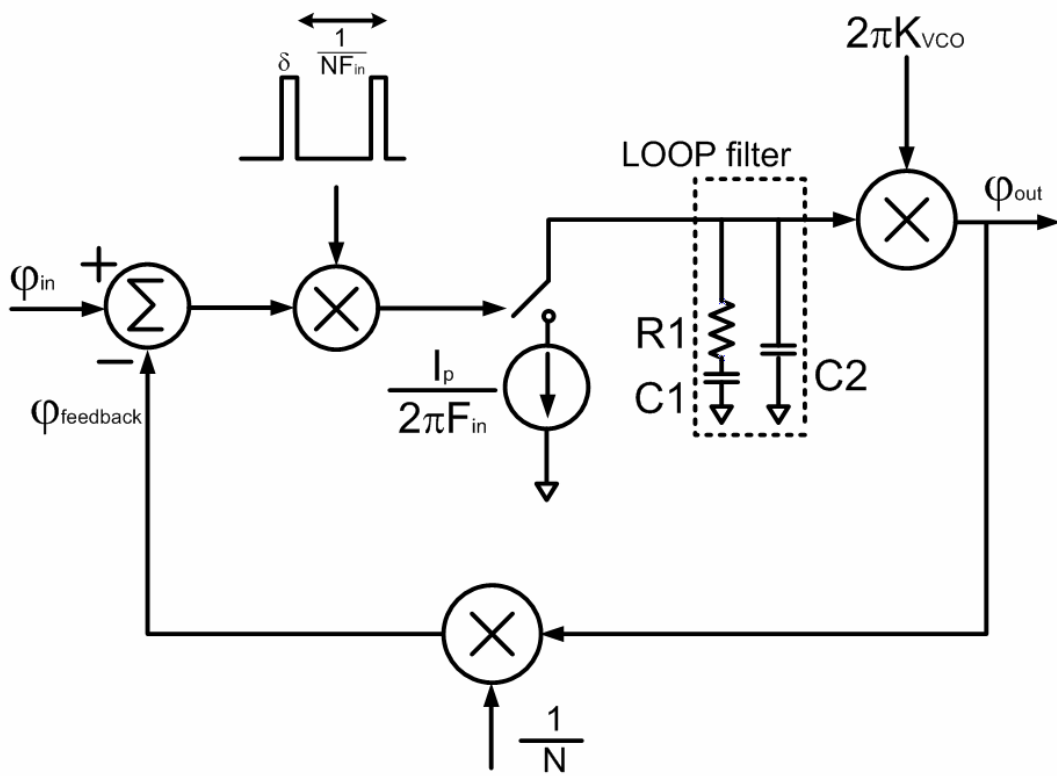
Figure 3.5    The mixed-signal model of the PLL
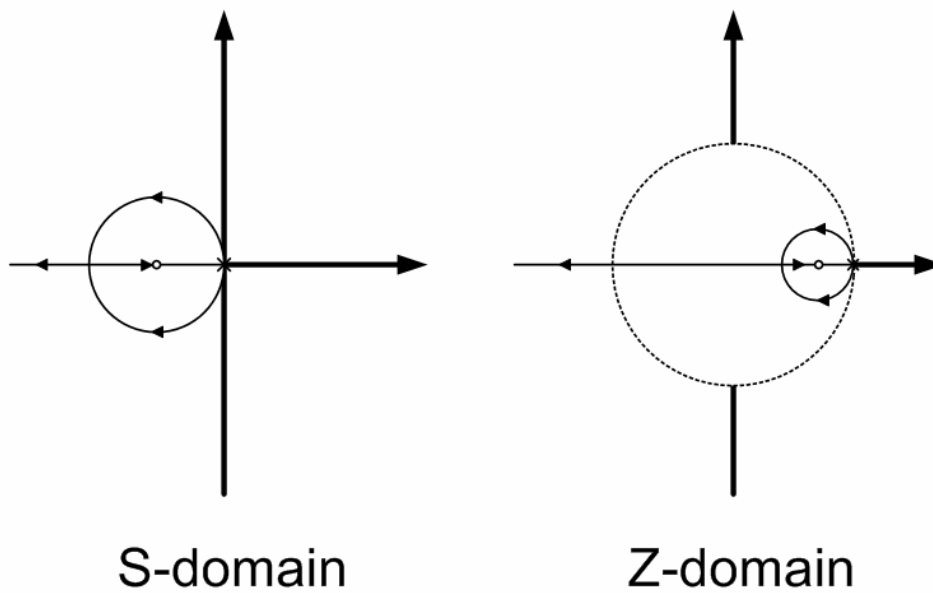


Figure 3.6    Root-locus plot for s-domain and the z-domain
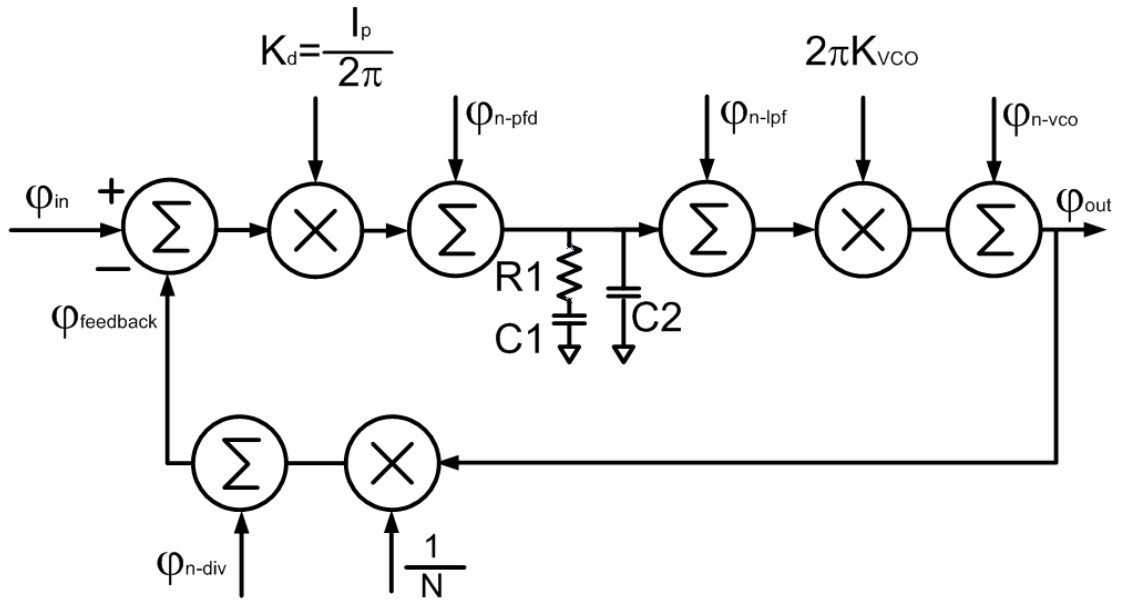
Figure 3.7    The noise in the PLL
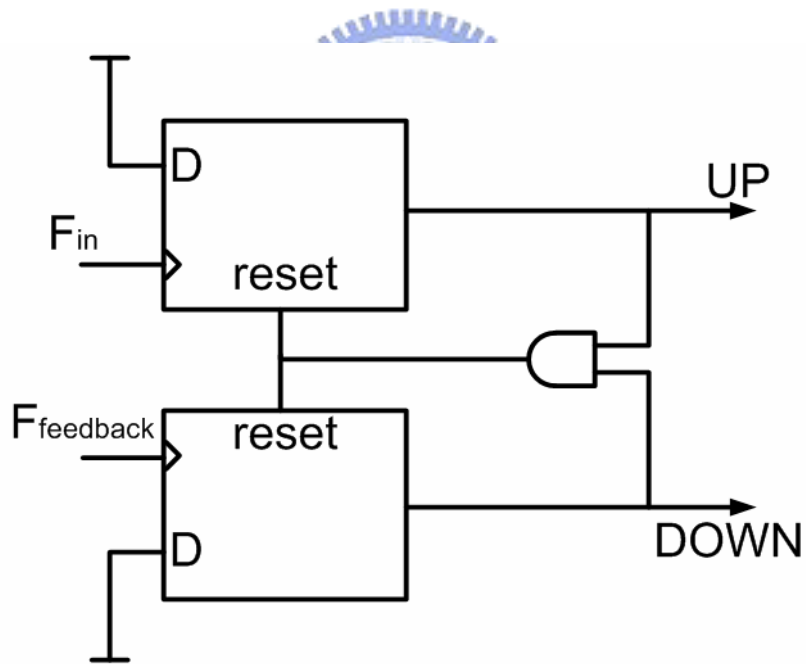


Figure 3.8    The block diagram of PFD
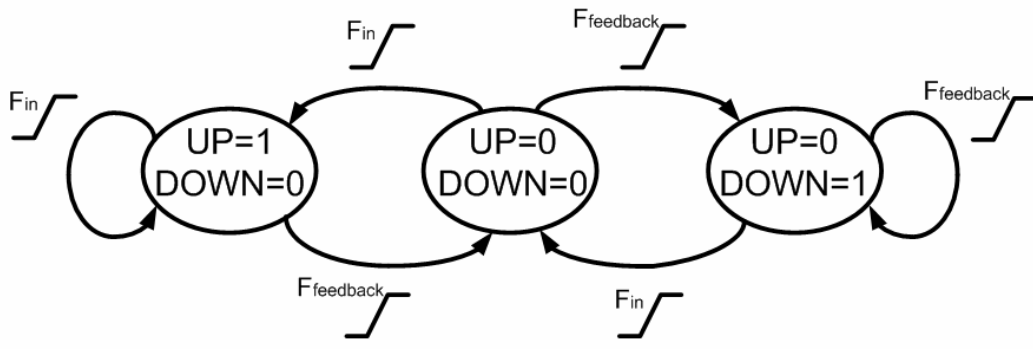
Figure 3.9 The state diagram of PFD
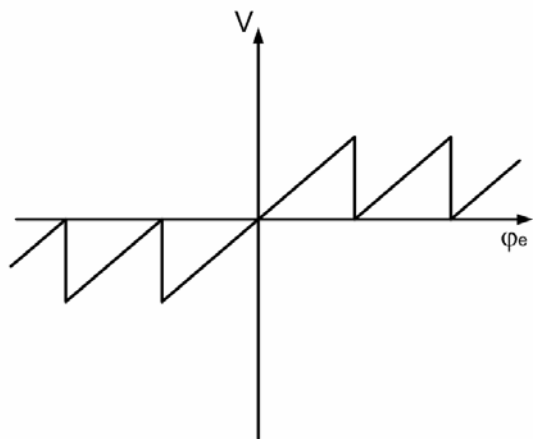


Figure 3.10 The characteristic curve of PFD
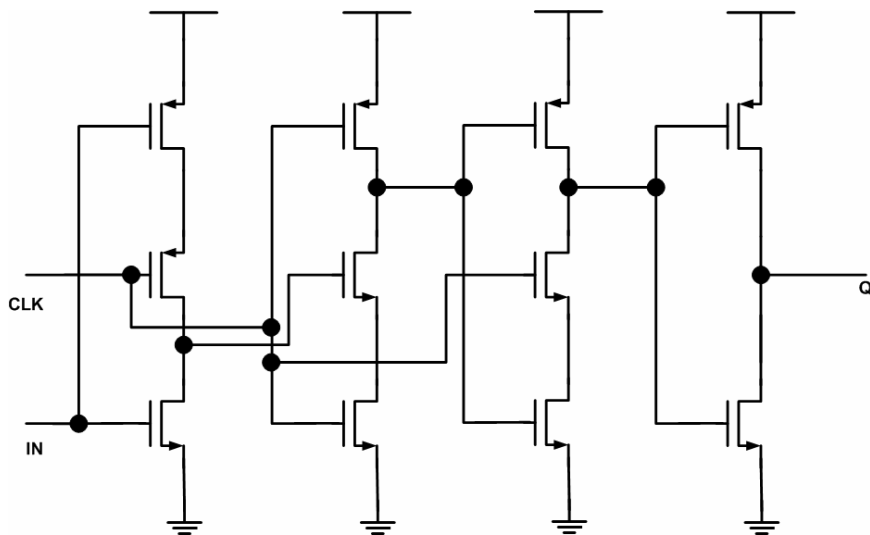


Figure 3.11 The TSPC DFF
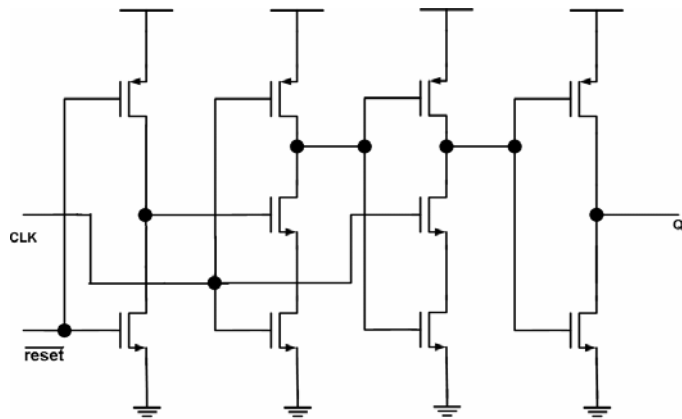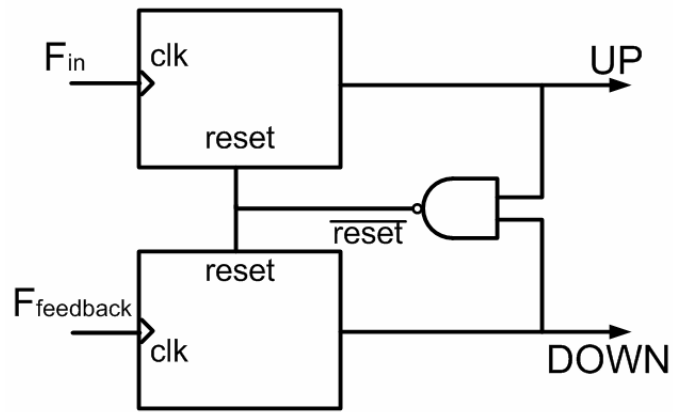
Figure 3.12    The circuit implementation of PFD
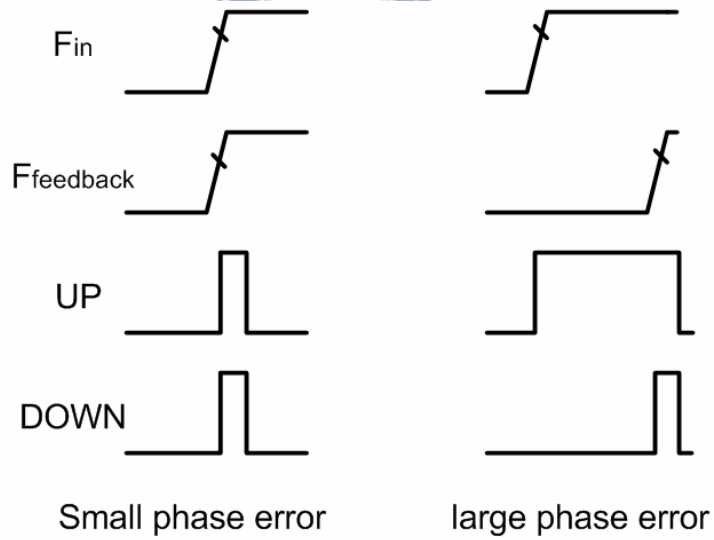


Figure 3.13    The characteristic of PFD
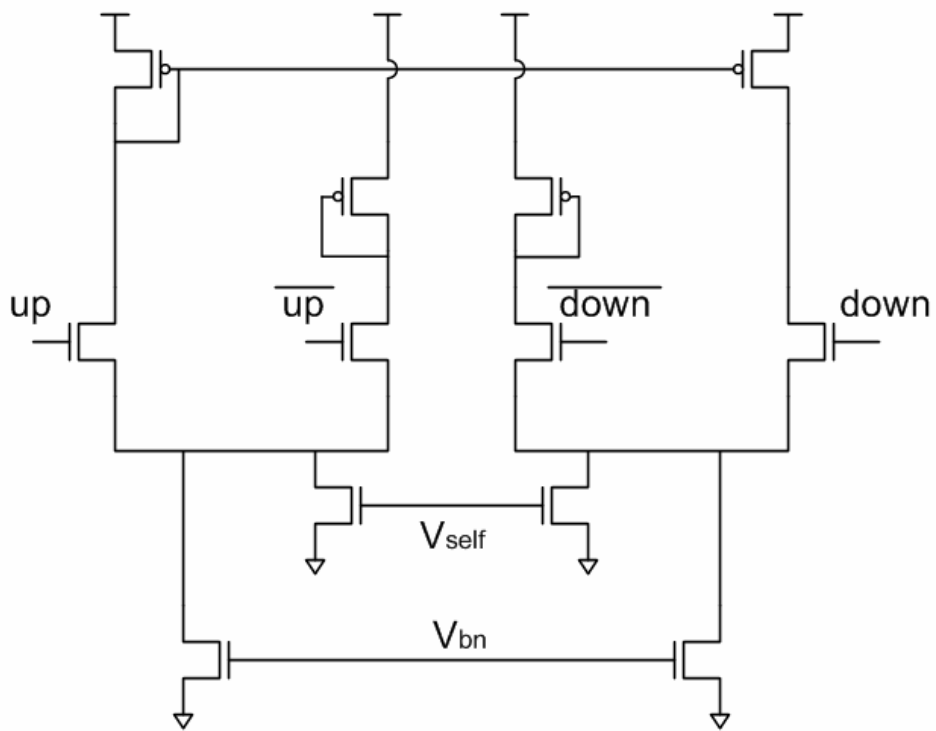
Figure 3.14    The circuit of CP
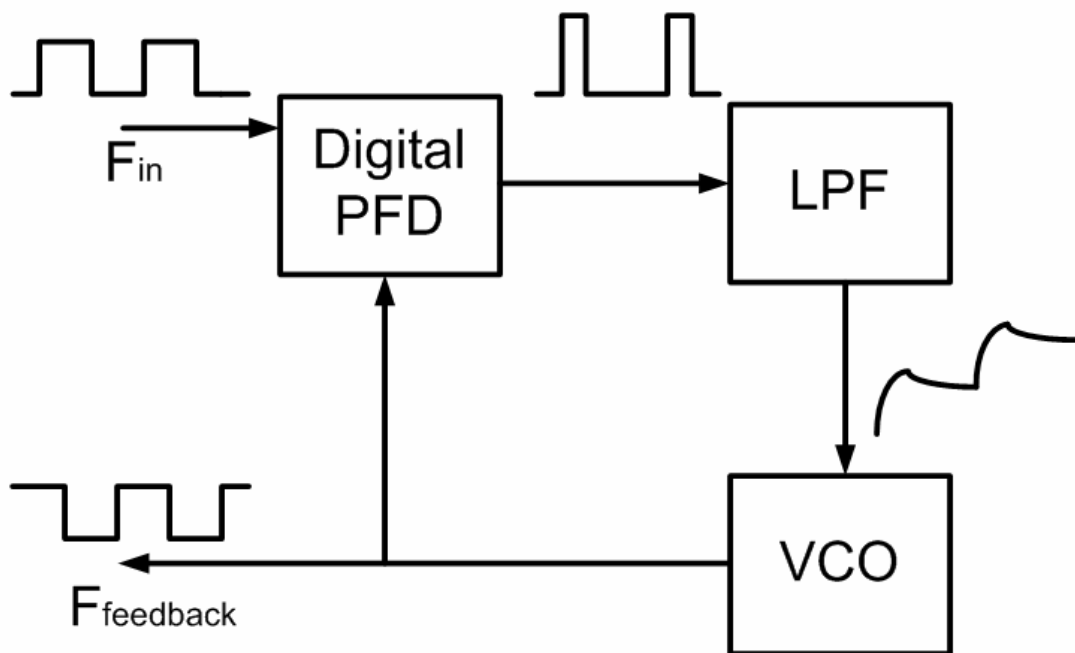


Figure 3.15    The characteristic of the control voltage
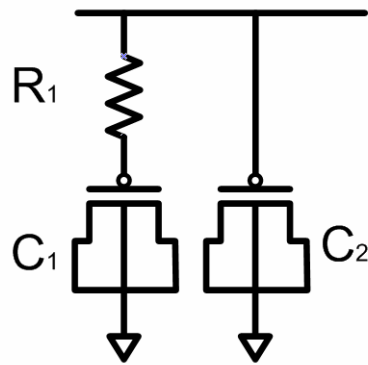
Figure 3.16    The loop filter
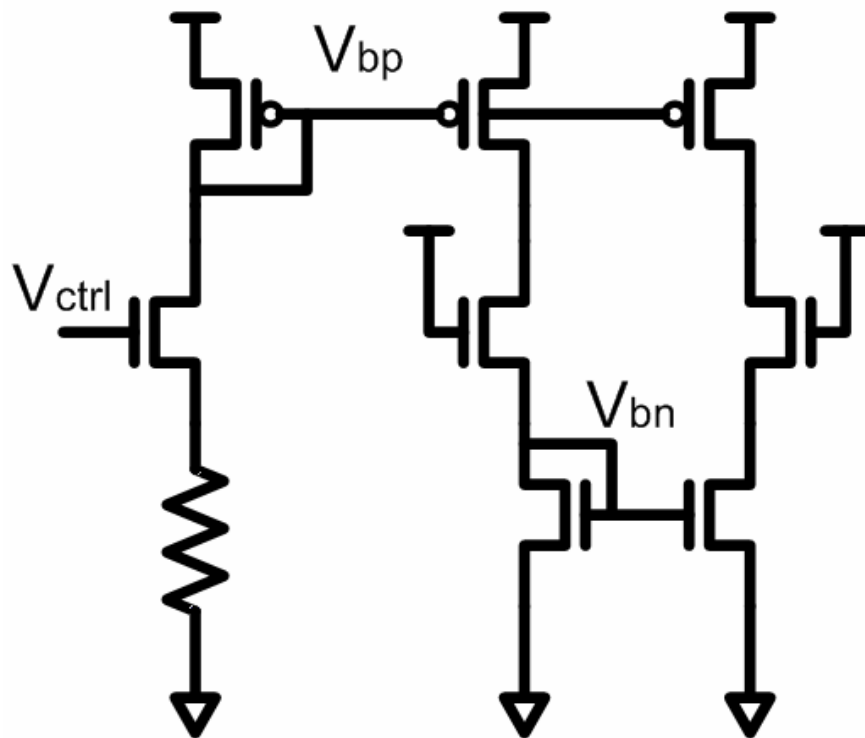


Figure 3.17    The simplified bias-generate circuit
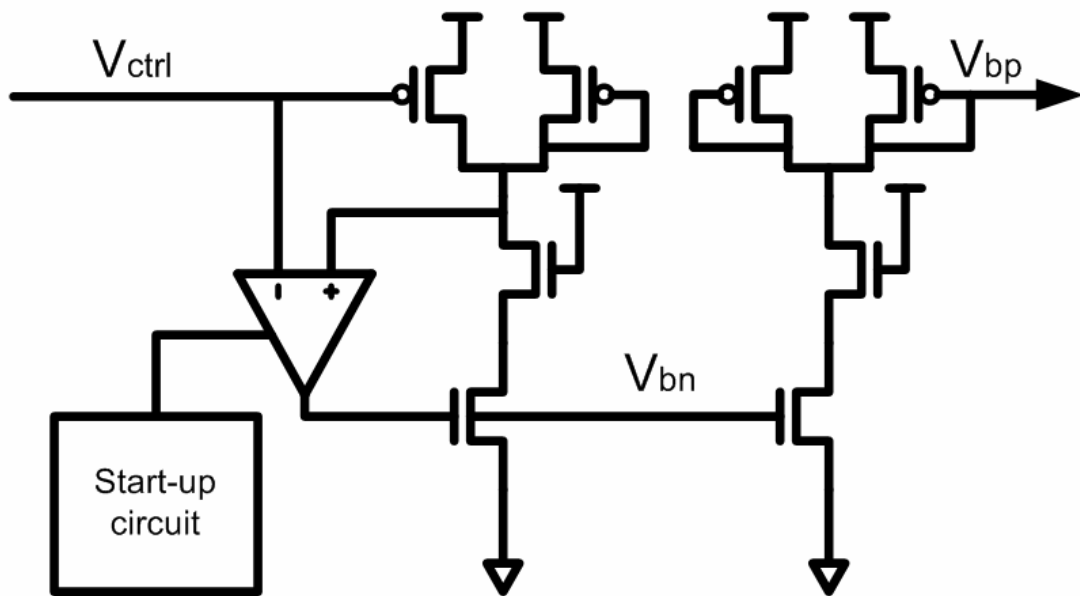
Figure 3.18    The bias-generate circuit
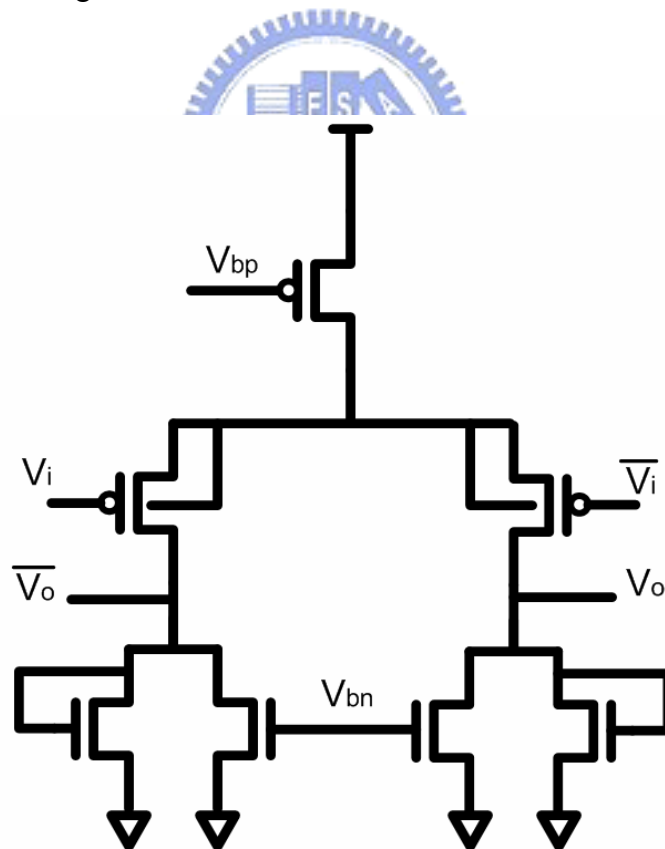


Figure 3.19    The basic cell of the VCO
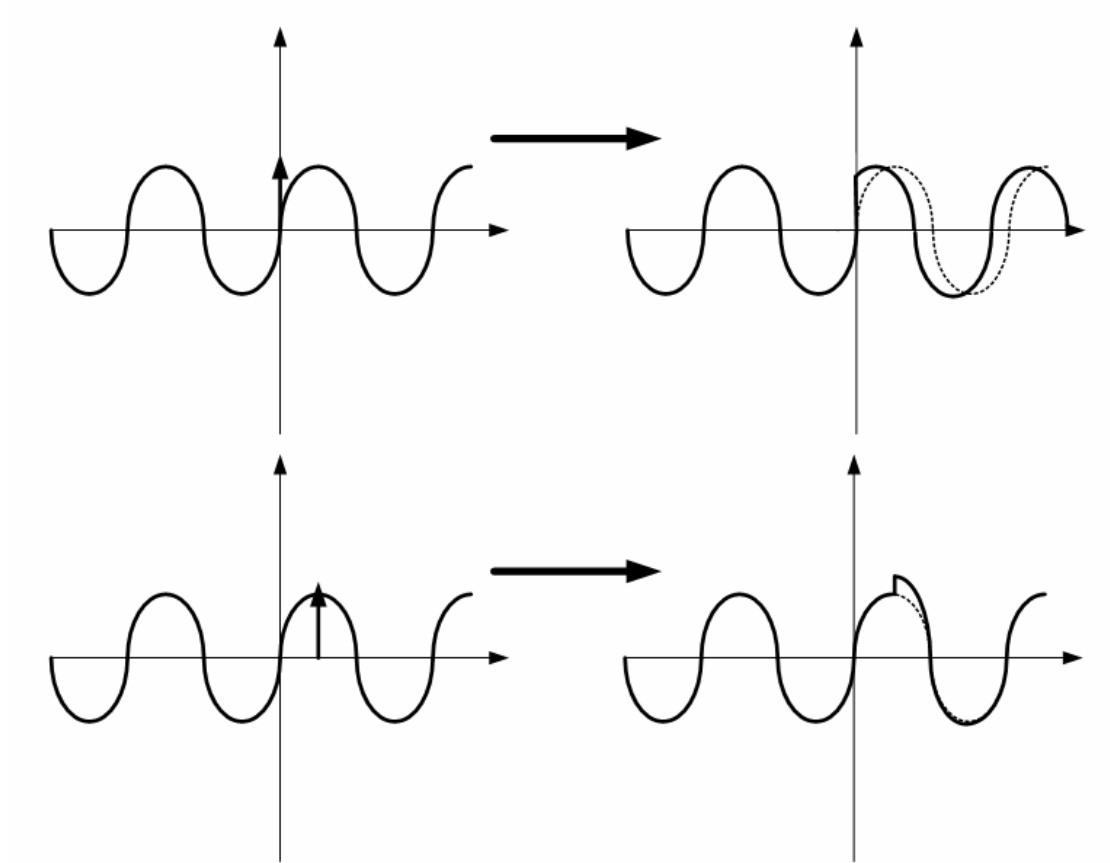
Figure 3.20    The linear-time-variant property of the VCO
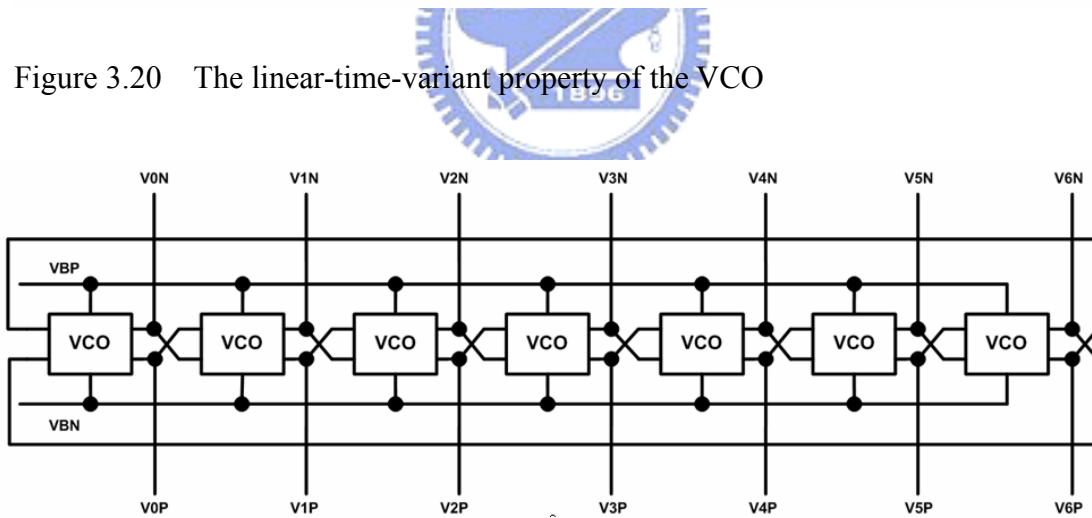


Figure 3.21    The seven stage VCO
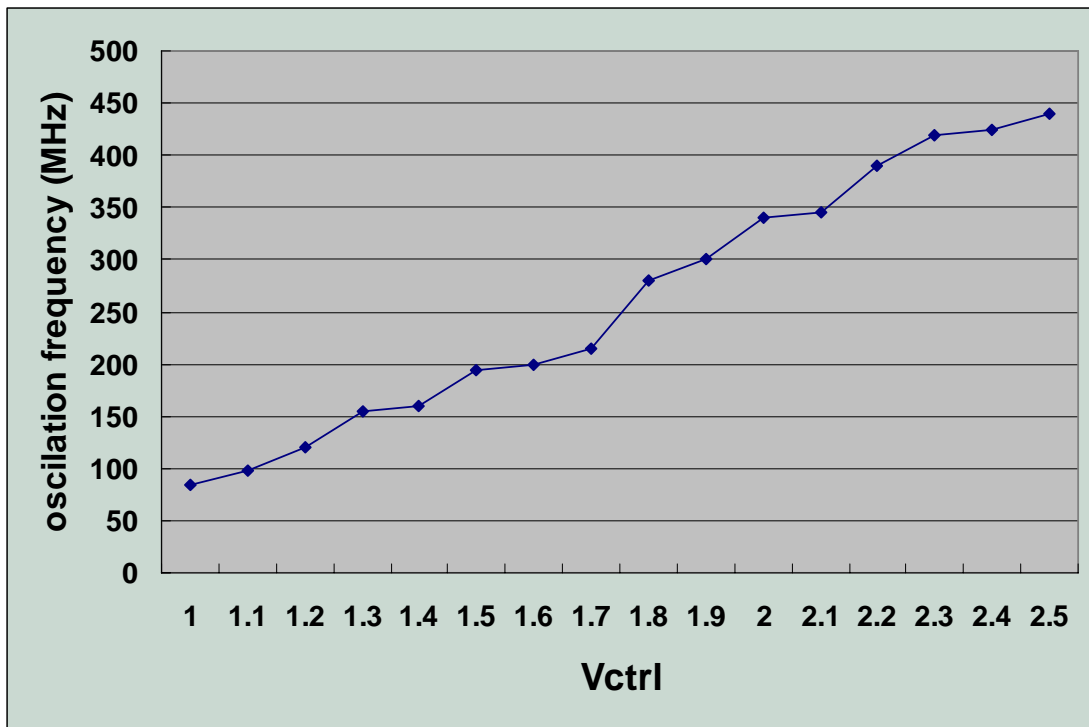
Figure 3.22　The simulated characteristic of VCO
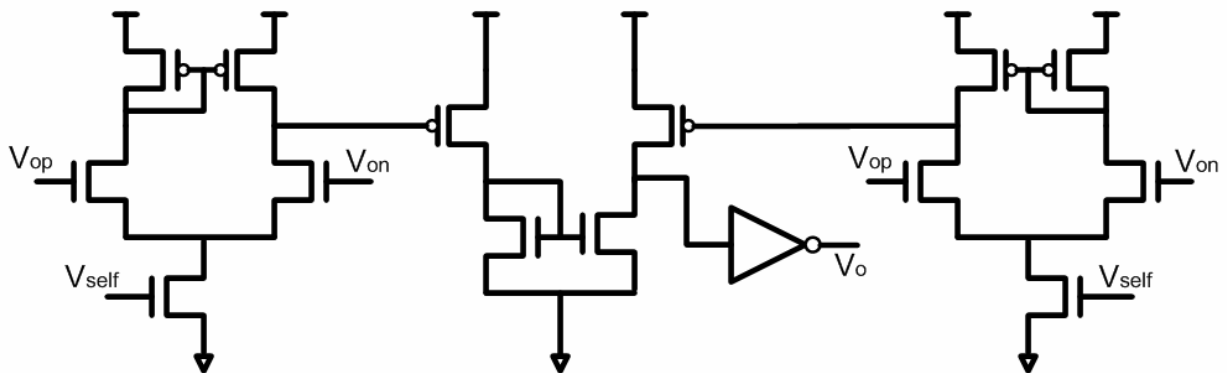


Figure 3.23　The differential-to-single-ended converter

# Chapter 4

# Design of Transmitter

## 4.1  INTRODUCTION

This chapter is devoted to the design of the transmitter. The purpose of the transmitter is to signaling the electric message outside the chip. As process technologies continue to scale down, the on-chip data rate moves faster than the off-chip data rate and the interface between systems will become an even more significant bottleneck. Therefore, how to design high-speed I/O interface circuits is an important issue [16]. The basic architecture of transmitter is shown in figure 4.1. For measurement, the PRBS is built inside the chip. The PRBS is tried to simulate the random signal that may be transmitted. Besides, the PLL will adjust the VCO according to the input clock and generate fourteen phase, full swing signals to serialize the seven parallel signals. The driver will be switch by this serialized signal and drive the transmission outside the chip to transfer electric message.

For higher operation frequency, the equalization technique can be employed to enhance the performance [17]. Besides, the LVDS transmitter can support very high speed data rate. Therefore, they can be embedded in the transmitter to have variety applications [18], [19]. The heavy data transmission requirement in the display system can be solved by LVDS solution [20].

## 4.2  THE DRIVER

As shown in figure 4.2, the traditional method, using simple taper buffer as driver and simple inverter as input buffer, is not appropriate for high speed signaling.

For the transmitted signal across the transmission line terminated by MOS gate, the signal reflection will be severe. Besides, for high speed signaling the performance merit is not just the rise/fall time but also timing accuracy. Therefore, severe signal reflection will corrupt the signal quality, which is not acceptable. Besides, the power consumption issue and the electromagnetic interfere are not ignorable in such case. Therefore, driver with small swing and proper termination is introduced and employed in many applications. For this purpose, there are several types of drivers which are often employed, depending on the application specification. They can be seen in figure 4.3. The first two, (a) and (b), are single ended and the latter two, (c) and (d) is differential ended. As discussed before, the differential ended one is preferred for its noise immunity properties. The driver choused is (d) for the termination scheme used in LVDS is double termination. Since the proposed output buffer is intended for operation in the gigabits-per-second range, the double termination scheme is used and the termination resistors are integrated in the output buffer ($R_{T-T}$) and in the receiver input buffer ($R_{T-R}$) [21], [22]. From the LVDS specification, the output DC voltage level should be well controlled. Hence a CMFB (common mode feedback circuit) should be employed to stabilize the DC voltage level. As shown in figure 4.4, the CMFB is done by average the two outputs to extract the DC voltage level [23], [24]. Then, this voltage will be compared with a reference voltage to adjust the current of the output buffer, hence the common mode voltage of outputs. However, the DC voltage level is extracted by two large resistors, which should not disturber the output. Hence, these two large resistors will consume large die area. For this reason, the other kind of output buffer is designed. As shown in figure 4.5, the output buffer with CMFB but not resistors is proposed. This is done by utilizing two equal-sized differential amplifiers to adjust the output current of the driver. However, which is not shown in these two figures is the compensation

53

capacitors and resistors. The driver with CMFB sometimes will be unstable. Therefore, extra care for stabilizing the feedback loop is important. Besides, as shown in this two figures, the Vsb is the bias voltage generated by a simple self-bias circuit. The figure 4.6 is the circuit of the self-bias circuit. Also, the generated by self-bias circuit is fed to PLL. The self-bias technique can reduce the error cause by PVT deviation.

## 4.3 PHASE-LOCKED-LOOP (PLL)

The PLL is the most critical part of the transmitter. The basic architecture of the PLL is shown in figure 4.7. As discussed before, the PFD, shown in figure 4.8, will compare the phase difference between the input clock and the VCO output, and then generate two signals to switch the charge pump. The control voltage of the VCO is then filtered by loop filter and adjusts the VCO to reduce the phase error. The VCO is shown in figure 4.9 and the chare pump and the loop filter is shown in figure 4.11. Besides, the PLL may not work properly for the PVT deviation. Hence the self-adjust technique is employed. The bias-gen circuit is shown in figure 4.12.

## 4.4 PSEUDO RANDOM BIT SEQUENCE (PRBS)

A pseudo random binary sequence (PRBS) is a test pattern that appears to be random, but is actually a predictable and periodical sequence with a very long interval, depending upon the structure. The period of the PRBS is not always increased with the increased stages. The feedback point is also an important factor. A PRBS is an algorithmically determined bit sequence that has the same statistical characteristics as a truly random sequence and simulates live traffic. The transmitter has a PRBS generator as shown in figure 4.13, it uses D-type flip flops and one OR logic gate to

realize algorithmically determined bit sequence. The circuit implementation of the D-type flip-flop which is utilized in the PRBS is true single-phase clock logic (TSPC) as shown in figure 3.11. The RESET pin in the PRBS is employed to trigger the PRBS in case of the all zero state and the CLK pin is connected to the external pulse generator in order to generate the same frequency pseudo random patterns as the external clock source. When the RESET pin is logic low, the PRBS is forced to enable. After a while, the RESET pin should be changed to logic high in order to keep the patterns correct. Since the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors. The bit length of the PRBS is $2^8-1$. Fig. 5.6 shows the simulated output signals of the seven PRBS outputs.

## 4.5 MULTIPLEXER
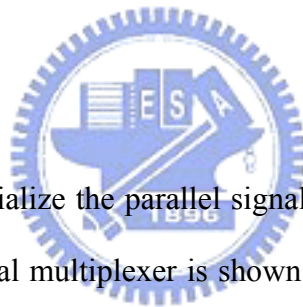
For the serial-link, to serialize the parallel signal channels into a single signal is the basic principle. The general multiplexer is shown in figure 4.15. Also, the timing diagram of the multiplexer is shown in figure 4.16. However, there are some drawbacks in this configuration. The serial connected NMOS switched by different phase clocks will induce a data dependant jitter, which is always referred as ISI. The ISI stands for inter-symbol interference. Charge-sharing and the memory will cause this multiplexer failed when operating at high frequency. Besides, for the purpose of high speed operation, the serial connected NMOS should be large devices. Or the multiplexer will not suitable for high speed operation.

The improved multiplexer is shown in figure 4.17. The ISI problem should be less severe for this configuration.

55

## 4.6 RETIMING THE DATA

For serializing multiple parallel signals, the transition of signals should be avoided. This problem can be shown as below. The configuration without synchronization is shown in figure 4.18. The CLK signal will set the timing of the internal digital circuit and the PLL will generate seven signals with equal phase separation. These signals with different phase will be employed to serialize the data. As shown in figure 4.19, the phase of PH0 and the digital signals should be approximately the same as the CLK signal. Nevertheless, PH0 and PH3 will set the bit time of D0 in the serialized signal. Therefore, there may not be enough time left for D0 to switch the multiplexer. Hence, the performance of the whole transmitter will be corrupted. For the same reason, the D6 may also has the same problem, which is shown in the figure 4.20.

In this case, the technique of synchronization is utilized. The configuration is shown in figure 4.21. The main idea of synchronization is to put the transition edge out of the sampling pulse period. For this purpose, at least two DFF must insert into the path. However, the sequence of the data will not be in order. Besides, the PLL may not be exactly in phase with CLK, and that will introduce another ambiguity into the sterilization process. With seven DFF switched by different phase signals, the data sequence still will not in order. Therefore, the synchronization scenario as figure 4.22 is shown. The data will be retimed to the output of PLL, which will actually determine the real timing of the data bits. Then, the extra DFF is inserted to serialize the data in order. The data sequence after synchronization is shown in figure 4.23
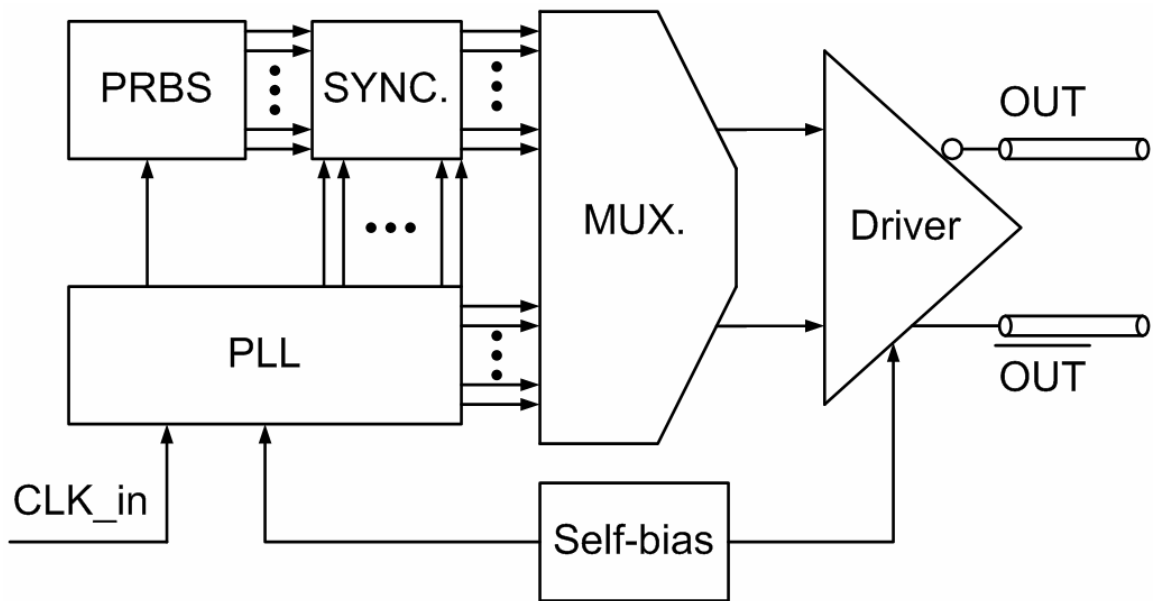
Figure 4.1     The basic architecture of the transmitter
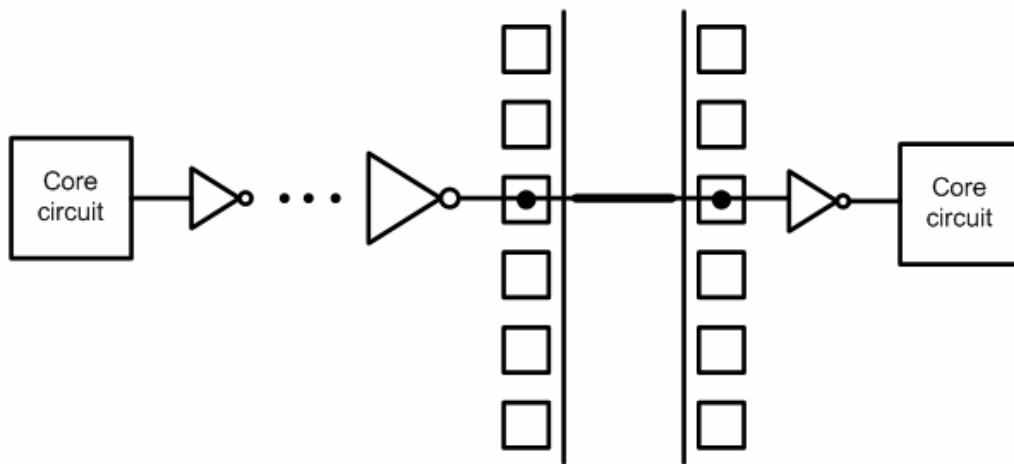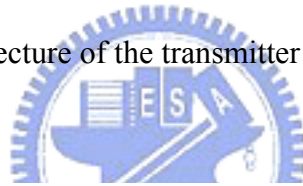


Figure 4.2     The traditional method of signaling
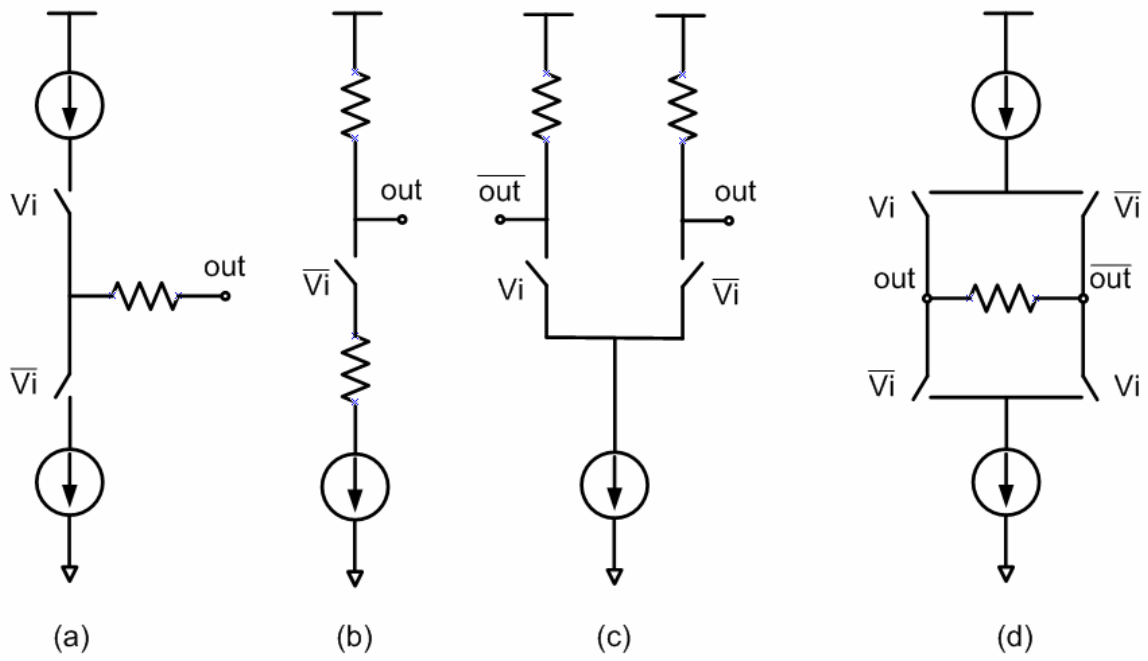
Figure 4.3    Several types of output drivers
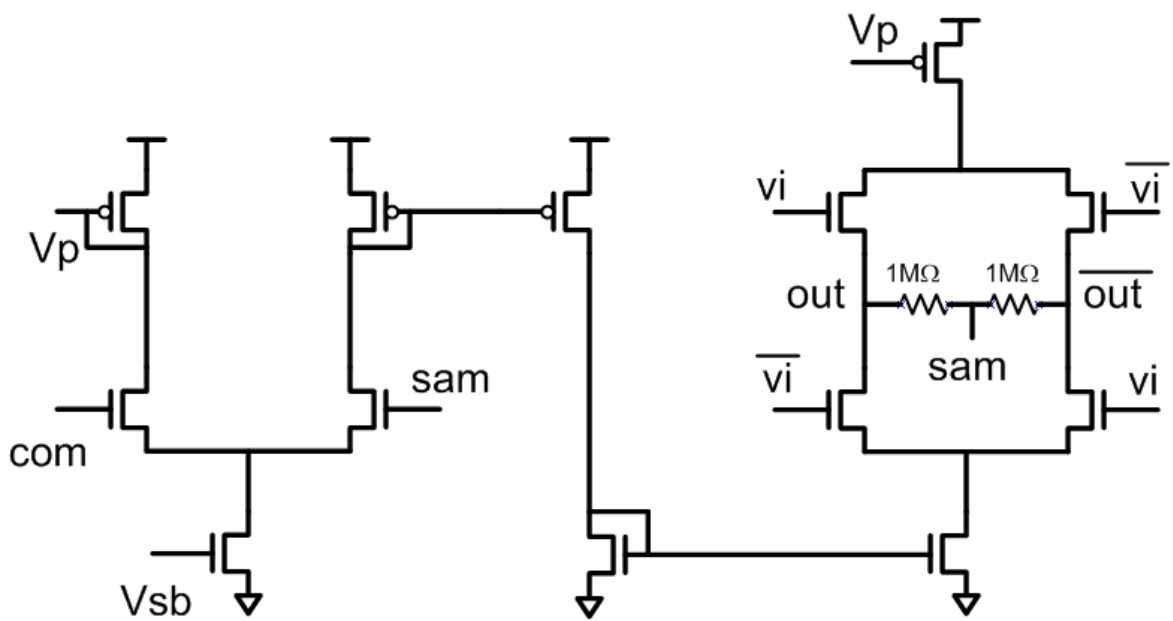


Figure 4.4    The 1$^{st}$ output buffer with CMFB
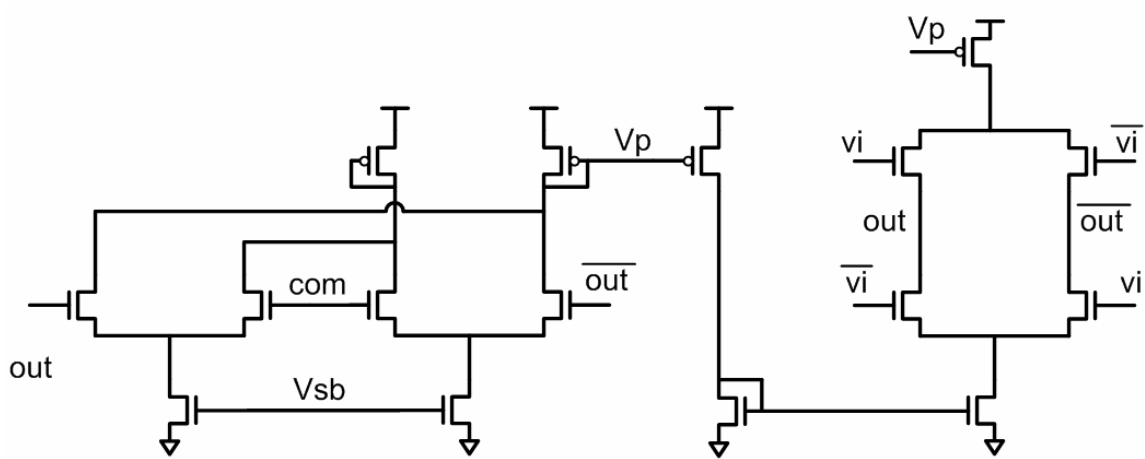
Figure 4.5    The 2$^{nd}$ output buffer with CMFB
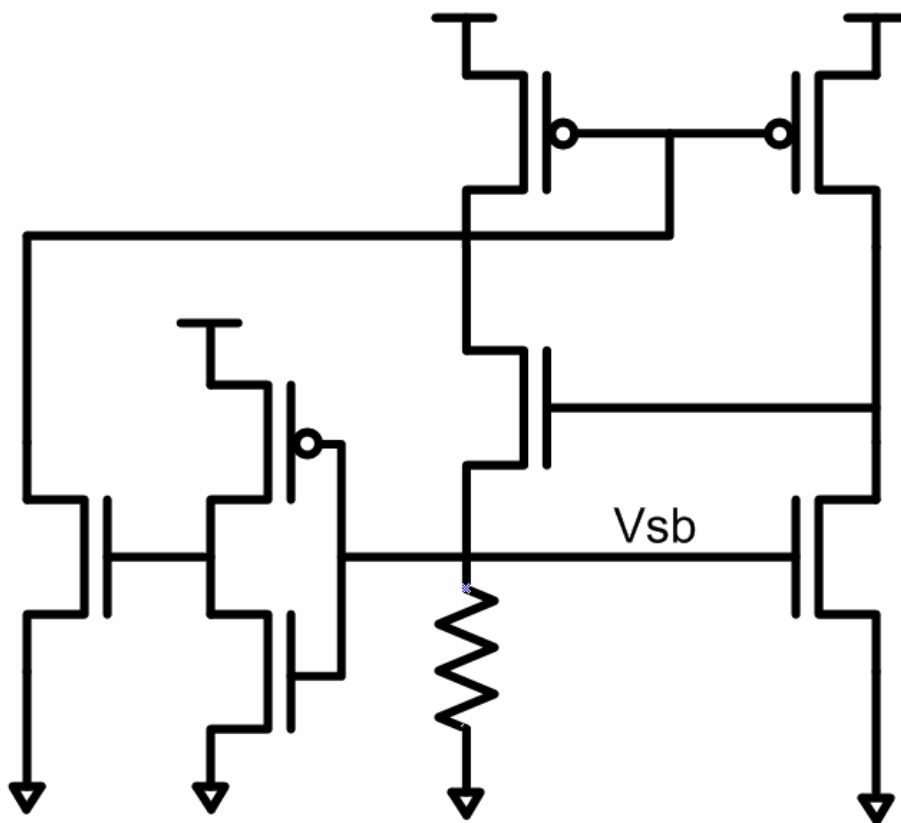


Figure 4.6    The self-bias circuit
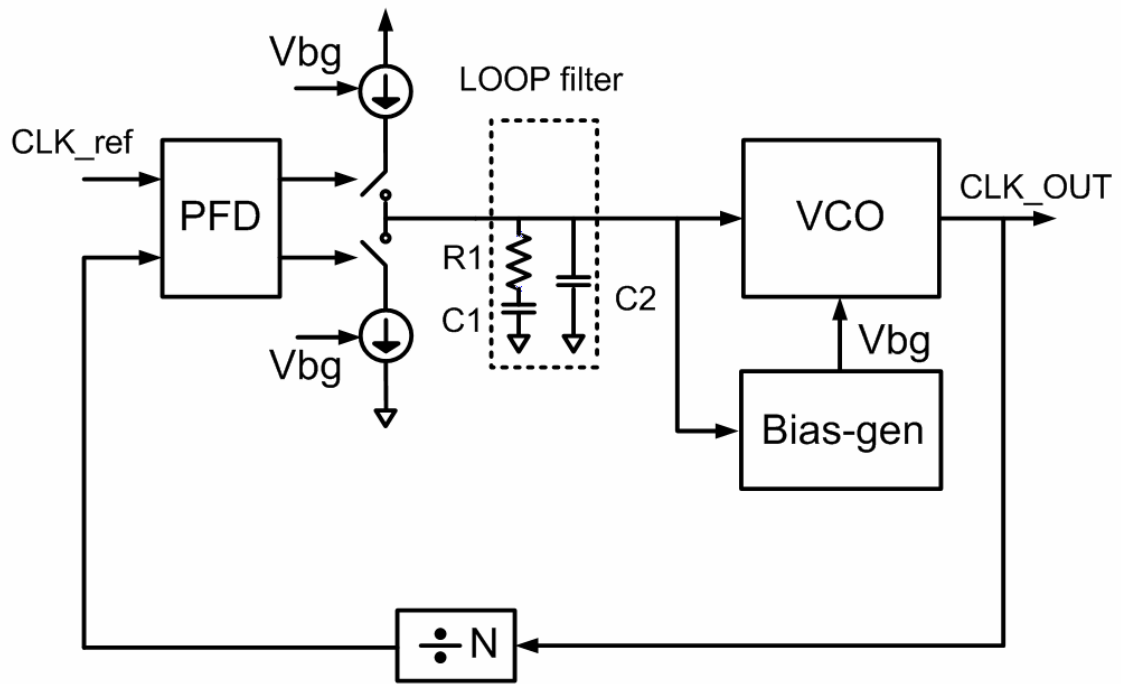
Figure 4.7    The basic architecture of PLL
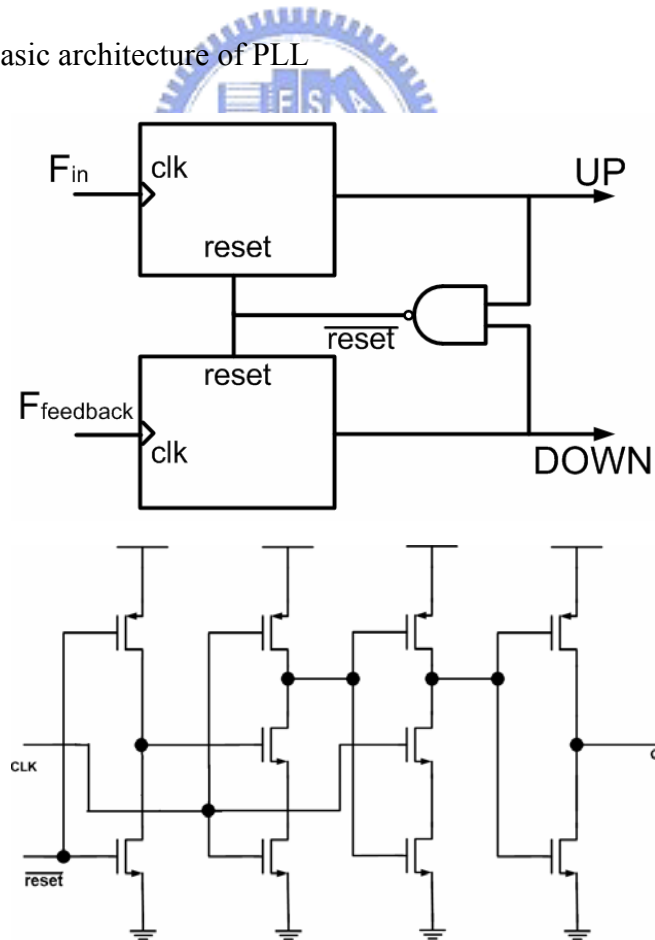


Figure 4.8    The circuit blocks of the PFD
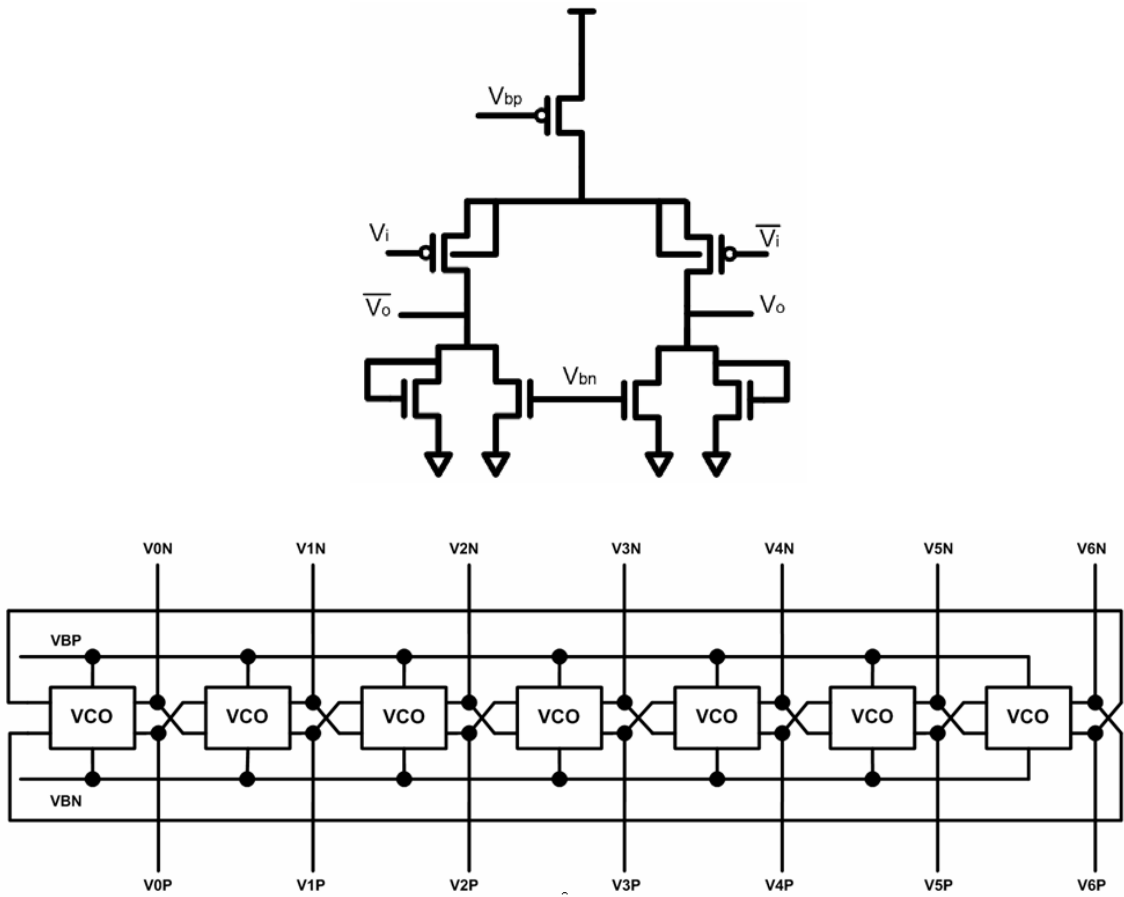
Figure 4.9    The VCO
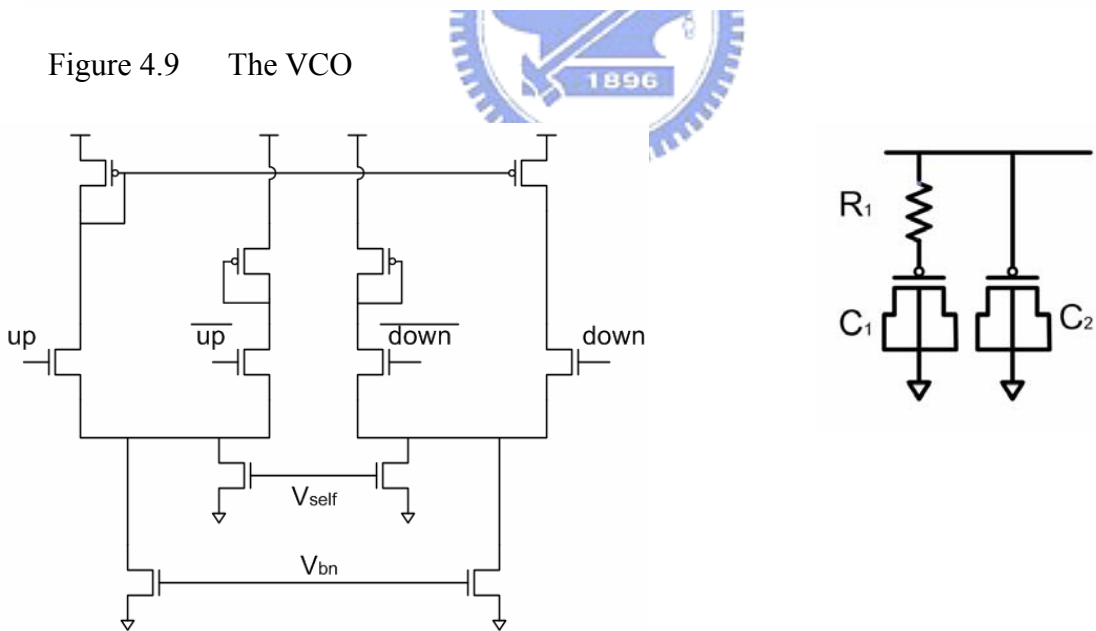


Figure 4.10    The charge pump and loop filter
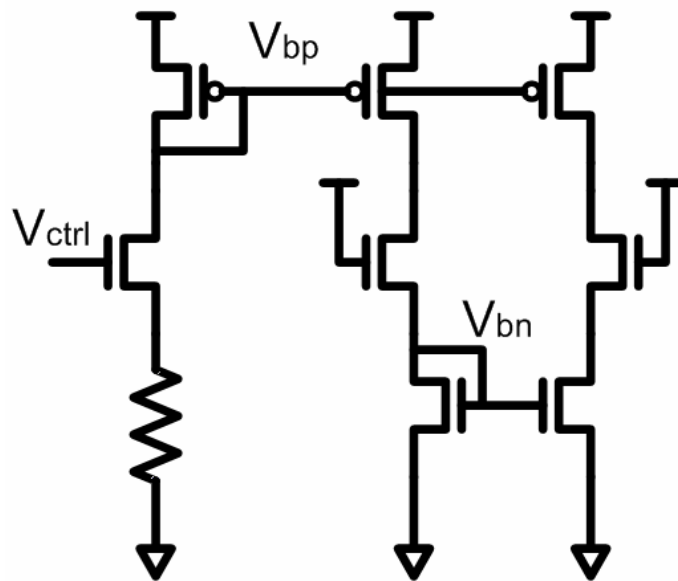
Figure 4.12    The bias-gen circuit
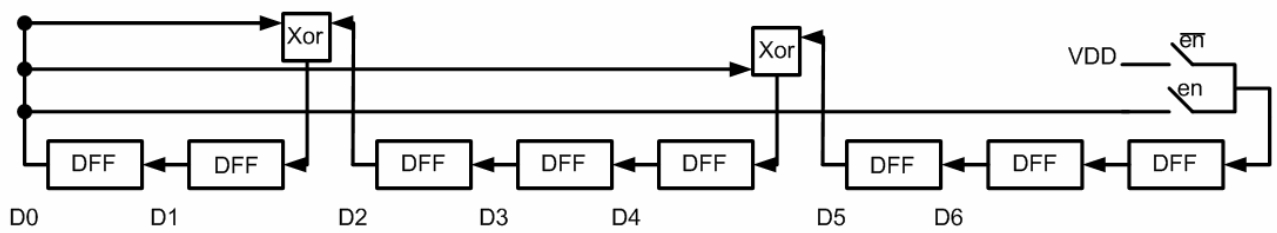


Figure 4.13    The PRBS
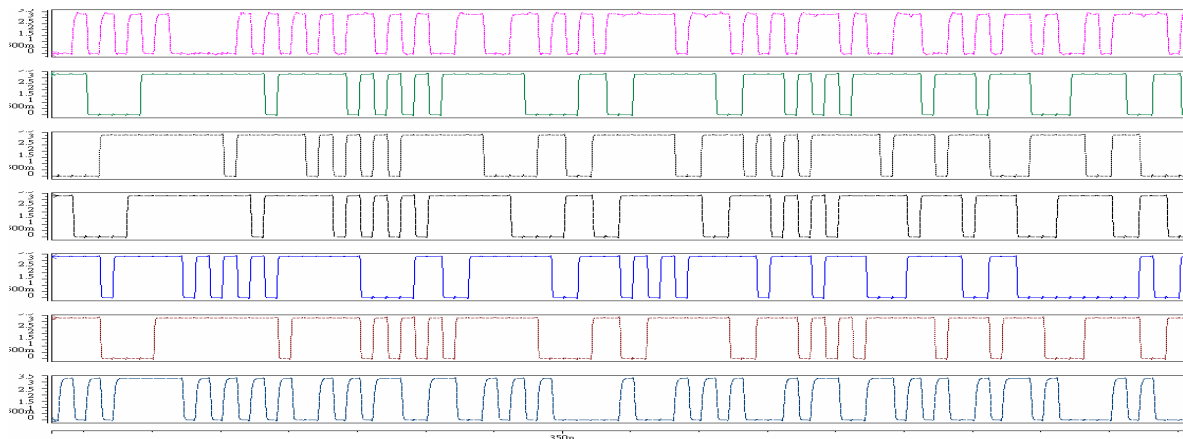


Figure 4.14    The simulation result of the PRBS
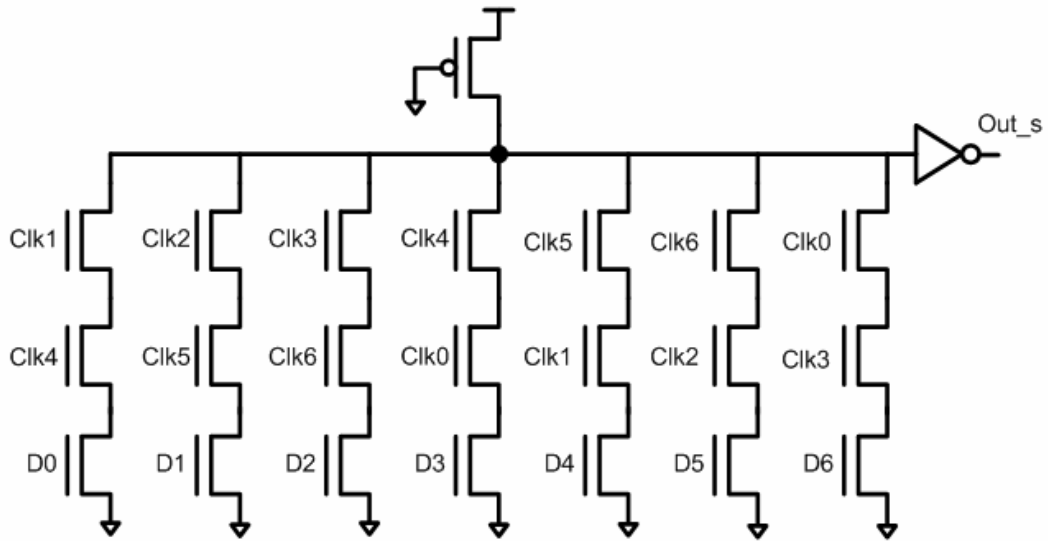
Figure 4.15    The multiplexer
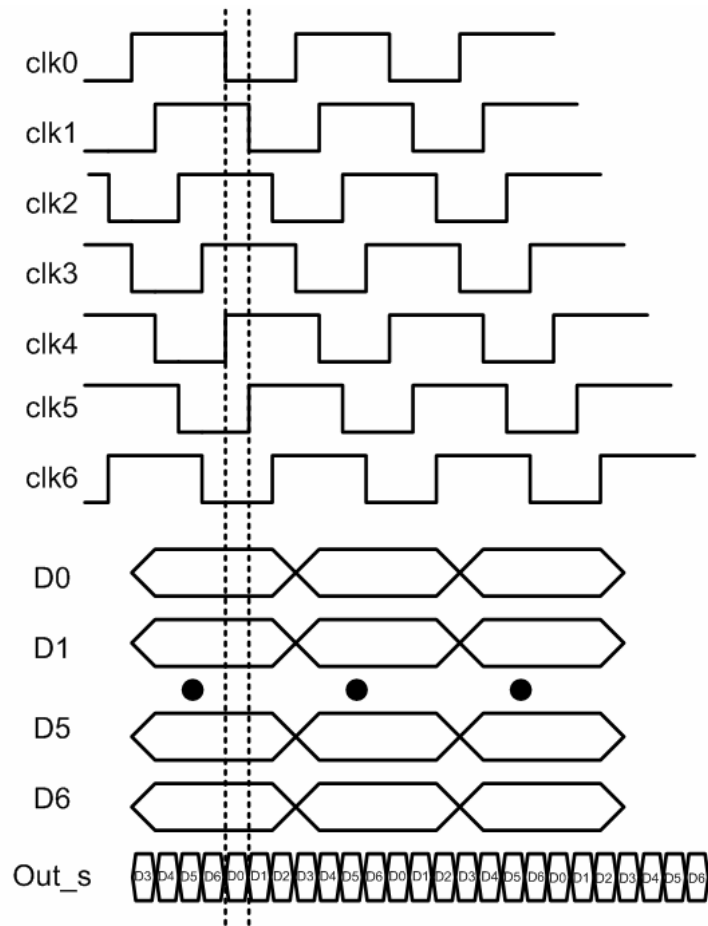


Figure 4.16    The timing diagram of the multiplexer
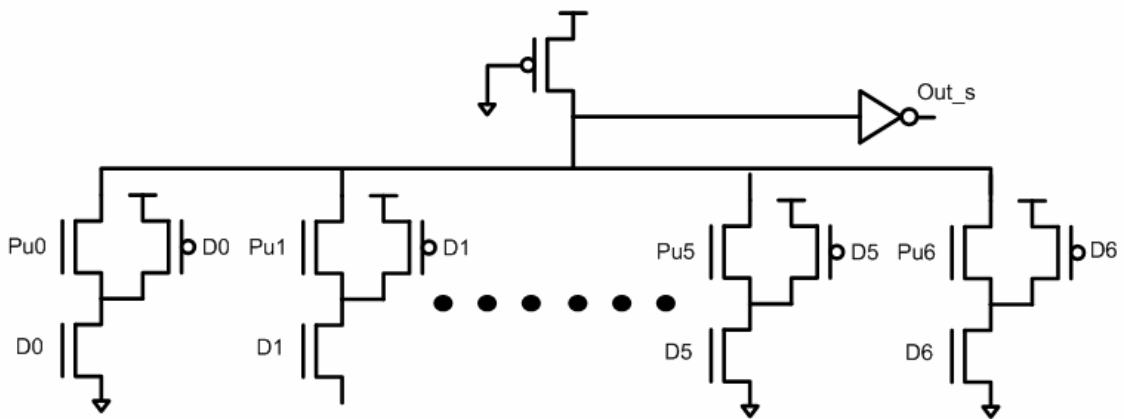
Figure 4.17      The improved multiplexer
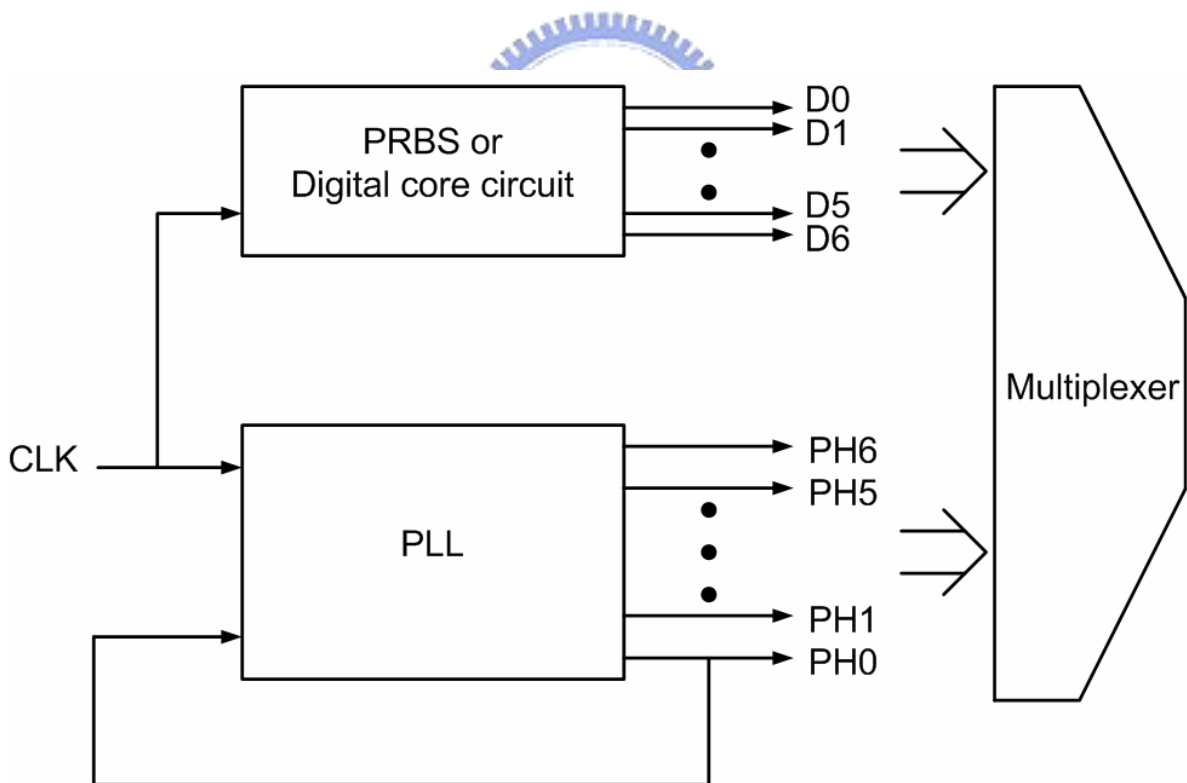


Figure 4.18      The circuit blocks of the non-synchronization configuration
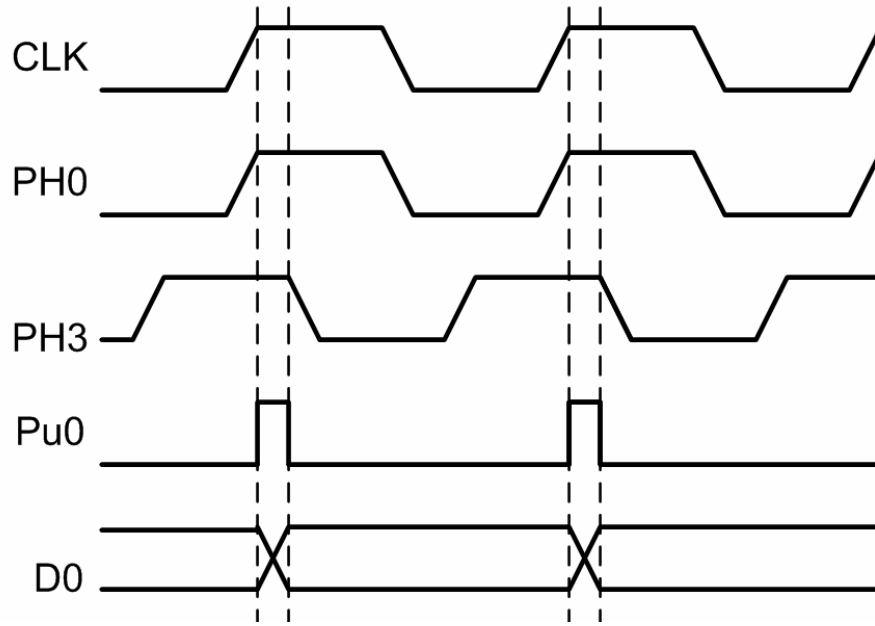
Figure 4.19    The timing diagram for non-synchronization configuration
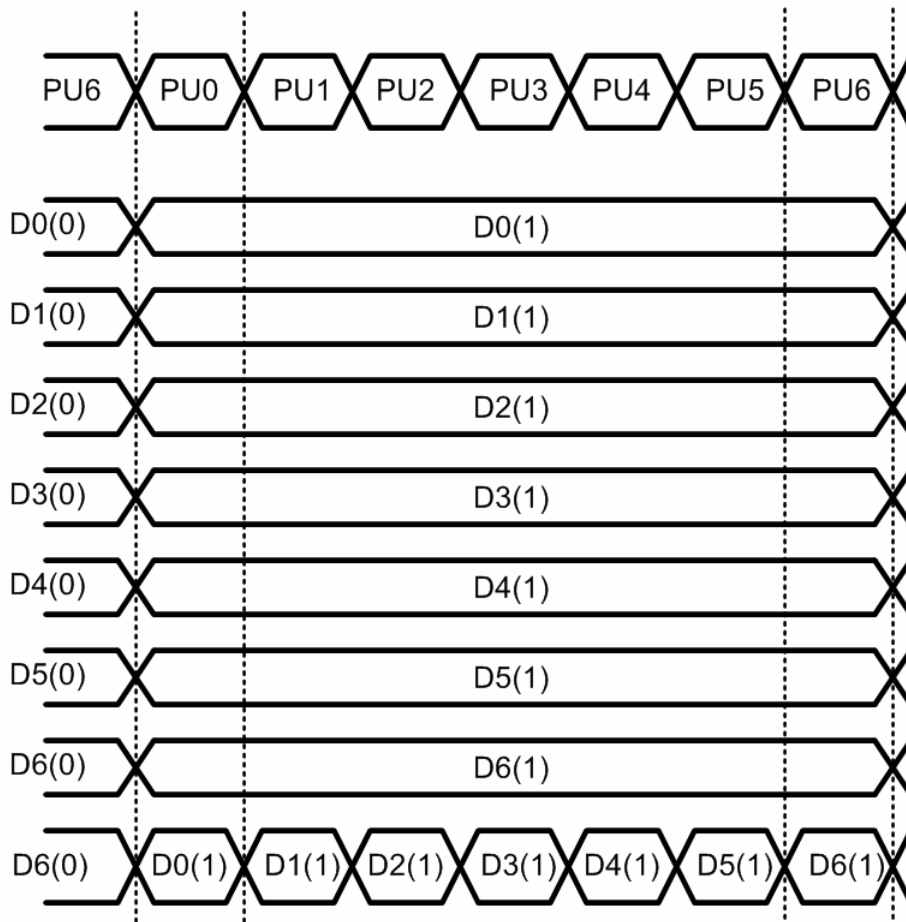


Figure 4.20    The timing diagram for configuration without synchronization
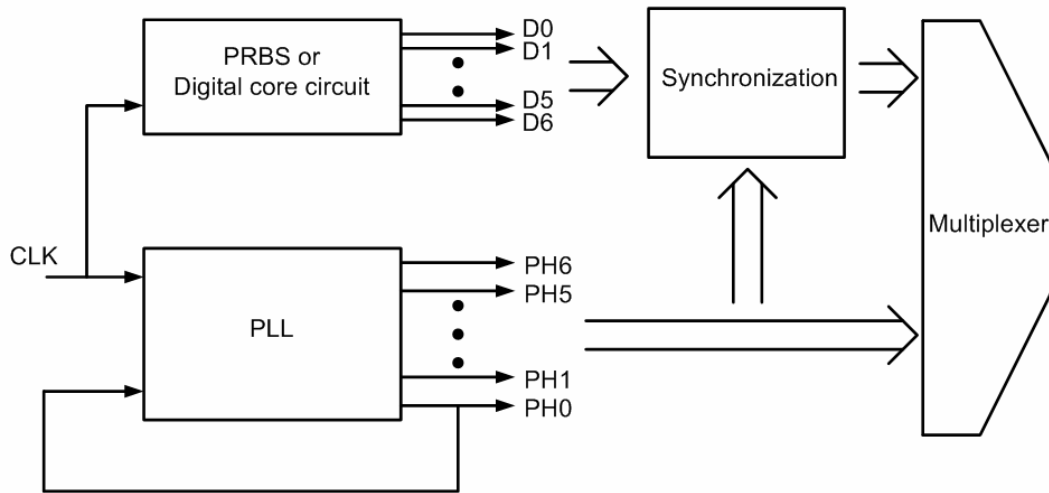
Figure 4.21    The configuration with synchronization
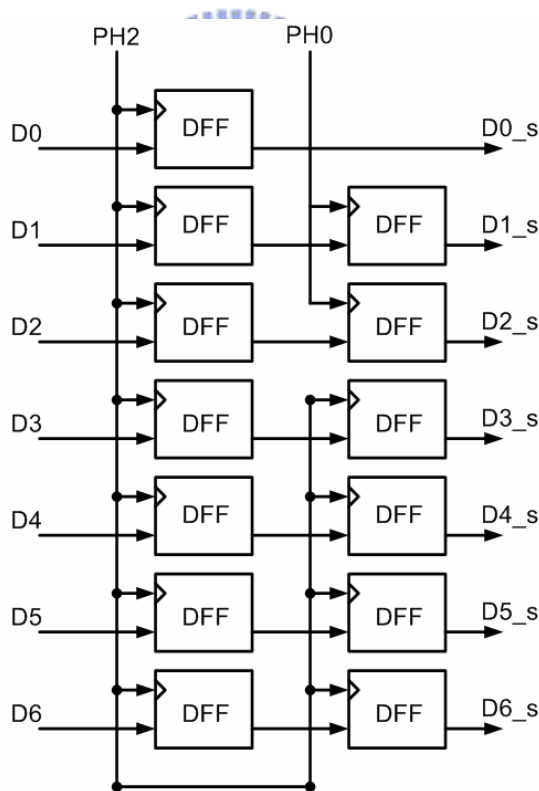


Figure 4.22    The scenario of synchronization
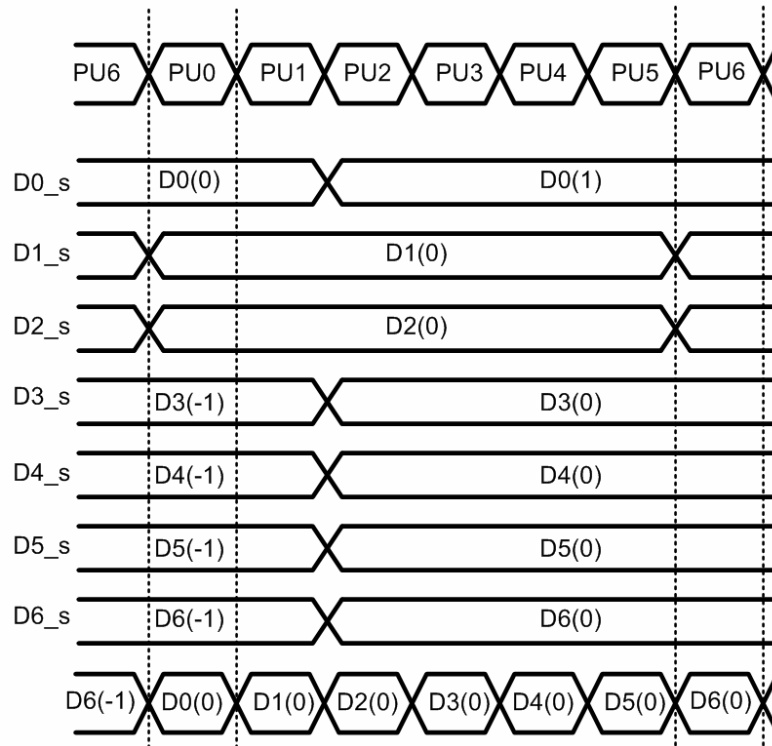
Figure 4.23    The timing diagram for configuration with synchronization

# Chapter 5

# Measurement Results

## 5.1 INTRODUCTION

This measurement result is shown in this chapter. Two measurement results are described. The first one is the PLL and the second one is transmitter.

## 5.2 MEASUEMENT FOR THE 1$^{ST}$ TAP-OUT

The 1$^{st}$ tap-out is mainly a PLL. The layout of the PLL is in figure 5.1. The PLL output is droved by LVDS transmitter. The die photo is shown in figure 5.2. Also, PCB for measurement is shown in figure 5.3. The chip is packaged and large decouple capacitor is employed to reduce the supply noise. In figure 5.4, the measurement setup is shown. HP 8131A is used as a function generator. TEK. DSA 601A is the oscilloscope. As shown in figure 5.5, the measured output of the transmitter is shown. The operating frequency is 100 MHz. The Pk-Pk jitter is about 83ps at 100 MHz, which is shown in figure 5.6. In figure 5.7, the measurement at 250 MHz is shown. Also the Pk-Pk jitter is about 89ps in the figure 5.8. The measurement results is concluded in table 5.1.

## 5.3 MEASUEMENT FOR THE 2$^{ND}$ TAP-OUT

As described before, the second measurement is the transmitter. The layout of the transmitter is shown in figure 5.9. There two kinds of output buffers and PLL with

slightly difference. They are shown in figure 5.10 and figure 5.11. The output buffers are different in the CMFB and the PLL is different in the VCO. The third quadrant is the main blocks for this measurement. However, measurement for the rest will be shown. In figure 5.12, the die photo is shown. The PCB and the measurement setup is shown in figure 5.13 and figure 5.14 separately. Since the transmitter has two outputs, one is for clock signal and the other is for data signal. The clock signal is droved by the PLL output. The output for the PLL is shown in figure 5.15 at 390 MHz. In figure 5.16 the difference between single ended output and the differential output is shown. As expected, the differential ended output should have better performance than single ended output. Figure 5.17, the measured eye diagram of the transmitter at 930 Mb/s with 30 cm cable. The peak-to-peak jitter is 10.4 %. Figure 5.18, the measured eye diagram of the transmitter at 1.4 Gb/s with 30 cm cable. The peak-to-peak jitter is 16.1 %. Figure 5.19, the measured eye diagram of the transmitter at 1.8 Gb/s with 30 cm cable. The peak-to-peak jitter is 17.1 %. Figure 5.20, the measured eye diagram of the transmitter at 2 Gb/s with 30 cm cable. The peak-to-peak jitter is 25 %.   Then, the cable length is increased to 70 cm. The measurement result is as below. Figure 5.21, the measured eye diagram of the transmitter at 930 Mb/s with 70 cm cable. The peak-to-peak jitter is 15.2 %. Figure 5.22, The measured eye diagram of the transmitter at 1.4 Gb/s with 70 cm cable. The peak-to-peak jitter is 18.9 %. Figure 5.23, The measured eye diagram of the transmitter at 1.8 Gb/s with 70 cm cable. The peak-to-peak jitter is 24.1 %. Figure 5.24, The measured eye diagram of the transmitter at 2 Gb/s with 70 cm cable. The peak-to-peak jitter is 36 .4%. Besides, the measurement for the other quadrants is shown in figure 5.25, 5.26 and 5.27. The operating speed is 1.4 Gb/s. As we can see, these blocks have similar results. However, the 4th quadrant is biased by external pin. The voltage level is set to 0.7 V, according to the simulation value. As we can see, the output voltage swing is smaller,

which is mainly because process deviation. This may prove that the employment of the self-bias technique is appropriate. The measurement result for the $2^{nd}$ tap-out is shown in table 5.2.

Table 5.1 the measurement results for the PLL in the 1st tap-out

| Function | PLL |
|---|---|
| **Simulation Results** | |
| Operate Voltage | 3.3 V |
| Charge Pump Current | 80 μA |
| Divided by N | N = 1 |
| VCO Gain | 220 MHz/V |
| C1 | 15.5 pF |
| C2 | 0.3 pF |
| R1 | 7 kΩ |
| Phase Margin | 72 ° |
| Loop Bandwidth | 12 MHz |
| **Measurement Results** | |
| Technology | UMC 0.13-μm 1P8M CMOS |
| Output Clock Jitter | 83ps @100 MHz |
| Power | 50 mW @ 200 MHz |

Table 5.2 the measurement results for the PLL in the 2<sup>nd</sup> tap-out

| Function | PLL |
|---|---|
| **Simulation Results** | |
| Operate Voltage | 3.3 V |
| Charge Pump Current | 80 μA |
| Divided by N | N = 4 |
| VCO Gain | 220 MHz/V |
| C1 | 65.2 pF |
| C2 | 1.02 pF |
| R1 | 3.5 kΩ |
| Phase Margin | 66 ° |
| Loop Bandwidth | 2 MHz |
| **Measurement Results** | |
| Technology | UMC 0.13-μm 1P8M CMOS |
| Output Clock Jitter | 90 ps @ 200 MHz |
| Power | 46 mW @ 200 MHz |
| **Function** | **Transmitter** |
| **Measurement Results** | |
| Operate Voltage | 3.3 V |
| Power Consumption (1) | 125 mW@1.4 Gb/s |
| Power Consumption (2) | 162 mW@2 Gb/s |
| Data Rate | Target at 1.225 Gb/s (Measured up to 1.8 Gb/s) |
| Technology | UMC 0.13-$\mu$m 1P8M CMOS |
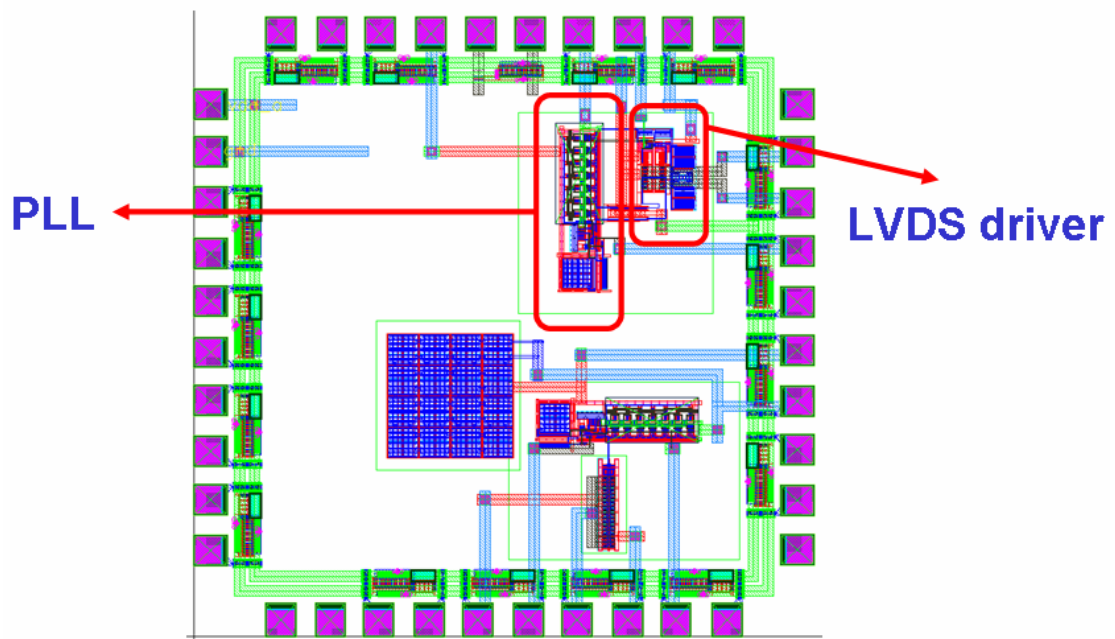
Figure 5.1    1st layout for the measurement
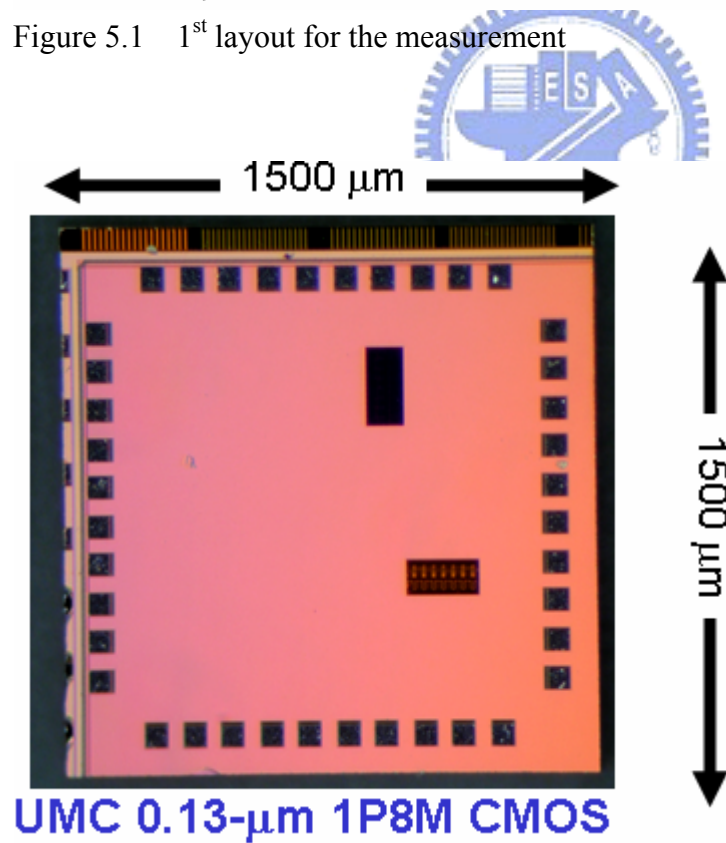


Figure 5.2    die photo for the 1st measurement
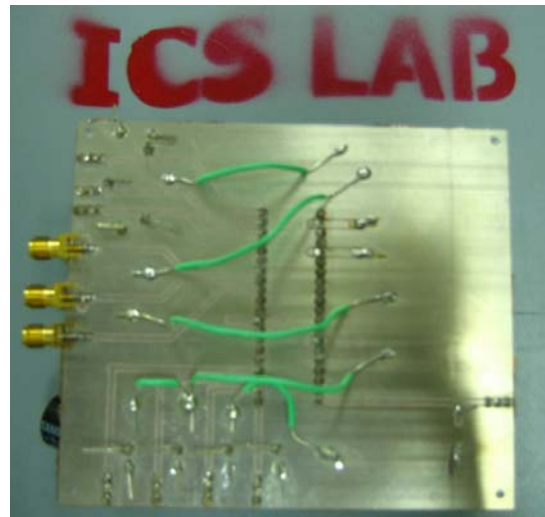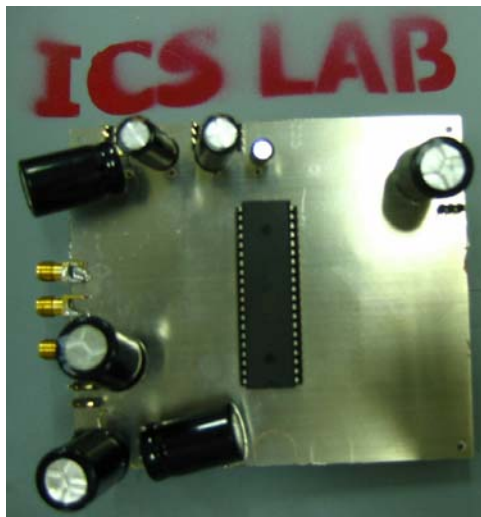
Figure 5.3    the PCB for the 1st measurement
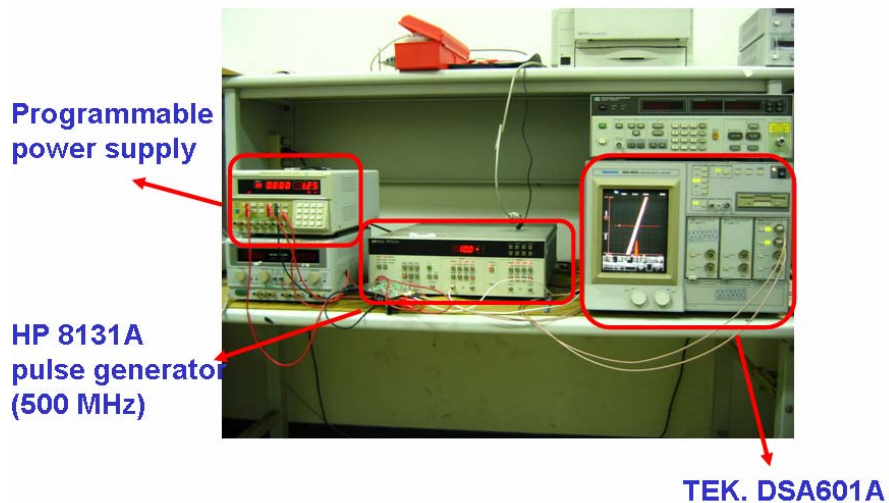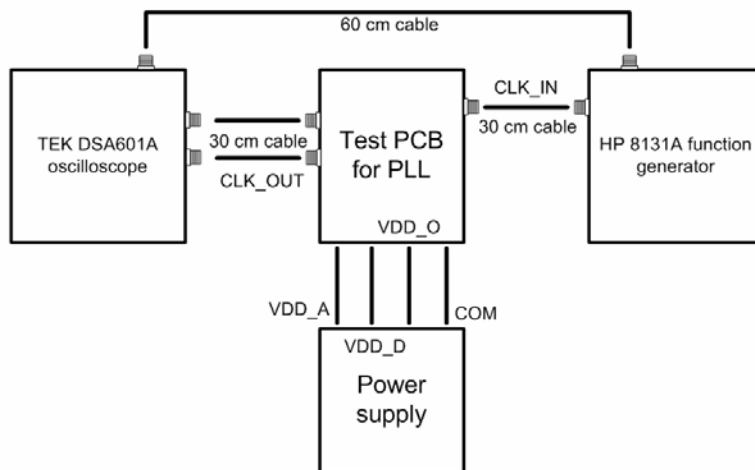


Figure 5.4    the measurement setup for 1st measurement
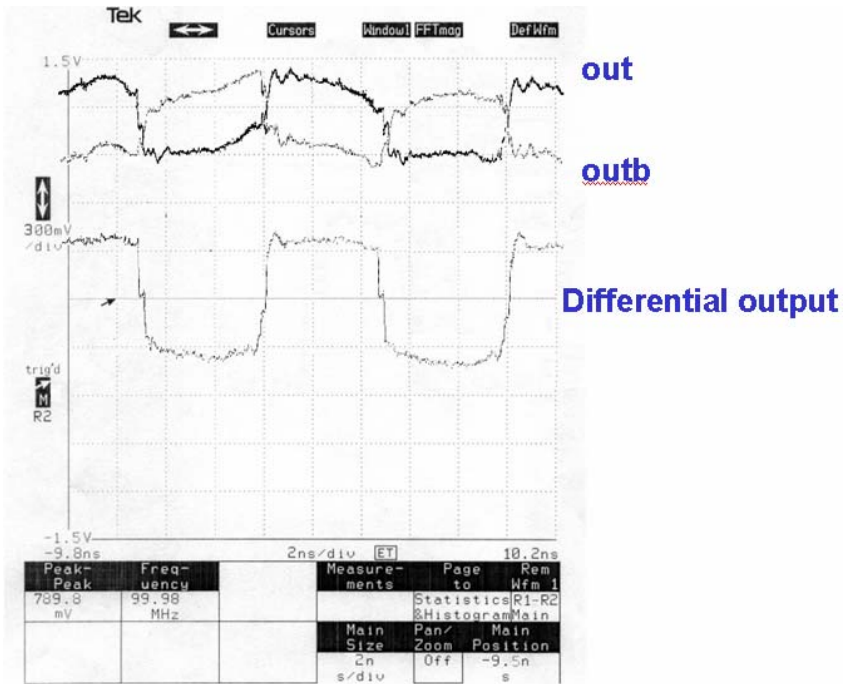
Figure 5.5    The measured output of the PLL at 100 MHz with package.
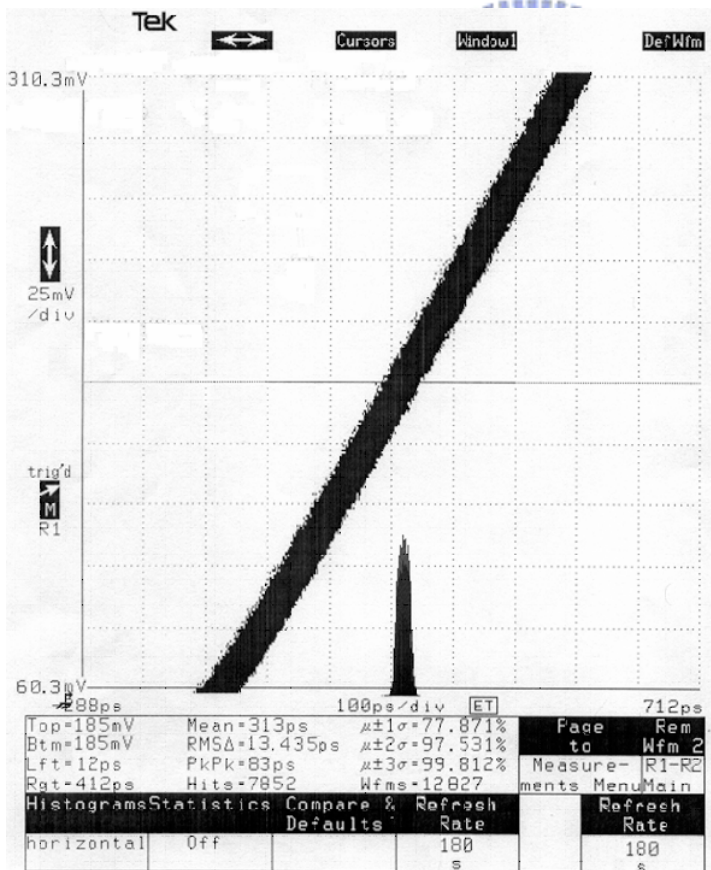


Figure 5.6    The measured jitter of the PLL at 100 MHz. The Pk-Pk jitter is about
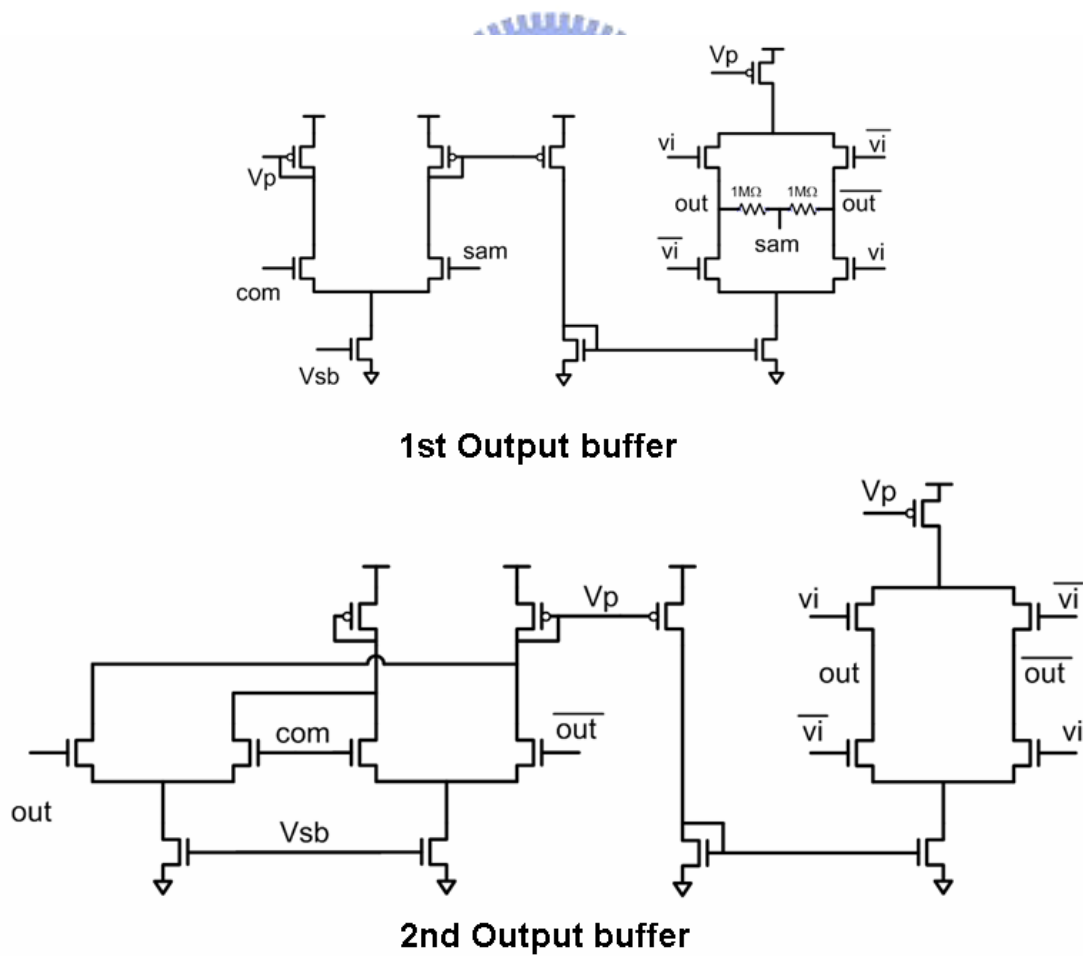
83ps.
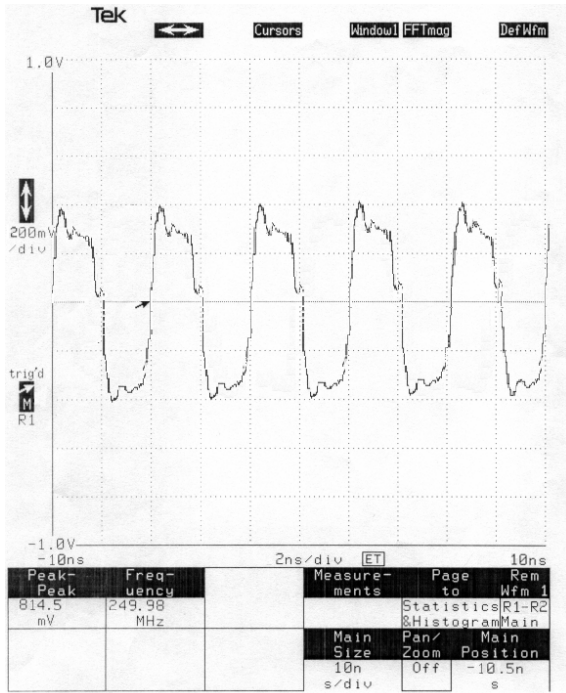
Figure 5.7    The measured output of the PLL at 250 MHz with package.
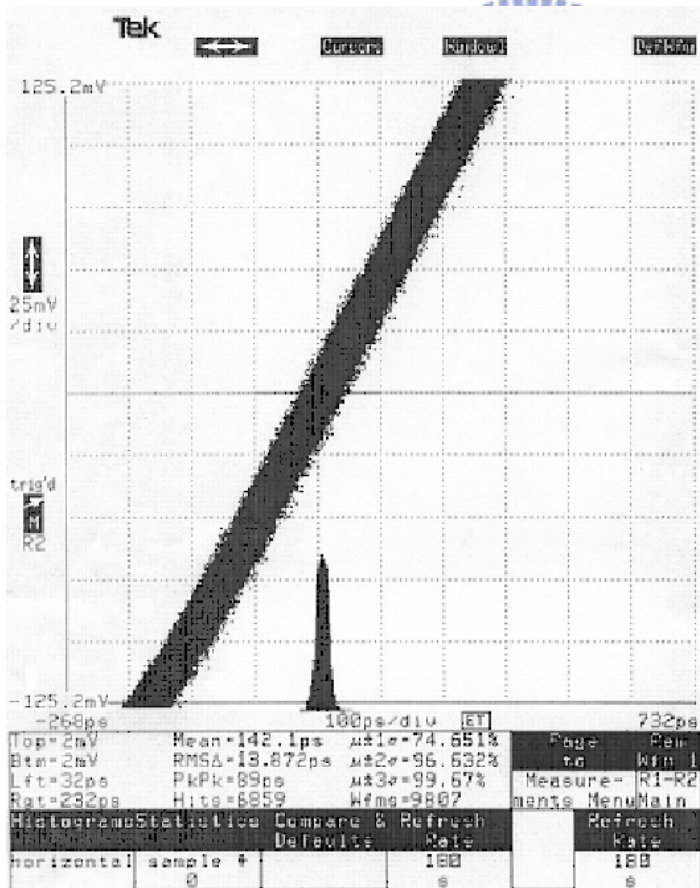


Figure 5.8    The measured jitter of the PLL at 250 MHz. The Pk-Pk jitter is about

89ps.
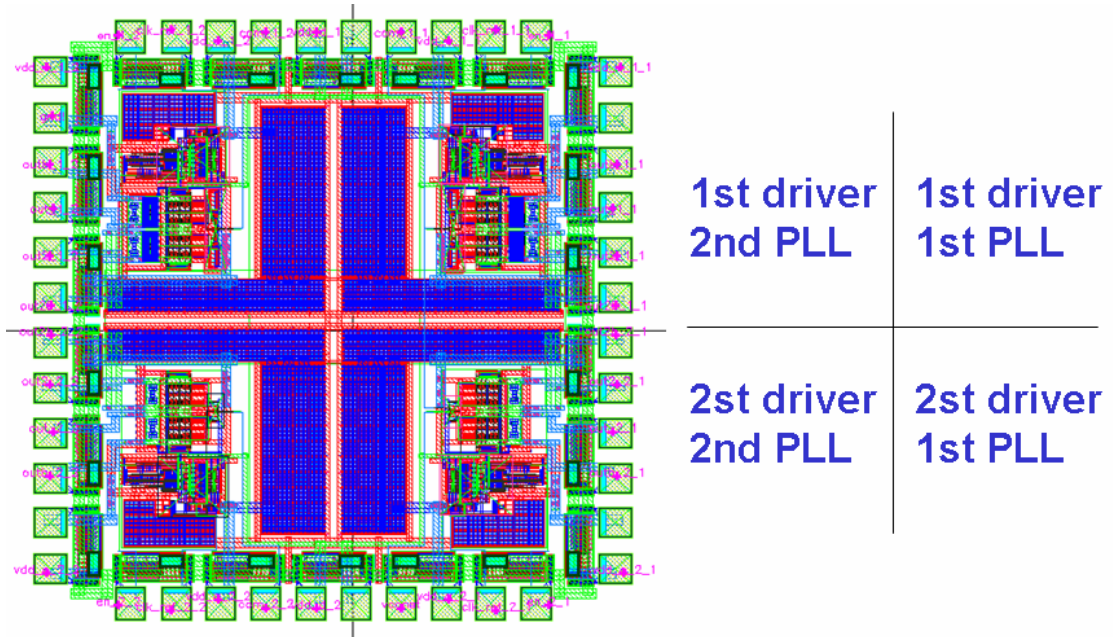
Figure 5.9    The layout of the 2<sup>nd</sup> tap-out



Figre 5.10    Two different kinds of output buffers

77
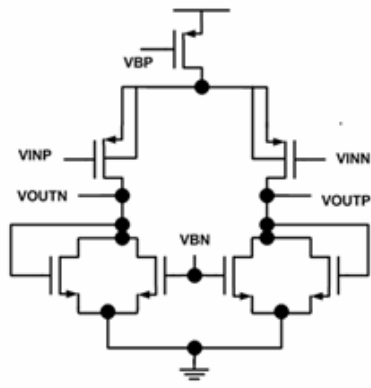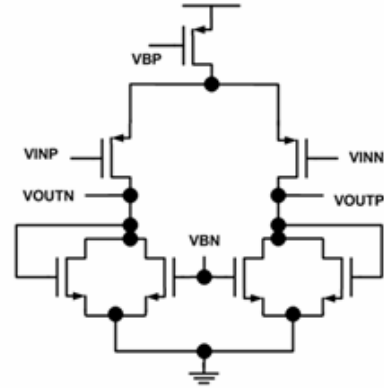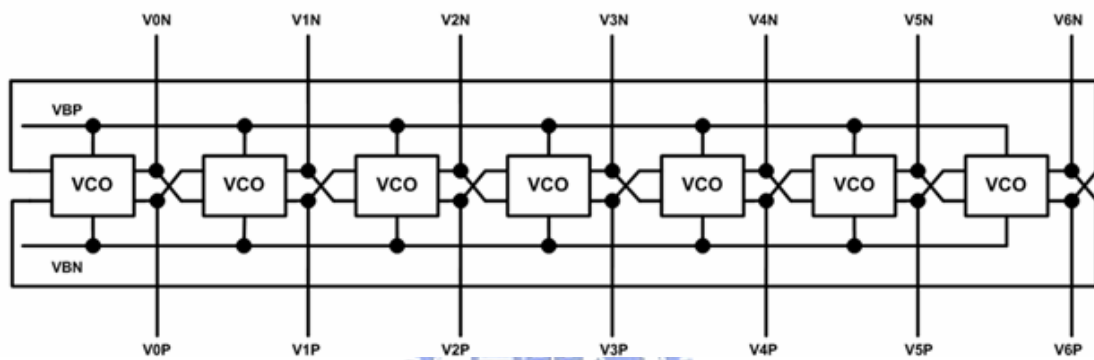
Figure 5.11    Two different kinds of PLL with different VCO
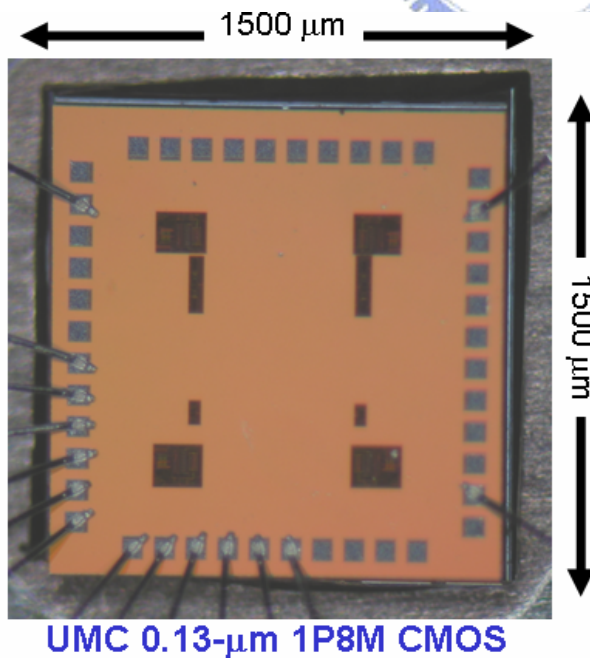


Figure 5.12    The die photo for the 2<sup>nd</sup> tap-out

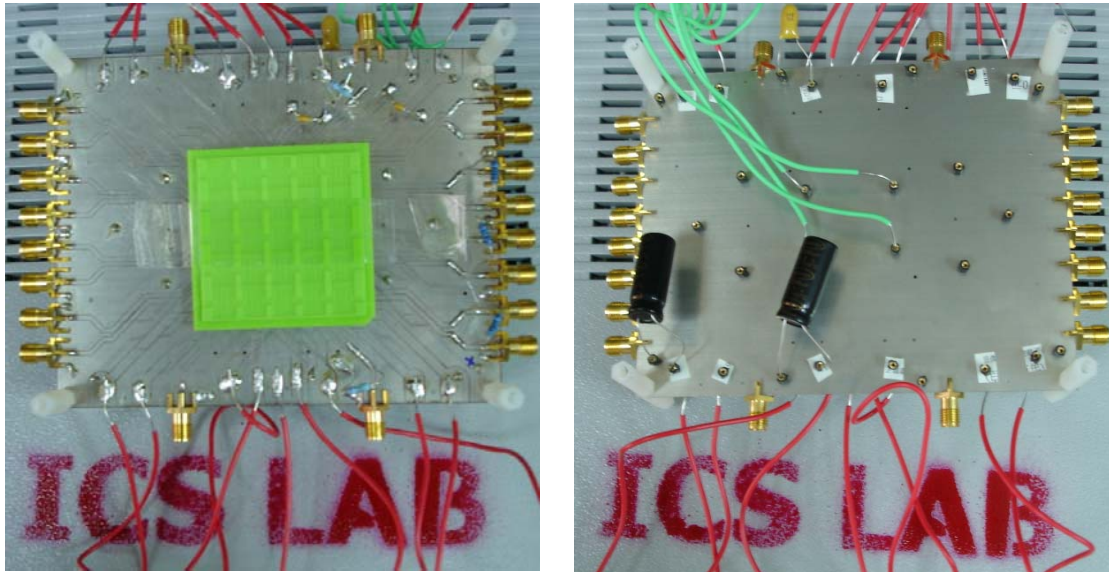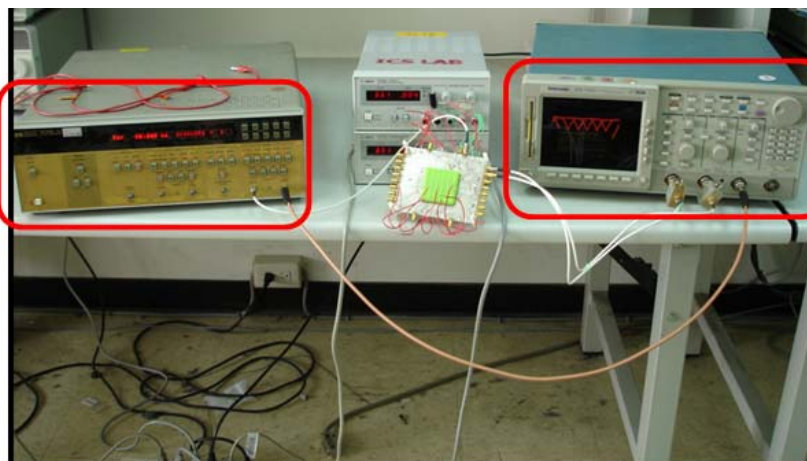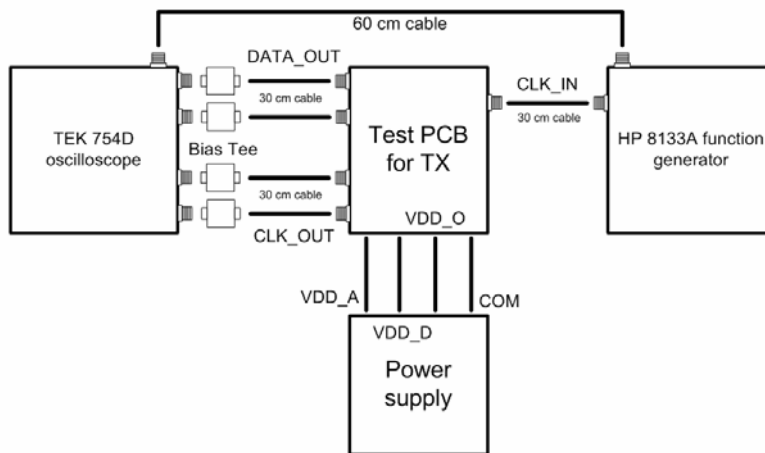Figure 5.13    the PCB for the 2<sup>nd</sup> measurement



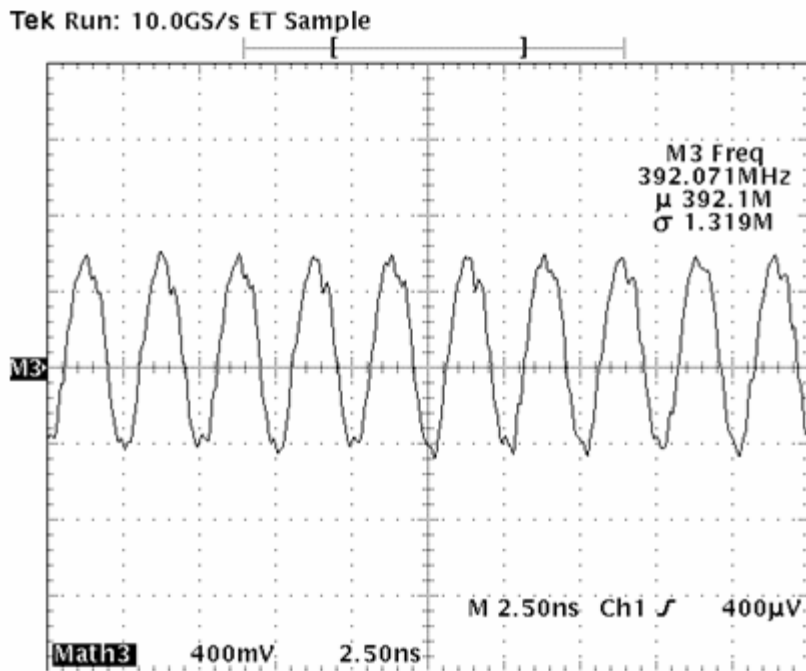Figure 5.14    The measurement setup for 2<sup>nd</sup> measurement

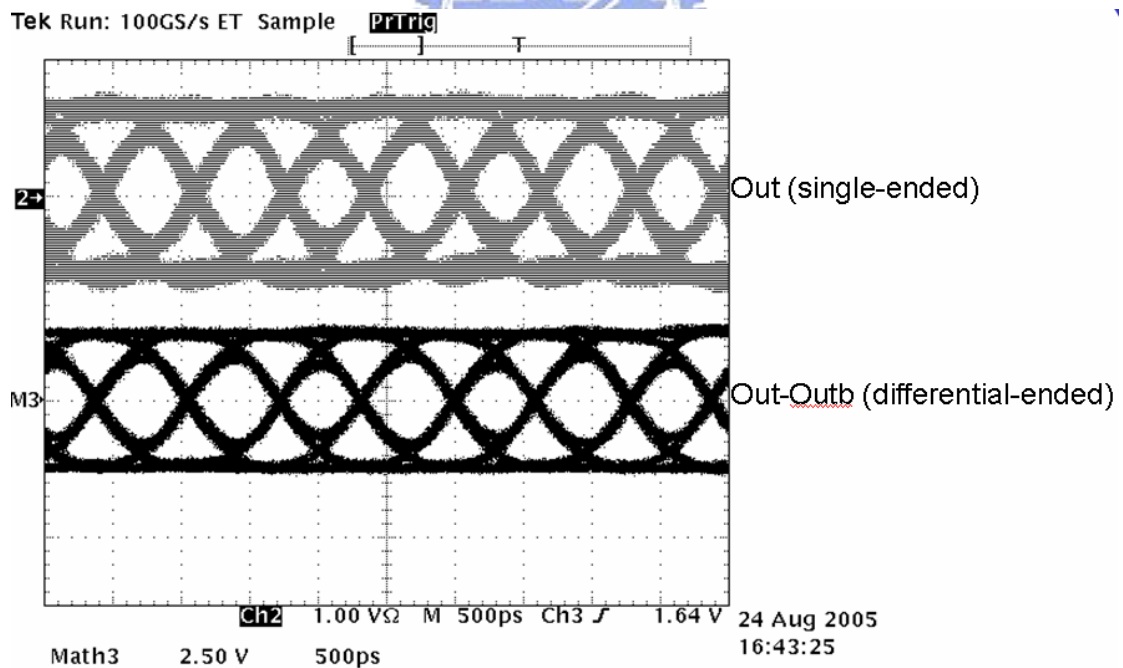Figure 5.15　The measured output for the clock signal at 390 MHz



Figure 5.16　The difference between single ended output and differential ended output. The operating speed is about 1.4 Gb/s.
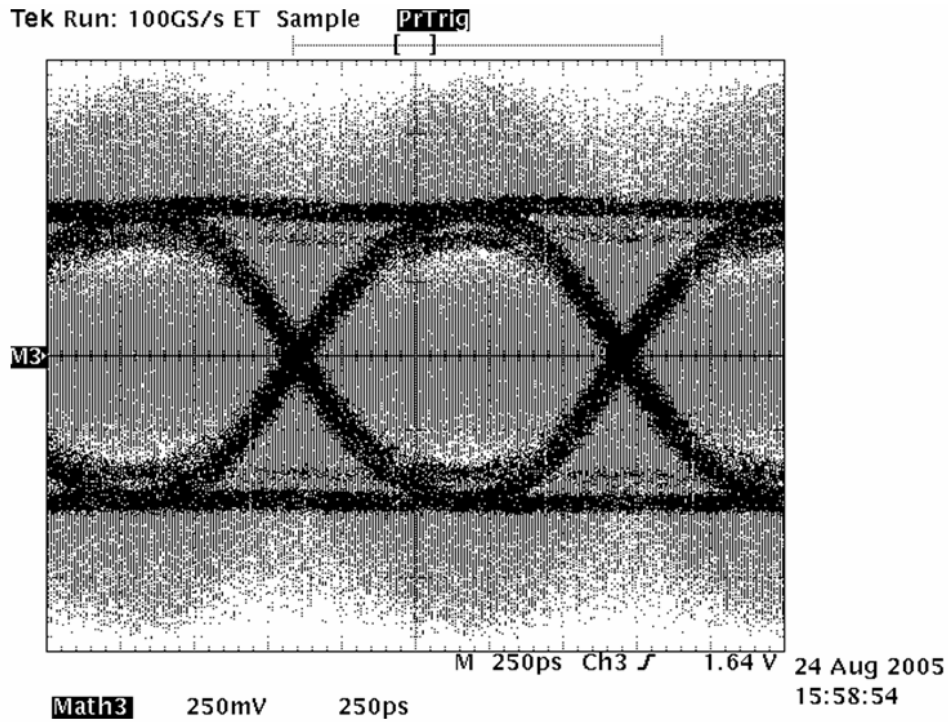
Figure 5.17　The measured eye diagram of the transmitter at 930 Mb/s with 30 cm
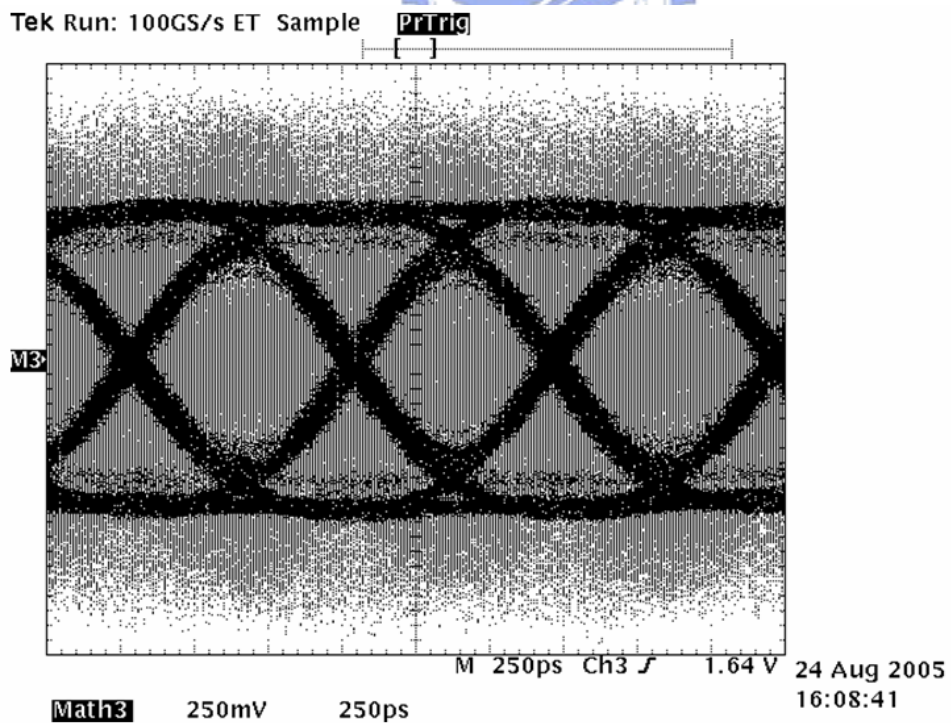cable. The peak-to-peak jitter is 10.4 %.



Figure 5.18　The measured eye diagram of the transmitter at 1.4 Gb/s with 30 cm
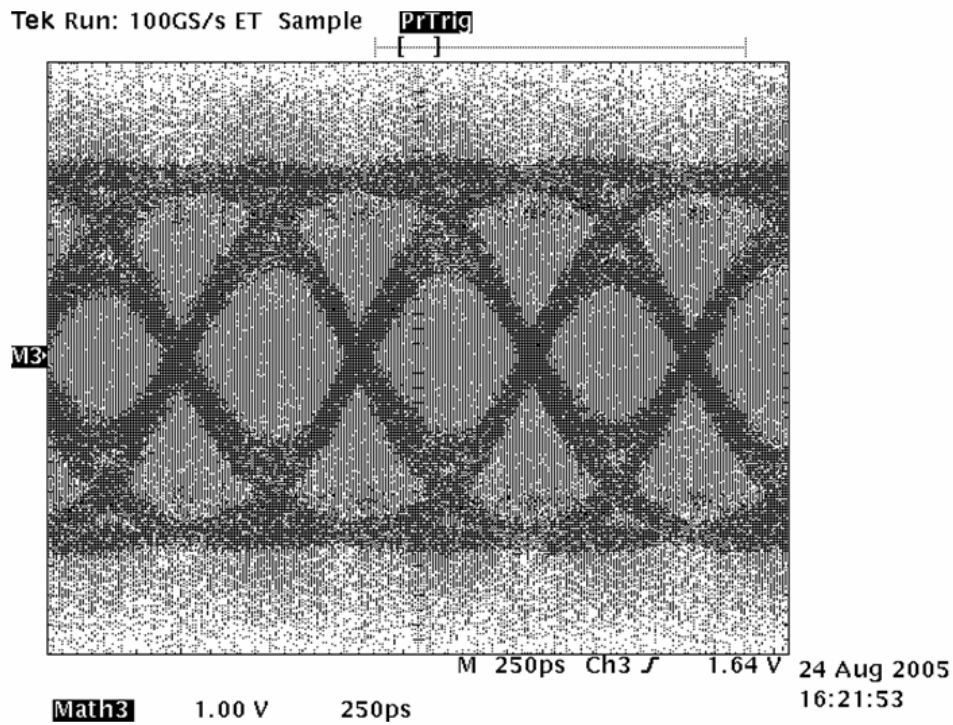cable. The peak-to-peak jitter is 16.1 %.

Figure 5.19   The measured eye diagram of the transmitter at 1.8 Gb/s with 30 cm cable. The peak-to-peak jitter is 17.1 %.
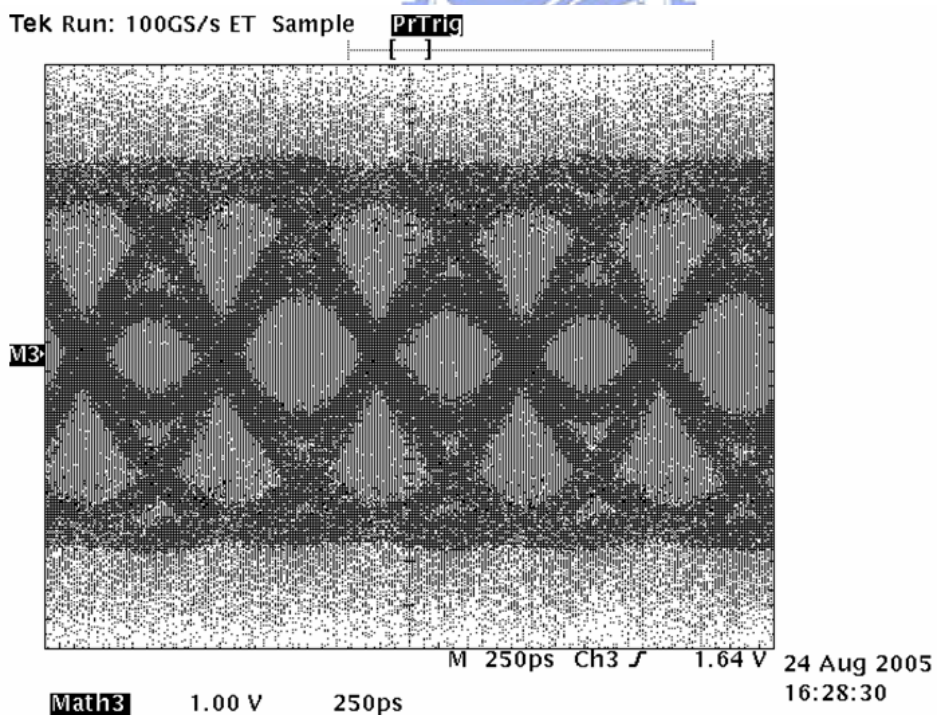


Figure 5.20   The measured eye diagram of the transmitter at 2 Gb/s with 30 cm cable. The peak-to-peak jitter is 25 %.

Figure 5.21    The measured eye diagram of the transmitter at 930 Mb/s with 70 cm

cable. The peak-to-peak jitter is 15.2 %.



Figure 5.22    The measured eye diagram of the transmitter at 1.4 Gb/s with 70 cm

cable. The peak-to-peak jitter is 18.9 %.

Figure 5.23  The measured eye diagram of the transmitter at 1.8 Gb/s with 70 cm cable. The peak-to-peak jitter is 24.1 %.



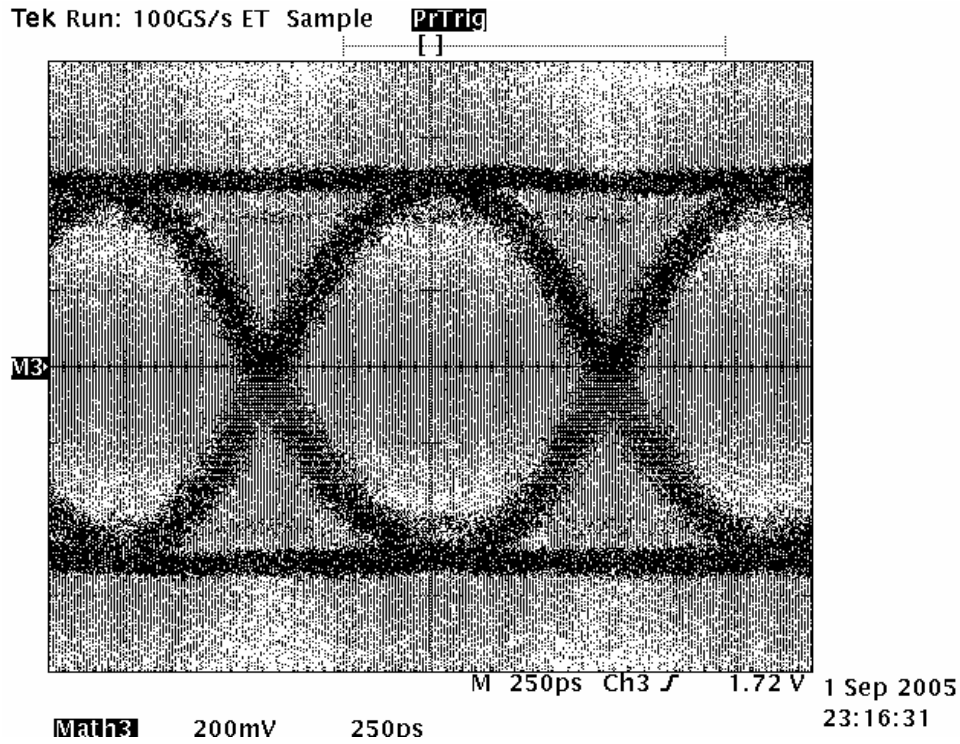Figure 5.24  The measured eye diagram of the transmitter at 2 Gb/s with 70 cm cable. The peak-to-peak jitter is 36 .4%.
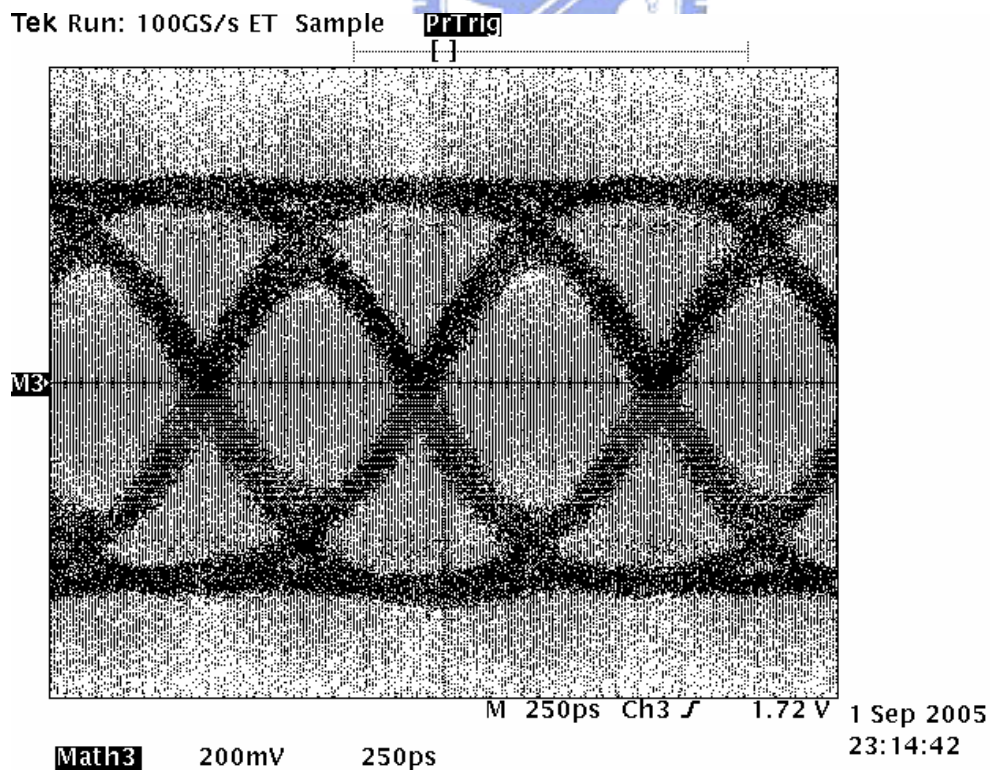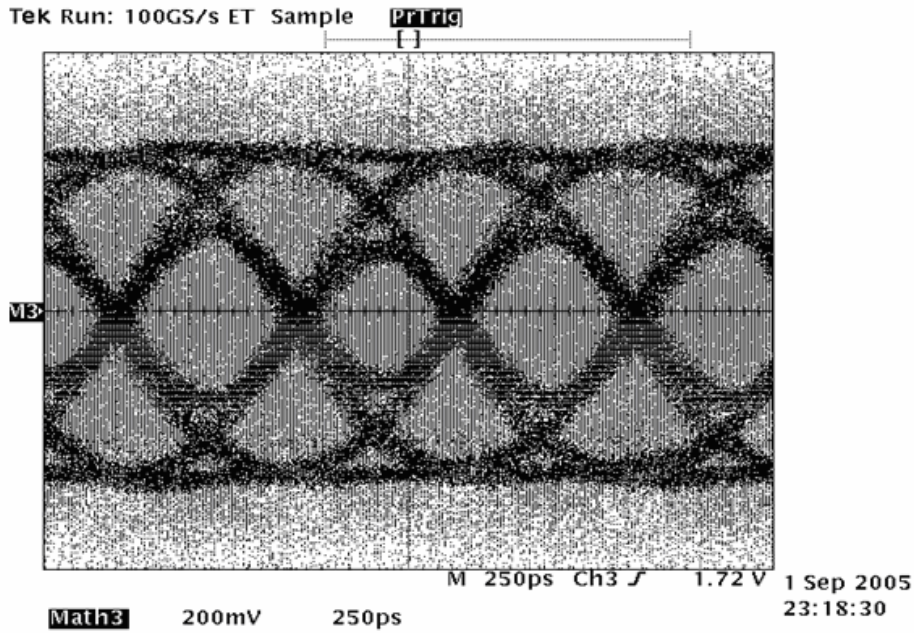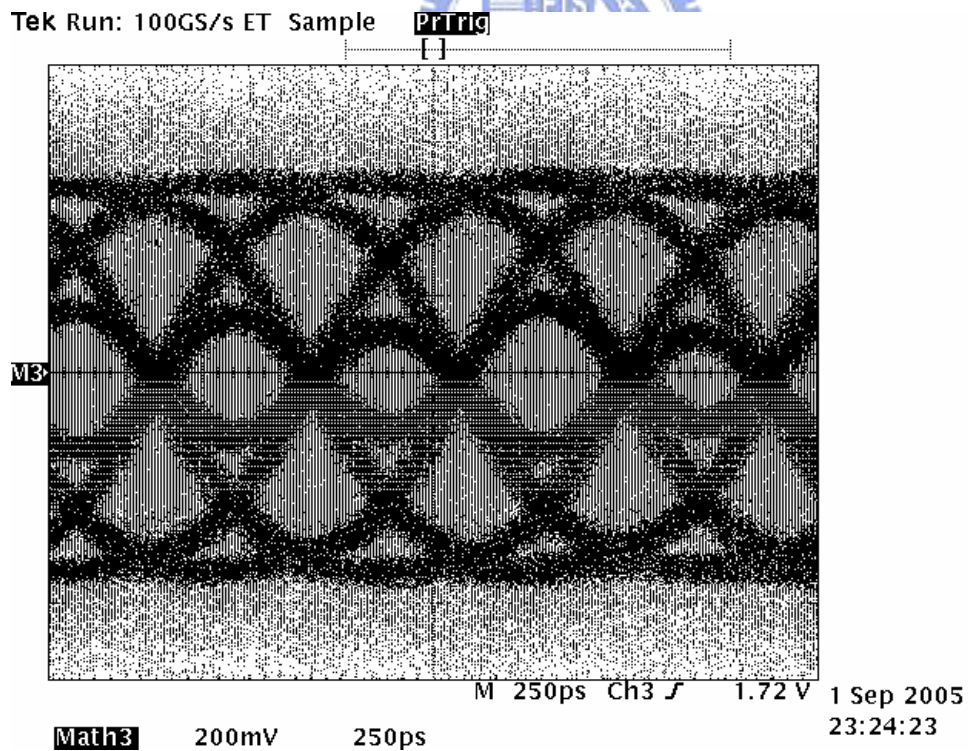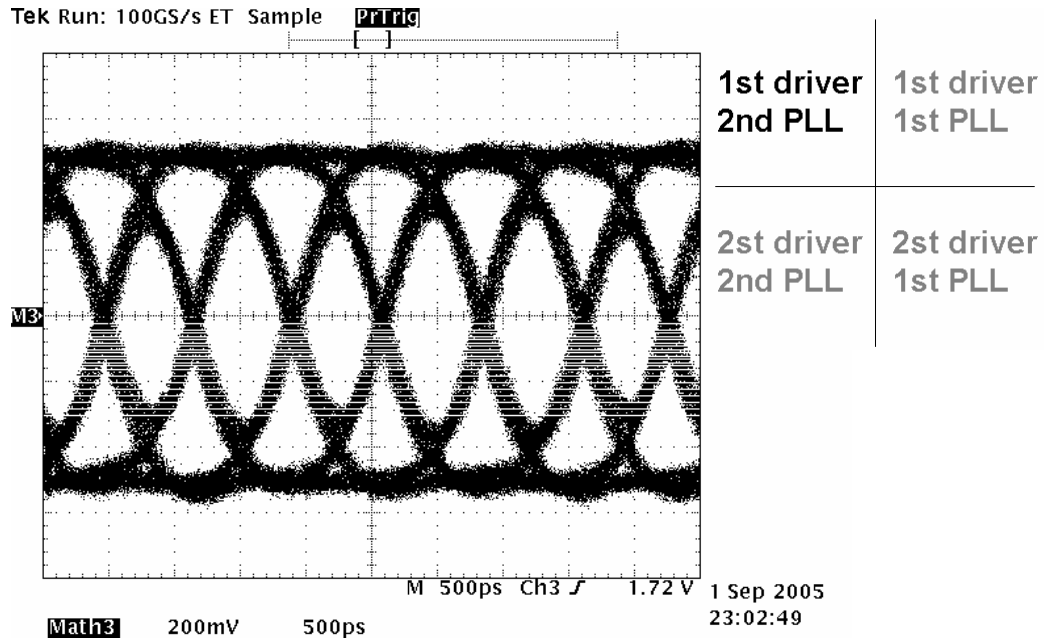
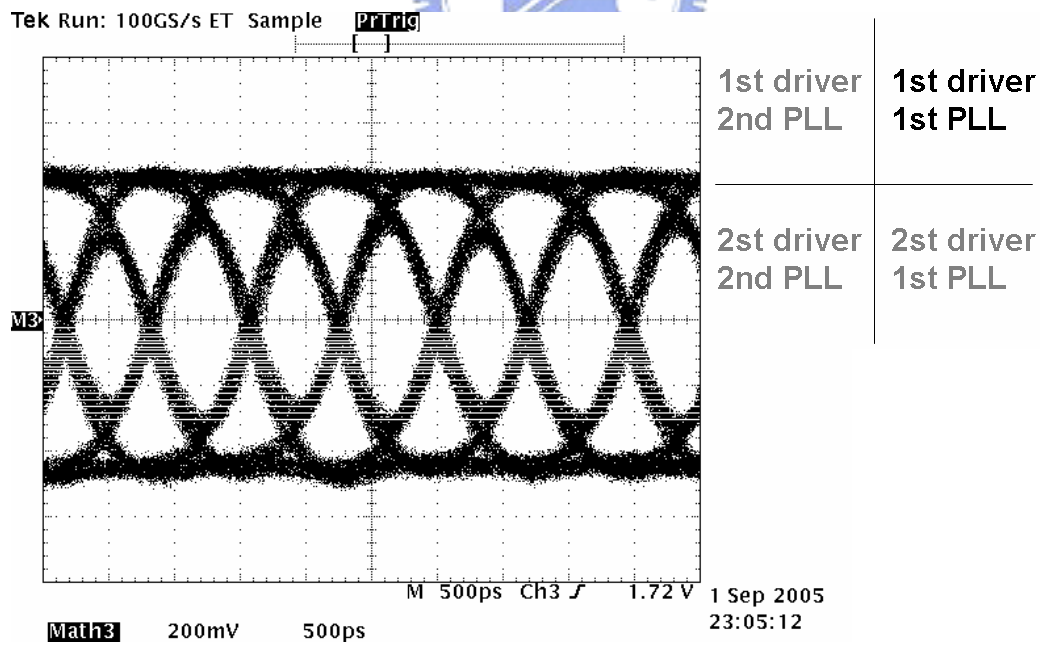Figure 5.25 The measurement result for the 1st quadrant at 1.4 Gb/s



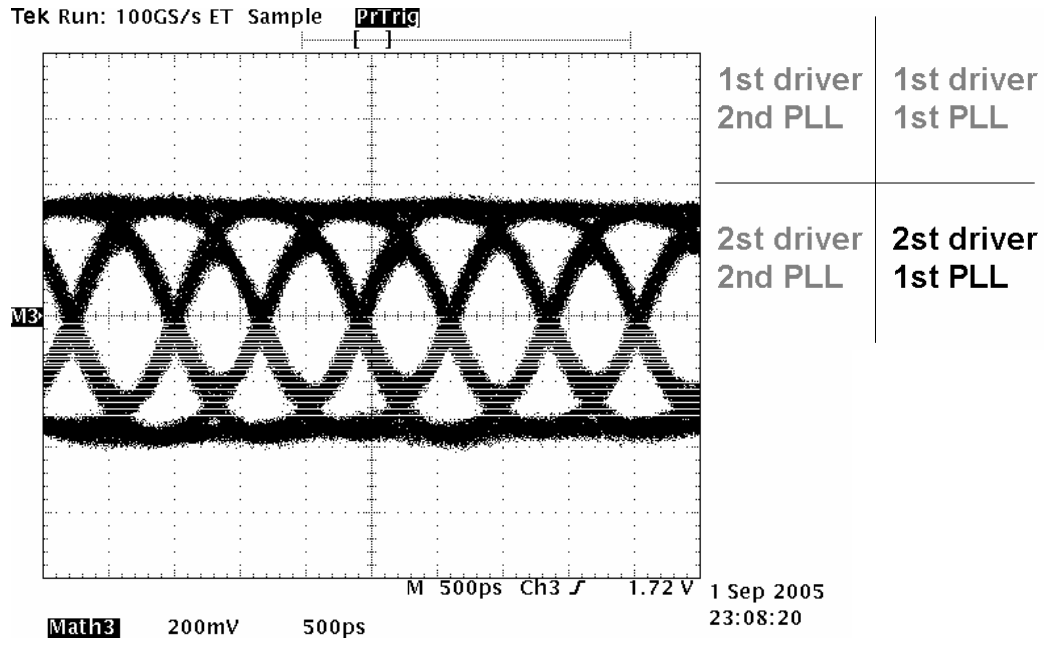Figure 5.26    The measurement result for the 2nd quadrant at 1.4 Gb/s

Figure 5.27    The measurement result for the 4<sup>th</sup> quadrant at 1.4 Gb/s

# Chapter 6

# Conclusion and Future Work

## 6.1 CONCLUSIONS

A transmitter that supports LVDS standard is developed and implemented. The transmitter can convert seven parallel signals into one serial signal. The measured data rate can be up to 1.8 Gb/s, which can support the UXGA resolution of flat panel displays for sure. Besides for this high data rate achievable, the transmitter can also embedded into other system to enhance the performance at lower cost.

The first important building block examined is the PLL. The PLL needs to generate seven phases required for the 7:1 multiplexer to serialize seven parallel data signals into one signal. Therefore the jitter of the PLL should be propagated to the transmitter output as the essential part. Then the transmitter is developed with the PLL and a self-test PRBS. The measurement results are shown in chapter 5. The circuit was implemented in a UMC 0.13μm 1P8M CMOS process with 3.3V device.

## 6.2 FUTURE WORK

From the measurement result, the transmitter can operate properly at 1.8 Gb/s, which verified the function described. There are still many issues need to be improved. The bandwidth-limited channels effect should be carefully treated for higher data rate. Techniques such as modulation, equalization, and coding can provide significant improvement in data bandwidth through transmitting more complex symbols instead of simple bits. The power supply noise should be took care more importantly. The jitter of the PLL should be reduced. The power noise and the PLL layout should be

more carefully handled. The bandwidth of the multiplexer should be enhanced to reduce the ISI problem of the transmitter output.

# REFERENCES

[1] K. Lee, *et al.*, "1.04 GBd low EMI digital video interface system using small swing serial link technique," *IEEE J. Solid-State Circuits,* vol. 33, no. 5, pp. 816-823, May 1998.

[2] *Interfacing between LVPECL, VML, CML, and LVDS levels*, Texas Instruments Inc., USA, 2002.

[3] *LVDS Owner's Manual & Design Guide*, National Semiconductor Corp., Apr. 1997.

[4] *Electrical characteristics of low-voltage differential signaling (LVDS) interface circuits, TIA/EIA-644,* National Semiconductor Corp., *ANSI/TIA/EIA*, 1996.

[5] *IEEE standard for low-voltage differential signaling (LVDS) for scalable coherent interface (SCI), 1596.3 SCI-LVDS standard, IEEE Std.* 1596.3-1996, 1994.

[6] H. Djahanshahi, F. Hansen, and C. A. T. Salama, "Gigabit-per-second ECL-compatible I/O interface in 0.35-um CMOS," *IEEE J. Solid-State Circuits*, vol. 34, no. 8, pp.1074-1083, Aug. 1999.

[7] *Performance of LVDS with different cables*, Texas Instruments Inc., USA, 2002.

[8] *High-speed gigabit data transmission across various cable media at various lengths and data rate*, Texas Instruments Inc., USA, 2000.

[9] *Understanding jitter and bit error for the TLK2500*, Texas Instruments Inc., USA, 2000.

[10] A. Boni, "1.2-Gb/s true PECL 100K compatible I/O interface in 0.35-μm CMOS," *IEEE J. Solid-State Circuits,* vol. 36, no. 6, pp. 979-987, June 2001.

[11]  I. A. Young, J. K. Greason, and K. L. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessor," *IEEE J. Solid-State Circuits*, vol. 27, no. 11, pp. 1599-1607, Nov. 1992.

[12]  J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits,* vol. 31, no. 11, pp. 1723-1732, Nov. 1996.

[13]  J. P. Hein and J. W. Scott, "Z-domain model for discrete-time PLL's", *IEEE Trans. Circuits and Systems*, vol. 35, pp. 1391-1400, Nov. 1988.

[14]  F. M. Gardner, "Charge-pump phase-lock loops", *IEEE Trans. On Commun.*, vol. 28, pp. 1849-1858, Nov. 1980.

[15]  A. Maxim, B. Scott, E. M. Schneider, M. L. Hagge, S. Chacko, and D. Stiurca, "A low-jitter 125-1250-MHz process-independent and ripple-poleless 0.18-μm CMOS PLL based on sample-reset loop filter," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1673-1683, Nov. 2001.

[16]  M. Horowitz, C. K. Yang, and S. Sidiropoulos "High-speed electrical signaling: overview and limitations," *IEEE Micro,* pp. 12-24, Jan./Feb., 1998.

[17]  W. J. Dally and J. Poulton, "Transmitter equalization for 4-Gbps signaling," *IEEE Micro*, pp. 48-56, Jan./Feb., 1997.

[18]  M. Fukaishi et al., "A 4.25-Gb/s CMOS fiber channel transceiver with asynchronous tree-type demultiplexer and frequency conversion architecture," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2139-2147, Dec. 1998.

[19]  M. Fukaishi et al., "A 20-Gb/s CMOS multichannel transmitter and receiver chip set for ultra-high-resolution digital displays," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1611-1618, Nov. 2000.

[20]  *DS90C383/DS90CF384 + 3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link – 65 MHz, + 3.3 V LVDS Receiver 24–Bit Flat Panel Display (FPD) Link – 65 MHz,* National Semiconductor Corp., Nov. 2000.

[21] B. Young, "Enhanced LVDS for signaling on the RapidIO[TM] interconnect architecture," in *Proc. IEEE Int. Electrical Performance of Electronic Packaging Conf., 2000,* pp.17-20.

[22] T. Gabara, W. Fischer, W. Werner, S. Siegel, M. Kothandaraman, P. Metz, and D. Gradl, "LVDS I/O Buffers with a Controlled Reference Circuit," in *Proc. ASIC Conf.* 1997, pp. 311-315.

[23] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O interface for Gb/s-per-pin operation in 0.35-μm CMOS," *IEEE J. Solid-State Circuits,* vol. 36, no. 4, pp. 706-711, Apr. 2001.

[24] S. Jamasb, R. Jalilizeinali, and P.M. Chau, "A 622MHz stand-alone LVDS driver pad in 0.18-μm CMOS," in *Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems*, 2001, pp. 610-613.

# 簡歷

姓　　名：周宗信

學　　歷：

台灣省立台中第一高級中學　　　　　(85 年 9 月~88 年 6 月)

國立交通大學電子工程學系　　　　　(88 年 9 月~92 年 6 月)

國立交通大學電子研究所碩士班　　　(92 年 9 月~94 年 9 月)

研究所修習課程：

| 類比積體電路 I | 吳介琮教授 |
|---|---|
| 類比積體電路 II | 吳重雨教授 |
| 數位積體電路 | 柯明道教授 |
| 積體電路設計實驗 I | 李鎮宜教授 |
| 積體電路設計實驗 II | 李鎮宜教授 |
| 積體電路之靜電放電防護設計特論 | 柯明道教授 |
| 電腦輔助設計 | 周景揚教授 |
| 元件物理（一） | 雷添福教授 |
| 個人通訊 | 林一平教授 |

Email： rihand.ee88@nctu.edu.tw