Static Noise Margin of Ultrathin-Body SOI Subthreshold SRAM Cells—An Assessment Based on Analytical Solutions of Poisson's Equation

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***Abstract*—This paper investigates the static noise margin (SNM) of ultrathin-body (UTB) SOI SRAM 6T/8T cells operating in the subthreshold region using analytical solutions of Poisson's equation validated with TCAD simulations. An analytical framework to calculate the SNM for UTB SOI SRAMs operating in the subthreshold region is presented. Our results indicate that for improving both read SNM (RSNM) and write SNM (WSNM), the back-gating technique is more effective in the subthreshold region than in the superthreshold region. The 6T UTB SOI subthreshold SRAM cell with the back-gating technique by increasing the strength of the pull-up transistors and decreasing the strength of the pass-gate transistors shows comparable RSNM with the 10T bulk subthreshold SRAM and an improvement in RSNM variation. Due to better electrostatic integrity, the back-gating technique (pull-up transistors with positive back-gate bias, pull-down/pass-gate transistors with negative back-gate bias) mitigates the 6T UTB SOI SRAM RSNM variation significantly with some improvement in RSNM. Increasing cell β-ratio shows a limited improvement on RSNM and has no benefit on the SNM variability for the subthreshold operation. The UTB SOI 8T SRAM cell exhibits RSNM 2$\times$ larger than the 6T SRAM cell in the subthreshold region. Both negative bit-line voltage (VBL) and boosted word-line voltage (VWL) are more effective than lower cell supply voltage to improve WSNM, and negative VBL shows a larger improvement in WSNM than boosted VWL.**

***Index Terms*—Poisson's equation, SOI, static noise margin (SNM), subthreshold SRAM, ultrathin body (UTB).**

I. Introduction

SUBTHRESHOLD operation is an efficient technique to achieve ultralow power consumption for circuits by lowering the power supply ($V_{\rm dd}$) below the threshold voltage [1], [2]. Ultrathin-body (UTB) SOI MOSFET with thin buried oxide (BOX) has emerged as a promising candidate to extend CMOS scaling [3]–[5]. Due to its better control of short-channel effects, lower subthreshold swing, and reduced leakage and random dopant fluctuation resulting from the use of undoped (or lightly doped) thin silicon film, UTB SOI MOSFET is very attractive for the subthreshold circuit applications. Conventional 6T bulk subthreshold SRAM cells face many challenges with increasing process variations in deep sub-100 nm technologies [6]–[8]. Various 8T [6] and 10T [7], [8] bulk SRAM cells have been proposed to improve the stability, margin, and performance in the subthreshold region. Several studies have discussed the methodologies for improving the static noise margin (SNM) in UTB SOI (FD/SOI) SRAMs [9]–[11]. However, the stability of UTB SOI 6T/8T SRAMs operating in the subthreshold region has rarely been examined. Furthermore, 6T bulk SRAM cells fail to deliver the density and yield requirement in the subthreshold region due to the reduced SNM, whereas the 6T UTB SOI SRAM cells with the back-gating technique may provide sufficient margin for the subthreshold operation.

In this paper, we present an analytical framework that accurately describes the read static noise margin (RSNM) and write static noise margin (WSNM) for UTB SOI SRAM cells in the subthreshold region. Based on our theoretical model, the methodology for enhancing the stability of UTB SOI SRAMs in the subthreshold region is examined. This paper is organized as follows. In Section II, we describe an analytical UTB SOI subthreshold SRAM framework including an analytical subthreshold current model and the methodology for calculating subthreshold SNM. Section III investigates the RSNM of UTB SOI 6T/8T SRAM cells in the subthreshold ($V_{\rm dd} = 0.4$ V) and superthreshold ($V_{\rm dd} = 1$ V) regions, including the impact of the back-gating techniques. Section IV examines the corresponding WSNM and evaluates the effectiveness of commonly used circuit techniques, such as lower cell supply voltage (VCS), boosted word-line voltage (VWL), and negative bit-line voltage (VBL), for improving WSNM in the subthreshold region. Section V concludes this paper.

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II. Analytical UTB SOI Subthreshold SRAM Framework

A. Analytical Subthreshold Current Model

Our theoretical subthreshold drain current for UTB SOI MOSFET is derived from the analytical potential solution in the subthreshold region. The channel potential distribution

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$\phi_{\mathrm{ch}}(x,y)$ in the subthreshold region satisfies the Poisson's equation

$$\frac{\partial^2\phi_{\mathrm{ch}}(x,y)}{\partial x^2}+\frac{\partial^2\phi_{\mathrm{ch}}(x,y)}{\partial y^2}=-\frac{qN_{\mathrm{ch}}}{\varepsilon_{\mathrm{ch}}}. \tag{1}$$

Since there is no charge in the BOX region, the BOX potential distribution $\phi_{\mathrm{box}}(x,y)$ satisfies the Laplace equation

$$\frac{\partial^2\phi_{\mathrm{box}}(x,y)}{\partial x^2}+\frac{\partial^2\phi_{\mathrm{box}}(x,y)}{\partial y^2}=0 \tag{2}$$

where N_{ch} is the channel doping concentration. $\varepsilon_{\mathrm{ch}}$ is the permittivity of the channel. The required boundary conditions can be described as

$$\phi_{\mathrm{ch}}(T_{\mathrm{ch}},y)+T_i\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i}\cdot\left.\frac{\partial\phi_{\mathrm{ch}}(x,y)}{\partial x}\right|_{x=T_{\mathrm{ch}}}=V_g-V_{\mathrm{fb}} \tag{3a}$$

$$\phi_{\mathrm{ch}}(x,0)=-\phi_{\mathrm{ms}}+V_s \tag{3b}$$

$$\phi_{\mathrm{ch}}(x,L_g)=-\phi_{\mathrm{ms}}+V_d \tag{3c}$$

$$\phi_{\mathrm{box}}(-T_{\mathrm{BOX}},y)=V_{\text{back-gate}}-V_{\text{fb,back-gate}} \tag{3d}$$

$$\phi_{\mathrm{box}}(x,0)=[V_{\text{back-gate}}-V_{\text{fb,back-gate}}]+\frac{(-\phi_{\mathrm{ms}}+V_s)-[V_{\text{back-gate}}-V_{\text{fb,back-gate}}]}{T_{\mathrm{BOX}}}x \tag{3e}$$

$$\phi_{\mathrm{box}}(x,L_g)=[V_{\text{back-gate}}-V_{\text{fb,back-gate}}]+\frac{(-\phi_{\mathrm{ms}}+V_d)-[V_{\text{back-gate}}-V_{\text{fb,back-gate}}]}{T_{\mathrm{BOX}}}x \tag{3f}$$

$$\varepsilon_{\mathrm{ch}}\cdot\left.\frac{\partial\phi_{\mathrm{ch}}(x,y)}{\partial x}\right|_{x=0}=\varepsilon_{\mathrm{ox}}\cdot\left.\frac{\partial\phi_{\mathrm{box}}(x,y)}{\partial x}\right|_{x=0} \tag{3g}$$

$$\left.\frac{\partial\phi_{\mathrm{ch}}(x,y)}{\partial y}\right|_{x=0}=\left.\frac{\partial\phi_{\mathrm{box}}(x,y)}{\partial y}\right|_{x=0} \tag{3h}$$

where T_{ch}, T_i, and T_{BOX} are the thicknesses of channel, gate insulator, and BOX, respectively. L_g is the gate length. ε_i and $\varepsilon_{\mathrm{ox}}$ are the permittivities of gate insulator and BOX, respectively. V_g, $V_{\text{back-gate}}$, V_d, and V_s are the voltage biases of gate, back gate, drain, and source, respectively. V_{fb} and $V_{\text{fb,back-gate}}$ are the flatband voltages of gate and back gate, respectively. ϕ_{ms} is the built-in potential of the source/drain to the channel.

The corresponding 2-D boundary value problem can be divided into two subproblems: a 1-D Poisson's equation and a 2-D Laplace equation. Using the superposition principle, the complete channel potential solution is $\phi_{\mathrm{ch}}(x,y)=\phi_{\mathrm{ch},1}(x)+\phi_{\mathrm{ch},2}(x,y)$, where $\phi_{\mathrm{ch},1}(x)$ and $\phi_{\mathrm{ch},2}(x,y)$ are solutions of the 1-D and 2-D subproblems in the channel, respectively. The 1-D solution $\phi_{\mathrm{ch},1}(x)$ can be expressed as in (4a), (4b), and (4c), shown at the bottom of the page.

In solving the 2-D subproblem, the boundary condition of gate dielectric–channel interface (3a) is simplified by converting the gate dielectric thickness to $(\varepsilon_{\mathrm{ch}}/\varepsilon_i)$ times and replacing the gate dielectric region with an equivalent channel-material region. The electric field discontinuity across the gate dielectric and channel interface can thus be eliminated. For the channel/BOX interface, both potential distribution in the channel $(\phi_{\mathrm{ch},2}(x,y))$ and that in the BOX $(\phi_{\mathrm{box},2}(x,y))$ have to be considered to satisfy the boundary conditions (3g) and (3h).

The 2-D solution $\phi_{\mathrm{ch},2}(x,y)$ can be obtained using the method of separation of variables

$$\begin{aligned}\phi_{\mathrm{ch},2}(x,y)&=\sum_n\{[c_n\cdot\sinh(\gamma_n y)+c_n'\cdot\sinh(\gamma_n(L_g-y))]\\&\quad\cdot\sin(\gamma_n x)+e_n\cdot\sinh(\lambda_n(T_{\mathrm{ch}}+(\varepsilon_{\mathrm{ch}}/\varepsilon_i)T_i-x))\\&\quad\cdot\sin(\lambda_n y)\}\end{aligned} \tag{5a}$$

where

$$\lambda_n=(n\pi)/L_g \tag{5b}$$

$$\gamma_n=(n\pi)/(T_{\mathrm{ch}}+(\varepsilon_{\mathrm{ch}}/\varepsilon_i)T_i). \tag{5c}$$

The coefficients c_n, c_n', and e_n in (5a) can be expressed as

$$\begin{aligned}c_n=\frac{1}{\sinh(\lambda_nL_g)}\Bigg[&2(-\phi_{\mathrm{ms}}+V_d-B)\cdot\frac{1-(-1)^n}{n\pi}\\&+2A\left(T_{\mathrm{ch}}+\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i}T_i\right)\cdot\frac{(-1)^n}{n\pi}\\&+2\left(T_{\mathrm{ch}}+\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i}T_i\right)^2\cdot\frac{(-1)^n-1}{(n\pi)^3}\Bigg]\end{aligned} \tag{5d}$$

$$\begin{aligned}c_n'=\frac{1}{\sinh(\lambda_nL_g)}\Bigg[&2(-\phi_{\mathrm{ms}}-B)\cdot\frac{1-(-1)^n}{n\pi}\\&+2A\left(T_{\mathrm{ch}}+\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i}T_i\right)\cdot\frac{(-1)^n}{n\pi}\\&+2\left(T_{\mathrm{ch}}+\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i}T_i\right)^2\cdot\frac{(-1)^n-1}{(n\pi)^3}\Bigg]\end{aligned} \tag{5e}$$

$$e_n=\frac{(RHS_n/LHS_n)}{\sinh((n\pi/L_g)(T_{\mathrm{ch}}+(\varepsilon_{\mathrm{ch}}/\varepsilon_i)T_i))} \tag{5f}$$

$$\phi_{\mathrm{ch},1}(x)=-\frac{qN_{\mathrm{ch}}}{2\varepsilon_{\mathrm{ch}}}x^2+A\cdot x+B \tag{4a}$$

$$A=\frac{(V_g-V_{\mathrm{fb}})-[V_{\text{back-gate}}-V_{\text{fb,back-gate}}]+\frac{qN_{\mathrm{ch}}}{2\varepsilon_{\mathrm{ch}}}\left(T_{\mathrm{ch}}^2+2\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i}T_iT_{\mathrm{ch}}\right)}{T_{\mathrm{ch}}+\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i}T_i+\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{ox}}}T_{\mathrm{BOX}}} \tag{4b}$$

$$B=\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{ox}}}T_{\mathrm{BOX}}\cdot A+[V_{\text{back-gate}}-V_{\text{fb,back-gate}}] \tag{4c}$$

where

$$LHS_n = \lambda_n \cdot \coth(\lambda_n T_{\text{BOX}}) + \frac{\varepsilon_{\text{ch}}}{\varepsilon_{\text{ox}}}\lambda_n \cdot \coth\left(\lambda_n\left((\varepsilon_{\text{ch}}/\varepsilon_i)T_i + T_{\text{ch}}\right)\right) \tag{5g}$$

$$\begin{aligned} RHS_n = & 2\frac{\varepsilon_{\text{ch}}}{\varepsilon_{\text{ox}}}A \cdot \frac{1-(-1)^n}{n\pi} \\ & + \sum_m \Bigg\{ \Bigg[c_n \cdot \frac{\frac{(2\varepsilon_{\text{ch}}/\varepsilon_{\text{ox}})\cdot(-1)^{n+1}}{n\pi}\cdot \sinh(\lambda_m L_g)}{1+(\gamma_m/\lambda_n)^2} \\ & + c'_n \cdot \frac{\frac{(2\varepsilon_{\text{ch}}/\varepsilon_{\text{ox}})}{n\pi}\cdot\sinh(\lambda_m L_g)}{1+(\gamma_m/\lambda_n)^2}\Bigg] \\ & \cdot \lambda_m - d_n \frac{m\pi}{T_{\text{BOX}}}\frac{(-1)^{m+n+1}}{n\pi} \\ & \cdot \frac{2\sinh\left(\frac{m\pi}{T_{\text{BOX}}}L_g\right)}{1+(\gamma_m/\lambda_n)^2} - d'_n \frac{m\pi}{T_{\text{BOX}}}\frac{(-1)^m}{n\pi} \\ & \cdot \frac{2\sinh\left(\frac{m\pi}{T_{\text{BOX}}}L_g\right)}{1+(\gamma_m/\lambda_n)^2}\Bigg\} \end{aligned} \tag{5h}$$

$$\begin{aligned} d_n = & \frac{2}{\sinh(\gamma_n L_g)}\Bigg\{[V_{\text{back-gate}} - V_{\text{fb,back-gate}}] \\ & \cdot \frac{1-(-1)^n}{n\pi} + [(-\phi_{\text{ms}} + V_d - B)] \\ & \cdot \frac{(-1)^{n+1}}{n\pi}\Bigg\} \end{aligned} \tag{5i}$$

$$\begin{aligned} d'_n = & \frac{2}{\sinh(\gamma_n L_g)}\Bigg\{[V_{\text{back-gate}} - V_{\text{fb,back-gate}}] \\ & \cdot \frac{1-(-1)^n}{n\pi} \\ & + [(-\phi_{\text{ms}} - B)] \cdot \frac{(-1)^{n+1}}{n\pi}\Bigg\}. \end{aligned} \tag{5j}$$

Our analytical potential solution has been verified with TCAD simulation [12]. Fig. 1 shows that our model is fairly accurate for various channel doping (N_{ch}). Based on the potential solution, the subthreshold current can be derived by

$$I_d = \frac{q\mu_n W(kT/q)\left(n_i^2/N_{\text{ch}}\right)\left[1-\exp\left(-V_d/(kT/q)\right)\right]}{\int_0^{L_g} dy \Big/ \int_0^{T_{\text{ch}}} \exp\left[q\phi_{\text{ch}}(x,y)/(kT)\right]dx}. \tag{6}$$

Fig. 2(a)–(d) shows that our UTB subthreshold current model is quite applicable across relevant ranges of important device design parameters such as T_{ch}, L_g, $V_{\text{back-gate}}$, and V_d. The UTB SOI subthreshold current model shows excellent agreement with TCAD simulations for UTB SOI devices.

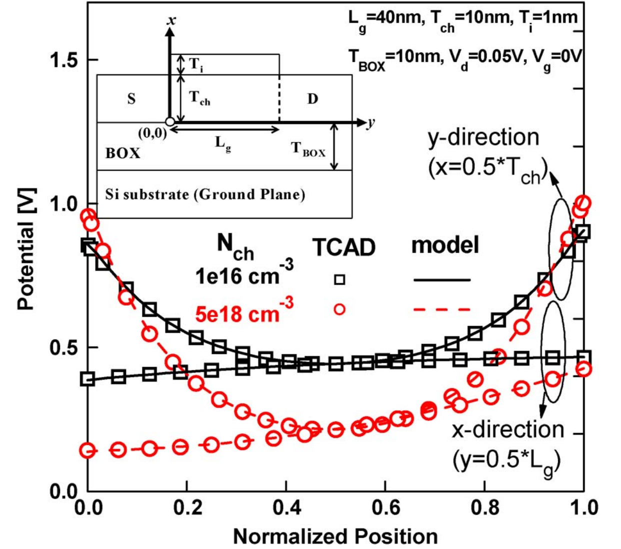


Fig. 1. Analytical potential distributions compared with the results of TCAD simulations. Inset shows the schematic sketch of UTB SOI MOSFET with thin BOX structure investigated in this paper.

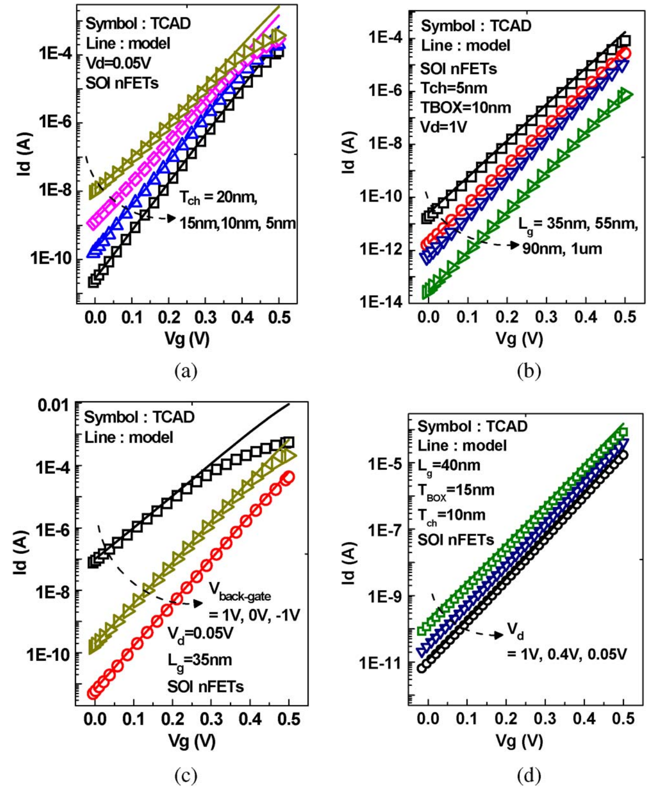


Fig. 2. Comparison of the UTB SOI subthreshold current model with TCAD simulations across ranges of important device design parameters such as (a) T_{ch}, (b) L_g, (c) $V_{\text{back-gate}}$, and (d) V_d. The UTB SOI subthreshold current model shows excellent agreement with TCAD simulations.

B. Methodology for Analytical Subthreshold SNM Calculation

The SNM is defined as the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell. With the subthreshold current model, the SNM can be derived by solving Kirchhoff's current conservation law at cell storage nodes VR and VL, respectively [13]: $\text{I(NR)} = \text{I(PR)} + \text{I(AR)}$, $\text{I(NL)} = \text{I(PL)} + \text{I(AL)}$. The SNM is obtained from the maximum possible square method, which is defined as

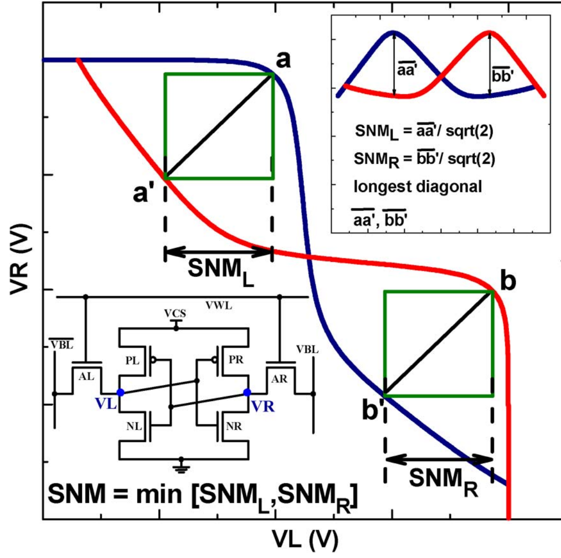


Fig. 3. By solving Kirchhoff's current conservation law at cell storage nodes VR/VL, the cell static transfer characteristics can be obtained. The SNM estimation is based on "maximum possible square" method. Inset shows that with a 45° rotated coordinate system, the longest diagonal can be easily obtained.

the square with the longest diagonal, as shown in Fig. 3. The longest diagonal can be easily obtained by using a 45° rotated coordinate system, as shown in the Fig. 3 inset [14]. Thus, the SNM is determined by the minimum value between SNM_L and SNM_R. Fig. 4(a) and (b) shows that our analytical framework to calculate the subthreshold SNM for the UTB SOI SRAM shows excellent agreement with TCAD simulations for Hold, Read, and Write modes. Thus, RSNM and WSNM [15], [16] can be obtained from Fig. 4(b), respectively.

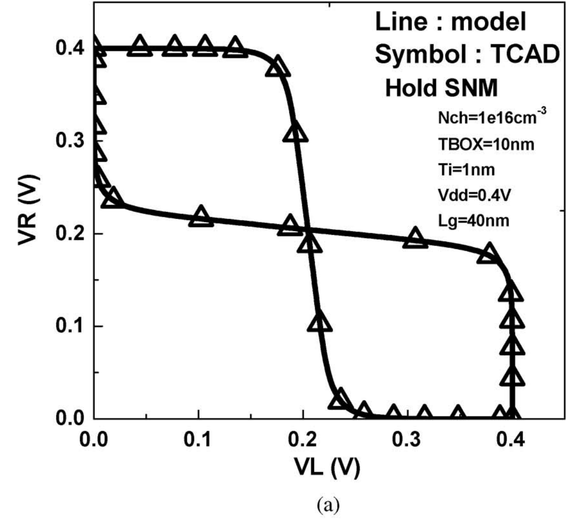
In the following sections, we investigate the RSNM and WSNM for the UTB SOI SRAMs with $N_{\mathrm{ch}} = 1e16\ \mathrm{cm}^{-3}$, $T_{\mathrm{BOX}} = 10$ nm, $L_g = 40$ nm, $T_i = 1$ nm, $T_{\mathrm{ch}} = 10$ nm, at $V_{\mathrm{dd}} = 0.4$ V (subthreshold) and 1.0 V (superthreshold). Notice that a single midgap work function is used. The use of midgap gate material allows a single electrode for both NMOS and PMOS. It also provides high threshold voltage for both NMOS and PMOS to reduce the SRAM cell leakage, and enables the subthreshold operation with a reasonable V_{dd}. Furthermore, it is consistent with the cost consideration for the subthreshold SRAMs for which the intended applications are cost-sensitive implantable devices, medical instruments, and wireless sensor network.

III. RSNM FOR UTB SOI SUBTHRESHOLD SRAMs

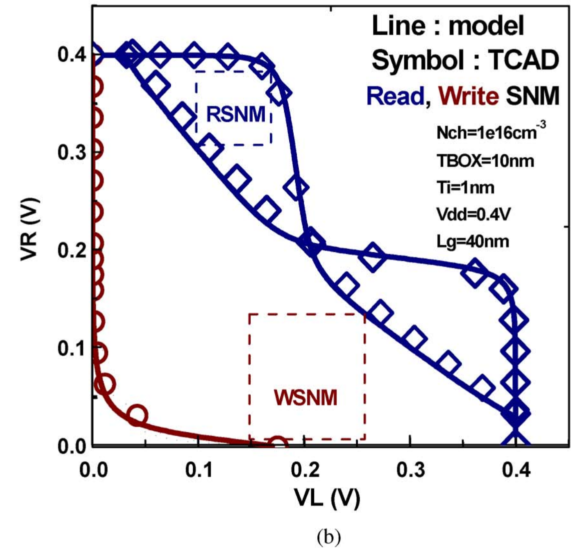
This section analyzes the impact of the back-gating technique on RSNM of the UTB SOI SRAMs in the subthreshold mode and superthreshold mode, and compares several methods (listed in Table I: Read Mode) to improve RSNM and variability.

A. Impact of the Back-Gate Bias on RSNM

The back-gating technique can be used in UTB SOI SRAMs to enhance its stability and margin. However, the extent of the



(a)



(b)

Fig. 4. Analytical framework to calculate the subthreshold SNM for the UTB SOI SRAM cell verified with TCAD simulations for (a) Hold, (b) Read, and Write modes.

improvement in RSNM by using the back-gating technique is different between the subthreshold mode ($V_{\mathrm{dd}} = 0.4$ V) and the superthreshold mode ($V_{\mathrm{dd}} = 1$ V). Fig. 5(a) shows the schematic of a 6T UTB SOI SRAM cell with the back-gating technique for case (A), (B), and (C) listed in Table I. Fig. 5(b) shows the normalized RSNM comparison between the subthreshold and superthreshold modes. From case (A) to case (B), the back-gate bias (V_{bgp}) of the pull-up transistors (PL, PR) changes from V_{dd} to 0 V, which lowers the threshold voltage (V_{th}) of PL/PR. The lowered V_{th} of PL/PR increases the trip voltage of the cell inverter to help prevent the data flip during Read operation, thus improving the RSNM [17]. From case (B) to case (C) ($V_{\mathrm{bgax}} = -0.4$ V, Below-GND back-gate bias), the back-gate bias (V_{bgax}) of pass-gate transistors (AL, AR) changes from 0 to -0.4 V, which increases the V_{th} of AL/AR. The increased V_{th} of AL/AR helps reduce the Read disturb voltage in the cell storage node to improve the RSNM. Fig. 5(b) shows that case (B) and case (C) show 23% and 61% RSNM improvement in the subthreshold mode, respectively; and only

TABLE I
UTB SOI SRAM CELLS FOR INVESTIGATING RSNM/WSNM, RSNM VARIATION, AND PERCENT CHANGE IN RSNM

UTB SOI SRAM		case	cell	Cell β-Ratio	Vbgp (V)	Vbgax (V)	Vbgn (V)
◆Subthreshold mode (Vdd = 0.4V) ◆Superthreshold mode (Vdd = 1V)	Read Mode	(A)	6T	1	**Vdd**	**0**	
		(B)	6T	1	**0**	**0**	
		(C)	6T	1	**0**	**-0.4**	
	Write Mode	(H)	6T	1	**0**	**0**	
		(I)	6T	1	**Vdd**	**0**	
		(J)	6T	1	**Vdd**	**Vdd**	
Subthreshold mode (Vdd = 0.4V) Read Mode		(D)	6T	1	**0.4**		**-0.4**
		(E)	6T	1	**1**		**-1**
		(F)	6T	**2**	0		0
		(G)	**8T**	1	0		0

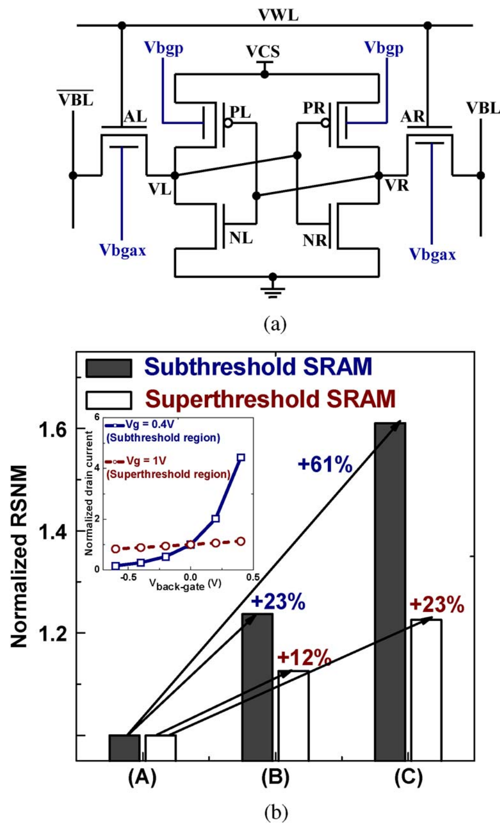


Fig. 5. (a) Schematic of a 6T UTB SOI SRAM cell with the back-gating technique for case (A), (B), and (C). The back-gate bias of the pull-down transistors (NL, NR) is connected to GND. For the subthreshold mode, $V_{\mathrm{dd}} = 0.4$ V; for the superthreshold mode, $V_{\mathrm{dd}} = 1$ V. (b) Normalized RSNM comparison between the subthreshold mode (model) and the superthreshold mode (TCAD mixed-mode simulation). Inset shows the impact of the back-gate bias on normalized drain current for both the subthreshold region and superthreshold region.

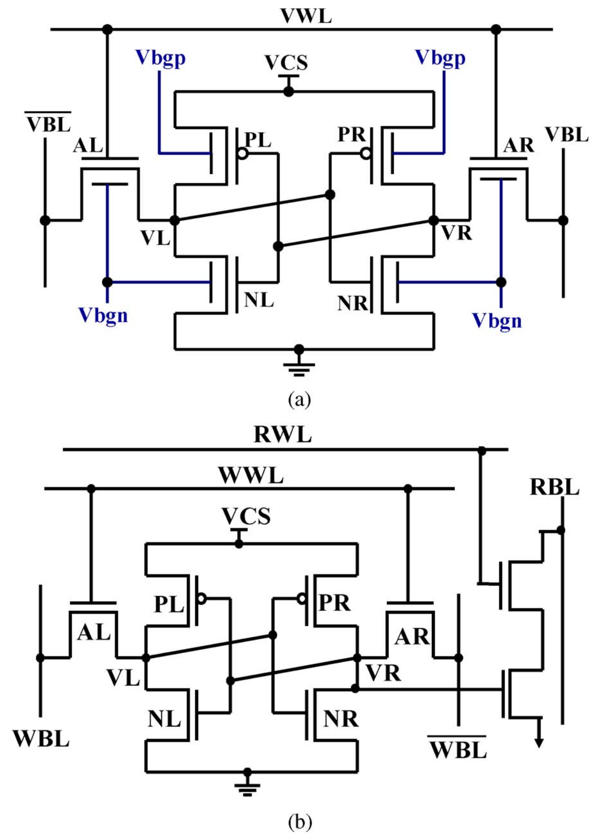


Fig. 6. (a) Schematic of a 6T SRAM cell with the back-gating technique for case (D) and (E) listed in Table I. (b) Schematic of an 8T SRAM cell for case (G) listed in Table I.

12% and 23% RSNM improvement in the superthreshold mode. Therefore, the back-gating technique is more effective in the subthreshold mode than in the superthreshold mode to improve the stability of the SRAM cell. The impact of the back-gate bias on the normalized drain current in the subthreshold and superthreshold region is shown in the Fig. 5(b) inset. It can be clearly seen that the normalized drain current is more sensitive to the back-gate bias in the subthreshold region than in the superthreshold region, and this is the reason that the back-gating technique is more effective for the SRAM cell operating in the subthreshold mode.

B. RSNM for UTB SOI Subthreshold SRAMs

Fig. 6(a) shows the schematic of a 6T SRAM cell with the back-gating technique for case (D) and (E) listed in Table I. Case (F) indicates a 6T SRAM cell with cell β-ratio $= 2$. Cell

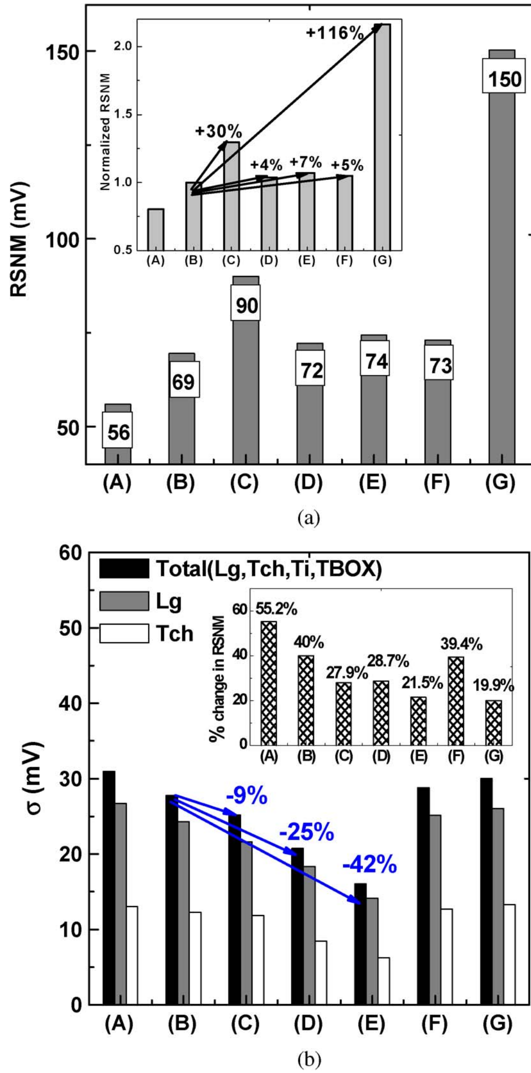


Fig. 7. Comparison of different UTB SOI SRAM cell structures (listed in Table I) on (a) RSNM, (b) RSNM variation caused by parameter variation such as $L_g, T_{\rm ch}, T_i, T_{\rm BOX}$ variation (-20% to 20%), and percent change in RSNM. The 6T SRAM cell with $V_{\rm bgax} = -0.4$ V (Below-GND back-gate bias) shows 30% improvement in RSNM. The 8T SRAM cell [case (G)] shows 2× larger RSNM. The 6T SRAM cell with $V_{\rm bgp} = 1$ V and $V_{\rm bgn} = -1$ V (case (E), Above-$V_{\rm dd}$/Below-GND back-gate bias) shows a significant improvement in RSNM variability.

β-ratio is defined as the ratio of the pull-down transistors (NL, NR) width/length (W/L) to the pass-gate transistors (AL, AR) W/L. Fig. 6(b) is the schematic of an 8T SRAM cell for case (G), which has been known to have better RSNM and lower $V_{\rm MIN}$ due to decoupling of Read current path from the cell storage node. Fig. 7 compares the nominal RSNM, RSNM variation (σ), and percent change in RSNM for UTB SOI subthreshold SRAM cells listed in Table I. RSNM variation (σ) caused by parameter (P) variation is defined as: $\sigma = [\mathrm{RSNM(P + 20\%)} - \mathrm{RSNM(P - 20\%)}]$. Percent change in RSNM is defined as the ratio of σ to the nominal RSNM. Fig. 7 shows that from case (B) to case (C), increasing the $V_{\rm th}$ of pass-gate transistors by using the back-gating technique results in 30% improvement in the nominal RSNM and 9% improvement in RSNM variation. The pass-gate NFET with negative back-gate bias [case (C)] has better electrostatic integrity, which improves its RSNM

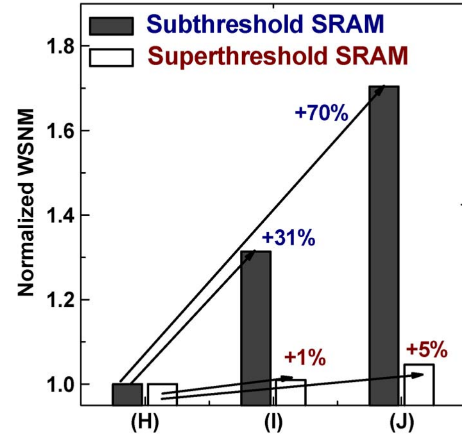


Fig. 8. Normalized UTB SOI SRAM WSNM comparison between the subthreshold mode (model) and the superthreshold mode (TCAD mixed-mode simulation) for various back-gating techniques listed in Table I.

variation. The nominal RSNM of case (C) (90 mV at $V_{\rm dd} = 0.4$ V) is comparable to the value of the 10T bulk subthreshold SRAM cell (∼90 mV at $V_{\rm dd} = 0.4$ V) [8]. In other words, the 6T UTB SOI SRAM cell with the back-gating technique can provide sufficient margin for the subthreshold operation as compared with the 10T bulk subthreshold SRAM cell. The 8T UTB SOI SRAM cell [case (G)] shows 116% larger nominal RSNM compared with the 6T cell [case (B)]. The 6T UTB SOI SRAM cell with $V_{\rm bgp} = 1$ V and $V_{\rm bgn} = -1$ V (case (E), Above-$V_{\rm dd}$/Below-GND back-gate bias) mitigates the RSNM variation significantly by 42% and improves RSNM by 7% as compared with case (B). Thus, case (G) and case (E) show comparable percent change in RSNM, as shown in Fig. 7(b) inset. Increasing cell β-ratio [case (F)] improves nominal RSNM by 6% and shows no benefit on the RSNM variation suppression. Therefore, case (F) shows comparable percent change in RSNM as case (B).

IV. WSNM FOR UTB SOI SUBTHRESHOLD SRAMs

This section compares the impact of the back-gating technique on WSNM in the subthreshold mode and superthreshold mode, and evaluates the effectiveness of commonly used circuit techniques to improve WSNM for UTB SOI subthreshold SRAMs.

A. *Impact of the Back-Gate Bias on WSNM*

Aside from RSNM, the back-gating technique is also quite effective for improving WSNM. Fig. 8 compares WSNM for different kinds of the back-gating techniques listed in Table I in the subthreshold and superthreshold modes. From case (H) to case (I), the back-gate bias ($V_{\rm bgp}$) of the pull-up transistors (PL, PR) changes from 0 V to $V_{\rm dd}$, which increases the $V_{\rm th}$ of PL/PR. The data holding current through PL/PR reduces because of the increased $V_{\rm th}$ of PL/PR which makes the cell easier to flip during Write operation. From case (I) to case (J), the back-gate bias ($V_{\rm bgax}$) of the pass-gate transistors (AL, AR) changes from 0 V to $V_{\rm dd}$, which lowers the $V_{\rm th}$ of AL/AR. Thus, the Write current from the cell storage node to the bit

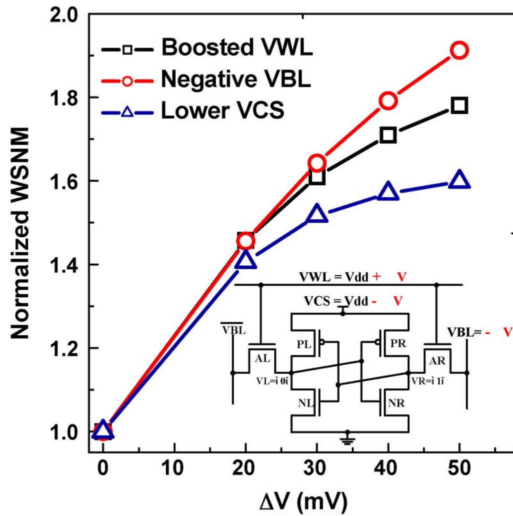


Fig. 9. Comparison of the normalized WSNM for UTB SOI subthreshold SRAM cell for different circuit techniques including boosted VWL, negative VBL, and lower VCS. Inset shows the schematic of these three circuit techniques to improve WSNM for 6T UTB SOI subthreshold SRAM cell.

line through AL/AR increases which improves the WSNM. Fig. 8 shows that the back-gating technique is more effective in improving WSNM in the subthreshold mode than in the superthreshold mode. This is because the ratio of the pass-gate current to the pull-up (holding) current is larger in the subthreshold mode than in the superthreshold mode when the back-gating technique is used.

B. Effectiveness of Circuit Techniques in Improving WSNM for UTB SOI Subthreshold SRAMs

Fig. 9 compares the normalized WSNM for UTB SOI subthreshold SRAM cell with techniques shown in Fig. 9 inset including boosted VWL, negative VBL and lower VCS. Both boosted VWL and negative VBL increase the strength of the pass-gate transistors (AL, AR) and improve WSNM. Lower VCS makes pull-up transistors (PL, PR) weaker to facilitate Write operation. Lower VCS also makes latching effect weaker, which hinders Write operation. For the WSNM improvement, both negative VBL and boosted VWL are more effective than lower VCS, and negative VBL shows a larger improvement in WSNM than boosted VWL. Notice that boosted VWL increases the V_{GS} of the access pass-gate transistors (AL. AR), while negative VBL increases both V_{GS} and V_{DS} of the access pass-gate transistors.

V. Conclusion

An analytical framework to calculate SNM for UTB SOI SRAMs operating in the subthreshold region is presented to investigate the RSNM and WSNM. For both the RSNM and WSNM improvement, the back-gating technique is more effective in the subthreshold mode than the superthreshold mode. The 6T UTB SOI subthreshold SRAM cell with the back-gating technique (case (C), $V_{\mathrm{bgax}} = -0.4$ V, Below-GND back-gate bias) shows comparable RSNM with the 10T bulk subthreshold SRAM cell and an improvement in RSNM variation. The 6T UTB SOI SRAM cell with $V_{\mathrm{bgp}} = 1$ V and $V_{\mathrm{bgn}} = -1$ V (case (E), Above-V_{dd}/Below-GND back-gate bias) mitigates the RSNM variation significantly by 42% with some improvement in RSNM. Increasing cell β-ratio shows a limited improvement on RSNM and has no benefit on SNM variability for the subthreshold operation. The UTB 8T SRAM cell exhibits RSNM 2× larger than the 6T SRAM cell in the subthreshold region. For the WSNM improvement, both negative VBL and boosted VWL are more effective than lower VCS, and negative VBL shows a larger improvement in WSNM than boosted VWL.

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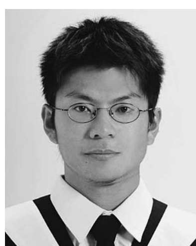

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