國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

超寬頻無線網路應用之
低功率互補金氧半射頻前端發射器設計

Low Power CMOS RF Transmitter Front-End Design for
Ultra-Wideband Wireless Applications

研 究 生：黃相霖　　Hsiang-Lin Huang

指導教授：溫瓌岸　博士　　Dr. Kuei-Ann Wen

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超寬頻無線網路應用之

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摘　要

本論文針對超寬頻(UWB)無線網路應用提出低功率互補式金氧半(CMOS)射頻前端發射器之設計。本文提出之前級放大器(Pre-Amplifier)採用低功率電流共用散佈並接放大器架構，使 PMOS 與 NMOS 電晶體偏壓於相同直流電流，以達成低功耗和超寬頻之設計目標。經由 0.18-μm CMOS 製程進行電路實作，量測出 1-7.9GHz 的超大頻寬與 15mW 的極低功耗，同時具有 7.3dB 的最大功率增益、2dBm 的最大輸出功率，驗證此低功率電流共用散佈並接放大器架構之優點。將此優異放大器架構應用於超寬頻射頻前端發射器，再利用回授電阻固定輸出電壓，以保持其優異特性，加上被動式混波器，以符合低功耗與高頻寬之要求。封裝量測結果顯示，超寬頻的前端發射器在 3-8.3 GHz 可獲得平均功率轉換增益-12dB 有著±2dB 變動，同時在 LO 頻率 3.4GHz 的測試下有著 0dBm 的最大輸出功率。此超寬頻射頻前端發射器參考多頻帶正交頻率多重分割技術規格草案的第一、二、三頻帶組需求，運作頻帶從 3GHz 到 8.3GHz，並以射頻/基頻共同模擬來驗證其高增益以及良好線性度之特性。

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National Chiao-Tung University

ABSTRACT

This thesis presents a low-power design of a direct conversion CMOS RF transmitter front-end for ultra-wideband (UWB) wireless applications. To achieve low power consumption and wide operating bandwidth, the proposed Pre-amplifier employing low power dc feedback current reuse distributed amplifier which the dc current flows through the PMOS to NMOS transistors to reuse the same bias current. A circuit implementation in 0.18-μm CMOS process shows a 1-7.9GHz bandwidth. The amplifier provides a maximum forward gain (S21) of 7.3dB while drawing 15 mW from a 1.6V supply. The maximum output power of 2dBm has been measured. In this thesis, design optimization for the low power current reuse distributed amplifier in wide bandwidth applications is also presented. The novel topology of current reuse distributed amplifier is applied to the RF front-end design for the UWB direct conversion transmitter and uses the feedback resistance to fix the output dc voltage in order to maintain excellent performance. In the RF front-end, a wideband passive mixer is designed for the purpose of low power, and high bandwidth before the Pre-amplifier. The measurement results exhibit that the UWB direct conversion transmitter of package version achieves conversion gain of -12dB from 3-8.3GHz with ±2 dB variation, and obtain

the maximum output power of 0dBm at LO frequency 3.4GHz. The UWB transmitter front-end referenced to the band group #1, 2 and 3 of the Multi-Band OFDM with operation frequency range 3-8.3 GHz demonstrates low power, high gain, and wide bandwidth. It is also verified by a RF/Baseband co-simulation.

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誌于　　2005

黃相霖

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Chapter 1

Introduction

Recently, the Federal Communications Commission (FCC) in US approved the use of ultra-wideband (UWB) technology for commercial applications in the 3.1-10.6 GHz [1]. UWB provide unprecedented high-connectivity consumer products in the home, such as video conferencing, wireless video and audio distribution systems, new home entertainment appliances, diskless computers, and position location and navigation applications. This technology will be potentially a necessity in our daily life, from wireless USB to wireless connection between DVD player and TV, and the expectable huge market attracts various industries. The IEEE 802.15.3a task group (TG3a) is currently developing a UWB standard from the proposals submitted by different companies. It is now left with two primary proposals, Multi-Band OFDM and Direct Sequence UWB. The newly unlicensed UWB opens doors to wireless high-speed communications and has been exciting tremendous academic research interest.

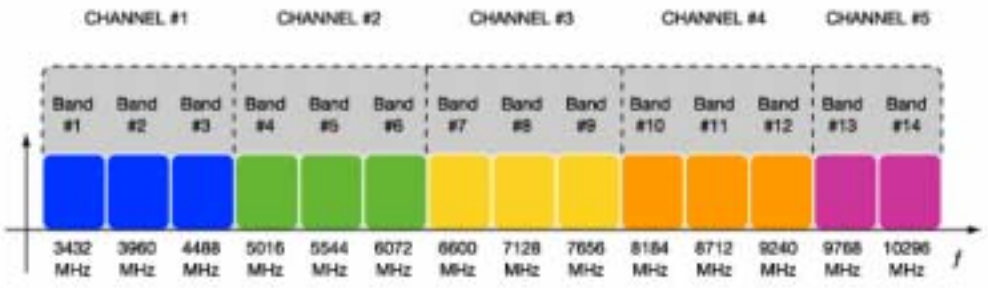


Figure 1.1 The Multi-Band OFDM frequency band plan[1]

1.1 Motivation

The IEEE802.15.3a task group sets targets of low power consumption and low cost. The complementary metal-oxide semiconductor (CMOS) technology is the best candidate to make it since the physical layer implemented in CMOS process consumes less power than others and can be easily integrated with existing MAC layer implemented in CMOS technology and consequently lowers cost much [2]. The research goal of this thesis is to implement a low-power transmitter front-end in the low-cost CMOS technology for wireless UWB applications. As a consequence, a low power preamp of ultra-wide bandwidth and mixers are required to cover all the frequency of interest, and according system budget the total power consumption of transmitter should be limited in 20mW. According to the Table 1.1, the power consumption for transmit path in 0.13μm topology for high speed is 180mW. The power consumption by using 0.18μm topology in 1.6V power supply is 221.5mW. Figure 1.2 shows that each block of power consumption.

$$180mW \times \frac{1.6}{1.3} = 221.5mW$$

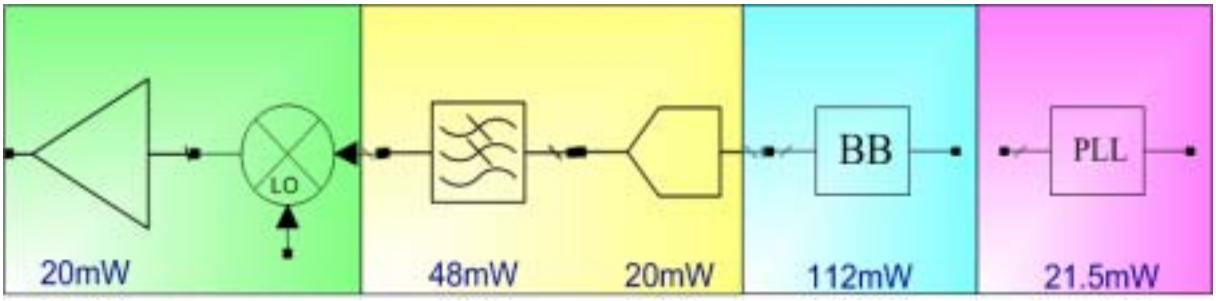


Figure 1.2 Suggested system power consumption

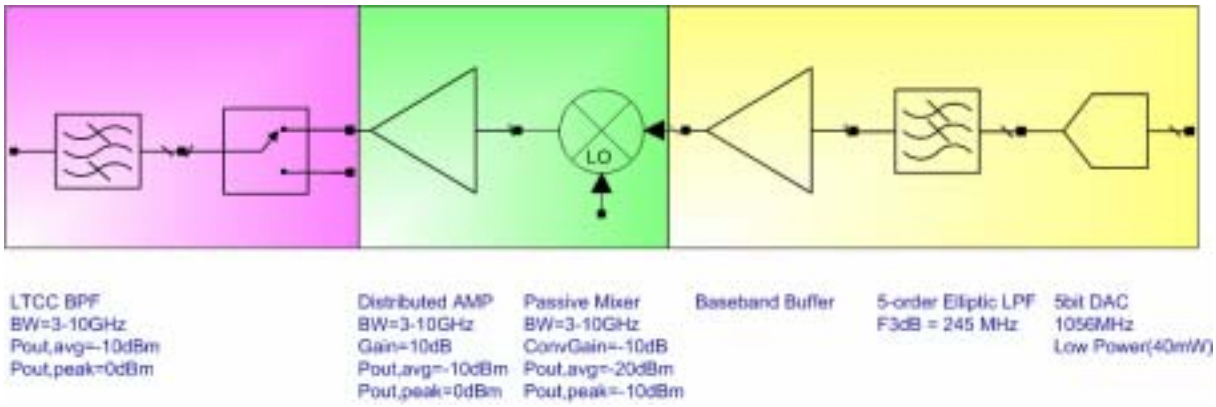


Figure 1.3 System Budget

Figure 1.3 shows the system budget that the specification of UWB transmitter is defined. The UWB transmitter includes the up-conversion mixer and distributed amplifier. The output power of transmitter should be larger than 0dBm and bandwidth is 3-10GHz. For low power issue, the power consumption should be limited in 20mW.

Process Node	Rate (Mb/s)	Transmit	Receive
90 nm	110	93 mW	155 mW
	200	93 mW	169 mW
	480	145 mW	236 mW
130 nm	110	117 mW	205 mW
	200	117 mW	227 mW
	480	180 mW	323 mW

Table 1.1. Power consumption for Mode1 DEV(3-Band)

1.2 Organization of Thesis

The content of this thesis is focused on analysis CMOS transmitter front-end and applications in actual design for IEEE 802.15.3a WLAN system. The organization of this thesis is overviewed as follows.

Chapter 2 gives some basic concept in RF transmitter design.

Chapter 3 provides the analysis of current reuse distributed amplifier. The analysis will be focused on power gain. A novel topology with current reuse feature is proposed.

Chapter 4 demonstrates the application of the proposed transmitter in the UWB system with verification by RF/Baseband co-simulation.

In Chapter 5, the low power UWB preamp is implemented in 0.18μm CMOS technology and performs in measurement results. The preamp is further modified and integrated with up-conversion mixers to constitute a UWB transmitter front-end to specifically fit the requirements of Band Group #1, 2 and 3 of the MB-OFDM proposal. And some measurement results will be described.

In Chapter 6, concludes with a summary of contributions and suggestions for future work.

Chapter 2

Basic Concepts in RF Transmitter Design

This chapter presents some basic concepts in UWB transmitters design, the general design considerations will be introduced including both system level and circuit level. Beginning with introduction to transmitter design considerations, Section 2.2 describes the concept of distributed amplifiers. In Section 2.3, distributed amplifier topologies and concept are discussed Section 2.4 gives a general introduction to transmitter mixers.

2.1 Transmitter Design Considerations

A transmitter front-end composes of a mixer and pre-amplifier. In the transmitter design, the signal level comes out from baseband circuit is quite large, even about 100dB larger than the noise. As a consequence, the noise contribution of transmitter is comparatively small and becomes negligible. The noise contribution of transmit path is not as critical as that of the receive path. To process the large power without distortion, the major goal of transmitter design is to achieve a high linearity performance. Since the signals are processed by these cascaded stages, it is important to know how to obtain high IP3 and P1dB. Consider two or more nonlinear stages in cascade as shown in Figure 2.1 [3]. If the input-output characteristics of each stage are expressed, respectively, as

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.1}$$

$$y_2(t) = \beta_1 y_1(t) + \beta_2 y_1^2(t) + \beta_3 y_1^3(t) \tag{2.2}$$

M

the input third intercept point can be derived as

$$\frac{1}{A_{IP3}^2} \approx \frac{1}{A_{IP3,1}^2} + \frac{\alpha_1^2}{A_{IP3,2}^2} + \frac{\alpha_1^2 \beta_1^2}{A_{IP3,3}^2} + \mathrm{K} \tag{2.3}$$

where $A_{IP3,1}$ and $A_{IP3,2}$ represent the input IP3 of the first and second stages and so on.

From equation (2.3), it can be simply observed that the nonlinearity of latter stages becomes more critical to overall IIP3 performance and the gain of the front stages would degrade the overall IIP3. From this point of view, the preamp in the transmitter front-end must have high IP3, and the high gain of upconversion mixers is prohibited.

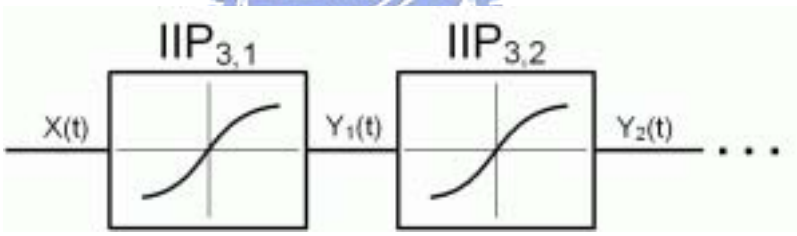


Figure 2.1 Cascaded Nonlinearity Stages

Besides, the P1dB is another parameter to measure nonlinearity. It is well-known that the odd order distortion may degrade the magnitude of fundamental component, and P1dB occurs when the magnitude of fundamental component decreases by 1dB. In the normal operation, it must be ensured all devices are worked in the correct bias condition. If any device leaves the correct bias condition, the signal will suffer from large distortion and become more nonlinearity.

2.2 Concept of Distributed Amplifier(DA)

The distributed amplification using a cascade of discrete transistors allows a more relaxed gain-bandwidth trade-off than a conventional amplifier. By combining the input and output capacitances of the transistors with lumped inductors to form artificial transmission lines, DA is capable of giving a flat, low-pass response up to very high frequencies. Consequently, DAs find many applications in wideband systems such as UWB which has lately drawn an enormous attention and interest due to its potential for short-range high-speed wireless applications including automotive collision-detection systems, through-wall imaging systems, high-speed indoor networking, etc. GaAs based DAs were well developed in 1980's [4]-[7], owing to high transistor cut-off frequencies, low loss and high isolation of the III-V substrate. Recently, DAs in complementary metal oxide semiconductor (CMOS) process have emerged due to their integration ability with baseband circuits, the enhancement of the cut-off frequency of silicon transistors, and low cost [8]-[13].

Although, the wideband characteristic of DAs is suitable for UWB systems, the total power consumption of all cascaded stages of DAs tends to be too high to meet the low power requirement which is one of the most important design criteria in the applications for UWB systems [14].

2.2.1. Discrete Transmission Line

In a common source distributed amplifier, a discrete component transmission line is constructed out of the gate-source input admittance-the gate line. Another identical transmission line structure is drain-source input admittance-the drain line. If the gate transmission structures and drain transmission structures are identical, a wave can be launched

on the gate line and be coherently amplified onto the drain line. It is a simple matter to construct transmission line with identical properties on the gate and drain lines assuming a unilateral transistor over a very wide range of frequencies. Consider the following circuit (Z and Y are arbitrary complex impedances and admittance, respectively, and all voltages and currents are phasors) [15]:

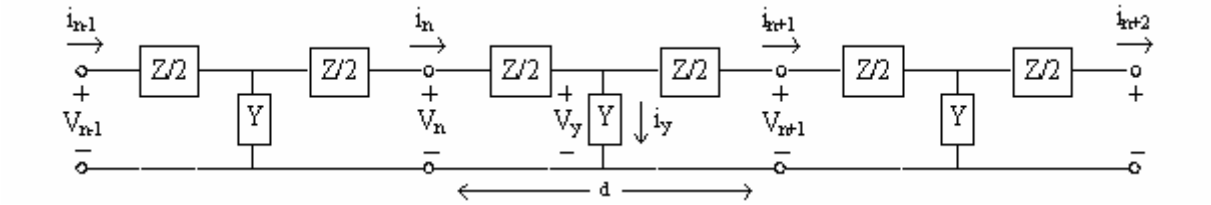


Figure 2.2 LC ladder

Applying Kirchoff's laws to the circuit we arrive at the following equations:

$$\left.\begin{aligned} i_y &= Yv_y \\ i_n &= i_{n+1} + i_y \\ v_n - v_y &= \tfrac{1}{2}Zi_n \\ v_y - v_{n+1} &= \tfrac{1}{2}Zi_{n+1} \end{aligned}\right\} \Rightarrow \left\{\begin{aligned} i_{n-1} - (ZY+2)i_n + i_{n+1} &= 0 \\ v_n - v_{n+1} - \tfrac{1}{2}Z(i_n + i_{n+1}) &= 0 \end{aligned}\right. \tag{2.4}$$

Assuming traveling waves on the circuit of the form, $v_n = Ve^{-j\theta n}, i_n = Ie^{-j\theta n}$, we obtain the following expressions for the wave impedance and phase shift per segment

$$\begin{aligned} Z_{line} &= \sqrt{\tfrac{Z}{Y}}\cos\tfrac{1}{2}\theta = \sqrt{\tfrac{Z}{Y}}\sqrt{1+\tfrac{1}{4}ZY} \\ \theta &= \cos^{-1}(1+\tfrac{1}{2}ZY) = 2\sin^{-1}\sqrt{-\tfrac{1}{4}ZY} \end{aligned} \tag{2.5}$$

For a line consisting of ideal shunt capacitors and ideal series inductors we have:

$$Z_{line} = \sqrt{\frac{L}{C}}\sqrt{1+\frac{1}{4}ZY} \quad \text{where} \quad \omega_c = \frac{2}{\sqrt{LC}}. \tag{2.6}$$

A parallel analysis for a π section discrete transmission line yields:

$$Z_{line} = \sqrt{\frac{L}{C}} / \sqrt{1-\frac{\omega^2}{\omega_c^2}} \quad \text{where} \quad \omega_c = \frac{2}{\sqrt{LC}} \tag{2.7}$$

Form equation (2.7) we see that the impedance of the line is frequency dependent and the line has a cutoff frequency such that no waves of higher frequency can propagate. In a typical FET implementation the shunt capacitors are partly provided by the FET and transmission line serve as the inductors. Thus, for a given impedance of the line, the gate source (or drain source) capacitance becomes a limiting factor to the bandwidth for the distributed amplifier.

2.3 CMOS Distributed Amplifier

A schematic of the convention CMOS distributed amplifier is shown in Figure 2.3. The common source based DA has a cascade of N identical NMOSs with their gates connected to a transmission line with characteristic impedance of Z_g, and their drains connected to a transmission line with characteristic impedance of Z_d.

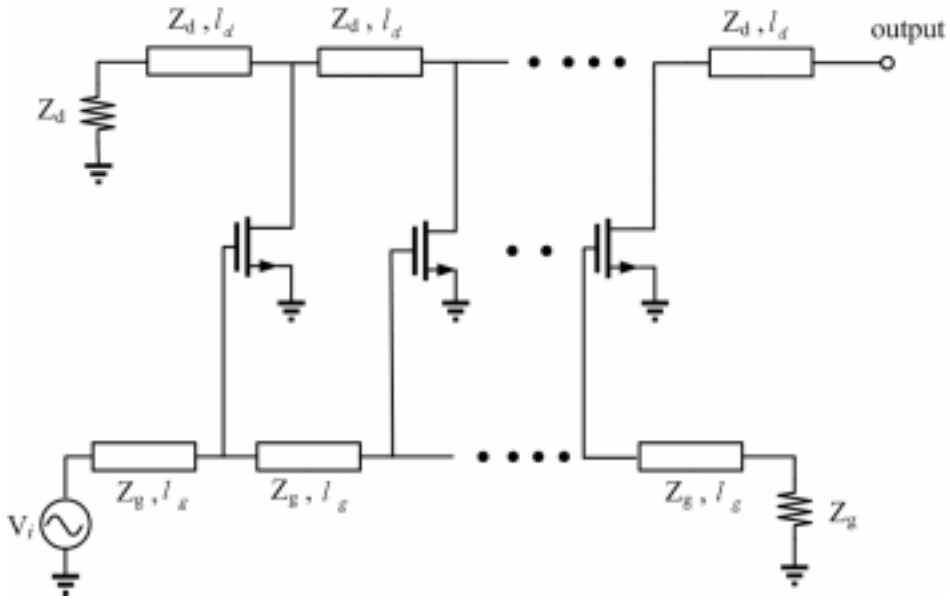


Figure 2.3 N-stage distributed amplifier

As the signal travels down the gate line, each transistor is excited by the traveling voltage wave and transfers the current to the drain line through its transconductance. If the phase velocities on the gate and drain lines are identical, then the signals on the drain line add in the forward direction as they arrive at the output. There is also a backward traveling wave component on the drain line, but the individual contributions to this wave will not be in phase; the residual will be absorbed in the termination Z_d. Consider a simplified equivalent circuit of FET is shown in Figure 2.4[16]. R_i is the effective input resistance between the gate and source terminals and C_{gs} is the gate-to-channel capacitance. R_{ds}, and C_{ds}, are the drain to-source resistance and capacitance, respectively. C_{gd} is the gate-to-drain capacitance and gm is the transconductance. In our analysis, the device will be considered unilateral and C_{gd} will be neglected.

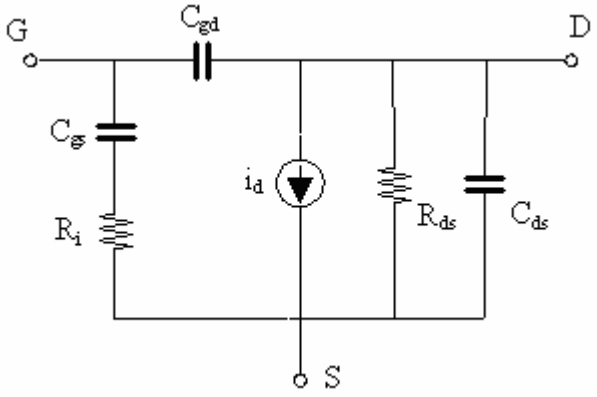


Figure 2.4 Simplified equivalent circuit of a FET

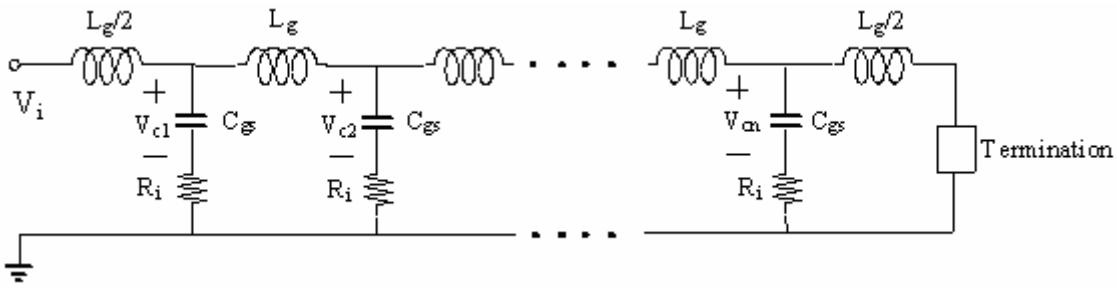


Figure 2.5 Gate transmission line

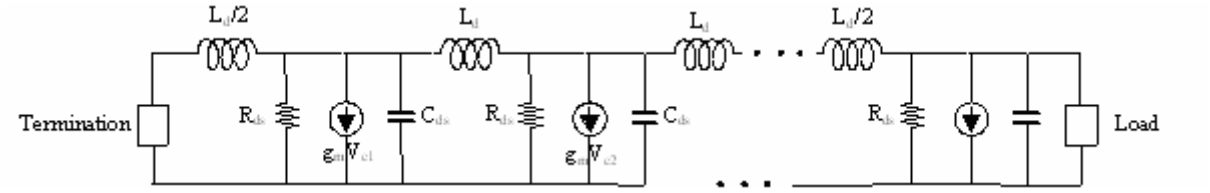


Figure 2.6 Drain transmission line

The equivalent gate and drain transmission lines are shown in Figure. 2.5 and 2.6 . The lines are assumed to be terminated in their image impedances at both ends. The current delivered to the load is given by

$$I_o = \frac{1}{2} g_m e^{-\theta_d/2} \left[\sum_{k=1}^{n} V_{ck} e^{-(n-k)\theta_d} \right] \tag{2.8}$$

where V_{ck} is the voltage across C_{gs} of the k-th transistor and $\theta_d = A_d + j\Phi_d$ is the propagation function on the drain line. A_d and Φ_d are the attenuation and phase shift per section on the drain line. n is the number of transistors in the amplifier. V_{ck} can be expressed in terms of the voltage at the gate terminal of the k-th FET as[17]

$$V_{ck} = \frac{V_i e^{-(2k-1)\theta_g/2 - j\tan^{-1}(\omega/\omega_g)}}{[1+(\frac{\omega}{\omega_g})^2]^{\frac{1}{2}}[1-(\frac{\omega}{\omega_c})^2]} \tag{2.9}$$

where V_i is the voltage at the input of the amplifier and $\theta_g = A_g + j\Phi_g$ is the propagation function on the gate line. A_g and Φ_g are the attenuation and phase shift per section on the gate line, $\omega_g = 1/R_i C_{gs}$ is the gate-circuit radian cutoff frequency, and ω_c is the radian cutoff frequency of the lines. By requiring gate and drain lines have the same cutoff frequency, the phase velocities are constrained to be equal. Therefore, we have Φ_g ; $\Phi_d = \Phi$.

From equation (2.8) and (2.9), I_o can be expressed as

$$I_o = \frac{g_m V_i \sinh[\frac{n}{2}(A_d - A_g)] e^{-n(A_d+A_g)/2} e^{jn\Phi - j\tan^{-1}(\omega/\omega_g)}}{2[1+(\frac{\omega}{\omega_g})^2]^{\frac{1}{2}}[1-(\frac{\omega}{\omega_c})^2]\sinh[\frac{1}{2}(A_d - A_g)]} \quad (2.10)$$

The power delivered to the load and input power to the amplifier are given, respectively, by

$$P_o = \frac{1}{2}|I_o|^2 \,\mathrm{Re}[Z_{ID}]\,;\ \frac{1}{2}|I_o|^2 \sqrt{L_d/C_d[1-(\omega/\omega_c)^2]} \quad (2.11)$$

and

$$P_i = \frac{|V_i|^2}{2|Z_G|^2}\mathrm{Re}[Z_{IG}]\,;\ \frac{1}{2}|V_i|^2 \Big/ \sqrt{L_g/C_g[1-(\omega/\omega_c)^2]} \quad (2.12)$$

where Z_{ID} and Z_{IG} are the image impedances of the drain and gate lines. Therefore, the power gain of the amplifier is

$$G = \frac{g_m{}^2 Z_g Z_d \sinh^2[\frac{n}{2}(A_d - A_g)] e^{-n(A_d+A_g)}}{4[1+(\frac{\omega}{\omega_g})^2][1-(\frac{\omega}{\omega_c})^2]\sinh^2[\frac{1}{2}(A_d - A_g)]} \quad (2.13)$$

where $Z_g = \sqrt{L_g/C_g}$ and $Z_d = \sqrt{L_d/C_d}$ are the characteristic impedance of the gate and drain lines, respectively. From equation (2.13), the magnitude of the voltage gain of a single amplifier stage can be shown to be

$$A = \frac{g_m[Z_g Z_d]^{1/2} \sinh[\frac{n}{2}(A_d - A_g)] e^{-n(A_d+A_g)/2}}{2[1+(\frac{\omega}{\omega_g})^2]^{1/2}[1-(\frac{\omega}{\omega_c})^2]^{1/2}\sinh[\frac{1}{2}(A_d - A_g)]} \quad (2.14)$$

The design equation for attenuation on gate and drain line is shown in [17]

$$A_g = \frac{(\omega_c/\omega_g)X_k{}^2}{\sqrt{1-[1-(\omega_c/\omega_g)^2]X_k{}^2}} \quad (2.15)$$

$$A_d = \frac{\omega_d/\omega_c}{\sqrt{1-X_k{}^2}} \quad (2.16)$$

where $X_k = \omega/\omega_c$ is the normalized frequency

$$\omega_g = 1/R_i C_{gs} \quad , \quad \omega_d = 1/R_{ds} C_{ds} \tag{2.17}$$

and

$$\omega_c = \frac{2}{\sqrt{L_g C_{gs}}} = \frac{2}{\sqrt{L_d C_{ds}}} \tag{2.18}$$

It is evident from the equation that the gate line attenuation is more sensitive to frequency than drain line attenuation. Therefore, the power gain of the amplifier can be expected to be predominantly controlled by the attenuation on the gate line and the dc gain by the attenuation on the drain line.

2.3.1 Broadband Distributed Amplifier Topology

In the design of pre-amp, there are several common goals including maximizing the output power of the pre-amp and providing the sufficient power gain. Recently several CMOS distributed amplifiers had been reported for broadband communication applications. In this section, we discuss some distributed amplifier architectures, and introduce the most popular DA architectures.

The first popular architecture of distributed amplifier is cascode distributed amplifier as show in Figure 2.7[12]. The cascode configuration, known for its high maximum available gain, wide bandwidth, improved input-output isolation, and variable gain control capability. The effect of Miller multiplication can be reduced through the use of cascode stages. However, the capacitance associated with the cascode junction cannot be absorbed by a transmission line, thus limiting the bandwidth. Conventional cascode FETs suffer from a large feedback capacitance, the drain-source capacitance of the common-gate transistor. This makes it tend to be unstable and thus more difficult to use in an amplifier circuit compared to common-source

architecture.

According to the system power budget, the total power consumption of RF transmitter front-end must limit to 25mW. The power gain of the pre-amplifier must provide sufficient gain to meet the specification. However the cascode DA architecture has maximum available gain but consumes large power which does not meet the UWB system power budget. We propose the current reuse distributed amplifier to meet the system power budget and provide sufficient power gain.

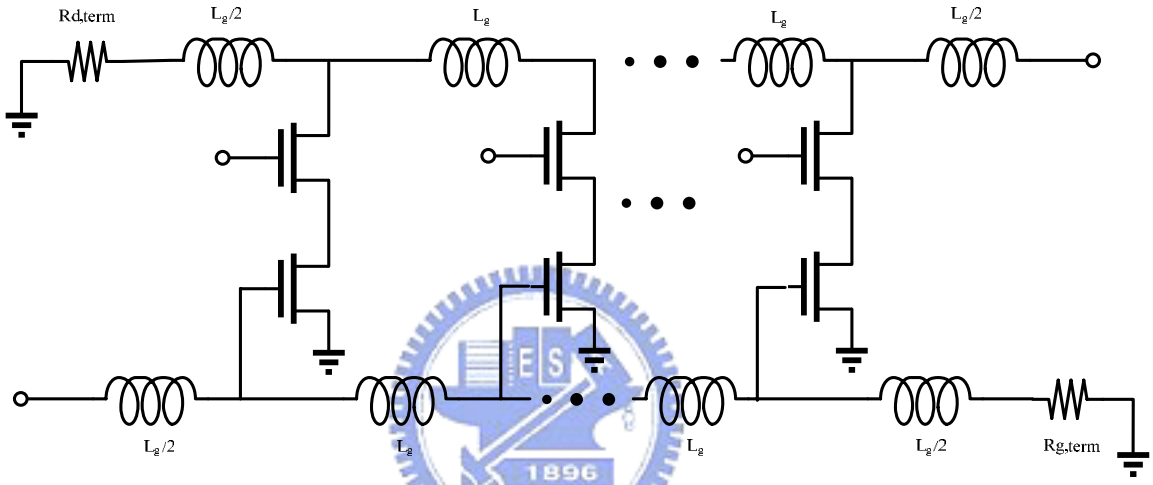


Figure 2.7 Cascode distributed amplifier

A cascade DA is illustrated in Figure 2.8. In this topology, AC coupling capacitor is used for connecting these two common source distributed amplifier. It cascades two or more common source distributed amplifier in order to get high available gain, and better input-output isolation than common source topology. But the drain bias voltage of the preceding cascaded stage must be high enough to provide the gate – source voltage required for next cascaded stage, further limiting the voltage drop across the inter-stage impedance. The cascaded topology doesn't have good linearity to provide enough output power and requires plenty of inductors. If all the load resistances of each gain stage are the same, the equation of the gain of the cascaded common source distributed amplifier can be written as:

$$A_V = \left(\frac{n}{2} g_m R_o \right)^N \tag{2.19}$$

where

N is number of stage cascaded.

n is number of stage.

g_m is gain stage transconductance.

R_o is output resistance of each stage.

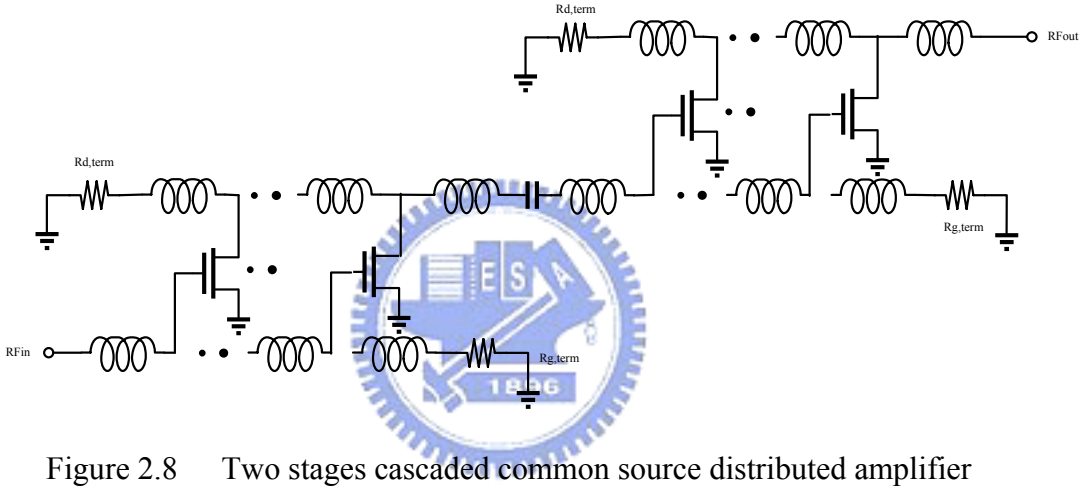


Figure 2.8 Two stages cascaded common source distributed amplifier

The third topology of the distributed amplifier cascades two stage cascode distributed amplifier. The CTDA circuit topology is illustrated in Figure.2.9 [18]. It could be regarded as two conventional two-stage cascode distributed amplifier in cascade. DC set up can be accomplished in the same way as that of conventional DAs. The cascode gain cell can reduce the effect of the miller multiplication to extend the bandwidth. It has high maximum available gain, better input-output isolation, and high output impedance. However CTDA using that cascode topology usually has high power dissipation and needs many inductors to form artificial transmission line.

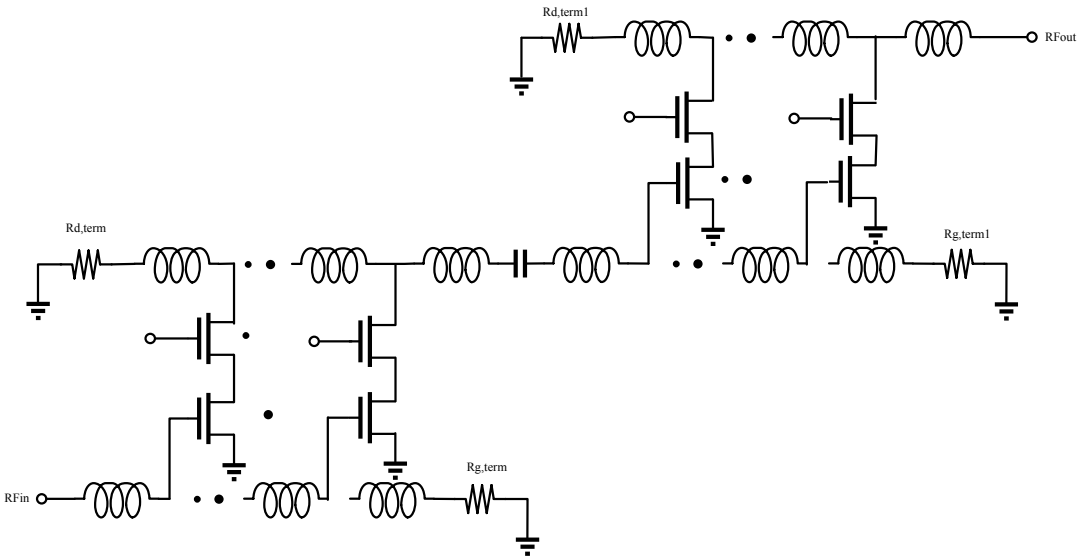


Figure 2.9 Cascaded two-stage cascode distributed amplifier

The gain of CTDA can be written as

$$A_V = \left(\frac{1}{2} \cdot 2 \cdot g_m \cdot R_o \right)^N \tag{2.20}$$

where

N is number of two-stage cascode distributed amplifier cascaded.

The forth topology is cascaded single stage distributed amplifier as shown in Figure 2.10 [19]. The structure of the cascaded single-stage distributed is essentially a cascade connection of single-stage distributed amplifiers with omission of idle gate and drain termination for the intermediate stages. The gain of the cascaded single-stage distributed amplifier (CSDA) increases exponentially with *2N*. This makes the CSDA more attractive for the CMOS process where the transconductance of the device, g_m, is inherently low. It has all the inductors accompanied by series resistors, the CSDA does not require low-loss integrated inductors. This property is highly desirable as the quality factor (Q) of the inductors is typically poor in the CMOS process owing to relatively high substrate conductivity in silicon. In the DA structure, parasitic feed-forward capacitances in active devices can upset phase matching between drain and gate artificial transmission lines, causing passband gain ripple in the

frequency response of the amplifier. For the CMOS DA, the problem is more aggravated as the capacitance C_{gd} is relatively large due to additional overlap capacitance in the self-aligned structure of MOS devices. By contrast, the passband response of the CSDA exhibits practically no sensitivity to C_{gd}, yielding superior passband flatness in the CMOS CSDA. Nevertheless it does not provide sufficient output power and consume plenty of power consumption, in addition it uses plenty inductors and is unsuitable for UWB pre-amplifier design. Nevertheless, if the gain of each stage is not large, the amplifier gain can not increase very fast. In addition, extra component such as RF choke may be needed to set up bias condition. The available power gain of cascaded single-stage distributed amplifier is given by

$$G_{av} = g_m^{\,2N} R_I^{\,2(N-1)} R_o^{\,2} / 4 \tag{2.21}$$

where

R_I is the inter-stage impedance.

g_m is the transconductance of each of $M1-MN$.

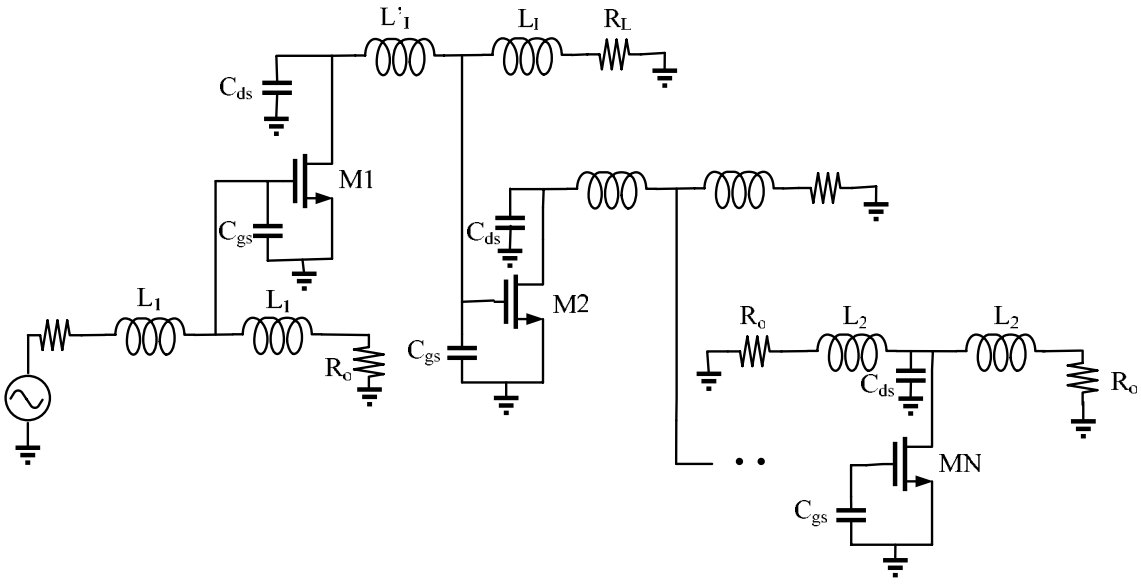


Figure 2.10 Cascaded single-stage distributed amplifier

Assuming all the load resistances of each gain stage are the same, therefore, the gain

efficiency of cascaded single stage DA will depend on $g_m R_o$. If the gain of each stage $g_m R_o$ is large, the gain efficiency will increase. In addition, extra components such as RF choke may be needed to setup dc operating voltage. (However, the area is increased)

2.4 Mixer Topology

Mixer topology can be roughly separated into two parts, active mixer and passive mixer. A typical active mixer configuration is shown in Figure 2.11 .The impressive advantage of active mixer is it provides some gain and good isolation from V_{LO} to V_{BB}. However, the active mixer suffers from several drawbacks. It exhibits worse linearity and power consumption. This is a significant disadvantage for the UWB system considered here because the UWB system it requires low power consumption and sufficient linearity.

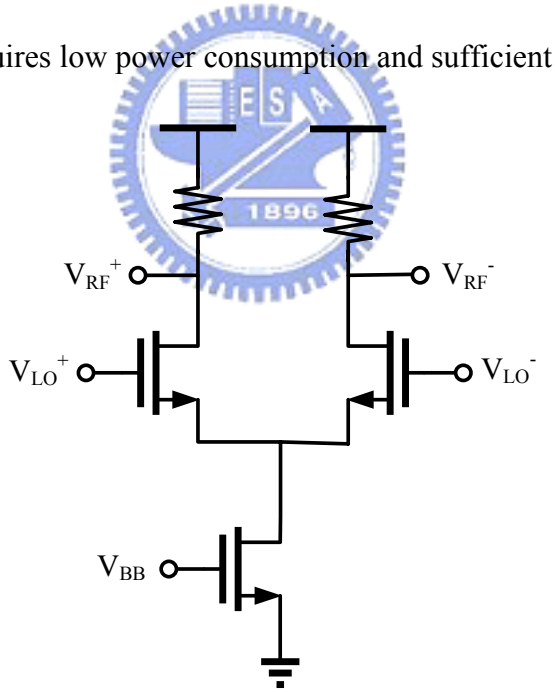


Figure 2.11 single balance mixer

As shown in Figure 2.12 is passive mixer. The modulation is performed by biasing a CMOS transistor in triode region. The baseband voltage signal is applied at the drain/source of the mixer transistor and the local oscillator voltage at the gates resulting in a modulated voltage.

Therefore, the passive mixer has the benefit of no DC power consumption, easier implementation and high linearity.

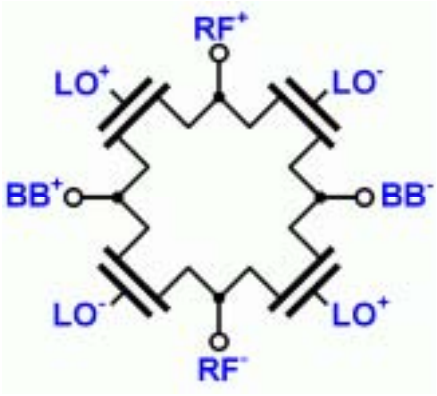


Figure 2.12 Passive mixer

Chapter 3

Low Power Current Reuse DA Design

In this chapter, a current reuse distributed amplifier is proposed for low-power ultra-wideband wireless applications. Section 3.1 addresses design concepts of wideband approaches. The proposed distributed amplifier consists of a PMOS and a NMOS in parallel to reuse the bias current and is described in section 3.2. The further analysis of current reuse DA will also be discussed. In Section 3.3, the DC feedback current reuse distributed amplifier is proposed to maintain the performance. The proposed DA is illustrated in Section 3.4. Section 3.5, design considerations will be discussed. The passive mixer will be discussed in Section 3.6.

3.1 Design Concept

The goal of this work is to cover the 3-10.6GHz frequency range for the band group #1~3 of MB-OFDM proposal. The output power should be larger than 0dBm to meet the transmitter of ultra-wide bandwidth specification.

3.2 Analysis of Current Reuse DA

The principal defect on the traditional distributed amplifier is that power consumption is

generally huge due to several stages cascaded to supply sufficient gain level. However, in UWB system considerations, the power consumption is the neck of a bottle. We propose a current reuse distributed amplifier to reduce power consumption without degrading any gain-bandwidth product. As shown in Fig. 3.1, a PMOS and a NMOS with inverter configuration are together the base transconductance amplifier stage in proposed DA. We define the NMOS dimension of common source topology is $\frac{1}{2}(\frac{W_o}{L_o})$, the NMOS and the PMOS dimension of current reuse DA is $\frac{W_n}{L_o}=\frac{W_p}{L_o}$.

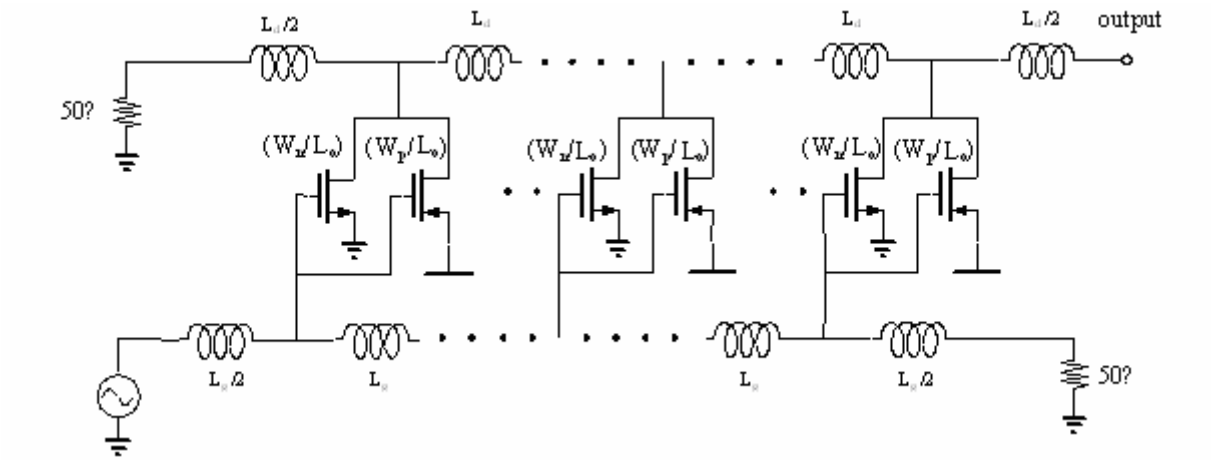


Figure 3.1 The schematic of the proposed DA

The goal is to achieve the gain-bandwidth product with less current. In order to get the same bandwidth as that of a common source based DA, the total device width of PMOS and NMOS of proposed DA is selected to equal the device width of the common source based DA. Accordingly, the device dimensions of NMOS and PMOS in proposed topology are therefore

$$\frac{W_n}{L_o}=\frac{W_p}{L_o}=\frac{1}{2}(\frac{W_o}{L_o}) \tag{3.3}$$

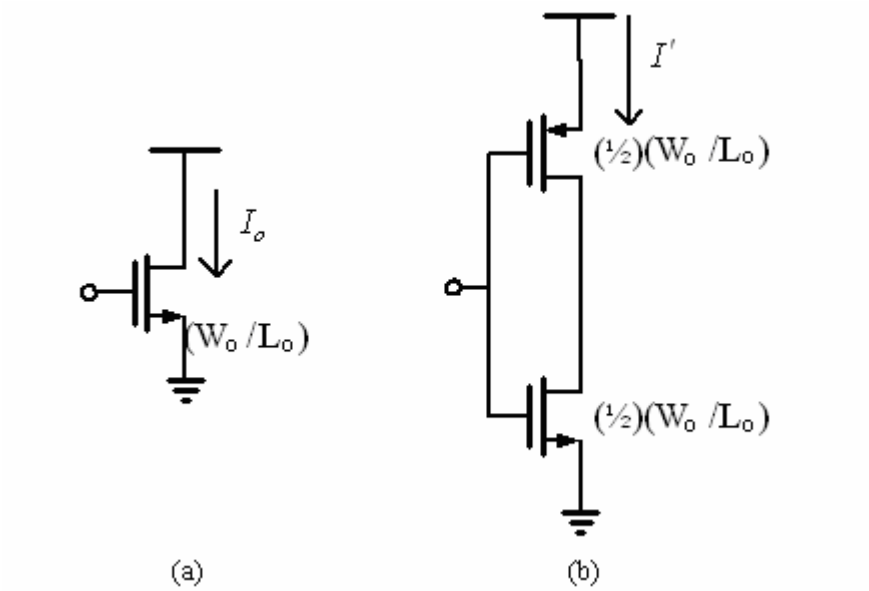


Figure 3.2 Comparison of current consumption between the conventional DA (a) and propose DA(b)

As a consequence, the bandwidth of presented current reuse DA is nearly the same as that of the basic common source configured counterpart. As shown in Figure 3.2, the input capacitance of current reuse topology is equivalent to the input capacitance of common source topology.

The transconductance of each amplification stage of common source configuration is

$$g_{mo} = \sqrt{2\mu_n C_{ox} \frac{W_o}{L_o} I_o} \tag{3.4}$$

The transconductance of each amplification stage consisting of a PMOS with device dimension of $\frac{W_p}{L_o} = \frac{1}{2}(\frac{W_o}{L_o})$ and a NMOS with device dimension of $\frac{W_n}{L_o} = \frac{1}{2}(\frac{W_o}{L_o})$ in inverter configuration is

$$
\begin{aligned}
g_{mt} &= g_{mn} + g_{mp} \\
&= \sqrt{2\mu_n C_{ox} \frac{W_o}{2L_o} I'} + \sqrt{2\mu_p C_{ox} \frac{W_o}{2L_o} I'} \\
&= g_{mo}(1 + \sqrt{\frac{\mu_p}{\mu_n}}) \sqrt{\frac{I'}{2I_o}}
\end{aligned}
\tag{3.5}
$$

From equation (2.13) and (3.5), the gain of proposed current reuse DA is thus

$$
\begin{aligned}
Gain' &= K_o g_{mt}^2 \\
&= K_o \cdot \frac{1}{2} \cdot g_{mo}^2 (1 + \sqrt{\frac{\mu_p}{\mu_n}})^2 \frac{I'}{I_o} \\
&= Gain_o \cdot \frac{1}{2} \cdot (1 + \sqrt{\frac{\mu_p}{\mu_n}})^2 \frac{I'}{I_o}
\end{aligned}
\tag{3.6}
$$

In today CMOS technology, the electron mobility is about three times of the hole mobility.

Assumes $\mu_n \approx 3\mu_p$

$$
\begin{aligned}
Gain' &= Gain_o \cdot \frac{1}{2} \cdot (1 + \sqrt{\frac{\mu_p}{3\mu_p}})^2 \frac{I'}{I_o} \\
&= Gain_o \cdot 1.25 \cdot \frac{I'}{I_o}
\end{aligned}
\tag{3.7}
$$

We let the $Gain' = Gain_o$ and $BW' = BW_o$

That is, to achieve the same gain-bandwidth product, only 80% of the bias current is required.

3.2.1 Optimization

In order to get better performance of the current reuse distributed amplifier. We can further

reduce the power consumption by adjusting the ratio of the NMOS and PMOS dimension and extend the previous analysis of gain and bandwidth. To maintain the same bandwidth, we define the device size of common source and current reuse stage as shown in Figure 3.3.

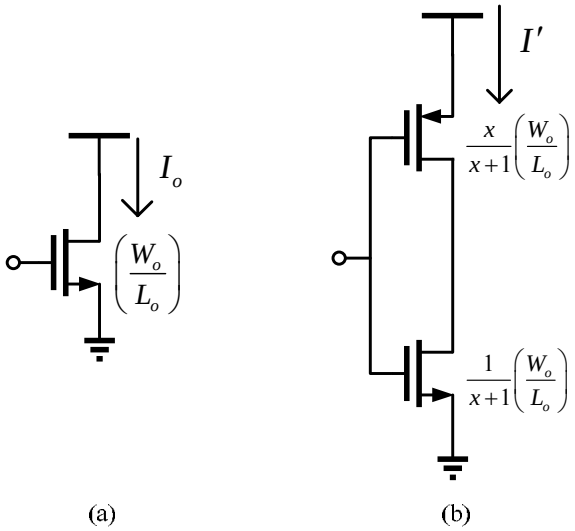


Figure 3.3 Further comparison of current consumption between the common source DA(a) and current reuse DA(b)

$$\frac{(W_n/L_o)}{(W_p/L_o)} = x \tag{3.8}$$

$$\Rightarrow \left(\frac{W_n}{L_o}\right) = \frac{x}{x+1}\left(\frac{W_o}{L_o}\right), \quad \left(\frac{W_p}{L_o}\right) = \frac{1}{x+1}\left(\frac{W_o}{L_o}\right) \tag{3.9}$$

From equation (2.13), the power gain is proportional to the transconductance square. The power gain of proposed current reuse DA is

$$\begin{aligned} Gain' &= K_o g_{m'}^2 = K_o (g_{mn} + g_{mp})^2 \\ &= K_o \left(\sqrt{2\mu_n C_{ox}(\frac{W}{L})_n I'} + \sqrt{2\mu_p C_{ox}(\frac{W}{L})_p I'}\right)^2 \\ &= K_o \left(g_{mo}\sqrt{\frac{I'}{I_o}(\frac{x}{x+1})} + g_{mo}\sqrt{\frac{I'}{I_o}(\frac{1}{x+1})\frac{\mu_p}{\mu_n}}\right)^2 \\ &= Gain_o \left(\sqrt{\frac{I'}{I_o}(\frac{x}{x+1})} + \sqrt{\frac{I'}{I_o}(\frac{1}{x+1})\frac{\mu_p}{\mu_n}}\right)^2 \end{aligned} \tag{3.10}$$

From previous analysis, we can keep the same performance as common source DA, $Gain' = Gain_o$. The electron mobility is about three times of the hole mobility. The current consumption is

$$I' = I_o \times (x+1) \frac{1}{(\sqrt{x} + \sqrt{\frac{\mu_p}{\mu_n}})^2} \tag{3.11}$$

Equation (3.11) shows the relation between current consumption and the ratio of device dimension. As shown in Figure 3.4, there is an optimum value of the ratio of device dimension for the lowest power consumption. We choose the ratio of device dimension is 3. Therefore, only 75% of the bias current is required.

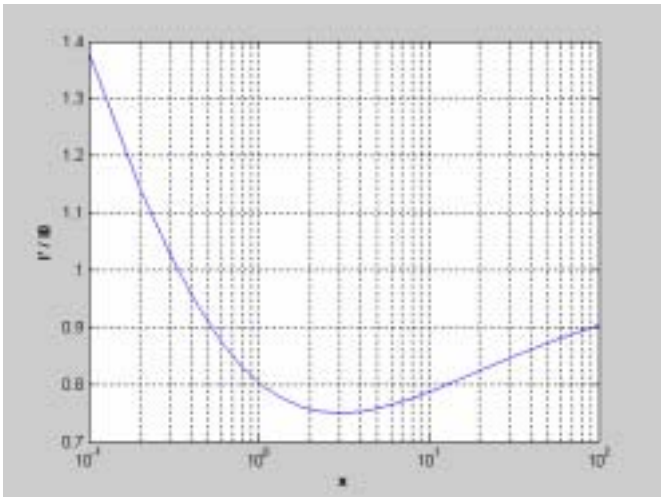


Figure 3.4 Current consumption versus the ratio of device dimension

Next, the output resistance will influence the performance of current reuse DA. Figure 3.5 shows the transmission circuit for the drain line of the DA. For the drain line, the series impedance and shunt admittance per unit length are

$$Z = j\omega L_d,\ Y = \frac{1}{R_{ds} l_d} + j\omega (C_d + C_{ds}/l_d)$$

The characteristic impedance of the drain line can be written as

$$Z_d = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_d}{C_d + C_{ds}/l_d}}$$

and the propagation constant can be simplified using the small loss approximation as

$$\gamma_d = \alpha_d + j\beta_d = \sqrt{ZY} = \sqrt{j\omega L_d[\frac{1}{R_{ds} l_d} + j\omega(C_d + C_{ds}/l_d)]}$$

$$\cong \frac{Z_d}{2R_{ds} l_d} + j\omega\sqrt{L_d(C_d + C_{ds}/l_d)}$$

According to the transmission line theory, the power gain of DA is

$$G = \left| \frac{e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g} - e^{-\gamma_d l_d}} \right|^2 \frac{Z_g \cdot Z_d}{4} g_m^2$$

So, the output resistance R_{ds} will affect the α_d. The output resistance of dc feedback current reuse distributed amplifier is R_{ds} of NMOS shunt the R_{ds} of PMOS. However, the α_d of dc feedback current reuse DA will increase. The power gain of dc feedback current reuse DA will decrease by increased α_d.

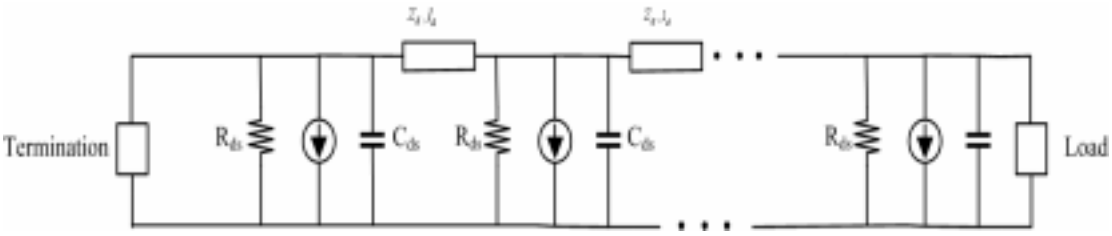


Figure 3.5 transmission circuit for the drain lie of the DA

3.2.2 Output Power Considerations

The comparison between common source DA and current reuse DA is discussed. If we choice the ratio of device dimension of current reuse DA as 3, the power consumption only needs 75%. However, the transmitter of ultra-wideband specification considers not only power

consumption but also the magnitude of output power. As shown in Figure 3.6 is output power versus the ratio of the dimension of current reuse DA.

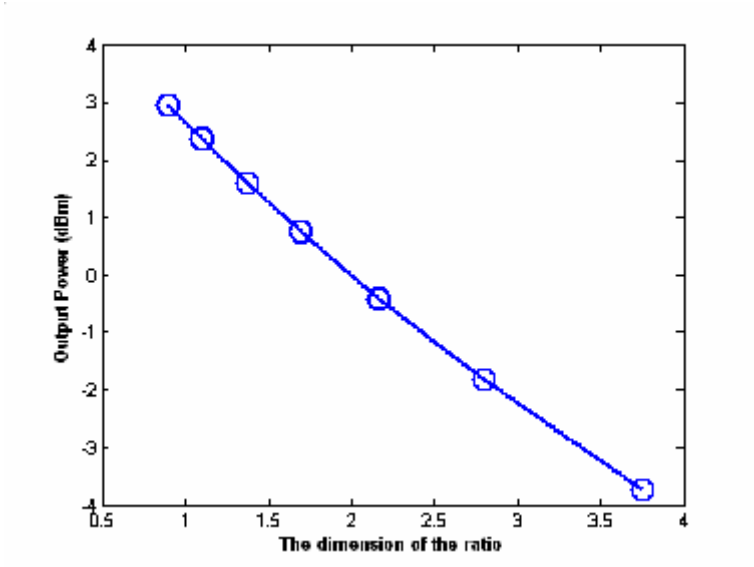


Figure 3.6 Output power versus the ratio of the dimension of current reuse DA

In ultra-wide bandwidth transmitter specification, the output power should be larger than 0dBm. The ratio of device dimension must be lower than 1.7 for output power. After the optimization, we choice the finger of NMOS is 22, the finger of PMOS is 16 to meet the specification. And the ratio of device dimension of current reuse DA is 1.375.

3.2.3 Verification

Previous analysis is deriving with the mathematics formula, and then we will verify our inference with simulation. The target simulation specifications are $|S21|$; $8.1dB$, $|S11| < -12dB$, $|S22| < -12dB$ over a bandwidth of 10GHz. The results are presented in the following format. Plots for $|S21|$, $|S11|$ *and* $|S22|$ are obtained from ADS and are used to compare current reuse DA and common source DA. Power is calculated from the current consumption ($P_{dc} = I_{dc} \times V_{dd}$). Figure 3.7 and 3.8 show the simulation results of S21, S11 and

S22 plots for compare with common source DA and current reuse DA. From the simulation results, the bandwidth and power gain are nearly the same. The input return loss and output return loss all are lower than -12dB. Deeply concerned to the power consumption of each distributed amplifier is $12.3mA\times V_{dd}$ for common source DA and $10.23mA\times V_{dd}$ for current reuse DA. The ratio of power consumption is proportional to the bias current. Therefore, the ratio of power consumption is $\frac{I'}{I_o}=83\%$. The ratio of power consumption of equation (3.11) is 78% similarly the simulation results. This analysis will be verified by the simulation. This error is made of channel length modulation and the difference of V_{DS} voltage.

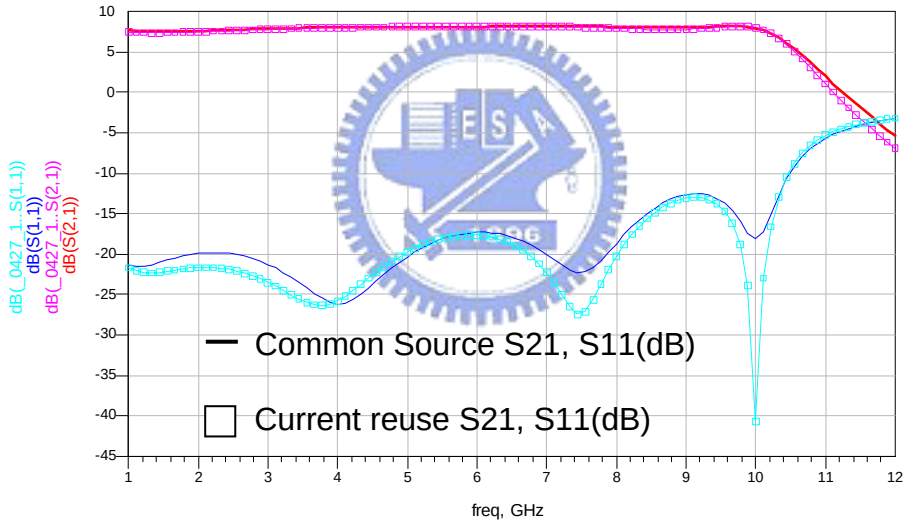


Figure 3.7 Comparison with Convention DA and Current reuse DA (S21,S11)

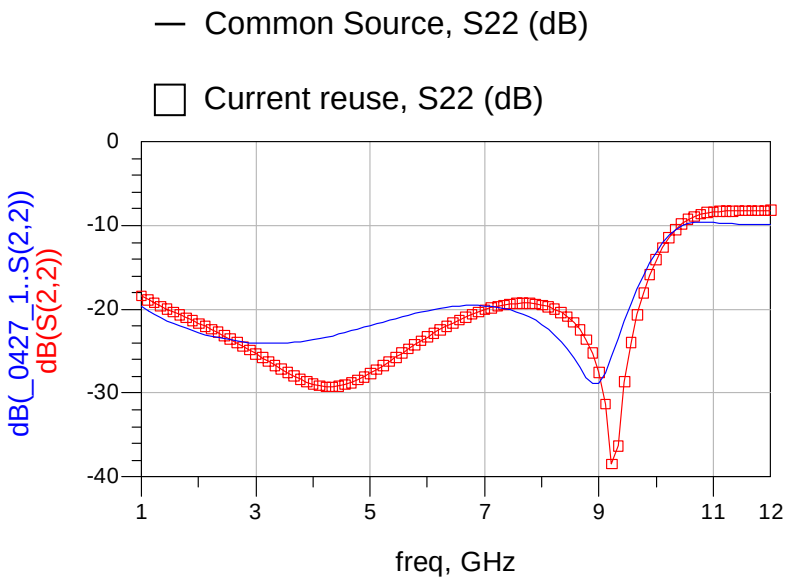


Figure 3.8 Comparison with Convention DA and Current reuse DA (S22)

3.3 DC Feedback Current Reuse DA (Stability)

The current reuse DA has better performance than common source DA. Nevertheless, the inverter configuration which the output dc bias will suffer from large variation at the output dc bias if there is a slight variation in the input dc bias. As shown in Figure 3.9, the voltage transfer function of inverter configuration that there is a small input swing to bias the inverter topology in the correct bias region (in this design, saturation region). That is, all devices will be ensured to work in the correct bias region and amplify the small signal.

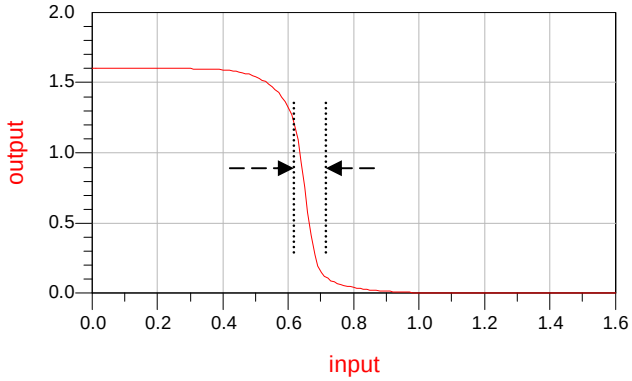


Figure 3.9 Voltage transfer function of inverter configuration

The simulation results to verify the effect of input dc bias variation. Figure 3.10 shows the power gain of current DA with input dc bias variation. It is observed that the input dc bias with slightly change of ±0.02V causes the power gain of current reuse DA to degrade 0.3dB. However, the input dc bias varying ±0.03V leads the power gain of current reuse DA to lower 1.3dB. It is a huge effect to current reuse DA and should be overcome. Therefore, a dc feedback is required in the current reuse distributed amplifier to conquer this drawback.

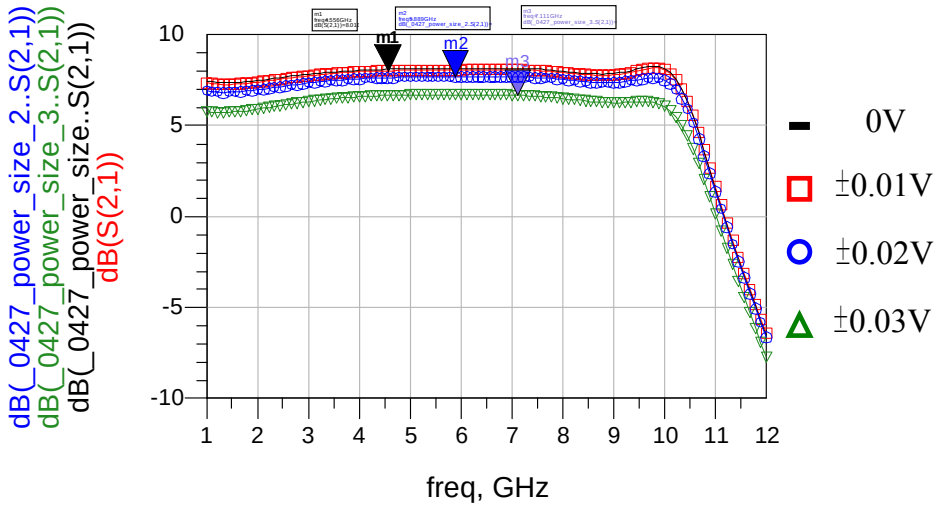


Figure 3.10 Power gain of current reuse DA with input dc bias variation

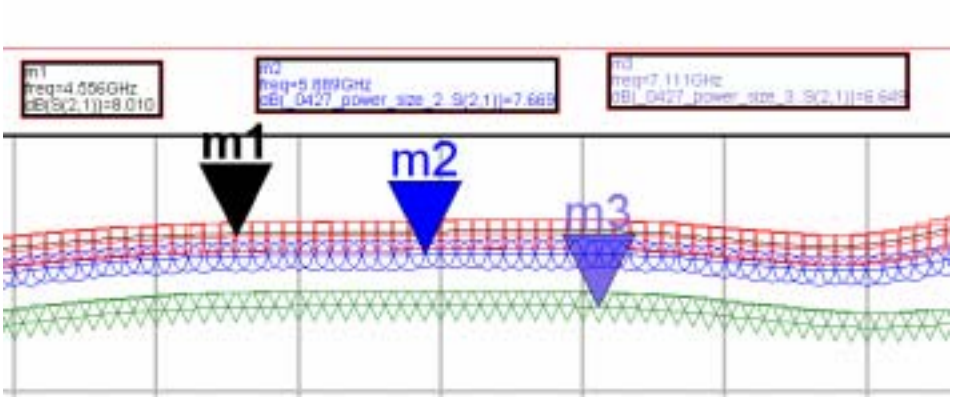


Figure 3.11 Enlarge

Figure 3.12 shows the schematic of dc feedback current reuse distributed amplifier. The dc feedback current reuse DA adds a feedback resistor, connecting the gate transmission line and the drain transmission line. Consequently the DC Bias voltage of output node is equal to that of input node.

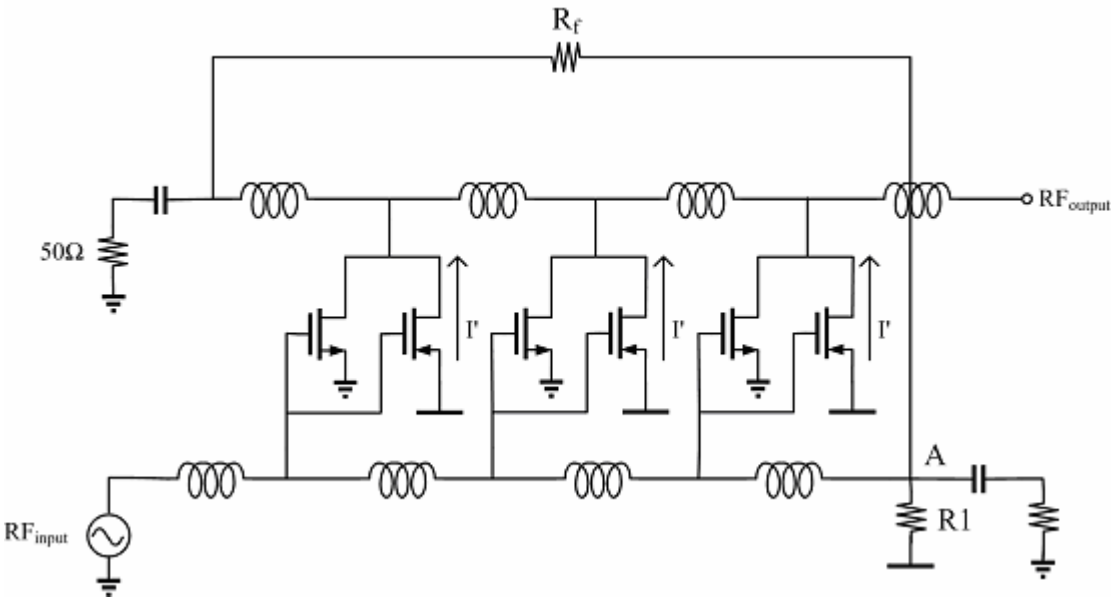


Figure 3.12 The schematic of dc feedback current reuse distributed amplifier

According to the voltage transfer function of inverter configuration, the output voltage decreases if the input voltage increases slightly. The dc current flows through the resistor R1,

the feedback resistor R_f and the NMOS transistors. The resistor R1 has a voltage drop. That is, the voltage of gate decreases if the input dc bias increases. It uses the dc feedback to fix the output DC voltage in order to keep every transistor in correct operation region. If the circuit does not contain the resistor R1, and the input dc bias direct connects with the node A. The output voltage will drop off when the input voltage increases slightly. Although the resistor R_f also has the voltage drop, the output voltage can not be fixed to a stable voltage. Therefore, every transistor can not operate in correct bias region.

Figure 3.13 shows the power gain of dc feedback current reuse DA with input dc bias variation. Figure 3.13 and Figure3.10 are simulated results with the same input dc bias variation. Hence, dc feedback current reuse DA is not affected by the dc bias variation.

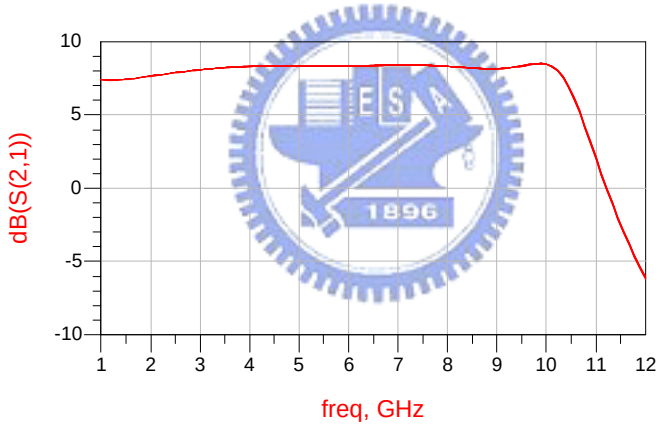


Figure 3.13 Power gain of DC feedback current DA with input dc bias variation

The value of dc feedback resistance will affect the S-parameter. If the value of resistance is not suitable, the amplifier may be unstable and can not work in desirable frequency range. In normal specification of amplifier, the S11 and S22 should be lower than -10dB cover the frequency band. Figure 3.14 demonstrates the simulation result under different resistance value (350Ω, 600Ω, 800Ω, 1000Ω). If the value of dc feedback resistance is too large, the current flow through the feedback resistance will make huge voltage drop in feedback

resistance. Thus, the auto-correction ability for the gate dc bias of the feed-back resistance will decrease. The performance of the dc feedback current reuse distributed amplifier is greatly affected by dc bias variation. Second, the noise figure increases as the feedback resistance increases. It is nearly the same to power gain under the condition of different resistance value.

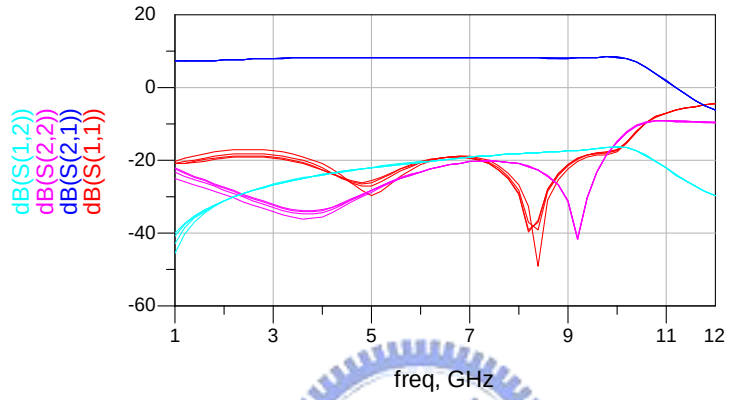


Figure 3.14 Different value of resistance

3.4 The Proposed Distributed Amplifier

In our previously proposed technique, each stage employs inverter type topology to amplifier the signal. Figure 3.15 shows the schematic of current reuse DA is constructed with a NMOS or PMOS transistor in each stage. The bias current flows from second stage PMOS to first stage NMOS transistor. The bias current flows from fourth stage PMOS to third stage NMOS transistor. In order to match the phase shifts in both the gate and drain line the size of each stage has to be equal.

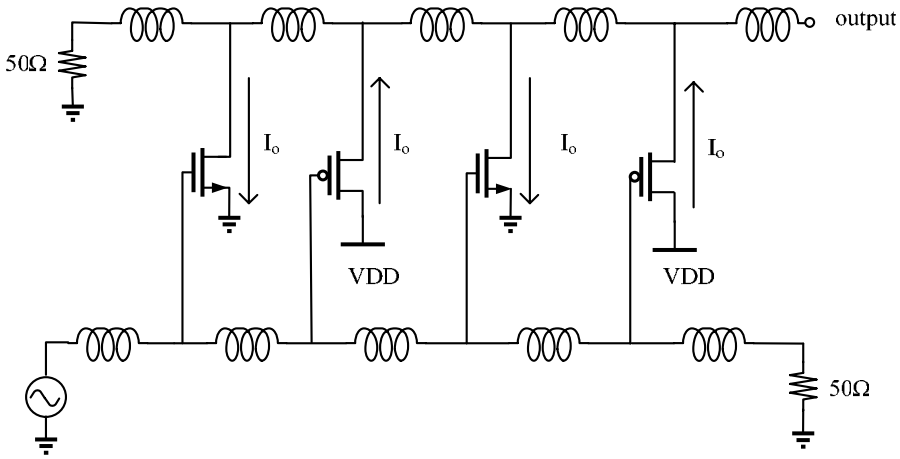


Figure 3.15 The current reuse DA is constructed with a NMOS or PMOS transistor in each stage

3.5 Design Considerations

From equation (2.13), the power gain of the DA increase with Z_g and Z_d . Using higher Z_g and Z_d help improve the gain without any increase in power consumption. Higher characteristic impedance of gate Z_g and drain Z_d can obtain higher power gain but the cutoff frequency will be lower. Therefore, the bandwidth will be limited. Traditionally, DA has been terminated with an impedance of 50Ω. In order to minimize the losses caused by the impedance mismatches that the characteristic impedance of the artificial transmission line is selected to be 50Ω. From equation (2.6), (2.18), Z_o can be expressed in terms of f_c and C as

$$Z_o = \frac{1}{\pi f_c C} \tag{3.12}$$

It is observed that for a given f_c, C and Z_o are inversely proportional to each other. Capacitances of the gate lines primarily from the gate- source capacitance of the MOSFET is

$$C \propto WLC_{ox} \tag{3.15}$$

where C_{ox} is the oxide capacitance. W and L are the width and length of the MOSFET. L is

fixed considering minimum length devices. C is determined by W. Further from equation (3.11) and output power of DA can be selected the size of the transistor. The transconductance and DC bias current of a long-channel MOSFET are given by

$$g_m = \sqrt{2k'\frac{W}{L}I_D} = \frac{I_D}{V_{ov}/2} \tag{3.16}$$

where $k' = \mu C_{ox}$ is called the process transconductance parameter.

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_{ox}V_{ov}^2 \tag{3.17}$$

where V_{ov} is called the gate drive of the device and μ is the channel mobility.

From equation (3.12), it can be simply observed that decreasing C increases both f_c and Z_o, but this comes from a lower width and less g_m. Second, for a given I_D, increasing W decreases V_{ov}.

Third, increasing W, increase C which in turn decreases f_c and Z_o. Next, the number of gain stage of distributed amplifier will be discussed. According to [16], the optimal number of gain stage *N* which maximum the gain at a operating frequency is given. Besides, the specification of UWB transmitter needs 0dB conversion gain and low power consumption. Figure 3.16 shows the power gain of different number stage. The power gain of four stages is almost about 9.2dB covering the bandwidth, but it will increase more chip area and consume more power. The power gain of two stages is average 5.5dB over the bandwidth and does not meet the specification. Thus, the optimization number of stage is 3.

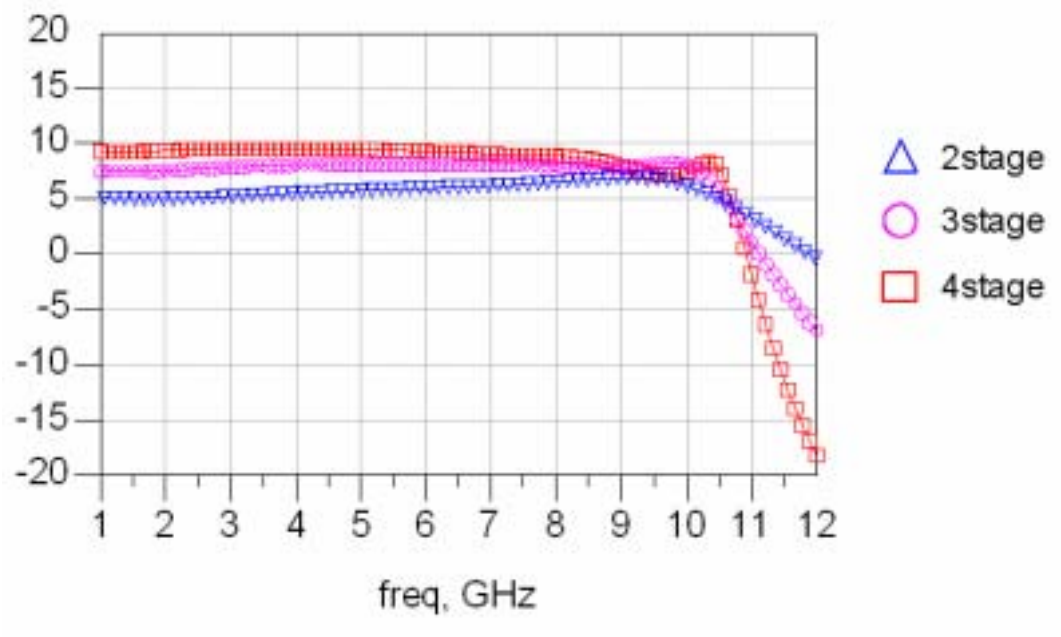


Figure 3.16 Power gain of different number of stage

3.6 Passive Mixer

Passive mixer is to be like traditionally active mixer which has the conversion gain. However, the active mixer consumes power and normally operates narrowband application. And traditionally active mixer is differentially output, it needs a differential-to-single (D/S) converter to transfer the differential signal to single output in order to amplify the small signal by dc feedback current reuse distributed amplifier. Furthermore, the differential-to-single circuit may consume power consumption and could not work in wideband application. The wideband passive mixer is designed for the purpose of low power, high linearity and wide bandwidth as shown in Figure 3.17.

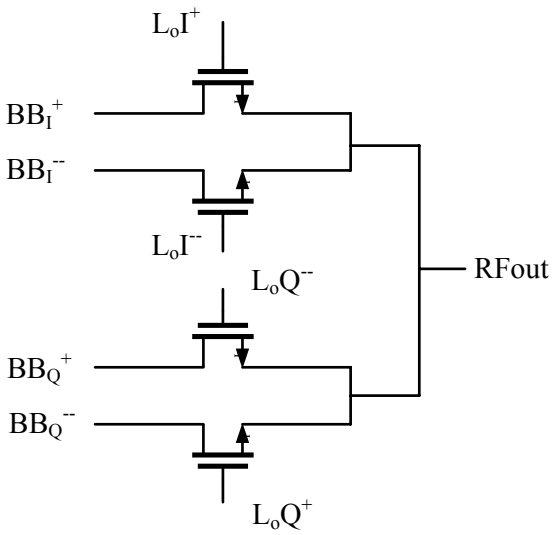


Figure 3.17 Passive mixer

Chapter 4

Transmitter in UWB System

The transmitter circuit is put in the UWB system for verification and will be discussed in this chapter. Section 4.1 introduces the MutiBand OFDM proposal and focuses on RF related information. Section 4.2 discusses RF/Baseband co-simulation. The simulation results for transmitter application in the UWB system is shown in section 4.3.

4.1 MB-OFDM Proposal

The FCC approved spectrum, 3.1-10.6 GHz, is divided into 14 bands where each band has bandwidth of 528 MHz. As summarized in Table 4.1, the relationship between center frequency and band number is given by the following equation. Band center frequency = $2904 + 528 \times n_b, n_b = 1...14$ (MHz). This definition provides a unique

numbering system for all channels that have a spacing of 528 MHz and lie within the band 3.1 – 10.6 GHz. Based on this, five band groups are defined, consisting of four groups of three bands each and one group of two bands. Band group 1 is used for Mode 1 devices (mandatory mode). The remaining band groups are reserved for future use.

Band Group	BAND_ID	Lower frequency	Center frequency	Upper frequency
1	1	3168 MHz	3432 MHz	3696 MHz
	2	3696 MHz	3960 MHz	4224 MHz
	3	4224 MHz	4488 MHz	4752 MHz
2	4	4752 MHz	5016 MHz	5280 MHz
	5	5280 MHz	5544 MHz	5808 MHz
	6	5808 MHz	6072 MHz	6336 MHz
3	7	6336 MHz	6600 MHz	6864 MHz
	8	6864 MHz	7128 MHz	7392 MHz
	9	7392 MHz	7656 MHz	7920 MHz
4	10	7920 MHz	8184 MHz	8448 MHz
	11	8448 MHz	8712 MHz	8976 MHz
	12	8976 MHz	9240 MHz	9504 MHz
5	13	9504 MHz	9768 MHz	10032 MHz
	14	10032 MHz	10296 MHz	10560 MHz

Table 4.1. OFDM PHY band allocation

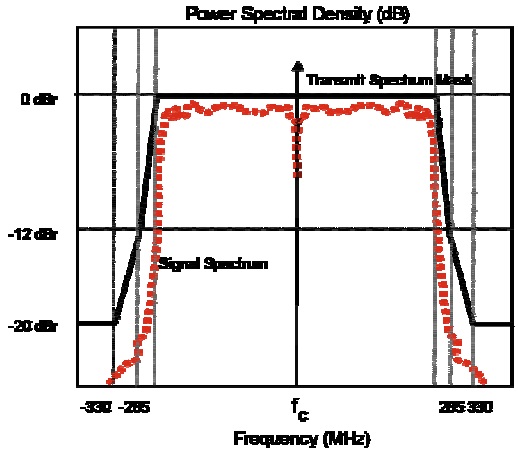


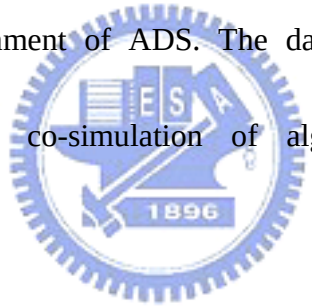
Figure 4.1. Transmitter power spectral density mask in MB OFDM proposal.

The transmitted spectrum shall have a 0 dBr (dB relative to the maximum spectral density of the signal) bandwidth not exceeding 260 MHz, –12 dBr at 285 MHz frequency offset, and –20 dBr at 330 MHz frequency offset and above. The transmitted spectral density of the transmitted signal mask shall fall within the spectral, as shown in Figure 4.1. Next the co-simulation results will verify the transmitter output spectrum satisfying the power spectral density mask

4.2 RF/Baseband Co-Simulation

Figure 4.2 shows the model of the RF/Baseband co-simulation. In the left of Figure 4.2 shows the baseband signal generated by matlab and ADS. One of the building

blocks is the RF transmitter behavior model which consists of RF front-end and analog modules as shown in Figure 4.3. Band selection filer, variable gain amplifier, mixer, and pre-amplifier in discrete modules are included. However, the band selection filter and variable gain amplifier are ideal modules. The mixer and pre-amplifier are real circuit level to replace the ideal module in order to verify the system simulation. The bottom of the Figure 4.2 is the UWB receiver module. The co-simulation of circuit-level RF with algorithm-level baseband can be applied to evaluate the effects on error vector magnitude (EVM). The co-verification platform is fulfilled in the DSP environment of ADS. The data flow simulator and circuit envelope simulator enables co-simulation of algorithm-level baseband with circuit-level RF front-end.



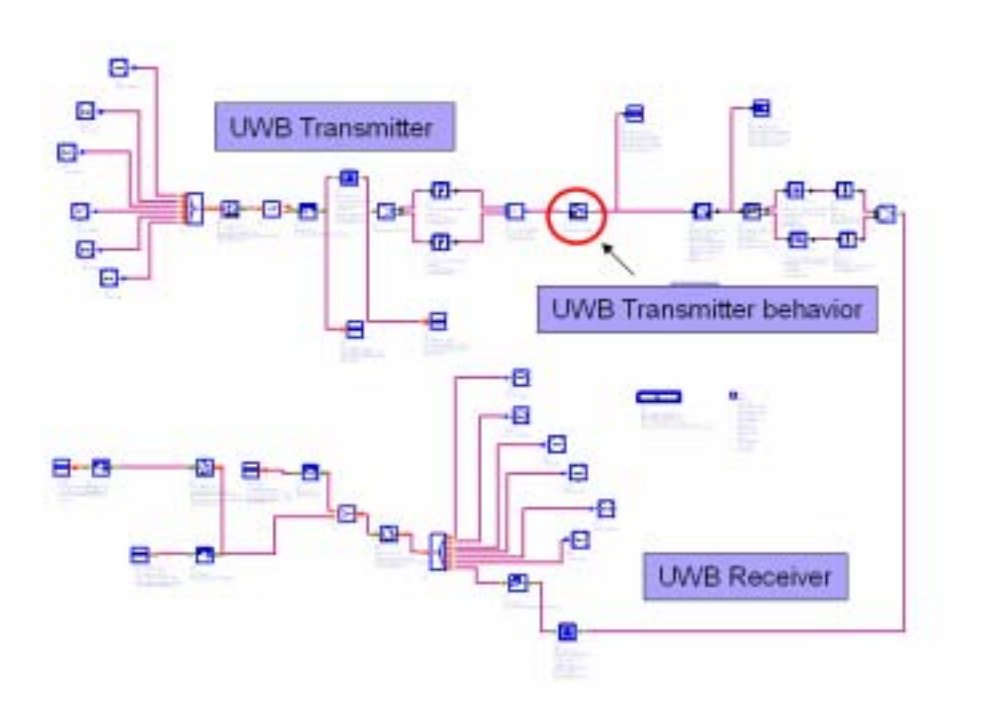


Figure 4.2. RF/Baseband co-simulation model.

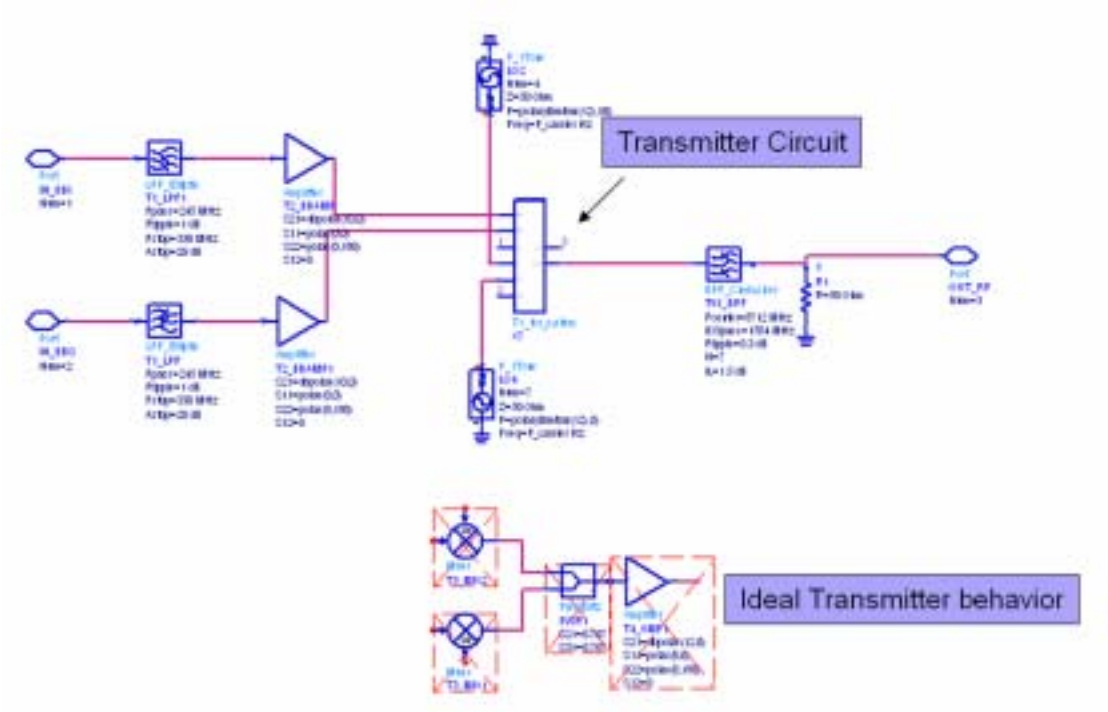


Figure 4.3. UWB Transmitter behavior model.

4.3 Simulation Results

Figure 4.4-4.7 shows the RF/Baseband co-simulation with the transmitter circuit is conducted for Band_ID 2, 5, 8, 11. It's covers the frequency range from 3GHz to 10Ghz. We select the center band of each band group to simulate in order to make sure covers every band groups. Figure 4.4 shows the simulation results of center frequency is 3960MHz. The power spectrum density at the transmitter output is plotted. The power spectrum density is conformed to transmitter power spectral density mask in MB OFDM proposal. After total output power adds the channel loss (-40dB), the total output power is -5.5dBm which is the average output power. The specification of average output power of UWB transmitter is -10dBm. The EVM results are close to those with behavior building block of transmitter.

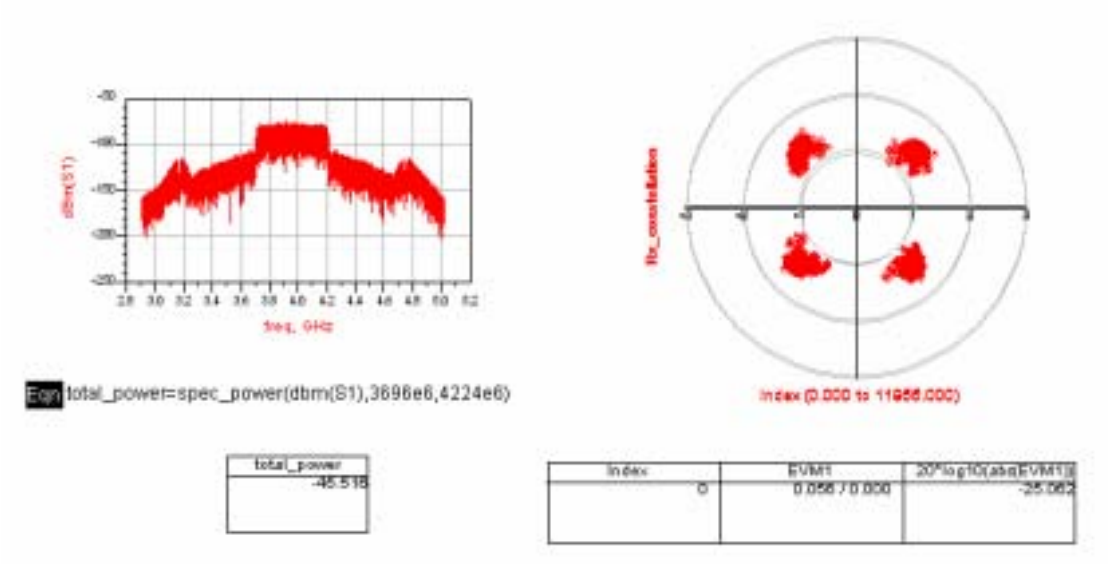


Figure 4.4. Co-simulation results – BAND_ID #2.

The co-simulation for BAND_ID #5 is illustrated in Figure 4.5. It performs better EVM value than BAND_ID #2. The pre-amplifier has large gain in 5GHz to compare with other frequency.

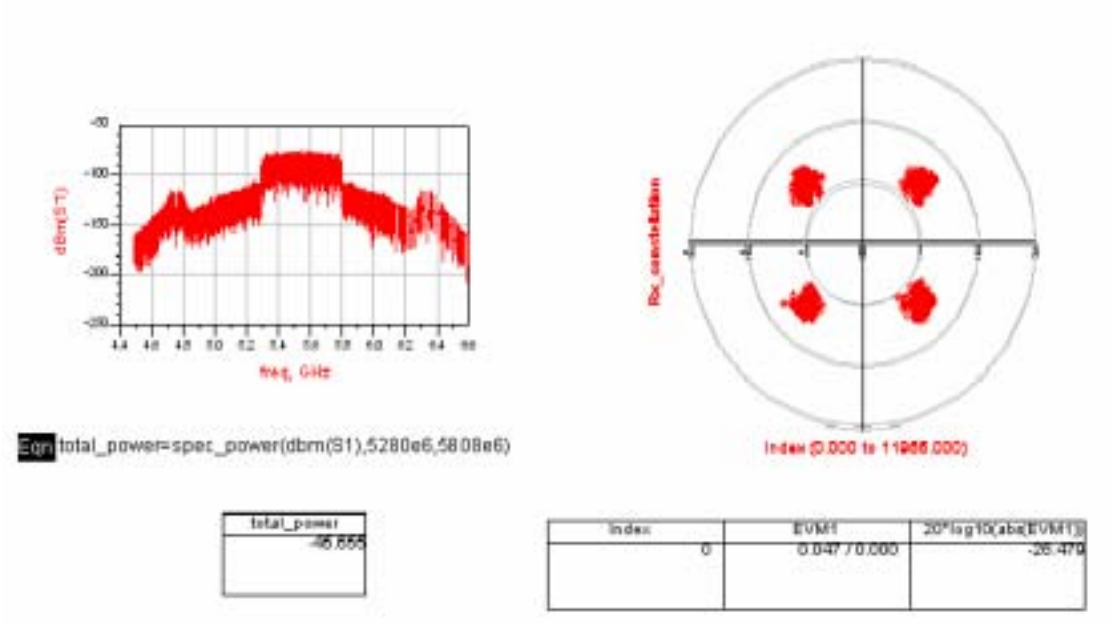


Figure 4.5. Co-simulation results – BAND ID #5.

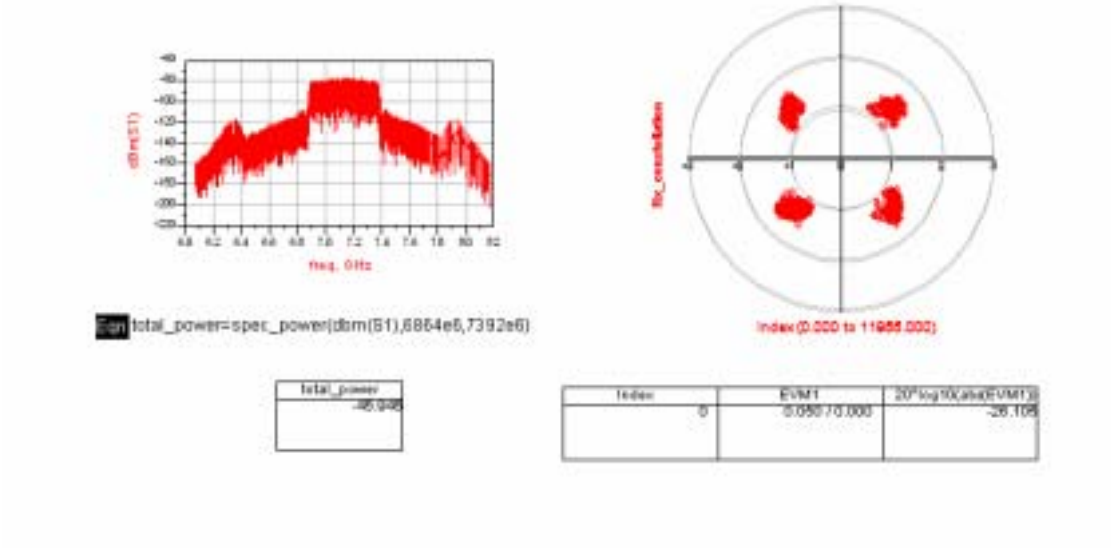


Figure 4.6. Co-simulation results – BAND_ID #8.

Figure 4.6, 4.7 shows the specific center frequency of 7128MHz and 8712MHz for band group 3, 4. The co-simulation results show that the proposed transmitter circuit performs well in the UWB applications. With the verification of RF/Baseband co-simulation, the proposed transmitter design is further studied by chip implementation and measurement which are described in the next chapter.

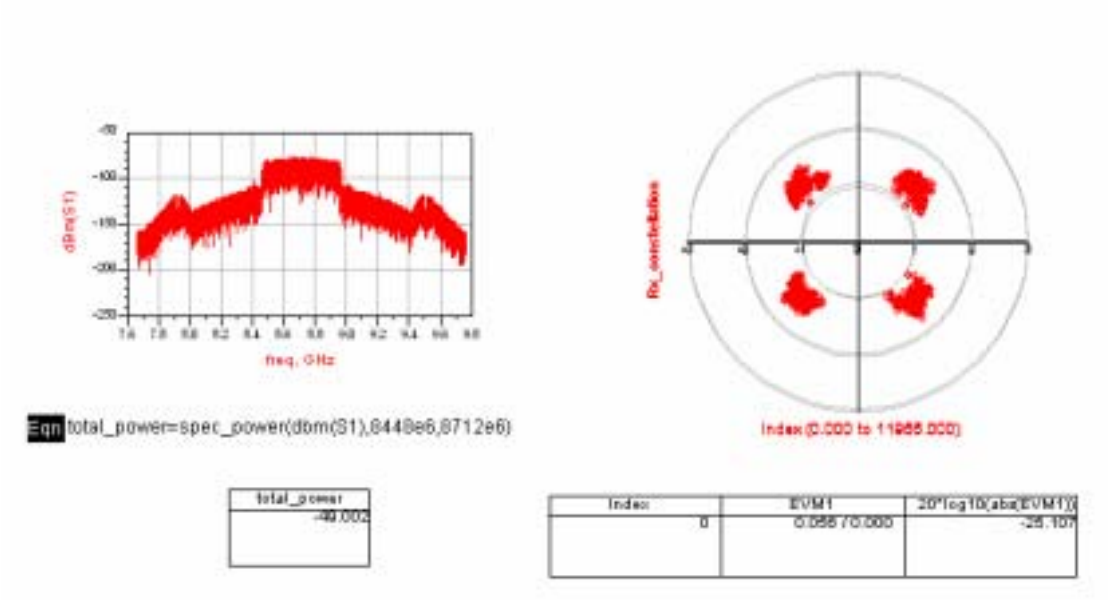


Figure 4.7. Co-simulation results – BAND_ID #11.

Chapter 5

Implementation and Measurement

After all the design and simulation result has been finished. This chapter will consider some back-end design including layout skill, design of printed circuit board (PCB), measurement setup…etc. Section 5.1 we will discuss some chip layout considerations. Section 5.2 addresses in ESD protection. Package effect is provided in Section5.3. In section 5.4 the PCB design is shown. Measurement setup is given in Section 5.5. Finally, the measurement results will be shows in Section 5.6. Section 5.7 summarizes this design work.

5.1 Chip Layout Considerations

Poor layout causes the performance degradation of the circuits, or even results in function fail. For the RF circuits operating in several GHz, the wavelength is in order of centimeters. In the microwave point of view, the wave flows through the metal line, changing its phase according to wave length and wire length. Since the output current of distributed amplifier will be added in the output port, the gate line length is equivalent to the drain line length in order to keep the same phase shift. Therefore, in layout consideration we must carefully draw the gate line length identical to the drain line length. Thus, each signal path will travel the same length from input (gate transmission line) to output (drain transmission line). Then the signal on the drain line adds in the forward direction as they arrive at the output. How to determine the

width of signal path is an important problem. The parasitic capacitance will be increased, if we increase the width of signal path. Nevertheless, narrow width of signal path will add parasitic inductor and resistor. To overcome the problem, we will consider transmission line concept. Many CAD tools can provide the characteristic impedance of the planar transmission line. Our design employs a 50Ω microstrip line, whose parameters are listed as follows: dielectric constant ε =4.1 (SiO_2), the height is 2.1 μm. Therefore, the width of a microstrip line can be obtained as 4 μm. The DC path should be wide enough to supply large current and increase the bypass capacitance to filter out supply noise. Overlapping of metal line is also prohibited. If they must be crossed, the influence must be taken into consideration. The length of four LO signals should be kept equal in order to get the same phase delay. Figure5.1 shows the layout of current reuse DA. Figure 5.2 shows the layout of dc feedback current reuse DA. The pad to pad distance must fit the probe for measurement.

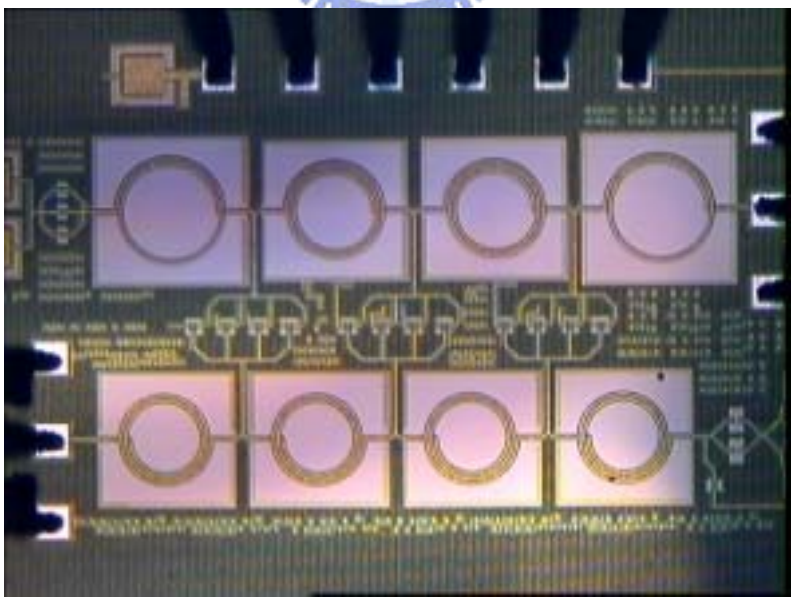


Figure 5.1. Microphotograph of current reuse DA

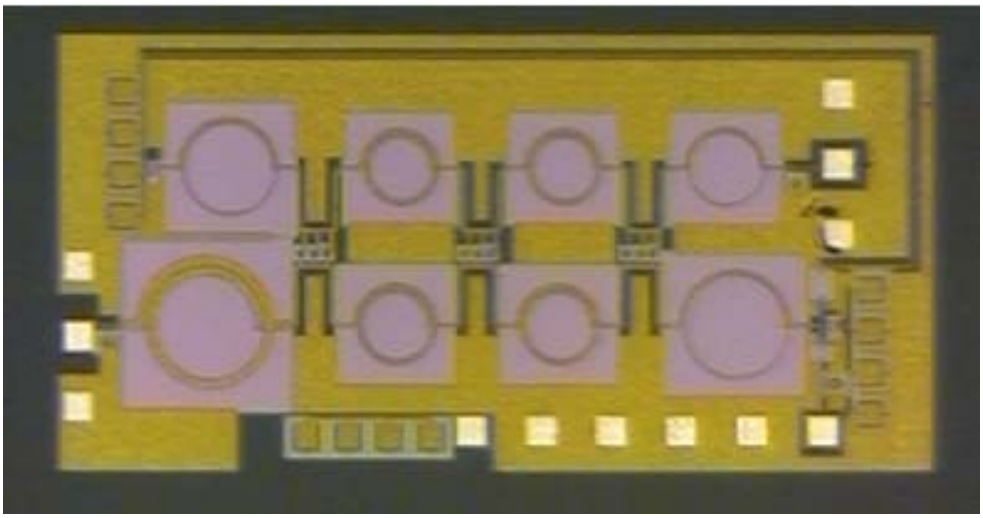


Figure 5.2. Microphotograph of DC feedback current reuse DA

5.2 ESD Protection

In package version, the electrostatic discharge (ESD) protection is added to each I/O pin. In 0.18μm process, the voltage limit that gate oxide can tolerate is only about 5V. Without any protection circuit, the MOSFET can be damaged permanently in about 10 potential applied at gate.

Therefore, the ESD circuits are shown in Figure 5.3. Diode chain protection guides the tremendous charge to VDD or GND, and a large ground NMOS will break down once a large potential across the VDD and GND, and induces the charge in VDD flows through NMOS to GND. The devices used in ESD have special restrictions. The gate ground MOS should avoid lightly-doped-drain which is common in deep submicron process. The distance between drain contact and boundary of gate and diffusion must be large too sustain higher static charge. Contacts on guard ring are also prohibited because that makes the break down of ESD device harder. This circuit is provided by UMC with 3.6kV human body mode (HBM) tolerance and induces around 40fF parasitic capacitance at each pad.

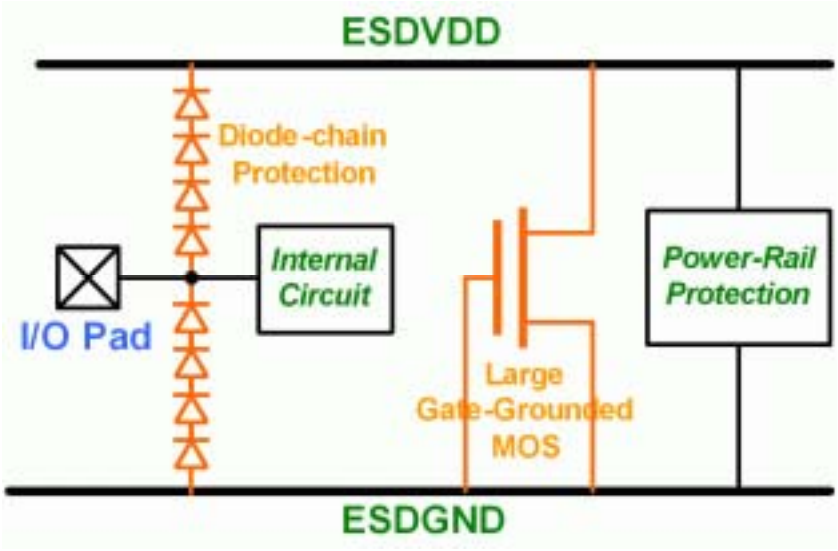


Figure 5.3. ESD Protection Circuits

5.3 Package Effect

The QFN20D package provided by SPIL is employed in our design. This package is limited by 20 I/O pins. The overall area of package is 2.5*2.5 mm^2. The package model for bond-wire is illustrated in Figure 5.4. For DC supply pins, especially VDD and GND, the 1nH parasitic inductor can change circuit performance or induce oscillation. So, the more bonds connect with dc supply pin to shunt the inductance smaller is essential. However, the high Q nature of the bonding wires can replace the on-chip spiral inductors to improve the circuit performance. Since different pins have different inductance values, with maximum difference of 0.2 nH, detailed inspection on the package model is required before using it. Figure 5.5 shows the microphotograph of UWB transmitter (package version). The pin assignment is summarized in Table. 5.1.

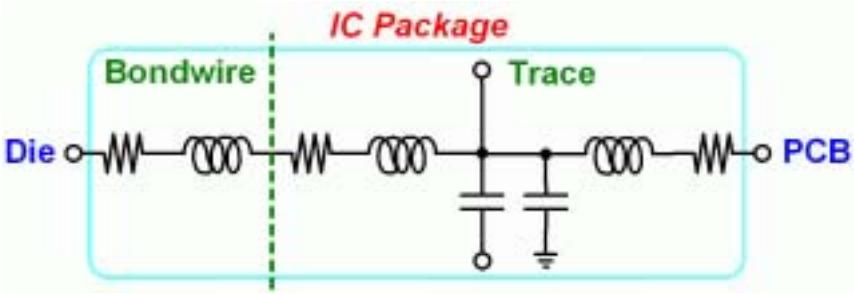


Figure 5.4. Package Model

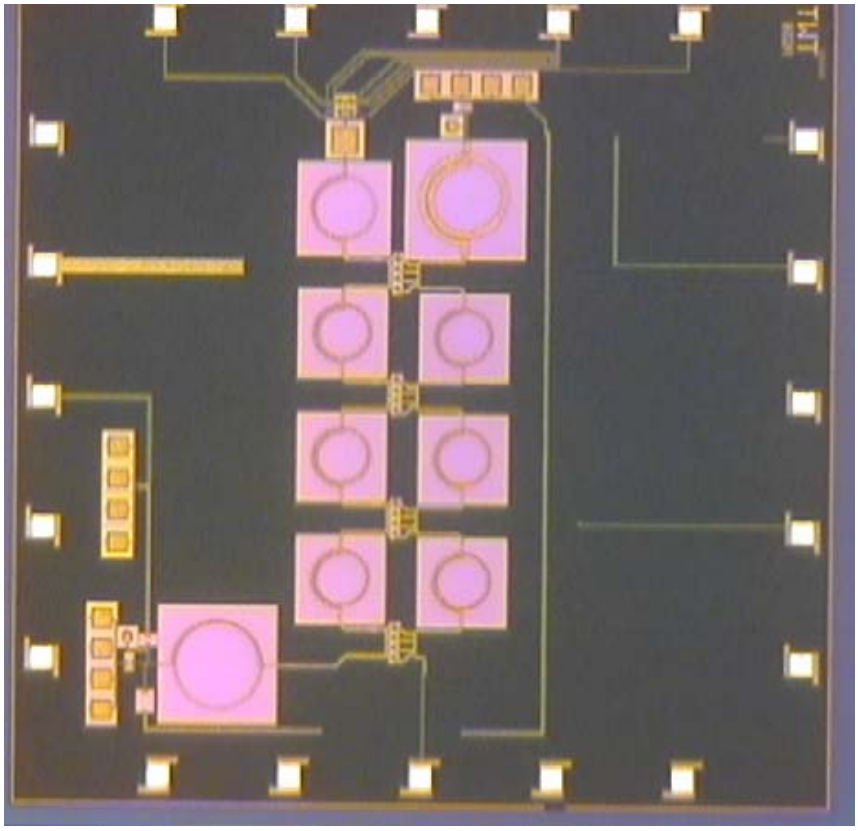


Figure 5.5. Microphotograph of UWB transmitter (package version)

Pin Number	Pin Name	Function
1	LOI+	0 degree of Signal of local oscillator
2	LOI-	180 degree of Signal of local oscillator
3	GND	GND
4	LOQ-	2700 degree of Signal of local oscillator
5	LOQ+	90 degree of Signal of local oscillator
6	GND	GND
7	VDD	1.6V power supply
8	VBIAS	0.65 power supply
9-12	GND	GND
13	Output	RF-output
14	GND	GND
15	ESD-VDD	3.3V power supply
16	BBI+	0 degree of 10MHz IF signal
17	BBI-	180 degree of 10MHz IF signal
18	GND	GND
19	BBQ+	90 degree of 10MHz IF signal
20	BBQ-	270 degree of 10MHz IF signal

Table 5.1. Pin Assignment of Package

5.4 PCB

Fig 5.6 shows the PCB layout using Protel. Our design employs a 50Ω microstrip line, which parameters are listed as follows: dielectric constant $\varepsilon_r = 3.38$, substrate thickness is 8mil, conductor conductivity is 5.8×10^7 Siemens/meter and conductor thickness is 34μm. Thus, the width of a microstrip line can be obtained as 17mil. We use "RO4003" as our dielectric owning to this material has less loss at high frequency operation. There are two bypass capacitances in dc bias path. One is to filter high frequency noise another is to filter low frequency noise. Because small capacitances have high resonant frequency, large capacitances have low resonant frequency.

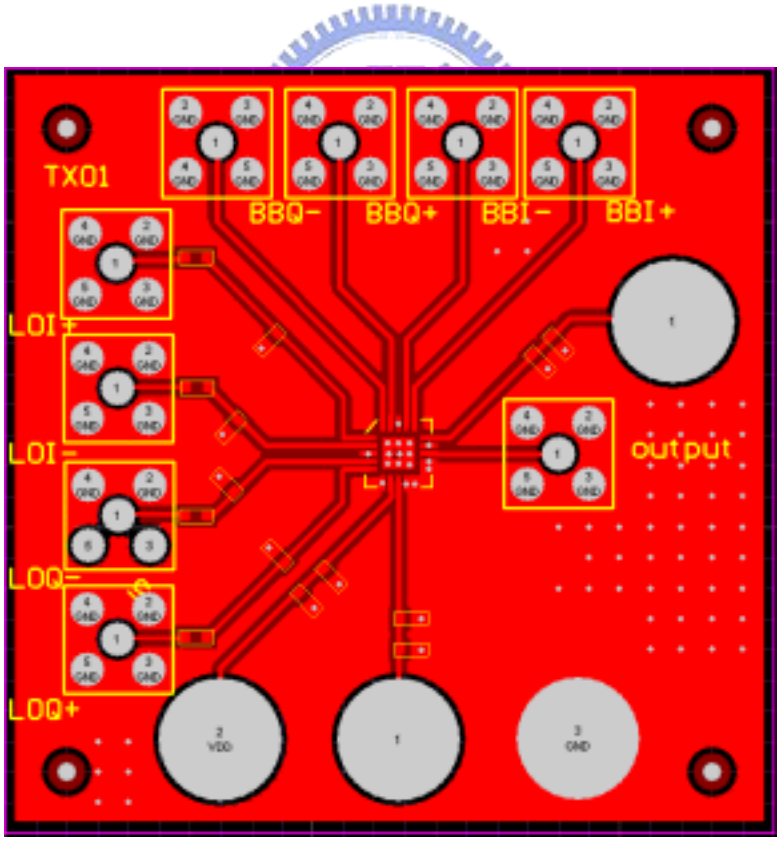


Figure 5.6. Layout of PCB

5.5 Measurement Setup

The measurement set up for RF circuit is an important issue. Next, we will discuss the measurement instruments and off chip components.

5.5.1 Instruments

Equipments needed to perform the measurement are listed below:

Signal Generator (ESG, Agilent E4438C) 250K~6.0GHz x1

Signal Generator (ESG, Agilent E4432C) 250K~3.0GHz x2

Spectrum Analyzer (PSA, Agilent E4407B) 9kHz ~26.5GHz x1

Power Supply (Agilent E3610A) 0~8V 3A,0~15V 2A x1

Designing the circuit must consider the impedance matching, and the network analyzer is required to examine the matching condition. However, the input impedance of Spectrum Analyzer (E4407B) is 50Ω.

5.5.2 Transformer

A transformer is used at input of transmitter to convert base band signal comes from ESG to differential and then input to the passive mixer. The transformer is shown in Figure5.7 which is produced by Mini-Circuits ADT4-6T.

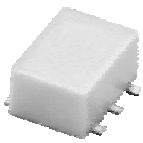


Figure 5.7. Transformer

5.5.3 Bias-Tee

Bias tee is used for combining the LO signal generated from ESG and DC voltage. The Bias-Tee is shown in Figure5.8 which is produced by Mini-Circuits ZNBT-60-1W.

Figure 5.8. Bias-Tee

5.5.4 Quadrature Phase Shifter

A quadrature phase shifter is used to convert single-tone signal comes from LO ESG of (3432MHz, 3960MHz, 4488MHz) band-group #1, band-group #3, to four output signals with quadrature phases. This quadrature phase shifter is designed and simulated by ADS and implemented on PCB using microstrip line.

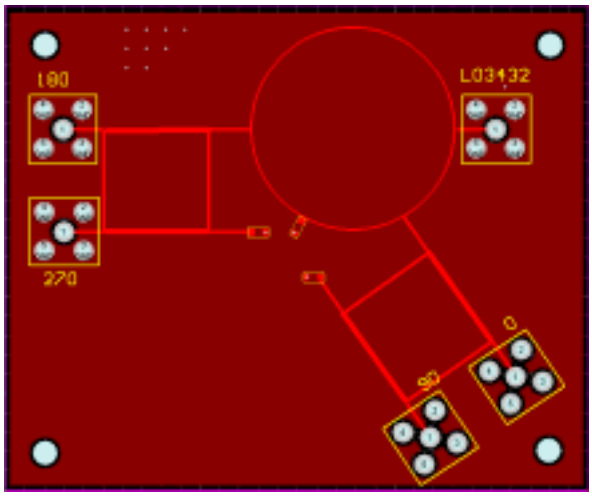


Figure 5.9. Quadrature Phase Shifter on PCB

The measurement phase and gain error of quadrature generator are listed in Table 5.2.

The phase error of the quatrature phase shift is within 10 ° .

Port Number	1	2	3	4
Loss	9.94 dB	8.4 dB	9.2 dB	12.8 dB
Phase	81.2 °	0 °	178 °	279 °

Table 5.2. Measured loss and phase of quadrature phase shift(Lo frequency 4488MHz)

5.5.5 Measurement Setup

The measurement setup for one-tone test is shown in Figure 5.10. Three signal generators have been used to supply two base band I/Q signals with 90° phase difference, and one LO signal. Two transformers and one quadrature phase shifter have been used for measurement. Output is detected by Agilent E4407B Spectrum Analyzer with another terminated by 50Ω.

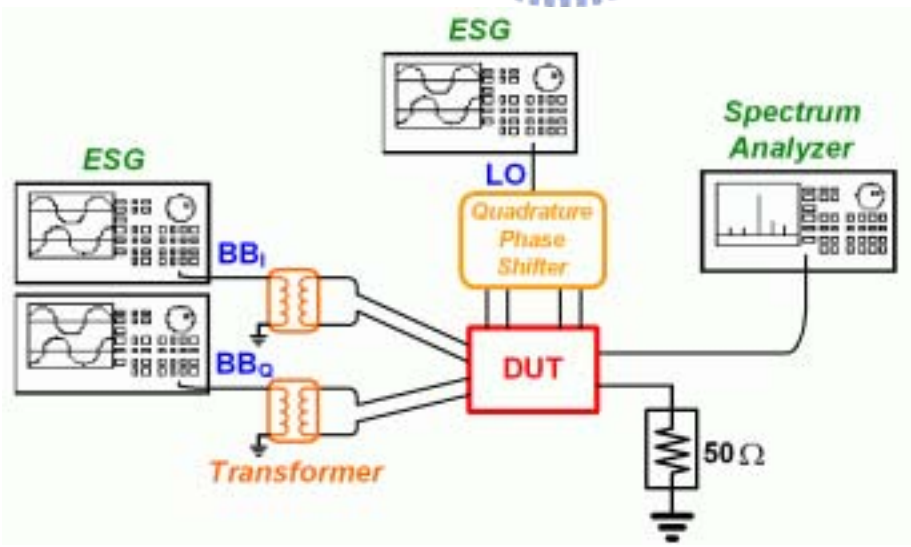


Figure 5.10. The measurement setup for one-tone test

5.6 Measurement Results

In this section, the measurement results of current reuse distributed amplifier, the dc feedback current reuse DA and the UWB transmitter package version is illustrated.

5.6.1 Current Reuse Distributed Amplifier

Figure 5.11 shows the measurement results of S-parameter of current reuse DA. The presented DA has 8GHz bandwidth which covers the frequency range of band groups 1, 2 and 3 of UWB applications, and 4-dB gain with 0.4-dB variation in the band of interesting. The maximum input return loss is -7.6 dB at 5GHz and S11 is below -10dB up to 7 GHz. The output return loss has a maximum value of 8.3 dB at 7.7 GHz and below 10dB up to 8.3GHz. The total power consumption is 23mW.

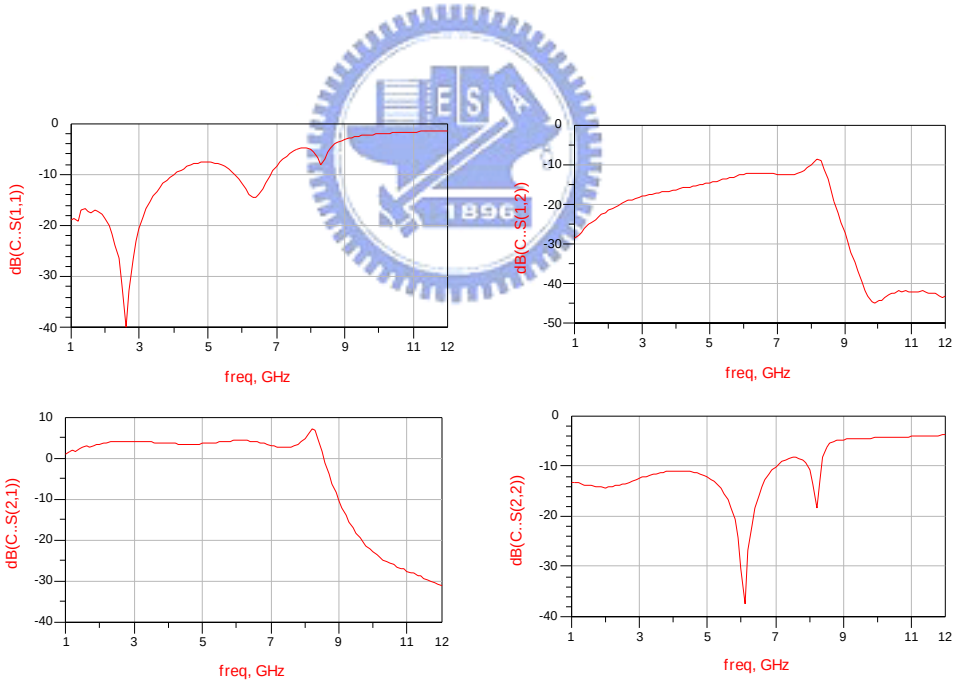


Figure 5.11. Measurement results of S-parameter

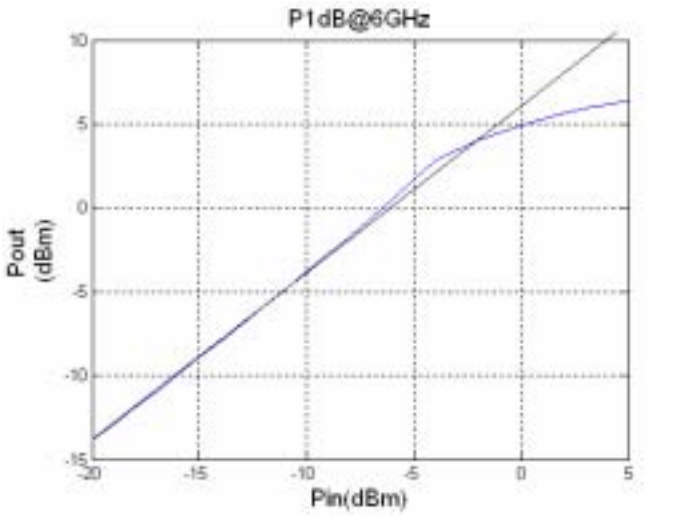


Figure 5.12. Measured output 1dB compression point of the current reuse DA

One-tone test of 6GHz is performed to measure the output 1dB compression point (OP1dB). Figure 5.12 shows the measured P1dB is 4dBm.

5.6.2 DC Feedback Current Reuse Distributed Amplifier

Second, the measurement results of DC feedback current reuse distributed will be illustrated. Figure 5.13 shows the measurement results of S-parameter of DC feedback current reuse DA. The presented DA has 7.9GHz bandwidth, which covers the frequency range of band groups 1, 2 and 3 of UWB applications, and 7-dB gain with 0.4-dB variation in the band of interesting. The maximum input return loss is –6.8 dB at 7.9GHz and S11 is below -10dB up to 7.6 GHz. The output return loss has a maximum value of 7.9 dB at 7.9 GHz and below 10dB up to 7.8GHz. Figure 5.14 and 5.15 show the S11 and S22 smith chart. One-tone test of 6GHz is performed to measure the output 1dB compression point (OP1dB). Figure 5.16 shows the measured OP1dB is 2dBm.

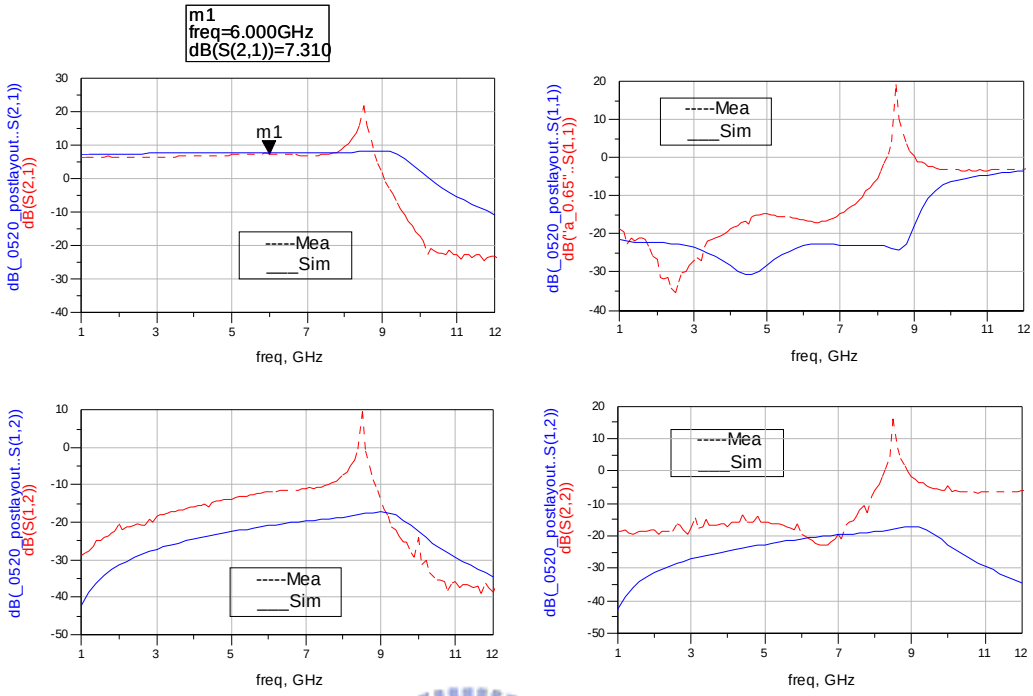


Figure 5.13. DC feedback current reuse DA measurement results S-parameter

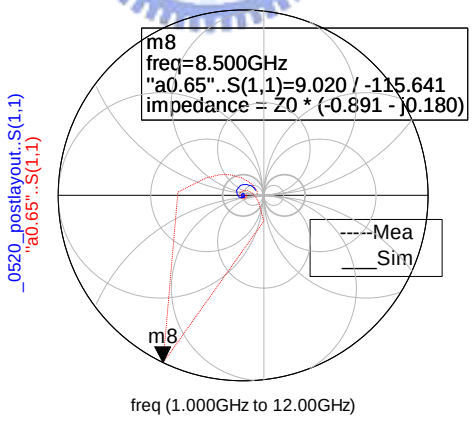


Figure 5.14. S11 in Smith Chart

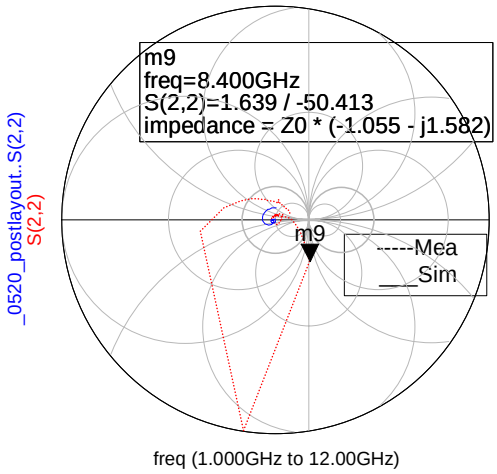


Figure 5.15. S22 in Smith Chart

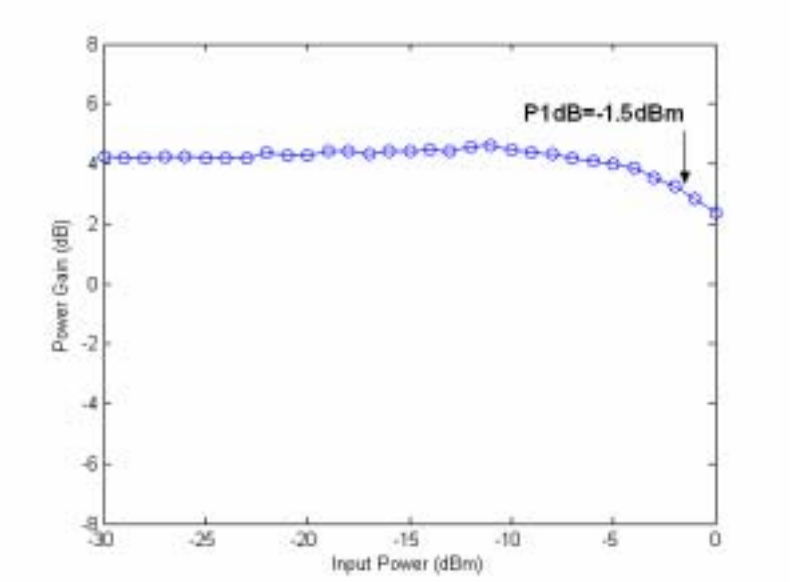


Figure 5.16. DC feedback current reuse DA measurement results-P1dB

Figure 5.17 shows the of DC feedback current reuse DA with input dc bias variation (±0.02V) which verify that it can maintain the performance in different dc level.

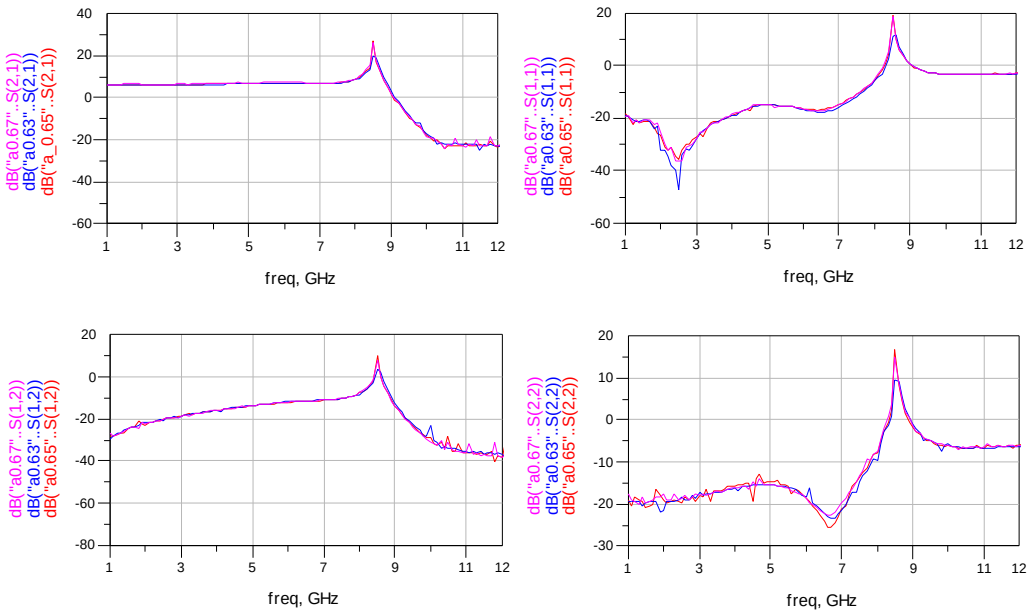


Figure 5.17. DC feedback current reuse DA with input dc bias variation(±0.02V)

5.6.3 The Analysis and Improvement of Oscillation Situation

There are two possible reasons for the oscillation situation.

(1) Feedback Resistance

The signal may pass through the feedback resistance from output to input to make S12 >0. Figure 5.18.shows the value of input resistance of different dc feedback resistance. As shown in figure 5.18, the input resistance does not change to negative value when dc feedback resistance changes from 345Ω to 915Ω. The positive input resistance does not let the signal pass through the feedback resistance from output to input to make S12>0.

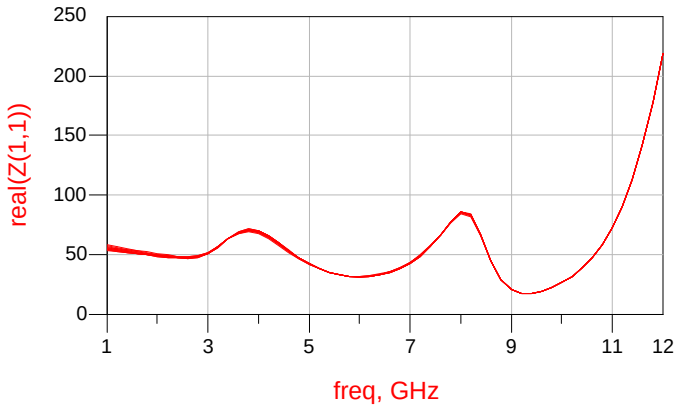


Figure 5.18. The input resistance of different dc feedback resistance

Next, if the termination resistance has large variation, the signal may be reflected to the feedback path. Figure 5.19 shows the value of input resistance of different termination resistance. As shown in Figure 4, the input resistance does not change to negative value when termination resistance is 30Ω. The positive input resistance does not let the signal pass through the feedback resistance from output to input to make S12>0.

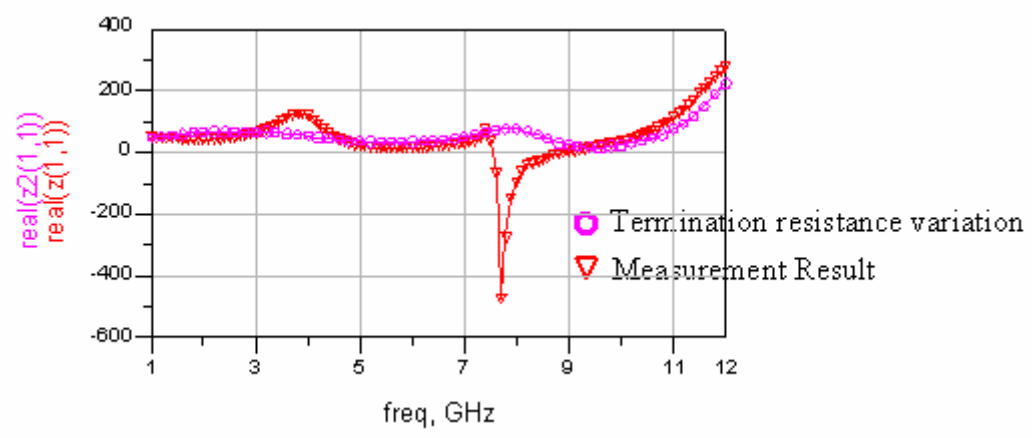


Figure 5.19. The input resistance of different condition

(2)C_{gd} feedback

Next, the C_{gd} capacitance may make the circuit unstable. For this reason, we add the C_{gd} (90fF)

capacitance in the first and third stage of DC feedback current reuse distributed amplifier as shown in Figure 5.20. Figure 5.21 shows that the S-parameter simulation result of adding C_{gd} in the circuit is similar to the measurement result.

The simulation results and measurement results also show it oscillates at 8.3GHz. The C_{gd} capacitance may be generated by substrate coupling or gate and drain mutual inductors.

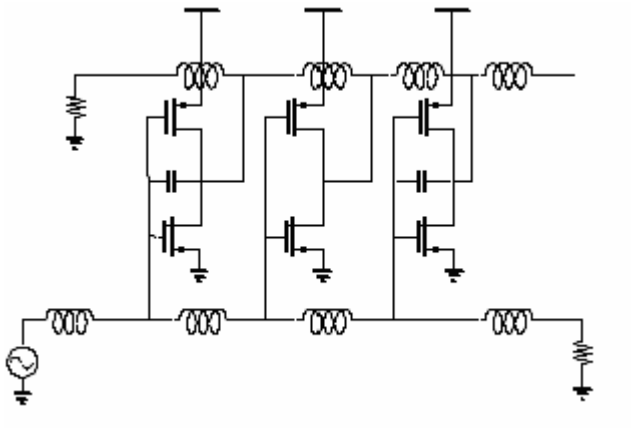


Figure 5.20. Add capacitances in DC feedback current reuse DA

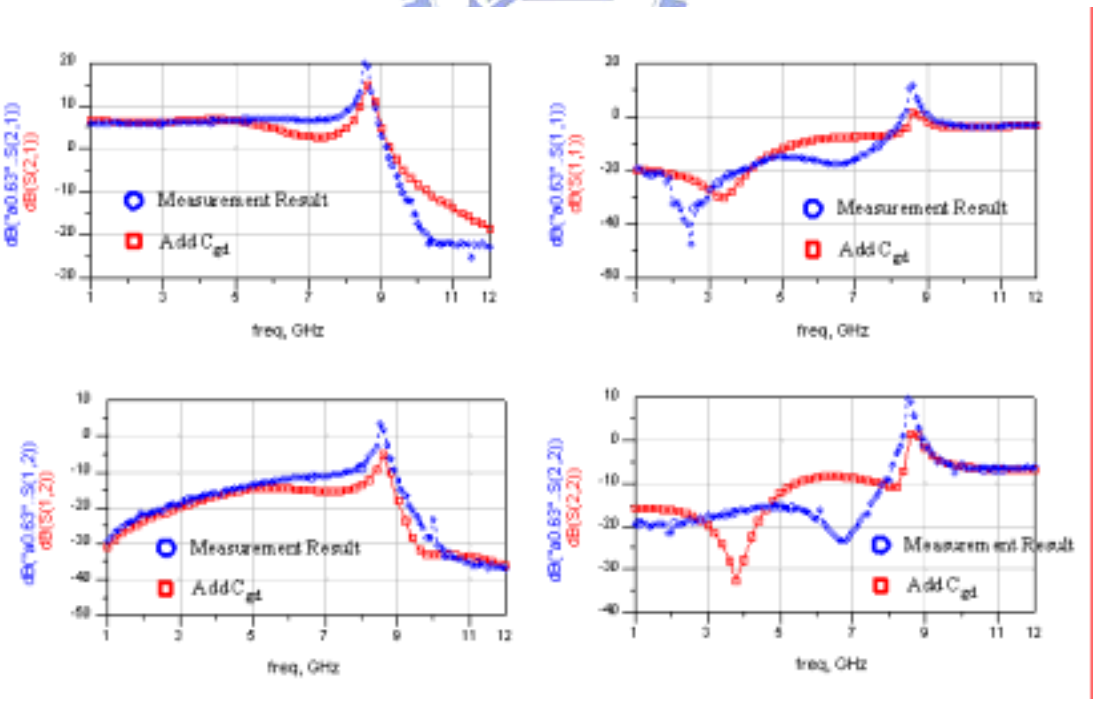


Figure 5.21. Simulation results of adding Cgd in the circuit and measurement result

5.6.4 UWB Transmitter (package version)

Since the frequency range of UWB is 3-10.6GHz, we use several baluns to cover the frequency range. Each of the center frequency is (3432MHz, 3960MHz, 4488MHz, 5250MHz, 6600MHz, 7128MHz, 8184MHz). The measured data are recorded and plotted by MATLAB. Figure 5.22 shows the output spectrum of one-tone up-conversion. The frequency of BB signal is 10MHz for measurement. The measured RF output frequency locates at 3.16GHz with -0.8dBm power while the input LO frequency locates at 3.15GHz with 5dBm power and the BB input signal is 10MHz with 13dBm power. After calibrating the loss contributing from cable, SMA connector, and the quadrature phase shifter at RF output path of 2.6dB and at LO path of 17dB, the power conversion gain of upper-side band is equal to $-0.8-(13)+2.6 \approx -11.2$, when the equivalent LO power is 5dBm.

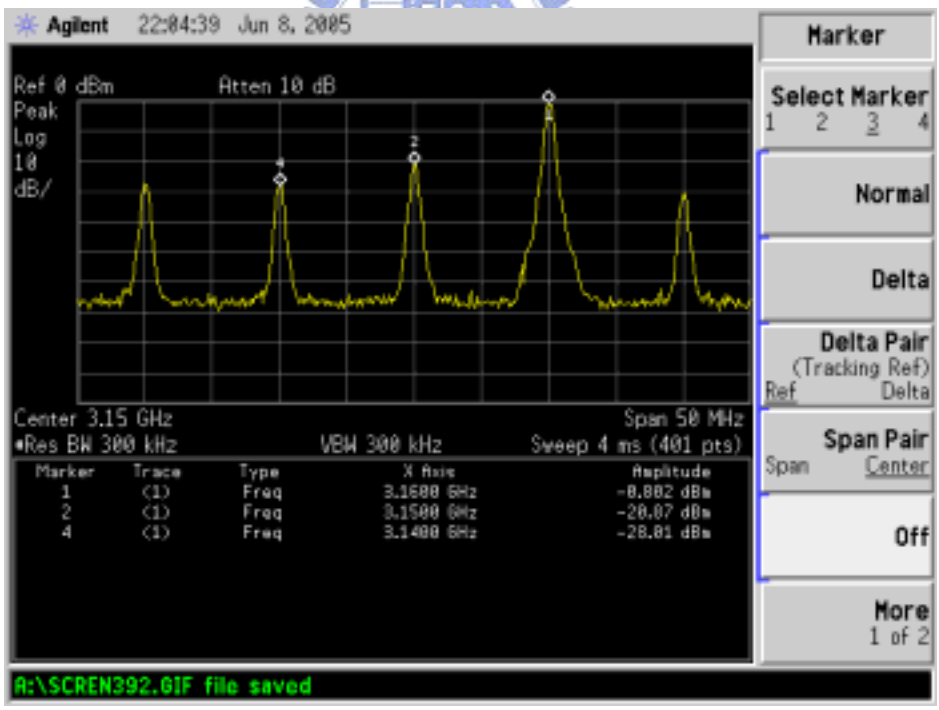


Figure 5.22. Output spectrum of one-tone up-conversion.

The frequency response of output power is shown in figure 5.23. The maximum output power is 0dBm at 3GHz of LO frequency. The average output power is -2dBm covers the frequency

of 3-8.3GHz.

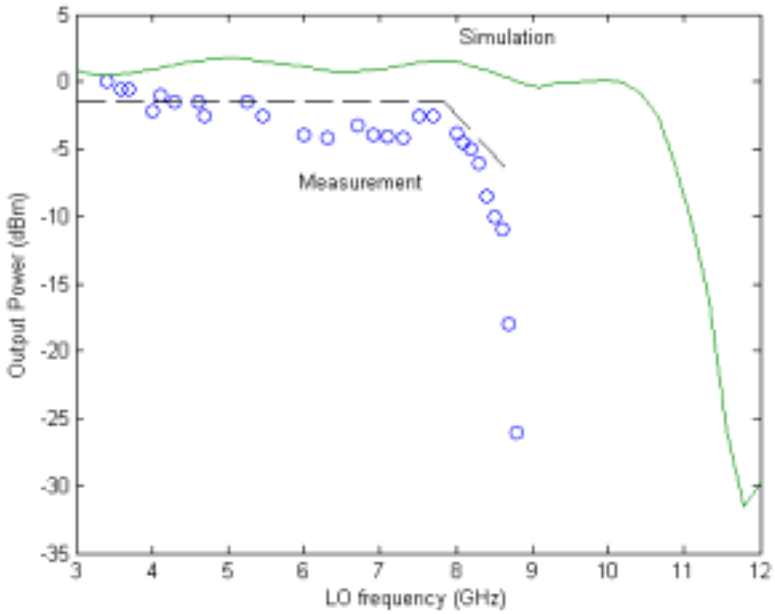


Figure 5.23. Frequency response of output power

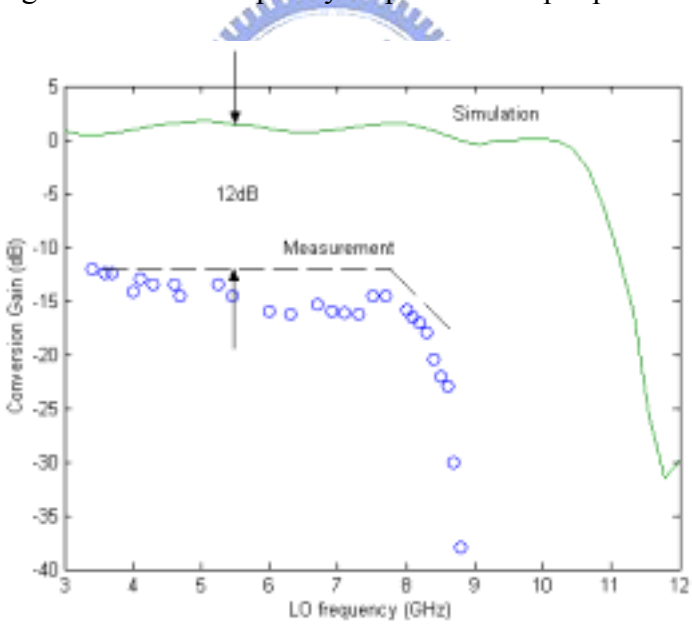


Figure 5.24. LO frequency vs. Conversion Gain

Figure 5.24 shows the average conversion gain is -12dBm covers the frequency range of 3-8.3GHz. Figure 5.25 shows the LO power vs. output Power in order to decide the LO power is 5dBm.

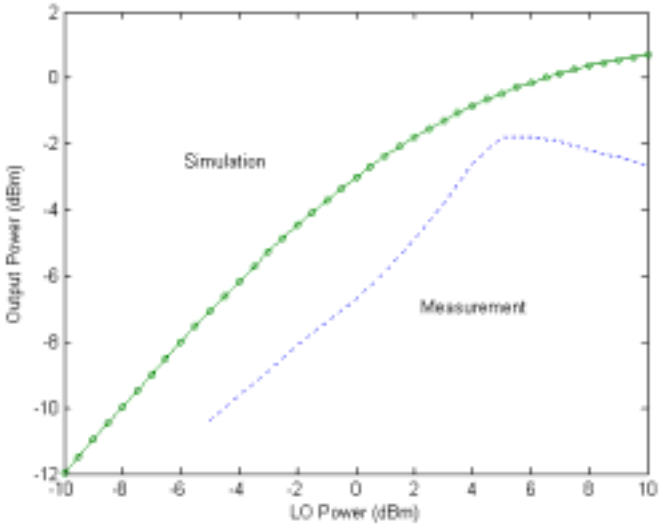


Figure 5.25. LO Power vs. Output Power

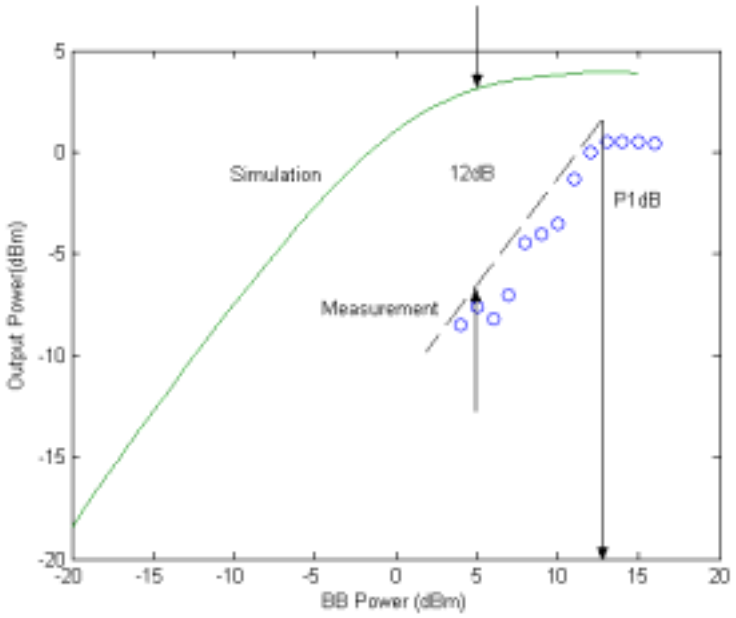


Figure 5.26. OP-1dB compression point

Figure 5.26 indicates that the output 1-dB compression occurs at 0dBm when the BB power of 13dBm is applied. The Lo frequency is 3432MHz to test output 1dB compression point.

5.7 Comparison & Summary

Table 5.3 summarizes the measurement results of current reuse DA (work1) and DC feedback current reuse DA (work2) for on wafer testing. We define the figure of merit (FOM) is the gain bandwidth product over the power consumption in order to compare with other topology.

$$FOM = \frac{Gain \times Bandwidth}{PowerConsumption} \tag{5.1}$$

	Tech	Gainmax (dB)	BW (GHz)	NFmin (dB)	OP1dB (dB)	Gain Cell	PDC (mW)	FOM
Work(1)	0.18μm	5.2dB	8	4.7dB	4dBm	CR	23	1.8
Work(2)	0.18μm	7.3dB	7.9	NA	2dBm	CR	15	3.845
[20]	0.35μm	6.5dB	6.3	3.4dB	10dBm	CS	50	0.819
[8]	0.6μm	7.7dB	4	5.4	7dBm	CS	83.4	0.369
[9]	0.6μm	7dB	7.5	8.7dB	N/A	Diff CS	216	0.243
[21]	0.35μm	20dB	3.5	2dB	N/A	CC	86.7	0.8
[22]	0.13μm	17dB	8	N/A	3.5dBm	CS	100	1.36
[12]	0.18μm	8.1dB	22	4.3	5.3dBm	CC	52	3.42

Table 5.3. Measurement Summary and Comparison

Parameters	This work	Specification
IC process	CMOS 0.18μm	CMOS 0.18μm
Die size	6.25 mm^2	6.25 mm^2
Power Consumption	20.8mW	20mW
Frequency	3~8.3 GHz	3-10.6GHz
Conversion Gain	-12 dB	0dB
Output P1dB	0dBm	0dBm
Sideband rejection	28dB	NA
Carrier rejection	20dB	NA

Table 5.4. Measurement Summary

According to Table 5.4, the major distinction between simulation and measured data is conversion gain. The conversion gain is about -12dB below the simulation results. Although the package model is added in the simulation, but it seems that the model is not accurate enough. In the package version design, the solder on the PCB implementation also affect the signal. The solder may lead to extra loss. Furthermore, the PCB design is not good enough.

Chapter 6

Conclusions and Future work

6.1 Conclusions

In this thesis, a novel topology current reuse distributed amplifier for UWB Pre-amplifier is proposed. Design optimization for the low power current reuse distributed amplifier in wide bandwidth applications is also presented. The novel topology of current reuse distributed amplifier is applied to the RF front-end design for the UWB direct conversion transmitter and using the feedback resistance to fix the output dc voltage in order to maintain excellent performance. Implemented in 0.18-μm CMOS technology, the Current Reuse topology provides a maximum forward gain (S21) of 5.2dB while drawing 23 mW from a 1.8V supply. The maximum output power of 4dBm and a high linearity IIP3 of 13 dBm have been measured. The measurement results of dc feedback current reuse DA provides a

maximum forward gain (S21) of 7.3dB while drawing 15 mW from a 1.6V supply. The maximum output power is 2dBm. UWB transmitter front-end of package version shows the average conversion gain is -12dBm and the average output power is -1dBm covers the frequency range of 3-8.3GHz. The output 1-dB compression point occurs at 0dBm using the frequency of 10MHz BB signal.

6.2 Future Works

In future works, we will improve the performance for each of the circuits. The dc feedback current reuse DA should use the EM simulation tools to verify the performance. Input and output port should add the m-derived matching network to reform the return loss and stability. The switch preamplifier and mixer can be applied in UWB system for different band groups. Finally, we should suggest implementing an on chip VCO in order to mitigate the difficulty on measurement. Therefore, the bulky quadrature phase shift could be saved.

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G.L.;Wiesbauer, A.; Sandner, C.;Radio Frequency Integrated Circuits (RFIC)Symposium, 2004. Digest of Papers. 2004 IEEE6-8 June 2004 Page(s):87 - 90

Publication List

1. **Hsiang-Lin Huang, Mei-Fen Chou, Wen-Shen Wuen and Kuei-Ann Wen and Chun-Yen Chang, "A low power CMOS Distributed Amplifier," 7th 2005 IEEE Wireless and Microwave Technology Conference, Clearwater, April 2005.**

Vita

Hsiang-Lin Huang

eric.ee92g@nctu.edu.tw

Hsiang-Lin Huang was born in Taipei, Taiwan, R.O.C., in 1981. He received the B.S. degree in electronic engineering from Chung Cheng University, Chia-Yi, in 2003. He worked toward the M.S. degree in electrical engineering at the National Chiao-Tung University, Hsinchu, Taiwan from 2003 to 2005.

His current research interests include RF front-end circuits for communications.

Education

M.S. Degree in Electronics Engineering, National Chiao Tung University 2005

B.S. Degree in Electronic Engineering, Chung Cheng University 2003

住址：台北市新生南路一段 165 巷 27 號 3 樓