A Wide Tuning Range G_m–C Filter for Multi-Mode CMOS Direct-Conversion Wireless Receivers

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***Abstract*—A third-order channel selection filter for multi-mode direct-conversion receivers is presented. The filter is designed with a Butterworth prototype and with the target wireless applications of Bluetooth, cdma2000, Wideband CDMA, and IEEE 802.11a/b/g/n wireless LANs. Linear-region MOS transistors are used to perform voltage-to-current conversion. The wide tuning range is achieved by the current multipliers and linear voltage-to-current converters. Implemented in the TSMC 0.18 μm CMOS process, the measurement results show that the filter can operate successfully over a cutoff frequency range of 500 kHz to 20 MHz, and is compliant with the requirements of different wireless applications. The power consumption is 4.1 mW to 11.1 mW for minimum and maximum cutoff frequencies respectively from a 1.2 V supply voltage. The circuit performance compares favorably with previously reported works.**

***Index Terms*—Current multiplier, direct-conversion receiver, multi-mode, transconductor, wide tuning range.**

I. Introduction

As THE LEVEL of integration in RF transceivers increases, CMOS emerges as the technology with the greatest potential for cost effectiveness where RF, mixed-signal and digital circuits are integrated in a single system-on-chip (SoC). This is particularly true when multi-mode wireless chip sets are embedded into mobile computing or multimedia systems. When designing a wireless receiver, one of the most important tasks is to design the channel filtering to separate the desired signal from the unwanted ones. Recent demand for multi-standard transceivers calls for adopting direct-conversion architectures to achieve the highest level of integration and for ease of system design. Fig. 1 shows a block diagram of a direct-conversion receiver. It converts the RF signal with both desired and unwanted signals, directly to baseband. Since the unwanted signals are still left at adjacent channel, the received signal is selected by the channel selection filter for further demodulation. However, an array or a stack of channel selection filters in a multi-standard radio design may not be power-efficient and would need large chip areas. Therefore, there is a strong motivation to realize a single baseband channel select filter such that it meets the requirements of multi-mode applications.

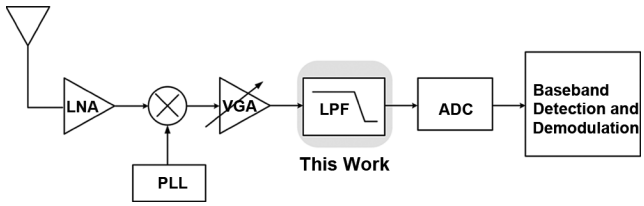

Fig. 1. Simplified block diagram of a direct-conversion receiver.

This work focuses on the design of such a multi-mode channel selection filter and is targeting direct-conversion radio architectures. The filter is designed based on a *G_m–C filter* topology, and has a wide continuous tuning range. The large tuning range is designed to meet the wireless specifications of Bluetooth (650 kHz), cdma2000 (700 kHz), Wideband CDMA (2.2 MHz), IEEE 802.11a/g (10 MHz), IEEE 802.11b (12 MHz), IEEE 802.11n (20 MHz) wireless LANs applications. These specifications cover the frequency range from 650 kHz to 20 MHz.

Most G_m–C filters encounter noise and linearity tradeoff when they are utilized for large tuning-range application. They usually suffer from either low linearity or high noise. From system level analysis, the input-referred noise within the specified bandwidth can be determined by giving the RF front-end gain. The noise level defines the sensitivity of a receiver where the minimum acceptable level can be detected, and the gain of the RF front-end section should be chosen so that the output stage would not saturate under system specification. From the Friis equation, the noise figure (NF) of the receiver is given by

$$\mathrm{NF}_{\mathrm{Total}} = \mathrm{NF}_{\mathrm{RF}} + \frac{\mathrm{NF}_{\mathrm{BB}} - 1}{A_{\mathrm{RF}}^2} \tag{1}$$

where $\mathrm{NF}_{\mathrm{Total}}$, $\mathrm{NF}_{\mathrm{RF}}$ and $\mathrm{NF}_{\mathrm{BB}}$ are the noise figure of receiver, RF front-end, and analog baseband. The analog baseband includes the analog filter and the programmable gain amplifier. When the output impedance of the RF front-end is given by Rs_{RF}, the input-referred noise of analog baseband section can be expressed as

$$\mathrm{NF}_{\mathrm{BB}} = 1 + \frac{v_{n,out}^2}{4kTRs_{\mathrm{RF}}A_{\mathrm{BB}}^2} = 1 + \frac{v_{n,in}^2}{4kTRs_{\mathrm{RF}}} \tag{2}$$

where k is the Boltzmann coefficient and $v_{n,in}^2$ is the input-referred noise power specified for 1 Hz bandwidth. Therefore, we can relax required noise specification by giving a larger RF

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front-end gain. However, we should note that the linearity performance is defined by

$$\frac{1}{A^2_{\mathrm{IP3,Total}}} = \frac{1}{A^2_{\mathrm{IP3,RF}}} + \frac{A^2_{\mathrm{RF}}}{A^2_{\mathrm{IP3,BB}}} \tag{3}$$

where $A_{\mathrm{IP3,Total}}$, $A_{\mathrm{IP3,RF}}$ and $A_{\mathrm{IP3,BB}}$ are the input third-order intercept point (IIP3) of the system, RF front-end, and analog baseband sections. It is clearly shown that larger RF front-end gain will amplifier blockers and relax the noise performance of the baseband section. To define the noise specification in the system design, the RF front-end gain can be obtained by giving largest blocker in RF front-end stage, and can be enlarged by pushing the linearity requirement to the baseband stage. Then, the noise specification of the baseband stage can be relaxed. The analysis for a multi-mode receiver front-end requires a range of input signal magnitude specifications that cover all the operation modes. Assuming that the receiver provides a NF of 9 dB, an overall IIP3 of -9 dBm, and a gain requirement between 10 and 100 dB, the range of all the requirements for the baseband section is the result of an optimal tradeoff among gain, noise, and linearity throughout the receiver blocks. By giving the system analysis and the scenario simulated over the receiver, the acceptable levels of the filter IIP3 for GSM/cdam2000, Wideband CDMA, and IEEE 802.11 mode are 19.2 Bm, 21.1 dBm, and 19.6 dBm, respectively.

For the G_m–C topology, a transconductor is used as a basic building block [1]–[5], and the transconductance value is proportional to the -3 dB cutoff frequency of the filter. The application mode is selected by changing the transconductance, and a tuning ratio of 30 is required. However, when process and temperature variations are taken into account, a tuning ratio of more than 50 should be achieved and the linearity performance should be still maintained at acceptable levels.

In this paper, Section II develops the proposed high linearity transconductor with a wide transconductance tuning range. The third-order Butterworth G_m–C filter which meets the required specification is presented in Section III. Section IV presents the measurement results and compares the proposed design with the state of the art. Finally, conclusions are addressed in Section V.

II. Proposed Transconductor Circuit

The main function of a transconductor is to convert the input voltage into the output current with a linear transformation factor, and the transconductor employed in filters must be linear over the input signal swing range. On the other hand, the transconductance should be tuned to compensate for process and temperature variations, and we can model it as a voltage controlled current source. In the circuit implementation, bipolar transistors offer wide transconductance tunable range because the collector current can be varied with little change in the base-emitter voltage. In contrast, the bias of the MOS transistors should be varied significantly and the supply voltage would then limit the tuning range, which implies the requirement of a higher supply voltage. Thus, a high linearity and wide tuning range transconductor in a low voltage CMOS technology would not only be needed for multi-mode wireless applications but also be helpful to combine with digital circuits for a system on a chip design.

A. The Voltage-to-Current Conversion in CMOS Technology

Fig. 2(a) shows a conventional transconductor, where the voltage-to-current conversion is obtained by using an operational amplifier through a passive resistor. The current is then sensed and mirrored to the output node. In this circuit, an array of resistors should be used to make the transconductance tunable. This method will increase the chip area and the precision of the transconductance would be limited by the choice of the programmable resistors. To achieve transconductance tuning, a single linear region transistor, shown in Fig. 2(b), is used to replace the passive resistor. This circuit is a MOSFET-only configuration. When the NMOS operates in the linear region, a linear drain current is obtained, and a linear voltage-to-current relationship for the circuit in Fig. 2(b) is presumably obtained. From a simplified BISM Level 3 model, the drain current is given by

$$I_{\mathrm{D,lin}} = K_{\mathrm{lin}}(V_{\mathrm{GS}} - V_{\mathrm{thn}})V_{\mathrm{DS}} - \frac{1}{2}\alpha K_{\mathrm{lin}} V^2_{\mathrm{DS}}$$
$$\text{where} \quad \alpha = 1 + \frac{1}{2}\gamma\,(2\Phi_f + V_{\mathrm{BS}})^{-1/2} \tag{4}$$

where γ is the body effect factor and Φ_f is the surface inversion potential. $K_{\mathrm{lin}} = \mu_n C_{\mathrm{ox}}(W/L)$, W and L are the width and length of the device, respectively, C_{ox} is the oxide capacitance per unit channel area, μ_n is the low-field mobility, and V_{thn} is the NMOS threshold voltage. V_{GS} and V_{DS} are the gate-to-source and drain-to-source voltages, respectively. By taking the process and temperature variation into consideration, α can be chosen to be a value of 1.2.

We can now see that the output current would not really hold a linear relationship to the input voltage owing to the additional second term in (4), which thus degrades the linearity of the transconductor. We can find that the second term in (4) forms a square-law equation. Previous research [6] reports that another transistor could be added to cancel out the second term in (4) based on the large signal square-law equation in the saturation region. Thus, the output current would be proportional to the input voltage, and the transconductance can be tuned by adjusting the bias voltage at the gate terminal. In the circuit, the -40 dB total harmonic distortion (THD) was reported. There are several disadvantages of this linearization technique. First, extra complex circuit should be included for current cancellation, and this technique needs an extra operational amplifier, which implies more power consumption. Second, the constraint of linear region operation, $V_{\mathrm{GS}} - V_{\mathrm{t}} > V_{\mathrm{DS}}$, should be held and this condition is hard to sustain under wide tuning requirement. Finally, it would not work well in modern nanoscale CMOS technologies owing to the fact that short channel effects would alter the square-law behavior and then degrades nonlinearity cancellation.

Since the compensation technique reported in [6] is based on a single-ended structure and is not suitable to provide the required high linearity and low power for transconductor design in modern CMOS process, a differential structure can be simply used to cancel out the second term in (4). Therefore, we can take the single-ended circuit of Fig. 2(b) and use it in a fully differential mode as shown in Fig. 2(c). To obtain the voltage-to-current

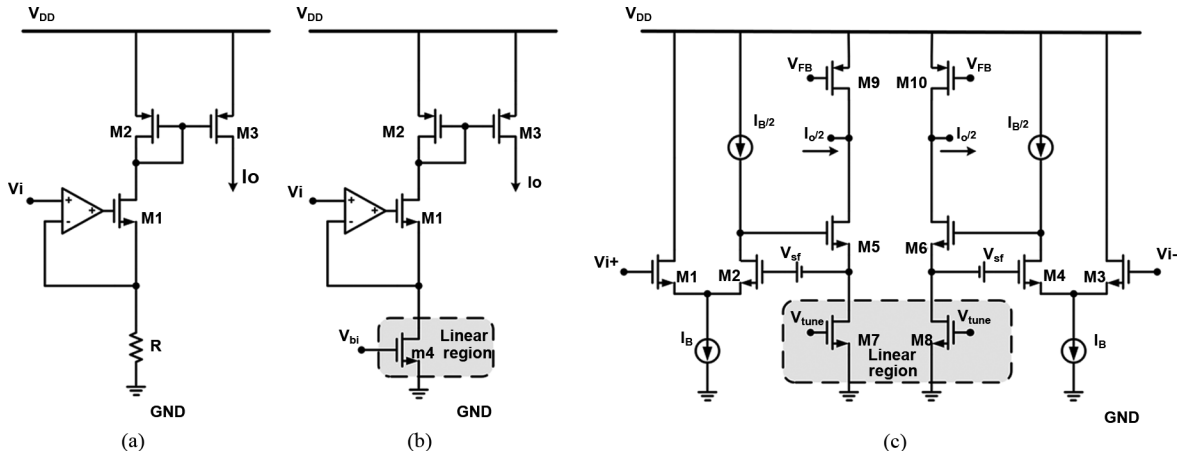

Fig. 2. (a) Conventional transconductor. (b) MOSFET-only transconductor. (c) Differential transconductor.

characteristics of the circuit, the input differential voltages at the gate of transistors M1 and M2, are given by

$$V_{i+} = V_{\rm cm} + \frac{v_d}{2} \tag{5}$$

$$V_{i-} = V_{\rm cm} - \frac{v_d}{2} \tag{6}$$

where $V_{\rm cm}$ is the input common-mode voltage and v_d is the input differential voltage. The gate terminals of the linear-region transistors M7 and M8 will be biased at an appropriate voltage, $V_{\rm tune}$, to make sure the linear region operation is achieved. The second term in (4) can be cancelled out by the inherent differential structure, and thus the output current would be given by

$$i_{\rm out} = K_{\rm lin}(V_b - V_{\rm thn} - \alpha V_{\rm cm})v_d. \tag{7}$$

The equation shows that a linear voltage-to-current conversion is obtained, and that the output current is dependent on the bias voltage and the input common-mode voltage.

B. The Proposed Transconductor With Tuning Scheme

Followed the basic concept of the differential structure in Fig. 2(c), wide range transconductance tuning is hard to achieve by adjusting $V_{\rm tune}$ and $V_{\rm cm}$. In general, $V_{\rm tune}$ should be biased at a higher voltage, such as the supply rail, and then the transistor would always work in deep linear region and perform a highly linear operation. Thus, a high linearity current multiplier would be required following the voltage-to-current conversion.

Fig. 3 shows the concept of the transconductor, which has a wide transconductance range. In the proposed transconductor, the linear voltage-to-current conversion is performed first, and then the transconductance is tuned over a wide range using the translinear loop that follows. The translinear loop is to provide the function of current multiplier. Through the use of the feedback loop, linear voltage-to-current conversion can be obtained owing to the fact that the input voltage would be equal to the drain voltage of transistors M1 and M2. Thus, the current flowing through resistors R_{1a} and R_{1b} would have a very high linearity relationship with the input voltage. The current multiplier is composed by transistors M1 to M4, resistors R_{1a} and

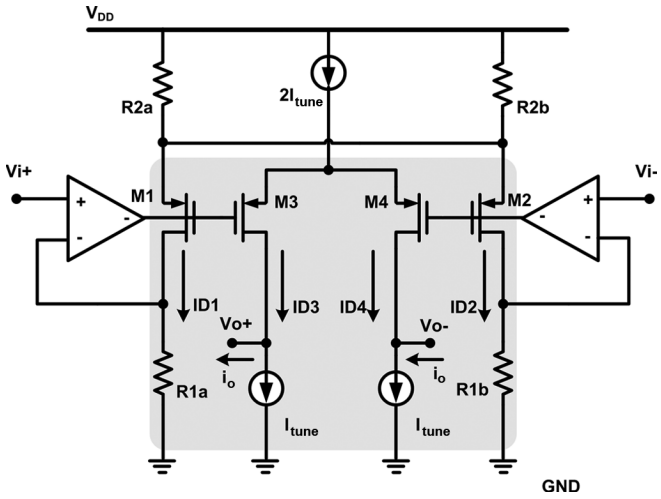

Fig. 3. Concept of a wide tuning range transconductor.

R_{1b}, and current source $I_{\rm tune}$. Transistors M1 to M4 are biased to operate in the weak inversion region while suitable device sizes are used. A single expression of the transistor model useful in weak, moderate, and strong inversion regions with $V_{\rm DS}$ larger than a few times of the thermal voltage $U_{\rm T}$, is employed [7]

$$I_{\rm D} = I_{\rm S} \ln^2 \left[1 + e^{(V_{\rm GS} - V_{\rm TH})/2nU_{\rm T}}\right] \tag{8}$$

where $I_{\rm S}$ is the fitting parameter, n is the subthreshold slope factor, $V_{\rm th}$ is the transistor threshold voltage, and $U_{\rm T}$ is the thermal voltage. The inversion factor defined by $F = I_{\rm D}/I_{\rm S}$ is often used to define the boundaries between the MOS inversion regions. When $F \gg 1$, the operation region is corresponding to the strong inversion. On the opposite, the operation region is corresponding to the weak inversion when $F \ll 1$. The expression can fit the case of the general weak to strong inversion equations. For a MOSFET operating in the weak inversion region, its current exhibits an exponential dependence on $V_{\rm GS}$, and can be expressed from (8) to obtain

$$I_{\rm D} = I_{\rm D0} \frac{W}{L} \exp\left(\frac{V_{\rm GS} - V_{\rm th}}{nU_{\rm T}}\right) \tag{9}$$

where W and L are the width and the length of the transistor, respectively, and I_{D0} is the reverse saturation current. From the above equation, we can find that

$$V_{\mathrm{SG1}} - V_{\mathrm{th}} = nU_{\mathrm{T}} \left(\frac{I_{\mathrm{D1}}}{I_{\mathrm{D0}}} \frac{L_1}{W_1} \right) \tag{10}$$

$$V_{\mathrm{SG2}} - V_{\mathrm{th}} = nU_{\mathrm{T}} \left(\frac{I_{\mathrm{D2}}}{I_{\mathrm{D0}}} \frac{L_2}{W_2} \right). \tag{11}$$

The device sizes of transistors M1 and M2 are set to be the same, and so are transistors M3 and M4. We can obtain from the linear conversion, $I_{\mathrm{D1}} = I_1 + i_i$ and $I_{\mathrm{D2}} = I_1 - i_i$, where $I_1 = V_{\mathrm{cm}}/R_{1(a,b)}$. We can have

$$\Delta V = V_{\mathrm{SG1}} - V_{\mathrm{SG2}} = V_{\mathrm{SG3}} - V_{\mathrm{SG4}} = nU_{\mathrm{T}} \ln \left(\frac{I_1 + i_i}{I_1 - i_i} \right). \tag{12}$$

The current output from the differential pair of transistors M3 and M4 can be expressed by

$$I_{\mathrm{D3}} = \frac{2I_{\mathrm{tune}}}{1 + e^{-\Delta V/nU_{\mathrm{T}}}} = \frac{2I_{\mathrm{tune}}}{1 + \left(\frac{I_1 - i_i}{I_1 + i_i} \right)} = I_{\mathrm{tune}} + \frac{I_{\mathrm{tune}}}{I_1} i_i \tag{13}$$

$$I_{\mathrm{D4}} = \frac{2I_{\mathrm{tune}}}{1 + e^{\Delta V/nU_{\mathrm{T}}}} = \frac{2I_{\mathrm{tune}}}{1 + \left(\frac{I_1 + i_i}{I_1 - i_i} \right)} = I_{\mathrm{tune}} - \frac{I_{\mathrm{tune}}}{I_1} i_i. \tag{14}$$

Finally, the output current i_o is given by

$$i_o = I_{\mathrm{D3}} - I_{\mathrm{tune}} = I_{\mathrm{tune}} - I_{\mathrm{D4}} = \frac{I_{\mathrm{tune}}}{I_1} i_i. \tag{15}$$

Thus, the output current is equal to a scaled value of the input current. The transconductance tuning can be achieved and the scaling can be determined by the bias current I_{tune}. In the circuit, the transconductance in the weak inversion region can be expressed as

$$\mathrm{G}_{\mathrm{m,weak}} = \frac{I_{\mathrm{tune}}}{V_{\mathrm{cm}}}. \tag{16}$$

In case of a large I_{tune} current, transistors M3 and M4 will enter into the saturation region while transistors M1 and M2 are still in the weak inversion region. From the equation of a differential amplifier in the saturation region, the output current i_o can be expressed as

$$i_o = \frac{I_{\mathrm{D3}} - I_{\mathrm{D4}}}{2} = \frac{K_{3,4}}{4} (\Delta V) \sqrt{\frac{4I_{\mathrm{tune}}}{K_{3,4}} - \Delta V^2} \tag{17}$$

where ΔV is the gate differential voltage expressed in (12), and the value can be simplified by neglecting high order terms from a Taylor series expansion. Therefore, we can have

$$\Delta V = nU_{\mathrm{T}} \ln \left(\frac{I_1 + i_i}{I_1 - i_i} \right) \approx nU_{\mathrm{T}} \frac{2i_i}{I_1}. \tag{18}$$

We can substitute (18) into (17) to obtain the output current. For a small ΔV^2 compared to $4I_{\mathrm{tune}}/K_{3,4}$

$$i_o \approx \frac{K_{3,4}}{4} (\Delta V) \sqrt{\frac{4I_{\mathrm{tune}}}{K_{3,4}}} = nU_{\mathrm{T}} \frac{i_i}{2I_1} \sqrt{K_{3,4} I_{\mathrm{tune}}}. \tag{19}$$

Then, the transconductance becomes

$$\mathrm{G}_{\mathrm{m,sat}} = nU_{\mathrm{T}} \frac{\sqrt{K_{3,4} I_{\mathrm{tune}}}}{V_{\mathrm{cm}}}. \tag{20}$$

From the above equation, the transconductance can be adjusted by current I_{tune}. We should note that the transconductance is dependent on the square value of I_{tune} at this condition, rather than the linear scaled fashion in (16).

When the tuning current I_{tune} becomes larger, transistors M3 and M4 will enter into the moderate inversion region. We can use (8) and F is defined between 0.1 and 10 to express moderate inversion operation. By using the expression for moderate inversion region, it is hard to have a simple general form for transconductance in the transconductor. Thus, the numerical behavior is applied to simulation, and the behavior shows that the tranconductacne is in proportional to the function of current I_{tune}, and has an inverse proportion to input common-mode voltage. The analysis also predicts the THD of less than -55 dB for the current multiplier in moderate inversion region where the worst case occurs at $F = 10$. The scaled output current can be combined with the highly linear voltage-to-current conversion, and then the proposed wide tuning range linear transconductor can be achieved.

C. The Final Circuit Implementation

Fig. 4 shows the final circuit implementation of the proposed transconductor. The linear region transistors are used as the resistor R_1 and R_{1b} in Fig. 3. Unfortunately, short channel effects still occur and high order nonlinearity components degrade the linearity of the *V-I* conversion, especially for nanoscale technologies because (4) is a simplified approximate model. Thus, any distortion components should be analyzed and a new design methodology should be applied to perform a high linearity conversion. For a linear region transistor, the transistor model which takes the mobility effect into consideration is expressed as [8]

$$I_{\mathrm{D,lin}} = K_{\mathrm{lin}} \left[\frac{(V_{\mathrm{GS}} - V_{\mathrm{thn}}) V_{\mathrm{DS}} - \frac{1}{2} \alpha V_{\mathrm{DS}}^2}{1 + \theta (V_{\mathrm{GS}} - V_{\mathrm{thn}})} \right] \cdot \left\{ 1 + \frac{R_{\mathrm{eq}} K_{\mathrm{lin}}}{V_{\mathrm{DS}}} \left[\frac{(V_{\mathrm{GS}} - V_{\mathrm{thn}}) V_{\mathrm{DS}} - \frac{1}{2} \alpha V_{\mathrm{DS}}^2}{1 + \theta (V_{\mathrm{GS}} - V_{\mathrm{thn}})} \right] \right\}^{-1} \tag{21}$$

where θ is the mobility reduction coefficient and R_{eq} is the default device equivalent resistance in the linear region. In the equation, the value of α would be set to one for simplification. By giving $V_{\mathrm{GS,13}} = V_{\mathrm{GS,14}} = V_{\mathrm{DD}}$, $V_{\mathrm{DS,14}} = V_{\mathrm{cm}} + v_d/2$, and $V_{\mathrm{DS,13}} = V_{\mathrm{cm}} - v_d/2$, we can derive the voltage-to-current characteristic of MOS transistors M13 and M14. To analyze the linearity of the V_{DS} voltage against the drain current, a Taylor

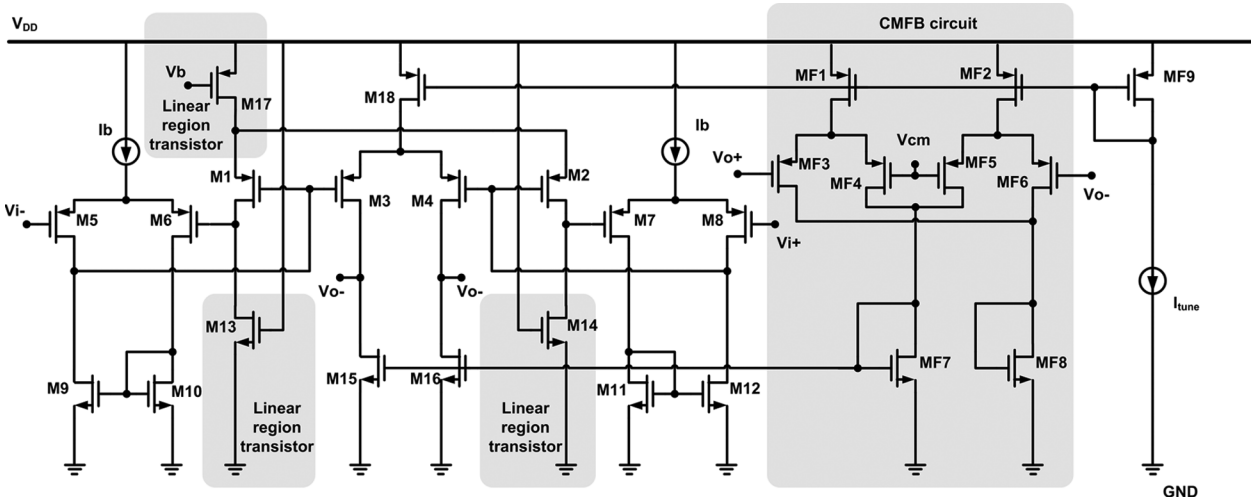

Fig. 4. Final implementation of the proposed transconductor with the CMFB circuit.

series expansion is used and then the relationship would be expressed by

$$\begin{aligned} I_{\mathrm{D,lin}} &= I_{\mathrm{D14}} - I_{\mathrm{D13}} \\ &= a_{1,\mathrm{lin}} v_d + a_{2,\mathrm{lin}} v_d^2 + a_{3,\mathrm{lin}} v_d^3 \\ &\quad + a_{4,\mathrm{lin}} v_d^4 + \cdots \end{aligned} \tag{22}$$

where $a_{1,\mathrm{lin}}$ and $a_{3,\mathrm{lin}}$ are as given in the equation at the bottom of the page.

Therefore, the third-order harmonic distortion term can be approximated to (23), shown at the bottom of the page.

Owing to the non-ideal characteristic of the linear region MOS transistor, the linearity performance would be degraded. In the equation, the first-order term defines the transconductance of the MOS resistor. The even-order harmonic terms can be cancelled out by the differential structure and thus the third-order harmonic distortion would become the dominant component. We can find that to minimize the third-order distortion term of the circuit, a small V_{cm} should be taken. In the theoretical analysis, a 20 dB increase can be achieved for a 3 dB decrease of the input common-mode voltage. However, compared with the calculated value, an 18.8 dB increase of linearity performance is obtained in simulation, and a value of smaller than -60 dB can be achieved for an optimized input common-mode voltage. In addition, since resistors R_{2a} and R_{2b} shown in Fig. 3 are used to provide a suitable bias point when tuning the transconductance, the resistance would be small in our circuit and can be replaced by a transistor in the linear region. Therefore, the transistor M17 with large aspect ratio in Fig. 4 is introduced.

Fig. 5 shows the large signal simulation with respect to the function of the differential input voltage. The tuning range of 2 μS to 110 μS corresponding to the scaled value of current I_{tune} can be obtained. The tuning ratio of more than 55 can be achieved, and it is suitable for our applications. We can find that transistors M3 and M4 would operate from weak inversion region to saturation region at large bias current, and the scaled function would become a radical expression.

The CMFB circuit, which is composed by transistors MF1 to MF8, is used for the differential structure. The aspect ratio of the transistor M18 would be twice the value of the transistors MF1 and MF2 for suitable operation. The purpose of the CMFB circuit is to balance the voltage over the entire range

$$a_{1,\mathrm{lin}} = \frac{K_{\mathrm{lin}} \left\{ R_{\mathrm{eq}} K_{\mathrm{lin}} V_{\mathrm{cm}}^2 + 4 \left(V_{\mathrm{DD}} - V_{\mathrm{th}} - V_{\mathrm{cm}} \right) \left[1 + \left(R_{\mathrm{eq}} K_{\mathrm{lin}} + \theta \right) \left(V_{\mathrm{DD}} - V_{\mathrm{th}} \right) \right] \right\}}{\left\{ 2 + R_{\mathrm{eq}} K_{\mathrm{lin}} \left[2 \left(V_{\mathrm{DD}} - V_{\mathrm{th}} \right) - V_{\mathrm{cm}} \right] + 2 (V_{\mathrm{DD}} - V_{\mathrm{th}}) \theta \right\}^2}$$

$$a_{3,\mathrm{lin}} = \frac{-4 R_{\mathrm{eq}} K_{\mathrm{lin}}^2 \left[1 + \theta \left(V_{\mathrm{DD}} - V_{\mathrm{th}} \right) \right] \left[1 + \left(R_{\mathrm{eq}} K_{\mathrm{lin}} + \theta \right) \left(V_{\mathrm{DD}} - V_{\mathrm{th}} \right) \right]}{\left\{ 2 + R_{\mathrm{eq}} K_{\mathrm{lin}} \left[2 \left(V_{\mathrm{DD}} - V_{\mathrm{th}} \right) - V_{\mathrm{cm}} \right] + 2 (V_{\mathrm{DD}} - V_{\mathrm{th}}) \theta \right\}^4}$$

$$\mathrm{HD}_3 \cong \frac{R_{\mathrm{eq}} K_{\mathrm{lin}} \left[1 + \theta \left(V_{\mathrm{DD}} - V_{\mathrm{th}} \right) \right] v_d^2}{16 \left[1 + \left(\theta + R_{\mathrm{eq}} K_{\mathrm{lin}} \right) \left(V_{\mathrm{DD}} - V_{\mathrm{th}} \right) - V_{\mathrm{cm}} \right]^2 \left(V_{\mathrm{DD}} - V_{\mathrm{th}} - V_{\mathrm{cm}} \right)} \tag{23}$$

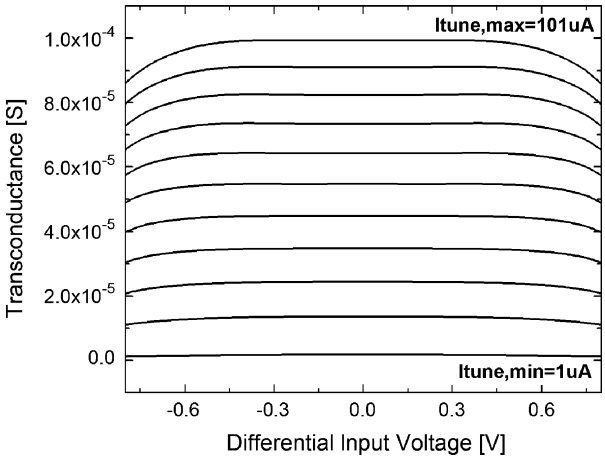

Fig. 5. Simulated G_m range of the proposed transconductor.

of the transconductor output nodes. The feedback loop forces the output common-mode voltage to the desired value, and then the linearity of the input transistors in the following transconductor circuit would be maintained. In our circuit, the maximum output swing range is defined by the maximum input signal, and the correct swing operation is confirmed by simulation. To obtain higher gain at low supply voltage, large sizes of transistors MF3 to MF6 are selected and these transistors operate in the weak inversion region. However, the CMFB gain would be reduced at large input swing. When the gain of the CMFB circuit is reduced, it will lead to an offset voltage to the input node of next stage and then affect the linearity of voltage-to-current conversion. Thus, the distortion would become a little worse than expected when large signal appears within the filter cutoff frequency. This effect can be recovered by using extra resistors to replace differential pair for averaging differential signals.

D. Nonidealities in the Proposed Circuit

The thermal noise is a combination of the noise generated by the voltage-to-current conversion core and the current multiplier. In order to obtain the noise performance, a noise model validated in the weak to strong inversion region is required. As the model in [9] is introduced, the input-referred thermal noise is as shown in (24) at the bottom of the page, where k is the Boltzmann constant and δ is the noise parameter at saturation, subthreshold, and linear regions. From the equation, the noise contribution can be divided into two parts. One is contributed by the feedback amplifier, which is composed by transistors M5 to M12, and the other is the devices in the negative feedback network. To reduce the noise of the feedback amplifier, we can increase the transconductance of input transistors M5 to M8. For the differential input stage with a biased current source, the transconductance is proportional to the current and thus it results in a tradeoff between the noise performance and the power consumption. In this design, larger aspect ratio would be used by taking the gate overdrive voltage and the voltage headroom of the current source into consideration. To reduce the noise contributed in the negative feedback network, we need to maintain large amplifier gain and increase transconductance of transistors M13 and M14. Usually, the amplifier gain is large enough, so the transconductance of transistors M13 and M14 dominates the noise contribution. Transistors M13 and M14 are operated in the linear region, and the transconductance can be increased by giving a large transistor aspect ratio and gate overdrive voltage. We should note that to achieve a larger transconductance, the bias current would become larger to consume more power. Thus, a small input common-mode voltage can be used to maintain the bias current while the overall transconductance derived from (16) and (20) tends to increase. In this circuit, even the high linearity current multiplier would contribute extra noise in the wide tuning transconductor, it is fortunate that half of the multiplier is combined with the voltage-to-current core, and thus only transistors M1 to M4 are added for current scaling. This condition reduces the contributed noise from the current multiplier. In our simulation, a 3 dB increase of the aspect ratio could result in about 3 dB increase of the noise performance.

The impact of flicker noise should also be taken into consideration. In this design, the device sizes of the transistors which determine the flicker noise are increased to reduce the flicker noise, and the transistor length is designed to ten times of the minimal size used in the process. The larger size of the device also decreases the effect of channel length modulation and increase the output impedance. We should note that the large device size would induce more parasitic capacitance, and thus not only the unity-gain frequency is decreased but also the voltage-to-current conversion linearity at high speed is degraded. Since the flicker noise contributes only part of the noise in our design, the tradeoff between the noise and speed should be taken into consideration.

The mismatch is caused by the random variation of the process in physical quantities of identically designed devices. The random mismatch comes from the fabrication tolerances, and it produces the even-order distortion terms in differential structure. In the circuit, the linearity of the voltage-to-current conversion core is not sensitive to the mismatch owing to

$$\overline{V_{\mathrm{n,in}}^2} = \frac{4kT}{gm_{13,14}^2}\left(\frac{\delta_{3,4}gm_{1,2}^2}{gm_{3,4}} + \delta_{1,2}gm_{1,2} + \delta_{13,14}gm_{13,14}\right)\left[\frac{gm_{13,14} + gm_{5,6,7,8}\left(ro_{5,6,7,8}||ro_{9,10,11,12}\right)gm_{1,2}}{gm_{5,6,7,8}\left(ro_{5,6,7,8}||ro_{9,10,11,12}\right)gm_{1,2}}\right]^2 + \frac{8kT}{gm_{5,6,7,8}^2}\left(\delta_{5,6,7,8}gm_{5,6,7,8} + \delta_{9,10,11,12}gm_{9,10,11,12}\right) \quad (24)$$

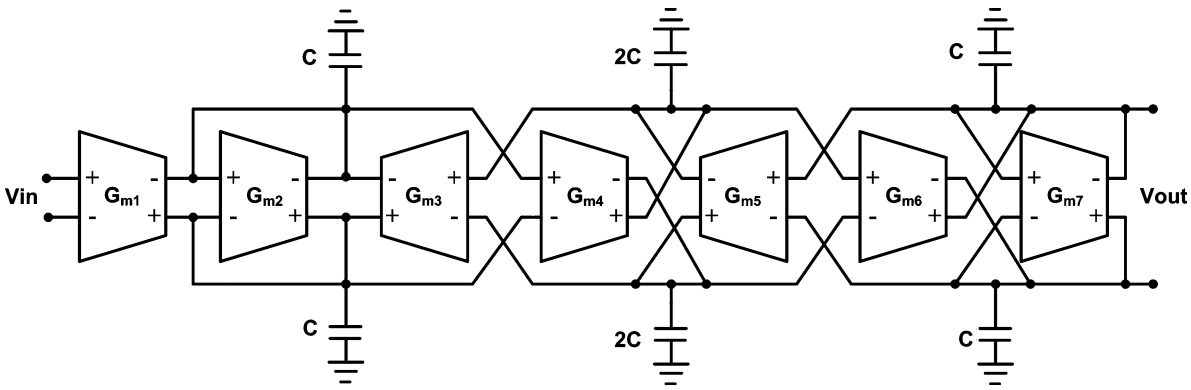

Fig. 6. Block diagram of the third-order Butterworth filter.

the feedback topology. The mismatch of the input transistor dimensions and threshold voltage will just produce a DC offset voltage at the resistor terminals. Thus, the converted output current would behave only first-order fashion to the input voltage. When the linear region transistors are introduced, the offset voltage will induce a slight variation of transconductance as the short channel effect is simply neglected, and then the linearity performance can be hold. However, when the mismatch between linear region transistors M13 and M14 occurs, the voltage-to-current conversion would provide second-order distortion and degrade the linearity performance. In addition to the voltage-to-current conversion core, mismatch problem would get a higher nonlinear effect on the current multiplier. Simulation results show an increase of 3 dB in the second harmonic distortion term for a 2% mismatch of transistors M1 and M2. Thus, large transistor length is suitable for the multiplier in our design. This condition also helps the multiplier to achieve a higher linearity operation since it tends to work under the weak inversion operation.

III. Filter Architecture

From the demonstration of the passive ladder prototype, the third-order Butterworth low-pass G_m–C filter, consisting of seven identical transconductors, is used as shown in Fig. 6.

In this low-pass filter design, the time constant of the filter is determined only by the G_m/C ratio, where G_m is the transconductance and C is the loading capacitance. The loading capacitor is realized from metal–insulator–metal structure. The transconductance would be programmable and has a nominal value of 50 μS. The -6 dB gain loss of the passive prototype has been compensated at the input of the filter by increasing the transconductance by a factor of two. The other transconductors would be set to the same value so that frequency tuning can be achieved from a single source. Dynamic range scaling was applied, and we have made sure the output swing of each transconductor is equal to the maximum range. Since the filter is synthesized by Butterworth ladder prototype, which behaves all-pole characteristic, the quality factor is equal to 1. Therefore, no peaking will appear near the cutoff frequency. The cutoff frequency of the G_m–C filter is tuned by changing the bias current $I_{\rm tune}$ in our proposed transconductor. The automatic frequency tuning circuitry has not been investigated for this filter. However, the tuning circuitry can be developed with digitally controlled circuits in a system on chip solution by choosing a number of current sources for multi-mode selection. In addition, Q tuning circuits are not considered here with the intrinsic quality of the low Q structure.

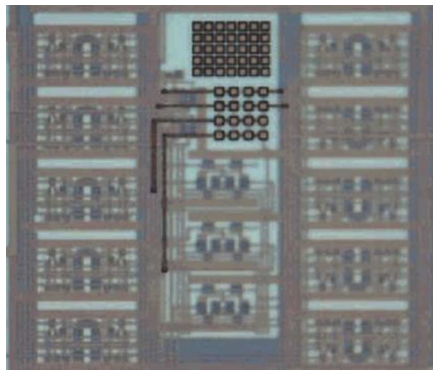

Fig. 7. Chip micrograph.

The output common-mode voltage of each block would be fixed by three CMFB circuits in the filter. The CMFB circuit is shown in Fig. 4. The bias current of the CMFB circuit should be changed according to the $I_{\rm tune}$ value, and then the performance of the common-mode control topology can be maintained.

IV. Measurement Results

The transconductor and the filter were designed in the TSMC 0.18 μm CMOS process. The chip micrograph is shown in Fig. 7 with the active area less than 0.23 mm^2.

The transconductor has been examined in the frequency domain to obtain its linearity performance. Fig. 8 shows the spectrum of the transconductor through inter-modulation characterization by applying two-tone signals near 20 MHz with the amplitude of 0.6 $V_{\rm pp}$ voltage. In this measurement, the transconductance is 100 μS and the loading resistor is 50 ohm. The result shows the third-order inter-modulation distortion (IM3) is around -54 dB. The measured performance is smaller than the expected value from simulation. This is owing to the deviation of the feedback amplifier gain and the effect of parasitic capacitance at high frequency.

Fig. 9 illustrates the filter frequency response at 1.2 V supply voltage. We should note that the magnitude is normalized owing

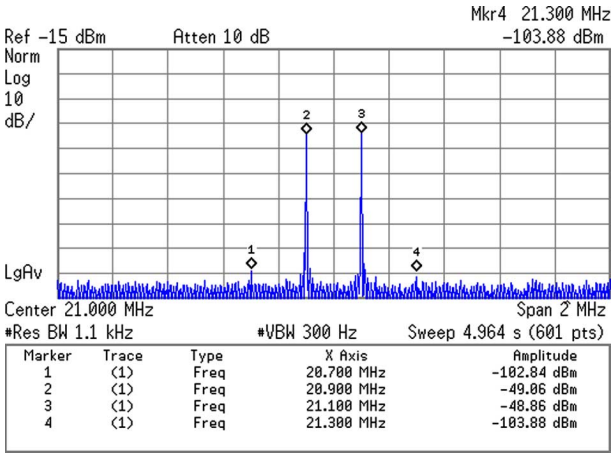

Fig. 8. Two-tone test of the proposed transconductor.

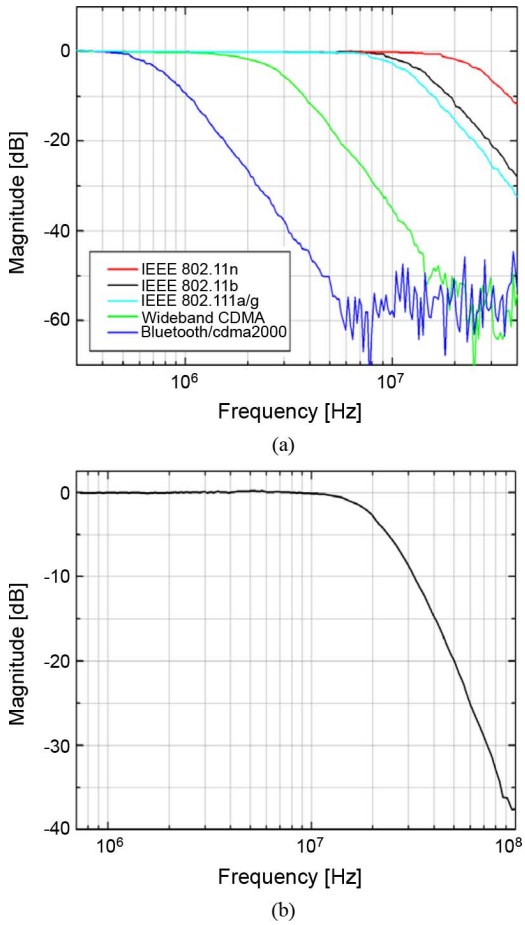

Fig. 9. (a) Measured frequency responses of the proposed multi-mode filter. (b) Frequency response of IEEE 802.11 mode with an extension to 100 MHz.

to the use of the output buffer. The cutoff frequency can be tuned from 500 kHz to 20 MHz, and the range covers the specifications of Bluetooth, cdma2000, Wideband CDMA, and IEEE 802.11a/b/g/n wireless LANs. The IM3 test yield the IIP3 results of 22.3 dBm, 21.8 dBm, 20.5 dBm, 20.2 dBm, and 19 dBm for each wireless specification, respectively.

The measured input-referred noise spectrum density at 70 °C is summarized in Table I. Since the cutoff frequency of the

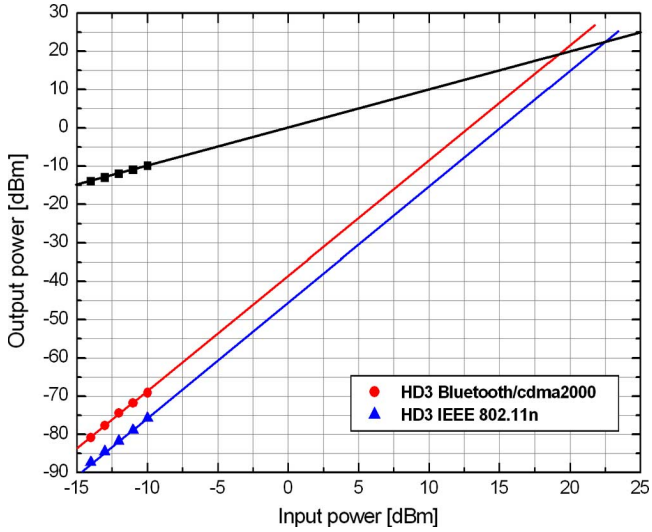

Fig. 10. In-band IIP3 between Bluetooth/cdma2000 and IEEE 802.11n setting.

G_m–C filter is programmed by adjusting the transconductance, the filter can be considered as a constant-capacitance network. In [10], the integrated output thermal noise is shown to be independent to the frequency scaling factor from analysis, and the dynamic range is almost the same over the tuning range. We can find that the measured input-referred noise density value in Table I has an inverse proportion factor rather than a square-rooted inverse proportion factor to the scaled frequency. The deviation of the expected value is owing to the circuit flicker noise at low frequency and extra circuit on PCB board at high frequency. The measured noise gives an 80 dB dynamic range at IEEE 802.11 mode for −40 dB IM3.

The DC offset decreases the dynamic signal swing, and then reduce the gain and linearity performance of the receiver. The offset cancellation loop/algorithm is usually used to compensate DC values while still maintaining the well performance of the system. The measured input second-order intercept point (IIP2), which can stand for the second-order distortion performance for every wireless mode, is also shown. Moreover, the linearity performance of out-of-band blocking interferences is measured. The value is described by out-of-band IIP3 in Table I. The IIP3 plot for highest and lowest cutoff frequency setting is shown in Fig. 10.

Table II summarizes the filter type and detailed information for several filters reported in recent years. A figure of merit (FOM), which is independent to the tuning ratio, is used to evaluate the filter performance [11]

$$\mathrm{FOM} = \frac{(P_{\mathrm{tot}}/N)}{f_{\mathrm{c}} \times \mathrm{SFDR} \times N^{4/3}} \tag{25}$$

where P_{tot} is the total power of the filter, N is the number of poles, f_c is the cutoff-frequency, $\mathrm{SFDR}(N)^{4/3}$ is the normalized spurious-free dynamic range, with

$$\mathrm{SFDR} = \left(\frac{\mathrm{IIP3}}{P_n}\right)^{2/3} \tag{26}$$

where P_n is the input-referred noise power. In this paper, the FOM of this filter is plotted versus the supply in Fig. 11 and

TABLE I
PERFORMANCE SUMMARY OF THIS WORK

Technology	0.18-μm CMOS				
Supply	1.2-V				
Filter Prototype	3-rd order Buttorworth Lowpass Filter				
Tuning Range	500 kHz – 20 MHz				
Application	Bluetooth/ cdma2000	Wideband CDMA	IEEE 802.11 a/g	IEEE 802.11 b	IEEE 802.11 n
IIP3	22.3 dBm	21.8 dBm	20.5 dBm	20.2 dBm	19 dBm
IIP2	40 dBm	39.3 dBm	-	-	30.8 dBm
Out-of-band IIP3	17.5 dBm	17.3 dBm	-	-	13 dBm
Power	4.1 mW	4.7 mW	7.1 mW	8.2 mW	11.1 mW
Input-referred noise density	425nV/√Hz	128nV/√Hz	29nV/√Hz	24nV/√Hz	12nV/√Hz

TABLE II
COMPARISON WITH PREVIOUSLY REPORTED WORKS

Reference		[12] ESSCIRC 2003	[13] ESSCIRC 2004	[14] JSSC 2005	[15] JSSC 2006	[11] JSSC 2007	This Work
Technology		0.18μ CMOS	0.18μ CMOS	0.25μ BiCMOS	0.13μ CMOS	0.13μ CMOS	0.18μ CMOS
Area		0.83mm^2	0.125mm^2	0.25 mm^2	0.45mm^2	0.52 mm^2	0.23mm^2
Type		G_m-C	G_m-C	G_m-C	Active-G_m-RC	Active-RC	G_m-C
Supply voltage		1.8	1.8	2.5	1.2	1.2	1.2
Filter order		6	4	3	4	2-6	3
-3dB frequency		1.5MHz-12MHz	0.5MHz-12MHz	50kHz-2.2MHz	2.11MHz-11 MHz	350kHz-23.5MHz	500kHz-20MHz
Tuning ratio		8	24	40	5.5	67	40
Application		W-CDMA/ IEEE 802.11a/b/g	BlueTooth /W-CDMA/ IEEE 802.11a/b/g/	GSM /BlueTooth /W-CDMA/ CDMA2000	UMTS/ IEEE 802.11a/b/g	Software defined radio	BlueTooth/ cdma2000/W-CDMA /IEEE 802.11a/b/g/n
IIP3	**Min**	7.2dBm	9.4dBm	22dBm	21dBm	20dbm	19 dBm
	Max	9.3dBm	11.1dBm	28dBm		-	22.3 dBm
Power	**Min**	10mW	1.1mW	2.5mW	3.4mW	0.72mW	4.1mW
	Max	15mW	4.5mW	7.3mW	14.2mW	21.6mW	11.1mW

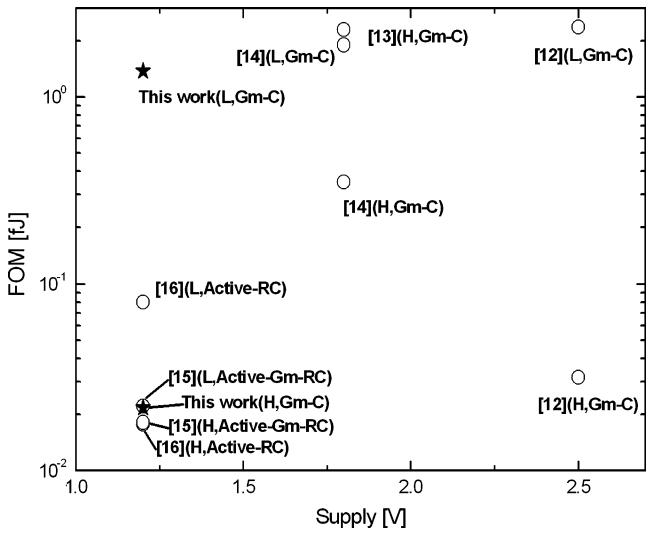

Fig. 11. FOM versus supply comparison with previously published works.

favorably compared to other published works, where some of them are not G_m–C prototypes. In this figure, symbols L and H denote the lowest and highest frequency for each filter, respectively.

V. CONCLUSION

The CMOS implementation of a third-order Butterworth low-pass G_m–C filter for multi-mode applications is presented. The transconductor is designed by the combination of a voltage-to-current circuit and a current multiplier to achieve both the high linearity and wide tuning range simultaneously. Through the use of the wide tuning range linear transconductor as a building block, the cutoff frequency of the channel selection filter can be widely tuned from 500 kHz to 20 MHz, which meets the specifications of Bluetooth, cdma2000, Wideband CDMA, and IEEE 802.11a/b/g/n wireless LANs under direct-conversion architecture. The theoretical analysis of the operation and the measurement results are provided to demonstrate the validity of the filter.

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