國 立 交 通 大 學

電子工程研究所

碩 士 論 文

應用於 Serial ATA 6Gbps
之可程式化展頻時脈產生器

A Programmable Spread Spectrum Clock Generator for Serial ATA 6Gbps

指導教授：周 世 傑　博士

研 究 生：莊 誌 華

中　華　民　國　95　年　7　月

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指導教授：周世傑　　Advisor：Prof. Shyh-Jye Jou

研 究 生：莊誌華　　Student：Chih-Hua Chuang

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應用於 Serial ATA 6Gbps 之可程式化展頻時脈產生器

學生：莊誌華　　指導教授：周世傑

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摘　　要

現代的電路系統操作速度越來越快，其所控制時間的電路也越來越重要。因此，鎖相迴路在所有高速的系統中扮演一個非常重要的角色。例如：頻率合成器、倍頻器、資料回復電路等等。因為這些系統需要一個準確的時脈，一個低抖動的鎖相迴路是我們所設計的一個重點。

且隨著晶片操作速度越來越快，時脈信號所造成的高頻電磁雜訊干擾(Electro-Magnetic Interference, EMI)通常會影響到其他電路的操作。且當操作速度越快時，這種問題就越嚴重。傳統的解決方法是將電磁雜訊干擾加以屏蔽，或是控制時脈信號的上升速度，但是缺點是昂貴的成本與龐大的體積。較先進的解決方法是直接在晶片上降低電磁雜訊干擾，以達到低成本與高彈性空間。改變時脈信號的中心頻率是最常被採用的方法。這種方法被稱為展頻時脈技術(Spread Spectrum Clocking)，因為時脈信號的頻譜被展開成較寬的頻帶。

在本論文中，我們先簡單的介紹了鎖相迴路及展頻時脈產生器的基本觀念。並在第五章提出了如何降低電壓抖動的方法以及可程式化展頻時脈產生器的架構。我們的展頻時脈產生器是以調變多重相位的方法來達到展頻的效果並

且符合 Serial-ATA 6Gbps 的規格。可程式化展頻時脈產生器可依系統的需求，選擇對 10 個輸出相位或是 20 個輸出相位作展頻。各有各的優缺點，接下來會詳細的討論並驗證之。

本論文包含了鎖相迴路及展頻時脈產生器的設計、模擬、和製作，並且附上鎖相迴路在 0.18 毫米互補式金氧半的製程實現後的量測結果，證明我們所提出的設計在實現與應用上是可行，並且符合 Serial-ATA 6Gbps 的規格。

A Programmable Spread Spectrum Clock Generator for Serial ATA 6Gbps

student：Chih-Hua Chuang　　Advisors：Dr. Shyh-Jye Jou

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ABSTRACT

As chips work at faster operation speed, the timing issue becomes more and more important. So the PLL plays an important role in all high-speed systems, such as: frequency synthesizer, clock multiplier, Clock and Data Recovery (CDR) circuit, and clock de-skew application. Consequently, a low-jitter PLL is important because these systems require a stringent timing specification.

Due to the operation speed is becoming faster and faster, many higher order harmonics of the signal are generated. These signals often generate Electric-Magnetic Interference (EMI) that affects the operation of other equipments. When the operation speed is higher, the EMI problem is more severe.

The conventional techniques to reduce EMI tend to enclose or reduce the amount of the generated radiation, such as shield cables and coaxial wires, but they are usually costly and bulky. Modern EMI reduction is done on-chip without using

heavy shielding materials to the goal of low-cost and flexibility.

Altering the center frequency of internal clocks is a widely adopted EMI reduction technique. The technique is called Spread Spectrum Clocking (SSC) because the spectrum of the clock is spread over a broader range. It also offers the best immunity with respect to manufacturing process variation. Serial-ATA (SATA) specification defines an EMI reduction method using SSC.

A low-jitter programmable spread-spectrum clock generator using switching phases and the modified ΔΣ modulator is presented in this thesis. The circuits are proposed, simulated, and implemented in a standard 0.18um CMOS technology. Our low jitter PLL is achieved through VCO with low K_{VCO} by using medium-threshold voltage PMOS and passive resistance. The spectrum in the clock generator with modulation on phases can be spread by 10 phases or 20 phases depending on the system's requirement, such as power saving or low jitter in time domain. Besides, the programmable spread spectrum generator is also fit with the specification of Serial-ATA 6Gbps. Finally, the experiment results show that the architecture achieves spread spectrum function as expectations.

誌　　謝

真的很開心，終於到了論文完成的這一天。同樣不免俗的我必須抒發我心裡的感激。我必須承認，我要感謝的人太多了。首先要感謝的是引領我碩士生涯入門的李崇仁教授，教導我研究的態度。接下來要感謝的是我的論文指導教授周世傑老師，在這段時間不斷的鞭策我們，並且為我們定下每一時期的短程目標與終極目標，才能使我們能準時畢業。

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這麼長的歲月，要感謝的人當然不只這些。所有的授課老師、學長姐、同學、學弟妹們，我也要在這裡說聲謝謝你們大家，因為你們大家的牽成，才有今天的我，謝謝你們。

莊誌華

國立交通大學

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Introduction of Timing Module for Serial Link

Recently, the advance in IC fabrication technology along with aggressive circuit design have led to an exponential growth of the speed and integration levels of digital IC's. However, these advancements have led to some chips being limited by the chip-to-chip data communication bandwidth. This limitation has motivated research in the area of high-speed link that interconnect systems. So that the increasing demands for the data bandwidth in network has driven the development of high-speed and low-cost serial link technology. The serial link technology can lower the numbers of transmission lines to decrease volumes and cost, and decrease the EMI effect. The population applications are such as USB2.0, IEEE-1394b, RAM Bus, Serial ATA, and PCI express.

Fig. 1.1 shows the transmitter architecture of 6Gbps for Serial ATA [1]. The transmitter is composed of a phase-locked loop, PISO, buffer, driver and pre-emphasis. High speed parallel to serial data conversion is achieved by means of time-division 5 to 1 multiplexer controlled by a multi-phases PLL which oscillates in 1.2GHz. Finally, the serial data of 6Gbps is sent to the receiver through the channel. The REG and CMUX need 5 phases of the 1.2GHz clock respectively. We use the different 5 phases

to control the REG and CMUX in order to prevent influencing each other. As a result, our goal is to design a low-jitter 5-stages ring oscillators and 10-phases clocking for a 6Gbps serial link transmitter.

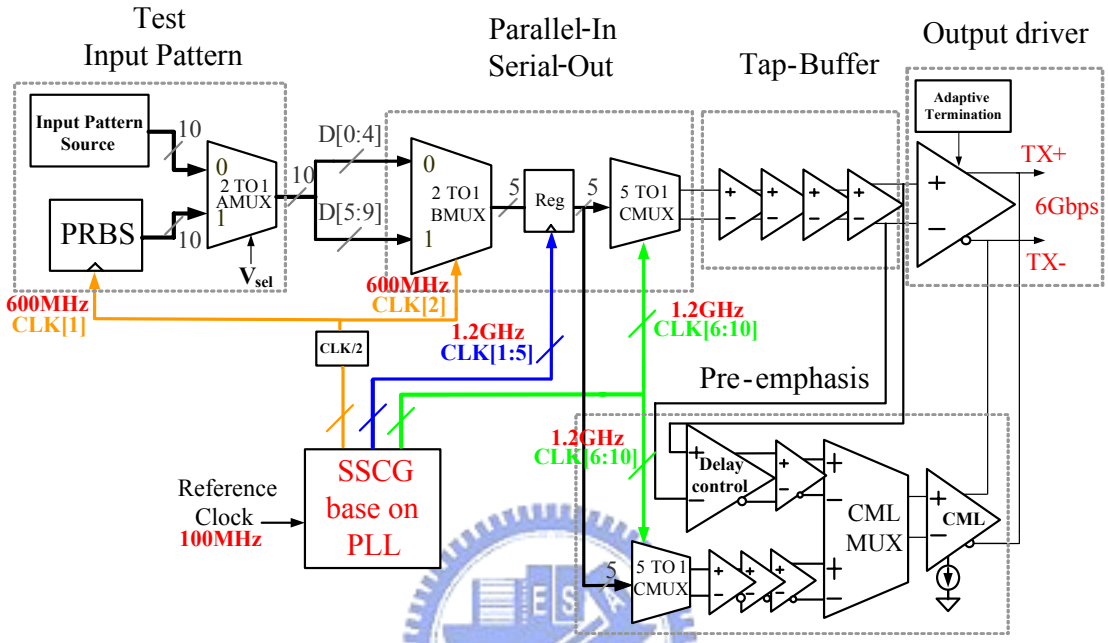


Fig. 1.1 Architecture of Serial-ATA transmitter with PLL

1.2 Motivation

As chips work at faster operation speed, the timing issue becomes more and more important. PLL (phase-locked loop) can generate a clean and stable clock to work as timing source, so the PLL plays an important role in all high-speed systems, because these systems require a stringent timing specification.

PLL is already widely used in SoC designs. It is often applied to communication applications, such as: frequency synthesizer, clock multiplier, Clock and Data Recovery (CDR) circuit, and clock de-skew application. The design of PLL is a trade-off among jitter performance, frequency / phase resolution, lock-in time, area cost, power consumption, circuit complexity and design time. So how to design a suitable PLL for system requirement is the most important issue in the system timing.

There are two of VCO: LC tank and ring oscillator. The things we are concerned in choosing the VCO structure are the low phase noise, sufficient tuning range and acceptable power consumption. LC tank oscillators are widely used in the wireless communication applications due to their ease of achieving high frequency with power consumption [2], but its disadvantage is difficult to implement a good inductor and frequency running range small. So the performance of the frequency synthesizer is sensitive to the process variations. However, ring oscillators are much easier implementing high quality IC. It also has wider tuning range and occupies smaller area than a LC tank. It can also easily provide multiple phases and this is the main reason we choose the ring oscillator in our VCO.

Besides, due to the operation speed is becoming faster and faster, many higher order harmonics of the signal are generated. These signals often generate Electric-Magnetic Interference (EMI) that affects the operation of other equipments. In a portable device, the high-speed interfaces between peripheral storages and the other signal processing units are the main noise sources. When the operation speed is higher, the EMI problem is more severe.

There are many methods to diminish EMI; and all have positive and negative effects on the products. Among these methods, spread spectrum is the simplest and the most efficient one. It also offers the best immunity with respect to manufacturing process variation.

Spread spectrum scheme is to slightly modulate a narrowband clock's signal frequency, and spread it over a wider bandwidth: In this way, energy peaks at specific frequencies are diminished. This approach reduces the EMI of fundamental clock frequency, as well as the higher order harmonic components. Therefore the EMI radiation of the whole system is reduced.

As external storage devices are widely used, high-speed serial links connecting hosts and external devices are becoming popular. Serial AT Attachment (SATA) is one of the most promising technologies providing large bandwidth up to 6Gbps (in SATAIII). SATA specification defines an EMI reduction method using spread-spectrum clocking (SSC), which reduces the peak EMI emission by spreading carrier frequency. EMI reduction using SSC has been studied and explored in several papers. However, it is more important to consider the time-domain impact of SSC in addition to the EMI peak reduction since the major concern in serial data transmission is signal integrity in the time domain. A low-jitter programmable spread-spectrum clock generator using switching phases and the ΔΣ modulator is presented in this thesis.

Low jitter PLL is achieved through VCO with low K_{VCO} by using medium-threshold voltage PMOS and passive resistance. The spectrum in the clock generator can be spread by 10 phases or 20 phases depending on the requirement, such as power saving or low jitter in time domain. Our SSCG for Serial ATA Specification is down spread 5000 ppm with a triangular waveform of modulation frequency 30~33KHz. The proposed circuit is fabricated in a 0.18-um CMOS process. The non-spread spectrum clocking has a peak to peak jitter of 3.1ps and the maximum EMI reduction is -17.8dB in 20 phases spread spectrum mode which the power dissipation is only 28mw.

1.3 Thesis Organization

This thesis will introduce the basic theorem of the low jitter PLL and programmable spread spectrum clocking. Besides, the circuit implementation in PLL and SSCG is also explained in detail. The thesis is organized as follows:

Chapter 2 begins with the brief introduction of the charge-pump PLL. We describe the way to analyze PLL in the linear model. Then we discuss the open loop transfer function as well as closed loop transfer function.

In Chapter 3, we describe the principle of SSCG using switching phase scheme. The most important design is to let the ΣΔ modulator control the jumping phases and make a spreading spectrum clock.

Chapter 4 begins with the introduction to EMI problem and several solutions used for the EMI reduction. The most significant part explains the concept of spread spectrum using frequency modulation technology. Other parameters, like modulation profile and modulation frequency and timing impacts, are also discussed.

In Chapter 5, a low jitter programmable spread spectrum clock generator using switching phase is presented. The SSCG is fabricated in 0.18μm CMOS 1P6M process. We first introduce the architecture of the proposed programmable spread spectrum clock generator and the behavior simulation in MATLAB. The following sections describe the implementations and simulations in Hspice of each building block. Finally, we show the measurement setup and the measurement results.

Chapter 6 gives conclusions to our work. Suggestions for future works are recommended at the ending of this thesis

Chapter 2

Principles of Phase-Locked Loop

2.1 Introduction to PLL

Due to the demand for higher performance and lower cost in electronic systems, and the advance of integrated-circuit (IC) technologies in terms of speed and complexity, Phase-locked loop (PLL) become more and more popular in the last twenty years. PLL plays an important role in radio, telecommunications, wireless systems, and computers, especially for the serial link transceiver. Because whether parallel-to-serial data conversion in the transmitter or serial-to-parallel data conversion in the receiver, the generating phases of PLL are needed.

A PLL is a feedback circuit that causes a particular system to track with another reference signal. In other words, a PLL is a circuit synchronizing an output signal with a reference in frequency as well as in phase. In the locked state, the phase error between the oscillator's output signal and the reference signal is zero, or remains constant.

If a phase error builds up, the feedback system of PLL will act on the oscillator such that the phase error will be reduced to a minimum. Finally, the phase of the output signal is again locked to the phase of the input signal. That is why we call it as phase-locked loop.

The main applications of PLL are as follows:

1. Clock recovery: Some data streams, especially high-speed serial data streams, (such as the raw stream of data from the magnetic head of a disk drive) are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL. In order for this scheme to work, the data stream must have a transition frequently enough to correct any drift in the PLL's oscillator. Typically, some sort of redundant encoding is used; 8B10B is very common.

2. Deskewing: If a clock is sent in parallel with data, that clock can be used to sample the data. Because the clock must be received and amplified before it can drive the flip-flops which sample the data, there will be a finite, and process-, temperature-, and voltage-dependent delay between the detected clock edge and the received data window. This delay limits the frequency at which data can be sent. One way of eliminating this delay is to include a de-skew PLL on the receive side, so that the clock at each data flip-flop is phase-matched to the received clock.

3. Clock generation: Most electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple gigahertz and the reference crystal is just tens or hundreds of megahertz.

4. Spread spectrum: All electronic systems emit some unwanted radio frequency energy. Various regulatory agencies (such as the FCC in the United States) put limits on this emitted energy and any interference caused by it. The emitted noise

generally appears at sharp spectral peaks (usually at the operating frequency of the device, and a few harmonics). A system designer can use a spread-spectrum PLL to reduce interference with high-Q receivers by spreading the energy over a larger portion of the spectrum. For example, by changing the operating frequency up and down by a small amount (about 1%), a device running at hundreds of megahertz can spread its interference evenly over a few megahertz of spectrum, which drastically reduces the amount of noise seen by FM receivers which have a bandwidth of tens of kilohertz.

2.2 Brief History

The very first phase-locked loops were implemented as early as 1932 by Bellescize; this French engineer is considered the inventor of "coherent communication." However, The PLL found industrial applications only when it became available as an IC. The first PLL ICs appeared around 1965 and were called linear PLL (LPLL)[3], because each block is analog device. An analog multiplier was used as the phase detector and the loop filter was built from a passive or active RC filter. In the following years the first digital PLL (DPLL) was invented in 1970. It is in effect a hybrid device. The only digital circuit is phase detector, e.g., made from an EXOR gate or a JK-flipflop. But the remaining blocks were still analog. A few years latter, the "all-digital" PLL (ADPLL) was invented. Each block is digital. The loop filter is from Up/Down counter. The VCO is from DCO. Finally, software PLL was presented. The PLL functions are performed by a computer program rather than a piece of specialized hardware.

2.3 Basic Operations in PLL

A basic PLL consist of five parts (Fig. 2.1): phase/frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO) and frequency divider. The interpolator is not always needed unless you want to create more phases.

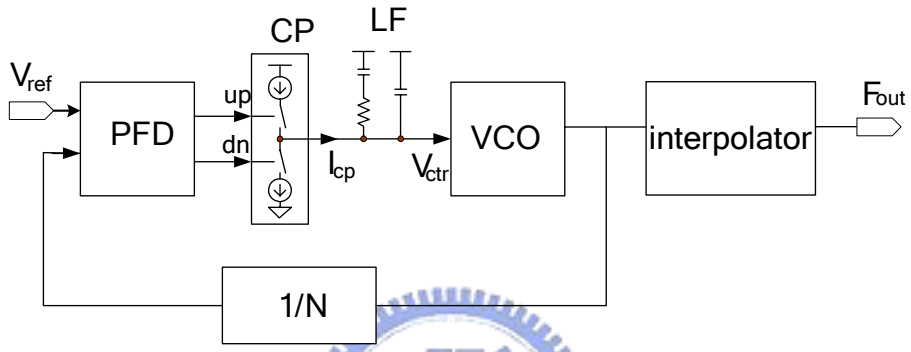


Fig. 2.1 The block diagram of PLL

The operation principle of the PLL is as follows: the PFD compares the frequency and phase errors between the reference signal and the feedback signal from the output of the divider, thus producing digital up or down signals to control the CP.

If the phase from the divider lags that of the reference, the phase detector causes the charge pump to change the control voltage. The CP would change the single digital signals to the corresponding differential analog voltage signals so that the oscillator speeds up. Likewise, if the phase leads ahead the reference, the phase detector causes the charge pump to change the control voltage to slow down the oscillator. The low-pass filter smoothes out the abrupt control inputs from the charge pump so that the LP filters out the higher frequencies of the voltage signals and preserve the DC components. The pass DC voltage is used to control the frequency of VCO. The output signal of VCO would pass through the frequency divider and be fed

into the PFD again. Therefore the PLL will continuously compare the two signal's frequencies and phases until they are equal. We called that it is locked.

Although the operation of acquisition is nonlinear, the operation close to be locked is almost linear. So we will derive the linear model of each block first.

2.3.1 Phase/Frequency Detector and Charge Pump

The traditional phase detector compares the phases of the reference signal and the feedback signal. But it suffers from a severe problem: the acquisition range is on the order of w_{LPF}. In other words, the loop locks only if the difference between w_{ref} and w_{out} is less than roughly w_{LPF}.

In order to solve the acquisition problem, modern PLL incorporate frequency detection in addition to phase detection. At the beginning, the FD makes w_{out} toward w_{ref} while the PD remains disable. When w_{out} is closed to the w_{ref}, the PD becomes the dominant part to compare the phases. Such a scheme increases the acquisition range to the tuning range of the VCO.

For periodic signals, we can combine the two loops by creating a circuit that can detect both phase and frequency difference. We call it as tri-state phase/frequency detector (PFD), by using two edge-triggered D type flipflops and a logic gate, as illustrated in Fig. 2.2. If Q_A=Q_B=0, and REF goes high, Q_A rises. Next, if this event is followed by a rising transition on DIV, Q_B goes high and the AND gate resets both flip-flops and vice versa. Fig. 2.3 shows the timing diagram of tri-state PFD and Fig. 2.4 shows its state diagram.

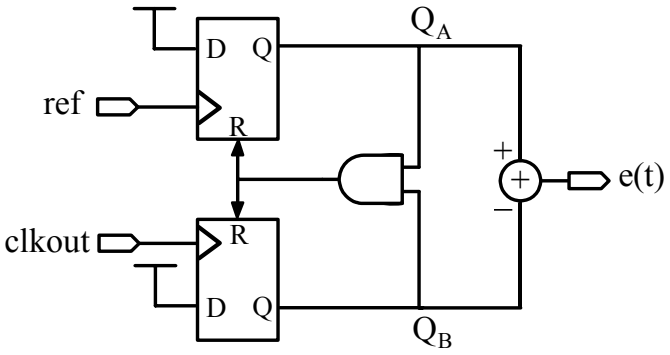


Fig. 2.2 Architecture of tri-state PFD

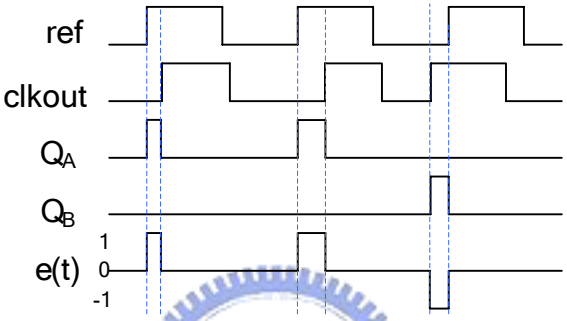


Fig. 2.3 Timing diagram of tri-state PFD

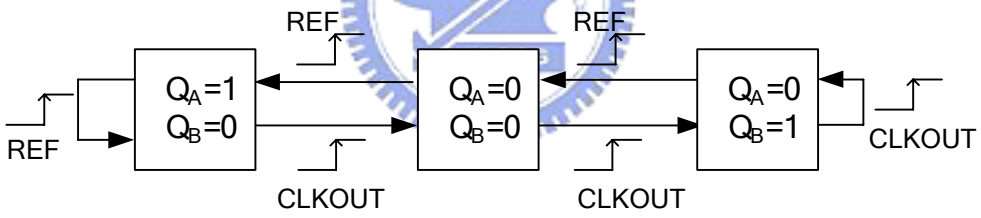


Fig. 2.4 State diagram for PFD

We define the output as the average value of e(t), which is the difference of Q_A and Q_B, and the input as the phase error between REF and CLKOUT. We derive the tri-state PFD characteristic, as shown in Fig. 2.5. In addition to its wide detection range of $\pm 2\pi$, we note that phase error characteristic is asymmetric about zero phase. Such a characteristic allows positive frequency differences to be distinguished from negative frequency differences. So the average value is now positive or negative according to the sign of frequency offset and the PLL will always relock.

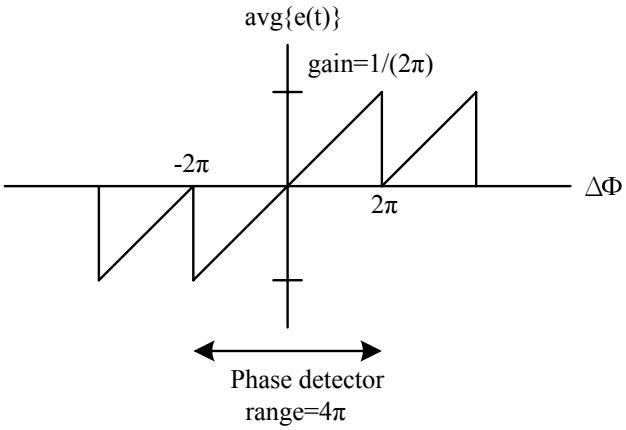


Fig. 2.5 Tri-state PFD characteristic

Another PFD structure is XOR-based PFD. as illustrated in Fig. 2.6. If REF=CLKOUT=0, and REF goes high, REF/2 rises. Next, if this event is followed by a rising transition on CLKOUT, CLKOUT/2 goes high and the XOR gate detects the difference of the two signals and vice versa. Fig. 2.7 shows the timing diagram of XOR-based PFD.

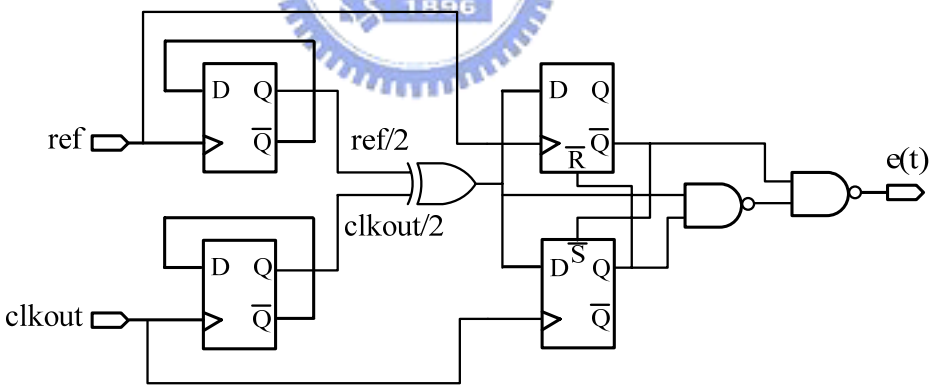


Fig. 2.6 Architecture of tri-state PFD

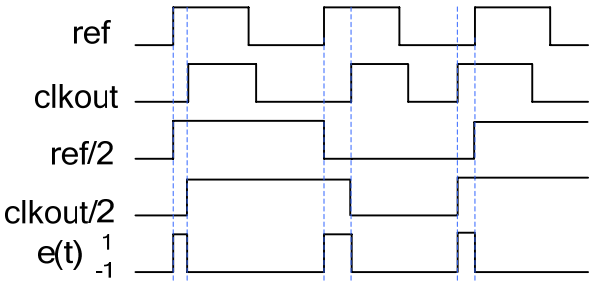


Fig. 2.7 Timing diagram of XOR-based PFD

Fig. 2.8 is the XOR-based PFD characteristic. But Its detection range only 2π, we also note that phase error characteristic is asymmetric about zero phase. Average value of phase error is positive or negative during cycle slipping depending on sign of frequency error and the PLL will always relock.

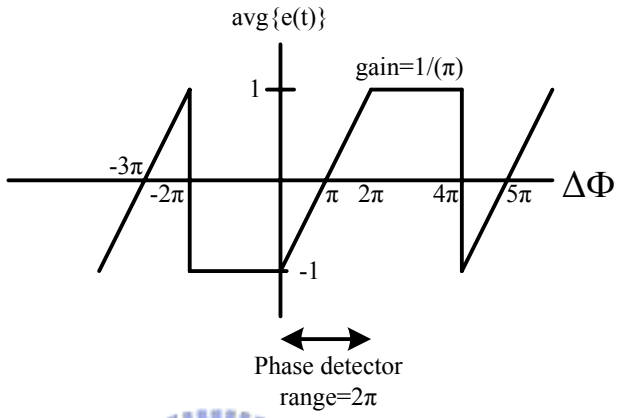


Fig. 2.8 XOR-based PFD characteristic

The Charge Pump (CP) is an analog circuit that converts the Q_A and Q_B signals (in the tri-state PFD) to the corresponding variation in the control voltage of the VCO. A simple model is as shown in Fig. 2.9. When Q_A is low and Q_B is high, the switch S_1 is off and S_2 is on. Then the I_{DN} discharges the output capacitor and the voltage falls. On the contrary, if Q_A is high and Q_B is low, the switch S_1 is on and S_2 is off. Then the I_{UP} charges the output capacitor and the voltage rises. If both Q_A and Q_B are low, both switches are off and the output voltage is floating. If both Q_A and Q_B are high, the both switches are on. In the ideal situation, I_{UP} is equal to I_{DN}, so the output voltage remains unchanged.

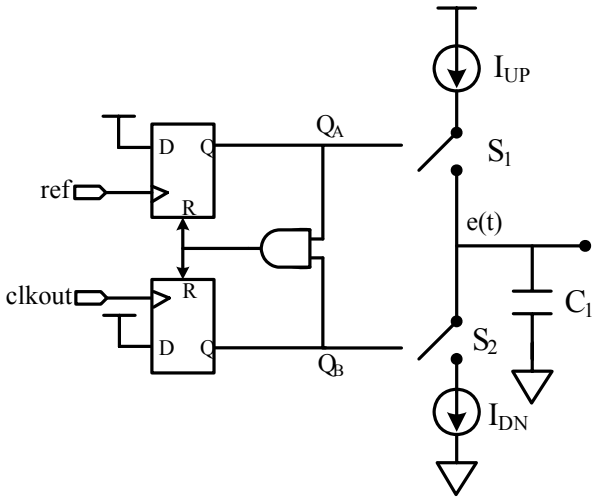


Fig. 2.9 PFD with charge pump

A noticeable problem is the dead zone when we discuss the PFD combined with CP. Due to the parasitic capacitance at the switches, the Q_A or Q_B may not have enough time to reach its logic high value to turn on the switch. That is, if the phase error is below some small value ϕ_0, the switch will not be turned on, and the CP will not charge or discharge the control voltage. The control voltage will be floating and no longer a function of $\Delta\phi$. The VCO will accumulate as much random phase error as ϕ_0 to be able to turn on switches. Therefore it will cause jitter in the VCO's output. One way to solve such a problem is to increase the reset time of the PFD. If the pulse is long enough to turn on the switch at $\Delta\phi=0$, it is able to produce the proportional net current with respect to little increment in the phase difference.

If the charge or discharge current of CP is I_P, the phase error between REF and CLKOUT is $\Delta\phi$, the average error current in a cycle is I_e. Besides, α=1 in tristate PFD and α=2 in XOR-based PFD.

$$I_e = \frac{\Delta\phi \times \alpha}{2\pi} I_p \tag{2.1}$$

$$K_d = \frac{I_e}{\Delta\phi} = \frac{\alpha \times I_p}{2\pi} \tag{2.2}$$

2.3.2 Voltage Controlled Oscillator and Interpolator

VCO is one of the important component of PLLs. It mainly decide the performance of the PLLs. As implied by the name, its frequency is near linear function of its input control voltage. The transfer function can be written as:

$$\omega_{out} = \omega_0 + K_{VCO} V_c \tag{2.3}$$

where ω_{out} is the output frequency of VCO, ω_0 is the free running frequency, K_{VCO} is gain or sensitivity of the VCO, (usually in rad/s/V). Next, we want to derive the phase transfer function, since the phase is the integration of frequency to time:

$$\int \omega_{out} dt = \omega_0 t + K_{VCO} \int V_c dt \tag{2.4}$$

We only interest the second term of the total phase. We call $K_{VCO}\int_0^t V_{cont} dt$ as the "excess phase", denoted by ϕ_{ex}. In actual, in the analysis of PLLs, we only consider the VCO as input of control voltage and output of excess phase. If the system is LTI, then we get:

$$\phi_{ex} = K_{VCO} \int V_c dt \tag{2.5}$$

$$\frac{\phi_{ex}}{V_c} = \frac{K_{VCO}}{s} \tag{2.6}$$

Therefore the VCO acts as an integrator, providing a pole at $s = 0$ in the open loop transfer function in the PLL.

The interpolator is not always needed in PLLs but it depends on your design. My thesis is constructed by a 1.2GHz, 5 stage ring-oscillator based, 10 phase PLL. It is enough for using in transceiver and receiver. But if it is used in SSCG, the jitter in the output of VCO will a little larger. So we decide using interpolators, which are used to

interpolate the third signal from two reference signals to create 20 phase in the output of VCO. The interpolated phase position will be decided by the proportion of two source current[4][5].

2.3.3 Loop Filter

The dc component of the control voltage is proportional to phase error ΔΦ. So we need a low pass filter to avoid unwanted frequency terms, i.e. $2\,w_{ref}$, $3\,w_{ref}$, etc. The simplest LPF is to connect a capacitor to the control voltage. V_{out} can be expressed as:

$$V_{out} = \frac{I_p}{2\pi C_P} t \cdot \phi_0 u(t) \tag{2.7}$$

The impulse response is therefore given by

$$h(t) = \frac{I_P}{2\pi C_P} u(t) \tag{2.8}$$

yielding the transfer function

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi C_P} \cdot \frac{1}{s} \tag{2.9}$$

Consequently, the transfer function contains a pole at the origin. From (2.6) and (2.9), we can derive the open-loop transfer function as:

$$\frac{\phi_{out}}{\phi_{in}}(s)\Big|_{open} = \frac{I_p}{2\pi C_p} \frac{K_{vco}}{s^2} \tag{2.10}$$

Since the loop gain has two poles at the origin, this topology is called a “type II” PLL. Here the type is means the number of poles at origin in open loop gain and another named order is means the highest exponent in the denominator of closed loop gain. The simplest type II PLL is unstable because the loop gain has two poles at the origin. As illustrated in Fig. 2.10, each integrator contributes a constant phase shift

of 90°. Thus the system will oscillate at the gain crossover frequency. So we have to add a zero to increase phase margin.

We can add a resistor in series with the loop filter capacitor. The open-loop transfer function is derived as follows:

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_p}{2\pi}\left(R_1 + \frac{1}{sC_1}\right) \tag{2.11}$$

It follows that the PLL open-loop transfer function is equal to

$$\frac{\phi_{out}}{\phi_{in}}(s)\Big|_{open} = \frac{I_p}{2\pi}\left(R_1 + \frac{1}{sC_1}\right)\frac{K_{vco}}{s} \tag{2.12}$$

As shown in Fig. 2.11, because of the zero $1/(R_1C_1)$ the phase margin will increase and the system will not oscillate at the unit-gain frequency. However, a severe problem is induced in such method. Due to the charge pump drives the resistor in series with capacitor, each time a current is injected into the loop filter and then produces large voltage jump. Even in the locked condition, the mismatches between charge and discharge current and the charge infection, clock feedthrough of switches produce voltage jumps in V_C. It makes ripples of control voltage of VCO and degrades the purity of the output frequency spectrum.

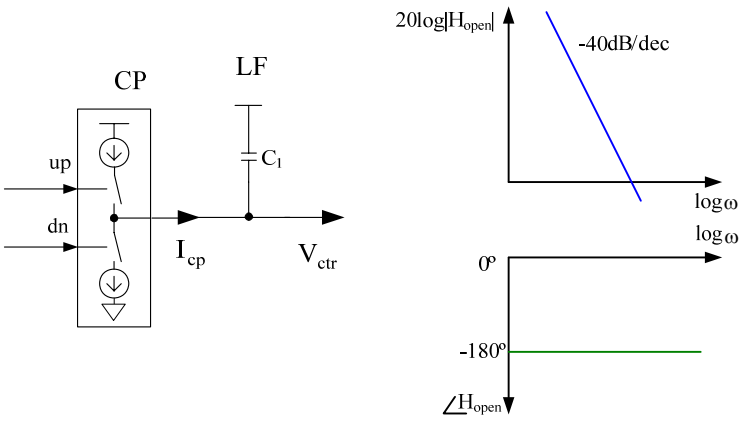


Fig. 2.10 Stability of 2-pole PLL

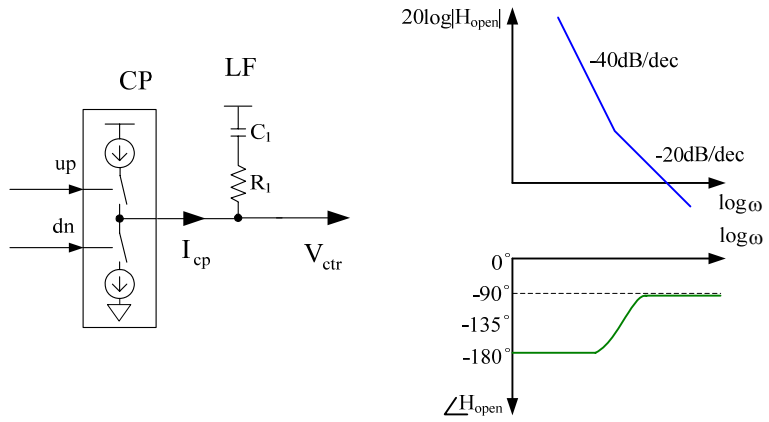


Fig. 2.11 Stability of 2-pole 1-zero PLL

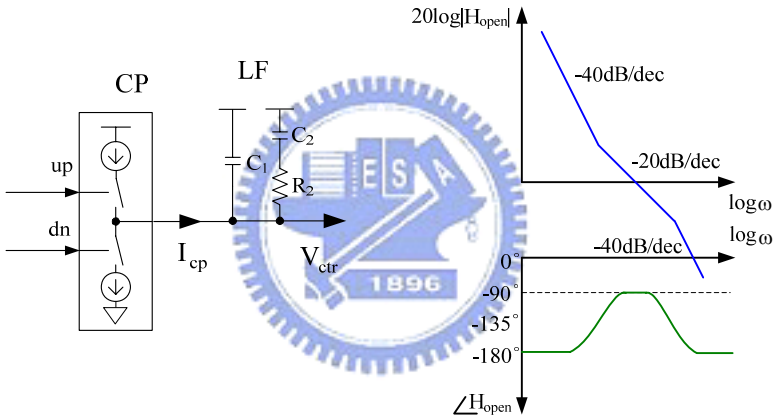


Fig. 2.12 Stability of 3-pole 1-zero PLL

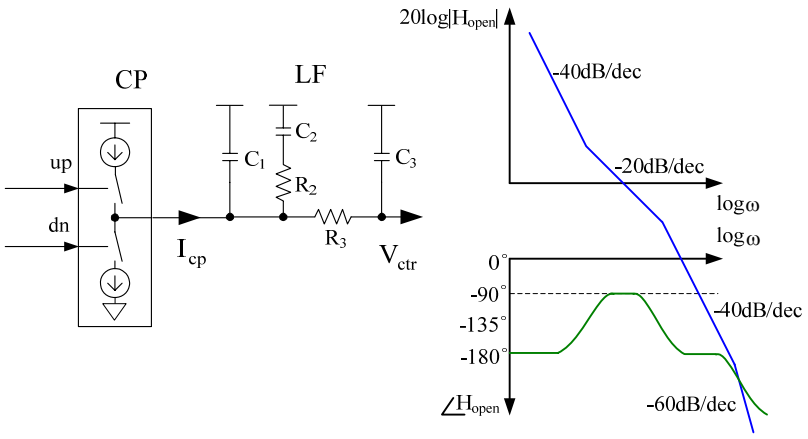


Fig. 2.13 Stability of 4-pole 1-zero PLL

We can ease this effect by adding a second capacitor in parallel with R_2 and C_2. The loop filter is now of 2nd order and the open loop transfer function of PLL now is of third-order and has stability problem, as shown in Fig. 2.12. But if we make C_2 is about one-fifth to one-tenth of C_1, the open-loop transfer function is near the second-order and would be stable.

$$F(s) = K_h \frac{s + w_2}{s\left(\frac{s}{w_1} + 1\right)} \tag{2.13}$$

where $K_h = \frac{C_2 R_2}{C_1 + C_2}$, and $\omega_2 = \frac{1}{C_2 R_2}$, $\omega_1 = \frac{C_1 + C_2}{C_1 C_2 R_2}$

Moreover, current switching in the charge pump at the reference frequency f_{ref} would cause unwanted sidebands at the frequency spectrum of VCO. We can add additional LPF to suppress the spur that is f_{ref} offset from the carrier frequency, as shown in Fig. 2.13. The loop filter transfer function is

$$F(s) = K_h \frac{s + w_2}{s\left(\frac{s}{w_1} + 1\right)\left(\frac{s}{w_3} + 1\right)} \tag{2.14}$$

where $K_h = \frac{C_2 R_2}{C_1 + C_2}$, and $\omega_2 = \frac{1}{C_2 R_2}$, $\omega_1 = \frac{C_1 + C_2}{C_1 C_2 R_2}$

$$\omega_3 = \frac{1}{C_3 R_3}$$

The additional pole must be lower than the reference frequency in order to significantly attenuate the spurs. However, it must be at least five times higher than the loop bandwidth, or the loop will almost assuredly become unstable.

2.3.4 Divider

If we want to synthesize any high frequency, we need a divider in the feedback path. The only relation between the frequency of VCO ω_{vco} and the frequency of the output signal of divider ω_{clkout} is

$$\omega_{clkout} = \frac{1}{N}\omega_{vco} \tag{2.15}$$

We integrate both sides of the equation, and thus get the phase relationship:

$$\theta_{clkout} = \frac{1}{N}\theta_{vco} \tag{2.16}$$

Generally speaking, the divider modulus is variable if you want variable frequency in the output of VCO if the oscillation of VCO is supported. So we also called the PLL frequency synthesizer.

2.4 Analysis of PLL Linear Model

Although PLL is a nonlinear system, we can analysis it in the way of section2.3. The transfer functions of the main blocks in PLL are already derived. Continuously, we will analysis the open loop transfer function of PLL.

2.4.1 Analysis of Open Loop Transfer Function

First we calculate the open loop transfer function G(s) with 2nd order loop filter:

$$G(s) = \frac{K_{PD}F(s)K_{vco}}{sN}$$

$$= -\frac{K_{PD}}{C_1 + C_2}\frac{1 + s/\omega_2}{s(1 + s/\omega_1)}\frac{K_{vco}}{s}\frac{1}{N} \tag{2.17}$$

For the sake of convenience, we make $\omega_2 = T_2^{-1}$ and $\omega_1 = \omega_2\left(1+C_2/C_1\right) = T_1^{-1}$. The open loop gain is:

$$\left|G\left(s\right)\right|_{s=jw} = -\frac{K_{PD}K_{vco}\left(1+jw/\omega_2\right)}{\omega^2 C_1 N\left(1+jw/\omega_1\right)}\frac{T_1}{T_2} \tag{2.18}$$

And the phase margin is:

$$\phi\left(\omega\right) = \tan^{-1}\left(\frac{w}{w_2}\right) - \tan^{-1}\left(\frac{w}{w_1}\right) + 180° \tag{2.19}$$

To insure stability, we want to have the maximum phase margin at the crossover frequency. We differentiate $\phi(\omega)$ being equal to zero to get the frequency where the phase margin is maximum.

$$\frac{d\phi}{d\omega} = \frac{1}{1+\left(\omega/\omega_2\right)^2}\frac{1}{\omega_2} - \frac{1}{1+\left(\omega/\omega_1\right)^2}\frac{1}{\omega_1} = 0 \tag{2.20}$$

$$\omega_p = \sqrt{\omega_1\omega_2} \tag{2.21}$$

And therefore the maximum phase margin ϕ_p is:

$$\phi_p = \tan^{-1}\left(\frac{\omega_p}{\omega_2}\right) - \tan^{-1}\left(\frac{\omega_p}{\omega_1}\right) + 180° \tag{2.22}$$

From Eqn.(2.18), let $G\left(j\omega_p\right)=1$, we can get C_1:

$$C_1 = \frac{K_d K_{vco} T_1}{\omega_p^2 N T_2}\left\|\frac{\left(1+j\omega_p/\omega_2\right)}{\left(1+j\omega_p/\omega_1\right)}\right\| \tag{2.23}$$

Thus if we decide the loop bandwidth ω_c, and the phase margin ϕ_c, we can derive w_1 and w_2 from the following equations:

$$\omega_1 = \frac{\omega_p}{\sec\phi_p - \tan\phi_p} \tag{2.24}$$

$$\omega_2 = \frac{\omega_p^2}{\omega_1} \tag{2.25}$$

Therefore, we can get the C_2 and R_2, respectively.

$$C_2 = C_1\left(\frac{\omega_1}{\omega_2} - 1\right) \tag{2.26}$$

$$R_2 = \frac{1}{C_2\omega_2} \tag{2.27}$$

If we use the 3rd order filter as the loop filter of PLL, due to the additional LPF, the added attenuation with regard to F_{ref} is

$$ATTEN = 20\log\left[(2\pi F_{ref} R_3 C_3)^2 + 1\right] \tag{2.28}$$

So if we decide the ATTEN of loop filter, we can get $\omega_3 = \frac{1}{C_3 R_3}$ by

$$T_3 = \frac{1}{\omega_3} = \sqrt{\frac{10^{(ATTEN/10)} - 1}{(2\pi F_{ref})^2}} \tag{2.29}$$

As we mentioned above, the ω_3 must be lower than the reference frequency, in order to significantly attenuate the spurs. Because ω_3 will degraded the phase margin, we must recalculated the open loop unit gain ω_c and the relationship between ω_1, ω_2, ω_3 and ω_c. Similar to the Eqn.(2.20), we use the same way to derive the relation between ω_1, ω_2, ω_3 and ω_c.

$$T_2 = 1\Big/\left[\omega_c^2\,(T1 + T3)\right] \tag{2.30}$$

From the ref [8], we can get the new open loop unit gain ω_c as

$$\omega_c = \frac{\tan\phi \cdot (T_1 + T_3)}{\left[(T_1 + T_3)^2 + T_1 T_3\right]} \times \left[\sqrt{1 + \frac{(T_1 + T_3)^2 + T_1 T_3}{\left[\tan\phi \cdot (T_1 + T_3)\right]^2}} - 1\right] \tag{2.31}$$

From Eqn.(2.18), let $G(j\omega_c) = 1$, we can get C_1:

$$C_1 = \frac{T_1}{T_2} \frac{K_{pd} K_{vco}}{\omega_c^2 N} \left[\frac{(1 + \omega_c^2 T_2^2)}{(1 + \omega_c^2 T_1^2)(1 + \omega_c^2 T_3^2)}\right]^{1/2} \tag{2.32}$$

Similar to the 2nd order filter, we can get

$$C_2 = C_1 \left(\frac{\omega_1}{\omega_2} - 1\right) \tag{2.33}$$

$$R_2 = \frac{1}{C_2 \omega_2} \tag{2.34}$$

The only variable components are R_3 and C_3. The single condition is Eqn.(2.29). A rule of thumb choose $C_3 \le C_1/10$, otherwise T_3 will interact with the primary poles of the filter. Similarly, choose R_3 at least twice the value of R_2. With the aid of simulation, we can get satisfactory results by using above analysis.

2.4.2 Analysis of Closed Loop Transfer Function

In the following, we will discuss the closed loop transfer function of using 2nd order loop filter. From the Eqn.(2.17), let $K = \frac{K_{PD} K_h K_{vco}}{N}$, which equals the loop bandwidth ω_c, and we obtain another expression of $G(s)$:

$$G(s) = \frac{K(s + \omega_2)}{s^2\left(1 + \frac{s}{\omega_1}\right)} \tag{2.35}$$

Thus the closed loop transfer function $H(s)$ is:

$$H(s) = \frac{N G(s)}{1 + G(s)} \tag{2.36}$$

$$= \frac{N K(s + \omega_2)}{s^2(1 + s/\omega_1) + K S + K\omega_2} \tag{2.37}$$

Because $H(s)$ is of 3rd order system, we cannot use the control theorem to analyze it. However, in the lower frequency, we can treat the CP-PLL with 2nd order loop filter as the 2nd open-loop system. Then the Eqn.(2.37) can be written as

$$H(s) = \frac{N K(s + \omega_2)}{s^2 + K S + K\omega_2} \tag{2.38}$$

Compared $H(s)$ with the normalized form for a 2nd order control system:

$$H(S) = \frac{2\zeta\omega_n S + \omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2} \tag{2.39}$$

where ζ = Damping factor , ω_n = Natural frequency

We can get the following relationships:

$$\zeta = 0.5\sqrt{K/\omega_2}\ ,\ \omega_n = \sqrt{K\omega_2} \tag{2.40}$$

If ζ is larger, the step response will oscillate and rapidly damp to the final value. However, it would have large overshoot. On the contrary, if ζ is too small, the step

response will converge slowly and need more time to stable. ω_n means the oscillation frequency of the system in the transient response. Fig. 2.14 shows the step response under various ζ . We can observe that the damping ratio among the range of $0.8 \le \zeta \le 1$ is a good choice if we want proper settling time and acceptable overshoot. Besides, we calculate the phase margin under various K/ω_2 , which is proportional to ζ . We can find that if the K/ω_2 is larger, the phase margin is larger. By choosing $0.8 \le \zeta \le 1$, we thus get $46.4° \le PM \le 62°$. Table 2.1 is the phase margin under various K/ω_2 .

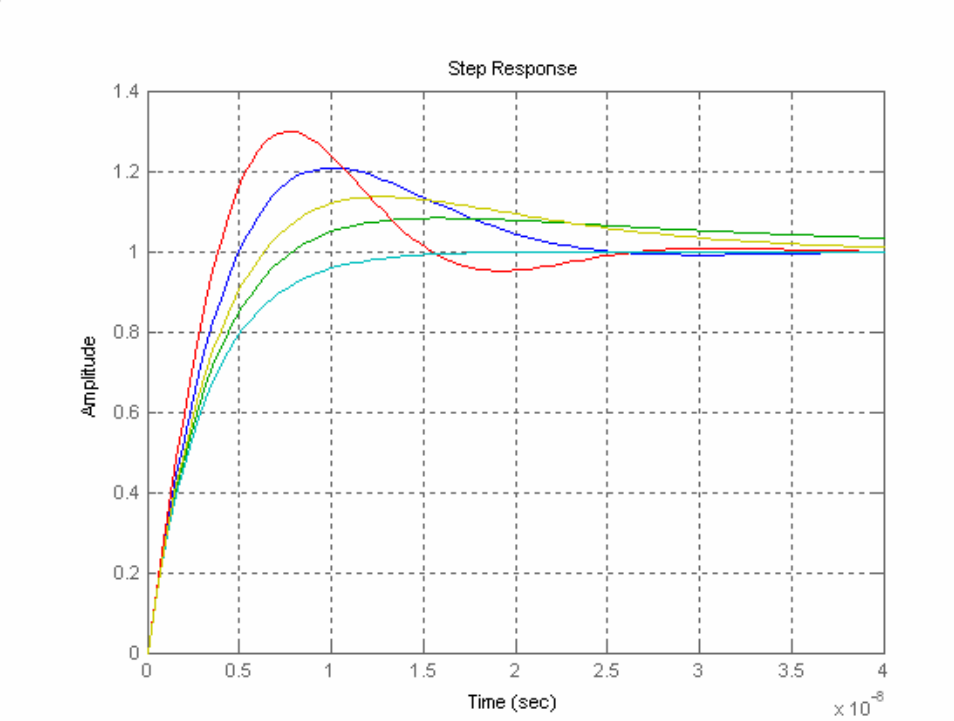


Fig. 2.14 Step response under various ζ

Table 2.1 Phase margin under various K/ω_2

K/ω_2	2.5	3	3.5	4	4.5	5
PM	46.4°	53.1°	58.1°	61.9°	64.9°	67.4°

Chapter 3

Basic of Spread Spectrum Clock Generator

3.1 Background: EMI Problem

Today, faster operating speeds of electrical devices result in more Electromagnetic Interference (EMI) at higher frequency. EMI can pollute carefully managed radio spectrum which is caused by the radiation of unwanted radio frequency signals. In order to increase the working frequency, we hope to reduce the rising time and falling time and increase the effective working time. But EMI will occur in these electronic systems that has changing voltages and current rapidly, like charge and discharge. However, the Federal Communications Commission (FCC) in the United States has regulation rules about the maximum power of EMI (Fig. 3.1). The one that should pay attention to is that it concentrates on the peak power, not on the average power.

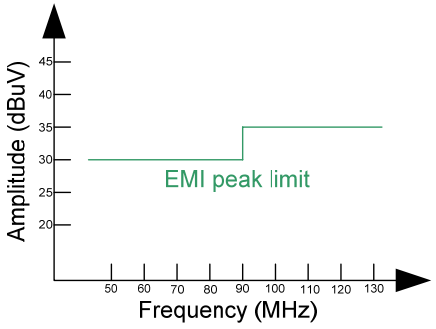


Fig. 3.1 FFC EMI peak limit

Today there are several methods to solve this problem (EMI)：metal shielding, multi-layer printed circuit boards, special casing, passive components, pulse shaping, slew-rate control, layout technique, and the spread spectrum clocking.

“Metal shielding” is the simplest method to lessen EMI effect. It only adds more power and ground layers to contain EMI instead of eliminating. There are two major drawbacks in this method: 1. The system manufacturing costs is increased. 2. It is not good choice for handheld and portable systems because weight is the important issue [9].

“Pulse shaping” does not decrease the steady power but decrease the transition power. It is to round off corners and removing some of the higher frequency components and their energy. There are also two drawbacks in this method: 1. We have difficulties at controlling the portion of transition in the waveform accurately. 2. If we rounding too much in switching region, the digital signals will look like analog signals so that those signals will degrade qualities.

“Staggering the output” is common used in SDRAMs. This method will temporally spread the energy. The energy at any instant will decrease by phase-shifting. There is a major drawback in this method: 1. Output-to-output are inherent and might by themselves occupy the time window [10].

“Spread spectrum clocking” is slightly modulating the frequency of clock signals and the energy of the signals will be dispersed to a controllable small range. This method is popularly used in all kinds of electronic devices [11].

Finally, although there are so many methods to eliminate EMI effect, we also can classify into two types: 1. Enclosing the EMI. 2. Reducing EMI at the source. We prefer use the latter and spread spectrum clocking belongs to it. There are two major advantages in this: 1. It makes improvement in the original of EMI source and

provides more efficient reductions in EMI effect. 2. It also has better immunity in manufacturing process variations.

3.2 Concept of Spread Spectrum

The basic idea of the spread spectrum clocking is to slightly modulate the frequency of clock signals and the energy of the signals will be scattered to a controllable wide range. The energy is distributed by modulating the signal slowly between two frequency boundaries. The peak energy of every harmonic component in the spectrum is decreasing after spreading spectrum modulation. The higher the order of harmonic, the more EMI attenuation is in energy peaks. We can see the power reduction in peak emissions, not in average emissions, so spread spectrum clocking can cause low EMI effect. If a system has a fixed frequency, then all address, data, and control signals will also switch at a multiple of fixed frequency. If the system reference frequency is modulated in a spread spectrum fashion, all clock-dependent outputs (such as address and data signals) will also exhibit this modulation. As a result, the cumulative EMI of the entire system will be reduced since each individual output signal's EMI level is reduced.

To understand how frequency modulation can lead to spread spectrum, we can analyze from frequency modulation (FM) because spread spectrum clocking technique is an application of FM [12]. A single-tone sinusoidal signal modulated by another sinusoidal signal is taken as the example:

Consider a sinusoidal modulating signal:

$$m(t) = A_m \cos(2\pi f_m t) \tag{3.1}$$

The instantaneous frequency of the resulting FM signal:

$$f_{instantaneous}(t) = f_c + k_f A_m \cos(2\pi f_m t) = f_c + \Delta f \cos(2\pi f_m t) \quad (3.2)$$

$$\Delta f = k_f A_m \quad (3.3)$$

The Δf is frequency deviation, which represents the maximum departure of the frequency of the FM signal from the carrier frequency f_c. The $\theta_{instantaneous}(t)$ of the FM signal is:

$$\theta_{instantaneous}(t) = 2\pi \int_0^t f_i(t)dt = 2\pi f_c t + \frac{\Delta f}{f_m}\sin(2\pi f_m t) = 2\pi f_c t + \beta \sin(2\pi f_m t) \quad (3.4)$$

$$where \quad \beta = \Delta f / f_m \quad (3.5)$$

β is called the modulation index which representing the phase deviation of the FM signals. Approximately saying, frequency modulation can be distinguished into two cases by the value of β: narrow-band FM and wide-band FM. The narrow-band FM is modulation smaller than specific radian. However, the wide-band FM is modulation larger than specific radian. Generally speaking, the spread spectrum clocking belongs to the wide-band FM.

Then, the relationship between β and maximum power will be discussed. The amplitude power of FM signal depends on the modulation index β. The physical explanation for this property is that the total power of an FM signal is fixed. So when we modulate a signal and generate a FM signal, the side frequency appears and the carrier frequency power decrease. The power is inverse proportion to the β. The total power of a signal is equal to the summation of the square of each harmonic amplitude and is fixed as shown in Fig. 3.2.

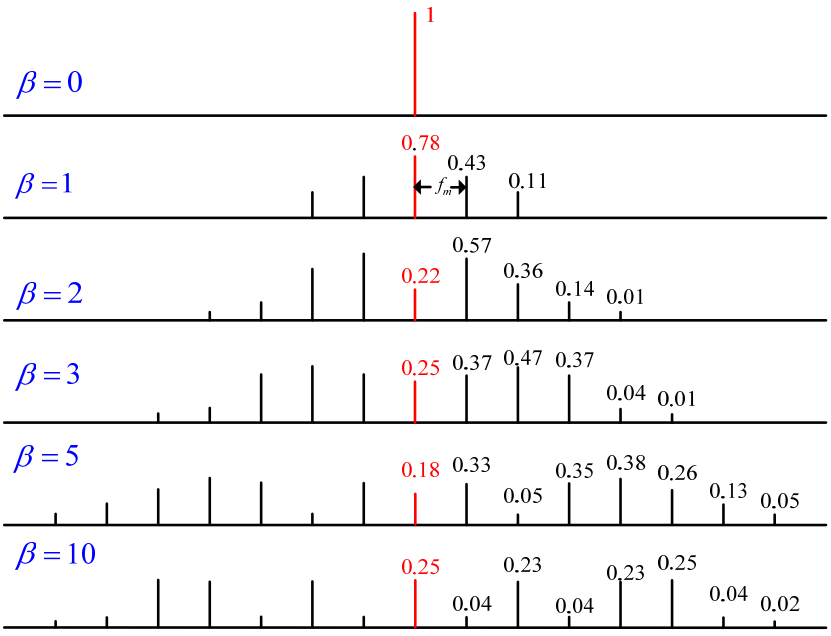


Fig. 3.2 Spectra of sinewave FM under various modulations

There is a knew Carson's rule [5]:

$$B_T \cong 2\Delta f + 2f_m = 2\Delta f\left(1 + \frac{1}{\beta}\right) \tag{3.6}$$

A square wave is composed of infinite sinusoidal components. For a frequency pulse train, each harmonic B_n is:

$$B_{nT} = 2(n\beta + 1)f_m \tag{3.7}$$

$$\text{If } \beta >> 1, \text{ then } \quad B_{nT} = nB_T \tag{3.8}$$

Finally, we can get a conclusion: the higher the harmonic number, the more is the spread-out power.

3.3 Spread Spectrum Parameter

Generally speaking, spread spectrum modes can be classified into three kinds according their spreading frequency comparing with original frequency: center-spread, up-spread and down-spread.

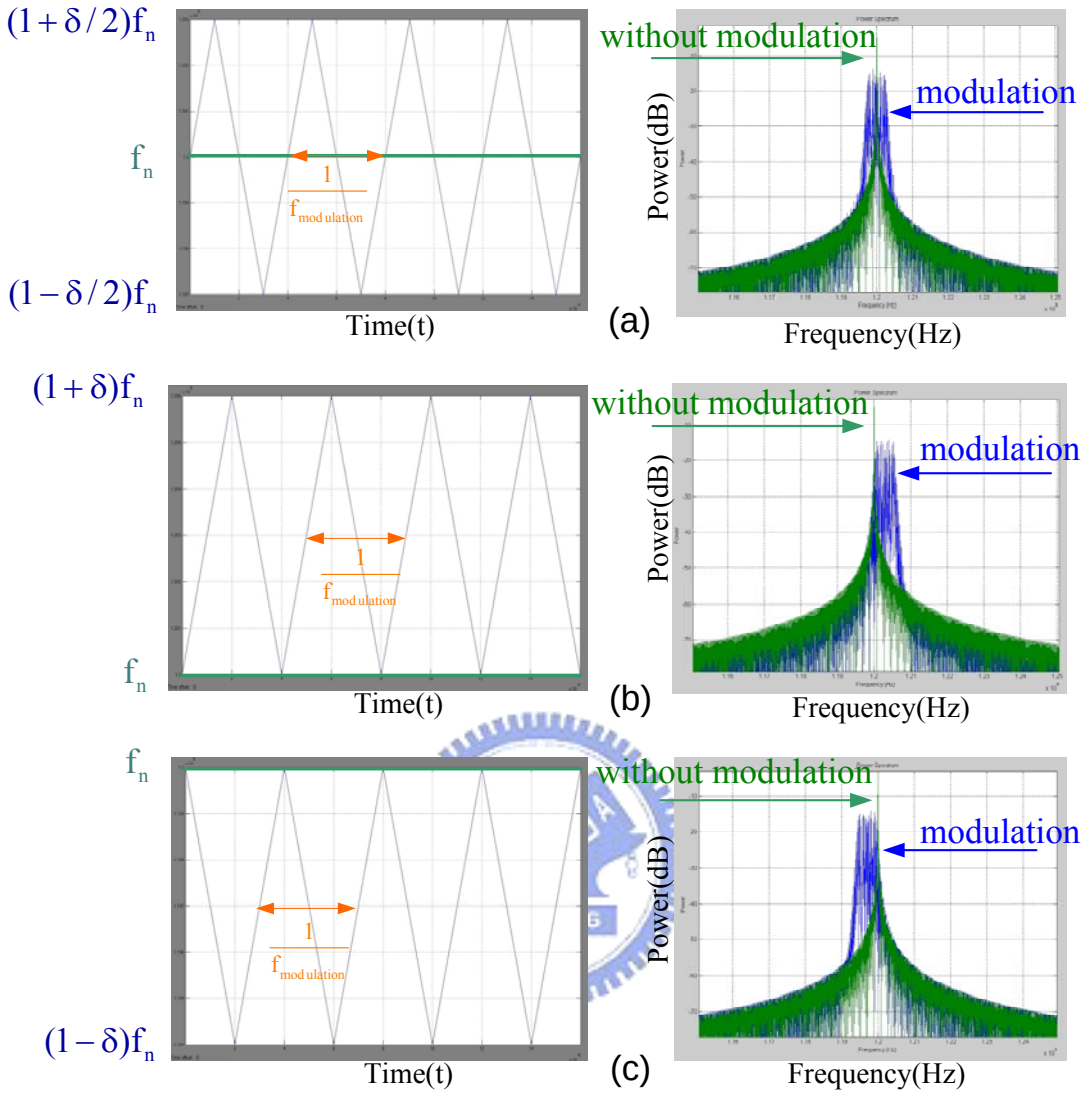


Fig. 3.3 Modulation profiles and spectrums of

(a) center-spread (b) up-spread (c) down-spread

Center-spread: as shown in Fig. 3.3(a), the frequency without modulating is f_n. δ is modulation deviation which means the total amount of spreading as a relative percentage of f_n, f_m is modulation frequency which means how often the modulation changes one time. The demanded frequency will change between $(1+\delta/2)f_n$ and $(1-\delta/2)f_n$. In this figure, f_n is 1.2GHz, δ is 5000ppm, so that the demanded frequency will spread between 1.197GHz and

1.203GHz. We also observe that every peak power of modulated frequency (blue part) is lower than normal frequency (green part).

Up-spread: as shown in Fig. 3.3(b), the demanded frequency will change between f_{normal} and $(1+\delta)f_n$, so that the demanded frequency will spread between 1.2GHz and 1.206GHz. Because it is more difficulties in higher working frequency and could make systems fail, some systems do not tolerate clock above the normal frequency. For this reason, up-spread is seldom adopted.

Down-spread: as shown in Fig. 3.3(c), The demanded frequency will change between f_{normal} and $(1-\delta)f_n$, so that the demanded frequency will spread between 1.194GHz and 1.2GHz. In other way, we can think this is center-spread with center frequency is 1.197GHz and δ is 2500ppm. Therefore, the maximum working frequency will not over normal frequency.

3.3.1 Modulation Frequency

In the main stream, the modulation frequency is commonly between 30 and 50KHz. Although the most systems specify the modulation frequency, we must understand the effect about EMI reduction with different modulation frequency. From Matlab simulation (Fig. 3.4), we can observe high frequency modulation results more attenuation in EMI effect. Although the higher modulation frequencies can cause more EMI reductions, we can not increase it in an unlimited manner. The modulation frequency should be as low as possible for the timing jitter issue. The less the modulation frequency is, the less the timing jitter will have. It is not easy for clock data recovery (CDR) to recovery data if the timing jitter is too large.

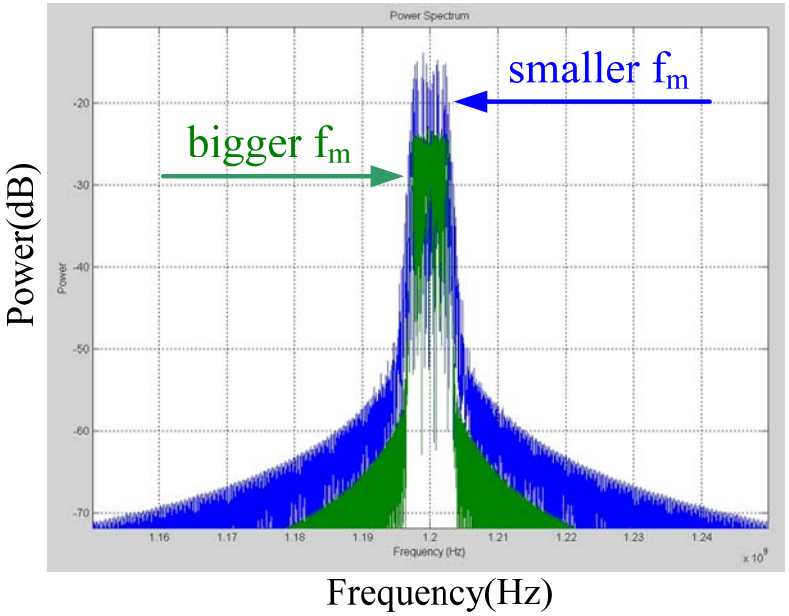


Fig. 3.4 Comparing between modulation frequency and peak attenuation

3.3.2 Modulation Profiles

The modulation profile is one of the most important parameters that affects the performance of spread spectrum. The shape of modulation profile determines the distribution of frequency. In other words, the modulation profile in time domain determines the shape of power energy in frequency domain. From Fig. 3.5, we can see all the V_C profiles in time domain and their corresponding spectrum in frequency domain. The input modulation profile is similar with the V_C profile in their VCO. The frequency distribution is closely related with V_C, and the V_C is closely related with modulation profiles. As the result, the frequency is closely related with their input modulation profiles.

Fig. 3.5(a) is the V_C without spreading spectrum. We can see the V_C is stable after transition time, that is, the frequency is fixed. So its power magnitude at the frequency is almost near 0dB.

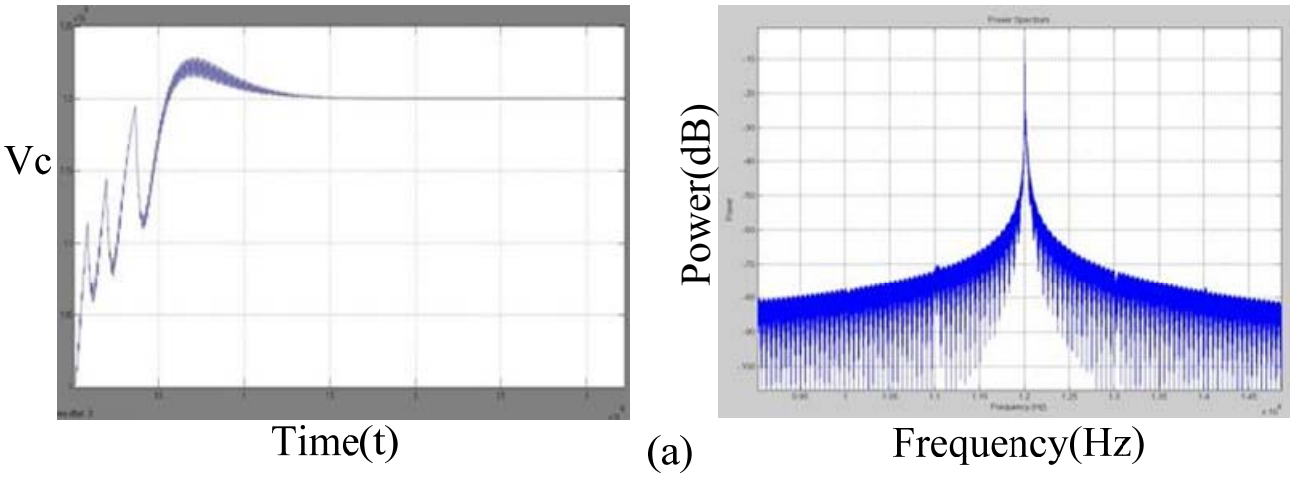
The modulation profile is sinusoidal in Fig. 3.5(b). We can also observe that the

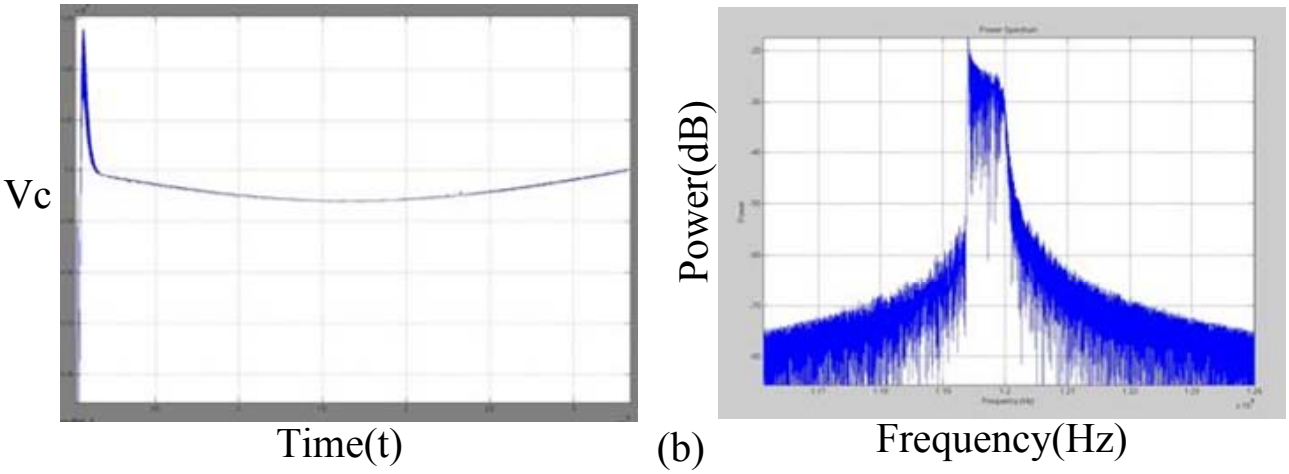
V_C is also sinusoidal. Because the time at lower frequency is longer than higher frequency, the frequency domain distribution is shown in Fig. 3.5(b).

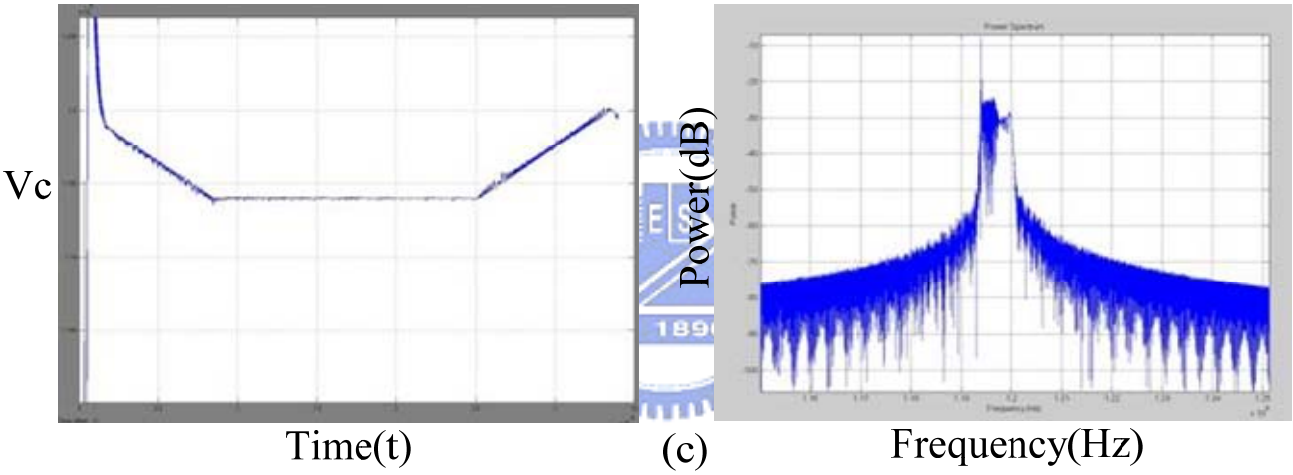
There is a trapezoid signal modulate the ΔΣ modulator in Fig. 3.5(c). The V_C is also show the ladder-shaped. Most of time V_C is in the low voltage, so the energy of low frequency is getting more magnitude.

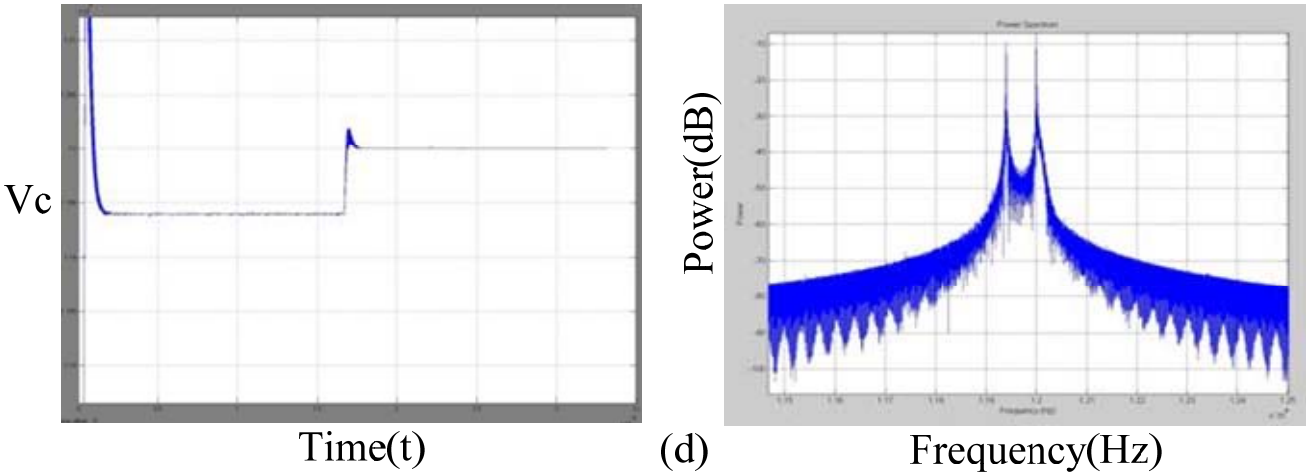
There are only two voltages in step modulation profile which results in only two voltages in V_C. Therefore, there are only two frequencies in frequency domain. So we can see the magnitude in that two frequencies are high, the others are low (Fig. 3.5(d)).

The above three modulation profiles can not spread the energy equally because of its frequency verses time is not fixed. The triangular modulation profile will get the best EMI reduction because of its frequency deviation is regular in fixed time and the spectrum will almost be plane (Fig. 3.5(e)). Consequently, the power magnitude will lower than other type modulation profiles.




Vc
Time(t)
(b)
Power(dB)
Frequency(Hz)


Vc
Time(t)
(c)
Power(dB)
Frequency(Hz)


Vc
Time(t)
(d)
Power(dB)
Frequency(Hz)

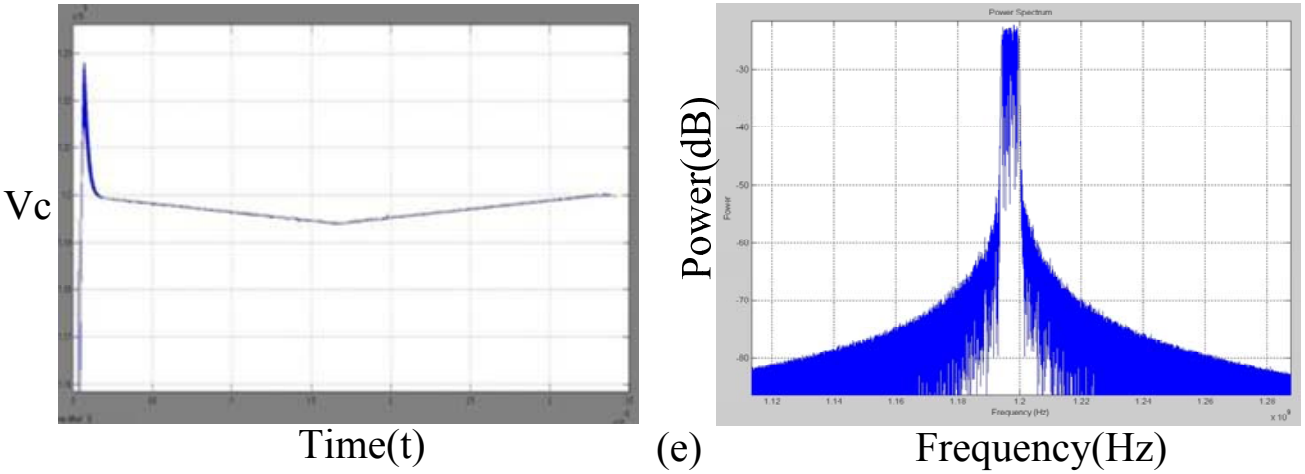
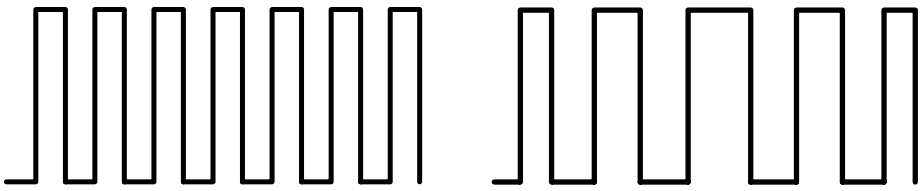


Fig. 3.5 Vc profiles and their corresponding spectrums (a) without modulation signal (b)sinusoidal modulation signal (c) trapezoid modulation signal (d) step modulation signal (e)triangular modulation signal

3.3.3 Timing Impacts

In a SSCG system, the frequency varies with time. So does the data if the transmitter uses the clock from the SSCG system. Despite of the modulation profiles, the clock waveform will look like that shown in Fig. 3.6(b).



(a) (b)

Fig. 3.6 Time domain behaviors (a) without modulating (b) with modulating

A. Cycle-to-Cycle Jitter

The cycle-to cycle jitter is not steady because it depends on the previous cycle time. From Fig. 3.7 we can see the relationship between cycle time and jitter.

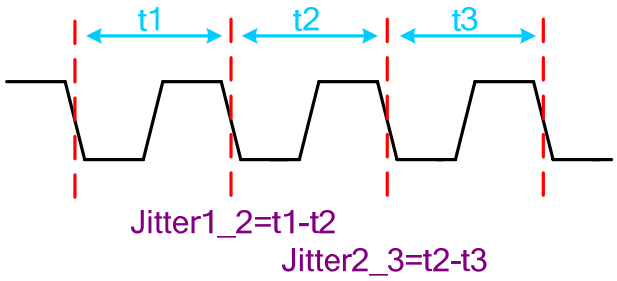


Fig. 3.7 Diagram of cycle to cycle jitter

Here we will derive some formulas about cycle to cycle jitters. The period difference between normal frequency and maximum modulation frequency is:

$$\Delta T_{total} = \frac{1}{(1-\delta) f_n} - \frac{1}{f_n} \approx \frac{\delta}{f_n} \tag{3.9}$$

The number of cycles (N) that exist in the time interval that the modulated clock moves from f_n to $(1-\delta) f_n$ is

$$N = \frac{f_{avg}}{2 f_m} \tag{3.10}$$

,where f_{avg} is the average frequency of the spread spectrum clock, and f_m is the modulation frequency. From triangular modulation profile, we can derive the average frequency is

$$f_{avg} = (1 - 0.5\delta) f_n \tag{3.11}$$

Therefore, the cycle-to-cycle jitter due to spread spectrum clock can be expressed as

$$\begin{aligned} \Delta T_{c-c} &= \frac{\Delta T_{total}}{N} = \frac{\delta}{f_n} \cdot \frac{2 f_m}{(1 - 0.5\delta) f_n} \\ &= \frac{2 f_m \delta}{(1 - 0.5\delta) {f_n}^2} \end{aligned} \tag{3.12}$$

For a 1.2GHz spread spectrum clock with 0.5% triangular modulation and 31

KHz modulation frequency, the cycle-to-cycle jitter is

$$\Delta T_{c-c} = \frac{2 \times 31 \times 10^{3} \times 0.5\%}{(1-0.5 \times 0.5\%)(1.2 \times 10^{9})^{2}} = 2.15 \times 10^{-16} \quad (3.13)$$
$$= 0.215 fs$$

B. Long-Term Jitter

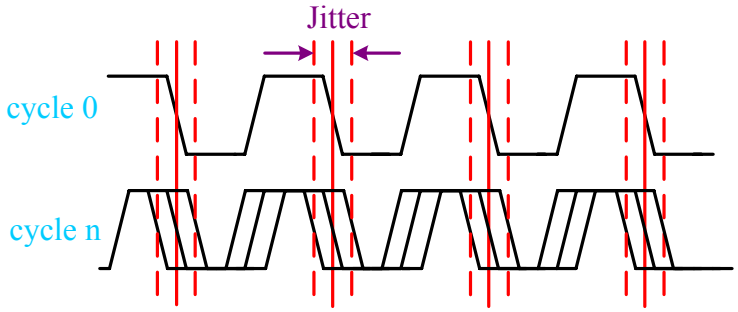


Fig. 3.8 Diagram of peak to peak jitter

Long-term jitter measures the maximum change in a clock's output transition form its ideal position. Therefore, Eqn.(3.9) can be viewed as the long-term jitter of a down-spreading clock signal. Similarly, for a 1.2GHz spread spectrum clock with 0.5% triangular modulation and 31 KHz modulation frequency, the long-term jitter is

$$\Delta T_{total} = \frac{\delta}{f_{nom}} = \frac{0.5\%}{1.2 \times 10^{9}} = 4.166 \times 10^{12} \quad (3.14)$$
$$\approx 4.2 ps$$

Thus, the cycle-to-cycle jitter of the spread spectrum clock is in a considerably small compared with non-spread clock signal. However, the long-term jitter of spread spectrum signal is significant.

Chapter 4

Principles of Spread Spectrum Clock Generator

4.1 Concept of SSCG Using Switching Phase

In general, SSCGs include four types. The first type is digital processing circuit technique [13][14]. This method has speed limit of action. The second type is to modulate the divider [15][16][17][18][19][20][21] (Fig. 4.1) and the major problem is to design proper bandwidth. The third type is to modulate the control voltage of the VCO [22][23][24][25] (Fig. 4.2). It has the drawback about accurate in controlling spreading. Finally, the fourth type is to modulate the multiphase in the output of VCO [26][27][28][29](Fig. 4.3) and this is also the basic theorem about our proposed SSCG because that it owns lowest jitter in all the types [26]. For example, if the divider is divided by N, the minimum variation in type II is $\frac{1}{N}$, but the minimum variation in type IV is only $\frac{1}{N \times P}$. However, one drawback is its control jumping logic will cause jumping spur. This is due to regular sequence of jumping modulus, it would cause spurs in the spectrum. The modern solution is to use the ΣΔ modulator to solve it. It can cause randomization and noise shaping. In the following, we will introduce the switch phase mechanism and the principle of ΣΔ

modulator.

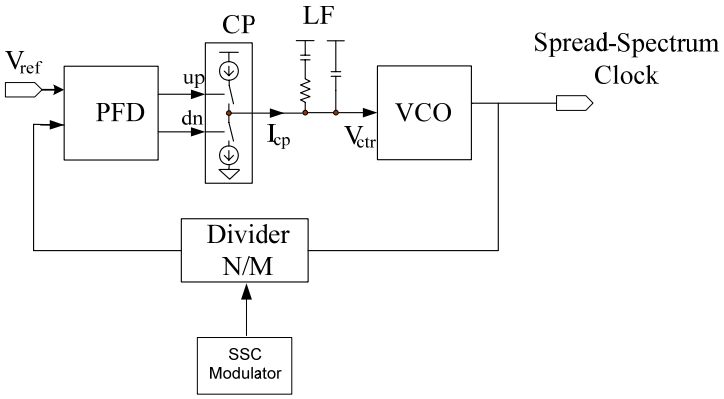


Fig. 4.1 Type II of SSCG

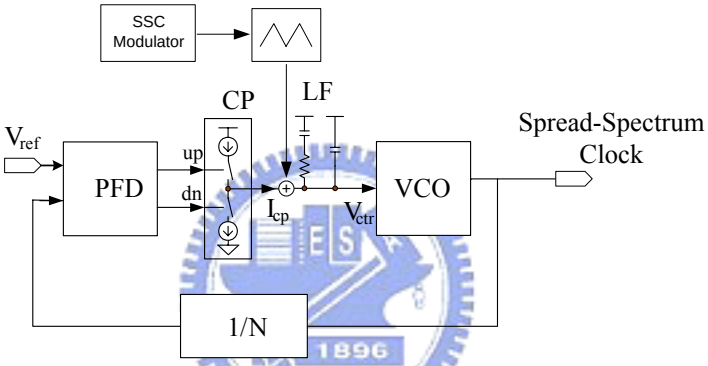


Fig. 4.2 Type III of SSCG

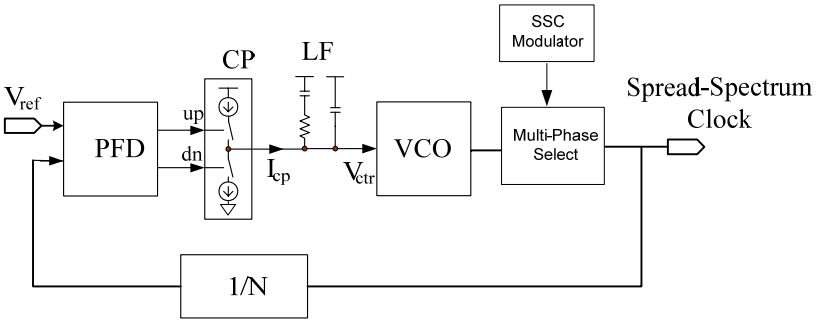


Fig. 4.3 Type IV of SSCG

4.2 The Switch Phase Mechanism

Fig. 4.4 is the timing diagram of 5 (P) phases from VCO. The time difference between any two phases is the same. We can see if the period of each phase is T_{VCO}, the time between previous phase and current phase is $T_D = T_{VCO} / 5 = T_{VCO} / P$,

where P is the number of phase.

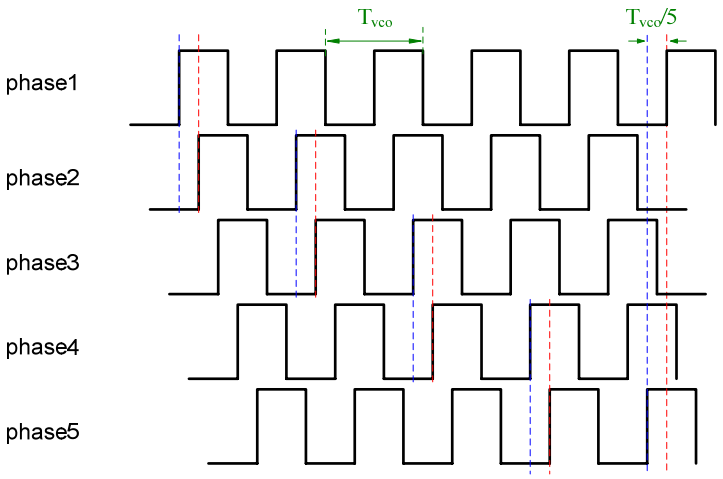


Fig. 4.4 Timing diagram of 5 phases from VCO

The output of VCO is feed into a divider which is divided by N. The period of divider output without switching phase is $N \times T_{VCO} = T_{ref}$. If we jump one phase in one T_{ref}, the period of divider output will be $(N + \frac{1}{P}) \times T_{VCO} = (1 + \frac{1}{N \times P}) T_{ref}$. The timing diagram is shown in Fig. 4.5.

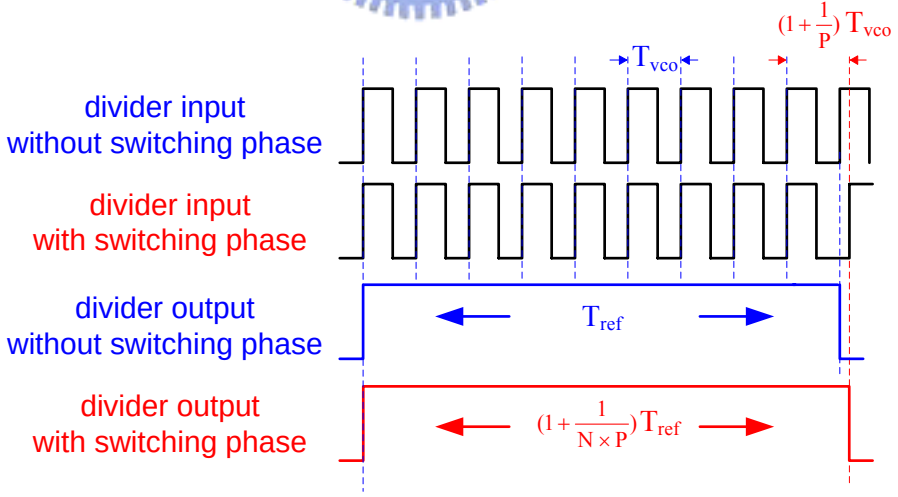


Fig. 4.5 Timing diagram of switching phase

So the period of the output from divider is longer the T_{ref}, the charge pump will charge the loop filter so that the V_C is higher and the period of the output from divider is decreased. The above mechanism is a transient behavior. When it is stable,

the output of the divider will be the same with T_{REF}. Thus, the new T_{VCO}' must be less than the original T_{VCO} so that the new T_{ref} will be the same as the original T_{ref}. This method can be used to vary the oscillation frequency of the VCO.

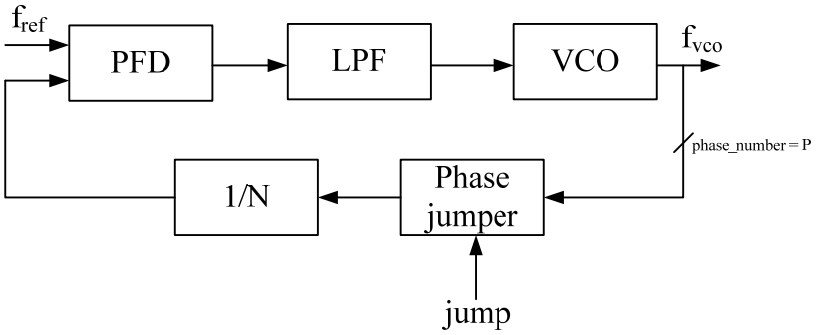


Fig. 4.6 Simple jumping phase PLL

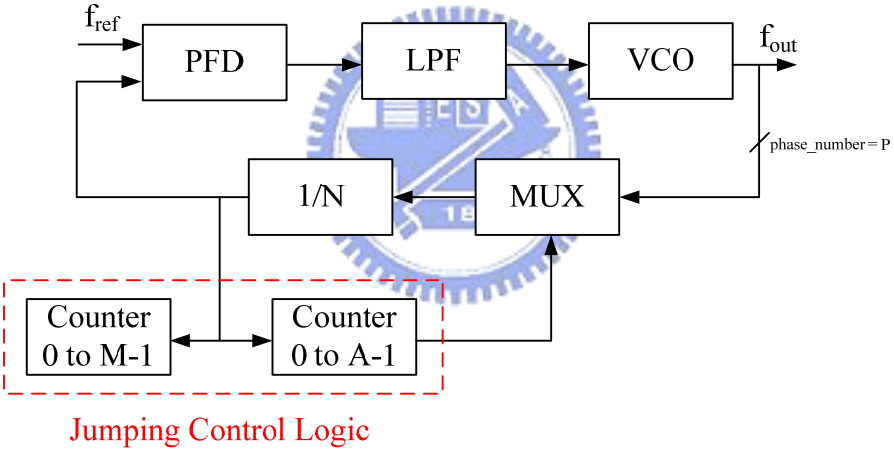


Fig. 4.7 Switching phase PLL using Boolean logic

Fig. 4.6 shows the basic architecture of switching phase PLL. In the locked state, f_{REF} is equal to divider output. So f_{vco} would finally equals $f_{vco} = f_{ref}(N + \frac{\alpha}{P})$ $= f_{vco\_original}(1 + \frac{\alpha}{N \times P})$, where α is the number of jumping phase. We incorporate the MUX into the feedback path and further replace the jumping control with Boolean logic as shown in Fig. 4.7. For M sequence of f_{ref}, if MUX jump one phase for A sequence and no jump for the following M-A sequence, then the output frequency can be derived as follows:

$$\left[A \cdot (1 + \frac{1}{N \cdot P}) + (M - A) \cdot 1 \right] \cdot N / f_{vco} = M / f_{ref} \tag{4.1}$$

$$\therefore f_{vco} = f_{ref} \cdot N \cdot \frac{A \cdot \left(1 + \frac{1}{N \cdot P}\right) + (M - A) \cdot 1}{M} = f_{ref} \cdot \left(N + \frac{A/M}{P} \right) = f_{ref} (N + \frac{\alpha}{P}) \quad , M > A \tag{4.2}$$

The equivalent jumping ratio is A/M. This value can vary between 0 and 1 in fine steps by proper choice of A and M.

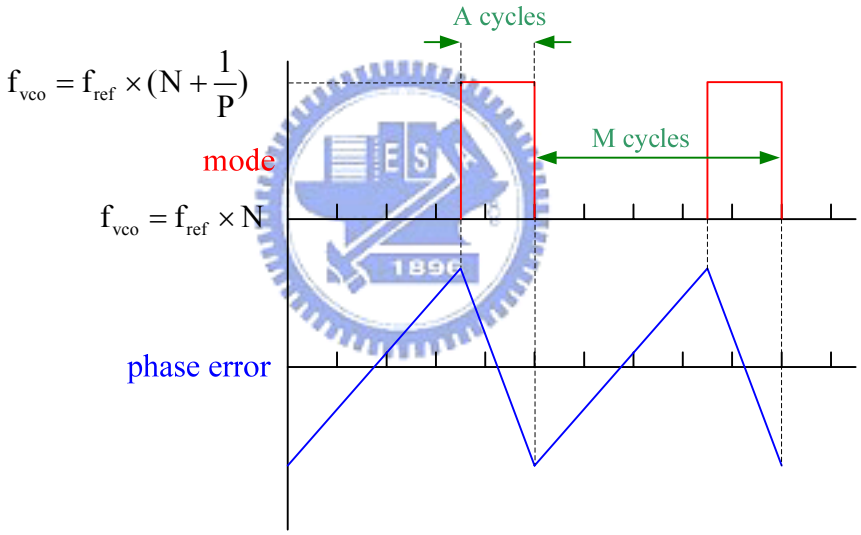


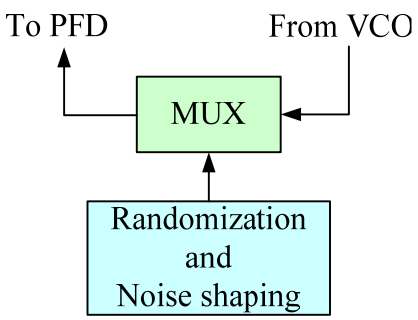
Fig. 4.8 Periodic accumulation error phenomenon

There is a problem we will meet when we use the jumping logic. When we use counters to control the modulus of the MUX, there is a periodic accumulation error, as given by Fig. 4.8. In the first M-A output pulses of the divider, the MUX jump 0 phase and the phase error accumulates. Then the phase error is gradually compensated after MUX jump 1 phase for A cycles. Since the phase error grows to significant values, the amplitude of the LPF output waveform is quite large, yielding jumping spurs f_{ref}/M offset from the carrier frequency. Because jumping spurs will

decrease the quality of communication, we should reduce it as much as possible. The most popular method is using ΣΔ modulator. We will explain it in detail in the next section.

4.3 Principles of ΣΔ Modulator

Because the reference spurs originate from the regular sequence of the MUX, we can eliminate spurs by randomize it. By randomization the choice of the jumping phase such that the average f_{VCO} is still given by $f_{REF} \times (N + \frac{\alpha}{P})$, which means individual multiplier factors occur for only short periods of time, the systematic fractional sideband would be converted to random noise. Besides, we can shape the resulting noise spectrum such that most of its energy appears at large frequency offsets. Therefore, the noise in the vicinity of the f_{REF} is sufficiently small and the noise at high offsets is suppressed by the LPF of the PLL, as shown in Fig. 4.9. With the ΣΔ modulator [30], the MUX modulus is near pseudo-random sequence and the quantization noise is differentiated in the signal band. The quantization noise comes from the reason that the MUX only can jump X or X+1, not X.Y, where the dot denotes a decimal point and X and Y represent the integer and fractional parts. Therefore, we can consider that the ideal MUX modulus X.Y is quantized to X or X+1 (X+d(t)). Fig. 4.10 is the Noise shaping by means of a ΣΔ modulator. Fig. 4.11 shows the sequence of the $d(t)$, Y is always quantized to 0 or 1.



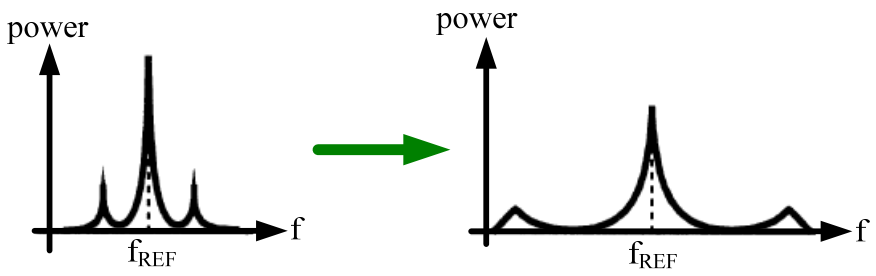


Fig. 4.9 Randomization and Noise shaping to eliminate unwanted spurs

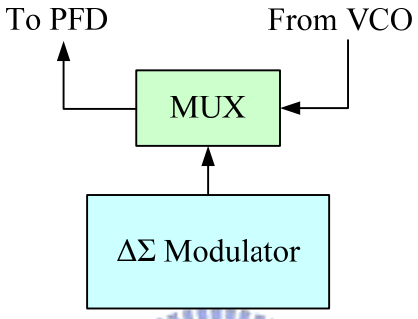


Fig. 4.10 Noise shaping by means of a ΣΔ modulator

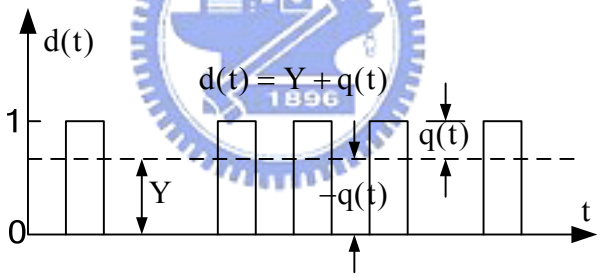


Fig. 4.11 Output waveform of decimal(t)

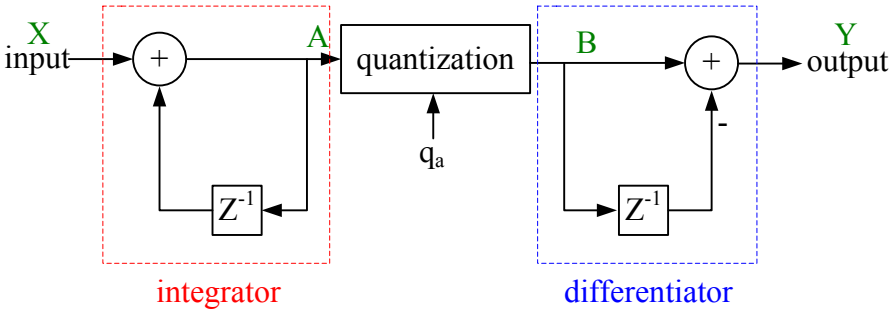


Fig. 4.12 Original ΣΔ modulator block diagram

The idea of ΣΔ modulator is to use an integrator and a differentiator, as shown in Fig. 4.12. The equation describe that the signal is through to the output, while the quantization noise is filtered by a high pass filter. The below equation is the transfer

function.

$$X + A z^{-1} = A \tag{4.3}$$

$$\therefore A = \frac{1}{1 - z^{-1}} X \tag{4.4}$$

$$B = A + q_a = \frac{1}{1 - z^{-1}} X + q_a \tag{4.5}$$

$$B - B z^{-1} = Y \tag{4.6}$$

$$\therefore Y = B(1 - z^{-1}) = \left(\frac{X}{1 - z^{-1}} + q_a\right)(1 - z^{-1}) = X + q_a(1 - z^{-1}) \tag{4.7}$$

The original ΣΔ modulator encounters overflow problem. In order to solve this problem, we can put subtraction of differentiator to the input as a negative feedback system and the transfer function does not change. However, the quantization just passes the differentiator and its power is lowered at signal band. Besides, the feed-back circuit is more stable than the feed-forward circuit. Fig. 4.13 shows the improved ΣΔ modulator and the continuous is the transfer function.

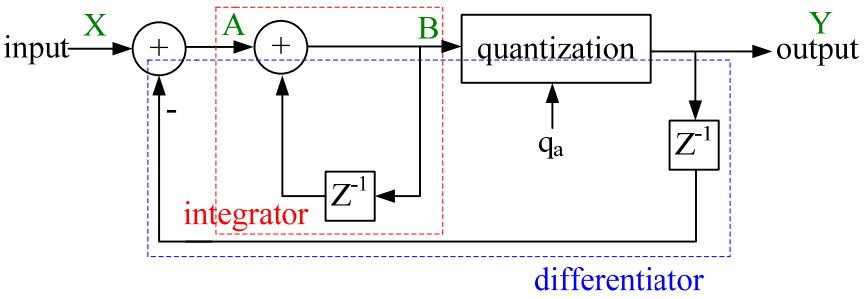


Fig. 4.13 Improved ΣΔ modulator block diagram

$$B = \frac{1}{1 - z^{-1}} A \ , \tag{4.8}$$

$$Y = \frac{\frac{1}{1-z^{-1}}}{1+\frac{1}{1-z^{-1}}z^{-1}} \times X + \frac{1}{1+\frac{1}{1-z^{-1}}z^{-1}} \times q_a \qquad (4.9)$$
$$= X + (1-z^{-1})q_a$$

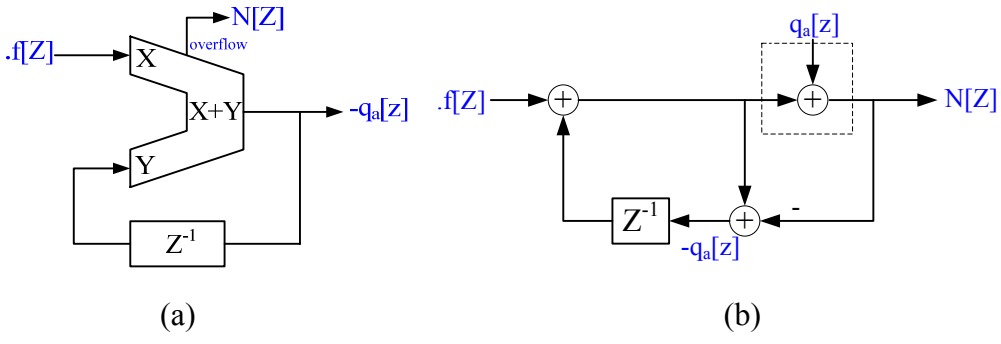
We can get the final transfer function in z domain as follows:

$$output = input + (1+Z^{-1})q_a, \qquad (4.10)$$

where q_a is the quantization. The implementation of ΣΔ modulator can be achieved by the accumulator. Fig. 4.14(a) shows the architecture of the accumulator and Fig. 4.14(b) shows its block diagram. In the same way, we can derive its transfer function in Eqn.(4.4), which is the same as Eqn.(4.3).

$$N[Z] = .f[Z] + (1+Z^{-1})q_a[Z] \qquad (4.11)$$
$$= .f[Z] + qe[Z]$$

The output DC value is $.f[Z] = \frac{A}{2^B} = \frac{A}{M}$ (Eqn. 4.2), where A is the input of the accumulator, B is the bit number of the accumulator and M is the maximum magnitude of the accumulator.



(a) (b)

Fig. 4.14(a) ΣΔ modulator using accumulator (b) Block diagram of ΣΔ modulator

Fig. 4.15(a) is the output waveform of the accumulator. Fig. 4.15(b) is the output waveform of the quantization error .We can see the overflow is either 0 or 1. The qe[z] will compensate the difference value. As shown in Fig. 4.16, we can

incorporate the ΣΔ modulator in the PLL to control the MUX modulus.

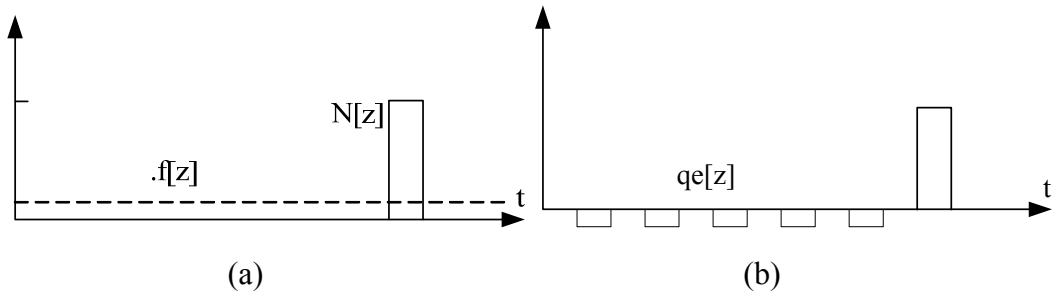


Fig. 4.15 Output waveform of (a) the accumulator (b) the quantization error

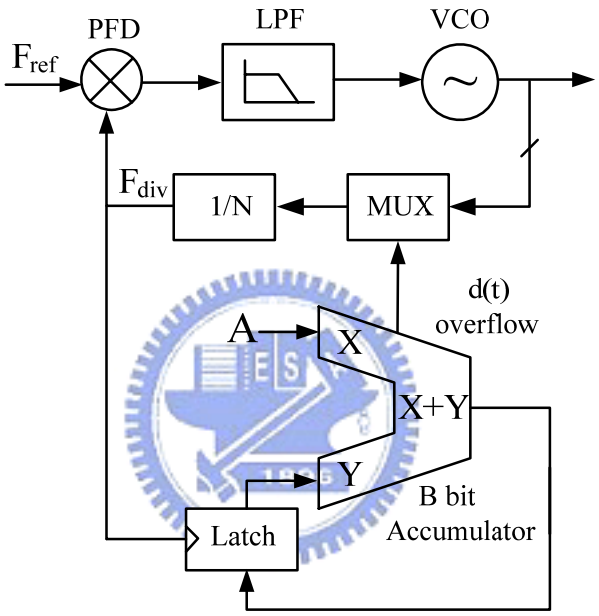


Fig. 4.16 Realization of ΣΔ modulator

It can be seen that, for a N-bit accumulator, the accumulator will produce an overflow on average $A/2^B$ every cycle of the F_{div} clock. Thus the average jumping phase is

$$J_{avg} = \frac{A \cdot \left(1 + \frac{1}{P}\right) + \left(2^B - A\right) \cdot 1}{2^B} = 1 + \frac{A}{2^B \times P} \tag{4.12}$$

To get more insight into ΣΔ modulator, we should analyze it in analytic function. The optimal output signal of divider is in equation:

$$f_{div} = f_{ref} = \frac{f_{out}}{N \times (1 + A/(2^B \times P))} = \frac{f_{out}}{N'} \tag{4.13}$$

And the actual frequency of divider is

$$\begin{aligned} f_e &= \frac{f_{out}}{N + A \cdot N/(2^B \times P) + qe(t)} \\ &= \frac{f_{out}}{N' + qe(t)} \end{aligned} \tag{4.14}$$

The normalized frequency error is

$$f_{diff}(t) = \frac{f_{div} - f_e(t)}{f_{div}} = 1 - \frac{1}{1 + \frac{qe(t)}{N'}} \cong \frac{qe(t)}{N'} \tag{4.15}$$

The quantization phase noise is

$$\theta_e(t) = 2\pi \cdot \int (f_{div} - f_e)dt = 2\pi \cdot \frac{f_{ref}}{N'} \cdot \int qe(t)dt \tag{4.16}$$

$$\theta_e'(t) = 2\pi \cdot \frac{f_{ref} \cdot qe(t)}{N'} \tag{4.17}$$

So the power spectral density of $\theta_e(t)$ is

$$S_{\theta_e}(f) = \frac{1}{(2\pi f)^2} \cdot S_{\theta_e'}(f) = \left(\frac{f_{ref}}{f \cdot N'}\right)^2 S_{qe}(f) \tag{4.18}$$

Now we recall that

$$qe[Z] = (1 + Z^{-1})q_a[Z], \quad q_a[Z] = \frac{1}{12 f_{ref}} \text{ [31]} \tag{4.19}$$

The noise transfer function in the discrete time domain can be converted into the continuous time domain by the following method.

$$|H(f)| = \sqrt{\left|\left(1 - Z^{-1}\right)\right|^2}\Bigg|_{z = e^{\frac{-j2\pi f}{f_{ref}}}} = 2\sin\left(\frac{\pi f}{f_{ref}}\right) \tag{4.20}$$

From Eqn.(3.11), we can get the final power spectral density of quantization noise is

$$S_{\theta_e}(f) = \frac{f_{ref}}{3\left(f \cdot N'\right)^2} \cdot \sin^2\left(\frac{\pi f}{f_{ref}}\right) \tag{4.21}$$

In order to obtain effectively the noise shaping toward the higher frequency, the higher order ΣΔ modulator is required. Fig. 4.17 and Fig. 4.18 show the Implementation and block diagram of 2nd order ΣΔ modulator. Thus we can get its transfer function as below:

$$N1[z] = .f[z] + \left(1 - z^{-1}\right) q_{a1} \tag{4.22}$$

$$N2[z] = -q_{a1} + \left(1 - z^{-1}\right) q_{a2} \tag{4.23}$$

$$\begin{aligned} N[z] &= N1[z] + \left(1 - z^{-1}\right) N2[z] \\ &= .f[z] + \left(1 - z^{-1}\right)^2 q_{a2}[z] \end{aligned} \tag{4.24}$$

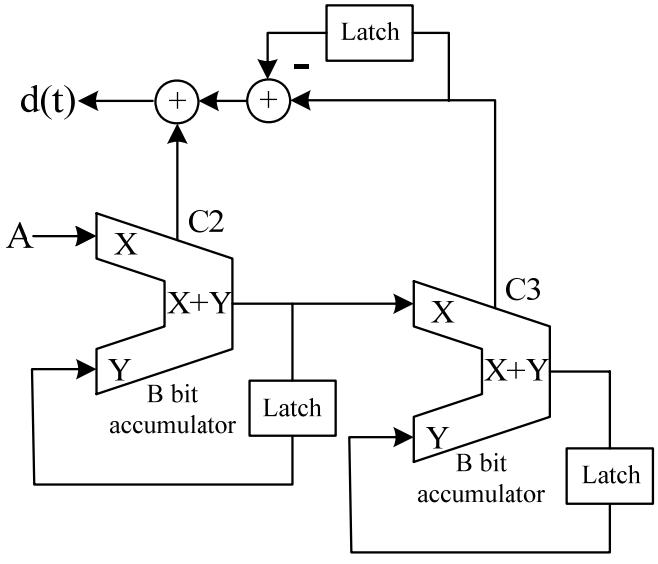


Fig. 4.17 Implementation of 2nd order ΣΔ modulator

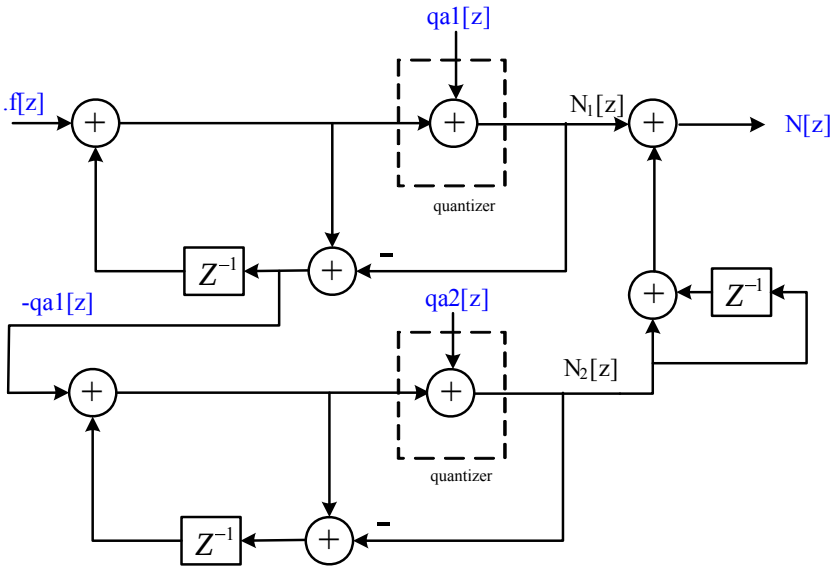


Fig. 4.18 Block diagram of 2nd order ΣΔ modulator

Fig. 4.19 shows the common 3rd order ΣΔ modulator: Multi-Stage Noise Shaping 1-1-1 (MASH 1-1-1)[32][33]. The block diagram is shown in Fig. 4.20. Thus we can get its transfer function.

$$N1[z] = .f[z] + (1 - z^{-1}) q_{a1} \tag{4.25}$$

$$N2[z] = -q_{a1} + (1 - z^{-1}) q_{a2} \tag{4.26}$$

$$N3[z] = -q_{a2} + (1 - z^{-1}) q_{a3} \tag{4.27}$$

$$\begin{aligned} N[z] &= N1[z] + (1 - z^{-1}) N2[z] + (1 - z^{-1})^2 N3[z] \\ &= .f[z] + (1 - z^{-1})^3 q_{a3}[z] \end{aligned} \tag{4.28}$$

Similarly, we can also change the noise transfer function to $H(f) = (1 - Z^{-1})^3$ and get the final power spectral density of output noise.

$$S_{\theta_e}(f) = \frac{16 f_{ref}}{3 (f \cdot N')^2} \cdot \sin^6 \left(\frac{\pi f}{f_{ref}} \right) \propto f^4 \tag{4.29}$$

The output PSD is now proportional to f^4, revealing that the quantization noise is suppressed in the signal band. As in general formula, if we use the i^{th} order ΣΔ

modulator, the PSD of the phase noise is [34]

$$S_{\theta_e}(f) = \frac{f_{ref}}{12(f \cdot N')^2} \cdot \left[2 \sin\left(\frac{\pi f}{f_{ref}} \right) \right]^{2i} \quad rad^2/Hz \qquad (4.30)$$

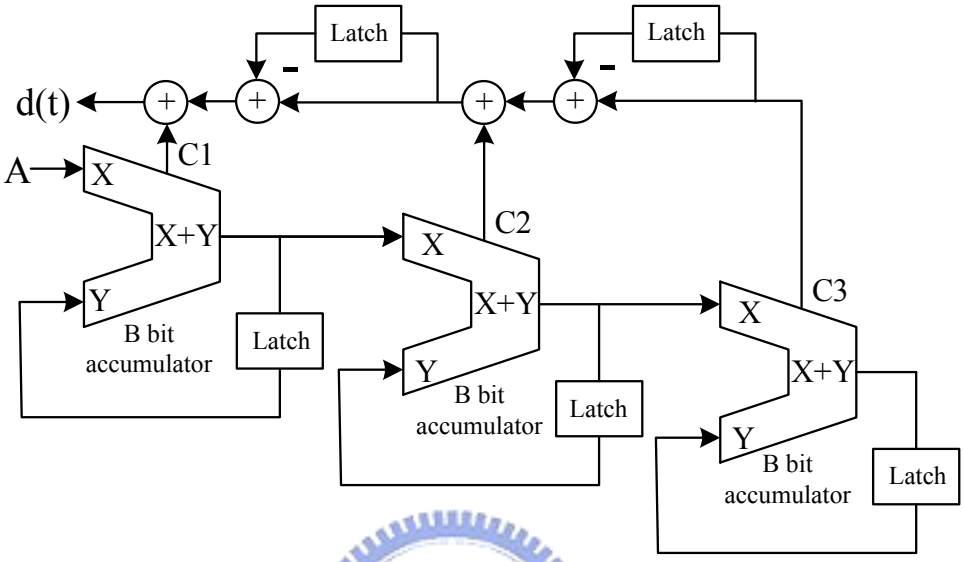


Fig. 4.19 Implementation of 3rd order ΣΔ modulator

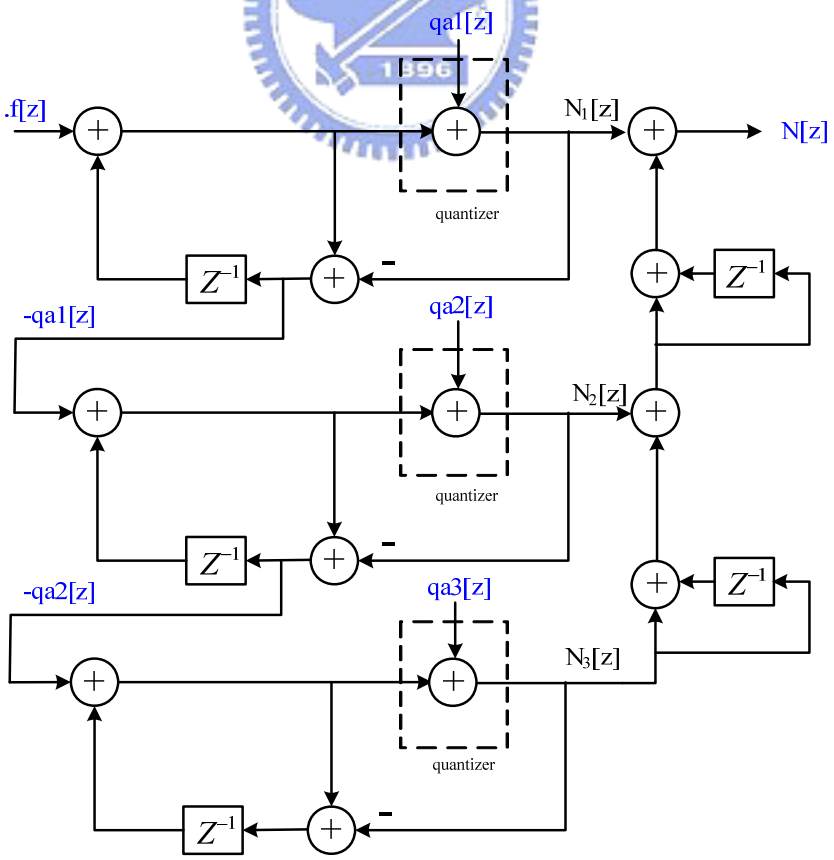
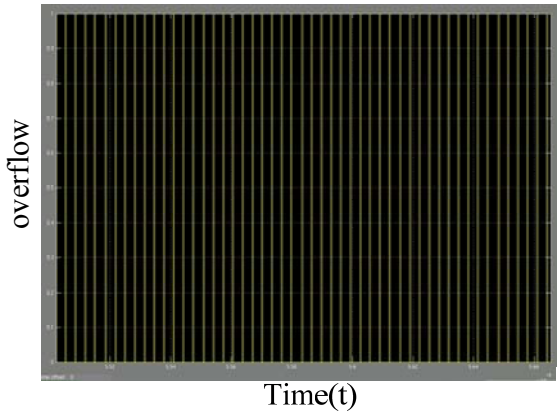
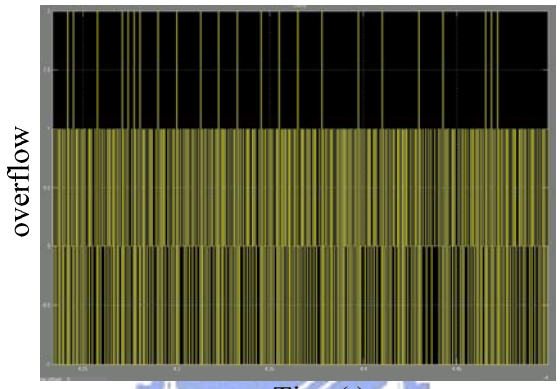


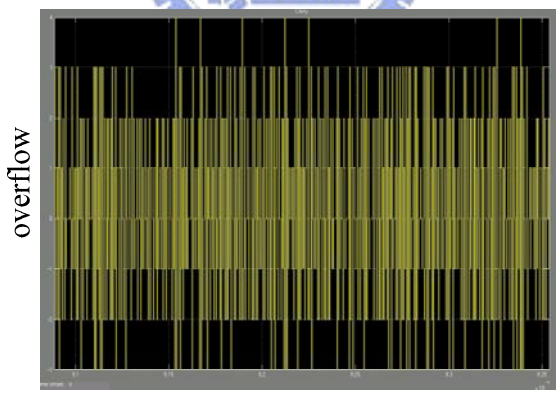
Fig. 4.20 Block diagram of 3rd order ΣΔ modulator



(a)



(b)



(c)

Fig. 4.21 d(t) of (a) 1st order ΣΔ modulator (b) 2nd order ΣΔ modulator (c) 3rd order ΣΔ modulator

Fig. 4.21 shows the output of ΣΔ modulators. We can observe the output is more highly changeable of the higher order ΣΔ modulator. Thus, the higher order ΣΔ modulator can move the quantization noise to higher frequency and the low pass

characteristic of PLL can filter out the noise.

Chapter 5

Spread Spectrum Clock Generator

5.1 Introduction

In general, PLL can generate a stable clock to control operations, but have problems about timing jitter. PLLs with a low jitter output clock is an important issue in all communication systems. In this chapter, a low jitter phase-lock-loop (PLL) and a programmable spread-spectrum clock generator (SSCG) for Serial ATA using switching phase is presented. Low jitter PLL is achieved through VCO with low KVCO by using medium-threshold-voltage PMOS and passive resistance. The spectrum in the clock generator can be spread by 10 phases or 20 phases. Our SSCG for Serial ATA Specification is down spread 5000 ppm with a triangular waveform of modulation frequency 30~33KHz. The proposed circuit is fabricated in a 0.18-um CMOS process. The non-spread spectrum clocking has a peak to peak jitter of 20ps and the maximum EMI reduction is -17.8dB in 20 phase spread spectrum mode which the power dissipation is only 28mw.

5.2 System architecture

The architecture of the programmable spread spectrum clock generator using

switching phase based on modify ΣΔ modulator is shown in Fig. 5.1. As implied by the name in this design, we can choose the SSCG spreading in 10 or 20 phases depending on the system specification. The advantage of spreading spectrum in 10 phases is power saving. The advantage of spreading spectrum in 20 phases is lower timing jitter.

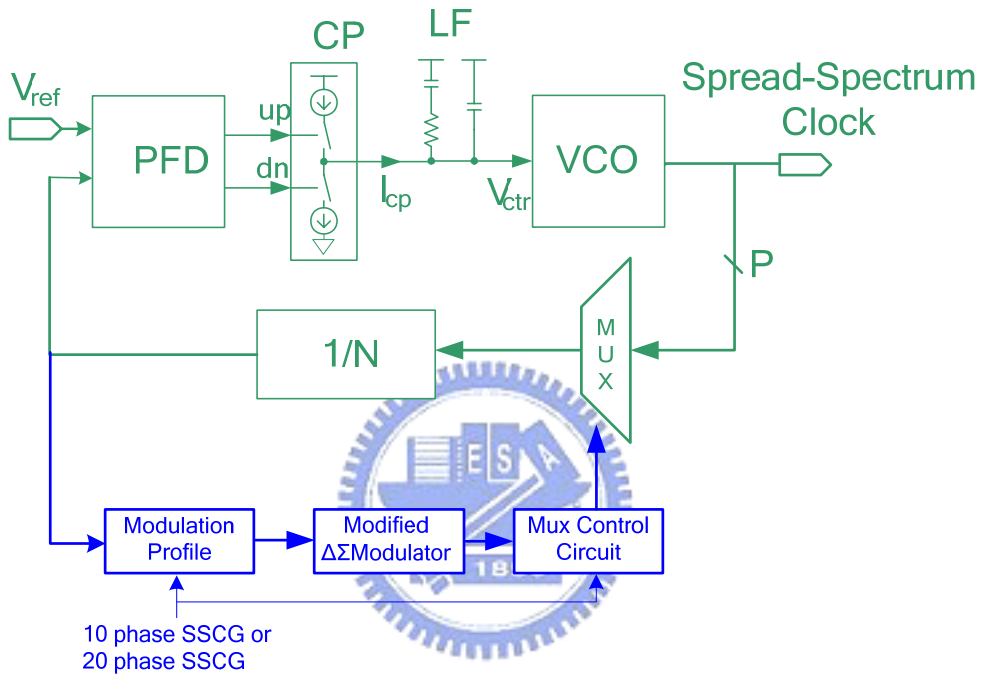


Fig. 5.1 The architecture of SSCG based on switching phase

The programmable SSCG is consists of PFD, CP, LF, VCO, MUX, divider, modulation profile generator, modified delta-sigma modulator and MUX control circuit.

Programmable modulation profile generator generate a proper periodic triangular profile into the modified ΣΔ modulator to generate number of phase jumping fed to the MUX control circuit to select MUX output. The advantage of using ΔΣ modulator is that it can shape the noise to a higher frequency and smooth effect of the PLL loop and results in continuous frequency modulation from a discrete staircase input.

Proper controlling of programmable modulation profile generator can control

modulation frequency and modulation deviation. The method we use to spread spectrum to fit with the specifications of serial-ATA 6Gbps version which is describe in the following sections.

If the output of modified ΣΔ modulator is 0, the MUX control circuit choose the original phase as the MUX output signal, then $f_{spread} = N \times f_{ref}$ where $f_{spread} = f_{nonspread}(1.2GHz)$, $f_{ref} = 100MHz$. When the output of modified ΣΔ modulator is 1, the MUX chooses an early phase (because of down-spread) as output signal and $f_{spread} = f_{ref}(N - \frac{1}{P})$, where P is the number of phase. For the same reason, if the output is 2: $f_{spread} = f_{ref}(N - \frac{2}{P})$. As we know, the relationship between input and output of ΣΔ modulator is A/M, where A is the input number of the modulator, M is the maximum magnitude of the accumulator in the modulator. Thus, we have:

$$f_{spread} = f_{ref}(N - \frac{A/M}{P})$$

$$= f_{nonspread}(1 - \frac{A/M}{N \times P}) \qquad (5.1)$$

,where m runs periodically through 0, 1, 2,…, A, A-1, …, 2, 1, 0. Thus the f_{spread} will change between two different specified frequencies (Fig. 5.2).

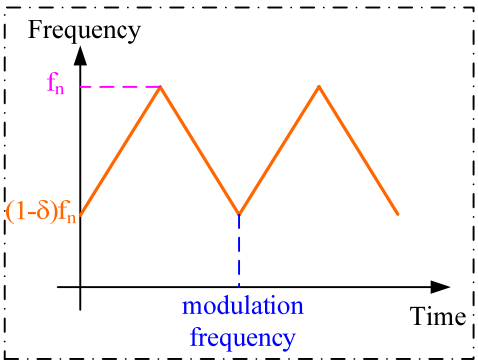


Fig. 5.2 The variation of frequency in spread spectrum

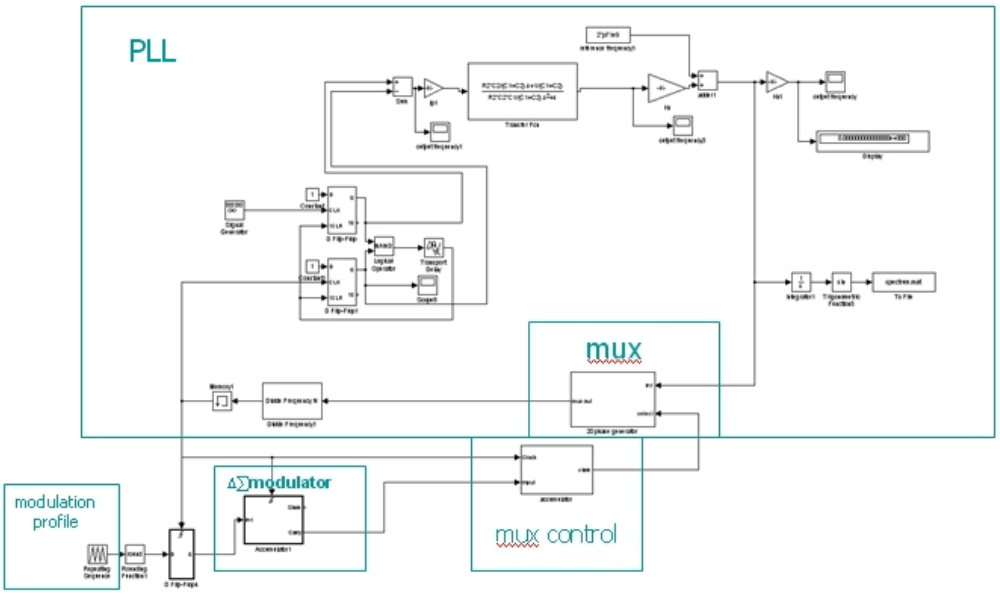
In order to conform with Serial-ATA specification (Table 5.1), we choose 5-bits accumulator to construct the modified ΣΔ modulator ($M = 2^B = 2^5$). In every modulation period ($30 \sim 33us$), we set A to be 19 to achieve -5000 ppm spread spectrum frequency range (in the situation of P=10, N=12, M=32, modulation deviation= $-\frac{A/M}{N \times P} = -\frac{19/32}{12 \times 10} = -4947.9ppm$). Moreover, if we want to decrease the jitter, we can use interpolators to produce 20 phases from 10 phases in 5 stage delay cells. Then, we can also spread spectrum in 20 phases by setting A=38 to fit with modulation deviation -5000ppm (modulation deviation = $-\frac{A/M}{N \times P} = -\frac{38/32}{12 \times 20} =$ -4947.9ppm). Other frequency between 0 to -5000ppm will also be generated by alternating the amount of input number to generate different frequency.

Table 5.1 SSCG in Serial-ATA specifications

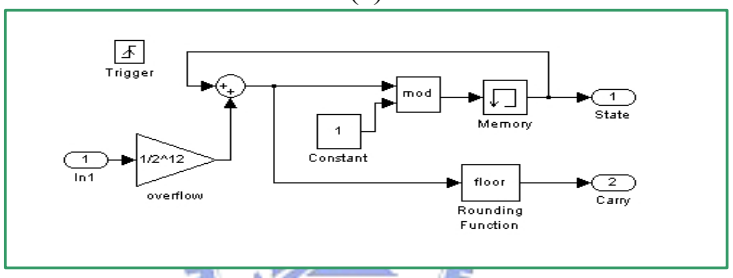
SSCG Parameter	Limit	Range
Spread Spectrum Modulation Frequency	Min	30KHz
	Max	33KHz
Spread Spectrum Modulation Deviation	Min	-5000ppm
	Max	0ppm

5.3 Behavior Simulation

Because of the great amount of gates counts in the phase-locked loop, the closed-loop simulation with HSPICE will take a lot of time. In order to rapidly and approximately know the behavior of PLL, we use SIMULINK to test and verify system parameters and transient response. Furthermore, we can observe the way the frequency of VCO is locked and the spectrum of the output of VCO is spread. Finally, we can design our chip according to the parameters in SIMULINK. Fig. 5.3 shows the SSCG behavioral model built in SIMULINK.



(a)



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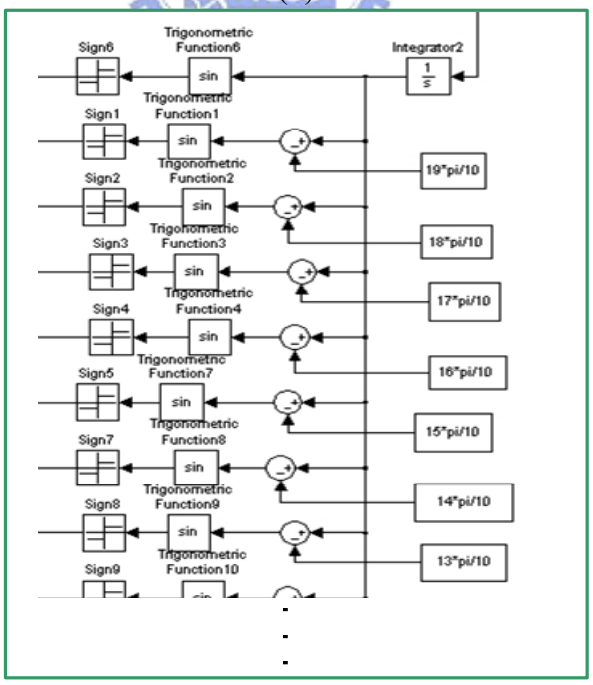
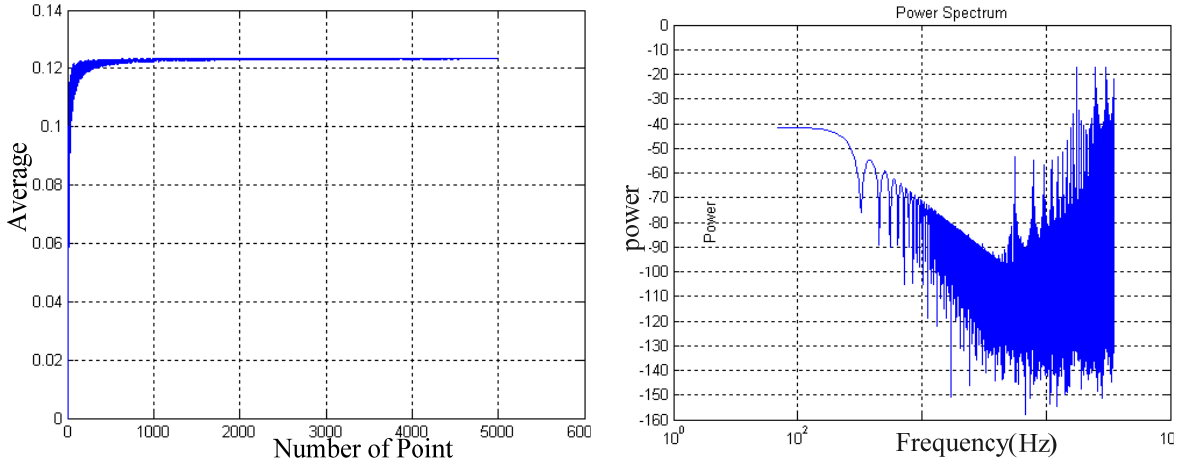


(c)

Fig. 5.3 SIMULINK model of the SSCG (a) SSCG based on the PLL

(b) 1st order ΣΔ modulator (c) Multi-phases generator

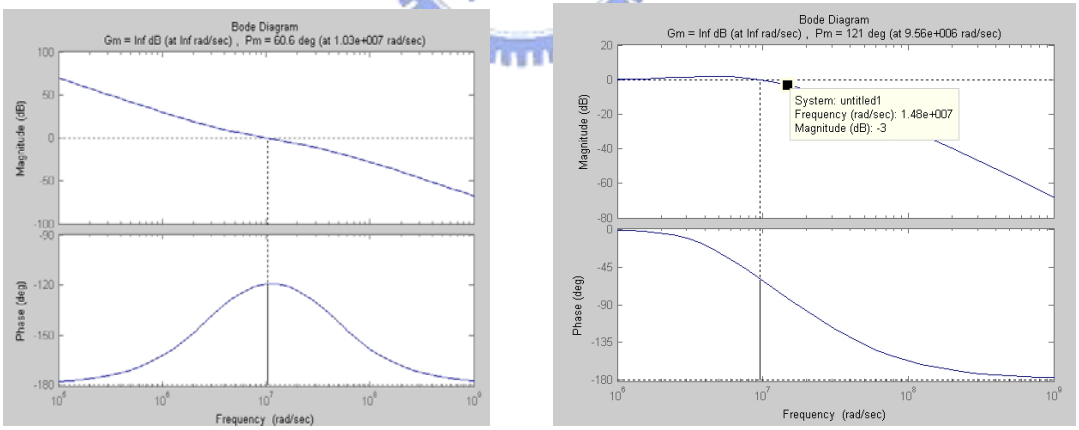
Fig. 5.4 shows the average output of 1st order ΣΔ modulator and the PSD of 1st order ΣΔ modulator



(a) (b)

Fig. 5.4 (a) Average output (b) PSD of 1st order ΣΔ modulator

Fig. 5.5 is the open loop Bode plot and close loop Bode plot respectively. We can observe that the phase margin is 60.6° and f_{3db}=14.8M rad/s /2π =2.35MHz.

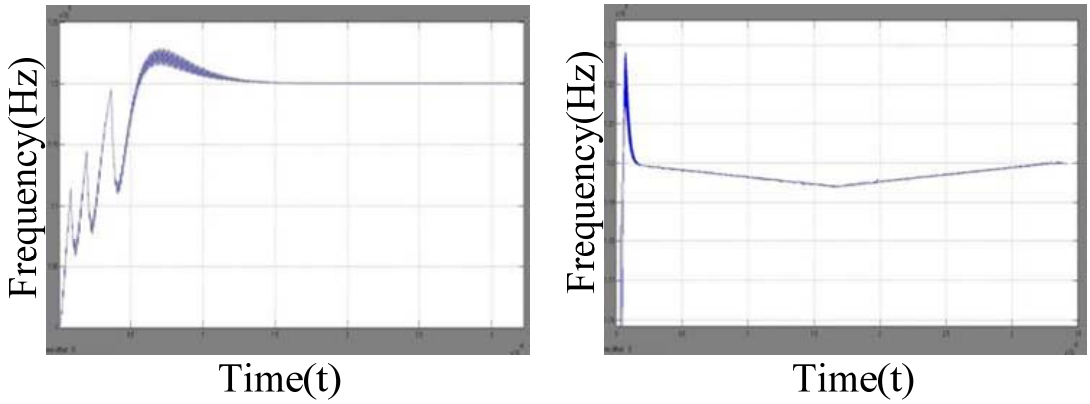


(a) (b)

Fig. 5.5 Frequency response of (a) Open Loop Bode Plot (b) Close Loop Bode Plot

Fig. 5.6 shows the transient response of the PLL without and with spread spectrum respectively. We can see the frequency in Fig. 5.6(a) is locked and stable. In Fig. 5.6(b), we use the built in blocks in the Matlab to construct the triangular

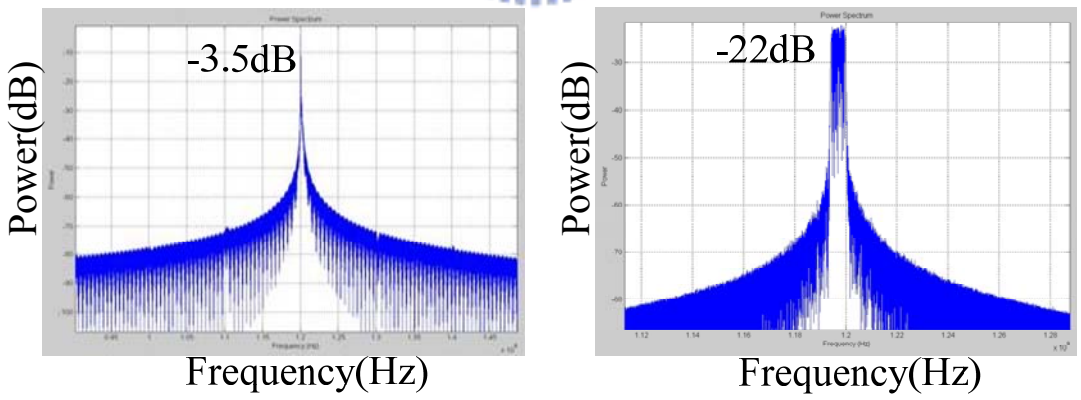
waveform to control the input of ΣΔ modulator. We can observe that the PLL also exhibit its frequency like a triangular waveform.



(a) (b)

Fig. 5.6 (a) Frequency of VCO without SSCG (b) Frequency of VCO with SSCG

Fig. 5.7 (a) and (b) is the spectrum of VCO in the PLL without and with SSCG. We can see the power spectrum at 1.2GHz is -3.5dB before spreading spectrum. After spreading spectrum, the power rapidly decrease to -22dB.



(a) (b)

Fig. 5.7 (a) Spectrum of VCO without SSCG (b) Spectrumof VCO with SSCG

5.4 Circuit Implementation

5.4.1 Phase / Frequency Detector

Fig. 5.8(a) show the most popular circuit of PFD, because it have advantage of low power, high speed, good dead zone effect, and good lock in phase and frequency. Because the behind charge pump need two different signals to drive, so the single to different circuit (Fig. 5.8(b)) is preserved. But there is different delay between these two paths (UP and UP_b), it will produce large sharp spikes on charge pump current [35]. So that we plus 1 transmission gate on the way of UP_b. Fig. 5.9 is the dynamic DFF we adopt. It has the advantages of avoiding charge sharing effect, reducing data dependence jitter, reducing spike, reducing pre-discharge and noise's influence effect, and optimizing critical path delay.

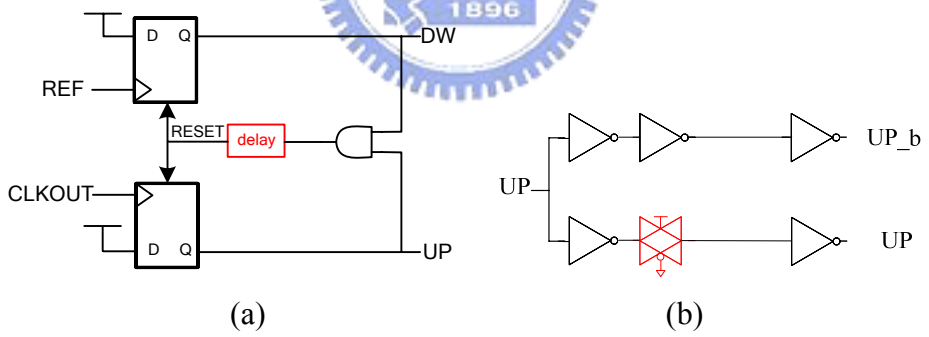


Fig. 5.8 Schematic of (a) PFD (b) Single to Different circuit

Fig. 5.10 is the timing diagram of PFD working operation. If the CLKOUT leads the REF, the UP signal will be high until the REF arrives. At the meantime, the RESET will produce a pulse signal to DFF to suspend charging or discharge. The charging time or discharge time is proportion to the phase difference between REF and CLKOUT. If the time difference between them is too small, owing to the finite rising time and falling time resulting from the capacitance, the pulse may not have

enough time to reach a logical high level, failing to turn on the charge pump switches. This is called dead zone. The dead zone would accumulate jitter. So we add the delay on the path of reset to have enough time to turn on MOS even the time difference is very small. Thus, zero dead zone is achieved (Fig. 5.11).

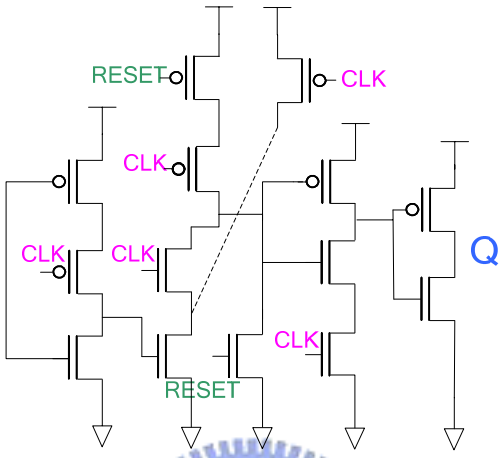


Fig. 5.9 Circuit of dynamic DFF

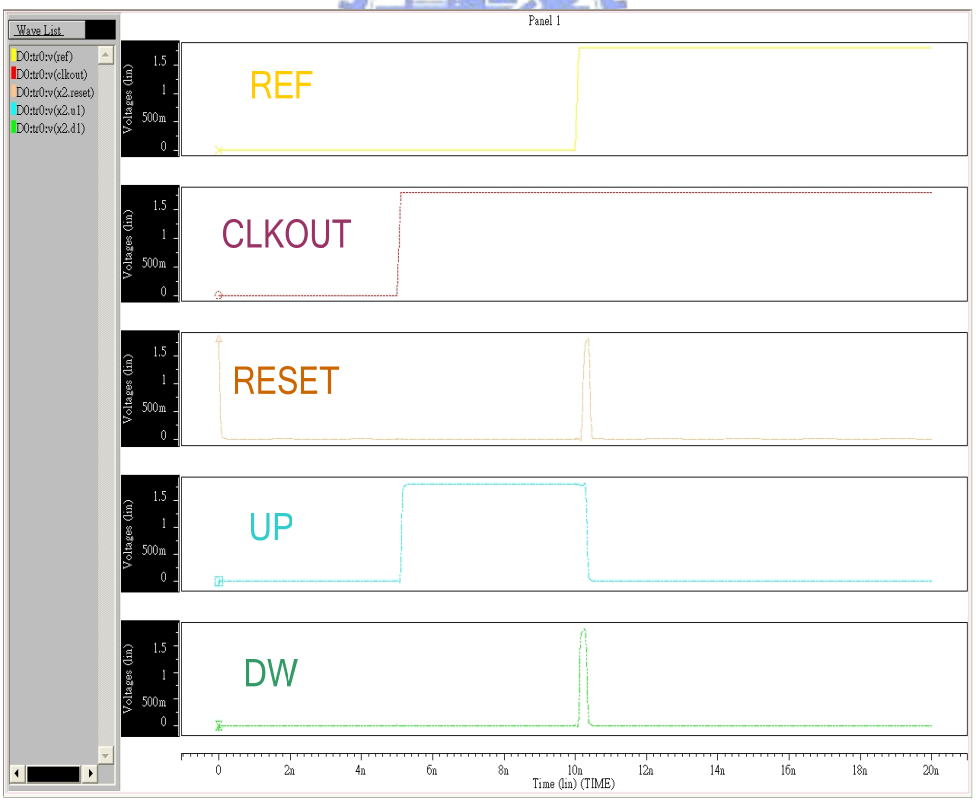
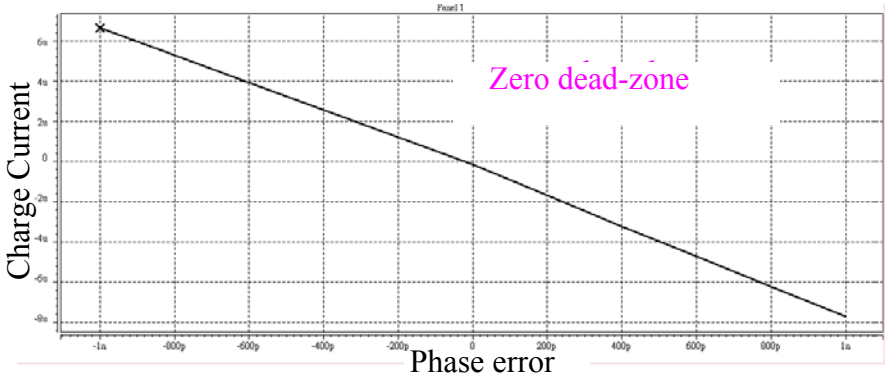


Fig. 5.10 Timing diagram of PFD



(a) (b)

Fig. 5.11 Timing diagram of Zero dead zone

5.4.2 Charge Pump

The charge pump (CP) is composed of current source and switches (Fig. 5.12). It converts digital signal from PFD into analog signal to control the amount of charging or discharging voltage which controlling the oscillator's frequency. Traditional charge pump (Fig. 5.12(a)) are popular before because they don't need an additional loop filter and offer low-power consumption with tri-state operation. However, it has many problems. For example, when the switches are OFF, the voltage at the output capacitor C_L is floating, while the voltages at the sources of PMOS and NMOS are rapidly pulled to VDD and GND respectively. Due to the non-ideal characteristics of the MOS switch, such as charge injection and clock feed-through, this rapid change in the source voltages creates glitches in the capacitor current, which results in a jump in the stored voltage V_C. Any jump in V_C adds undesirable spurious tones and phase noise to the output signal of the VCO. Besides, when the switches are OFF, the voltage at node X and Y are VDD and GND respectively and the output voltage V_C is floating. When the switches are turned ON, the voltage at node X will decrease and the voltage on node Y will increase, resulting in charge sharing between C_L, C_X

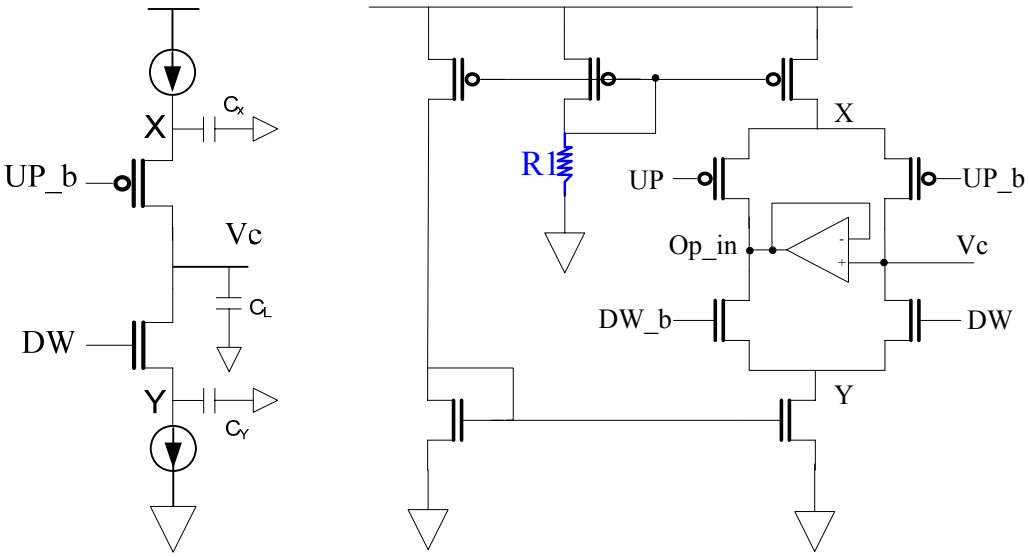
and C_Y, and a consequent deviation in the output voltage V_C. A possible approach is to add a unity gain amplifier as shown in Fig. 5.12(b)[36][37]. There are three main advantage of this approach:

1. The voltage at the X and Y is set to the voltage at the output node when the switches are turned off to reduce the charge sharing effect and charge injection when the switch is turned on.

2. There is always a way from VDD to GND, so the charging and discharging current is keep constant like we simulate in SIMULINK, not a variable value, for example, not from 0 uA to 30 uA or from 30 uA to 0 uA .

3. The charging current and discharging current are the same because they have the same current mirror.

However, the enhancing performance comes at the expense of extra complexity, area, and power consumption. Besides, the current is decided by the off-chip resistance (R1). We can adjust the value of resistance to get the best performance if there happens process variation.



(a) (b)

Fig. 5.12 (a) traditional charge pump (b) charge pump with active amplifier

As shown in Fig. 5.13, when CLKOUT arrives earlier than CLKOUT, the pulse width of UP_b will be longer than DW, causing there is net current charging the output capacitor and the V_C will arise and the frequency of CLKOUT will fall (in my design).

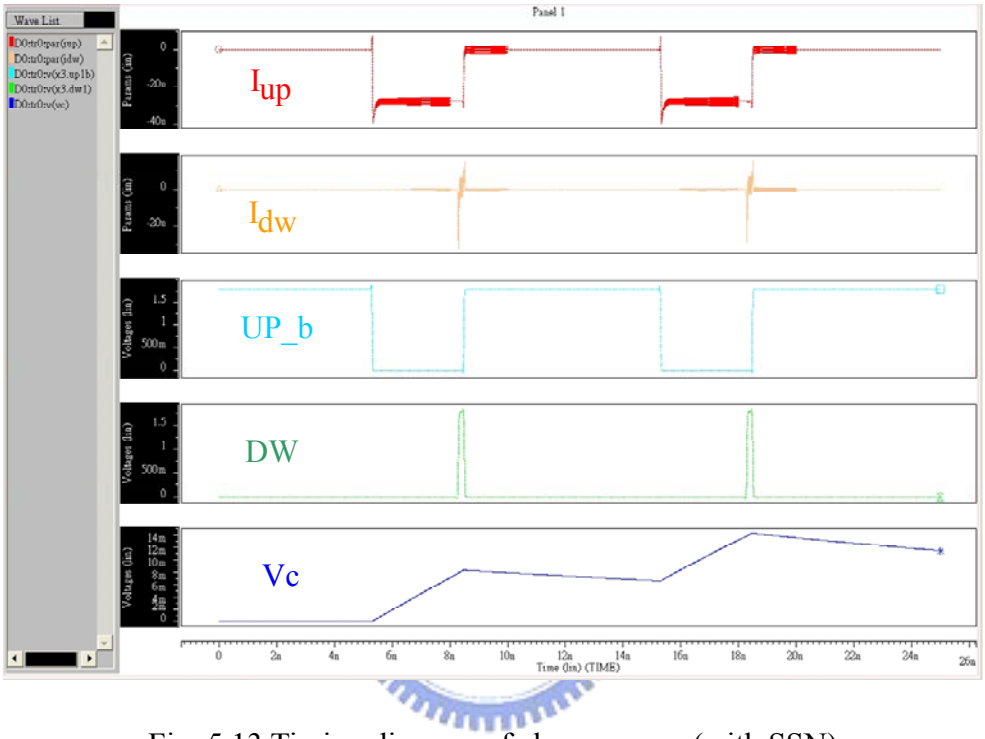


Fig. 5.13 Timing diagram of charge pump (with SSN)

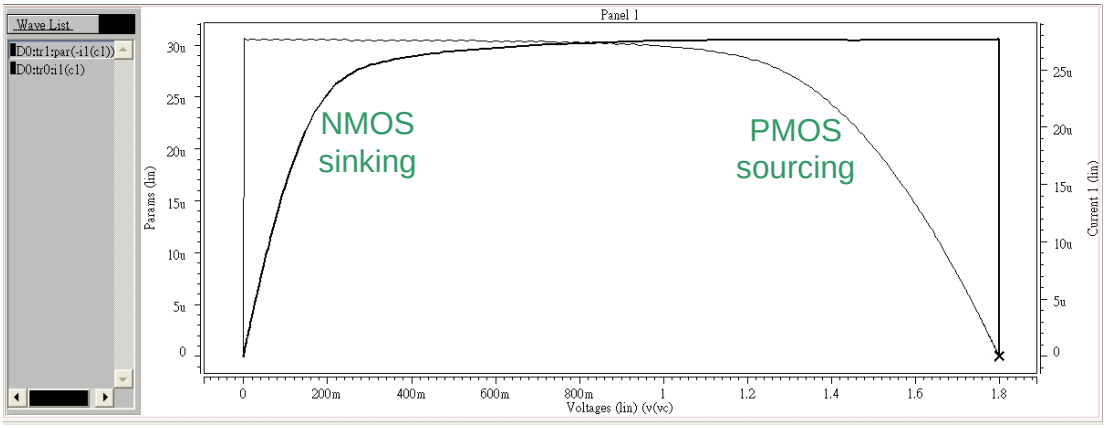


Fig. 5.14 Charge pump current matching characteristic

Fig. 5.14 compares the charging current and discharging current under various output voltages. It is obviously that they are only the same in a specific voltage because of the channel length modulation. We can ease the phenomenon by increase

the length of all transistors. Other method has been proposed by forcing the current of PMOS to be the same as that of NMOS [38].

5.4.3 Loop Filter

The usage of loop filter is to suppress the noise of V_C and determines the dynamic performance of the PLL. It filters out the high frequency voltage and passes the averaged value to the input of the VCO. The value of capacitance and resistance decide the stability and speed of PLLs. The value can neither too large nor too small because area and stability issue. In general, a second order or third order filter are commonly used. In our design, we adopt a second order filter (Fig. 5.15).

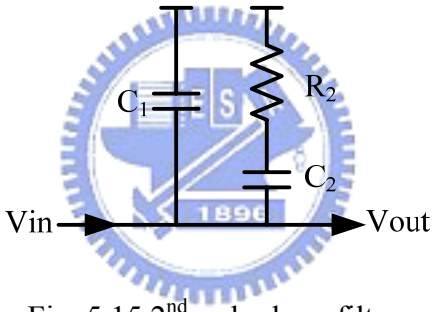


Fig. 5.15 2nd order loop filter

The C_1 is to suppress the spur of V_{in} and the C_2 and R_2 are to supply a zero in frequency domain. The relationship between zero, poles, reference clock and loop bandwidth are listed in Fig. 5.16. A good loop filter can also eliminate the effect of clock feed-through from the CP when it charge or discharge.

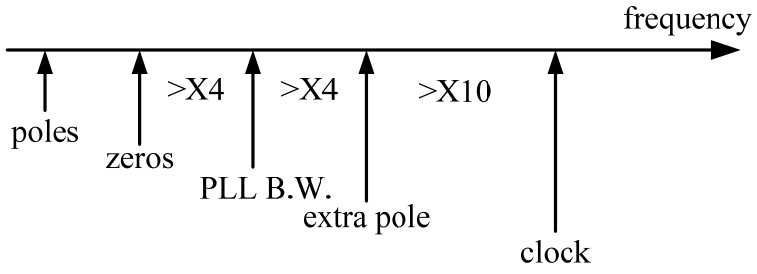


Fig. 5.16 Relationship between zero, poles, reference clock and loop bandwidth

5.4.4 Programmable Voltage-Controlled Oscillator

Voltage-Controlled Oscillators (VCO) is one of the most important elements in the PLL and critically determines the performance of a frequency synthesizer, such as loop gain, linearity, tuning range, central frequency and etc.

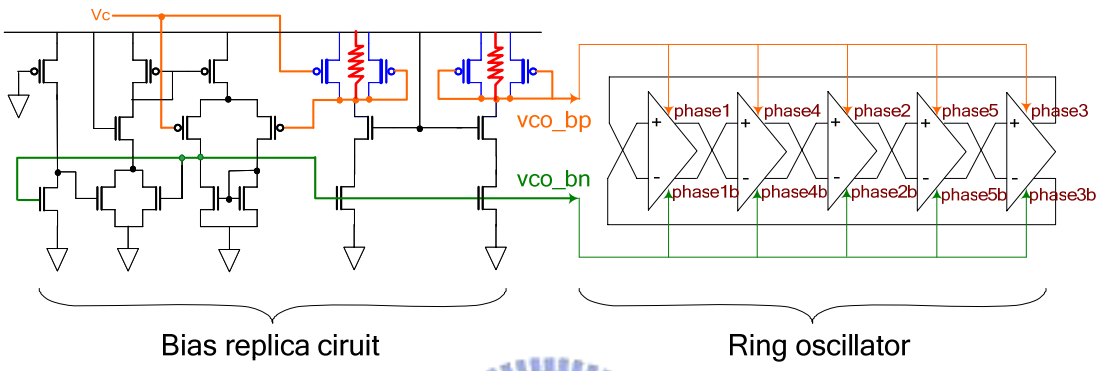


Fig. 5.17 Scheme of voltage control oscillator

In order to design a PLL used in Serial-ATA 6Gbps, we adopt a 5 stage ring oscillators which has 10 phases and oscillate in 1.2GHz. Fig. 5.17 is the schematic of the VCO structure.

Because the operation speed is very faster, we hope the jitter is less. There is an effective way to reduce jitter if we can decrease the K_{VCO}. There will be obvious spur in frequency domain even if a little jiggles in V_C if the K_{VCO} is large. The design below is to achieve this goal.

The basic bias replica circuit is presented in [39]. We use the medium-threshold PMOS and resistance instead of nominal-threshold PMOS in symmetric load (Fig. 5.18). The bias replica circuit translates V_C to vco_bp and vco_bn to bias the PMOS and NMOS in delay cells and copy the V_C to vco_bp. Because it isolates V_C from VCO, the noise in VCO will not affect V_C directly. The bias-replica circuit will have good behavior in anti-noise, anti-temperature variation, and anti-process variation.

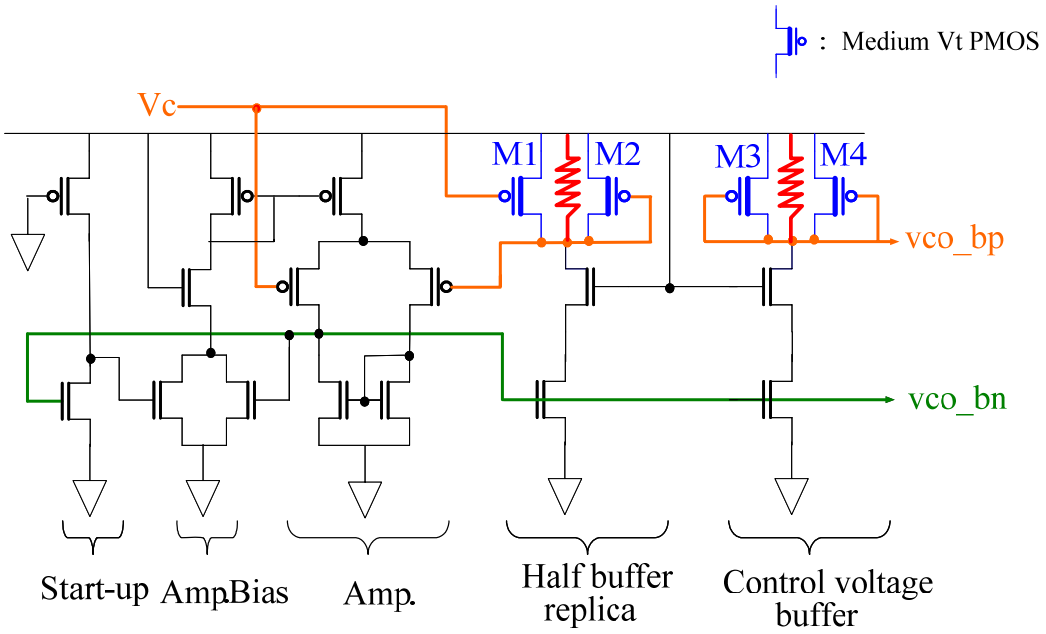


Fig. 5.18 Bias replica circuit

The basic delay call is presented in [40]. The delay cell is composed of a symmetric load and a voltage controlled current source. Similarly, we add the medium-threshold PMOS (M5~M8) and resistance (R1, R2) to replace nominal-threshold PMOS in symmetric load (Fig. 5.19(a)). The resistance variation ratio of the symmetric load is related with oscillating frequency variation (Kvco) seriously.

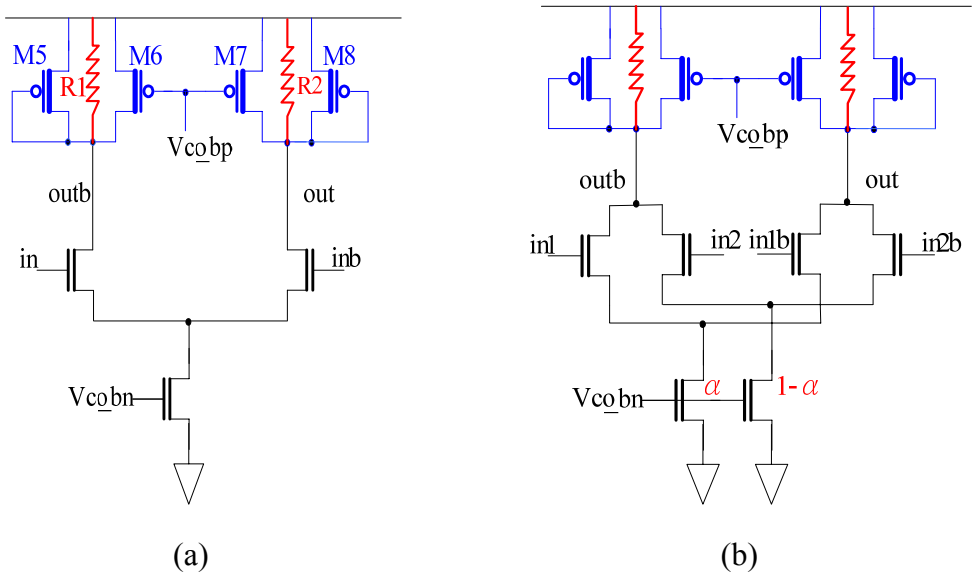


Fig. 5.19 (a) Delay cell (b)Interpolator

If the Kvco is high, there will be large jitter in the output of the VCO from the litter jiggle of the V_C. Thus, we want to have a low Kvco in our PLL. So we use the medium threshold PMOS transistors and passive resistance in the load of delay cells, interpolators and the bias replica circuit to achieve this goal. Table 5.2 is the comparison in PMOS and NMOS at various V_t. There are four mainly advantages in this design:

1. The working range in V_C will be larger: The medium threshold voltage (0.24v) PMOS in bias replica circuit (M1~M4 in Fig. 5.18) will work correctly even if the V_C higher. As a result, the Kvco will decrease because of large control voltage range of V_C.

2. Decreasing the process variation: We can decrease the process variation by increasing the gate length. But the oscillation frequency will not reach the frequency we need if we use normal threshold (0.51v) PMOS. So we can use medium threshold PMOS instead of normal threshold PMOS to raise the oscillator frequency and can also decrease the process variation (Fig. 5.19(a)).

3. Its operation will be in the deep saturation region: in this design, the medium threshold PMOS will work in more deep saturation region than in the normal threshold PMOS at the same frequency. In actual, the slope will be less and the Kvco will be smaller.

4. The passive resistance will decrease the velocity variation in the symmetry load: We add a proper passive resistance in the symmetric load. Although the speed will increase, the resistance variation will decrease. Consequently, the Kvco will be decreased again.

Table 5.2 PMOS and NMOS in 0.18um CMOS

	NORMAL Vt DEVICE	MEDIUM Vt DEVICE	NATIVE Vt DEVICE
Length range(um) (NMOS/PMOS)	0.18~20 / 0.18~20	0.3 ~10 / 0.25~10	0.5 ~20 / -----
Width range(um) (NMOS/PMOS)	0.22~900 / 0.22~900	0.22~100 / 0.22~100	0.22~100 / -----
Vt(approximate value) (V) (NMOS/PMOS)	0.51 / -0.5	0.24 / -0.24	0.03 / -----

Fig. 5.20 shows the characteristics of symmetric load and resistor to VCO. The current after adding resistor increases, in other words, the resistor decreases. Thus, the velocity variation decreases.

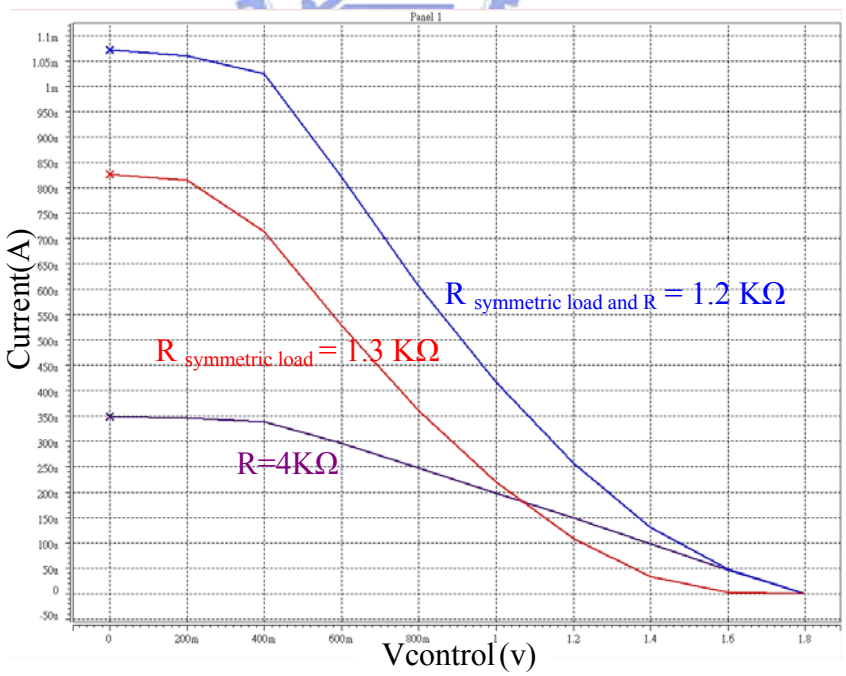
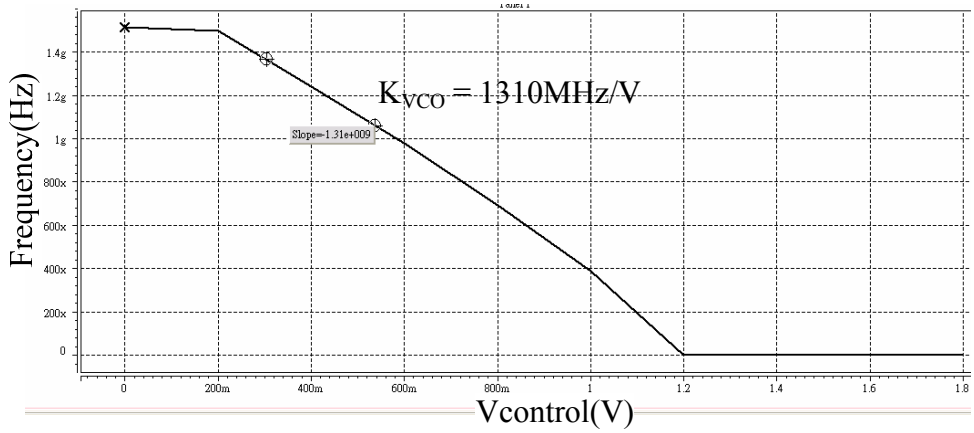
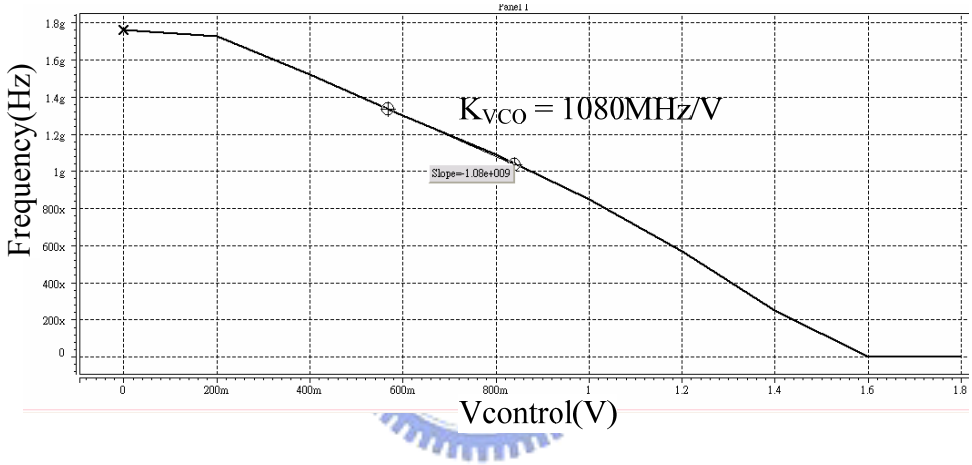


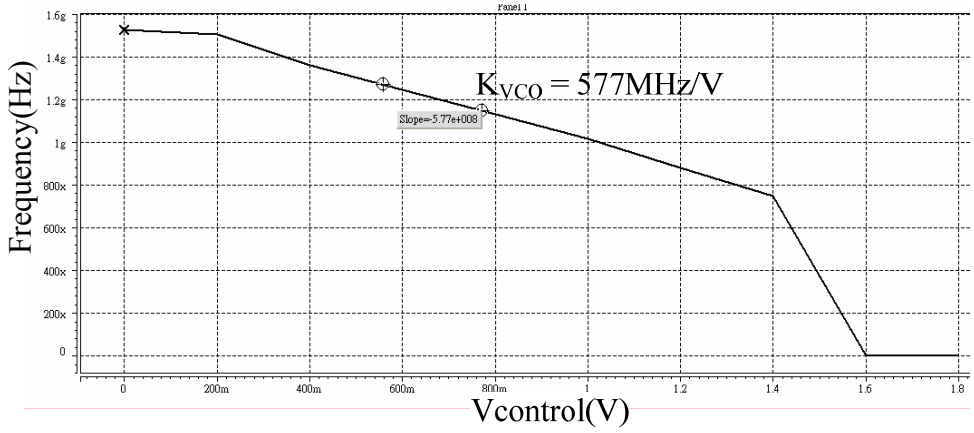
Fig. 5.20 characteristics of symmetric load and resistor to VCO



(a)



(b)



(c)

Fig. 5.21 Characteristics of VCO (a) with normal threshold PMOS (b) with medium threshold PMOS(c) with medium threshold PMOS and passive resistance in the symmetric load.

Fig. 5.21 is the frequency versus V_C curves. In the original circuit, the K_{VCO} is 1310MHz/V. Replaceing with medium threshold PMOS transistors, the K_{VCO} becomes 1080MHz/V. Finally, after we add passive resistors, the K_{VCO} decrease to 577MHz/V. The area and power is quite the same as the original design.

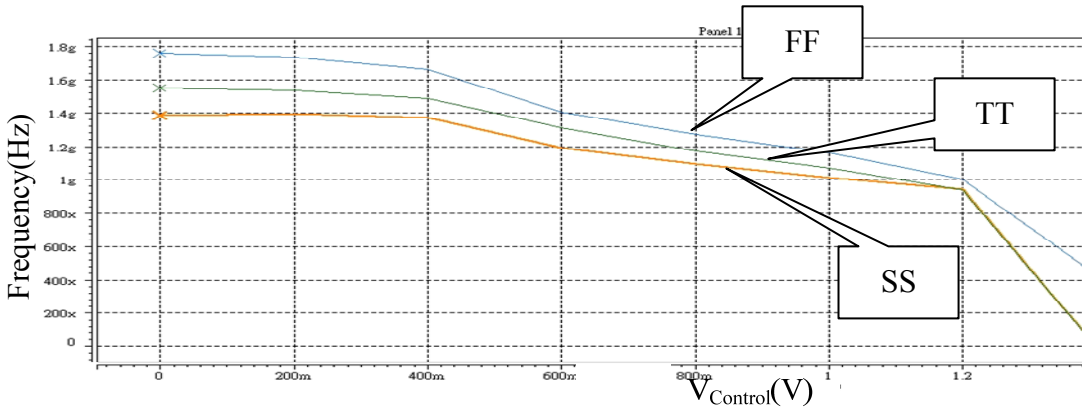


Fig. 5.22 Simulation results of the voltage-controlled oscillator

Fig. 5.22 shows the simulation of our final Kvco curve for different corner case. My central frequency is 1.2GHz at 0.74v in TT case. We can observe the frequency range covers 1.2GHz and Kvco is roughly 600MHz/V in each corner case. Furthermore, in order for the Kvco curve to cover 1.2GHz under the process variation or parasitic capacitance, we design the upper limit (1.6GHz) is double lower limit (1.0GHz).

In the SSCG aspect, we use interpolators (Fig. 5.19(b)) [41] to generate 20 phases so as to spread the spectrum in a more precise way. The current ratio α determines the interpolating phase to be near the leading phase or the lagging phase. When α is smaller than 0.5, the lagging phase controls large portion of current and dominates the interpolated phase. The size of interpolators should be the same as the delay cells. Fig. 5.23 is the diagram in the outputs of ring oscillators and interpolators. In our design, we use two bias circuits: one for ring oscillators, and another for interpolators. Thus, when we want to spread spectrum in 10 phases, we

can turn off the bias to shut down the interpolators to saving power. But this will cause more jitter in time domain. For example, there will be 8333ppm if jumping 1 phase in 10 phases SSCG ($\frac{1}{N \times P} = \frac{1}{12 \times 10}$). On the contrary, it only changes 4166ppm in 20 phases SSCG ($\frac{1}{N \times P} = \frac{1}{12 \times 20}$). Consequently, we can choose spread spectrum in 10 or 20 phases depending on our need, such as power saving or low jitter in time domain.

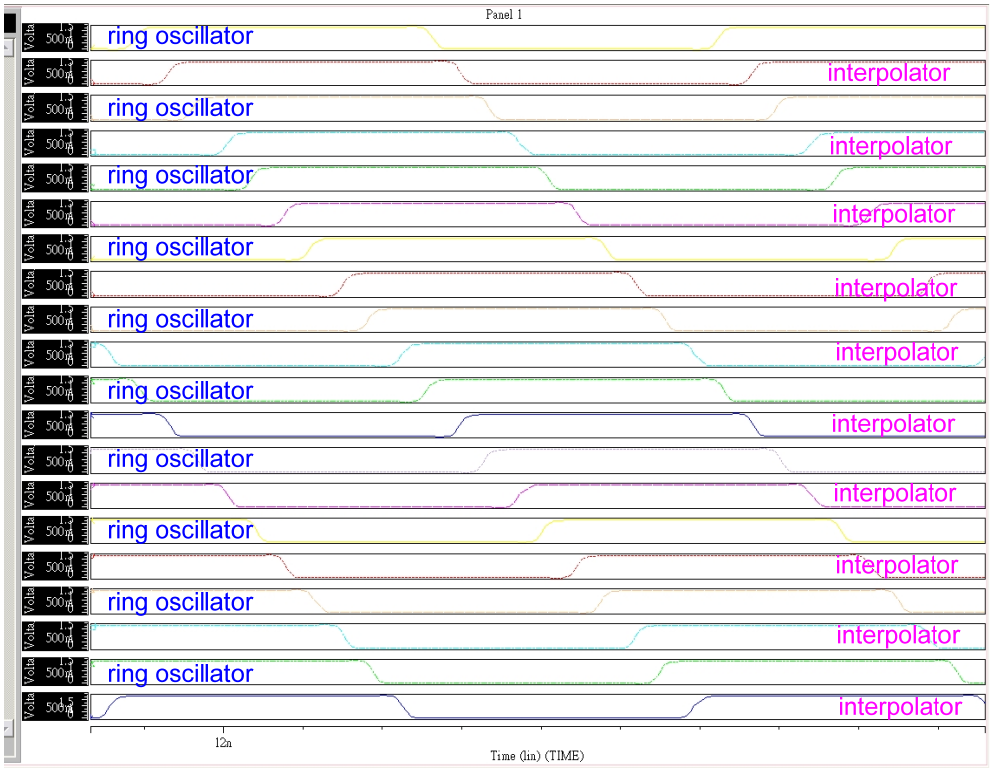
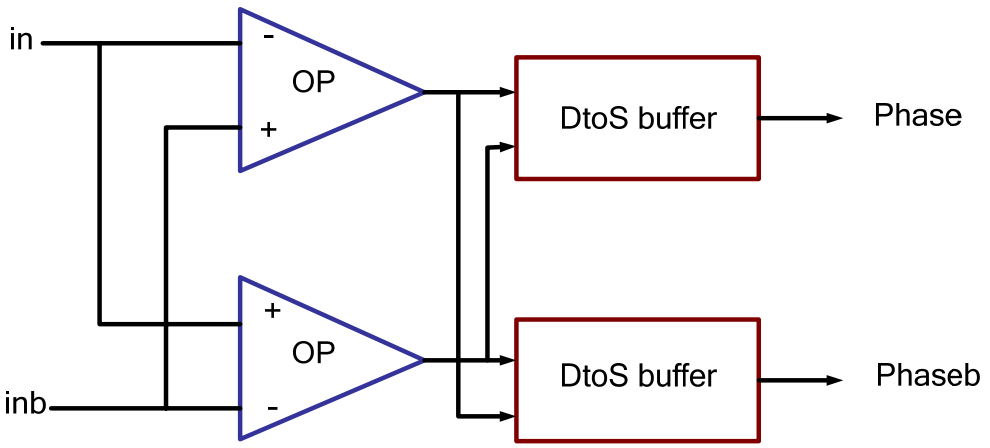


Fig. 5.23 Diagram of ring oscillators and interpolators



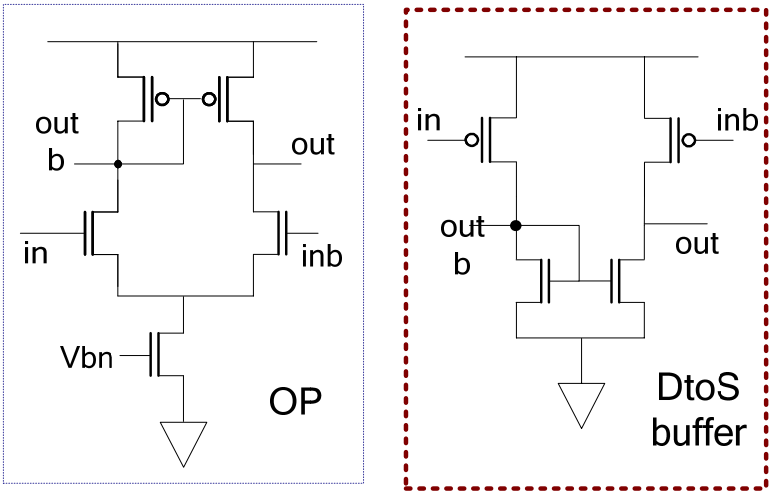


Fig. 5.24 VCO output buffer

The swing of the output in the delay cells will different for different V_C. In order that the divider behind the VCO will work correctly, the input wave should be full swing. We add the output buffer to the delay cells so that it will full swing and increase their driving ability (Fig. 5.24). The size of OP should be as small as possible to reduce the loading of delay cells. Fig. 5.25 is the diagram before and after buffer.

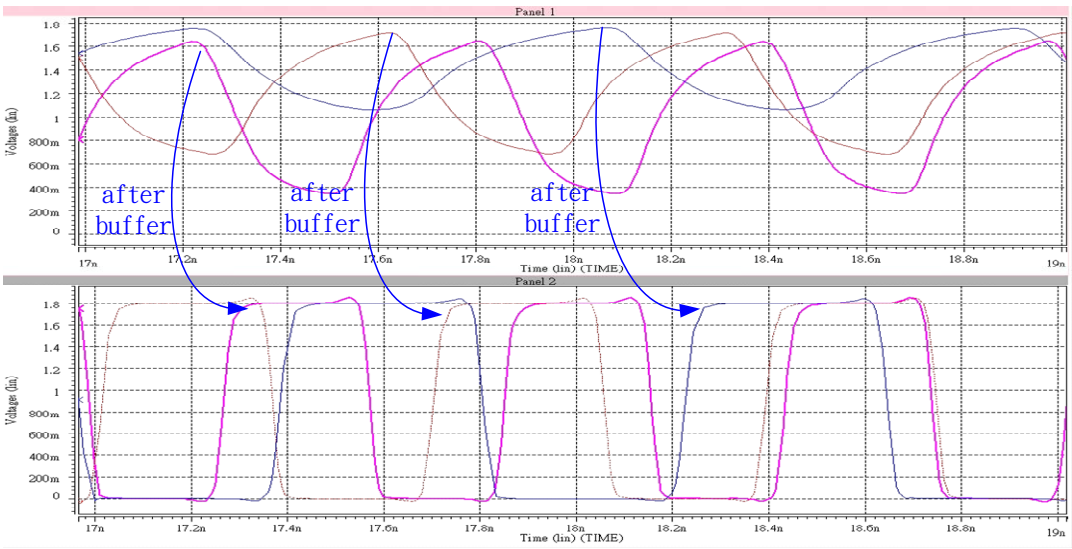


Fig. 5.25 Diagram of delay cell output and buffer output

5.4.5 Divider

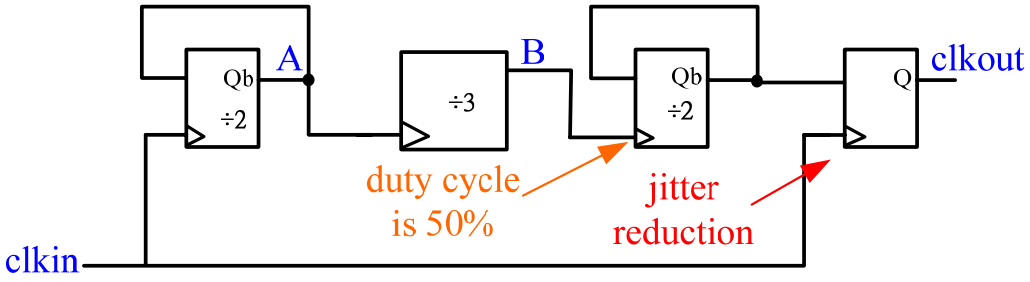


Fig. 5.26 Schematic of divider

Asynchronous divider has less power consumption but induces larger jitter due to jitter accumulation. On the contrary, synchronous divider has no accumulation but has larger capacitance loading. Because that REF is 100MHz and the output frequency is 1.2GHz, we need a circuit which can divide 12. Here we adopt a synchronous divider which divided by 3 and an asynchronous divider which divided by 2 (Fig. 5.26). Because asynchronous divider can spread the input jitter equally, we put the divider which is divided by 2 at the first stage. Then we can have duty cycle of 50% in the output wave, we put the same divider at the last stage. Hence, we put the divider which is divided by 3 at the middle stage. Finally, in order to reduce jitter accumulated by asynchronous circuit, we put a D flipflop after the divider. Fig. 5.27 is the timing diagram of the divider.

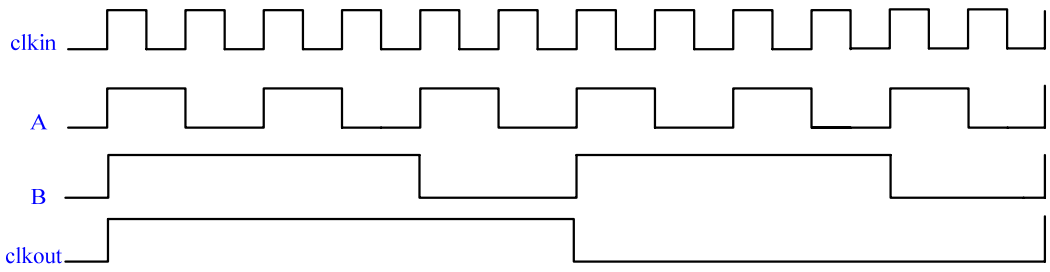


Fig. 5.27 Time diagram of divider

5.4.6 Programmable Modulation Profile Generator

The modulation profile will affect the energy distribution. From section 3.3.2, we know the triangular modulation profile can get the best spreading result because of its frequency deviation is regular in fixed time and the spectrum will almost be flattened. Actually, we use up/down counter to complete the triangular wave (Fig. 5.28). The Serial-ATA 6Gbps specifies the modulation frequency is 30~33KHz, and the modulation deviation is no more than 5000ppm down spread. In my circuit, the divider determines the modulation frequency of the SSCG, and the maximum number of this counter (19 and 38 mean the maximum value of the triangular) determines the modulation deviation of the SSCG. The divider in Fig. 5.28 can be implemented by another counter. This method can reduce the accumulation of jitter.

From section 5.2, we know modulation deviation in 10 phases SSCG $= -\frac{A/M}{N \times P}$ $= -\frac{19/32}{12 \times 10} = -4947.9\text{ppm}$, so the maximum number of the counter is 19. Thus, the totoal counting numbers are $19 \times 2 = 38$, so the divider in Fig. 5.28 can be 84 and the modulation can be within 30~33KHz (31.328KHz). The parameter in 20 phases SSCG is similar in this way.Table 5.3 is the parameter in 10 and 20 phases SSCG.

Below is the Boolean equation of the control circuit in the maximum number of wave:

$$\begin{aligned} F\_19 = {} & (S_0 S_1 \overline{S_2}\,\overline{S_3} S_4 \overline{S_5}) \times \overline{Sel} \\ & + (S_0 + S_1 + S_2 + S_3 + S_4 + S_5) \times Sel \end{aligned} \tag{5.2}$$

$$\begin{aligned} F\_38 = {} & (\overline{S_0} S_1 S_2 \overline{S_3}\,\overline{S_4} S_5) \times \overline{Sel} + \\ & (S_0 + S_1 + S_2 + S_3 + S_4 + S_5) \times Sel \end{aligned} \tag{5.3}$$

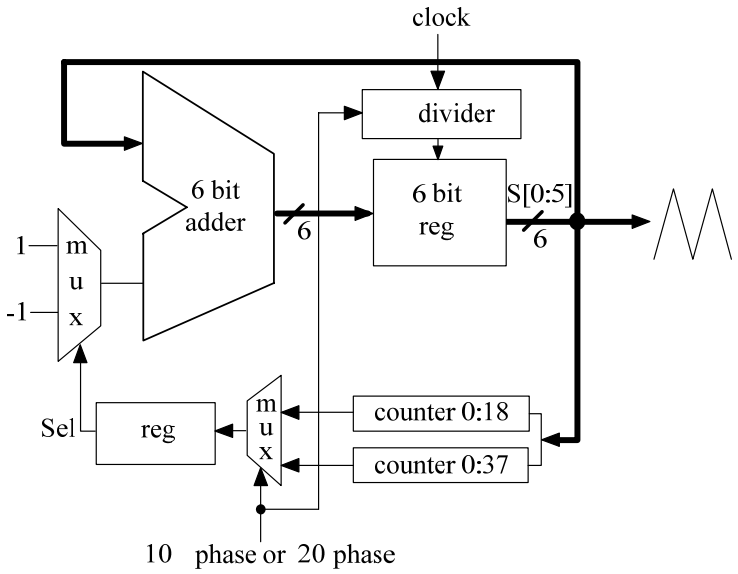


Fig. 5.28 Schematic of programmable profile generator

Table 5.3 Parameter in programmable modulation profile generator

	Top number of wave (modulation deviation)	Divider number (modulation frequency)
10 phase	0.6 x 2^5 = 19.2	(100MHz/38) / 84 = 31.328KHz
20 phase	1.2 x 2^5 = 38.4	(100MHz/76) / 42 = 31.328KHz

5.4.7 Modified Delta-Sigma Modulator

We use the 1st order delta-sigma modulator to control the number of phase jump. The reason we choose the 1st order delta-sigma modulator but not the higher order modulator is that Serial-ATA specifies the frequency must be down spread. The output of 2nd order delta-sigma modulator are -1, 0, 1, 2, and the -1 will up spread although the average is down spread. All of them can not plus 1, because it will cause more jitter. For example, the output originally 2 will be 3 after this step means that it will jump 3 phases in a PFD comparison time (10us) ($\frac{\alpha}{N \times P} = \frac{3}{12 \times 20} = 12500\text{ppm}$). Although the higher order delta-sigma modulator is not suitable here, it still has other

advantage, like the quantization noise is at higher frequency.

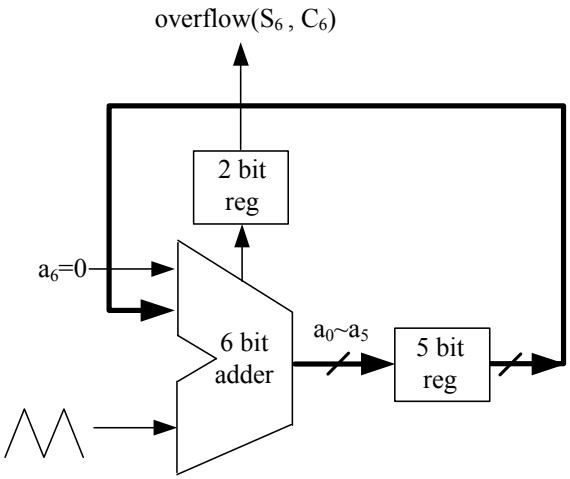


Fig. 5.29 Modified 1st order ΣΔ modulator

Traditionally, the input number is less than the maximum magnitude of the accumulator. As we know, the relationship between input and output of ΣΔ modulator is $m/\text{overflow}$, where m means the input number of modulator, overflow means the maximum magnitude of the accumulator in the modulator. Thus, the output of the traditional modulator only affects decimal; That's enough for SSCG in 10 phases, but not for 20 phases. The average number of jumping phase could be more than 1 in one PFD comparison time ($\frac{\alpha}{N \times P} = \frac{1.2}{12 \times 20} = 5000\text{ppm}$, need to jump 1.2 phase just reaching 5000ppm, meaning that it could jump 0, 1, 2 phases in one PFD comparison time). Hence, our design is to add 1 bit in the accumulator of the modified delta-sigma modulator, but maximum maginitude is the same (Fig. 5.29). Therefore, it will work correctly even if the input number exceeds the maximum magnitude of the accumulator (like that the input number is 38, maximum magnitude is 32, then the average output is $\frac{38}{32}$).

5.4.8 Programmable MUX Control Circuit

This circuit translates the input signal from the ΣΔ modulator to the corresponding MUX selecting signal in 10 and 20 phases SSCG (Fig. 5.30). On the basic of no change in the behind MUX, there is no change in input signals about 20 phases SSCG but this is not the same in 10 phases SSCG. If the input signal is 01 (jump 1 phase), we must translate it into 10 (jump 2 phase) in 10 phases SSCG because the other ten phases introduce by interpolators will be turned off.

Table 5.4 is the truth table. The transforming equation is listed below:

$$overflow1+ = overflow1 + overflow0 \times \overline{select} \quad (5.4)$$

$$overflow0+ = overflow0 \times select \quad (5.5)$$

Where $select = 0 : 10phase, select = 1 : 20phase$

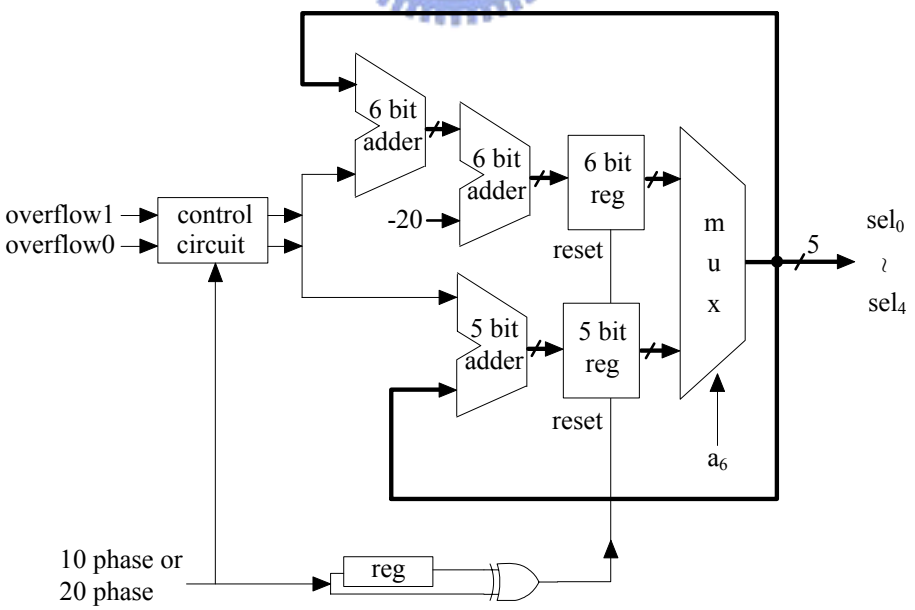


Fig. 5.30 Programmable MUX control circuit

Table 5.4 Transform equation of the control circuit

overflow1	overflow0	select	overflow1+	overflow0+
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	1
1	0	1	1	0

5.4.9 Multiplexer

The function of the multiplexer is to choose which phase should be divided by the latter divider and import the behind PFD. This is our basic theory in our spread spectrum clock generator. The multiplexer is composed of logic circuits (Fig. 5.31). One point we should pay attention is: The input of 20 to 1 multiplexer must be leading by leading in sequence because the specification of Serial-ATA is down spread. If the next phase is lagging, the PFD will judge that the frequency from the VCO is lagging from REF. Then the PFD will cause the charg-pump to charge the loop filter and the oscillation in the VCO will increase. This is called up-spread. On the contrary, if the next phase is leading, the PFD will judge that the frequency from the VCO is leading from REF. Then the PFD will cause the charg-pump to discharge the loop filter and the oscillation in the VCO will decrease. This is called down-spread.

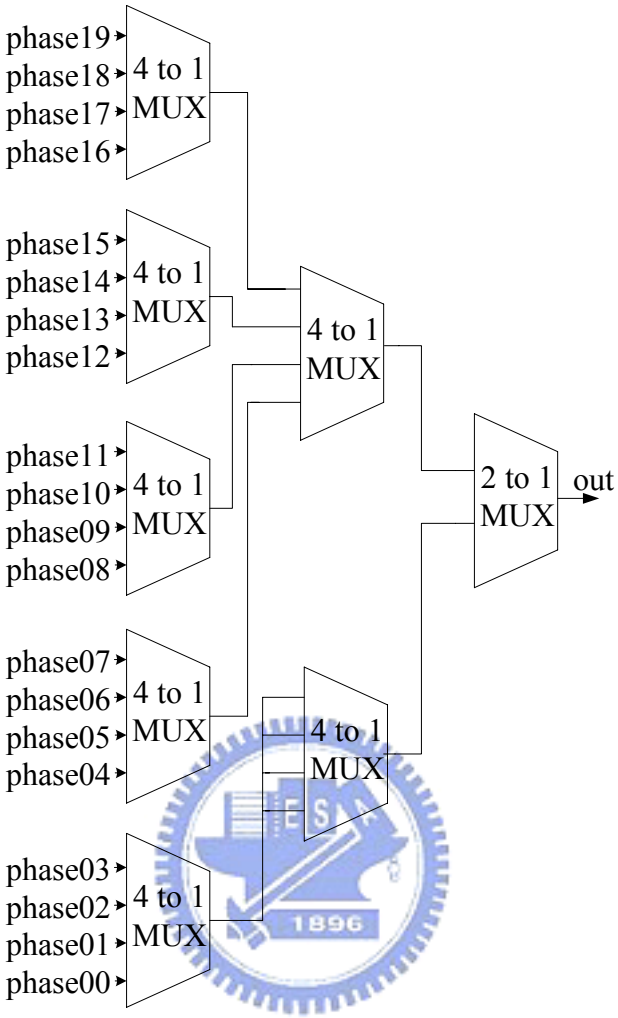


Fig. 5.31 20 to 1 Multiplexer

5.4.10 SSCG System

Here we show some important simulation results about our low jitter PLL and programmable SSCG. The post-simulation of V_C acquisition of PLL is shown inFig. 5.32. Fig. 5.33 is the diagram of phase1~phase5 in VCO (see Fig. 5.17). Fig. 5.34 is the diagram of these 5 phases delay time. We summarize the difference in 5 phases delay time in 100 stable cycle time and shown in Fig. 5.35. Each of these is comparing with 166.6666ps and listed in percentage. The delay time is depending on parasitic capacitance and the error (1ps) with standard delay (166.6666ps) is within

our accept range.

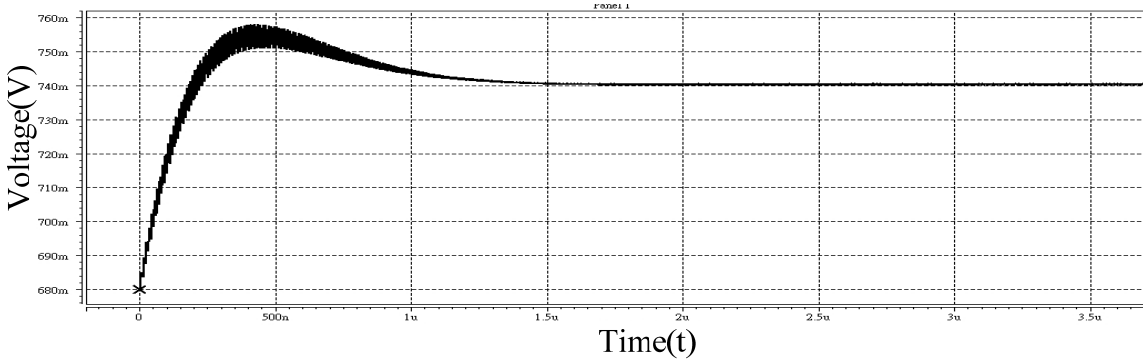


Fig. 5.32 Post-simulation of V_C acquisition of PLL

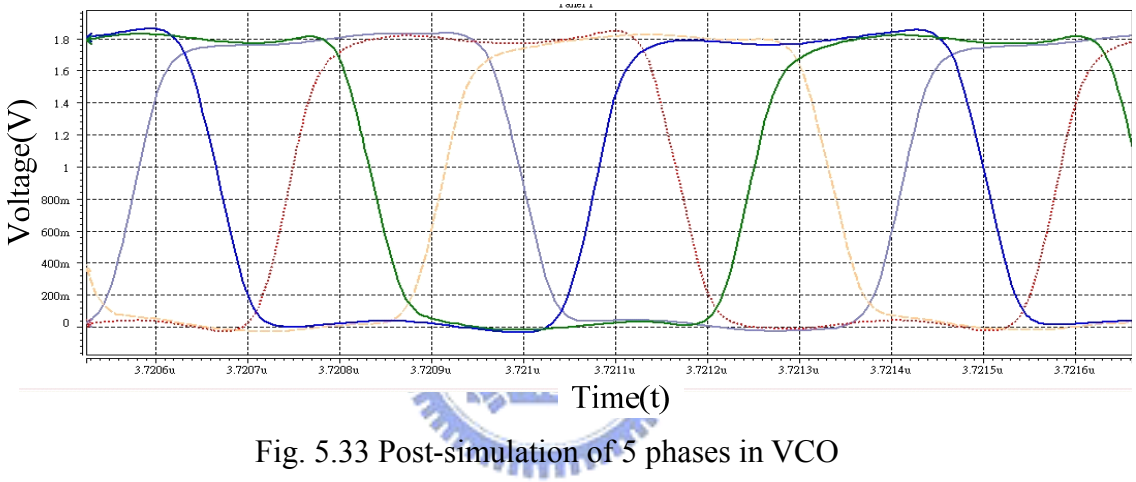


Fig. 5.33 Post-simulation of 5 phases in VCO

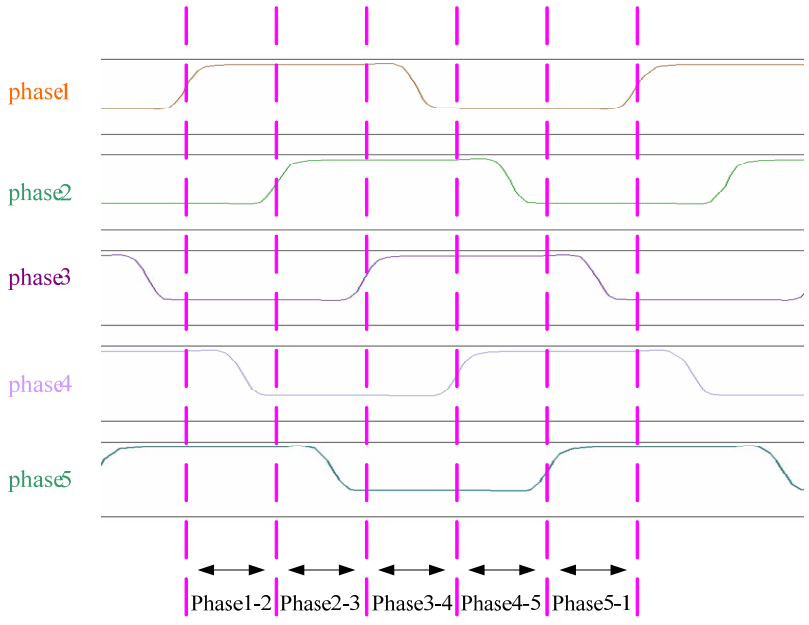


Fig. 5.34 Diagram of 5 phases delay time

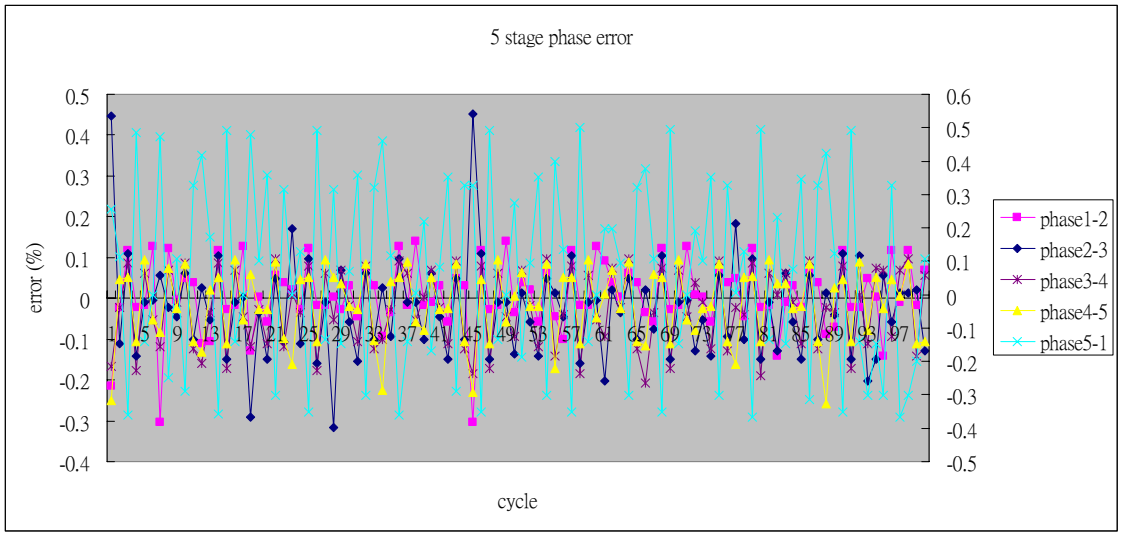
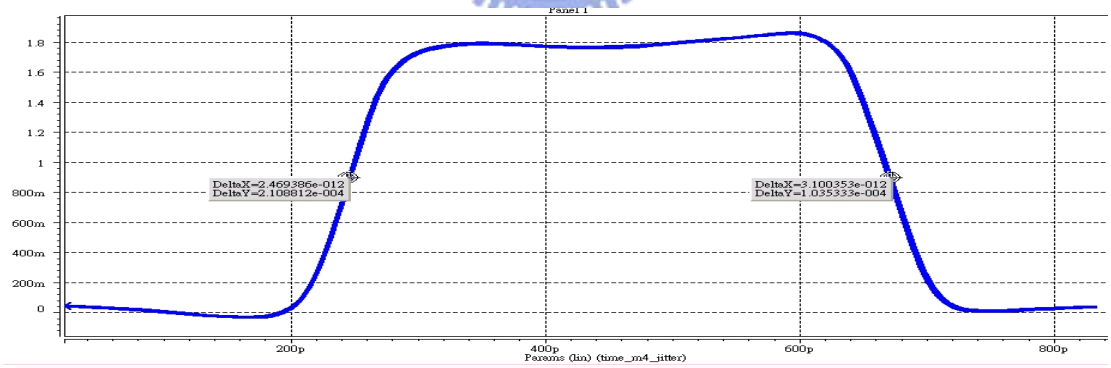
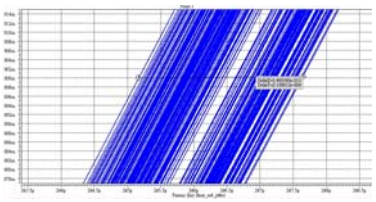


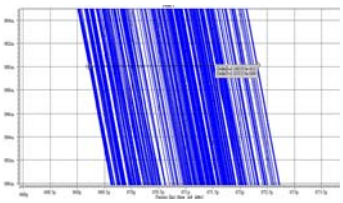
Fig. 5.35 Difference in 5 phases delay time (Post-Simulation)

Fig. 5.36 shows the rising peak-to-peak jitter of 2.46ps and falling peak-to-peak jitter of 3.1ps in post-simulation. Carrier Spectra without spread spectrum is 0dB at 1.2GHz after PLL locked is shown in Fig. 5.37.





P-P jitter=2.46ps
(600 cycles)



P-P jitter=3.1ps
(600 cycles)

Fig. 5.36 Peak to Peak jitter of PLL

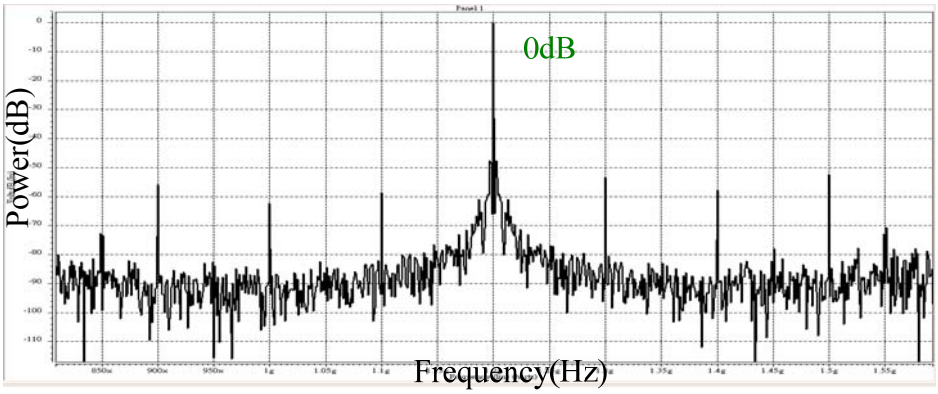


Fig. 5.37 Carrier Spectra without spread spectrum (0dBV @ 1.2GHz)

Fig. 5.38 shows the VCO control voltage in the 10 and 20 phases SSCG. We can obviously find that the control voltage is similar to triangular wave (modulation profile). Fig. 5.39 is the carrier spectra in 10 and 20 phases SSCG respectively. The spectrum is spread over a wider bandwidth, and therefore reduces the peak amplitude. Here the reduction of carrier amplitude is about 17.6dB and 17.8dB. If we want to compare the advantage in time domain about 10 phases and 20 phases SSCG, we can observe their Peak to Peak jitter (Fig. 5.40) or their Cycle to Cycle jitter (Fig. 5.41). We can see the jitter in 10 phases SSCG is larger than 20 phases SSCG from Fig. 5.40. In other words, the variation in timing and data is more violent. This is not good for clock/data recovery (CDR) and will increase its difficulty for recovering data. From Fig. 5.41, we also can conclude that the cycle time variation in 10 phases SSCG is more enormous than 20 phases SSCG. But an obvious drawback in 20 phases is consuming more power than 10 phases SSCG.

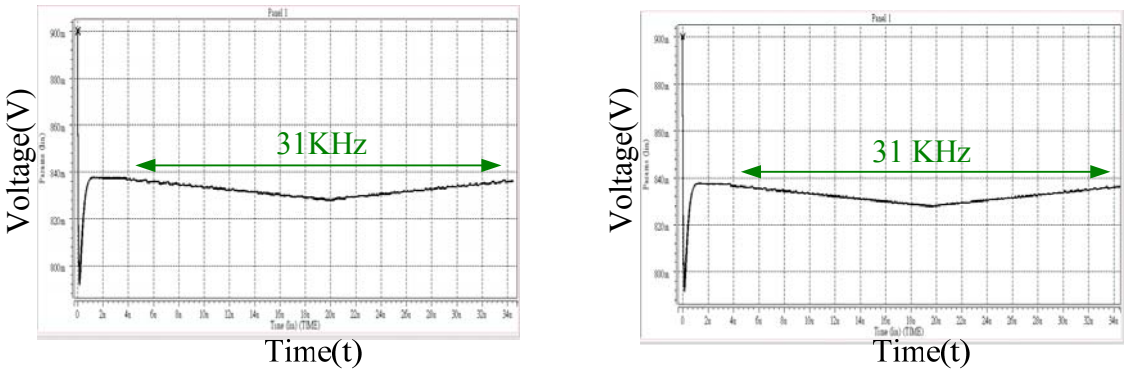


Fig. 5.38 VCO control voltage in (a) 10 and (b) 20 phases SSCG

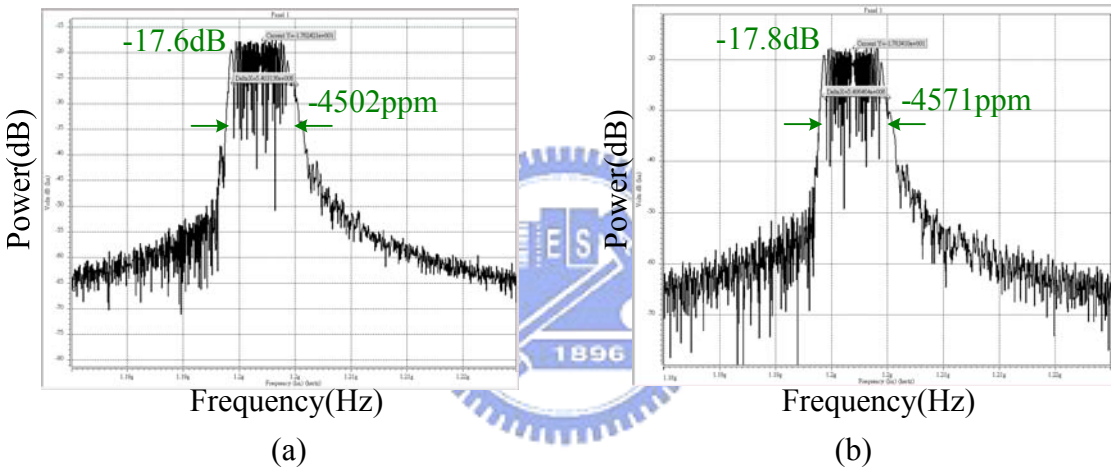


Fig. 5.39 Carrier Spectra with spread spectrum in (a) 10 and (b) 20 phases SSCG

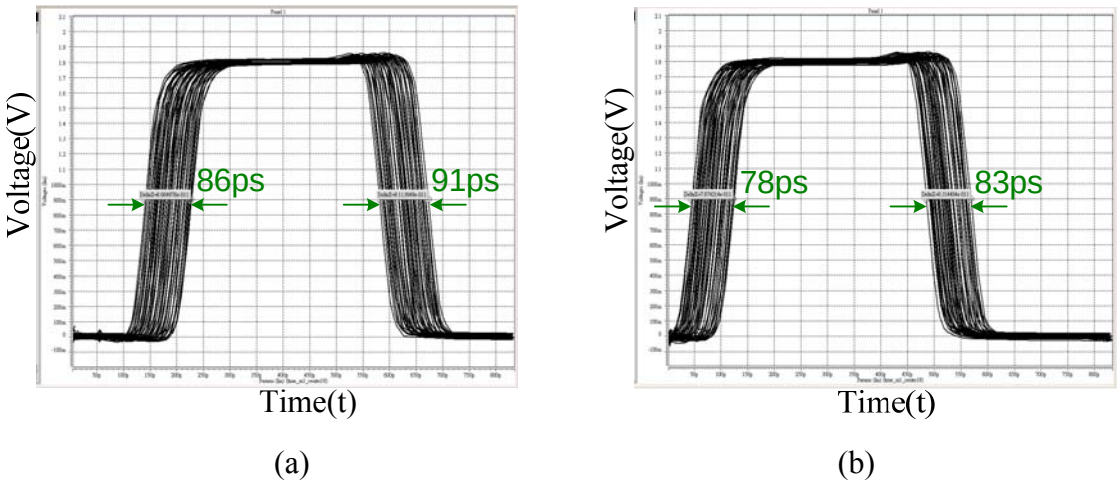


Fig. 5.40 P-P jitter in (a) 10 and (b) 20 phases SSCG

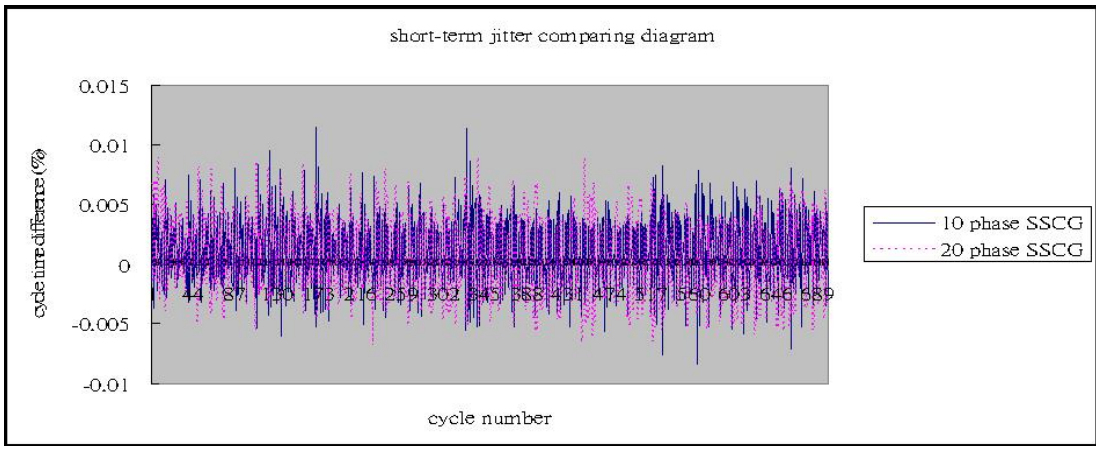


Fig. 5.41 Cycle to Cycle jitter in 10 and 20 phases SSCG

The simulated performance of the proposed low jitter PLL is summarized in Table 5.5. PLL performance in corner cases is listed in Table 5.6.

Table 5.5 PLL performance summary

Items	Performance
Technology	***TSMC 0.18um 1P6M CMOS***
Power Supply	***1.8V***
Crystal Frequency	***100MHz***
VCO Center Frequency@Vctr=0.74v	***1.2GHz***
VCO Tuning Range	***1.0~1.6GHz***
K_{VCO}	***600MHz/V***
Settling Time	***<5μs***
Cycle to Cycle Jitter	***1ps***
Peak to Peak Jitter	***20ps***
RMS Jitter	***3ps***
Core Area	***PLL:355um x 240um*** ***SSCG Control Circuit:95um x 210um***
Loop Filter	***C1=50.0pf*** ***C2=3.6pf*** ***R=6.8kΩ***
VCO Power Consumption	***11mW***
Total Power Consumption	***13.6mW***

Table 5.6 PLL performance in corner cases

	TT post simulation	FF post simulation	SS post simulation
Power Supply	***1.8 V***	***1.8 V***	***1.8 V***
Crystal Frequency	***100MHz***	***100MHz***	***100MHz***
VCO Center Frequency @Vctr=0.74V	***1.2 GHz***	***1.3 GHz***	***1.1 GHz***
VCO Tuning Range	***1.15 ~ 1.58 GHz***	***1 ~ 1.78 GHz***	***1.15 ~ 1.39 GHz***
Range/ f_c (%)	***430 MHz (35.8%)***	***780 MHz (65%)***	***240 MHz (20%)***
Settling Time ($\Delta f < 20ppm$)	***< 5 usec***	***< 5 usec***	***< 5 usec***
VCO Power Consumption	***11.0mW***	***12.5mW***	***9.8mW***
CP Power Consumption	***1mW***	***1.2mW***	***0.8mW***
Total Power Consumption	***13.6mW***	***15.5mW***	***12.5mW***

Table 5.7 Programmable SSCG performance comparison

	10 phase SSCG	20 phase SSCG
Interpolator Power	***-----***	***9.5mw***
SSCG Control Circuit Power	***4mw***	***4mw***
Total Power	***17.8mW***	***27.8mW***
EMI Reduction	***-17.6dB***	***-17.8dB***
Modulation Deviation	***0ppm ~ -4502ppm***	***0ppm ~ -4571ppm***
Cycle to Cycle jitter	***9ps***	***6ps***

Table 5.7 shows the comparison between 10 and 20 phases SSCG. The interpolator power consumes 9.5mW in 20 phases SSCG and don't need in 10 phases SSCG. So the total power in 20 phases is more than in 10 phases SSCG. However, the jitter in 10 phases SSCG is larger than in 20 phases SSCG. In the case of EMI

reduction, there is no obvious difference in 10 phases and 20 phases SSCG. The main reason is that although the charge or discharge time is different in 10 and 20 phases SSCG, the passing frequency is the same. So you can choose spreading spectrum in 10 phases or 20 phases depends on your concern in power or timing issue.

Table 5.8 Comparison of SSCG performance

	Our Work	ISSCC2005 [42]	ISCAS2005 [43]	ISSCC2005 [44]	JSSCC2003 [45]
Technology	***0.18um***	0.18um	0.18um	0.15um	0.35um
Modulation Method	***Modulation on phase***	Modulation on phase	Modulation on divider	Modulation on divider	Modulation on VCO
Divider Counter	***12***	60	73/75	37.5/75	260
VCO Output Phase	***10/20***	10	8	6	7
VCO Output Frequency	***1.2GHz***	1.5GHz	1.5GHz	1.5GHz	266MHz
Modulation Deviation	***5000ppm (6MHz)***	5000ppm (7.5MHz)	5000ppm (7.5MHz)	5000ppm (7.5MHz)	25000ppm (6.65MHz)
EMI Reduction	***17.8dB***	9.8dB	20.44dB	20.3dB	----
P-P jitter (non-SSC)	***20ps***	41ps	80ps	----	162ps
Power Consumption	***18mW/ 28mW***	----	55mW	54mW	300mW
Supply Voltage	***1.8v***	1.8v	1.8v	1.5v	3.3v

Table 5.8 shows the comparison of SSCG performance. We can see the power consumption in my design is very low comparing with other chips. The peak to peak jitter is also very small in our design comparing with other paper. Besides, the maximum power reduction is also pretty good in my SSCG performance. One of the reason about the maximum power reduction in [43][44] are larger than mine is its

frequency span is 7.5MHz (my frequency span is 6MHz). The more frequency span, the more EMI reduction can be achieved.

5.5 Experimental Results

The proposed low jitter PLL and programmable spread spectrum clock generator has been integrated in a 0.18-μm 1P6M CMOS process. In this section, we introduce the testing environment and the experimental results of the chip. Fig. 5.42 shows the chip layout of the SSCG. The total area of the chip is 1.16 × 1.28 mm^2, total pad number is 38. (Including SSCG, transmitter, adaptive termination, loop filter, decoupling capacitance, pad).

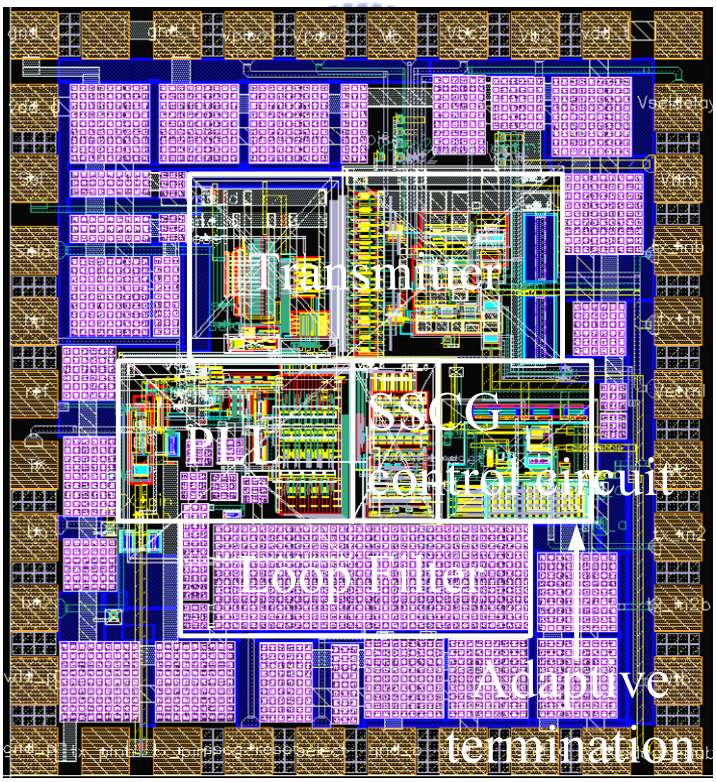


Fig. 5.42 Chip layout of SSCG

Fig. 5.43 is the chip layout of low-jitter PLL. The total area is 0.92 × 1.28 mm^2, total pad number is 34. (Including transmitter, signal, loop filter, decoupling capacitance, pad). Fig. 5.44 is the die microphotograph of Fig. 5.43.

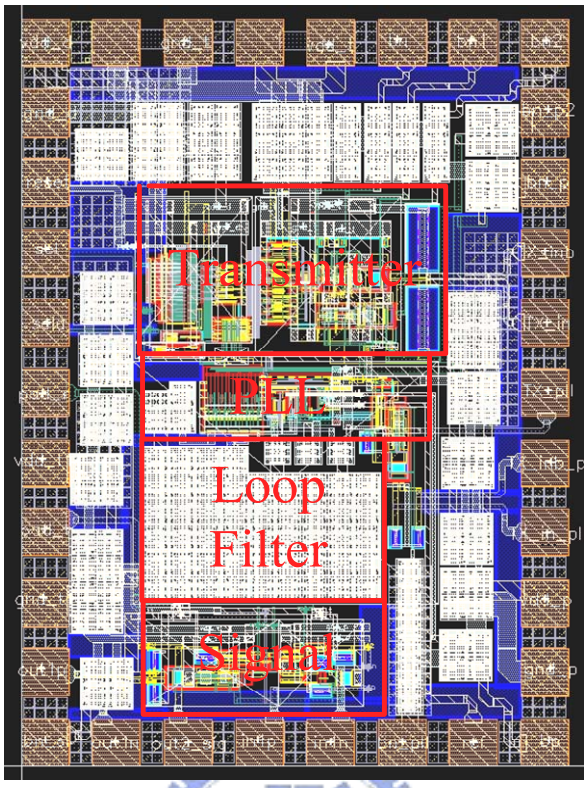


Fig. 5.43 Chip layout of low jitter-PLL

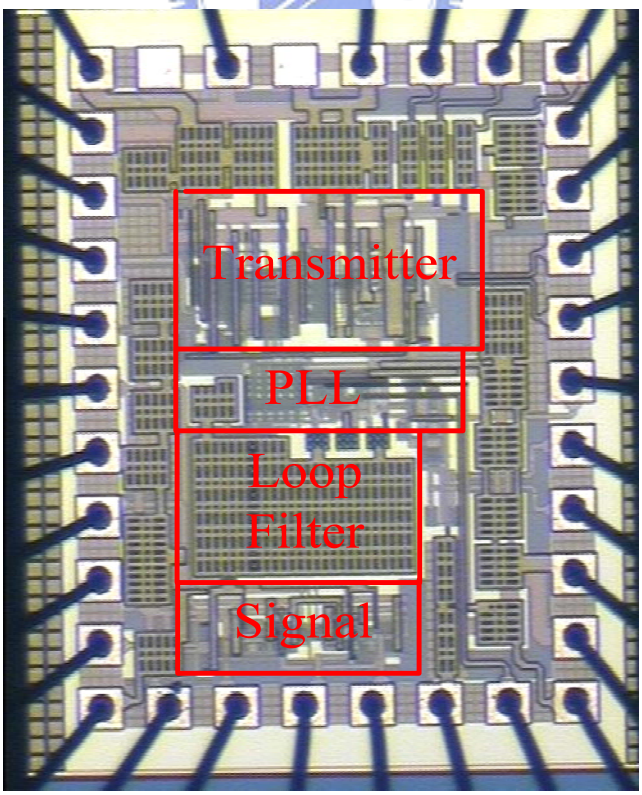


Fig. 5.44 Die microphotograph of low-jitter PLL

5.5.1 Measurement Setup

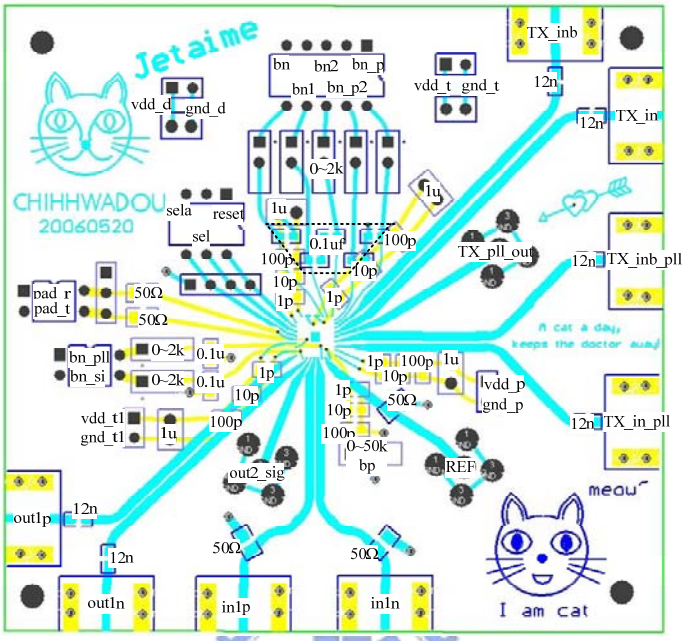
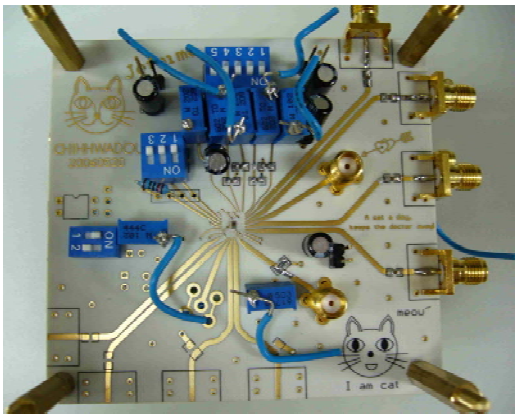
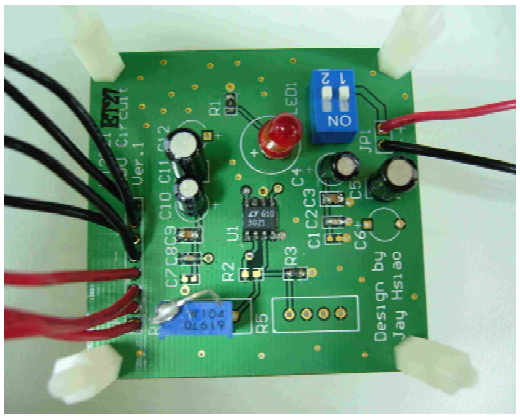


Fig. 5.45 PCB of low-jitter PLL

Fig. 5.45 is the layout of out PCB, and the materialization is shown in Fig. 5.46(a). Since the SSCG is a mixed-mode system, the powers and grounds of digital and analog parts should be separated. The analog and digital powers are generated by voltage regulator (Fig. 5.46(b)), because it generates more stable voltage than general power supply. The PCB stack type we choose is FR4 (Fig. 5.45). The second layer is GND and the third layer is VDD. We can separate the GND layer and VDD layer into two parts used for analog and digital respectively. The power from the instrument should go inside through bypass capacitances, as listed in 1p, 10p, 100p, 1u. The variable capacitance can eliminate noise from different frequency. Besides, the power which is into second layer and third layer can also pass a big capacitance before.



(a)



(b)

Fig. 5.46(a) PCB (b) Regulator

For impedance matching, a 50 Ω termination is employed. As shown in Fig. 5.47. The width of transmission wire is also designed to be 50Ω impedance (44mil). We use SMA connectors with 50 Ω impedance cable (RG223/U) to deliver signals from PCB to oscilloscope or from pulse data generator to PCB.

We also use two capacitances of 12nf to reject the common mode voltage in the differential output (AC coupling). The altering off-chip resistance is set to 0~50kΩ to compensate the degenerate K_{VCO} cause by process variation.

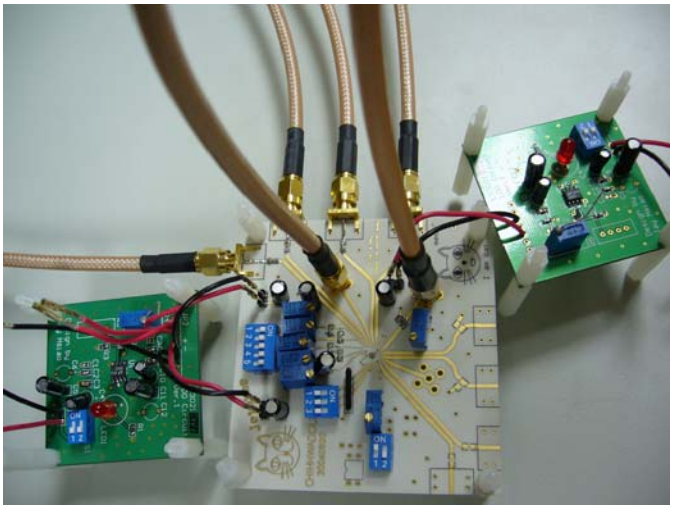


Fig. 5.47 Photograph of PCB and voltage regulator

The input reference clock of the SSCG is produced from the signal generator

(Agilent 81130A). The output spectrum is observed by a Spectrum Analyzer (Agilent E4440A) and the time domain waveform of DIVIDER is derived from the oscilloscope (Tektronix TDS9124C).

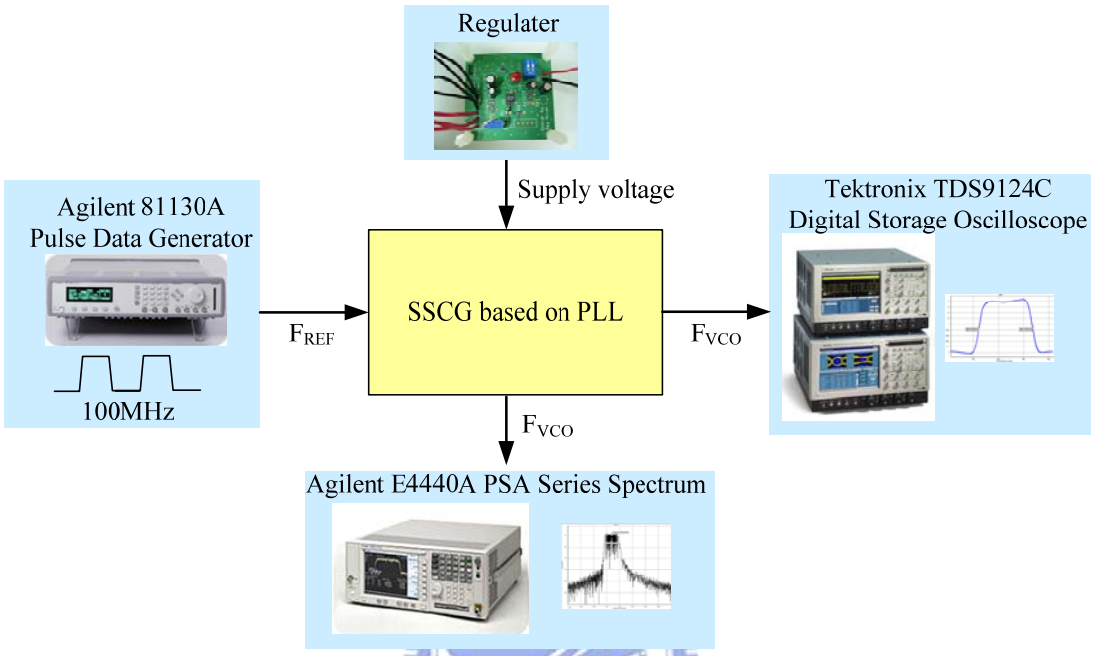


Fig. 5.48 Measurement setup of the programmable SSCG

5.5.2 Measured Waveform and Spectrum of PLL

Fig. 5.49 shows the differential output of the DIVIDER. We can see the two waveforms are quite symmetrical. The amplitude of each waveform is almost 0.5V, so the difference between the two waveforms is almost 1V. Fig. 5.50 is the difference waveform. We can see the frequency is 100MHz which is the same as reference frequency. Because the divisor is 12, the VCO output frequency is 1.2GHz. The duty cycle is near 50%. The rising time and falling time is about 130ps. The rising time and falling time of the DIVIDER should larger than the VCO because that it is from flip-flop. In other words, the rising time and falling time of the VCO is smaller than 100ps.

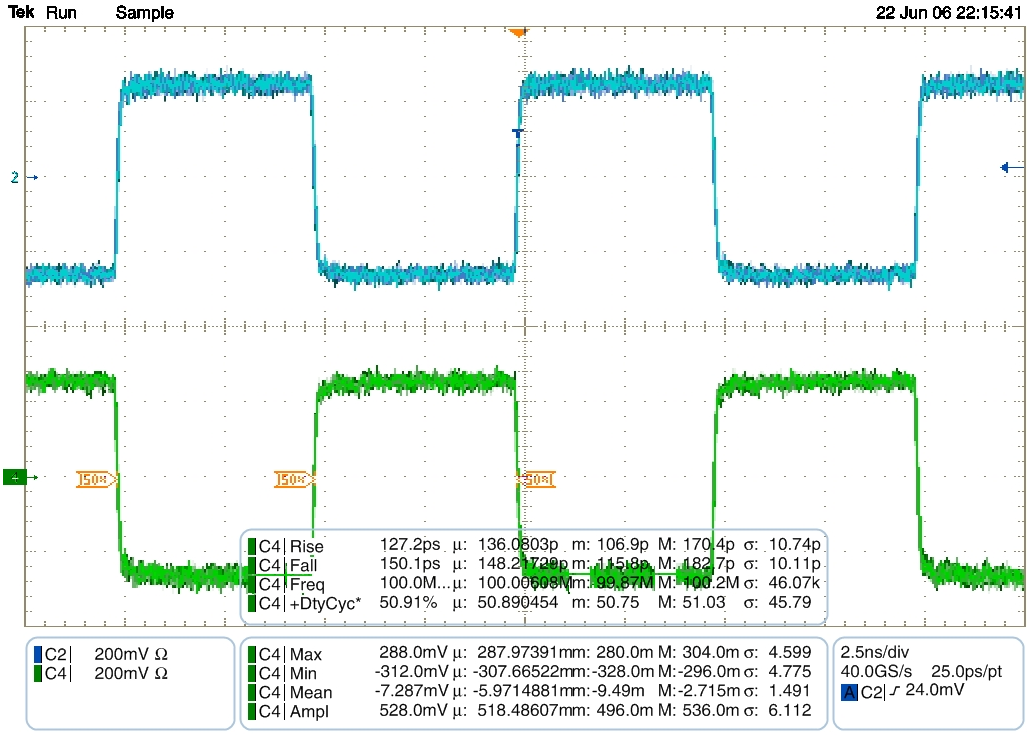


Fig. 5.49 Measurement of differential output from DIVIDER

Fig. 5.50 Measurement waveform of DIVIDER

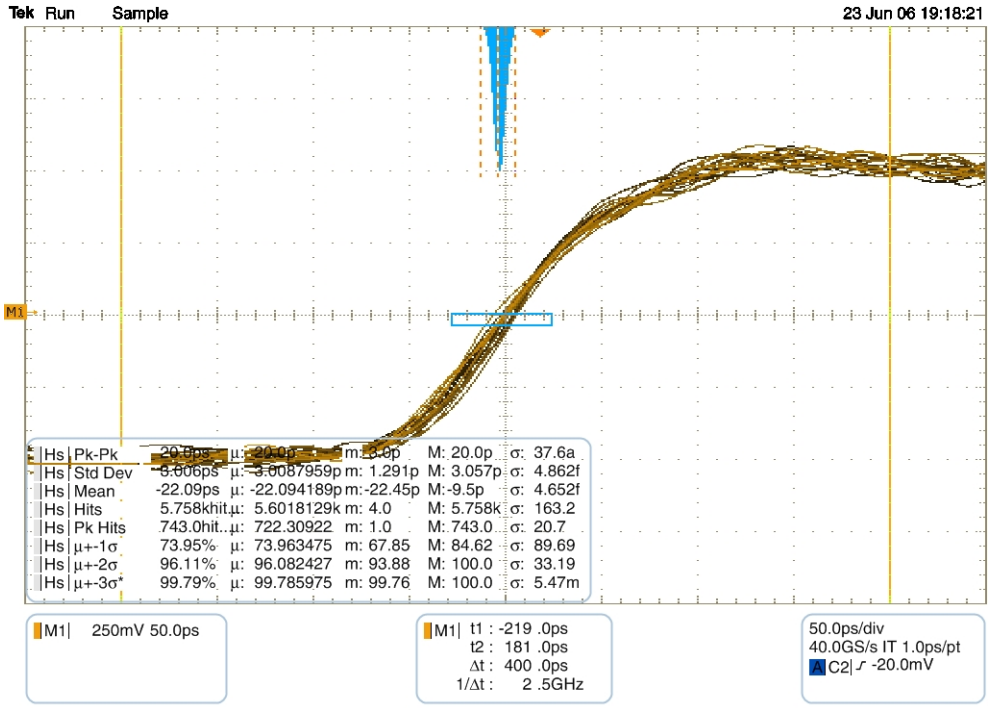


Fig. 5.51 Peak to Peak Jitter of DIVIDER

Fig. 5.51 is the measured jitter of our PLL. We can see the Peak to Peak jitter is 20ps and the RMS jitter is 3.0ps. These jitters are quite small comparing with other papers. This is almost the same as the jitter of the VCO because we have added a flip-flop behind the divider to synchronize the output and input of the divider.

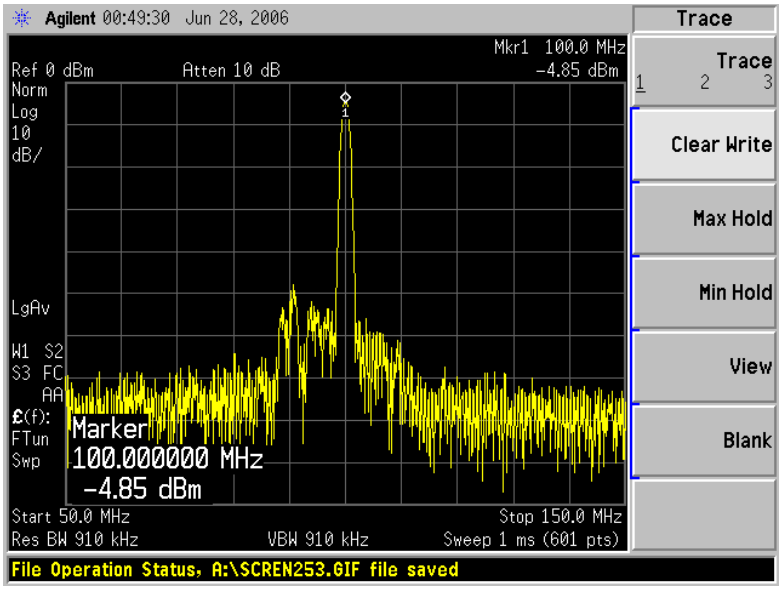


Fig. 5.52 Carrier Spectra when PLL locked

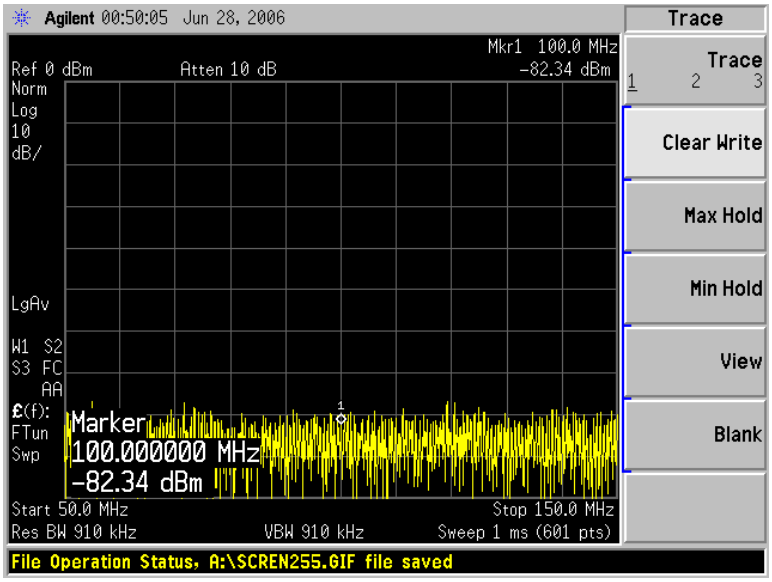


Fig. 5.53 Carrier Spectra in no signal

If we want to know the stability of our PLL, we can see the spectrum of our PLL. Fig. 5.52 show the carrier spectra when our PLL locked. The power is almost -4.85dBm at 100MHz. It is quite large comparing with no signal as shown in Fig. 5.53.

Chapter 6

Conclusions and Future Work

In this thesis, a low jitter phase-lock-loop (PLL) and a programmable spread-spectrum clock generator (SSCG) for Serial ATA using switching phase is presented. The proposed circuit is fabricated in a 0.18-um CMOS process.

Low jitter PLL is achieved through VCO with low K_{VCO} by using medium-threshold-voltage PMOS and passive resistance. The spectrum in the clock generator can be spread by 10 phases or 20 phases, depending on the system specification, such as power saving or low jitter in time domain. Our SSCG for Serial ATA Specification is down spread 5000 ppm with a triangular waveform of modulation frequency 30~33KHz.

The frequency range of PLL is from 1.15GHz to 1.58GHz. Core circuit is operated under 1.8V supply voltage. Total power consumption of PLL is about 13.6mW and the entire area is about 0.92 × 1.28 mm^2 , total pad number is 34, including transmitter, signal, loop filter, decoupling capacitance, pads. The measured RMS jitter is about 3.0ps and Peak to Peak jitter is about 20ps.

The SSCG circuit is also operated under 1.8V supply voltage. Total power

consumption is about 17.8mW and 27.8mW under the conditions of 10 phases and 20 phases. The entire area is about 1.16 × 1.28 mm^2, total pad number is 38, including SSCG, transmitter, adaptive termination, loop filter, decoupling capacitance, pads. The EMI reduction is about 17.6dB and 17.8dB respectively. The cycle to cycle jitter is 9ps and 6ps under the conditions of 10 phases and 20 phases.

Experimental results show that this architecture does achieve low jitter as expectations. The research in this thesis can be extended. How to design a PLL whose tuning range is wide but the K_{VCO} is still low is another important topic.

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