Boost DC-DC Converter With Fast Reference Tracking (FRT) and Charge-Recycling (CR) Techniques for High-Efficiency and Low-Cost LED Driver

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***Abstract*—An RGB LED driver with the fast reference tracking (FRT) and charge-recycling (CR) techniques is proposed to implement a high-efficiency and low-cost RGB backlight module in color sequential notebook computers' display. The proposed LED driver composed of an asynchronous 1.5 MHz DC/DC boost converter with the FRT and CR techniques was fabricated in TSMC 0.25 μm BCD 40 V technology to generate 16 V for 6-series red (R) LEDs or 21 V for 6-series green (G), or blue (B) LEDs. The FRT technique can speed up the reference tracking performance and effectively improve the up-tracking performance. However, the down-reference tracking depends on the load current and output capacitor. It is difficult to enhance the transient response without reducing the efficiency. Therefore, the CR technique is proposed to store extra energy on the recycling capacitor when the output voltage is switched from high- to low-supplying voltage level and releases the reserved energy back to the output node at next period. Furthermore, the output voltage can be rapidly switched between two different voltage levels by FRT technique without consuming much power owing to the restored energy by the CR technique. Experimental results show that the total power consumption of a notebook computer's 15.4' LCD panel can be reduced from 5 W in cold-cathode fluorescent lamp (CCFL) backlight module to about 2-3 W in RGB LED backlight module with the field color sequential (FCS) algorithm. Furthermore, after the implementation of the LED driver with the FRT and CR techniques, the power loss can be reduced to about 24% of that without the FRT and CR techniques.**

***Index Terms*—Charge recycling, feedforward technique, field color sequential, LCD, LED backlight, reference tracking.**

I. Introduction

FOR high-quality display in LCD panels, the selection of the backlight module becomes more and more important. The selection of backlight system not only affects the power consumption but also determines display quality. Today's most popular and power-efficiency backlight module is the white-LED backlight in LCD panels since the power dissipation can be reduced about 40% compared to conventional CCFL backlight module. Moreover, since the backlight module will affect the color gamut, it is popular to make the use of LED backlight in the LCD panels due to the higher color gamut. That is, the white-LED backlight has better color gamut than that of the cold-cathode fluorescent lamp (CCFL) backlight. The disadvantage of the white-LED backlight is that it still needs the color filter to determine the color of the images since the operation of liquid crystal only determines the gray level of the image. In addition, the white-LED backlight generates only 70%–80% National Television System Committee (NTSC) color gamut. In order to have better color gamut, the technique that uses RGB LED backlight for improve the color gamut, which is about 110% NTSC, becomes a trend of today's LCD display market [1], [2].

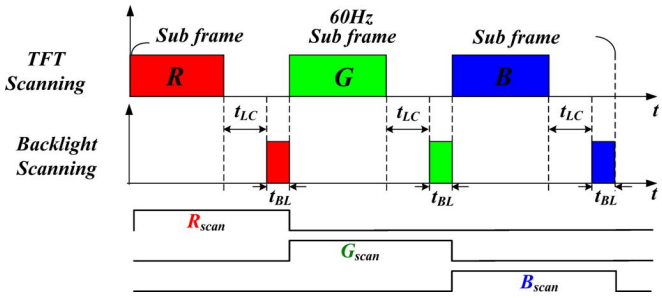

Fig. 1. The timing diagram of color sequential technique for the color filterless LCD panel.

According to the display method of the LCD panel, the liquid crystal, which is functioned as a gate, is turned to the position determined by the content of the display data. Then, the light from backlight module only pass one of three color filters to determine the correct color by the operation of the liquid crystal according to the image data. Therefore, the power loss due to the color filter is relatively large and the power consumption of the backlight module is difficult to be decreased because a lot of light is blocked by the color filter. Certainly, the best method is to remove the usage of the color filter. Recently, the field color sequential (FCS) algorithm [3] that effectively reduced color breakup and motion blur effects can save much power consumption of the backlight module without the requirement of color filter. Conceptually shown in Fig. 1, the conventional color sequential algorithm effectively reduces power consumption without sacrificing the color gamut because the LEDs are not turned on simultaneously but sequentially. One frame data operated by the rate of 60 Hz is divided into three sub-frames, which are $R_{\rm scan}$, $G_{\rm scan}$, and $B_{\rm scan}$. Thus, the rate of the three

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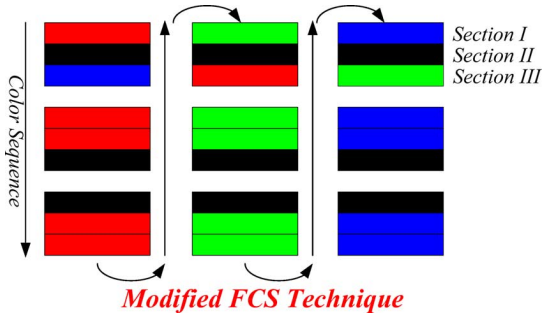

Fig. 2. The implementation of modified FCS algorithm for reducing the color breakup and improving the efficiency.

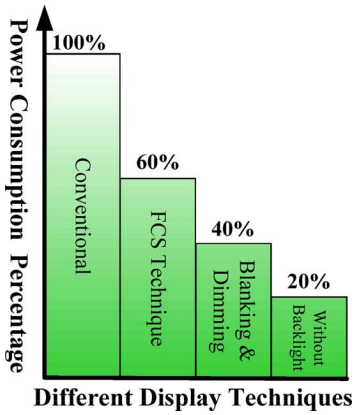

Fig. 3. The power consumption with different display techniques.

sub-frames is 180 Hz. For each sub-frame, the first step is the operation of thin film transistor (TFT) scanning for reading the image data. According to the image data, liquid crystal is turned to the correct position within time $t_{\rm LC}$. This step occupies the most of sub-frame time. When liquid crystal is turned to the suitable position, the LED backlight module emits correct light through the LCD panel to display correct image color. The rest of time $t_{\rm BL}$, which represents the lightening time for backlight module, can determine the value of brightness. However, the value of time $t_{\rm BL}$ is too small to provide the rated brightness since one frame is divided into three sub-frames. In order to extend the lightening time of backlight module, there are many techniques proposed [2]–[5] in high-performance color sequential display to achieve full color image. Furthermore, the modified FCS algorithm inserts black data and disrupts the color sequence to reduce the color breakup effect in the temporal and spatial domain. First, the implementation of modified FCS algorithm is to divide the LED panel to small divisions in the vertical directions to achieve a low-resolution LED panel for lighting the high-resolution LCD panel. In each division, the circulation is in the sequence of the color red, green, blue and black. Besides, the sequence order of each area is different. The modified FCS algorithm divides the full color picture into three divisions in spatial domain owing to the small-size panel of the notebooks and divides one frame into nine sub-frames in the temporal domain as shown in Fig. 2. In addition, the purpose of the insertion of black data is to prevent the color data from being mixed by other colors. Therefore, FCS algorithm can effectively reduce power consumption of RGB LED backlight module compared to the white-LED backlight module with compatible brightness, thereby becoming the most power-efficiency technique in the design of backlight modules of the LCD panel.

The comparison of power consumption between a conventional TFT-LCD with a white-LED backlight module and a FCS TFT-LCD with an RGB LED backlight module is illustrated in Fig. 3. Interestingly, the FCS algorithm can save 40% power compared to the conventional LCD display because there is no color filter that may reduces the brightness in the front of the LCD panel. Hence, the power consumption of the backlight module can be drastically minimized. Furthermore, this technique can be extended to contain the blanking/dimming technique according to the locally averaged image data. That is, a higher power saving result can be achieved and thus the power reduction can be more than 60%. Actually, the minimum power consumption of the LCD display can be reduced to 20% of the conventional design when the backlight system is turned off. However, the image only contains gray levels at this moment. For portable devices like notebook computers, the largest power consumption comes from the backlight module. The power consumptions in the recently LCD panels are reduced to 5 W in white LED backlight and 3 W in color sequential RGB backlight system, respectively, compared to 6 W in CCFL backlight. Therefore, it is important to decrease the power consumption in backlight module of the notebooks without sacrificing any image quality. However, the drawback of the FCS algorithm is the color breakup effect when the RGB LEDs emit light in sequence. Furthermore, the RGB backlight module employs impulse-type display method instead of the hold-type display by CCFL backlight technique for eliminating the motion blur [1]. The disadvantages of the conventional FCS algorithm can be alleviated by the implementation of the modified FCS algorithm.

The light illumination of LED is related to the amount of driving current and the forward voltage [6], [7]. However, it is unreliable that the light illumination is controlled by utilizing the forward voltage when temperature and time is changed [8], [9]. That is, it is inappropriate to make use of forward voltage to control the brightness of LED for getting high-quality image of LCD panel. In order to get uniform and sufficient luminance, the LCD backlight module requires many LEDs to be series-and parallel- connection. The series connection ensures the series LEDs have the same conduction current. The parallel connection needs a current balance (CB) circuit to maintain stable and uniform light illumination in every series connection as shown in Fig. 4. The DC-DC converter is used to offer a sufficient voltage to overcome all the forward voltage $V_{\rm LED}$ of series LEDs. Owing to the great variation of LED material, each of the series LEDs forward voltage $V_{\rm LED}$ is different. Hence, the current balance circuit is designed as the current of LED $I_{\rm CB}$ that is independent of the voltage $V_{\rm CB}$, which is the voltage across the current balance circuit. In general, the LED module will minimize the voltage $V_{\rm CB}$ [8], [9] for reducing the power consumption because the power consumption is equal to the product of $V_{\rm CB}$ and $I_{\rm CB}$. If the output voltage is larger than $V_{\rm LED}+V_{\rm CB(min)}$, the redundant voltage will be across the current balance circuit. Therefore, the power loss will be increased and the efficiency $\eta_{\rm LED}$ of the LED array, which depends on the ratio of the $V_{\rm LED}$ and the $V_{\rm out}$, will be decreased. In order

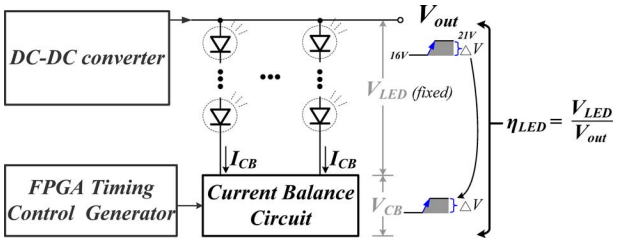

Fig. 4. Power consumption of the current balance circuit.

to improve the efficiency of LED backlight module, the value of the voltage V_{CB} must be minimized and the variation of the voltage V_{CB} will not affect the driving current I_{CB}.

In general, the forward voltages of red, green, and blue LEDs are different to each other owing to the characteristic of material. That is, the forward voltage of a red LED is approximately 2.5 V and the forward voltage of a green/blue LED is about 3.5 V [10]. For a 6-series R-LED branch, a boost DC-DC converter is needed to step up the supply voltage to about 16 V. Similarly, two separate boost DC-DC converters are required to boost the supply voltage to about 21 V for two 6-series green-LED and blue-LED branches. Therefore, the LEDs with different colors require different supplying voltages [11]. That is, the implementation of the LED driver of the modified FCS algorithm needs nine DC-DC converters for driving the notebook's panel with the advantages of much power saving on the current balance circuit. This expensive backlight module system is illustrated in Fig. 5(a) [12]–[15]. This paper proposes a new implementation of the RGB backlight module depicted in Fig. 5(b) for achieving low cost and high efficiency. It is obvious that only three DC-DC converters with current balance circuit are needed. The hardware cost and volume can be effectively reduced. Since the bandwidth of the boost converter is limited to the low-pass filter which is composed of the inductor and capacitor, the fast switching output voltage between 16 V and 21 V is very difficult in the conventional DC-DC boost converters. In order to effectively reduce the chip cost and footprint area, the implementation of fast FRT and CR techniques is utilized. The FRT technique can make the LED driver drives more than 6-series R- and G-/B-LEDs by fast increasing or decreasing the output voltage to correct voltage level. Furthermore, the CR technique is presented to store the extra energy when the output voltage is decreased from high-supplying voltage level for 6-series G-/B-LEDs to low-supplying voltage level for 6-series R-LEDs. Therefore, the CR technique can quickly decrease the output voltage and the stored energy can be sent back to the output node for rapidly increasing the voltage level back to the high-supplying voltage level. Therefore, the proposed LED driver with FRT and CR techniques achieve high-efficiency conversion and low-cost performance compared to the conventional design. Moreover, three DC-DC converters can be decreased to only one DC-DC converter at the sacrifice of power consumption. In Fig. 5(c), the CR mechanism is disabled and the output voltage is always stepped up to about 21 V for driving 6-series R, G, or B LEDs. Considering the case of the 6-series R-LEDs, if the output voltage is 21 V instead of 16 V, it will cause a large redundant voltage ΔV across the current balance circuit and

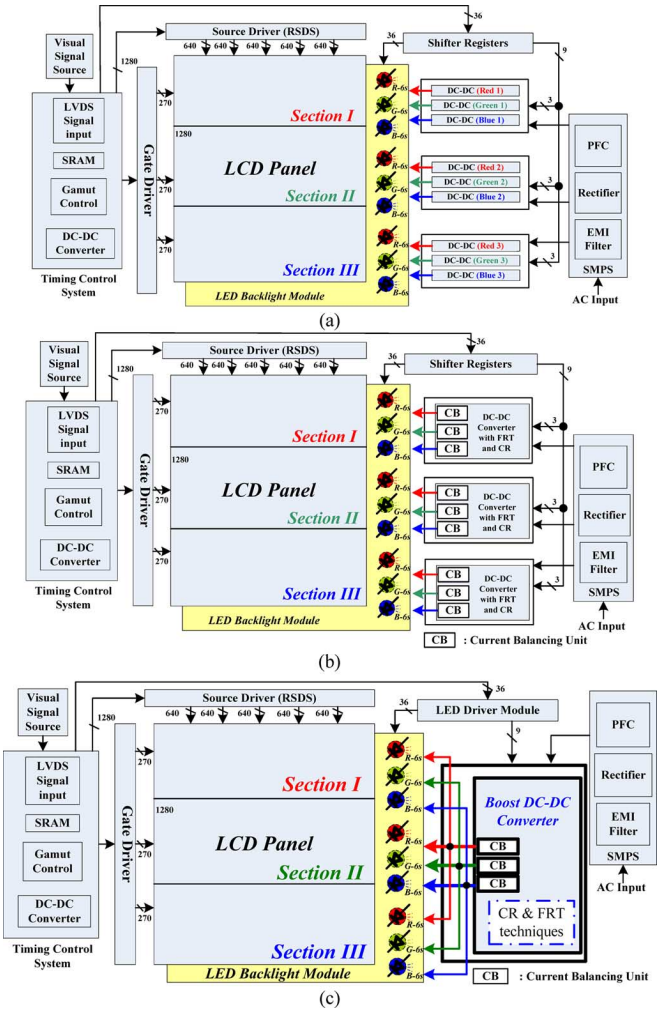

Fig. 5. (a) Conventional RGB LED backlight with nine DC-DC converters. (b) A high-efficiency RGB LED backlight with three DC-DC converters (c) A low-cost RGB LED backlight with only one DC-DC converter.

thus the efficiency is reduced. Therefore, the structure dissipated in Fig. 5(c) consumes more power than that in Fig. 5(b). Thus, a low-cost design methodology is presented for further reducing the external components and footprint area in RGB LED backlight module. Namely, the design methodology in Fig. 5(b) achieves a high-efficiency performance compared to Fig. 5(c). Nevertheless, the structure in Fig. 5(c) achieves low-cost implementation compared to Fig. 5(b).

An integrated LED driver with FRT, CR techniques, and current balance circuit is presented in this paper. In the Section II, the analysis of the reference tracking procedure with FRT and CR technique is presented. The FRT technique is utilized for rapidly switching between two different output voltages and the CR technique is proposed for saving much power dissipation during the transition between two different output voltages. Furthermore, the stability and transient response of the LED driver with FRT technique is also discussed in this section. Section III describes the circuit implementation composed of the voltage control current source (VCCS) compensator, the PWM generator, and the one-shot generator. Besides, the design of the current balance circuit is introduced to describe the power reduction due to the implementation of FRT and CR techniques. The

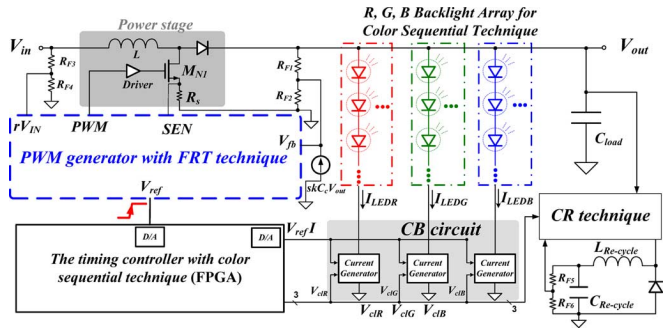

Fig. 6. The proposed LED driver contains the FRT, CR techniques, and the current balance (CB) circuit.

chip was fabricated in TSMC 0.25 μm BCD 40 V technology and experimental results are discussed in Section IV. Finally, a conclusion is made in Section V.

II. The Analysis of FRT Technique and CR Technique

The LED driver for FCS algorithm needs two characteristics to meet the requirements of the LCD response time. One is the fast reference voltage tracking [16], [17] for rapidly switching output voltage to meet the requirement of three colors LEDs and the other one is the charge-recycling [18], [19] for reducing power consumption. The schematic of the proposed RGB driver is shown in Fig. 6. The main blocks contain the PWM generator with FRT technique, the CR circuit, the CB circuit, and the timing controller implemented by FPGA.

A. The Operation Principle of the FRT Technique

The function blocks of PWM generator with FRT technique is shown in Fig. 7(a). The correction current I_c generated by the G_m amplifier represents the output voltage condition of the LED driver. Owing to the usage of the G_m amplifier, the characteristic of high bandwidth can result in fast load/line transient response and reference tracking. However, the static error is worse since the characteristic of low gain of the G_m amplifier. Therefore, the FRT technique utilizes the feedforward current I_{feed} to minimize the effect of I_c for improving the static performance. Furthermore, the feedforward current I_{feed} standing for the input voltage information also can improve line transient performance. The output of the sawtooth generator is a sawtooth waveform I_a with a high threshold current I_H defined as $V_{\text{ref}} \times G_m$ and a low threshold current defined as "0". Therefore, the sawtooth signal with reference voltage information can rapidly determine the value of the duty cycle, thereby regulating the output voltage to quickly track the variations of the reference voltage V_{ref}.

The duty cycle of a voltage-mode LED driver operated in continuous current mode (CCM) is defined as (1) and depicted in Fig. 7(b). At steady state, the correction current I_c can be neglected because the feedforward current I_{feed} is used to minimize the value of correction current I_c. The static performance

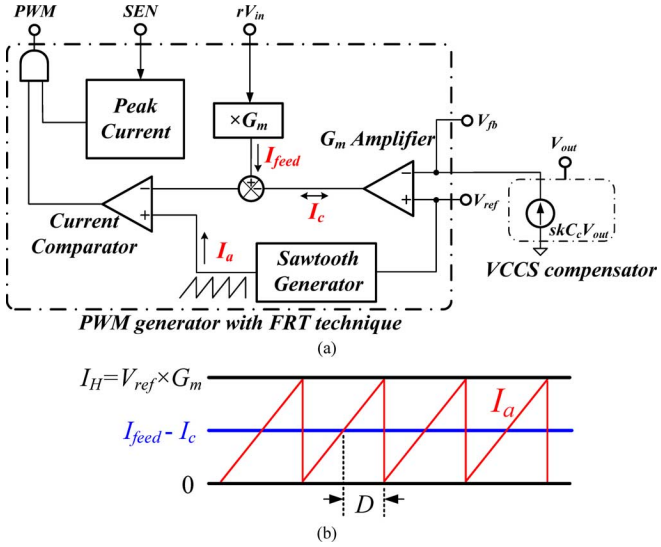

Fig. 7. (a) The PWM generator with FRT technique. (b) The determination of duty waveform in the PWM generator with FRT technique.

can be improved since the duty cycle of LED driver with FRT technique can be simplified as (2).

$$D = \frac{V_o - V_{\text{in}}}{V_0} = \frac{I_H - (I_{\text{feed}} - I_c)}{I_H} \tag{1}$$

$$D \approx \frac{V_{\text{ref}} \times G_m - I_{\text{feed}}}{V_{\text{ref}} \times G_m}, \text{ where } I_H = V_{\text{ref}} \times G_m. \tag{2}$$

When the LED driver is well-designed, the feedback voltage V_{fb} is equal to the reference voltage V_{ref} as shown in (3). According to (2) and (3), the expression of the duty cycle is rewritten as (4). It is obvious that the transient response of line/load can effectively improved due to the appearance of the input and output information in (4). Therefore, the FRT technique not only has fast line/load transient response with a minimized static error but also has fast reference tracking since the variation of I_H is proportional to the variation of the reference voltage.

$$V_{\text{ref}} = V_{fb} = \frac{R_{F2}}{R_{F1} + R_{F2}} V_o = rV_o$$
$$\text{where } r = \frac{R_{F2}}{R_{F1} + R_{F2}} \tag{3}$$

$$D = \frac{V_o - V_{\text{in}}}{V_o} = \frac{rV_o \times G_m - I_{\text{feed}}}{rV_o \times G_m}$$
$$\text{where } I_{\text{feed}} = rV_{\text{in}} \times G_m. \tag{4}$$

When output voltage is changed from low- to high-supplying voltage level, the output voltage can quickly increase by peak current level owing to the high bandwidth of G_m amplifier and FRT technique. However, when output voltage is changed from high- to low-supplying voltage level, the duty cycle of PWM generator can be decreased by fast response of G_m amplifier and FRT technique. Nevertheless, the drop of output voltage still depends on the load current and output capacitor. If the value of the load current is small [20], the recovery time of the regulated output voltage is prolonged. There is not any high-

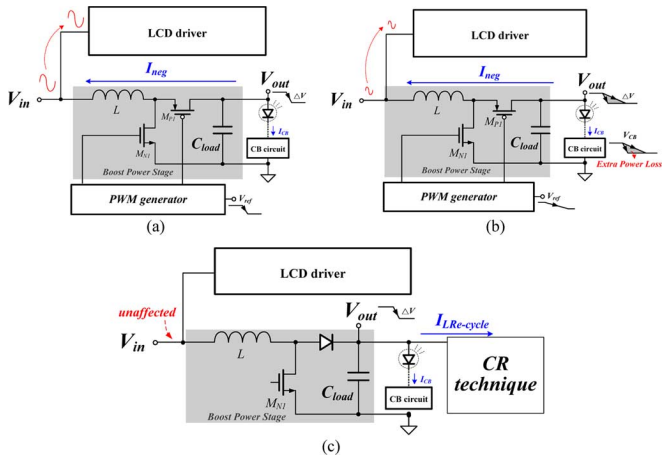

Fig. 8. (a) The negative current $I_{\rm neg}$ rapidly can pull down $V_{\rm out}$ but interferes with $V_{\rm in}$ based on the synchronous boost converter. (b) The slow slewing reference voltage can descend the negative current but the slow response of $V_{\rm out}$ will increase the power loss. (c) The asynchronous boost converter with the CR technique can rapidly pull down $V_{\rm out}$ and alleviate the interference in $V_{\rm in}$.

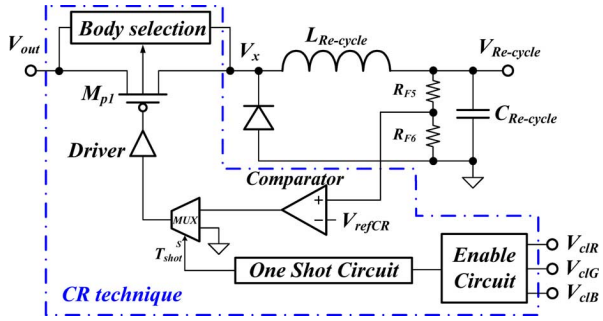

Fig. 9. The schematic of the charging-recycling technique.

efficiency method proposed to solve this problem [21]. Thus, the CR technique is presented to speed up the recovery time, thereby enhancing the power conversion efficiency due to the energy recycling.

B. The Operation Principle of the CR Technique

The low-supplying voltage level can be quickly raised to the high-supplying voltage level by the proposed FRT technique. However, the pulling down response time of the output voltage from high- to low-supplying voltage level depends on the values of the output capacitor and load current.

Generally, the synchronous boost converter can use the negative current through the inductor for storing the extra output energy back to the input voltage $V_{\rm in}$. However, the negative current $I_{\rm neg}$ may have influence on the operation of the LCD driver as shown in Fig. 8(a) since the input voltage needs to provide energy to the LCD driver. Certainly, the slow slewing reference voltage can descend the negative current $I_{\rm neg}$ to alleviate the interference in the input voltage as shown in Fig. 8(b). But the slow transient response of the output voltage results in much power loss on the current balancing circuit. Therefore, the asynchronous boost converter with the CR technique is used to reduce the interference on the input voltage for maintaining the steady input voltage without affecting the LCD driver as shown in Fig. 8(c). The CR technique can store the extra charge from the output capacitor $C_{\rm load}$ to the recycling capacitor $C_{\rm Recycle}$ and thus rapidly pulls down the output voltage to the low-supplying voltage level for driving R-LEDs. Hence, the LED diver can maintain high efficiency due to the minimized power consumption on the current balance circuit. The implementation of the CR technique is conceptually illustrated in Fig. 9.

At the beginning of the operation of the LED driver, the LED backlight module enters the soft-start period. The output voltage of the LED driver is slowly and smoothly raised to the low output voltage for driving R-LEDs. Simultaneously, the comparator turn on the power transistors M_{p1} and the voltage $V_{\rm Recycle}$ followed the output voltage $V_{\rm out}$ is also slowly pulled up to low-supplying voltage level in the CR technique. After the soft-start period, the LED driver enters the normal operation for the modified FCS algorithm. In addition, the FCS algorithm begins to display different color LEDs in sequence for reducing the effect of the color breakup. Therefore, three signals (V_{clR}, V_{clG}, V_{clB}) are enabled to turn on/off three different color LEDs. The LED driver needs to switch the output voltage between the high- and low-supplying voltage levels for minimizing the power consumption because the high-supplying voltage level for 6-series R-LEDs consumes much power due to the large voltage across the current balance circuit compared to G- or B-LEDs.

When the LED backlight module changes from G- or B-LEDs to R-LEDs, the signal V_{clR} is switched to low and the voltage $V_{\rm out}$ will be decreased from high- and low-supplying voltage levels. In the meanwhile, the one-shot circuit will generate the signal $T_{\rm shot}$ to turn on the power transistor M_{p1} and decide the duration of the storing period. Therefore, the CR technique is activated and the extra charge on the output capacitor is delivered to the recycling capacitor $C_{\rm Recycle}$ via the inductor and power transistor M_{p1}. Owing to the current continuity of the inductor, the CR technique can continuously deliver extra charge to the recycling capacitor $C_{\rm Recycle}$ even that the output voltage $V_{\rm out}$ is smaller than the voltage $V_{\rm Recycle}$. Therefore, the high-supplying voltage level can be rapidly pulled down due to the charge storage on the recycling capacitor. Therefore, the CR technique can totally deliver the extra charge from the output capacitor $C_{\rm load}$ to the external capacitor $C_{\rm Recycle}$ if the $C_{\rm Recycle}$ is chosen with a value similar to that of the $C_{\rm load}$. Therefore, the output voltage is rapidly pulled down to the lower regulation voltage for driving R-LEDs and the LED driver effectively stores the charge on the recycling capacitor $C_{\rm Recycle}$. And the one-shot time is defined as (5) by the laws of conservation of charge:

$$T_{\rm shot} = \frac{(C_{\rm load} \text{ or } C_{\rm Recycle}) \times V_{\rm diff}}{I_{\rm LRecycle(avg.)}}. \tag{5}$$

The difference voltage $V_{\rm diff}$ is defined as the difference between the high- and low-supplying voltage levels for controlling the charge storing or restoring procedure. $I_{\rm LRecycle(avg)}$ is an average inductor current in the charge storing procedure. Therefore, the period of CR technique is inversely proportional to the value of the inductor current $I_{\rm LRecycle}$ according to (5). During the charge-recycling procedure, the peak value of inductor current $I_{\rm peak}$ is approximated to $2 \times I_{\rm LRecycle(avg.)}$ and the slope of inductor current is defined as $\Delta V/{\rm L_{Recycle}}$. In addition, the

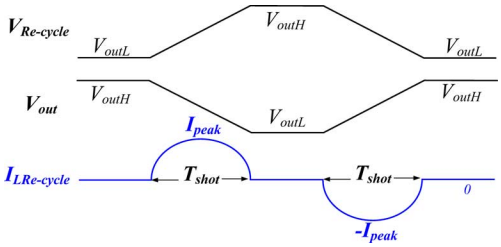

Fig. 10. The timing diagram of the proposed charge-recycling technique.

value of ΔV is nearly equal to $V_{\rm diff}/2$ and the peak current appears at time $t = T_{\rm shot}/2$. Therefore, based on (5), the period of charge-recycling process $T_{\rm shot}$ can be derived as (6).

$$I_{\rm peak} = \frac{\Delta V}{L} \cdot t \Rightarrow (I_{\rm LRecycle})_{\rm avg} = \frac{V_{\rm diff} \times T_{\rm shot}}{8{\rm L}_{\rm Recycle}}$$
$$\Rightarrow T_{\rm shot} = \sqrt{8{\rm L}_{\rm Recycle}(C_{\rm load} \text{ or } C_{\rm Recycle})}. \quad (6)$$

According to (6), the value of $T_{\rm shot}$ is proportional to square of the product of the values of inductor and capacitor. It means the larger the values of inductor and capacitor need more storing/restoring time. Furthermore, it is also important to limit the peak inductor current to prevent the circuit from being damaged by the large inductor current. Thus, the boundary of the peak current is expressed as (7).

$$I_{\rm peak} \le \sqrt{\frac{2(C_{\rm load} \text{ or } C_{\rm Recycle})}{{\rm L}_{\rm Recycle}}} V_{\rm diff}. \quad (7)$$

According to (6)–(7), the CR technique can utilize the larger inductor to decrease the peak inductor current and extend the period $T_{\rm shot}$ to accomplish the charge-recycling procedure. On other hand, when the one of the signals V_{clG} and V_{clB} is switched to low and the signals V_{clR} is switched to high, it means that the output voltage will be raised from low- to high-supplying voltage level for turning on the G-/B-LEDs. Therefore, the signal $T_{\rm shot}$ is generated by the one-shot circuit and the restoring period is started to restore the charge from the recycling capacitor to the output capacitor, thereby rapidly raising the output voltage back to its high-supplying voltage level. Hence, that means the restored charge can rapidly raise the output voltage back to it regulated voltage level and the rising recovery time is effectively decreased to extend the emission of the LED for ensuring the brightness. The timing diagram of charge-recycling procedure is conceptually depicted in Fig. 10. Moreover, since the recycling voltage $V_{\rm Recycle}$ switches between high- and low-supplying voltage levels, the body selection circuit is needed to avoid the forward biasing current for improving power efficiency.

The selection of the inductor and capacitor can ensure the CR technique smoothly transfers energy between two external capacitors depend on the equations (5)–(7). According to the previous designs, the pulling down response time depends on the load current and output capacitor. It is very hard to speed up the response time. However, due to the existence of the CR technique, the response time can be effectively reduced. Furthermore, when the output voltage $V_{\rm out}$ is needed to switch from low- to high-supplying voltage level, the stored energy is restored back to the output capacitor $C_{\rm load}$. Considering another condition that G-LEDs changes to B-LEDs or vice versa, the CR technique is not activated due to the same output voltage level for driving G- or B-LEDs. The CR technique not only saves much power when the backlight module changes from G- or B-LEDs to R-LEDs but also speeds up the transient response time.

C. Reference Tracking Procedure

The FRT and CR techniques can speed up the transient response of tracking response. Therefore, the reference tracking process of LED driver with mixed color sequential can be divided into four stages, which are described as follows.

1) Stage I: When the reference voltage $V_{\rm ref}$ steps from $V_{\rm ref1}$ to $V_{\rm ref2}$, the peak value I_H of the sawtooth current I_a is increased instantly due to reference tracking mechanism. The correction current I_c, which is the output of G_m amplifier, is also increased owing to a larger difference voltage between $V_{\rm ref}$ to V_{fb}. A feedforward current $I_{\rm feed}$ is determined by input voltage $V_{\rm in}$. The difference current between $I_{\rm feed}$ and I_c is compared to the sawtooth current I_a for determining duty cycle. Therefore, the current of $I_{\rm feed} - I_c$ is decreased instantly as a result that reference voltage $V_{\rm ref}$ is increased. Thus, by comparing I_a and $I_{\rm feed} - I_c$, the control signal $V_{\rm PWM}$ is switched to a high level and the turn-on time of power transistor MN_1 in Fig. 5 is limited to a predefined maximum duty that represents a peak current level. Thus, the boost converter is controlled by the peak current loop. At this time, the CR technique also conveys the energy from the capacitor $C_{\rm Recycle}$ to output capacitor $C_{\rm load}$. Therefore, the voltage $V_{\rm Recycle}$ is decreased by CR technique and the output voltage can be quickly increased. The output voltage is raised to a high-supplying voltage level for a forward conduction voltage of 6-series green or blue LEDs within a short time.

2) Stage II: When the output voltage $V_{\rm out}$ approaches the high-supplying voltage level V_{outH}, the correction current I_c is gradually decrease because the difference voltage between V_{fb} and $V_{\rm ref}$ is decreased and the characteristic of fast response of the G_m amplifier [22], [23]. Hence, the current of $I_{\rm feed} - I_c$ is increased rapidly and then the outputs of the PWM generator can substitute for the peak current control to regulate the output voltage of the LED driver. Certainly, the static error is minimized due to the insertion of feedforward current $I_{\rm feed}$ compared to the current-mode boost converter with current-domain control.

3) Stage III: When the reference voltage $V_{\rm ref}$ is decreased instantly from $V_{\rm ref2}$ to $V_{\rm ref1}$, the correction current I_c by the G_m amplifier is instantly decreased owing to a larger difference voltage between $V_{\rm ref}$ and V_{fb}. Furthermore, due to the reference tracking mechanism, the peak value of the sawtooth current I_a is decreased instantly. Thus, the current I_a is decreased and the value of $I_{\rm feed} - I_c$ is increased instantly as well. By comparing the values of I_a and $I_{\rm feed} - I_c$, the control signal $V_{\rm PWM}$ can be adjusted to a lowest level to turn off power transistor M_{N1} illustrated in Fig. 6. In addition, the CR technique is activated and stores extra energy on the capacitor $C_{\rm Recycle}$ at this time. Therefore, the output voltage of proposed LED driver is decreased according to load current and the CR technique. And the down

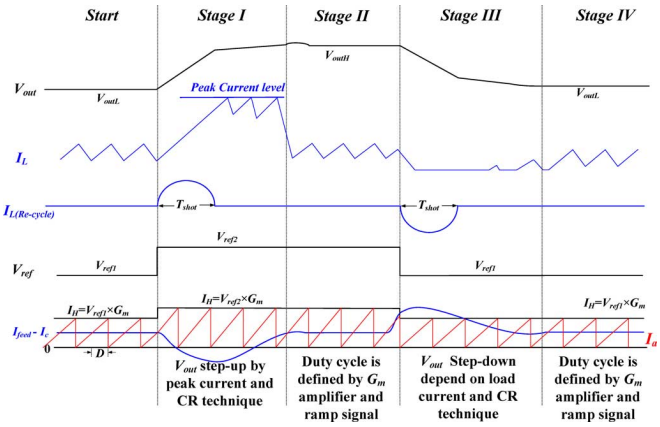

Fig. 11. The timing diagram of the proposed charge-recycling technique.

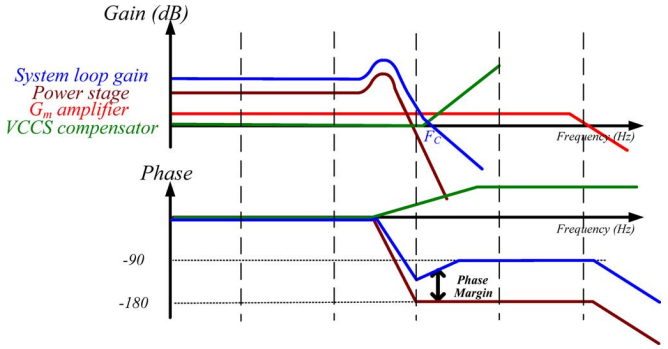

Fig. 12. The Bode plot of the proposed boost converter.

tracking can be quickly achieved compared to conventional converter after the implementation of the CR technique.

4) Stage IV: When the output voltage is decreased to the low-supplying voltage level V_{outL}, the correction current I_c is gradually increased. Due to the fast response of the G_m amplifier, the current of $I_{\text{feed}} - I_c$ is decreased instantly. The fast and stable pulse width control is guaranteed and the timing diagram of the up- and down-reference tracking response is shown in Fig. 11.

D. The Stability of the LED Driver With the FRT and CR Techniques

After the description of the FRT and CR techniques, the stability of the whole system must be guaranteed to ensure the stable operation. Because the CR technique is enabled in the transient time of reference tracking procedure, the stability analysis of LED driver can ignore the effect from the CR technique. Since the design of the LED driver is based on the voltage-mode boost converter design, the LED driver with FRT techniques is needed to be analyzed and compensated. The transfer function of a voltage-mode boost converter in CCM [24]–[26] is defined as (8).

$$T(s) = G_m(s) \times \frac{V_{\text{out}} r}{V_H D'} \times \frac{\left(1 - \frac{s}{\omega_z}\right)}{\left[1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right]}, \quad \text{where}$$

$$\omega_0 = \frac{D'}{\sqrt{\text{LC}}}, Q = D' R_{\text{Load}} \sqrt{\frac{C}{L}}, \text{and } \omega_z = \frac{D'^2 R_{\text{Load}}}{L}. \quad (8)$$

r is feedback resistor ratio defined by (3). V_H is the amplitude of the sawtooth signal. ω_0 is the double poles due to the output LC filter. The parameter Q is called the quality factor. ω_z is the right-half plane (RHP) zero of the boost converter in CCM operation. R_{Load} is the output equivalent load resistance. Instead of the error amplifier, the FRT technique uses the low-gain and high-bandwidth G_m amplifier to speed up the reference tracking time. $G_m(s)$ is used to stand for the transfer function of the G_m amplifier and can be treated as a low-gain amplifier with having a high-frequency pole. As illustrated in Fig. 6(a), in order to stabilize the whole system, a left-half plane (LHP) zero is inserted by the voltage-control current source (VCCS) compensator [27], [28] to enhance the phase margin. Then, the system transfer function of the proposed structure is modified as (9).

$$T(s) = G_m(s) \cdot \frac{V_{\text{out}} r}{V_H D'} \cdot \frac{\left(1 + \frac{s}{\omega_{z(\text{VCCS})}}\right)\left(1 - \frac{s}{\omega_z}\right)}{\left[1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right]},$$

where

$$\omega_{z(\text{VCCS})} = \frac{-1}{kC_c R_{F1}}. \quad (9)$$

$\omega_{z(\text{VCCS})}$ is an low-frequency LHP zero generated by the VCCS compensator. The parameter k is the amplified factor of the compensation capacitor C_c and is determined by the VCCS compensator. The stability of the proposed boost converter can easily promised by using a G_m amplifier with a high-frequency pole above the crossover frequency and a low-frequency zero $\omega_{z(\text{VCCS})}$. The Bode plot of the converter as illustrated in Fig. 12 show the adequate phase margin [29]. Therefore, the phase of the boost converter was approximately 45 degrees to ensure the stability of the system.

III. Circuit Implementation

A. The Design of the Voltage Control Current Source Compensator

The purpose of the voltage control current source (VCCS) compensator is to generate a low-frequency zero to extend phase margin. The design of the VCCS compensator is depicted in Fig. 13. Due to the variations of the output voltage, the small-signal current I_1 can be expressed as (10) by using small integrated capacitors C_{c1} and C_{c2}. In addition, the resistors R_1 and R_2 must be used to reduce the DC level of output voltage for avoiding that the capacitor C_{c1} is damaged by higher voltage.

$$I_1 = \frac{aV_{\text{out}}}{\frac{1}{sC_{c1}} + Z_x} \text{ where } a = \frac{R_2}{R_1 + R_2} \quad (10)$$

Z_x is output impedance seen at node X. The value of Z_x is low enough to be ignored since there is a negative feedback loop that is composed of transistors M_1 and M_3 [28]. Ideally, the small-signal current I_1 flows through transistor M_1 because the

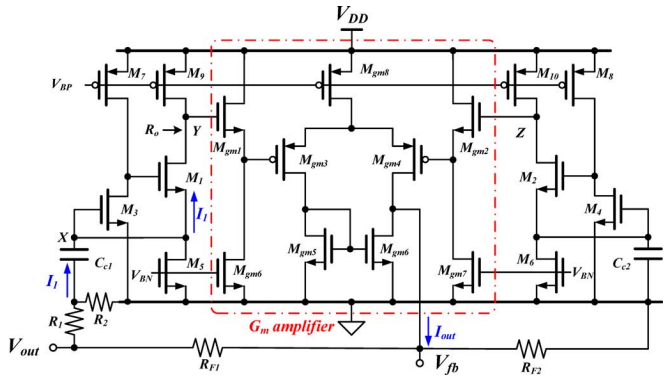

Fig. 13. The circuit of the VCCS compensator.

impedance at the source of transistor M_1 is much smaller than that of the bias current source. Thus, the small-signal voltage at node Y is equal to (11).

$$V_Y = I_1 \times R_o \tag{11}$$

R_o is the output resistance seen at node Y. In order to convert the small-signal voltage to current signal, a transconductance amplifier g_m is used and thus the output current of the VCCS circuit I_{out} is defined as (12).

$$I_{\text{out}} = g_m \times V_Y = \frac{g_m R_o V_{\text{out}}}{\frac{1}{sC_{c1}} + Z_x} = \frac{sC_C g_m R_o a V_{\text{out}}}{1 + sC_{c1} Z_x}$$
$$\approx sC_{c1} g_m R_o a V_{\text{out}} = skC_{c1} V_{\text{out}}. \tag{12}$$

where $k = g_m R_o (R_1/(R_1 + R_2))$ is the multiplication factor to amplify the effective value of the small compensation capacitor C_{c1}. That is only a small capacitor is needed to generate a LHP zero near the crossover frequency. Besides, the other parasitic poles in the VCCS compensator locate at higher frequency because the value of impedance Z_x is small. Therefore, these poles have no effect on the stability of the system. Therefore, a low-frequency zero is generated by the VCCS circuit without inserting any low-frequency pole.

B. The Implementation of the PWM Generator With FRT Technique

The circuit implementation of the PWM generator with FRT technique is shown in Fig. 14. The circuit is used to generate the prediction PWM control signal and consists of two voltage-to-current circuits, a G_m amplifier, and a current comparator. In order to have the same transconductance of the two voltage-to-current converters, the resistors R_1 and R_2 of the two voltage-to-current converters are designed to have the same value. The upper bond of the voltage V_{ramp} is defined as V_{ref} and the low bond of the voltage V_{ramp} is defined as ground. Therefore, the voltages V_{ramp} and rV_{in} are converted into current signals I_a and I_{feed} to implement the equations (2)–(4) by the two voltage-to-current converters with the same transconductance. The matching methods of layout technique are carefully used to reduce the process variation between the two resistors. The G_m amplifier [22] is used to convert the difference voltage between V_{fb} and V_{ref} to a

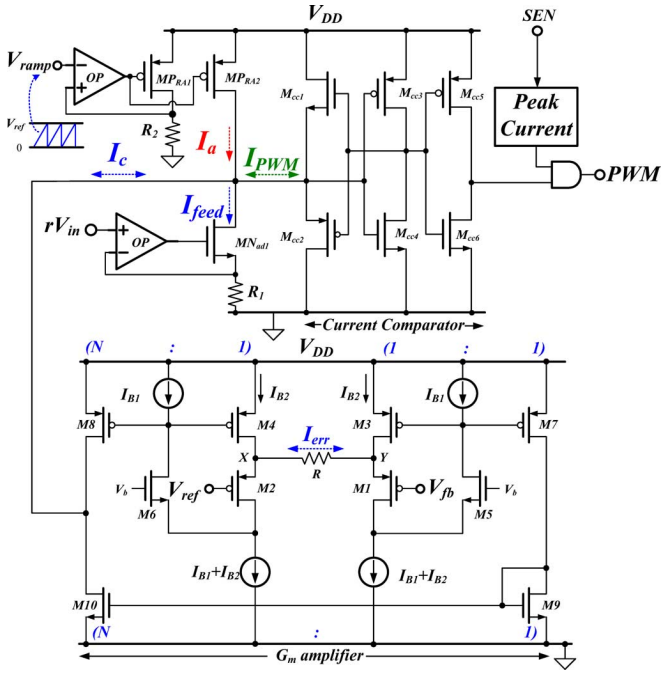

Fig. 14. The PWM generator with FRT technique consists of voltage-to-current converters, G_m amplifier, and current comparator.

current signal I_c. That is the signals V_{fb} and V_{ref} are applied to the gates of transistor M_1 and M_2, respectively. The output current I_c is injected to the input of the current comparator. The flipped-voltage-follower (FVF) is used to minimize the resistance seen at node X and Y for improving the linearity of the transconductance of the G_m amplifier. Obviously, the reduction of the impedance at node X or Y can be found as (13).

$$Z_x \approx \frac{1}{g_{m1}} \frac{1}{g_{m5} r_{o5}} \frac{1}{g_{m3} r_{o1}}. \tag{13}$$

Therefore, the transconductance of the G_m amplifier is approximated to $1/R$ due to the low impedance at node X and Y. After the operation of the three current mirrors, which are (M_3, M_7), (M_4, M_8), and (M_9, M_{10}), the correction current I_c is defined as (14).

$$I_c = 2N \frac{V_{\text{ref}} - V_{fb}}{R}. \tag{14}$$

The current I_{PWM} is the summation of the ramp current I_a, the feedforward current I_{feed}, and the correction current I_c at the input of the current comparator. Thereby, the value of the current I_{PWM} decides the duty of the PWM signal. Moreover, not only the prediction duty cycle can be decided by I_a and I_{feed} but also the correction current can adjust the duty cycle to regulate the output voltage.

C. The Proposed One-Shot Generator for Charge Recycling Technique

The FCS algorithm implemented by FPGA send the controlling signals (V_{clR}, V_{clG}, and V_{clB}) to turn on/off the different color LEDs in sequence as shown in Fig. 1. In addition, the LED driver not only supplies 16 V to supply 6-series R-LEDs but also supplies 21 V to 6-series G- or B-LEDs for minimizing the

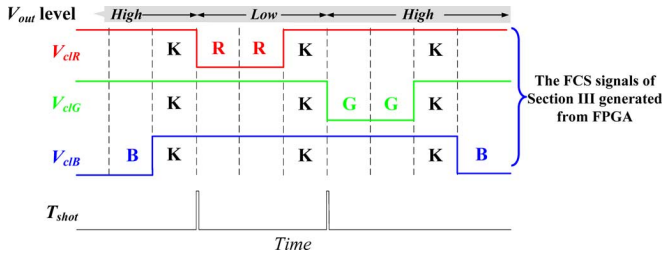

Fig. 15. The timing diagram of modifier FCS signal in Section I of the notebook and the one shot signal $T_{\rm shot}$.

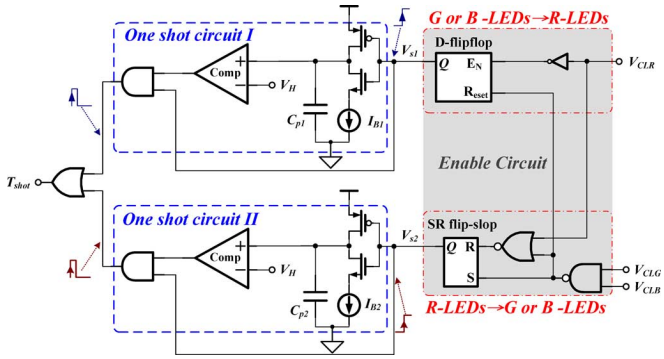

Fig. 16. The circuit of the one shot generator.

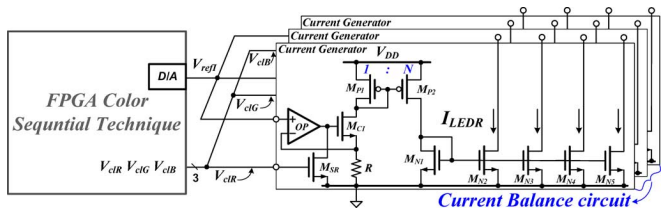

Fig. 17. The current balance circuit.

voltage across the current balance circuit to maintain high efficiency [8], [9]. According to the color of the backlight module in Section III of the notebook with FCS algorithm as illustrated in Fig. 3, the controlling signals V_{clR}, V_{clG}, and V_{clB} are turned on/off in sequence and can define the output voltage level as depicted in Fig. 15. The black (K) frame means that all the LEDs are turned off to reduce the effect of color breakup. Furthermore, the output voltage is kept constant when the black frame is inserted to the FCS algorithm. Until one of the controlling signals which need different output voltage level is switched to the low level, the output voltage will be changed to the appreciate voltage for reducing power consumption on the current balance circuit. Therefore, when the output voltage switches from high- to low-supplying voltage level or low- to high-supplying voltage level, the LED driver will start the CR technique to transmit the charge for speeding the reference tracking procedure.

These signals (V_{clR}, V_{clG}, and V_{clB}) used to generate the one-shot signal $T_{\rm shot}$ are shown in Fig. 15 to decide the turning on/off the power transistor M_{p1} of the CR technique in Fig. 9. Therefore, the one-shot generator, which is composed of the enable circuit and two one-shot circuits, utilizes the three signals (V_{clR}, V_{clG}, and V_{clB}) to start the CR technique as shown in Fig. 16. The enable circuit uses three input signals (V_{clR}, V_{clG}, and V_{clB}) to generate two signals V_{s1} and V_{s2}. The one-shot circuit produces the one-shot signal $T_{\rm shot}$ when one of the signals V_{s1} and V_{s2} is instantly pulled to high. Furthermore, the one-shot circuit I will be reset until the signal V_{s1} is switched to low and so does the one-shot circuit II. When the LEDs backlight module turns off the G- and B-LEDs, the controlling signals V_{clG} and V_{clB} reset the signal V_{s1} to low. Therefore, when the signal V_{clR} is switched from high to low means that the R-LEDs will be turned on, the signal V_{s1} will be instantly pulled to high and the output voltage should change from high- to low-supplying voltage level. Therefore, when the signal V_{s1} is pulled to high, the capacitor C_{p1} is discharged by biasing current I_{B1} to generate the one-shot signal $T_{\rm shot}$. Therefore, the signal $T_{\rm shot}$ is utilized to turn on the power transistor M_{p1} in Fig. 9 and thereby the CR technique is activated to store the energy on the recycling capacitor $C_{\rm Recycle}$. The length of the one-shot signal $T_{\rm shot}$ can be calculated as (15).

$$T_{\rm shot} = \frac{(V_{\rm DD} - V_H)C}{I_B} \tag{15}$$

Therefore, the one shot circuit can modulate the length of one-shot time by adjusting the capacitor and biasing current for achieving the preferable CR technique. In practice, the length of the one-shot time may be varied by the process variation. The value of the capacitor is trimmed to finely adjust the value of switching frequency [30]. Similarly, when the R-LEDs are turned off by the controlling signal V_{clR}, the SR-latch will reset the signal V_{s2} to low. Until one of the signals V_{clG} and V_{clB} is pulled to low, the signal V_{s2} will be switched to high and it represents that the LED driver should supply high-supplying voltage level to turn on the G- or B-LEDs. Therefore, the signal will enable the one-shot circuit to start the CR technique to restore the energy back to the capacitor $C_{\rm load}$. Thus, the CR technique can achieve the fast up- and down-reference tracking procedure and high efficiency without consuming much power.

D. Proposed Current Balance Circuit

In general, the light luminance of LEDs is controlled by the driving current [8], [9]. Therefore, the LEDs backlight module utilizes the current balance circuit to control the amount of driving current for regulating the constant light luminance of LEDs. The current balance circuit composed of three current generators is controlled by the signals $V_{\rm refI}$, V_{clR}, V_{clG}, and V_{clB} from the FPGA as shown in Fig. 17. The current generator utilizes the operation amplifier (OP) and the resistor R to operate as a voltage-to-current converter. Furthermore, the input signals $V_{\rm refI}$, which is converted by the digital-to-analog (D/A) converter in the FPGA, determines the value of the driving current in the series connection LEDs. Thus, the voltage signal $V_{\rm refI}$ is used to generate the constant current. After the two current mirrors pairs, which are (M_{P1}, M_{P2}), $(M_{N1} - M_{N5})$, the current $I_{\rm LEDR}$ can be used to drive the 4 brunches of LEDs and thus the variation of drain-source voltage of these transistors $(M_{N1} - M_{N5})$ will not have large influence on the value of current $I_{\rm LEDR}$. Moreover, the FPGA uses the three signals V_{clR}, V_{clG}, and V_{clB} to turn on/off the R-, G-, and B-LEDs for achieving the FCS algorithm as shown in Fig. 3. Using the R-LEDs as an example, the transistor M_{C1} operates

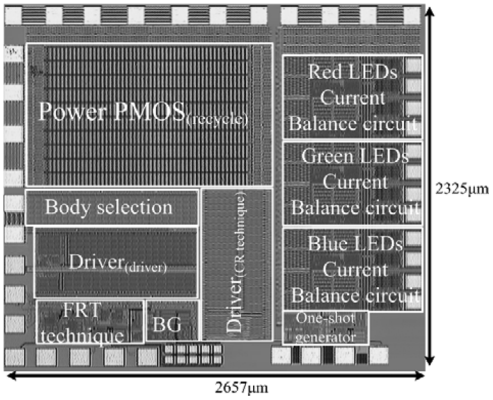

Fig. 18. The chip micrograph.

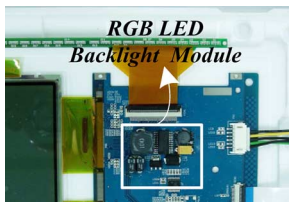

Fig. 19. The module of RGB LED backlight driver for color filterless panel display.

in the cut-off region when the signal V_{clR} is pulled to high level. Thus, the current $I_{\rm LEDR}$ is equal to zero and unable to drive the R-LEDs. In other words, when the V_{clR} is pulled to low and the transistor M_{SR} operates in cut-off region, the voltage-to-current converter will start to convert the reference voltage $V_{\rm refI}$ to current signal $I_{\rm LEDR}$ for driving the R-LEDs. Therefore, the current balance circuit is used to generate the constant current to drive the LEDs for constant light luminance. The FCS algorithm can be achieved by turning on/off the LEDs according the values of signals V_{clR}, V_{clG}, and V_{clB}. When the current generator is activated to convert the current, the transistors $(M_{N1} - M_{N5})$ operated in the saturation region generally stress the drain-source voltage for reducing the power consumption.

IV. Measured Results

The proposed LEDs driver with CR and FRT techniques was fabricated in 0.25 μm TSMC BCD 40 V technology and the micrograph of the chip is shown in Fig. 18. The RGB LED backlight module composed of LED driver with the FRT and CR techniques is depicted in Fig. 19 for 15.4' LCD panel of the notebook.

Fig. 20(a) shows the one DC-DC converter without the reference tracking technique supply only high-supplying voltage level as 21 V to drive all of the R-, G-, and B-LEDs. However, when the backlight module drives the R-LEDs by such high supplying voltage level, the voltage across the current balance circuit is larger than that during driving the G-/B-LEDs. Therefore, the efficiency of the LED backlight module is deteriorated. The LEDs driver with the FRT technique can speed the transient performance of reference tracking, and thereby reducing the power dissipation. However, the up-reference tracking procedure can

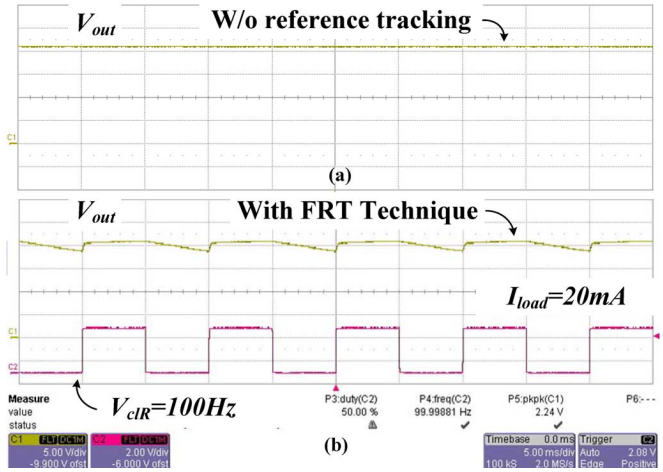

Fig. 20. (a) The waveforms of the LED driver without reference tracking technique. (b) The waveforms of the LED driver with the FRT Technique.

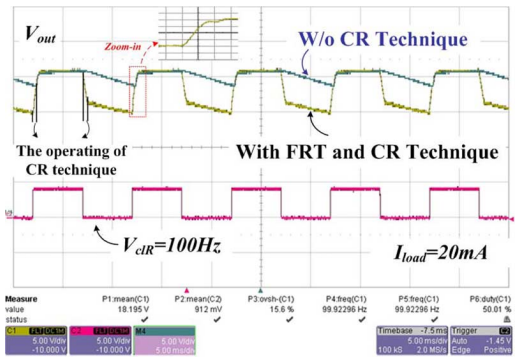

Fig. 21. The waveforms of the LED driver with or without the FRT and CR techniques.

be quickly achieved due to the FRT technique and the down-reference tracking depends on the output capacitor and load current. Unfortunately, when the value of the load current is small, the output voltage is slowly decreased by the small load current as shown in Fig. 20(b), which shows the signal V_{clR} decides the turning on/off of the R-LEDs. The low value of the signal V_{clR} means the output voltage needs to be low-supplying voltage level as 16 V. On other hand, the high value of the signal V_{clR} means the output voltage needs to be high-supplying voltage level as 21 V. Therefore, when the LED driver operates at light loads, large output voltage across the current balance circuit causes much power dissipated in the current balance circuit. Certainly, the extra energy is always dissipated on the current balance circuit at any load condition. Therefore, the proposed CR technique will reduce the power consumption on the current balance circuit and increase the efficiency of the LED driver. The waveforms of LED driver with CR and FRT techniques can effectively speed the up- and down- reference tracking procedures as shown in Fig. 21. Therefore, the CR technique can save much extra energy on the recycling capacitor $C_{\rm Recycle}$ and the detail waveform of CR and FRT techniques is shown in Fig. 22.

When the output voltage changes from high-supplying voltage level for G- or B-LEDs to low-supplying voltage level for R-LEDs, the one-shot generator sends the signal $T_{\rm shot}$ to turn on the power transistor M_{p1} for transmitting energy

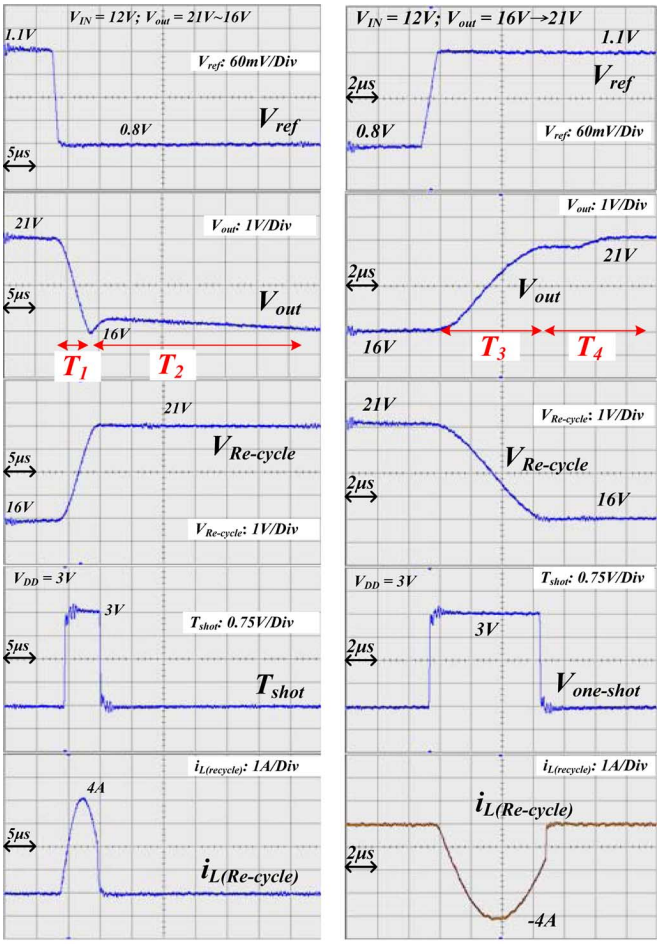

Fig. 22. (a) When $V_{\rm ref}$ changes from 1.1 V for G- or B-LEDs to 0.8 V for R-LEDs, the extra energy is stored in the auxiliary inductor $L_{\rm Recycle}$ and capacitor $C_{\rm Recycle}$, which is triggered by the one-shot generator. (b) When $V_{\rm ref}$ changes from 0.8 V for R-LEDs to 1.1 V for G- or B-LEDs, the extra energy stored in the auxiliary inductor $L_{\rm Recycle}$ and capacitor $C_{\rm Recycle}$ is released to the output node $V_{\rm out}$, which is also triggered by the one-shot generator.

from $C_{\rm load}$ to $C_{\rm Recycle}$. The duration of the signal $T_{\rm shot}$ is approximated to 7 μs as shown in Fig. 22(a). Simultaneously, the $I_{\rm L(Recycle)}$ transmits energy from the output capacitor $C_{\rm load}$ to the recycling capacitor $C_{\rm Recycle}$ at time T_1. Thus, the output voltage $V_{\rm out}$ can be rapidly decreased from 21 V to 17 V within time T_1. The value of T_1 about 7 μs is faster than other conventional structure. Furthermore, the recycling voltage $V_{\rm Recycle}$ is also raised from 17 V to 21 V because the extra charge is high efficiency to store on recycling capacitor $C_{\rm Recycle}$. Thus, the fast response from high- to low-supplying voltage level is demanded for achieving high performance of the FCS algorithm. And then the settling time T_2 depends on the value of the output capacitor $C_{\rm load}$ and load current. The output voltage is pulled down to near 17 V after the period T_1. This voltage level is enough to drive the 6 series R-LEDs with minimized power loss since the voltage stress across the current balance unit is smaller that of the high supplying level as 21 V. But the CR technique also dissipates power due to the conduction loss. However, the efficiency still can be improved due to low conduction loss during the short storing/restoring time. When the low-supplying voltage level steps to high-supplying voltage

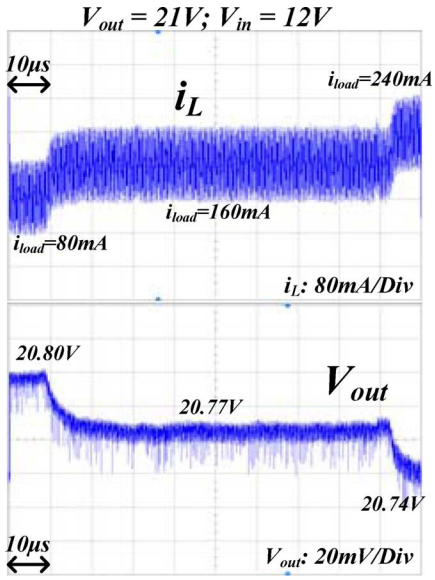

Fig. 23. Load regulation when load current changes from 80 mA to 240 mA.

level, the signal $T_{\rm shot}$ is sent to transferred the recycling energy on the $C_{\rm Recycle}$ back to the output capacitor $C_{\rm load}$ for rapidly raising the output voltage $V_{\rm out}$ to the regulated voltage. Thus, Fig. 22(b) shows the reversing current $I_{\rm L(Recycle)}$ from $V_{\rm Recycle}$ to $V_{\rm out}$ at time T_3. The output voltage $V_{\rm out}$ gets stored energy from the CR technique of the LED driver at time T_3 about 7 μs. Thus, the extra energy stored on the recycling capacitor $C_{\rm Recycle}$ is efficiently used to speed the up-reference tracking procedure. After the period T_3, the FRT technique is used to regulate the output voltage $V_{\rm out}$ to the high-supplying voltage level, which is 21 V, within time T_4.

The load regulation is shown in Fig. 23, the value of load regulation is 0.5 mV/mA when input voltage $V_{\rm in}$ is 12 V and the output voltage $V_{\rm out}$ is 21 V. The load transient time is only 10 μs when variation of load current is about 80 mA. It is obvious to find that the load regulation is improved [21] and the transient response time is short due to the FRT technique. The line regulation is shown in Fig. 24, the value of line regulation is 1.36 mV/V when the output voltage $V_{\rm out}$ is 21 V and load current $I_{\rm load}$ is 100 mA. Similarly, the recovery time of the line transient response is decreased within 10 μs. For a conventional boost converter design with PI compensation, it is very hard to decrease the line/load transient response time within 10 μs. Fig. 25 shows comparison of the power consumption between LEDs driver with or without CR and FRT technique. The LED driver without FRT and CR techniques always supplies 21 V and thereby the power still waste on the current balance circuit when the backlight module turn on the R-LEDs. However, the driver with FRT technique can reduce the power loss due to the small voltage across the current balance circuit. Furthermore, the proposed driver with FRT and CR techniques can reduce the power consumption and efficiently enhance reference tracking performance. When the RGB LED backlight module with FCS algorithm drives 12-branches LEDs and each branch consumes 20 mA, the LED driver without FRT and CR techniques consumes 1.04 W. However, the LED driver with the FRT and CR techniques switches different voltage level and consumes only

TABLE I
PERFORMANCE SUMMARY

Fabrication Process	TSMC 0.25μm BCD 40V 1P5M
Chip area	6.178mm^2(2325μm*2657μm)
Supply Voltage (V_{in})	8-13.5V
Output Voltage (V_{out})	16-30V
Switching Frequency	1.5MHz
Maximum Load Current	300mA
Inductor / Capacitor	L=10μH, $L_{Re\text{-}cycle}$=2.2μH / C_{load}=4.7μF, $C_{Re\text{-}cycle}$=4.7μF
Load Regulation	0.5mV/mA@V_{in}=12V, V_{out}=21V
Line Regulation	1.36mV/V@V_{out}=30V, I_{out}=80mA
Maximum CR Current	4A
Reference Tracking Speed	18us for 17V → 21V with I_{load} = 20mA 1.8ms for 21V → 17V with I_{load} = 20mA

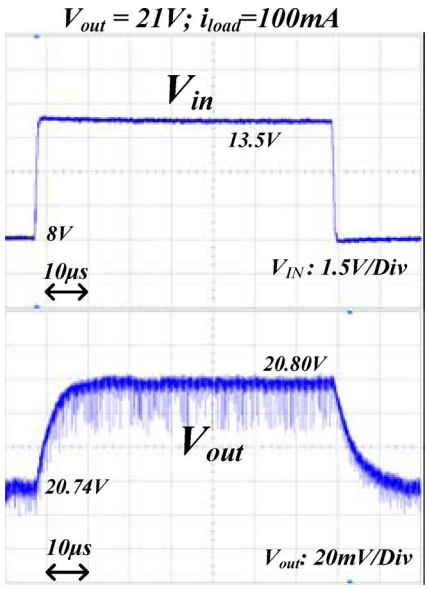

Fig. 24. Line regulation when input voltage changes from 8 V to 13.5 V and back to 8 V when load current is 80 mA.

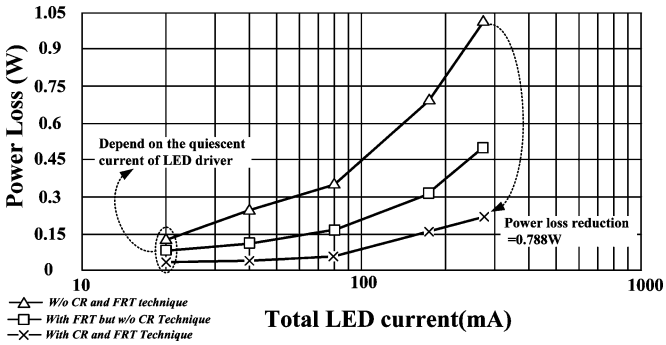

Fig. 25. Measured power loss of the LED driver with or without the FRT and CR techniques.

0.252 W. The power saving can achieve 0.788 W if the LED driver utilizes the proposed CR and FRT techniques. In addition, when the LED driver drives the one branch of the LED array, the current balance circuit consumes a little power. That is, the difference power consumption with or without CR and FRT technique is smaller than that of driving many branches of the LED array. The reason is the quiescent current of the LED driver dominates most of the power loss in driving one branch of the LED array. However, after the implementation of the CR and

Fig. 26. (a) The power consumption of LCD panel with color filter and CCFL backlight is larger than 5 W. (b) The power consumption of the color filterless LCD panel with the proposed RGB backlight driver is about 2-3 W.

FRT techniques, the power consumption on the current balance circuit still can be reduced. Furthermore, the transient response is also speeded up due to the restored charge by the CR technique. The performance summary is listed in Table I. Fig. 26(b) shows a notebook computer's 15.4' LCD panel is divided into three sections for the implementation of the FCS algorithm in Fig. 3. The color gamut is enhanced and the power consumption is reduced compared to the implementation with the CCFL backlight module as shown in Fig. 26(a).

V. CONCLUSION

An RGB LED backlight driver is proposed for rapidly switching between driving 6-series R- (about 16 V) and 6-series G-/B-LEDs (about 21 V). Owing to voltage difference about 5 V between driving series R- and series G-/B-LEDs, the FRT technique is presented to enhance line and load regulations. Besides, the CR technique stores extra energy on the recycling capacitor at the transition from high-supplying voltage (21 V) to low-supplying voltage (16 V). On other hand, it can restore the energy back to output node to speed up the raising of voltage back to 21 V at the stage of driving G-/B-LEDs. Both the transient response time and efficiency are enhanced. The proposed LED driver with the FRT and CR techniques was implemented in 0.25 μm TSMC BCD 40 V technology. Experimental results show that the load transition time can be reduced within 10 μs and the line transient response time can be reduced within 10 μs. It demonstrates the fast reference tracking performance achieved by the proposed FRT technique. The power consumption of the backlight module in the implementation of the FCS algorithm is smaller than 3 W. Furthermore, the power loss due to the LED driver can be effectively reduced to about 24% of the LED driver without CR and FRT techniques. The proposed LED driver with the

FRT and CR techniques can improve the reference tracking performance and reduce the power loss.

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