國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

2Gbps 低擺幅差動訊號傳輸之傳送器
A 2Gbps Reduced Swing Differential Signaling (RSDS) Transmitter

研 究 生　：　鄭鍵樺

指導教授　：　吳錦川　教授

中華民國九十四年八月


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碩士論文

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摘要

隨著積體電路製程技術的日新月異，處理器的運算速度愈來愈快，單位時間內處理的資料量也日益增多，通常，傳輸介面的電路所能達到的單位時間最大傳輸量往往是整體系統速度的關鍵限制，因此，本篇論文是描述一個應用於高速串列數位影像傳輸介面，使用低擺幅差動訊號傳輸之傳送器的設計，並致力於設計此傳送器之資料傳輸速度操作在 2Gbps 。

傳送器由一個四相位鎖相迴路、虛擬隨機位元串列產生器、二對一多工器和一擁有預先加強電路設計之輸出驅動器所組成，其中，四相位鎖相迴路的輸入頻率為125MHz，輸出為四個相位 平均分佈且頻率同為 1GHz 的時脈訊號，所包含的電路有相位/頻率偵測器、電荷幫浦、迴路濾波器、兩級差動壓控振盪器和一個除八的除頻器。此鎖相迴路所產生的平均分佈時脈提供給虛擬隨機位元串列產生器和二對一多工器，並將一組並列資料轉為串列輸出，再經由輸出驅動器並搭配預先加強電路，來增加傳送資料位元轉變期間所需的電流量，最後，將此串列資料傳送至傳輸線上，即完成整個傳送器的設計。

此傳送器採用 TSMC 0.35μm 2P4M CMOS 製程技術實現，當鎖相迴路輸入時脈為 66.67MHz 時，傳送器能正常傳送出 1066.67Mbps 的串列資料。

A 2Gbps Reduced Swing Differential Signaling (RSDS) Transmitter

Student：Chien-Hua Cheng　　Adviser：Prof. Jiin-Chuan Wu

Department of Electronics Engineering & Institute of Electronics
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Abstract

As the advancement of IC fabrication technology, the operation of processors has sped up. The amounts of data processed in each unit time become larger and larger as time goes by. For most of time, the key limitation of a whole system is the maximum data amounts of the transmission interface circuit transmitted in each unit time. Therefore, the thesis describes the design of a transmitter for a high-speed serial digital display interface by RSDS technique. We have devoted to design the data rate of the transmitter at 2Gbps.

The transmitter is composed of a four-phase PLL, PRBS circuits, 2-1 multiplexers and an output data driver with a pre-emphasis circuit. Among these devices, the input frequency of the four-phase PLL is 125MHz; it outputs four uniformly distributed clocks with 1 GHz frequency. The PLL comprises a Phase/Frequency Detector, a Charge Pump, a Loop Filter, a two-stage differential VCO and a divided-by-eight divider. It offers the PRBS and the 2-1 multiplexer with four uniformly distributed clocks to convert parallel pseudo-data into serial stream. Then, the serial data is transmitted by an output data driver with the pre-emphasis circuit. The pre-emphasis circuit is designed to increase the current during the data transition. In the end, the transmitter drives the serial data onto the transmission bus.

The transmitter is implemented in the TSMC 0.35μm 2P4M CMOS process. When the input reference frequency is 66.67MHz, the transmitter can transmit serial data at 1066.67Mbps successfully.

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鄭鍵樺

國立交通大學

中華民國九十四年八月

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Chapter 1

Introduction

1.1 Motivation

Over the last few years, the needs of the data processing applications in laptops and CRT replacement monitors have driven the performance requirement of LCD panels. As liquid crystal display televisions (LCD TVs) become the mainstream of high-end television market, the fundamental visual requirements have changed. LCD TVs are expected to achieve higher color depth, larger size, higher resolution, thinner profiles, and come with cinema-quality motion video. The increased requirements are driving the researches and designs on intra-panel interfaces to make progress day by day [1].

When we look at the interfaces of today, we see that high speed data links play a key role of the whole system due to the fact that the performance of many digital systems is limited by the interconnection bandwidth between different modules and/or chips. The primary components of the data links are transmitters, channels, and receivers. Among these components, high speed transmitters are expected to deliver larger amount of data in each unit time to reach for the required high speed data links.

The goal of this thesis is to design a CMOS serial data link transmitter with high speed based on the RSDS™ "Inter-panel" Interface Specification [2]. RSDS strands for Reduced Swing Differential Signaling. RSDS, like its predecessor LVDS (Low Voltage Differential Signal), originated from the LCD manufacturer's unique need for on glass interface with high speeds, reduced interconnect, low power, and a low EMI. Consequently, we are devoted to design the data rate of the transmitter at 2Gbps by means of RSDS™ specification.

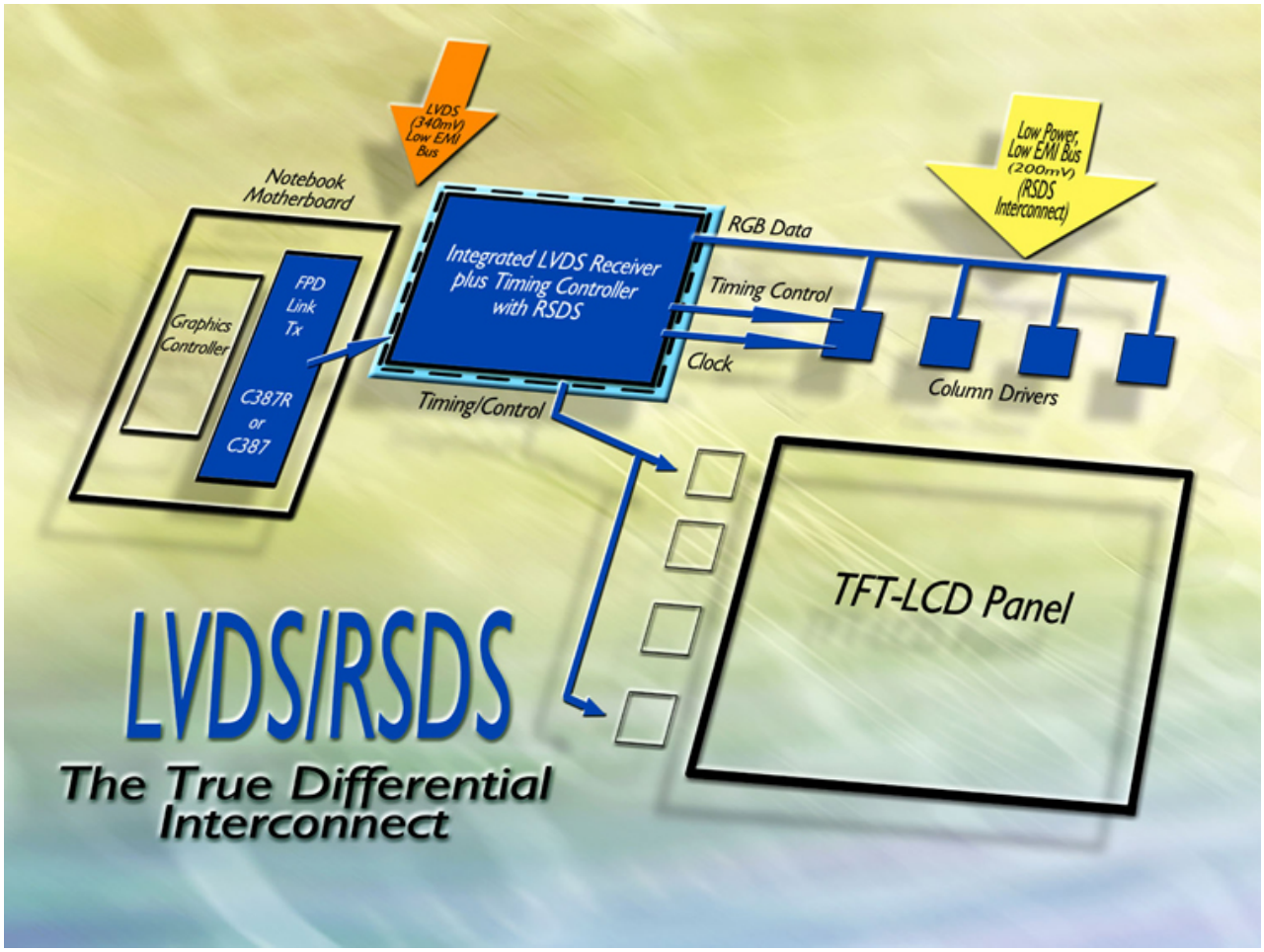


Fig. 1-1 RSDS technology used in energy-efficient Flat Panel Displays [3]

1.2 What is RSDS?

RSDS™ is an intra-panel interface bus standard. Fig.1-1 illustrates a typical

application block diagram of the TFT-LCD module. The RSDS™ buses are located between the Timing Controller (TCON) and the Column Drivers. RSDS™ interface is similar to LVDS interface, and they are similar except for their intended application. The primary difference of them is the output voltage swing scale (see Table 1-1). Since RSDS™ uses a low voltage differential swing (+/-200mV), lower EMI and lower power consumption can be realized. Furthermore, due to the low voltage swing, faster data rate can be achieved and higher resolution LCD TVs can be implemented in the future.

Table 1-1 RSDS and LVDS [4]

Characteristics	RSDS	LVDS
V_{OD} , Output Voltage Swing	+/- 200 mV	+/- 350 mV
R_{TERM}, Termination	100 Ω	100 Ω
I_{OD}, Output Drive Current	2 mA	3.5 mA
Data Mux	2:1	7:1
Content	RGB Data	RGB Data and Control
Application	Intra-system interface	System-System interface

1.3 Thesis Organization

This thesis consists of six chapters including the present chapter. Chapter 2 describes the background about the research of this thesis. It starts with the RSDS™ specification and brings out the considerations of the high speed serial link design. In chapter 3, the architecture and block circuits of the PLL which are the main portion of the transmitter are described clearly. Chapter 4 shows the whole architecture of the transmitter including the simulation results. The layout implementation and the measurement results of the

transmitter are given in Chapter 5. Finally, Chapter 6 summaries this work, draws a conclusion and discusses the future development about this thesis.

Chapter 2

Background

2.1 RSDS™ Specification [2]

2.1.1 Scope

RSDS™, Reduced Swing Differential Signaling, is an intra-panel interface bus standard. The RSDS™ standard defines the characteristics of transmitter and receiver along with the protocol for a chip-to-chip interface. The RSDS™ interface standard is intended to cover electrical characteristics and protocol of the data only. Additional Control signals that are required by the Source (Column) Driver and/or Gate (Row) Drivers are not covered in this specification, as they are unique to the specific LCD manufacturer's design.

2.1.2 Introduction of RSDS

The RSDS™ bus provides many benefits to the applications that include the following：

- Reduced bus width – enables smaller and thinner column driver boards
- Lower Dynamic power dissipation – extends system run time

- Low EMI generation – eliminates EMI suppression components and shielding
- High noise rejection – maintains signal image
- High throughput – enables high resolution display

The RSDS™ interface is intended to be used in display applications with resolutions between VGA through UXGA or higher. Higher resolution support is scaleable with RSDS™ and is only limited by the RSDS™ bus bandwidth supported by the transmitter/receiver pair.

2.1.3 System Diagram

Fig. 2-1 depicts a typical application block diagram of the LCD Module. The RSDS™ bus is located between the Panel Timing Controller and the Column Drivers. There are several connection schemes allowed which are discussed in the bus configuration section. This bus is typically nine pair wide for 6bit/color plus clock and is a multi-drop bus configuration, 1 transmitter and multiple receivers.

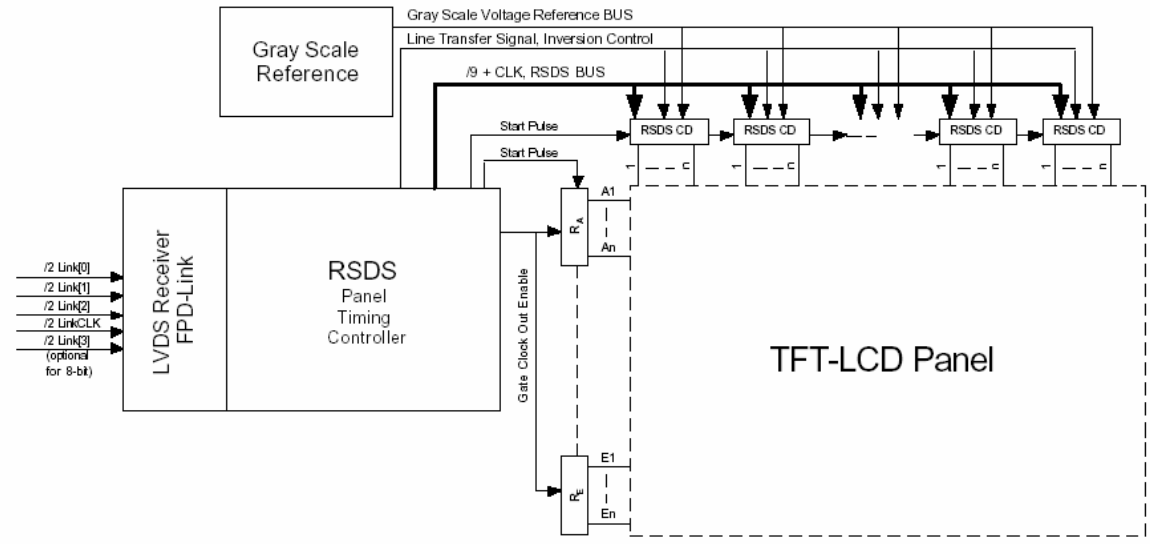


Fig. 2-1 Block Diagram of the LCD Module with Discrete Timing Controller

2.1.4 Electrical Specification

A typical RSDS™ interface circuit is shown in Fig. 2-2. The circuit contains three parts：a transmitter (TX), receivers (RX) and a balanced interconnecting medium with termination.

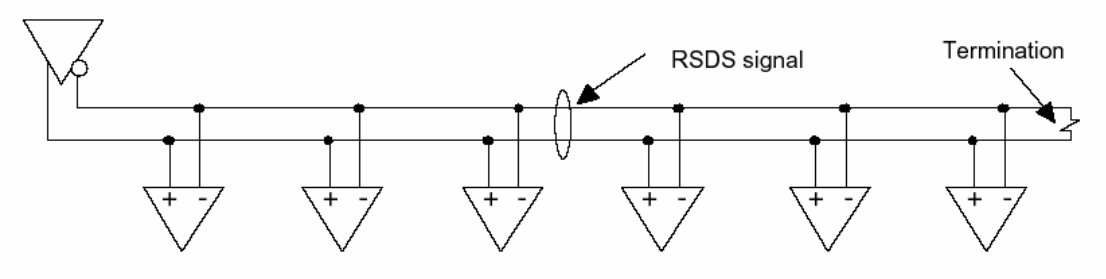


Fig. 2-2 RSDS™ Interface

2.1.5 RSDS™ Transmitter Characteristic

The Driver output consists of two complimentary outputs that are terminated at the end of the Data Bus. A differential voltage is generated from two single-ended outputs of the transmitter. As in LVDS, the single-ended outputs alternate between sourcing and sinking of a constant current. The differential voltage is the product of this constant current across the terminating resistance R_L as shown in Fig. 2-3.

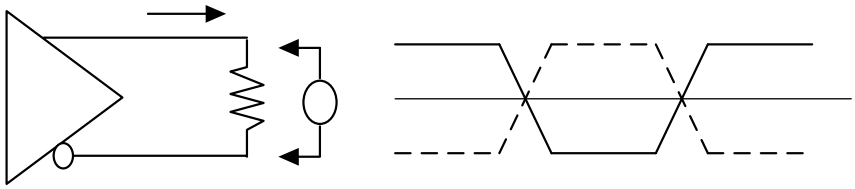


Fig. 2-3 RSDS™ reference circuit and transmitter output

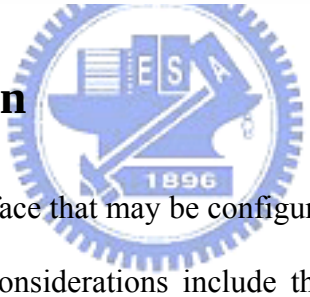
Due to a wide variation in the characteristic impedance of the transmission media (25Ω to 100Ω), it is recommended that the transmitter be designed with the capability to drive such loads with a minimal amount of signal integrity artifacts such as reflection, ringing,

overshoot, undershoot.

The following specifications (see Table 2-1) apply to both clock and data pairs over a specified range of termination resistance values and operating voltages.

Table 2-1 Electrical Specifications of RSDS™ transmitters

Parameter	Definition	Conditions / Note	MIN	TYP	MAX	Units
V_{OD}	Differential Output Voltage (Figure 4)	R_L = 100 Ohm	100	200	600	| mV |
V_{OS}	Offset Voltage (Figure 3)		0.5	1.2	1.5	V
I_{RSDS}	RSDS Driver Current		1	2	6	mA
T_R/T_F	Transition Time: Rise, & Fall (Figure 6)	20% to 80%, VOD =200 mV, CL ≅ 5 pF		500		ps
	RSDS Clock Duty Cycle		45	50	55	%



2.1.6 Bus Configuration

The RSDS™ is a versatile interface that may be configured differently depending upon the end application requirements. Considerations include the location of the TCON, the resolution of the panel, and the color depth for example. The common implementations include the following bus types：

- **Type 1 – Multi-drop bus width double terminations (shown in Fig. 2-4)**

In a Type 1 configuration, the source (TCON) is located in the center of the bus via a short stub. The bus is terminated at both ends with a nominal termination of 100 Ω. The interconnecting media is a balanced coupled pair with ideal (unloaded) differential impedance of 100Ω. However in actual applications the bus impedance can be much lower than ideal due to the additional loading or PCB characteristics. The number of RSDS™ data pairs is 9 or 12 depending upon the color depth supported. In this application, the RSDS™

driver will see a DC load of 50Ω instead of 100Ω. In this case, the output drive of the RSDS™ driver must be adjusted to comply with the VOD specification with the 50Ω load presented in the type 1 configuration.

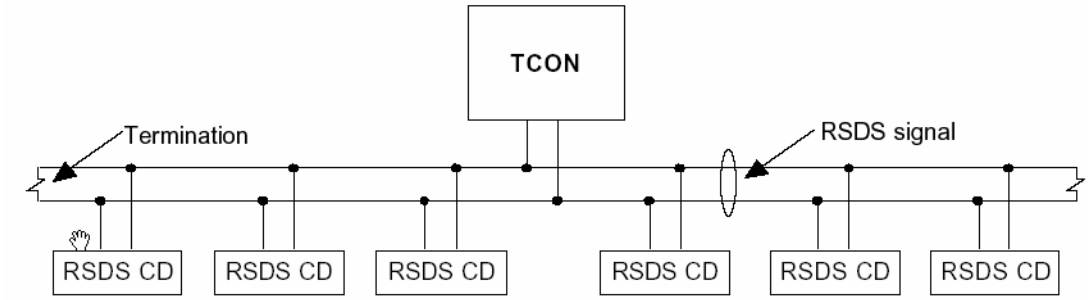


Fig. 2-4 Type 1 Bus Configuration

- **Type 2 – Multi-drop bus with single end termination (shown in Fig. 2-5)**

In a Type 2 configuration, the source (TCON) is located at one end of the bus. The bus is terminated at the far end with a nominal termination of 100Ω. The interconnecting media is a balanced coupled pair with nominal (unloaded) differential impedance of 100Ω. The bus may be a single or dual bus depending upon the panel's resolution. The number of RSDS™ data pairs is 9 or 12 depending upon the color depth supported for a single bus.

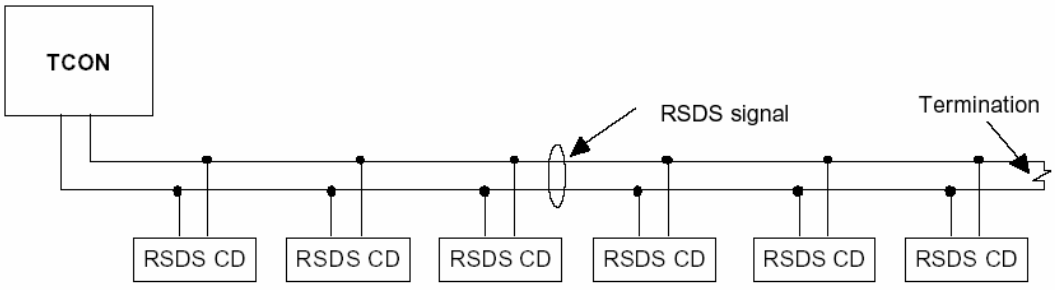


Fig. 2-5 Type 2 Bus Configuration

- **Type 3 – Double multi-drop bus with single termination (shown in Fig. 2-6)**

In a Type 3 configuration, the source (TCON) is located in the center of the application. There are two buses out of the TCON that run to the right and left respectively. Each bus is terminated at the far end with a nominal termination of 100Ω. The interconnecting media is

a balanced coupled pair with nominal (unloaded) differential impedance of 100Ω. The number of RSDS™ data pairs is 9 or 12 depending upon the color depth supported for a single bus for each bus. Note that the connection of the TCON to the main line is not a stub in this configuration, but rather a part of the main line. This helps to improve signal quality.

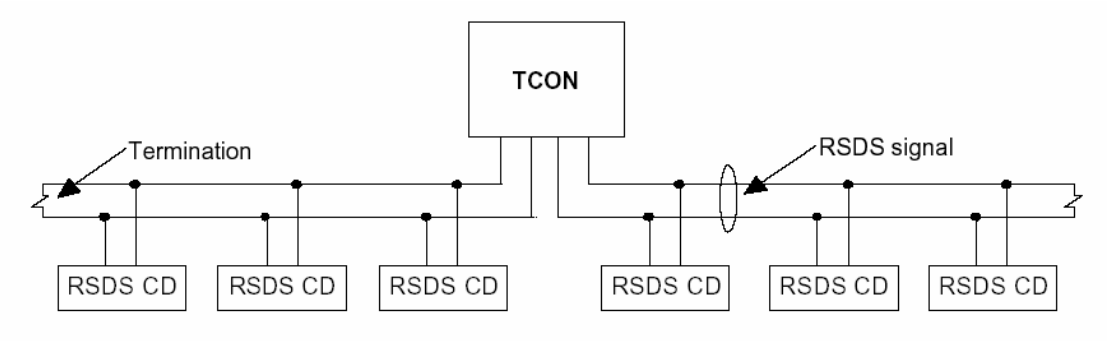


Fig. 2-6 Type 3 Bus Configuration

Note that in Fig. 2-4, 2-5 and 2-6, the complete bus is not illustrated; only a single RSDS™ pair is shown. The number of column drivers on the bus is also application specific and depends upon the panel resolution and also if a single or dual bus is used.

2.2 Basic Link Design

A general serial link is composed of three primary components：a transmitter, channels, and a receiver, as shown in Fig. 2-7. The data before transmission are usually arranged in parallel form in order to increase the bandwidth of the link. The transmitter has to convert the parallel data into serial stream before the output driver drives signals onto the channels. RSDS™ uses differential data transmission to deliver the serial data stream and the transmitter is configured as a switched-polarity current generator. A differential load resister at the receiver end provides current-to-voltage conversion. For operation in the Gbps range, an additional termination resistor is usually placed at the source (transmitter) end to

suppress reflected waves caused by crosstalk or by imperfect termination, due to package parasitic effect and component tolerance. Moreover, RSDS™ uses a lower voltage swing to achieve further advantages in terms of reduced crosstalk and radiated EMI. Therefore, the double termination scheme is used and the termination resistors are integrated in the transmitter (R_{T-T}) and in the receiver cell (R_{T-R}) [5].

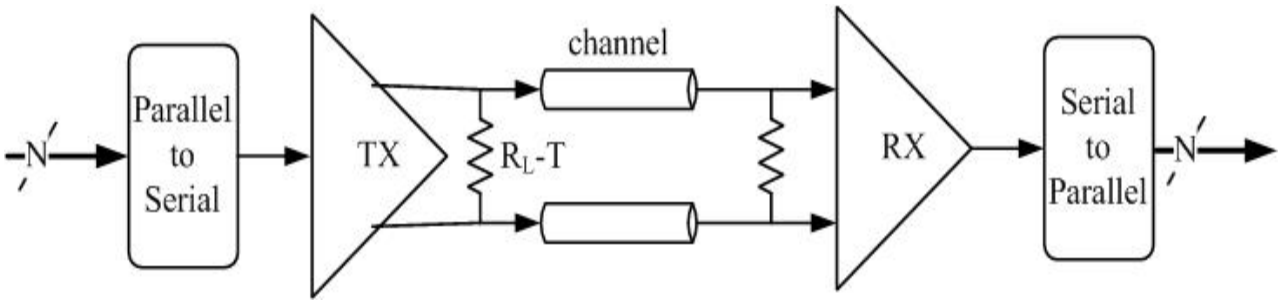


Fig. 2-7 Block diagram of the basic serial link

After the data are transmitted onto the channels successfully, the receiver amplifies and samples the received bit stream. The clock recovery circuit restores the clock of transmitter by detecting the transition edge of received data. Eventually, the receiver gets back the correct data by sampling the center point of the received bit stream at each transition edge of the recovered clock.

2.3 Interface Consideration

The RSDS™ bus can provide reliable, low power, low EMI data transmission at rates that exceed the requirements of XGA system with a 75Hz refresh rate. In order to build the most robust RSDS™ interface, certain precautions need to be taken. There are three main considerations for an RSDS™ based application[6]：

- RSDS™ Bus Configuration

For XGA and SXGA panels, there are three types of RSDS™ bus configurations, which are outlined in section 2.1.6. All of the bus configurations should be implemented in 50 Ω transmission lines. Each of them requires slightly different terminations and supply currents. Therefore, choosing the appropriate bus configuration is critical to a good system design.

- RSDS™ Layout

In general, a RSDS™ bus should be routed and laid-out with the same consideration as any high speed differential bus. The following are some of the basic high speed differential routing principles：

- Positive and negative traces of a differential pair should be the same length and routing as close together as possible
- Spacing between differential pairs should be double the spacing within a differential pair
- Changing layers along the bus should be minimized
- The number of vias attached to a bus should be minimized
- The bus should be electrically separated from other dynamic signals to minimize noise and crosstalk
- Forty-five degree angles should be used instead of right angles when changing the bus direction

- RSDS™ Bus Termination

The generalizations used are not exactly accurate and there will still be some inefficiency in the termination scheme. The error is caused by the fact that the RSDS™ bus is loaded with connections to 8 or 10 column drivers, each of which can be approximated by

a capacitive load on the bus line (typically 2-5pF per connection). Fig. 2-8 shows an example with the column driver capacitive loading included. The net result of the capacitive loading is to decrease the effective impedance of the traces. In order to better match the reduced impedance, the termination resistor may have to be lowered. Empirical evidence indicates that the termination resistor should be around 70 Ω in order to provide the best impedance that matches the differential traces.

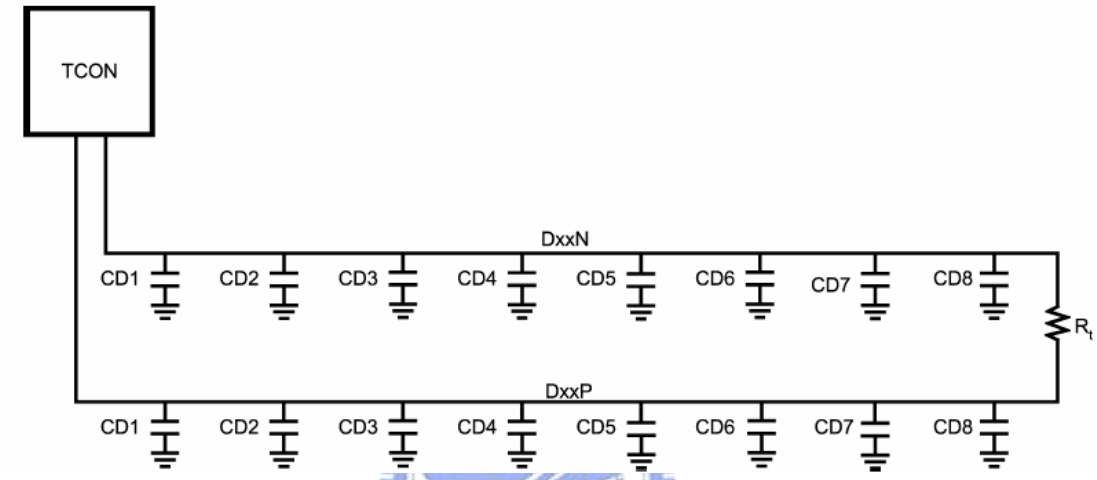


Fig. 2-8 Loading of RSDS Bus [6]

2.4 Eye Diagram

A transmitter delivers signals based on a kind of selected interface specification. When long stream bits of data are conveyed, it is inefficient and non-smart to check the bits one by one. Therefore, an eye diagram is made to understand the characteristics of transmitted bits conveniently.

An eye diagram of a signal overlays the signal's waveform over many cycles. Each cycle's waveform is aligned to a common timing reference, typically a clock. An eye diagram provides a visual indication of the voltage and timing uncertainty associated with the signal. The vertical thickness of the line bunches in an eye diagram indicates the

magnitude of AC voltage noise; whereas the horizontal thickness of the line bunches where they cross over is an indication of the AC timing noise or jitter. Fixed DC voltage and timing offsets are indicated by the position of the eye on the screen. The size of the eye opening in the center of an eye diagram indicates the amount of voltage and timing margin available to sample this signal. Thus, for a particular electrical interface, a fixed reticule or window could be placed over the eye diagram showing how the actual signal compares to minimum criteria window, know as the eye mask. If a margin rectangle with width equal to the required timing margin and height equal to the required voltage margin fits into the opening, then the signal has adequate margins.

Chapter 3

Phase-Locked Loop

3.1 Introduction

Phase-locked loops (PLL) are analog building blocks used extensively in many analog, digital and communication systems. Their use has become attractive for many applications such as clock recovery, frequency synthesizers, FM demodulators and others. These are only few applicable areas, but PLL has undoubtedly become an important building block in many electronic systems. Recently, as the needs for high speed data transmissions rise, the PLL technique plays a key role to implement the demand. In this chapter we first explore the architecture of the PLL, and then explain the circuit implementations for the PLL to achieve the clock rate at 1GHz. In this transmitter, we need a pair of complementary clock signals with 1GHz frequency to trigger the output driver. The detailed discussion of the transmitter operation will be shown in next chapter. The linear model, the noise and the stability are all taken into consideration in 3.4 and 3.5, followed by a section discussing the flow of design and the way to make proper decision on loop parameters of the PLL. The simulation results are presented in the final section of this chapter.

3.2 Architecture of PLL

Fig. 3-1 shows a block diagram of the basic PLL system. The system consists of a phase/frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator (VCO) and a frequency divider. The VCO is simply an oscillator whose frequency is proportional to an externally applied voltage. Before inputting the clock at reference frequency (Ref_CLK), the VCO oscillates at its free-running frequency. When the Ref_CLK signal is input, the phase/frequency detector detects both the Ref_CLK and the feedback signal (Fb_CLK). Afterward the detector and the charge pump produce a dc or low frequency signal proportional to the phase difference between Ref_CLK and Fb_CLK. The loop filter acts as a low pass filter and is used to extract the average value from the output of the charge pump. This signal is then amplified and used to drive the VCO. The VCO's oscillation frequency will be changed by the control voltage (V_{ctrl}) according to the reference frequency. A frequency divider being used in the diagram, the output clock's frequency of the VCO will be N times of the Ref_CLK signal. When the loop is locked, the negative feedback of the loop results in the output of the VCO being synchronized with the input signal. Moreover, the input signal (F_{ref}) and the feedback signal (F_b) are phase-aligned. The PLL turns out to be able to lock to the input signal successfully.

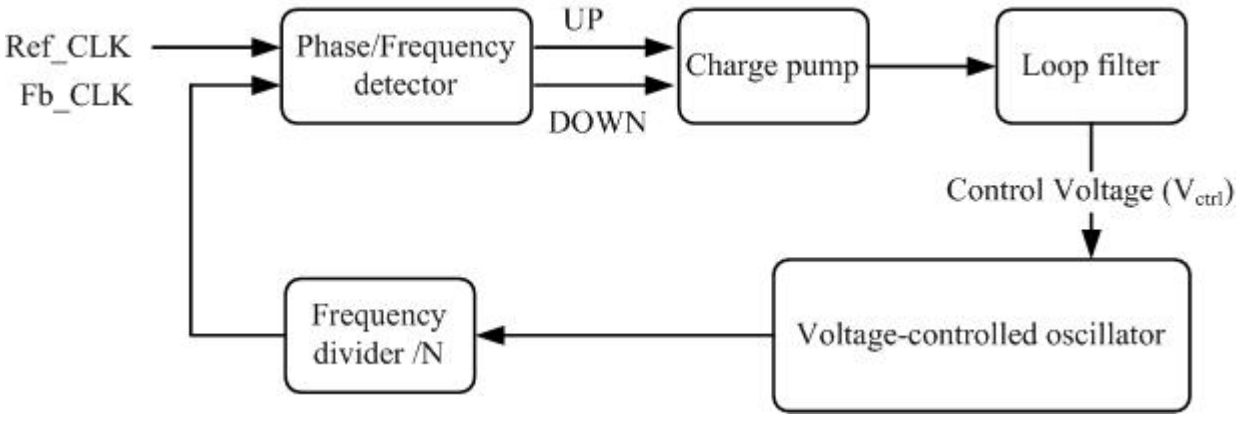


Fig. 3-1 Functional block diagram of charge pump PLL

3.3 Circuit Implementation

3.3.1 Phase/Frequency Detector

The phase/frequency detector (PFD) is a digital sequential circuit built based on a tri-state operation. It is used to detect the phase difference between the reference (Ref_CLK) and the feedback (Fb_CLK) signals. Fig. 3-2 shows the implementation of PFD [7][8]. The PFD is composed of two high speed TSPC (True-Single-Phase-Clocking [9]) D-flip flops, a NOR gate, inverters and a buffer in the reset path.

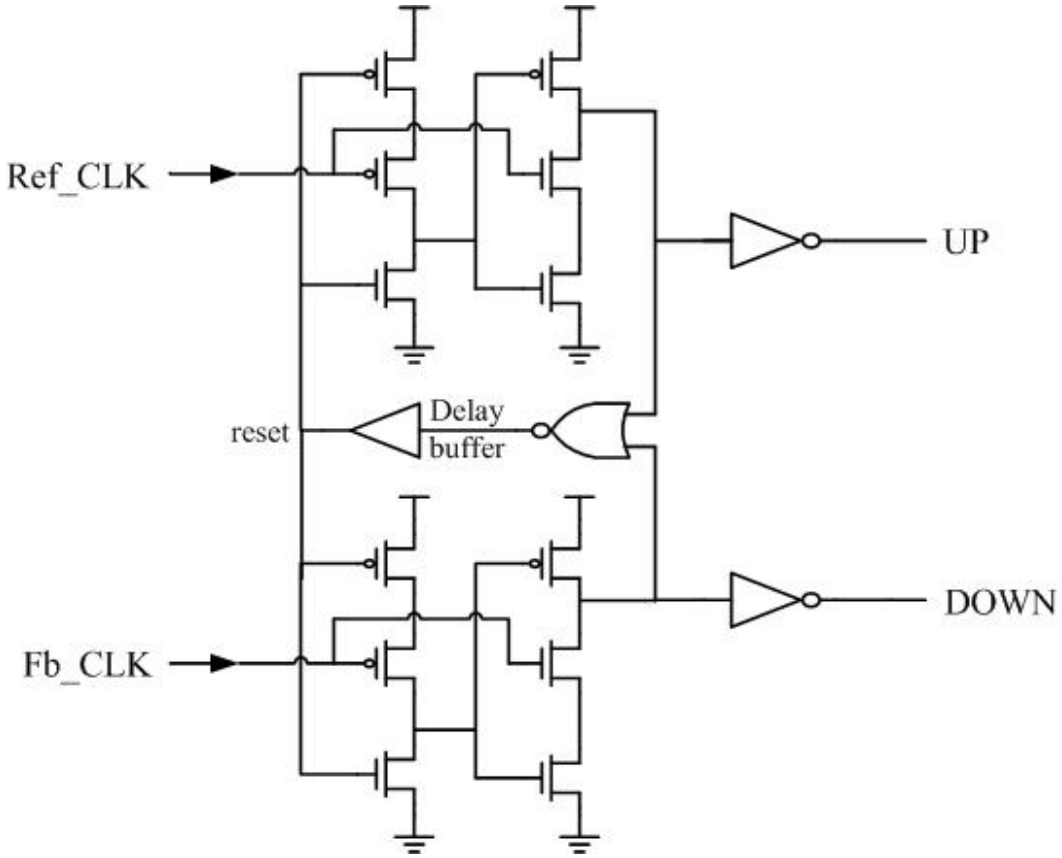


Fig. 3-2 Phase/Frequency detector with TSPC D-flip flops

The PFD is triggered by the positive edges of the Ref_CLK and the Fb_CLK. It detects the phase difference between them and outputs two signals, UP and DOWN, to represent the phase relationship of them as shown in Fig.3-3. If the Ref_CLK and the Fb_CLK are in

phase, the output waveforms of UP and DOWN will be the same. The controlled voltage and the oscillation frequency of the VCO remain invariable.

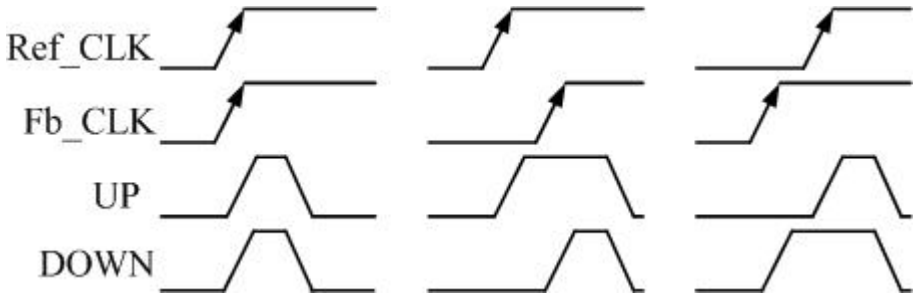


Fig. 3-3 Operation of PFD

When the Fb_CLK lags the Ref_CLK, the UP signal will be switched from low to high first. This will in turn increase the frequency of the VCO and the Fb_CLK signal. Then the positive edge of the Fb_CLK arrives and the DOWN signal will be switched from low to high, too. When both UP and DOWN signals are set at high, the reset signal will thus be turned to high in order to reset them to low. The comparison between Ref_CLK and Fb_CLK in this cycle is finished. In contrast, if the Fb_CLK leads the Ref_CLK, the output signals, UP and DOWN, of PFD will be used to decrease the frequency of the VCO and the Fb_CLK signal. This type of operation has a linear range of $\pm 2\pi$ and can act as both a phase detector and a frequency detector. This property will greatly enhance the locking range.

A low precision PFD has a wide dead zone as shown in Fig. 3-4, which results in increased jitter. Ideally, the PFD should have the ability to distinguish any phase error between Ref_CLK and Fb_CLK. The dead zone will occur in practical exercises when the loop is in a lock mode and the PFD cannot detect the small phase difference of Ref_CLK and Fb_CLK. The detected phase error will thus remain zero and this will result in an increase of unavoidable jitter of the PLL.

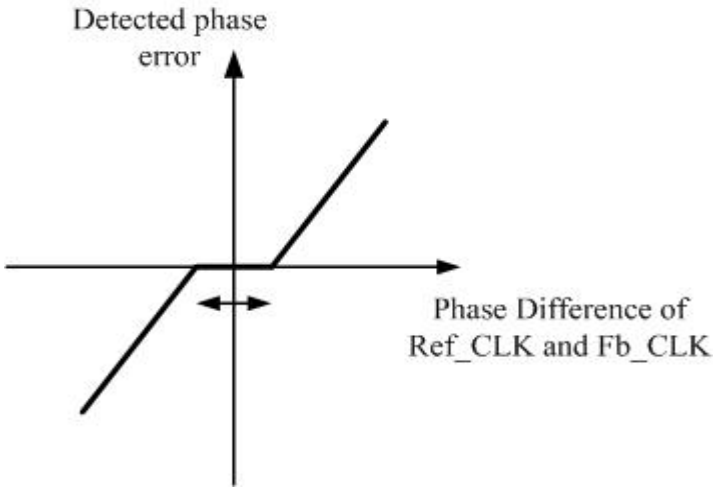


Fig. 3-4 The PFD dead zone

The delay buffer in the reset path is used to avoid the occurrence of dead zone. For in-phase inputs of Ref_CLK and Fb_CLK, the charge pump will see both UP and DOWN pulses for the same short period of time. If there is a phase difference between Ref_CLK and Fb_CLK, the width of UP and DOWN pulses will be proportional to the phase difference of the inputs. Fig.3-5 shows the SPICE simulation result of the proposed PFD circuit.

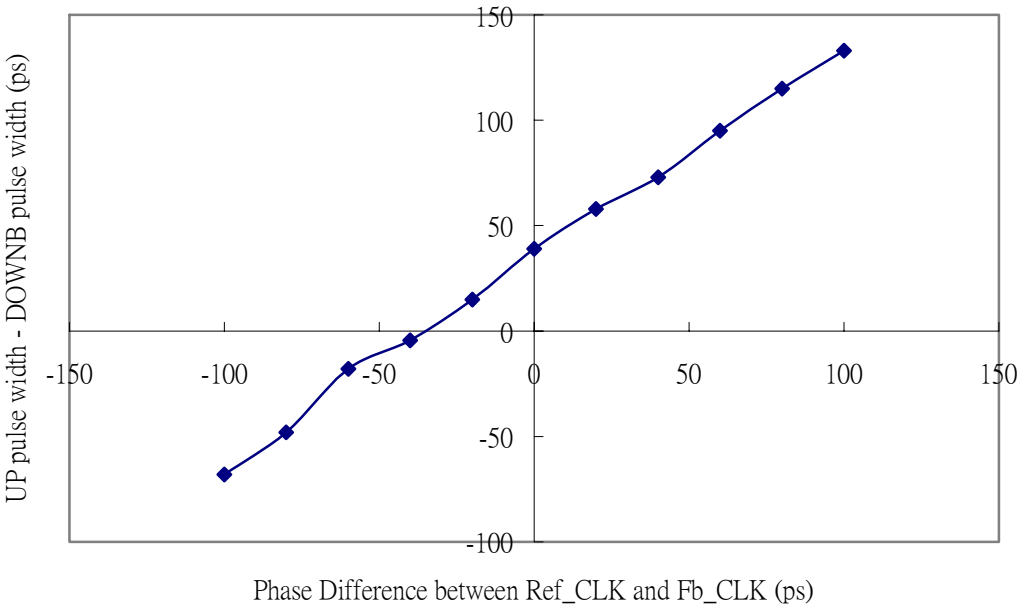


Fig. 3-5 simulation result of PFD without dead zone

3.3.2 Charge Pump

The charge pump (CP) cooperates with the PFD to change the control voltage of the VCO. The circuit implementation of the charge pump is shown in Fig. 3-6 [10]. It can charge and discharge the capacitance of the loop filter to vary the V_{ctrl} according to UP and DOWNB signals from the PFD. There are some problems in conventional charge pump circuits such as charge injection and clock feed through. These problems will result in a phase offset at the input of the PFD when the PLL is locked. In order to overcome these problems, the two switch devices are separated from the output voltage. Therefore, the output voltage is now isolated from the switching noise resulting from the overlap capacitance of the two switch devices. In addition, the intermediate node between the current source and switch devices will charge to the output voltage only by the gate overdrive of the current source devices, $V_{gs} - V_t$, an amount independent of the output voltage. The charge pump circuit can therefore control V_{ctrl} and successfully reduce the static phase offset.

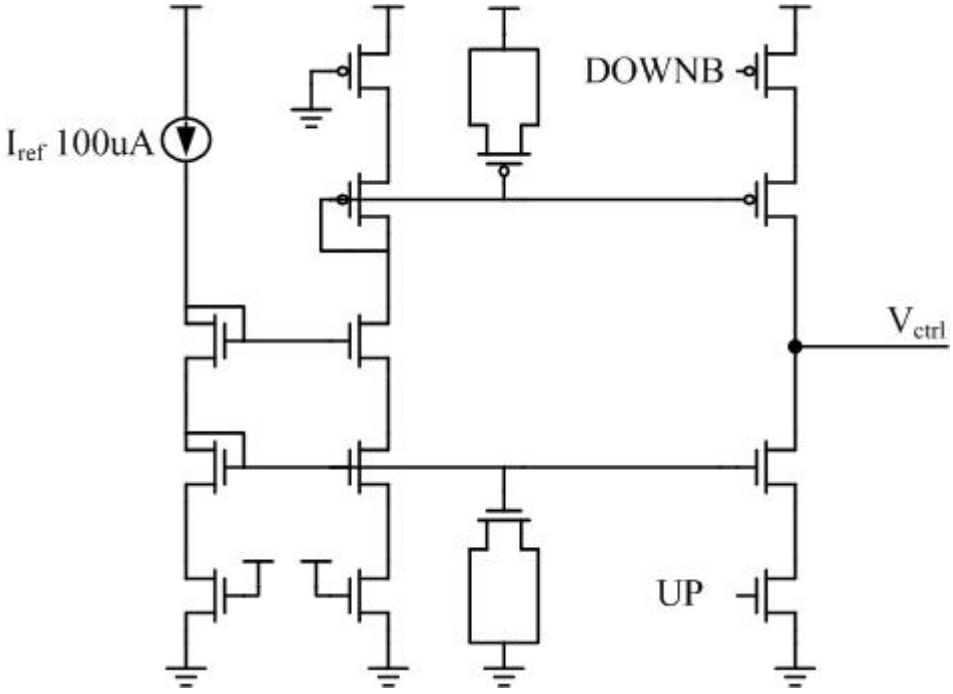


Fig. 3-6 Schematic of the charge pump

3.3.3 Loop Filter

The loop filter (LF) is a low pass filter used to extract the average value from the charge pump output. The schematic of the loop filter is shown in Fig. 3-7. It is usually composed of a resistor R_1 in series with capacitor C_1 and a capacitor C_2 in parallel.

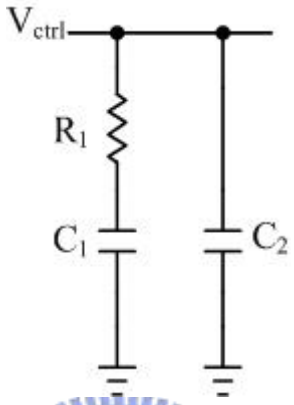


Fig. 3-7 Schematic of the loop filter

The loop filter provides a pole in the origin to provide an infinite DC gain so as to minimize the static phase error. The resistor R_1 and capacitance C_1 provide a zero in the open loop response in order to improve the phase margin to ensure overall stability of the loop. Finally, the use of the capacitance C_2 is to reduce the ripple noise on V_{ctrl} to mitigate the frequency jump. The transfer function of the loop filter can be expressed as

$$F(s) = Kh \times \frac{(s+\omega_z)}{s \times (1+s/\omega_p)} \tag{3-1}$$

and where

$$Kh = \frac{R_1 \times C_1}{C_1 + C_2} \quad , \quad \omega_z = \frac{1}{R_1 C_1} \quad , \quad \omega_p = \omega_z \times (1 + \frac{C_1}{C_2}) \tag{3-2}$$

The use of the capacitance C2 will make the overall PLL system third-order and affect the stability of the loop. In general, when the capacitance C_2 is much smaller than C_1, the third-order loop can be approximated to a second-order one.

3.3.4 Voltage Controlled Oscillator

The building blocks of the VCO include a replica-feedback current source bias circuit, a two-stage ring oscillator, differential-to-single-ended converter circuits and duty-cycle corrector circuits as shown below.

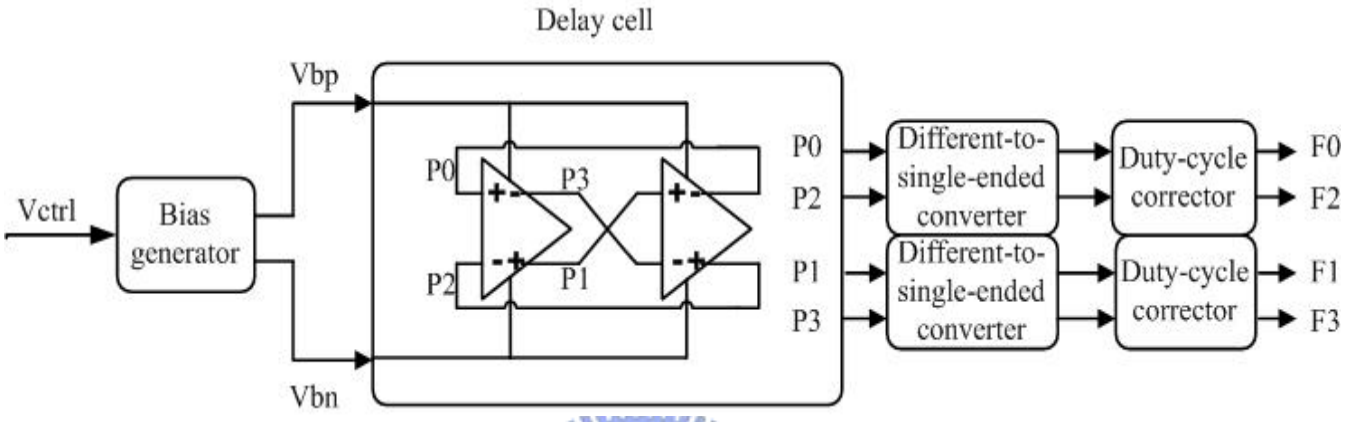


Fig. 3-8 Architecture of the VCO

The VCO is eventually designed to produce four full swing clock signals, F0~F3, at 1GHz frequency. In order to achieve low jitter operation, the circuit should have low power and substrate noise sensitivity. The VCO design is based upon the differential buffer delay cells with symmetric loads and replica-feedback biasing.

The replica-feedback current source bias circuit, shown in Fig. 3-9 [11], produces the bias voltages V_{bp} and V_{bn} from V_{ctrl}. It is used to continuously adjust the buffer bias current to provide the correct lower swing limit of V_{ctrl} for the buffer delay cells. If the supply voltage changes, the differential amplifier will adjust to keep the swing and thus the bias current constant. In so doing, it establishes a current that is held constant and independent of supply voltage. Besides, the bias generator also provides a buffered version of V_{ctrl} at the V_{bp} output using an additional Vctrl buffer. The buffer can isolate the control voltage V_{ctrl} from the capacitive coupling of the VCO delay cells.

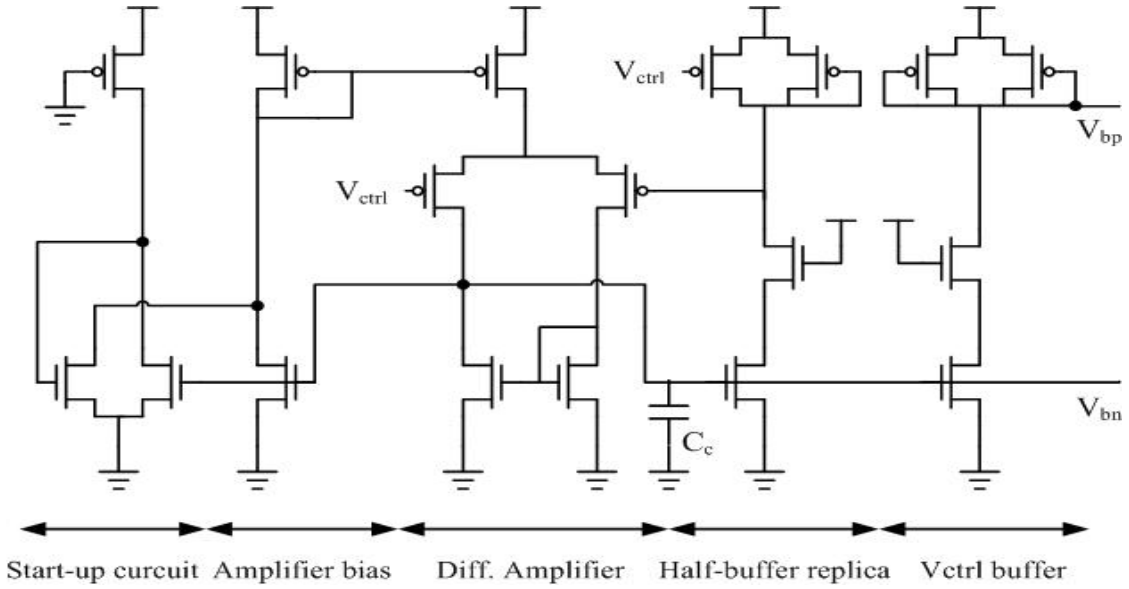


Fig. 3-9 the replica-feedback current source bias circuit

In order to achieve the goal of high speed and low power consumption, the two-stage ring oscillator architecture is chosen [12][13]. However, a conventional differential delay cell fails to satisfy the oscillation conditions. If the conventional delay cell is used in a two-stage ring oscillator, the system will not oscillate because the gain is under 0dB at the frequency in which the absolute phase changes 90°(180°/N), causing the insufficient gain problem. Therefore, the circuit implementations of the proposed delay cells are shown in Fig. 3-10. The designed characteristics are obtained by means of the positive partial feedback.

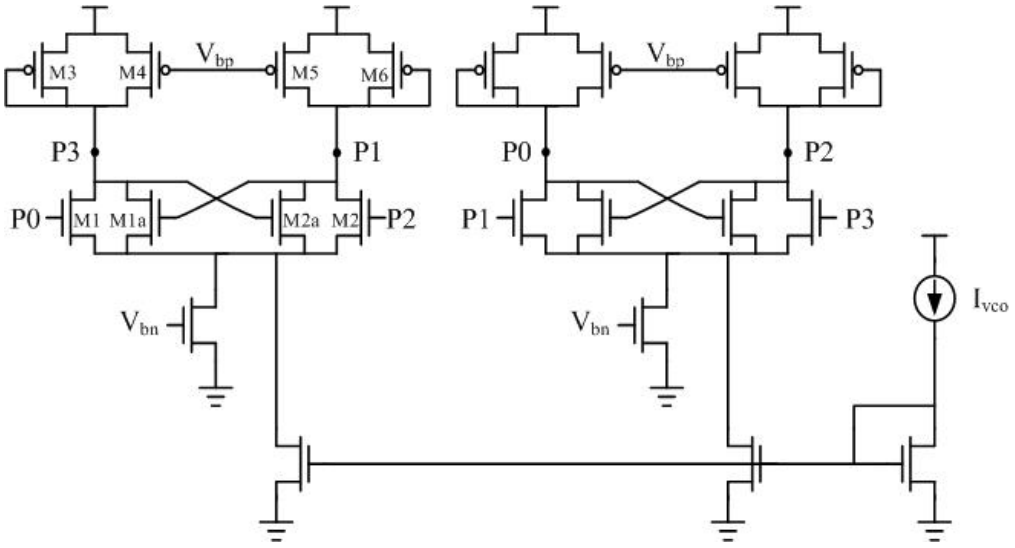


Fig. 3-10 Differential delay cells with partial positive feedback

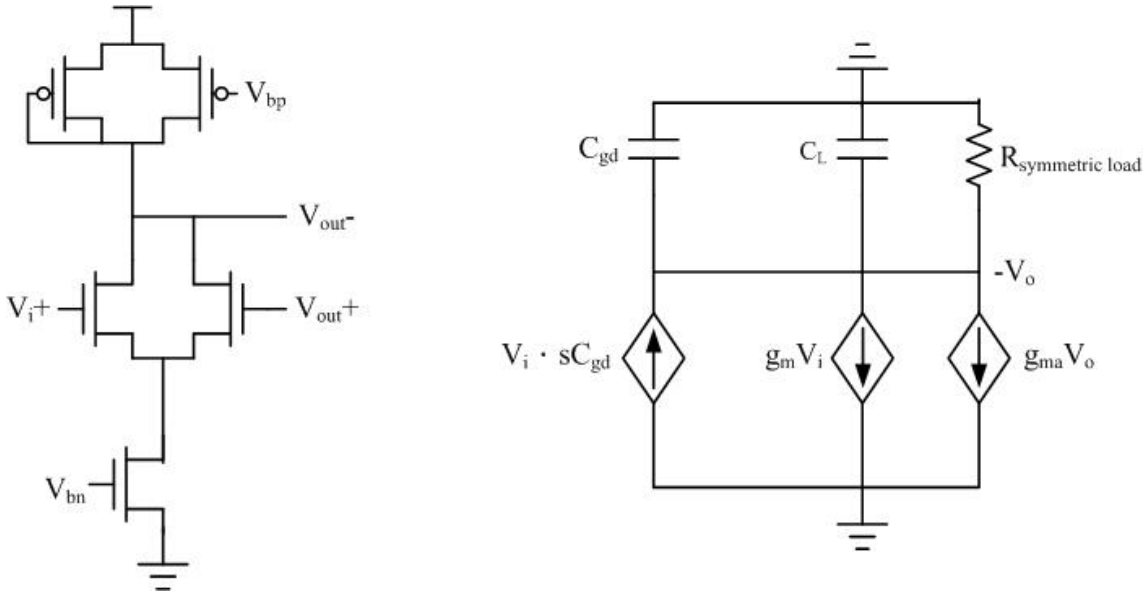


Fig. 3-11 Half-circuit and small signal model of a delay cell

As shown in Fig. 3-11, the transfer function of the proposed delay cell can be written as below

$$H(s) = A_0 \left[\frac{s/\omega_z - 1}{s/\omega_p + 1} \right] \tag{3-3}$$

where

$$A0 \approx \frac{g_m R}{1 - g_{ma} R} \quad , \quad \omega_p \approx \frac{g_m}{C_{gd}} \quad , \quad \omega_z \approx \frac{1 - g_{ma} R}{(C_L + C_{gd}) R} \tag{3-4}$$

where g_m and g_{ma} are respectively the transconductances of M1-M2 and M1a-M2a, C_{gd} is the gate-drain capacitance of M1-M2, C_L is the capacitance associated with one of the output nodes and R is the resistance of the symmetric load.

The symmetric load consists of a diode-connected PMOS device and an equally sized PMOS device as shown in Fig. 3-12. The effective resistance of it is directly proportional to the small signal resistance at the ends of the swing range which is just one over the transconductance for one of the two equally sized devices. The symmetric load can also cancel the first order of the common mode voltage noise. Therefore, it is used to have high dynamic supply noise immunity and provide high small-signal resistance.

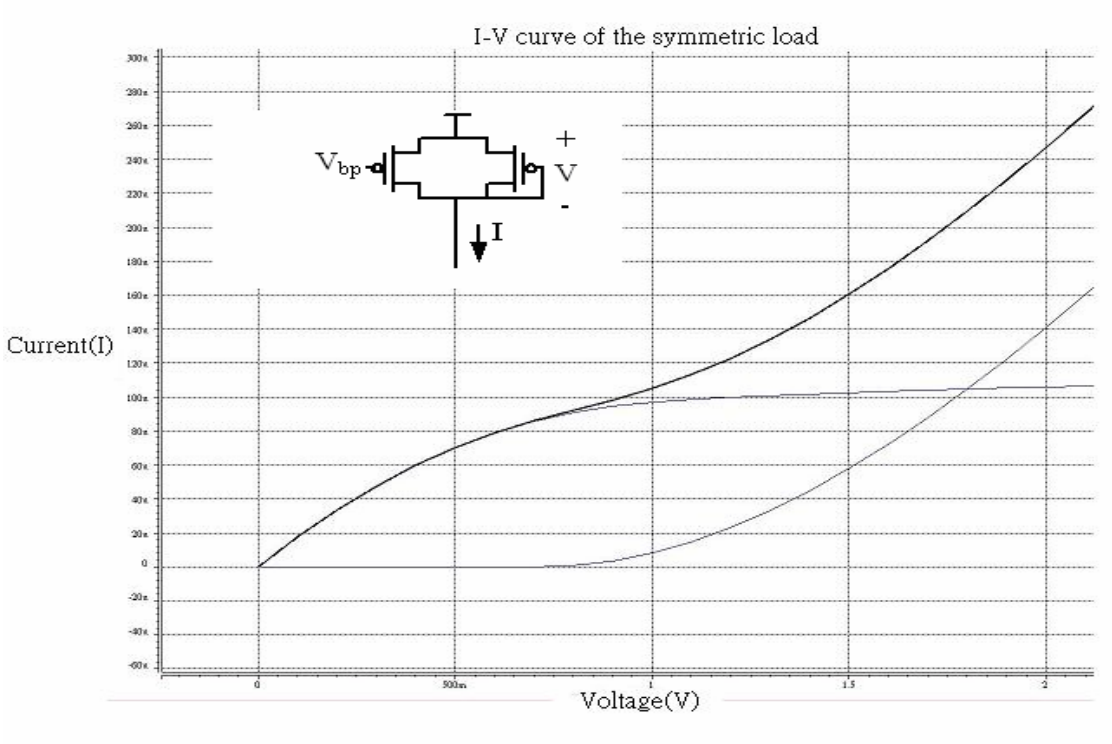


Fig. 3-12 Typical symmetric load and I-V characteristic

Substituting s=jω in the phase of equation (3-3) and making it equal to 90°, the oscillation frequency of the VCO is given by

$$\omega = \sqrt{\omega_z \times \omega_p} \tag{3-5}$$

The current source $I_{vco,}$ shown in Fig. 3-10, enables the establishment of a minimum current in the delay cells. The oscillation frequency does not disappear even when the control voltage does not fall in its nominal range. On the other hand, the VCO oscillates at an essential frequency. This can reduce the amount of the K_{VCO} to decrease the negative effect caused by the noise for the PLL.

The output clock signals from the delay cells swing in a small range and additional circuits are required to become full swing. In Fig. 3-13, the schematic of differential-to-single-ended converter is presented to amplify the input signals. According to Vbn, the circuit corrects the input common-mode voltage level and provides signal amplification.

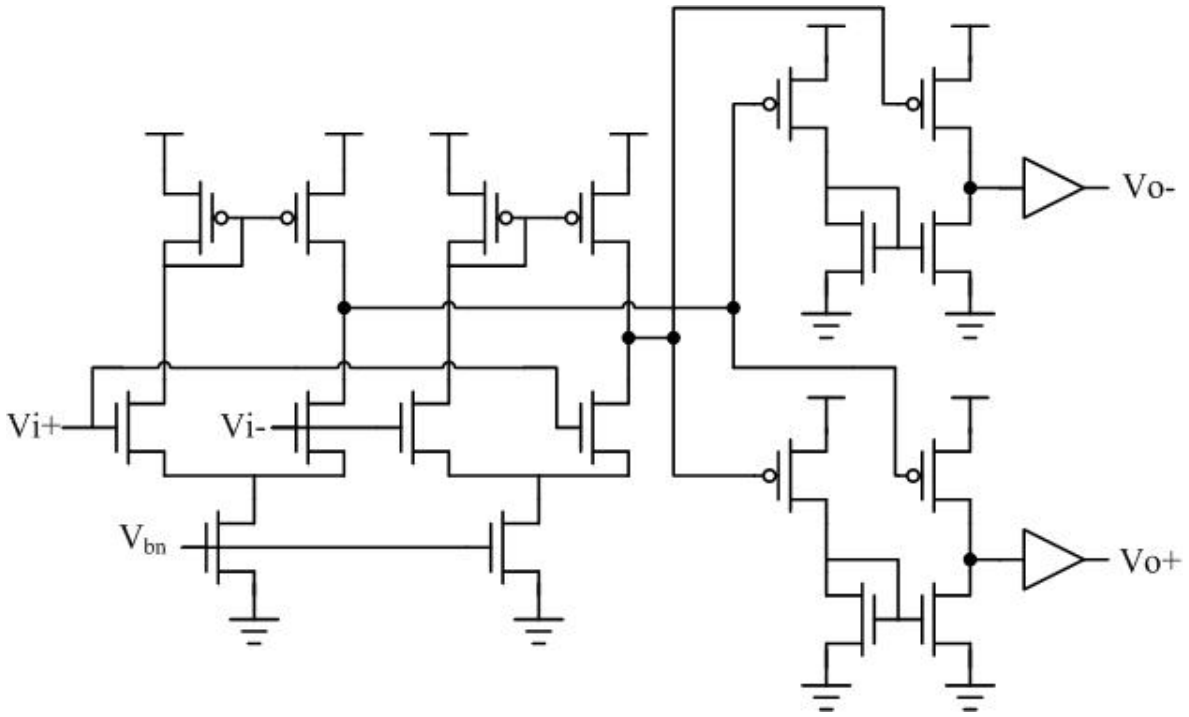


Fig. 3-13 Schematic of differential-to-single-ended converter

Maintaining a 50% duty-cycle ratio for clock signals is extremely important. The feedback clock signal to the PFD also needs a 50 % duty-cycle single-ended signal. The duty-cycle corrector [14], as shown in Fig. 3-14, utilizes multiphase signals generated from the two-stage differential VCO. The signals, Vo+ and Vo-, are used to charge and discharge the output node alternately. Since this duty-cycle corrector consists of only two transmission gates and two inverters, the silicon area is minimal and the power consumption is negligible.

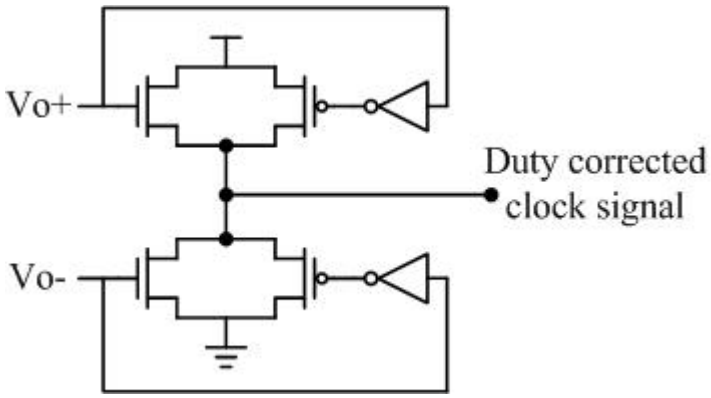


Fig. 3-14 Feed forward-type duty-cycle corrector schematic

The PLL used in this thesis has to output four clock signals at 1GHz frequency. The oscillation frequency range of the VCO needs to fit in with it. The transfer curve simulation result of the VCO is shown in Fig. 3-15.

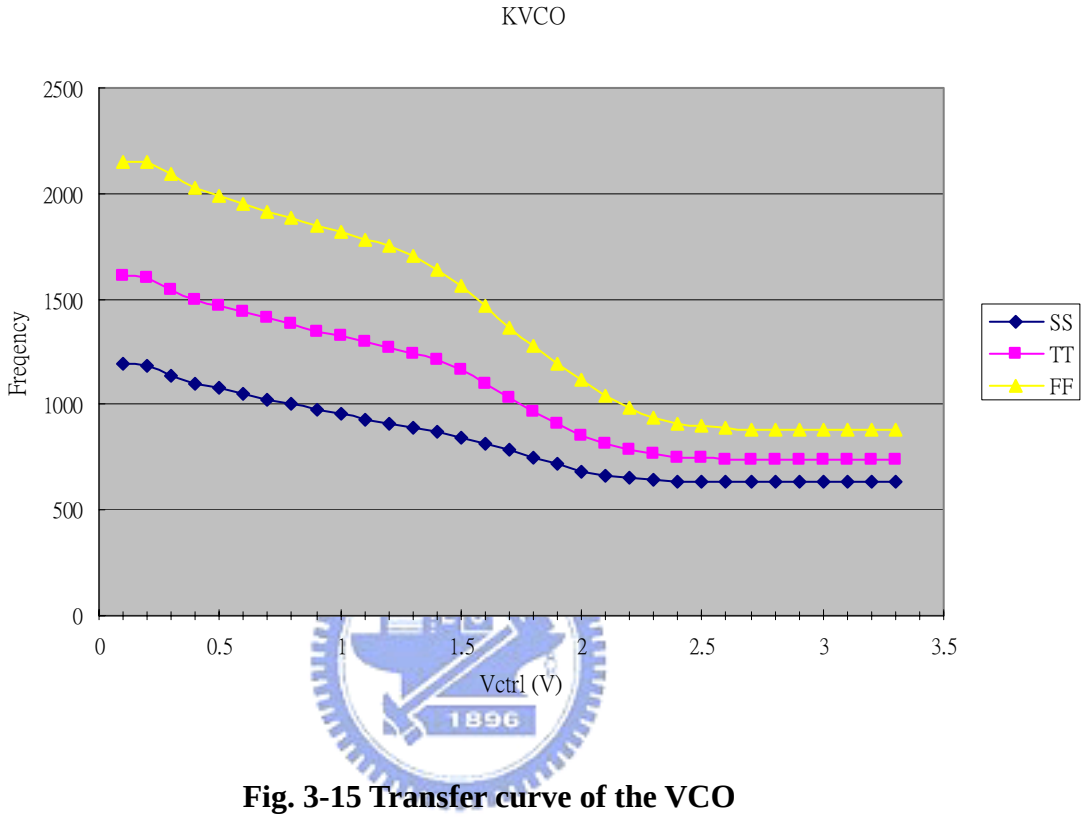


Fig. 3-15 Transfer curve of the VCO

3.3.5 Divider

The frequency of the input reference signal to the PFD is 125MHz but the VCO outputs four clock signals at 1GHz. A frequency divider is therefore needed to process the feedback signal to the PFD with a divided-by-eight circuit. The divided-by-two circuit is implemented as shown in Fig. 3-16 [15]. Then three divided-by-two circuits are cascaded to be a divided-by-eight circuit. The asynchronous counter has a bad property that it will accumulate the jitter stage by stage. As shown in Fig. 3-17, a synchronous counter is used at the last stage to re-sample the feedback signal, and it will eliminate the jitter accumulated at the asynchronous counters.

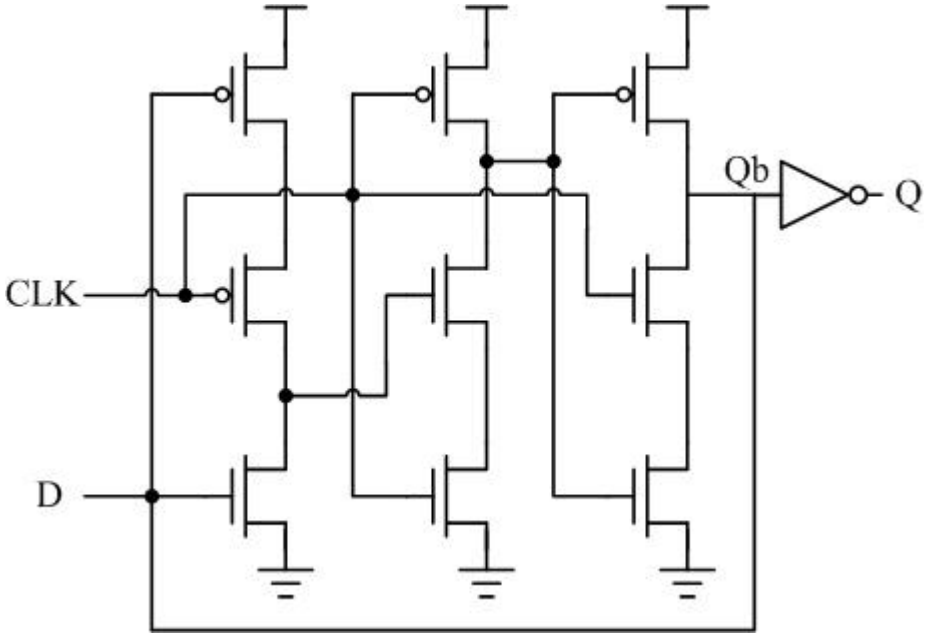


Fig. 3-16 Schematic of TSPC asynchronous divided-by-two circuit

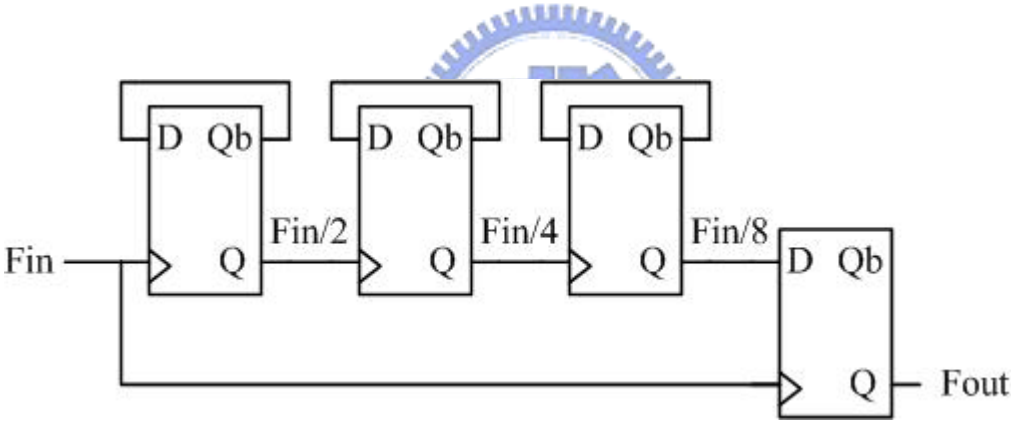


Fig. 3-17 Divided-by-eight circuit with asynchronous and synchronous counters

3.4 PLL Liner Model

Although the PLL is a highly nonlinear system, it has been found that its transient behavior can be reasonably well approximated by a linear model when it is in lock and the phase and frequency changes of input signal are slow and minimal about their operating or bias point. A signal flow graph for the linear small signal model of the PLL is shown in Fig. 3-18.

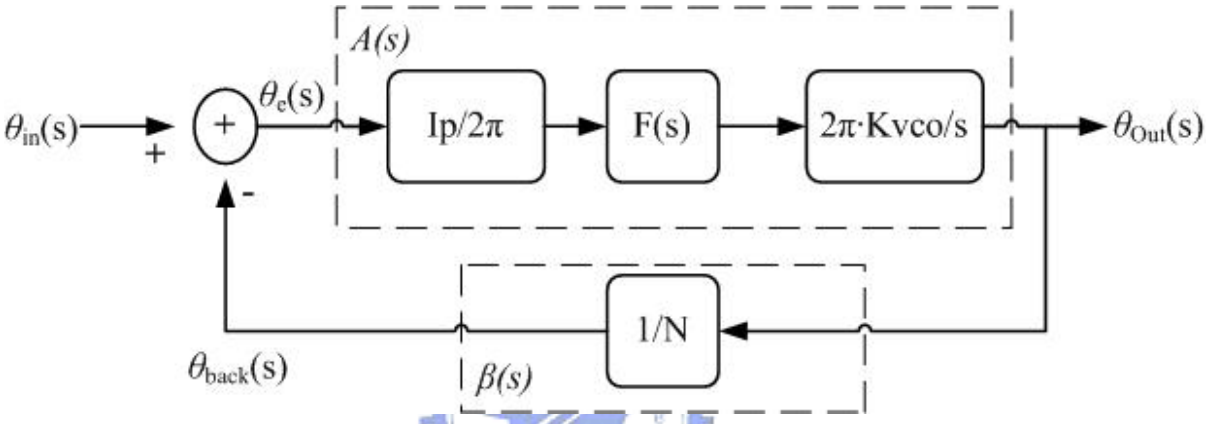


Fig. 3-18 Linear model of the PLL

When the PLL is in lock, the PFD detects the phase difference between the input signal (θ_{in}) and the feedback signal (θ_{back}), defined as $\theta_e=\theta_{in}-\theta_{back}$. The PFD produces UP and DOWN signals with different pulse widths which are proportional to θ_e. The CP is controlled by the UP and DOWN signals to offer a current signal. The average charge flowing into the LF is given by $I_{avg} = \theta_e \frac{I_p}{2\pi}$. The ratio of the current output over the input phase difference is defined as $\frac{I_p}{2\pi}$ (A/rad). As the proposed equation in section 3.3.3, the LF has a transfer function F(s) (V/A). The ratio of the VCO oscillation frequency to the control voltage V_{ctrl} is K_{vco} (Hz/V). Since

$$\omega(t) = \frac{\partial \phi(t)}{\partial t} \quad , \quad \phi(s) = \frac{\omega(s)}{s} \tag{3-6}$$

, the transfer function of the VCO should be transformed to another type which is $2\pi \frac{K_{vco}}{s}$

(rad/sec · V). Eventually, N is the divider ratio and the feedback factor is $\frac{1}{N}$. The output frequency of the VCO will be N times the input reference frequency. Based on the above definitions and the PLL linear model, the loop gain of the PLL can be expressed as

$$A(s)\times\beta(s)=\frac{\theta_{back}(s)}{\theta_e(s)}=\frac{I_p\times F(s)\times K_{vco}}{s}\times\frac{1}{N} \tag{3-7}$$

The closed loop transfer function of the PLL can be found as

$$H(s)=\frac{\theta_{out}(s)}{\theta_{in}(s)}=\frac{A(s)}{1+A(s)\beta(s)}=\frac{I_p\times K_{vco}\times F(s)}{s+\frac{I_p\times K_{vco}\times F(s)}{N}} \tag{3-8}$$

where

$$\omega_{3dB}=\frac{I_p\times K_{vco}\times F(s)}{N} \tag{3-9}$$

From analysis of LF in section 3.3.3, the shunt capacitance C_2 is typically much smaller than C_1. Therefore, the influence of the capacitance C_2 is neglected temporarily to simplify the equivalent system of the PLL. The characteristics of the transient response can be analyzed by a two-pole or second-order linear model of the PLL. With $F(s) = R_1 + (1/sC_1)$, the closed loop transfer function of the PLL above can be expressed as

$$H(s)=N\frac{(\frac{I_pK_{vco}}{NC_1})(1+sR_1C_1)}{s^2+(\frac{I_pK_{vco}}{N})R_1s+\frac{I_pK_{vco}}{NC_1}} \tag{3-10}$$

This can be compared with the classical two-pole system transfer function below

$$H(s)=N\frac{\omega_n{}^2(1+\frac{s}{w_z})}{s^2+2\zeta\omega_ns+\omega_n{}^2} \tag{3-11}$$

Then, the parameters such as natural frequency (ω_n), zero of the LP (ω_z) and the damping factor (ζ) can be derived as

$$\omega_n = \sqrt{\frac{I_p K_{vco}}{N C_1}} \tag{3-12}$$

$$\omega_z = \frac{1}{R_1 C_1} \tag{3-13}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{vco} C_1}{N}} = \frac{\omega_n}{2\omega_z} \tag{3-14}$$

The choice of the damping factor is a trade off between acquisition time and step response stability. If larger ζ is chosen, the system could have longer acquisition time. On the other hand, the system may be ringing for step response or become unstable with a smaller ζ.

3.5 Noise Analysis and Stability

The timing jitter could affect the maximum timing margin of the transmitter and the performance of the high speed serial link. The output jitter of the PLL is contributed by many different noise sources as shown in Fig. 3-19, where $\theta_{in}(s)$ is the reference noise, $i_n(s)$ is the PFD and CP noise, $V_n(s)$ is the LF noise and $\theta_n(s)$ is the VCO noise.

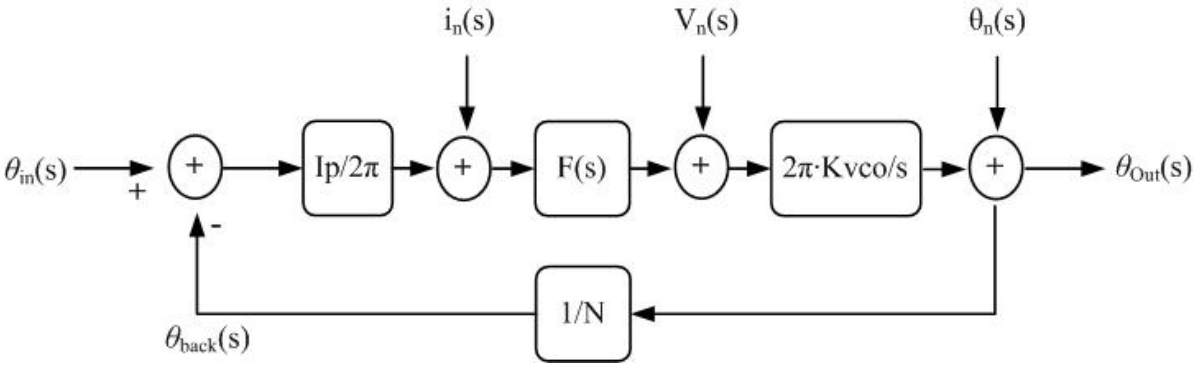


Fig. 3-19 The PLL linear model with different noise sources

Using the closed loop analysis, the transfer functions of different noise sources can be derived as

$$H_{in}(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{N \times K}{s + K} \tag{3-15}$$

$$H_{pfd\_cp}(s) = \frac{\theta_{out}(s)}{i_n(s)} = \frac{2N\pi}{I_p} \times \frac{K}{s+K} \tag{3-16}$$

$$H_{LF}(s) = \frac{\theta_{out}(s)}{V_n(s)} = 2\pi \times \frac{K_{vco}}{s+K} \tag{3-17}$$

$$H_{vco}(s) = \frac{\theta_{out}(s)}{\theta_n(s)} = \frac{s}{s+K} \tag{3-18}$$

where

$$K = \frac{I_p \times K_{vco} \times F(s)}{N} = \frac{I_p K_{vco}}{N} \times \frac{1+sR_1C_1}{sC_1} \text{ (When C2 is neglected)} \tag{3-19}$$

The noise transfer functions have different characteristics. The $H_{in}(s)$ and $H_{pdf\_cp}(s)$ are low pass functions, the $H_{LF}(s)$ is a band pass function and the $H_{vco}(s)$ is a high pass function. Based on the analysis, the loop bandwidth of the PLL should be maximized to meet the high pass function of the VCO to filter the timing jitter caused by the VCO. The maximum nature frequency ω_n of the PLL is restricted to the input reference clock frequency ω_{in}. Using the analysis from the PLL [16], the criteria of the stability limit can be derived as

$$\omega_n^2 < \frac{\omega_{in}^2}{\pi(R_1C_1\omega_{in} + \pi)} \tag{3-20}$$

Usually, ω_n is designed to be less than 1/10 of the PFD update rate ω_{in} to avoid the instability that is to say $\omega_n < 1/10\ \omega_{in}$.

3.6 Loop Parameter Design

The loop bandwidth and the phase margin are used to determine the component values of the LF. By substituting the equation (3-1) into the equation (3-9), the loop bandwidth can be described as

$$BW = \frac{I_p \times K_{vco}}{N} \times \frac{R_1 C_1}{C_1 + C_2} \tag{3-21}$$

From equation (3-15), the phase term will be determined based on the pole and zero of the loop filter such that the phase margin is calculated as

$$PM = \tan^{-1}\frac{BW}{\omega_z} - \tan^{-1}\frac{BW}{\omega_p} \tag{3-22}$$

By setting the derivative of the phase margin equal to zero, the phase margin is the maximum when the loop bandwidth is set to the average of pole and zero.

$$BW = \sqrt{\omega_z \omega_p} \tag{3-23}$$

We can define a new parameter γ as

$$\gamma = \frac{BW}{\omega_z} = \frac{\omega_p}{BW} \tag{3-24}$$

From equation (3-2), the capacitance ration of C1 and C2 can be represented by

$$\frac{C_1}{C_2} = \gamma^2 - 1 \tag{3-25}$$

The loop bandwidth can be written as

$$BW = \frac{I_p \times K_{vco}}{N} \times R_1 \left[1 - \frac{1}{\gamma^2}\right] \tag{3-26}$$

The design flow of a third-order PLL can be derived from equation (3-24), (3-25) and (3-26).Thus,the design flow can be summarized as follows：

(1) Determine the nominal value of N according to the input reference clock frequency and the output clock signals of the PLL.

(2) Determine the K_{vco} by the design of the proposed VCO circuit or referring to the data sheets of the employed commercial VCO.

(3) Depending on the desired noise and transient performance, determine the loop bandwidth (BW). It is usually designed to be less than 1/10 of the reference clock.

(4) If the filter is off-chip, set I_p to be around 100μA to 1mA. If an on-chip filter is used, decrease the value of I_p because of the trade off between the chip area and the selected pump current.

(5) Select the required phase margin (PM) specification. The zero and pole positions are then determined according to equation (3-24).

(6) With BW, I_p, K_{vco}, N and the ration of C_1 to C_2, R_1 can be calculated according to equation (3-26)

(7) Determine the value of C_1 with $\omega_z = \frac{1}{R_1 C_1}$

(8) Calculate the value of C_2 by the ratio of C_1 to C_2.

The parameters used in the PLL are listed in next section.

3.7 Simulation of Transmitter PLL

Table 3-1 shows the parameters used in the PLL of the transmitter. The MATLAB simulations based on equations (3-7) and (3-8) are shown in Fig. 3-20 and Fig. 3-21. Fig. 3-20 shows the loop gain simulation and it can be used to check the phase margin and stability of the PLL. Besides, Fig. 3-21 displays the closed loop gain simulation and the bandwidth of the PLL is presented in it. In the end, the simulations of the PLL by HSPICE code are shown in Fig. 3-22 and Fig. 3-23. Fig. 3-22 shows the PLL closed loop control voltage V_{ctrl} and Fig. 3-23 shows the four clock signals produced by the PLL.

Table 3-1 Parameters of the PLL

Technology			TSMC 0.35μm 2P4M CMOS
Function			**PLL**
Supply Voltage			3.3 V
Input Frequency			125 MHz
Output Frequency			1000 MHz
Charge Pump Current		(Icp)	100 μA
Loop Filter	-	C1	60 pF
	-	R1	8 kΩ
	-	C2	3.5 pF
VCO gain (Kvco)			400 MHz/V
Divider (N)			8
Loop Bandwidth			5 MHz
Phase Margin			56 degrees
Damping Factor			2.1
Natural Frequency			11.5 MHz

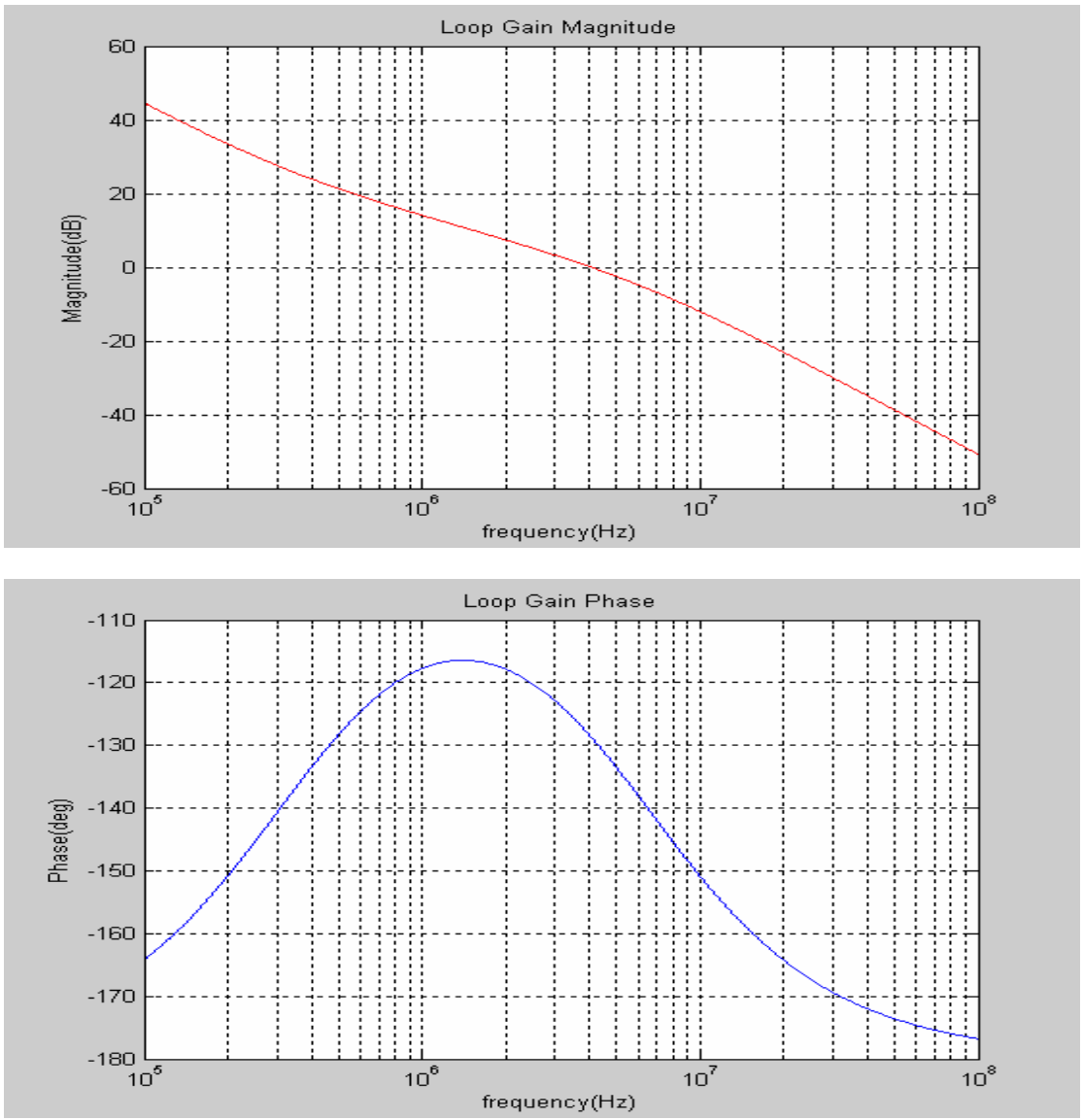


Fig. 3-20 Loop gain simulation of the PLL using parameters in Table 3-1

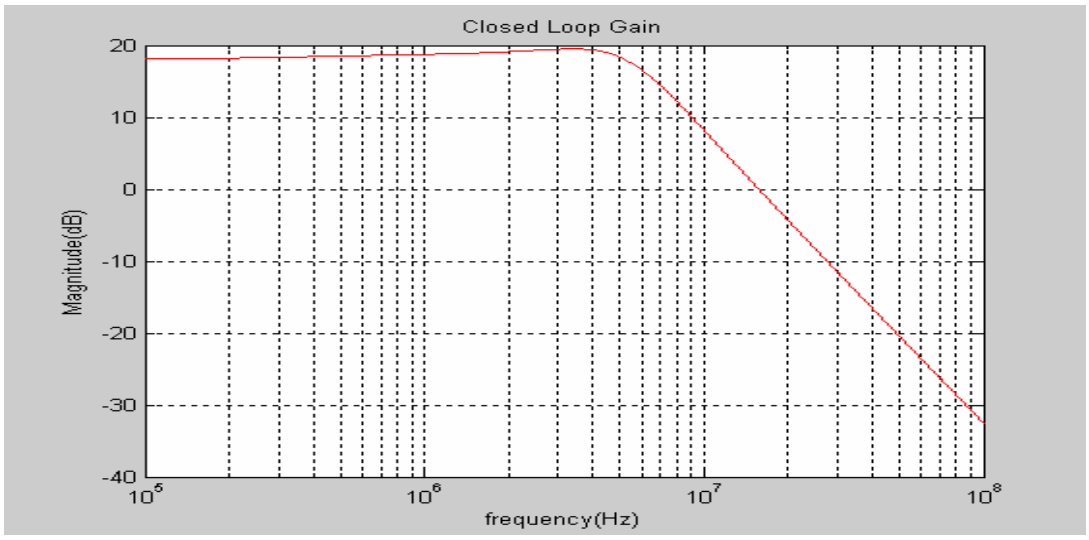


Fig. 3-21 Closed Loop Gain simulation of the PLL

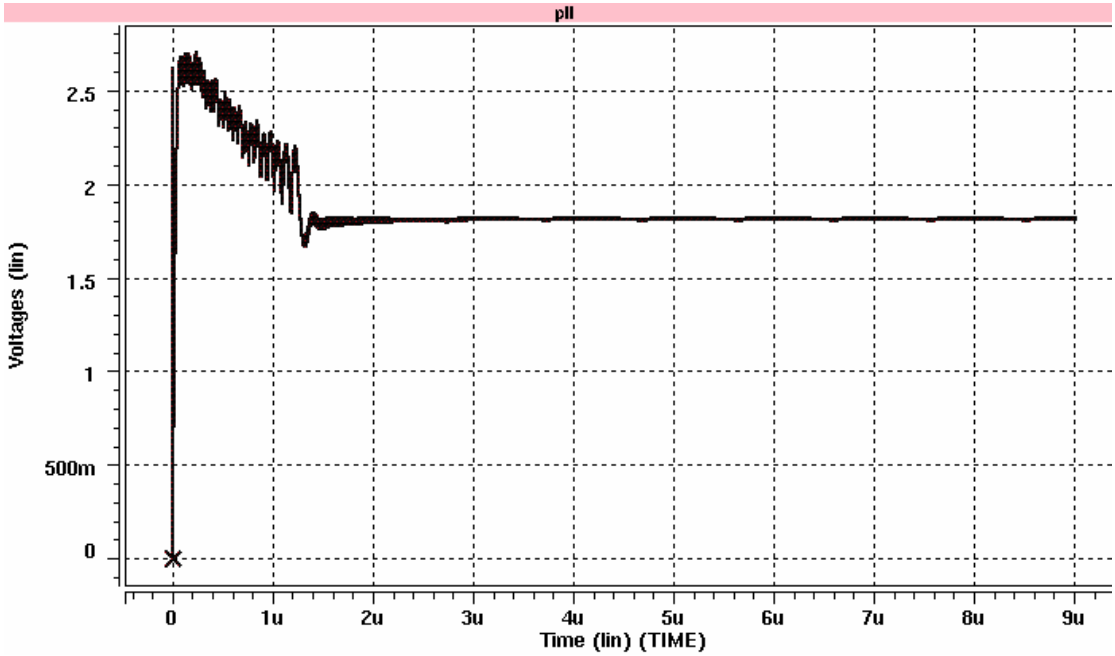


Fig. 3-22 Control-voltage simulation of the VCO

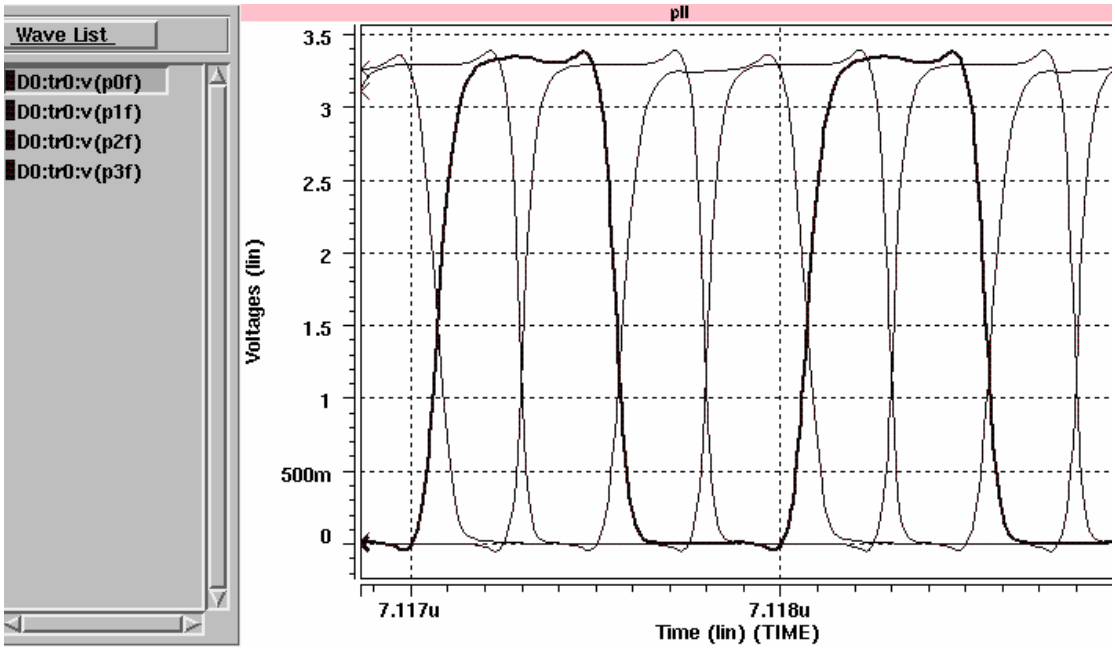


Fig. 3-23 Simulation of the four output clock signals of the PLL

Chapter 4

Transmitter

4.1 Architecture of Transmitter

Fig. 4-1 shows the block diagrams of the transmitter in this thesis. The transmitter consists of a PLL proposed in the chapter 3 to produce the clock signals at 1 GHz frequency. There are two primary signal paths in the architecture of the transmitter. A 2-1 MUX and a CLK driver are used to deliver the clock information (TxC±) in the sampler path. Besides, the other path is compared with a PRBS circuit, a D-flip flop delay circuit, two 2-1 MUXs, a pre-emphasis circuit and a data driver.

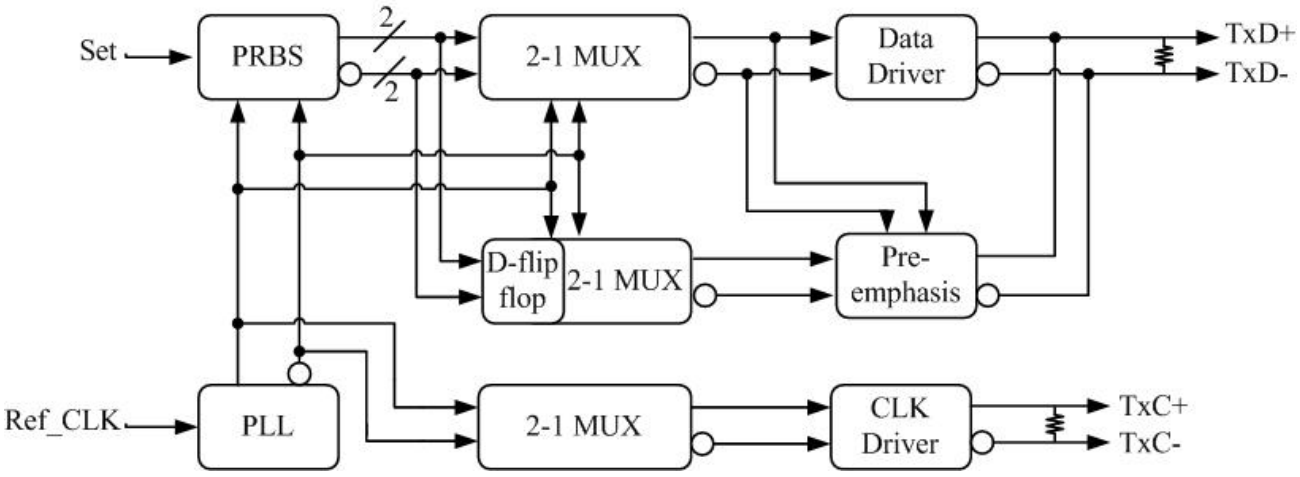


Fig. 4-1 Architecture of the transmitter

In order to test the function of the transmitter, the Pseudo Random Bit Sequence (PRBS) circuit is used to generate the data patterns and produces two parallel data streams at 1Gbps. Then, the 2-1 MUX alternately samples the two parallel data streams according to the clock signals of the PLL to form a serial data at 2Gpbs. Finally, the serial data (TxD±) are transmitted out through the data driver. Furthermore, due to the Inter-Symbol-Interference (ISI) issue which reduces the transmitted data's timing and voltage margins, an additional pre-emphasis circuit is applied to the data driver to have better performance. The detail circuit implementations of the transmitter are described in the following sections and the simulation results are also shown in the last section of this chapter.

4.2 Pseudo Random Bit Sequence

Pseudo random bit sequence (PRBS) generators are widely used for testing communication systems [17]. As shown in Fig.4-2, the proposed PRBS circuit is presented. Fig. 4-3 shows the circuit implementation of the D-flip flop delay cell used in the PRBS circuit. The PRBS circuit is a maximal-length sequence with polynomial $X^{11}+X^{9}+1$ and can actually produce two sequences. One is the trivial one that occurs when the initial state of the generator is all zeros. The other one, the useful one, has a length of 2^{11}-1. Therefore, the SET signal is used to avoid the situation of all zeros.

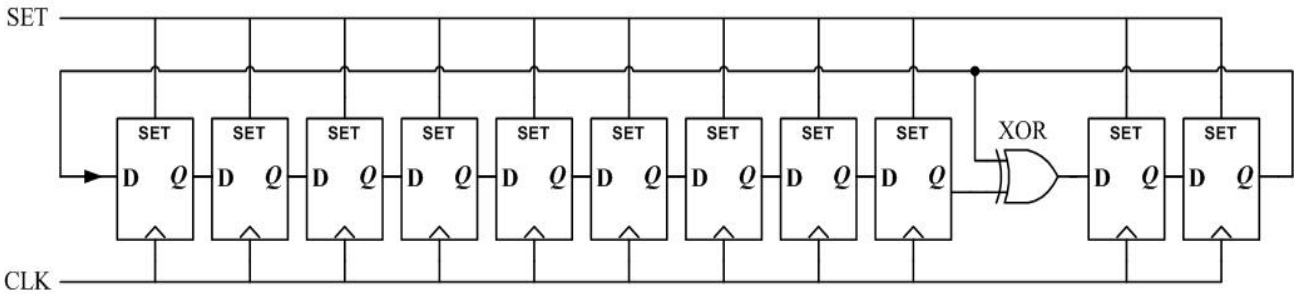


Fig. 4-2 Block diagram of the PRBS circuit

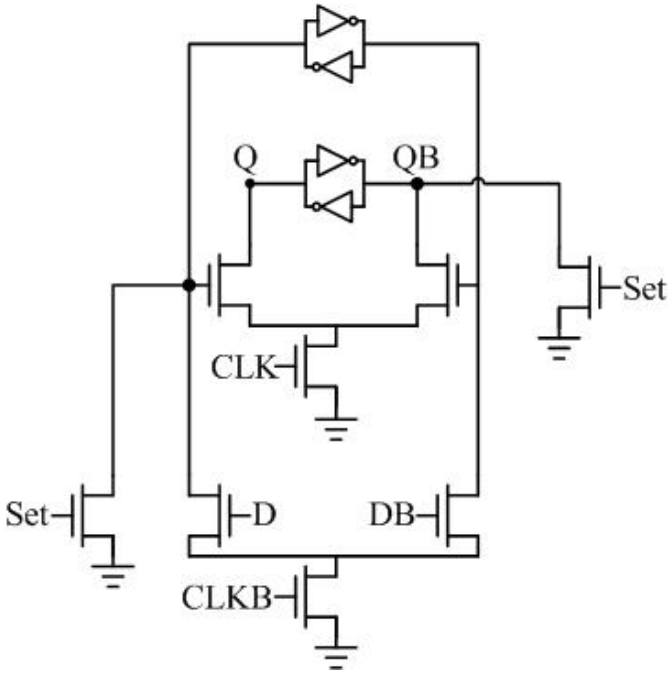


Fig. 4-3 D-flip flop delay cell of the PRBS circuit

4.3 2-1 Multiplexer

The multiplexer is used to transfer the parallel data produced by the PRBS circuit into the serial output data stream. Fig. 4-4 shows the schematic of the 2-1 transmission-gate multiplexer. The multiplexer samples the parallel data (PRBS1 and PRBS2) according to the complementary clock signals from the PLL at 1GHz frequency and the timing diagram is shown in Fig. 4-5. After that, the serial output data stream worked at 2Gpbs is prepared for the following circuit, data driver.

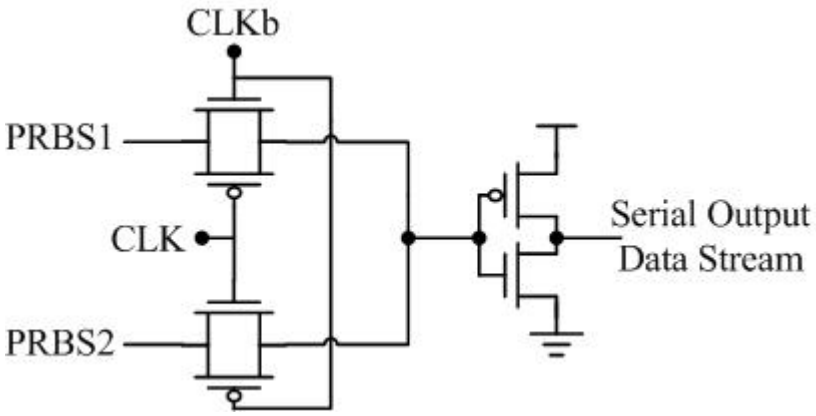


Fig. 4-4 Schematic of the 2-1 transmission-gate multiplexer

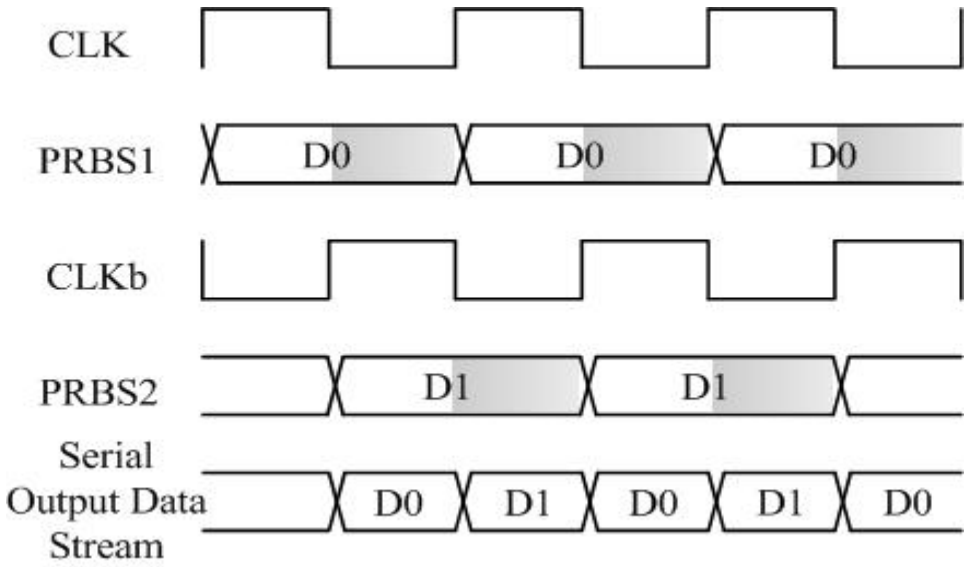


Fig. 4-5 Timing Diagram of the serial output data stream

4.4 Data Driver

The Data Driver is designed with good driving ability and wide bandwidth to transmit data onto outside circuits. As shown in Fig. 4-6, the simplified RSDS transmitter outputs consist of a current source which drives the differential pair line. The implemented circuit uses the typical configurations with four MOS switches in bridge configuration to control the direction of current on the R_{T_T}. With M1 and M2 switched on, the polarity of the output current is positive together with the differential output voltage. On the contrary, the polarity of the output current and voltage is reversed if M1 and M2 are switched off. The differential load resistor R_T provides current-to-voltage conversion. In order to obtain the correct output offset voltage of the RSDS^{TM} Spec., a feedback loop across a replica of the transmitter circuit is used, but in this case the effect of component mismatches between the transmitters and replica should be carefully taken into account.

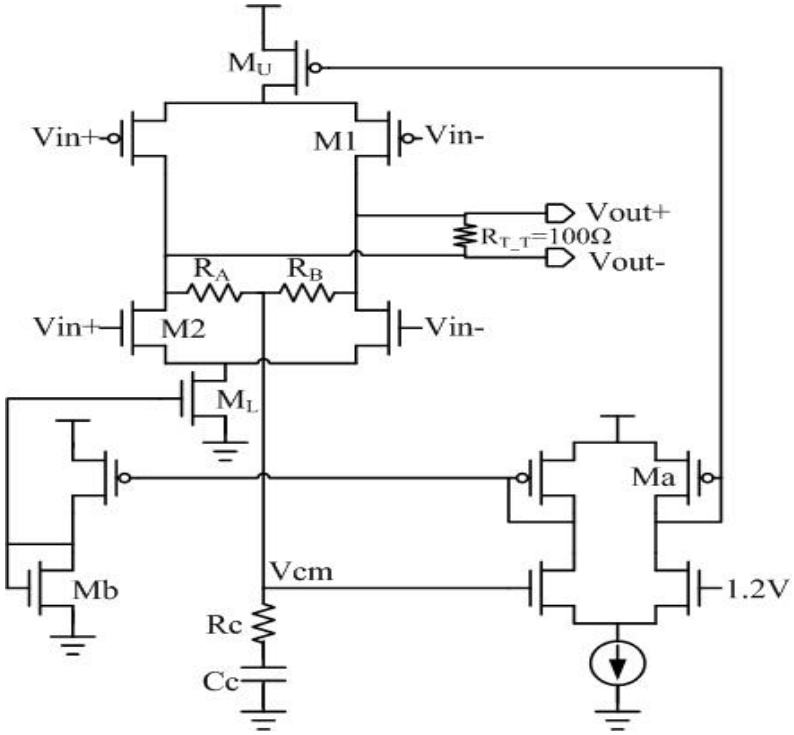


Fig. 4-6 Schematic of the transmitter driver and the closed-loop control circuit

In order to achieve higher precision and lower circuit complexity, a simple low-power common-mode feedback control is implemented such as the bottom part of Fig. 4-6. The common-mode output voltage is sensed by means of a high resistive divider R_A and R_B (R_A=R_B=50kΩ) and compared with a 1.2-V reference by the differential amplifier. The current flowing across M_a and M_b is mirrored to M_U and M_L. Usually, the large gain of device size M_U-M_a and M_L-M_b is used in order to make negligible the power consumption of the common-feedback circuit. To develop the correct voltage swing on the 50Ω load resistance (R_{T_T}//R_{T_R}), the amount of current should be designed properly. Besides, a large stability margin over PVT variations is achieved for the common-mode feedback by means of a pole-zero compensation, R_c and C_c. [5]

4.5 Pre-Emphasis Circuit

The main issue of the data driver is the settling time control and it is also the bandwidth limitation of the driver.

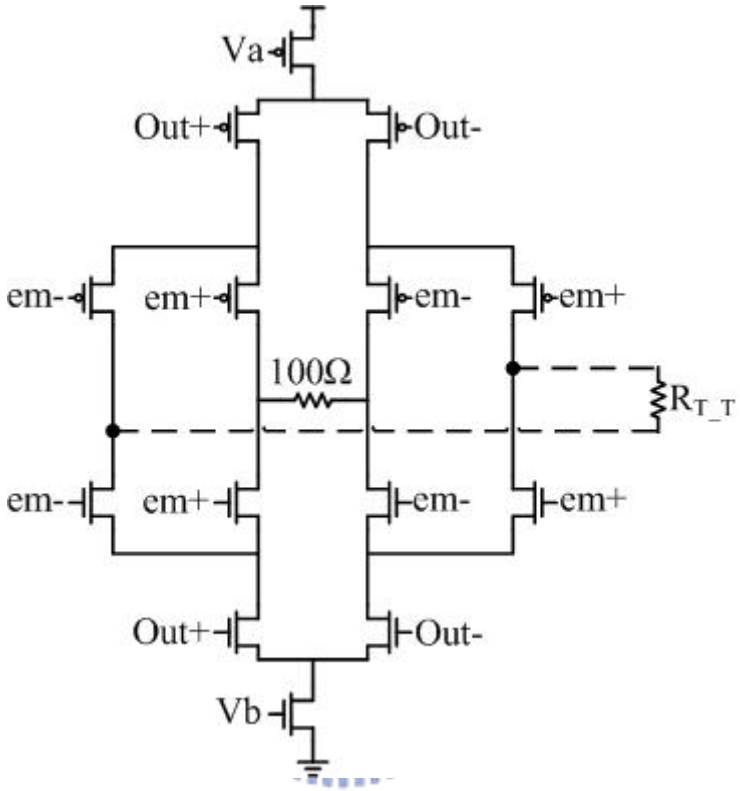


Fig. 4-7 Schematic of the pre-emphasis circuit

When the bit time of the data is smaller than the settling time of the data driver, the value of the previously transmitted signal will affect the current bit's waveform. The interference, called inter-symbol interference (ISI), reduces the maximum frequency at which the system can operate. Therefore, as shown in Fig. 4-7, a pre-emphasis driver is applied directly on the load resistance R_{T_T} to enhance the settling ability of the data driver.

Most of the output current comes from the data driver, controlled by the data multiplexer. The pre-emphasis circuit controls additional output current according to adjacent data. The operation of the pre-emphasis circuit is shown in Table 4-1.

Table 4-1 the operation of the pre-emphasis circuit

Out+	Out-	em+	em-	Pre-emphasis?
High	Low	High	Low	No
High	Low	Low	High	Yes
Low	High	High	Low	Yes
Low	High	Low	High	No

4.6 Transmitter Simulation Result

After transmitted from the transmitter data driver, the data output goes through the internal bonding pad, external bonding wire and the PCB circuit. The thin bonding wire can be inductive and the pad is inductive and capacitive. Finally, the output signal arrives at the receiver termination resistor R_{T_R}. Fig. 4-8 shows the simulation waveforms of the proposed transmitter outputs.

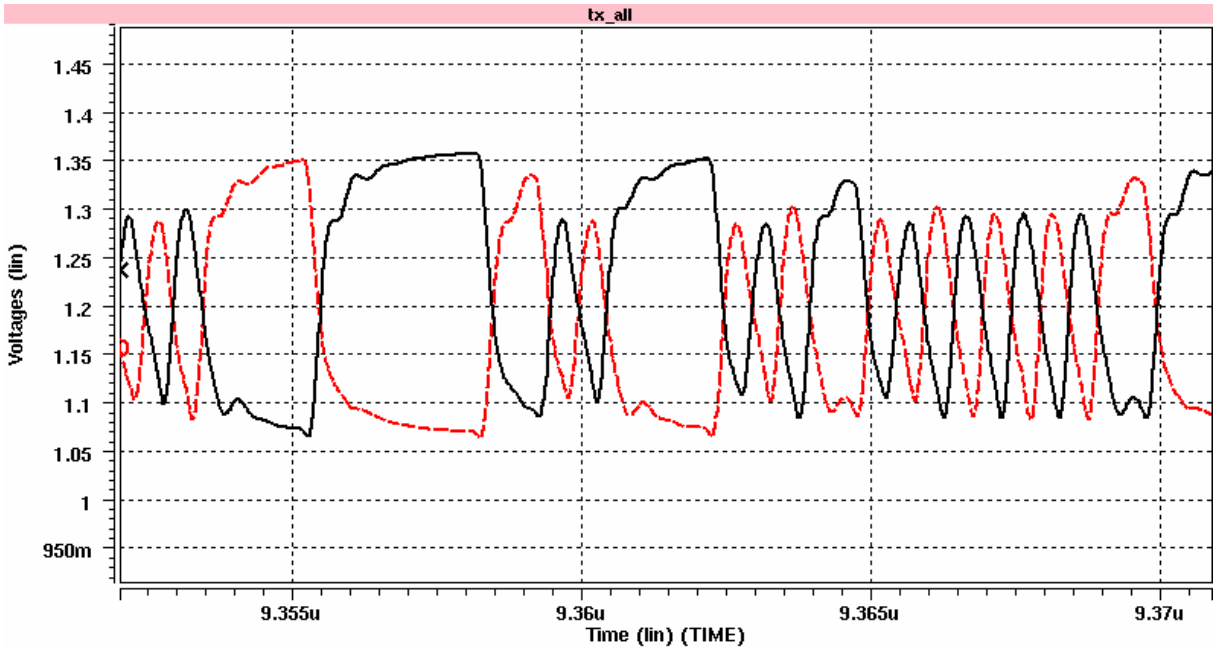


Fig. 4-8 Simulation result of the transmitter output waveform

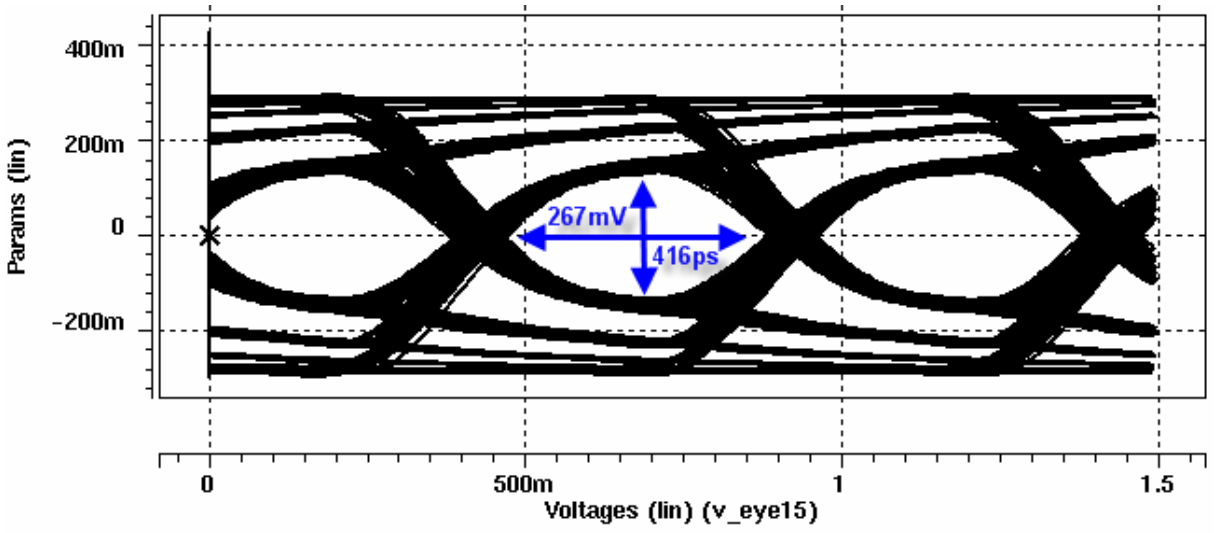


Fig. 4-9 Eye diagram of the signal at transmitting side without pre-emphasis

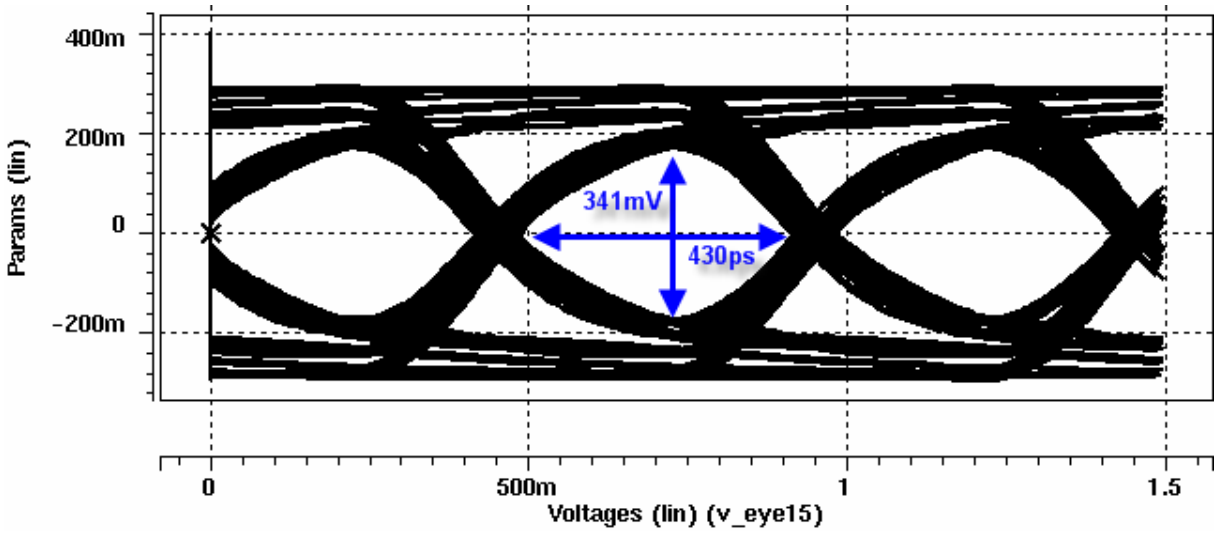


Fig. 4-10 Eye diagram of the signal at transmitting side with pre-emphasis

Chapter 5

Experimental Result

5.1 Experimental Setup

The transmitter chip is implemented in a TSMC 0.35μm 2P4M CMOS process. The chip (including the bonding pad) occupies 1.7 × 1.7 mm^2. Fig. 6-1 shows the chip layout micrograph of the transmitter with the major functional block outlined.

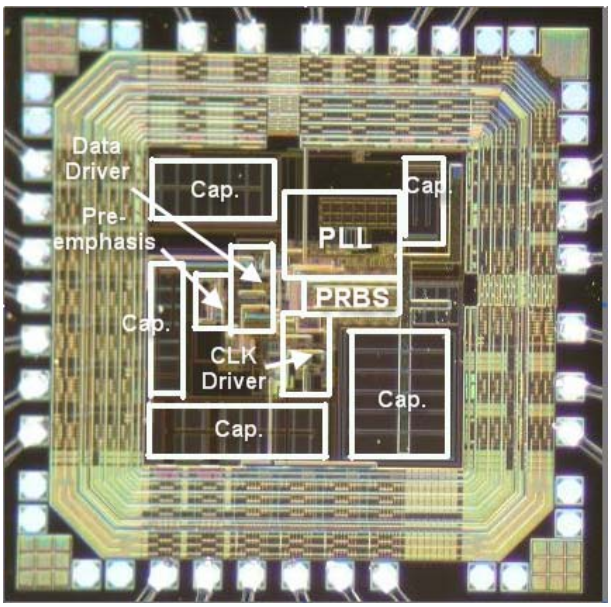


Fig. 5-1 Chip layout micrograph of the transmitter

The block diagrams of the transmitter test environment are shown in Fig. 6-2. The power supply provides the required voltage sources such as analog voltage, digital voltage and output-driver voltage on the test board. The pulse generator provides the reference clock signal (Ref_CLK) to the input of the PLL through a SMA connector. Finally, the differential serial link data outputs (TXD±) and clock outputs (TXC±) are fed to a phosphor oscilloscope.

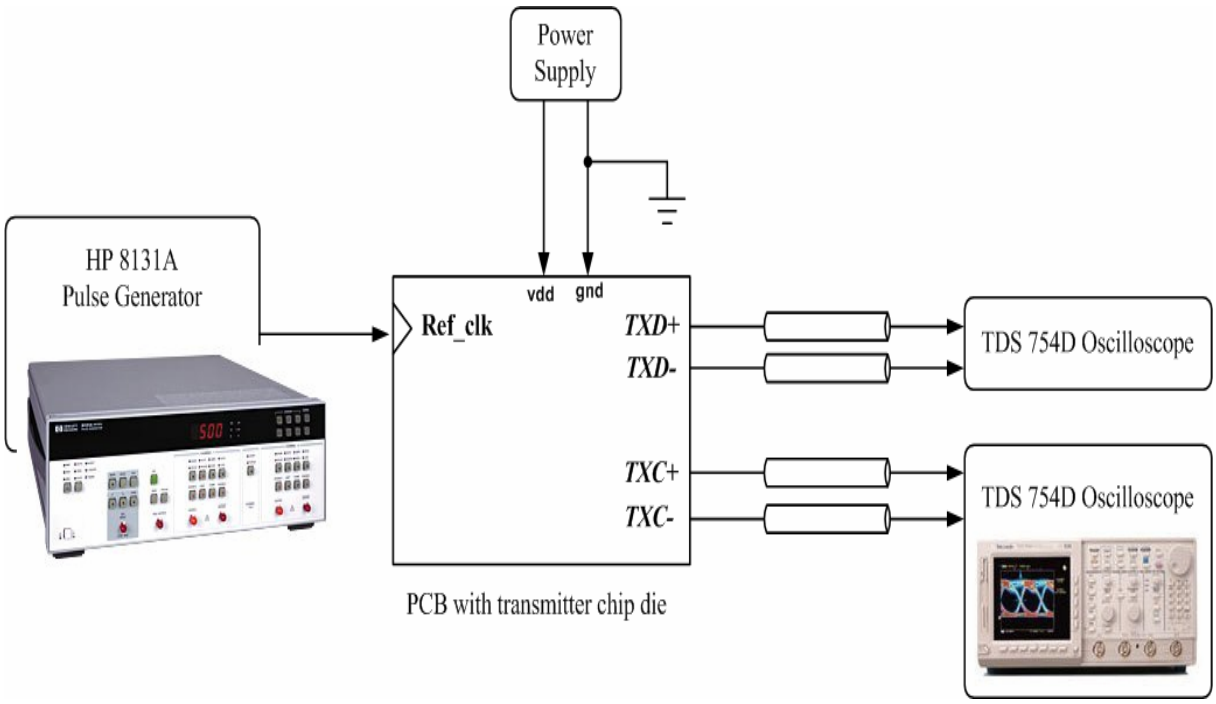


Fig. 5-2 the experimental setup of the transmitter

5.2 Layout and PCB Consideration

The layout of the transmitter chip has been carefully treated to reduce the noise effects. For example, the analog circuits are placed as far as possible from the digital parts. The double guard-rings are used to reduce the substrate noise from the digital parts to the sensitive parts. The power lines are separated from analog, digital and output driver parts.

Besides, the decoupling capacitors are added as much as possible in the free spaces to stabilize the power lines.

Fig. 6-3 shows the print circuit board (PCB) designed to test the transmitter. The power supplies are separated. Several additional capacitors are arranged to provide decoupling of both low-frequency noise with large amplitudes and high-frequency noise with small amplitudes. Furthermore, it is also important to place the discrete components and terminations close to the chip to reduce associated parasitic and signal reflections.

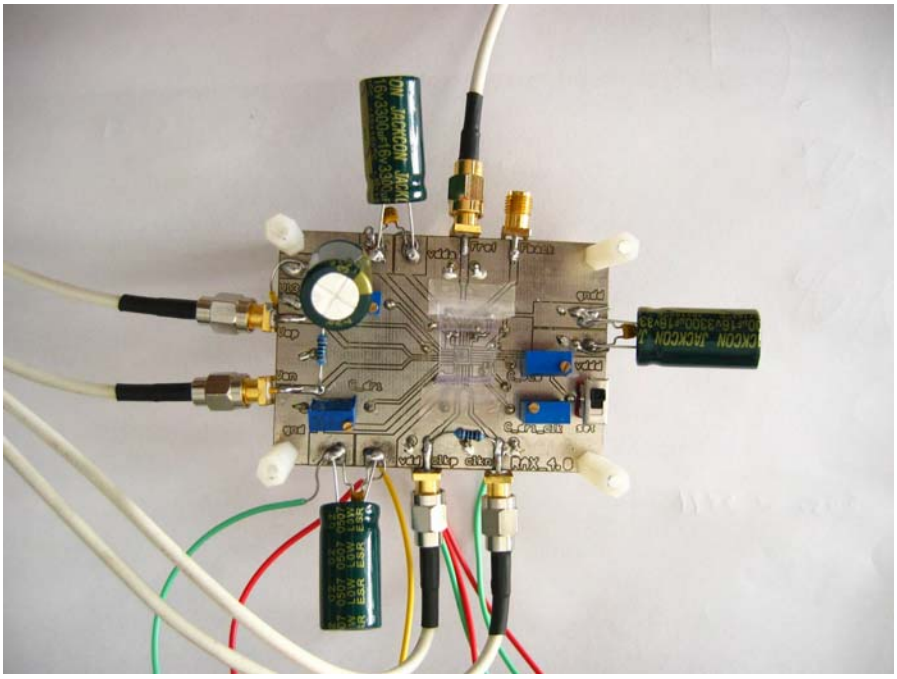


Fig. 5-3 the print circuit board layout

5.3 Transmitter Experimental Result

The transmitter is measured according to said environmental setup. Fig. 5-4 shows the differential output of the transmitter clock driver at VCO's free running frequency 270 MHz. In Fig. 5-5, the eye diagram of the transmitter data driver differential output at 540 Mbps (according to the Fig. 5-4). They indicate that the PRBS and Driver circuit can operate

normally. The random data are produced by the PRBS circuit build in the chip.

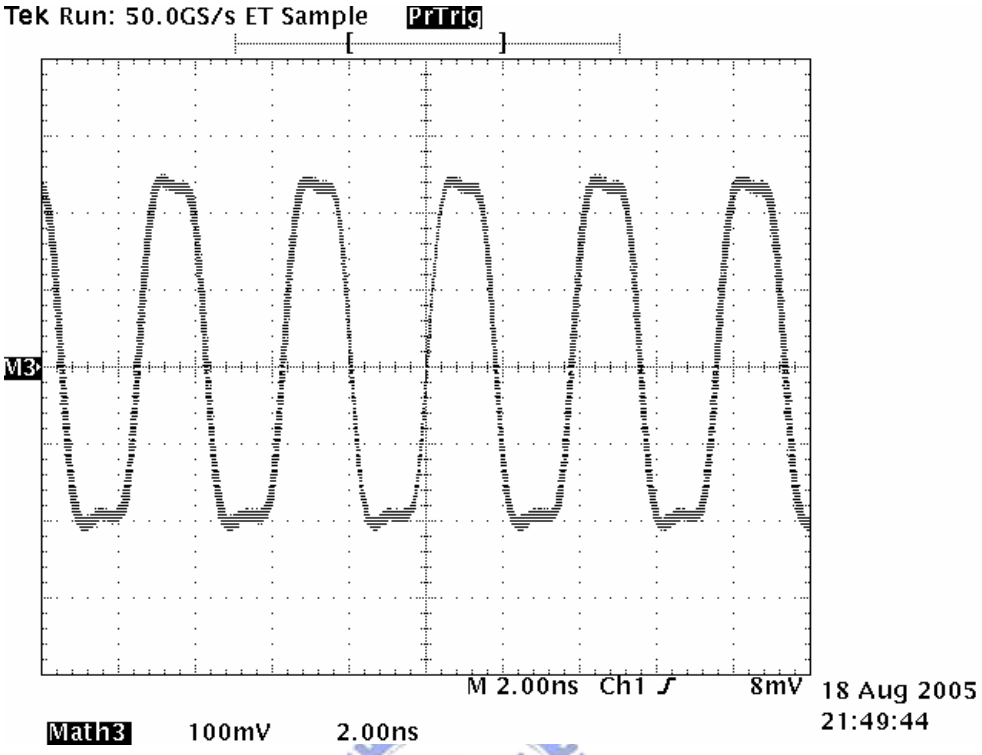


Fig. 5-4 the differential output of the transmitter clock driver

at VCO's free running frequency 270 MHz

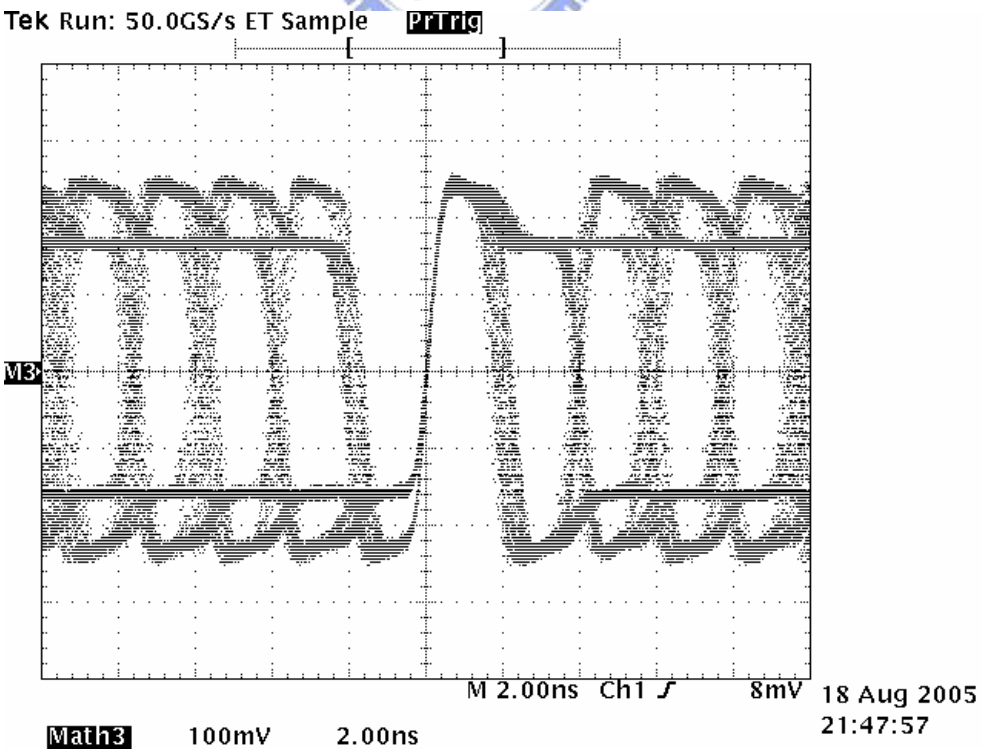


Fig. 5-5 the eye diagram of the transmitter data driver differential output

at 540 Mbps (according to the Fig. 5-4)

In Fig. 5-6, the differential output of the transmitter clock driver at 533 MHz is shown. Meanwhile, Fig. 5-7 shows the eye diagram of the transmitter data driver differential output at 1066 Mbps.

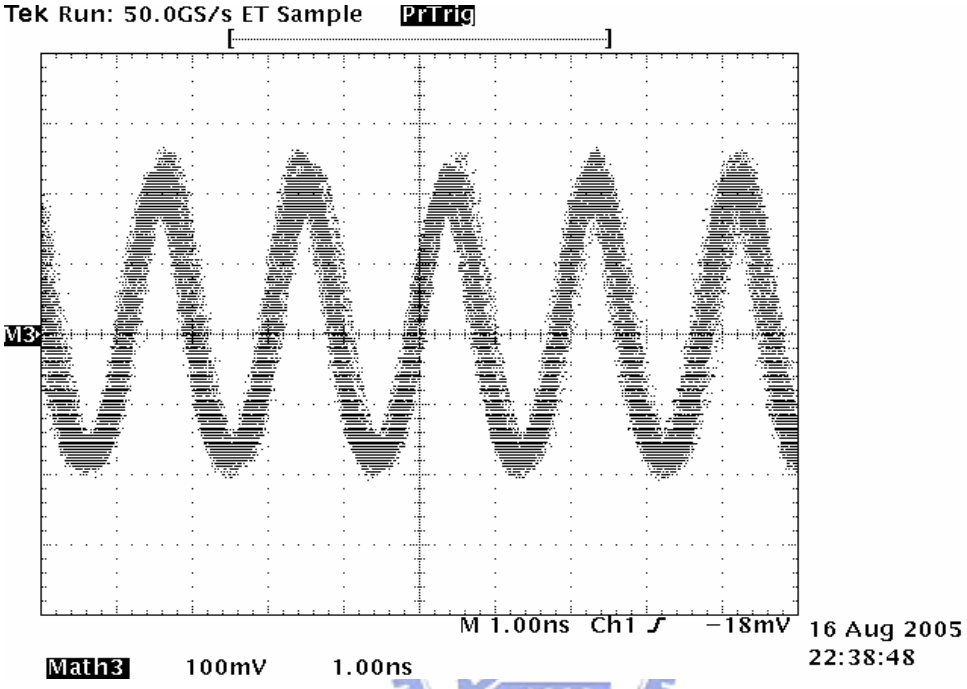


Fig. 5-6 the differential output of the transmitter clock driver at 533 MHz

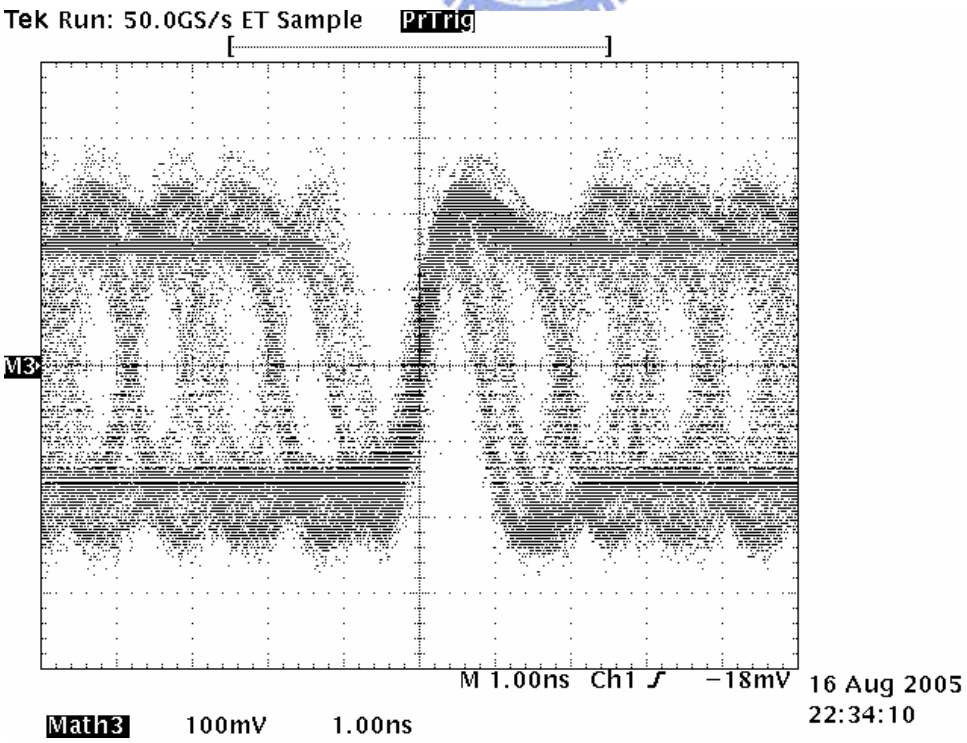


Fig. 5-7 the eye diagram of the transmitter data driver differential output at 1066

Mbps

In Fig. 5-8 and 5-9, the transmitter operates at high frequency. The clock rate is 727 MHz and the data rate is 1454 Mbps.

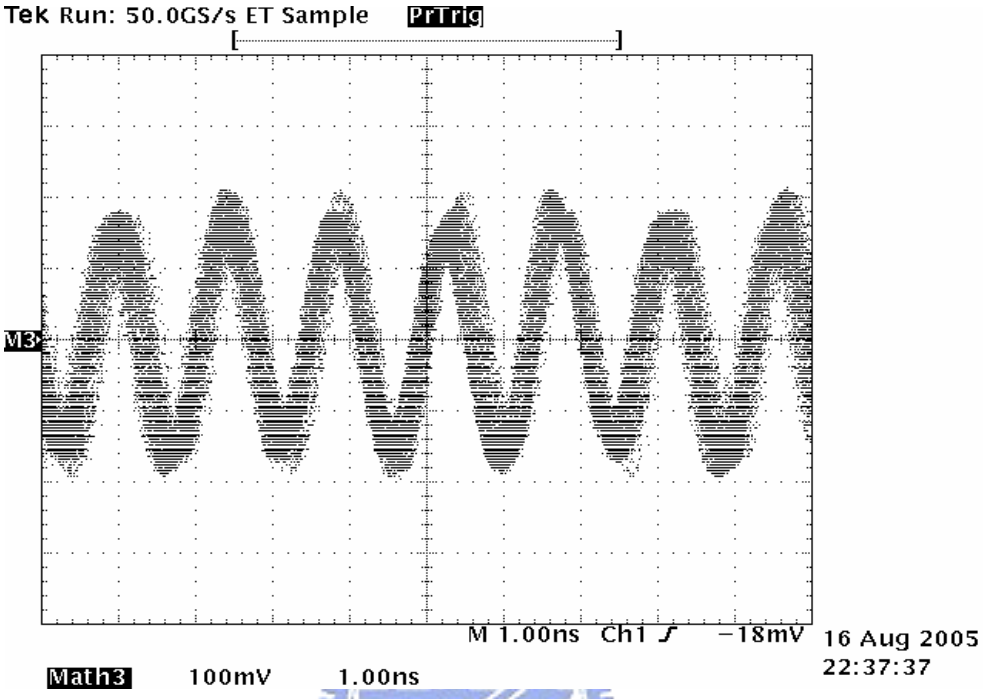


Fig. 5-8 the differential output of the transmitter clock driver at 727 MHz

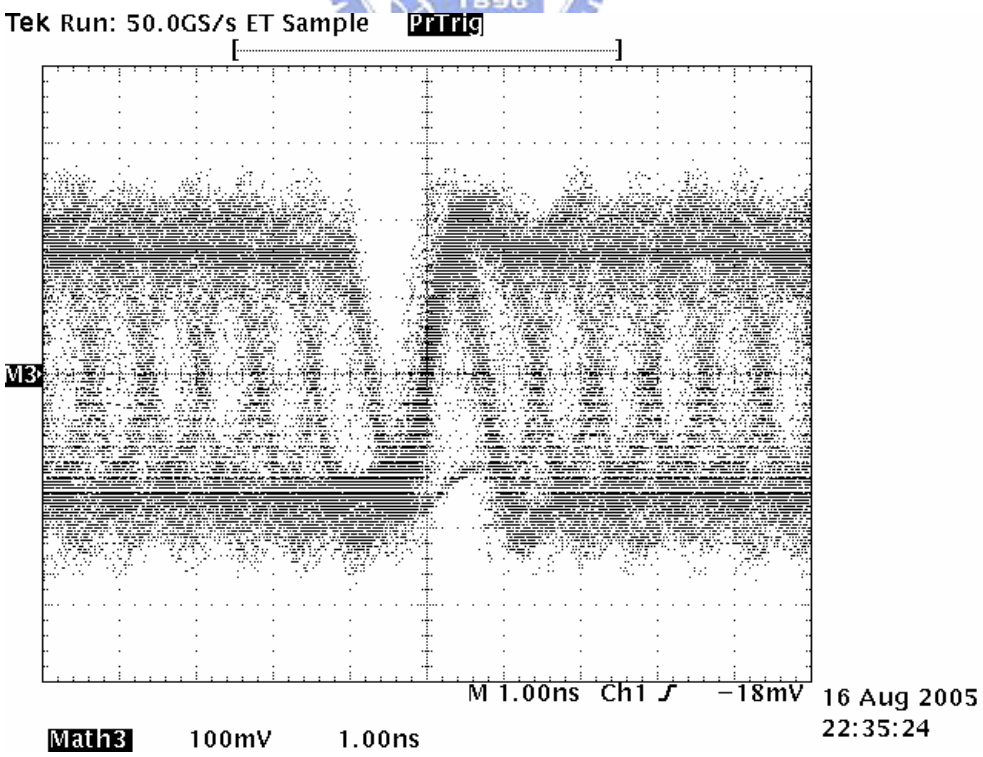


Fig. 5-9 the eye diagram of the transmitter data driver differential output at 1454

Mbps

The locked frequency of the PLL cannot be any higher in the normal design setup. Fig. 5-10 and Fig.5-11 show the experimental results of clock and data when the power supply voltage is turned to 4V.

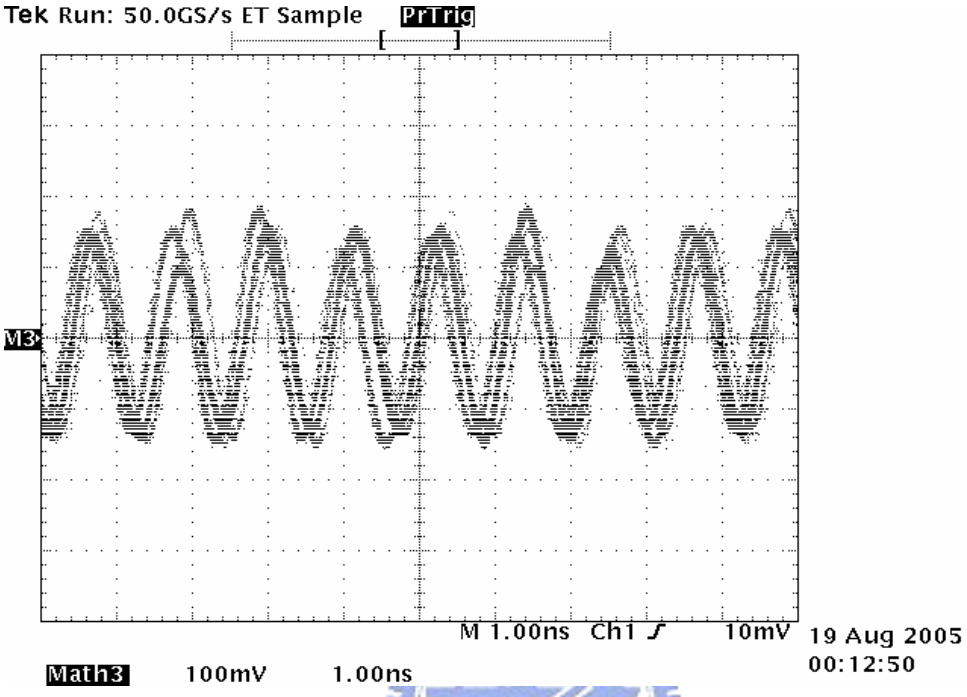


Fig. 5-10 the differential outpus of the transmitter clock driver at 930 MHz when vdd = 4V

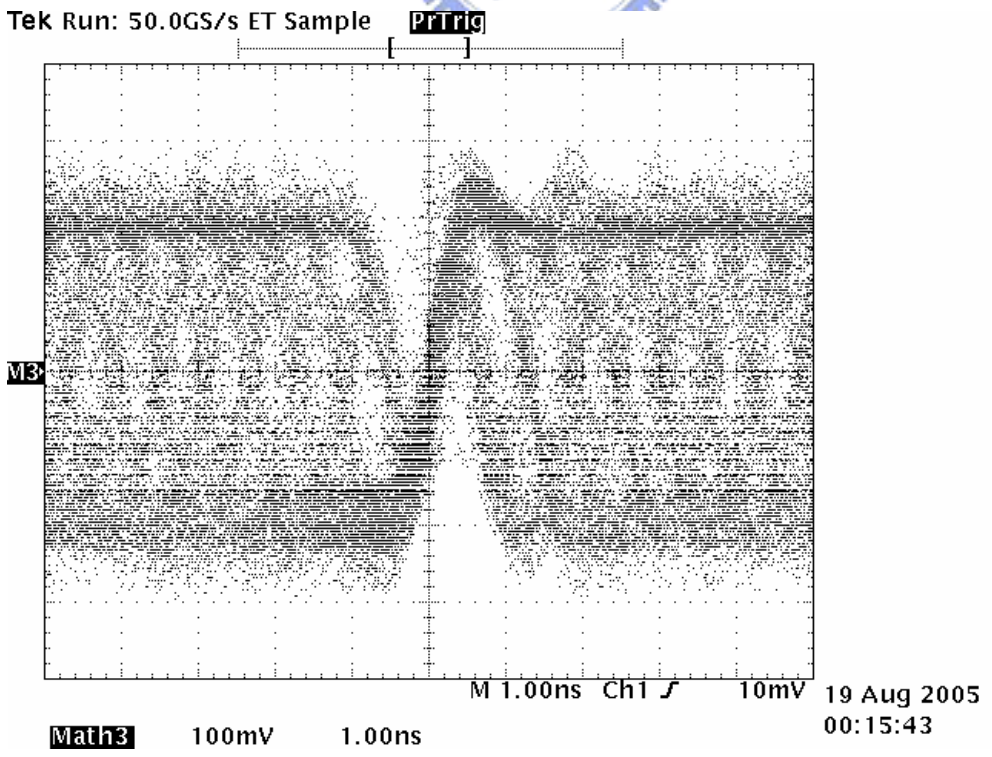


Fig. 5-11 the eye diagram of the transmitter data driver differential output at 1860

Mbps
when vdd = 4V

Chapter 6

Conclusions and Future Work

6.1 Conclusion

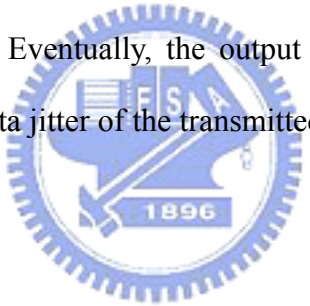
To transmit high speed signals and achieve lower power consumption, a transmitter circuit with the RSDS™ interface has been designed in this thesis. The chip is fabricated in a TSMC 0.35μm 2P4M CMOS process. The research results can be summarized as follows.

The transmitter is composed of a four-phase PLL, PRBS circuits, 2-1 multiplexers, an output clock driver and an output data driver with a pre-emphasis circuit. The input reference frequency of the four-phase PLL is 125MHz; it outputs four uniformly distributed clocks with 1 GHz frequency. The PLL comprises a Phase/Frequency Detector, a Charge Pump, a Loop Filter, a two-stage differential Voltage Control Oscillator and a divided-by-eight divider. The main issue of the PLL is to generate the required clock signals to the transmitter with timing jitter as small as possible. This may be down from system level to circuit level, including parameters design and layout considerations. Thus, the PLL outputs complementary clock signals to the multiplexers to convert parallel data to serial data. Finally, the output data driver drives the serial data onto the bus. Besides, the output clock driver drives the complementary clock signals onto another bus synchronously.

We have devoted to design a transmitter with the data rate at 2Gbps but the operation of the implemented chip can only achieve 1.4Gbps at most. Whole design issues and circuit operations are described in Chapter 3, 4 and the experimental results are shown in Chapter 5.

6.2 Future Work

The increasing demand for data bandwidth in communication systems has driven the development of high speed and low cost serial link technology. For the transmitter, the PLL output jitter must be reduced and the two-stage VCO must be designed carefully. The parasitic capacitors on the output nodes of the VCO and the noise effect by the large K_{VCO} should be also under consideration. Eventually, the output driver should be designed to reduce the increasing of additional data jitter of the transmitted data as far as possible.



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