Low Power Floorplanning/Placement Methodology Considering Performance Constraints and Voltage Islands Generation

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Abstract

Using voltage island methodology to reduce power consumption for System-on-a-Chip (SoC) designs becomes more and more popular recently. At present, this approach is mostly considered in system-level architecture. Since hierarchical design and reuse intellectual property (IP) are widely used, it is necessary to optimize the floorplanning/placement considering voltage island generation to solve critical path delay problems, reduce area and wirelength. Furthermore we can cooperate with the power management unit to attain low power consumption. We propose in this thesis a low power floorplanning/placement methodology considering performance constraints and voltage island generation. Our method is flexible and can be extended to hierarchical design. The experimental results show our method is effective to meet the performance constraints and reduce the power dissipation and the complexity of power routing.