

國立交通大學

電子工程學系

電子研究所碩士班

碩士論文

應用在802.11a和超寬頻系統之射頻CMOS線性功率  
放大器之設計

Design of RF CMOS linear Power Amplifier for 802.11a  
and UWB Applications

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## 摘要

可攜式的無線通訊系統元件的市場快速成長，對建立下一代的低功率射頻積體電路產品有很大的幫助。製程的進步使的CMOS單晶片的實現越來越容易，例如IEEE 802.11a/b/g/n這樣的無線區域網路，和802.15.3a標準無線廣播服務將變的可行。

這篇論文是關於設計射頻區塊中的重要元件—功率放大器的設計。第三章，設計一疊接架構的功率放大器。此功率放大器的最大輸出功率為22dBm，功率增益為26dB，P1dB為-3dBm，在3.3V的電壓供應下總電流消耗為204mA。第四章，設計一個利用電感電阻回授的3~10GHz超寬頻功率放大器。此功率放大器在3~10GHz的範圍內，有13~0dB的功率增益，雜訊指數4~7dB。在3~6GHz的範圍內，P1db為4dBm，PAE低於3%。在1.2V的供應電壓下總功率消耗為74.4mW。

全部的結果都根據ADS的模擬和台積電0.18 $\mu$ m製程。量測結果為國家奈米元件實驗室(NDL)中電路量測系統的量測結果。

# Design of RF CMOS linear Power Amplifier for 802.11a and UWB Applications

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## *Abstract*

The rapid growth of the market for portable wireless communication devices has given great push to the development of a next generation of low power radio frequency integrated circuits (RFIC) product. A single chip CMOS transceiver has been implemented available due to improve of process, some short range wireless systems such as IEEE 802.11a/b/g/n, Wireless Local Area Network (WLAN), and the 802.15.3a standards have made wireless computing and other broadband service possible.

This thesis describes the design of key RF block in the UWB transceiver- the power amplifier. In the Chapter3, a power amplifier by using cascode configuration is designed. The PA allows the maximum output power 22dBm, and has power gain 26dB, P1dB at -3dBm, and total current consumption 204mA at DC supply 3.3V. In the Chapter4, it describes a 3~10GHz power amplifier for UWB application, by use inductor-resistor feedback configuration. In practical measurement, we have power gain 13~0dB, and noise figure 4~7dB from 3~10GHz. The P1dB is 4dBm and PAE is lower than 3% from 3~6GHz. Total power consumption is 74.4mW with  $v_g$  1.2V and  $v_d$  1.2V condition.

All the above mentioned results are from simulation in ADS and using TSMC 0.18 $\mu$ m process. The practical measurement is according to NDL RFIC measurement systems.

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# Contents

Chapter1_INTRODUCTION	-1-
1.1 RF CMOS Transceivers	-1-
1.2 Wireless Transmission Protocols	-3-
1.3 motivation	-6-
Chapter2_ Basic concepts of Power Amplifier	-7-
2.0 Introduction	-7-
2.1 Amplifier parameter definitions	-8-
2.1.1 Weakly nonlinear effects: Power and Volterra series	-8-
2.1.2 Strongly nonlinear effects	-8-
2.1.3 Nonlinear device models for CAD	-9-
2.1.4 Gain match and Power match	-10-
2.1.5 Knee voltage effect	-11-
2.1.6 Load-Pull Measurement	-12-
2.1.7 Input and output VSWR	-13-
2.1.8 Power gain	-14-
2.1.9 Output power and P1dB	-14-
2.1.10 Power added efficiency (PAE), Drain efficiency ( $\eta_d$ ), and Power utilization factor	-14-
2.1.11 Spectral Regrowth	-15-
2.1.12 Adjacent channel power ratio (ACPR)	-16-
2.1.13 Peak-to-Average Ratio (PAR)	-17-
2.1.14 Nonlinearity effect in power amplifier use two-tone analysis	-17-
2.1.15 AM-to-PM Effect	-18-
2.2 Class of power amplifiers	-19-

2.2.1	Class A, AB, B, and C power amplifiers	-20-
2.2.2	Class D, E and F power amplifier	-23-
2.2.3	Power Amplifier Stability Issues	-24-
2.3	Challenges of RF power amplifiers in CMOS technology	-25-
2.3.1	Low breakdown voltage of deep sub-micron technologies	-25-
2.3.2	Substrates coupling effects	-25-
2.3.3	Large signal CMOS RF models	-25-
2.3.4	Low-Q passive element at the output matching network	-26-
2.3.5	Electro-migration and reliability of CMOS devices	-26-
<b>Chapter3_ Simulation of 5.2GHz Power Amplifier for 802.11a</b>		
<b>Application by using cascade</b>		<b>-28-</b>
3.1	overview of 802.11a WLAN standard	-28-
3.2	The PA issues of 802.11a transmitter	-29-
3.3	Simulation of Power Amplifier for 802.11a application	-33-
3.4	Simulation results of 5.2GHz Power Amplifier	-35-
3.5	layout consideration	-40-
3.6	Discussion	-41-
<b>Chapter4_UWB CMOS Power Amplifier</b>		
4.1	Introduction of IEEE802.15.3a and UWB	-42-
4.2	Design of CMOS Power Amplifier for UWB	-47-
4.2.1	The PA issues of UWB transmitter	-47-
4.2.2	Wide Bandwidth Matching with Inductor-Resistor Feedback	-28-
4.2.3	Gain flatness of amplifier with inductor-resistor feedback	-51-
4.2.4	Output matching with inductor-resistor feedback	-54-
4.3	Simulation of Power Amplifier for UWB application	-54-
4.4	Simulation results of UWB power amplifier	-56-

4.5	Layout and measurement consideration	-74-
4.6	Experiment results	-76-
4.7	Remark	-79-
Chapter5_Conclusion		-80-
<b>REFERENCE</b>		<b>-81-</b>



## List of Figures

<b>Figure 2.1:</b> conjugate match and load-line match	-11-
<b>Figure 2.2:</b> knee voltage of deep sub-micron CMOS transistor is larger than typical power transistor	-12-
<b>Figure 2.3:</b> Typical configuration of load-pull	-13-
<b>Figure 2.4:</b> Spectral regrowth due to amplifier nonlinearity	-16-
<b>Figure 2.5:</b> phase-shift distortion with input power increases	-19-
<b>Figure 2.6:</b> classification of Power amplifier	-20-
<b>Figure 2.7:</b> Reduced conduction angle current waveform	-20-
<b>Figure 2.8:</b> Fourier component of power amplifier relate to conduction angle	-22-
<b>Figure 2.9:</b> RF power and efficiency with conduction angle sweep; assume optimum load and harmonic short.	-23-
<b>Figure 3.1:</b> Channel of IEEE802.11a wireless WLAN	-29-
<b>Figure 3.2:</b> Efficiency vs. Back-off in PA for OFDM	-30-
<b>Figure 3.3:</b> Breakdown current of NMOS device	-31-
<b>Figure 3.4:</b> Practical measurement of I-V curve in NMOS	-32-
<b>Figure 3.5:</b> Typical amplifier design flow	-33-
<b>Figure 3.6:</b> Cascode configuration I-V curve and load-line simulation	-36-
<b>Figure 3.7:</b> Simulation of output band-pass filter	-36-
<b>Figure 3.8:</b> schematic of 5.2GHz PA	-37-
<b>Figure 3.9:</b> The stability of 5.2GHz PA	-38-
<b>Figure 3.10:</b> Gain and output power of 5.2GHz PA	-38-
<b>Figure 3.11:</b> IM3 of 5.2GHz PA	-39-
<b>Figure 3.11:</b> Input power vs. PAE in 5.2GHz PA	-39-
<b>Figure 3.13:</b> layout of PA	-41-



<b>Figure 4.1:</b> Example TX architecture for a multi-band OFDM system	-45-
<b>Figure 4.2:</b> The waveforms of DS-CDMA proposal	-46-
<b>Figure 4.3:</b> 13 bands and 4 groups are divided by MB-OFDM	-46-
<b>Figure 4.4:</b> The power level of UWB	-47-
<b>Figure 4.5:</b> Parallel resonance circuits	-48-
<b>Figure 4.6:</b> A CS amplifier with inductor degeneration	-49-
<b>Figure 4.7:</b> A source degeneration amplifier with inductor-resistor feedback	-50-
<b>Figure 4.8:</b> The equivalent circuit of a source degeneration amplifier with inductor-resistor feedback	-51-
<b>Figure 4.9:</b> NMOS with resistor feedback	-51-
<b>Figure 4.10:</b> Gain characteristic of resistor feedback	-53-
<b>Figure 4.11:</b> Gain flatness of cascading two feedback	-53-
<b>Figure 4.12:</b> Schematic and simulation result of I-V curve	-57-
<b>Figure 4.13:</b> Simulation of input impedance of a source degeneration amplifier	-58-
<b>Figure 4.14:</b> Input impedance of inductor-resistor feedback amplifier compare to equivalent	-59-
<b>Figure 4.15:</b> The gain and stability simulations of single stage inductor-resister feedback amplifier	-60-
<b>Figure 4.16:</b> Schematic and simulation result of I-V curve with inductor-resistor feedback.	-61-
<b>Figure 4.17:</b> Schematic of the two stage inductor-resistor feedback amplifier	-62-
<b>Figure 4.18:</b> Simulation of second stage with resistor feedback comparing to inductor-resistor feedback	-63-
<b>Figure 4.19:</b> Simulation of first stage with resistor feedback compare to inductor-resistor feedback	-64-
<b>Figure 4.20:</b> Simulation of inter-stage stability	-65-

<b>Figure 4.21:</b> Stability simulation from 0~20GHz of UWB power amplifier	-66-
<b>Figure 4.22:</b> S parameters simulation of UWB power amplifier	-66-
<b>Figure 4.23:</b> Power gain and PAE simulation of UWB power amplifier	-67-
<b>Figure 4.24:</b> P1dB and IIP3 simulation of UWB power amplifier	-68-
<b>Figure 4.25:</b> RF corner SS at 16.8°C simulation of UWB power amplifier	-69-
<b>Figure 4.26:</b> RF corner-SS at 85°C simulation of UWB power amplifier	-69-
<b>Figure 4.27:</b> RF corner-SS at 125.0°C simulation of UWB power amplifier	-70-
<b>Figure 4.28:</b> RF corner-FF at 16.8°C simulation of UWB power amplifier	-70-
<b>Figure 4.29:</b> RF corner-FF at 85.0°C simulation of UWB power amplifier	-71-
<b>Figure 4.30:</b> RF corner-FF at 125.0°C simulation of UWB power amplifier	-71-
<b>Figure 4.31:</b> RF corner-TT at 16.8°C simulation of UWB power amplifier	-72-
<b>Figure 4.32:</b> RF corner-TT at 85.0°C simulation of UWB power amplifier	-72-
<b>Figure 4.33:</b> RF corner-TT at 125.0°C simulation of UWB amplifier	-73-
<b>Figure 4.34:</b> resistor variation by +50% simulation of UWB power amplifier	-73-
<b>Figure 4.35:</b> resistor variation by -50% simulation of UWB power amplifier	-74-
<b>Figure 4.36:</b> layout of UWB PA	-75-
<b>Figure 4.37:</b> S parameter measurement of UWB PA	-77-
<b>Figure 4.38:</b> power gain and NF measurement of UWB PA	-77-
<b>Figure 4.39:</b> P1dB measurement of UWB PA	-78-

## List of Table

<b>Table 1.1:</b> short-range wireless standards	-5-
<b>Table 3.1:</b> Simulation results of 5.2GHz PA	-40-
<b>Table 4.1:</b> IEEE 802.15.3a Requirements	-43-
<b>Table 4.2:</b> The simulation specification of UWB power amplifier	-74-
<b>Table 4.3:</b> Measurement compare to simulation of UWB power amplifier	-78-

