chapter1

INTRODUCTION

1.1 RF CMOS Transceivers

The rapid growth of the market for portable wireless communication devices has given great push to the development of a next generation of low power radio frequency integrated circuits (RFIC) product. Such as wireless phones, cordless and cellular, global positioning satellite (GPS), pagers, wireless modems, wireless local area network (LAN), and RF ID tags, etc., require more low–cost and high power efficiency solutions to supply the demand for low-price product [1]. These listed devices use many standards.

The majority implementation of the RF integrated circuit used for wireless devices are encounter with various possibilities: CMOS, Bi CMOS, and GaAs MESFET, bipolar (BJT), hetero-junction bipolar transistor (HBT), and PHEMT, etc,. Traditional commercial implementation of RF ICs utilizes a mixture of these technologies [2]. Besides, RF devices always operate at their performance limits, consequently, some nonlinearity and high order effects become tremendous significant need to be taken into account.

We just focus on the CMOS technology, CMOS process reduce the minimum channel length from the present years, so the unity gain cut off frequency (f_t) is increasing. For example, a deep sub-micron prototype CMOS technology has realized devices with f_t exceeding 100 GHz [3] and minimum noise figures less than 0.5-dB at 2 GHz. The more commercially available sub-micron CMOS technologies have display f_t's of 20GHz and minimum noise figures of 1.6-dB at 2Ghz [4]. The VLSI capabilities of CMOS make it proper to very high levels of mixed signal radio integration while increasing the functionality of a single chip radio to cover multiple RF standards [5]. Due to the advancement of circuit design technology, circuit size is small and cost down consideration. With the work at [6] [7] [8], low cost and low power devices of RF front-end system implemented by CMOS technology, the prospect of a single chip CMOS system has received considerable interest. Even the SOC is difficult and hard to implement at this time, but a set of separate chips in the same CMOS technology may bring significant economic benefits [9].

A single chip CMOS transceiver has been implemented available due to improve of process, some short range wireless systems such as IEEE 802.11a/b/g/n, Wireless Local Area Network (WLAN), and the 802.15.3a standards have made wireless computing and other broadband service possible. These systems are proper that short range environment where users are highly mobile such that wired network

installations would cost higher. Traditional receivers like heterodyne architecture, were implemented by combine with individual component built using different technology, such as CMOS for base band, bipolar for the IF partition, and the RF partition used GaAs, bipolar, ceramic SAW filters. As the improvement of CMOS technology, direct-conversion transmitter become popular, CMOS has been used to implement all blocks in system, include RF front-end, the base band processor, the microprocessor, and the flash memory, etc, [10]. Because of the relaxed performance requirements, wireless systems allow for the low output power, for example, 0dBm-4dBm output power at Bluetooth standard.

However, CMOS technology still has several defects in RF environments, one of defect is low breakdown voltage, the big problem is to achieve higher levels of output power at such high frequencies as 2GHz, and up to 10GHz. So that the transmit power amplifier become one of the most challenging circuit to engineers.

1.2 Wireless Transmission Protocols

When we deal with RF power amplifiers, we also need to know how the base band signals be modulated. Different modulation technology relate to different design consideration. There are some second generation (2G) systems, for instance, global system for mobile communication (GSM), North American Digital cellular NADC (IS-54,IS-136) and personal digital cellular systems PHS in Japan. Nevertheless, 2G

systems are limited to voice and low date rate services. Third generation (3G) systems will be comment that provide broadband multimedia and high date rate transmit to each others [11]. For instance, UMTS, CDMA 2000, W-CDMA, and EDGE, they will be an increasing demand for multi-standard terminals. And the coexistence of the 3G with 2G systems would then require multi-mode, multi-band mobile terminals [12]. Ultra wideband (UWB) radio is the modern re-incarnation of a century old type of communication. The first cross-Atlantic wireless transmission by Gulielmo Marconi used spark-plug transmitters that can be thought of as impulse based UWB transmission.

We also deal with short-range wireless communication standards in Table 1.1. These standards used at unlicensed Industrial Scientific, and Medical (ISM) band. And some modulation scheme were used, such as Frequency Hopping Spread Spectrum (FHSS), Direct Sequence Spread Spectrum (DSSS), High Rate DSSS (HR/DSSS), and Orthogonal Frequency Division Multiplexing (OFDM).

On the power amplifier design point of view, different modulation methods have different exhibit on linearity. For instance, CDMA has higher peak to average ratio than GSM, so that require higher linearity power amplifier to limit the spectral re-growth, because of base band filtering utilized in digital systems. And GMSK, FM, GFSK, those do not require high linearity could have power control mechanisms that

necessitate efficiency enhancement techniques at lower power levels, like GSM. The control of output power in digital wireless standards is another feature require of power amplifiers. For instance, in IS-54 and GSM, the PA is turned on and off periodically to save power. And in IS-95, the output power must be variable in steps of 1 dB. In class 1 Bluetooth ratio, the output power must be controlled from 4dBm to 20dBm in steps of 2, 4, 6, or 8dB.

Table 1.1: short-range wireless standards

standard	Frequency range	Multiple access	Modulation	Data rate
IEEE802.11 DSSS	2.4 GHz	DSSS	DBPSK DQPSK	1Mbps 2Mbps
IEEE802.11 FHSS	2.4 GHz	FHSS	2GFSK 4GFSK	1Mbps 2Mbps
IEEE802.11 HR/DSSS	2.4 GHz	DSSS	CCK	5.5Mbps 11Mbps
IEEE802.11a OFDM	5.250 GHz 5.775 GHz	OFDM	BPSK/QPSK 16or64 QAM	6,9,12,18Mbps 24,36,48,54Mbps
Bluetooth	2.4 GHz	HFSS	GFSK	1Mbps
HomeRF2.0 (5 MHz)	2.4 GHz	HFSS	2GFSK 4GFSK	5Mbps 10Mbps

1.3 motivation

The objective of this thesis is to target the design issues encountered in the design and implementation of power amplifiers in standard CMOS technology, for short-range wireless applications. We have implemented, fabricated and tested two different PAs, which can be applied for the two proposals respectively. One is high power PA for 802.11a and can deliver an output power 22dBm to 50Ω load; one is wideband PA for ultra-wideband (UWB). Chapter 2 discusses the basic concepts of power amplifiers. Chapter 3 presents the specification, design, and implementation of a power amplifier targeting for 802.11a. Chapter 4 deals with wideband matching network by using inductor-resistor feedback, presents the 802.15.3a proposals, design, implementation of a power amplifier. Chapter 6 concludes this research effort with some future directions.

Chapter2

Basic concepts of Power Amplifier

2.0 Introduction

A logical starting point of power amplifier would be to recall some of the classical results of linear RF amplifier theory, because many PA designs are simple extensions or modifications of linear design. We can read the detail result of RF linear amplifier in many books, we skip those and assume some concepts of RF linear amplifier is well known.

As we discuss about power amplifier, some basic concepts should be explained. First PA operate at high out power state, CMOS devices could be saturated, therefore nonlinear effect become significant. If output power is 1Watt, and how much power the PA should be dissipated? Ideally, we want all the DC supply power be converted to RF, however it is impossible in practice. Therefore the efficiency is the important performance of PA. And some issue about optimum output power should be study, for instance, load line match and load-pull technology.

This chapter presents the main concepts and challenges of RF power amplifiers.

2.1 Amplifier parameter definitions

2.1.1 Weakly nonlinear effects: Power and Volterra series

Power series is a generalized formulation for nonlinear behavior in many elementary, but it has some limitations. There is no phase component in the linear output term, let alone the nonlinear terms. A much stronger formulation of the power series would be used include phase effects, called the Volterra series. Weak nonlinearities may be, for instance, inter-modulation distortion at levels lower than, say,-30dBc. Unfortunately, PA operating at or beyond the compression point requires different treatment, because the nonlinearities become “strong” and arise through the cutoff and clipping behavior of the transistor, and the Power and Volterra series is not sufficient accurate. The fifth- and seventh-order terms of Power series usually become significant as the 1dB compression point is approached and can dominate at still higher drive levels.

2.1.2 Strongly nonlinear effects

Strongly nonlinear effects refer to the distortion of the signal waveform that is caused by the limiting behavior of the transistor. The drain current exhibits cutoff, or pinch-off, when the channel is completely closed by the gate-source voltage and reaches a maximum, or open-channel condition, in which further increase of gate-source voltage results in little or no further increase in drain current.

2.1.3 Nonlinear device models for CAD

To devise a comprehensive model for a device, it is necessary to characterize both the weak and the strong nonlinear behavior. Unfortunately, each of the nonlinearity traits in a particular device arises from quite different aspects of the device physics. The PA designer is much more sensitive to some of the shortcomings of widely used computer-aided design (CAD) models than designers of many other kinds of RF devices. The central issue in modeling RF power transistors is scaling. The detailed modeling and curve fitting are done on a small periphery sample device and may be quite accurate. The PA designer has to take that small cell and scale up it, even hundreds, to “build” a power transistor. Unfortunately, such scaling is not a simple set of electrical nodal connections, and can not be handled easily enough on a modern circuit simulator. The large periphery device will display a range of secondary phenomena that may have been quite negligible in the small periphery device model cell. The low impedance by multiple parallel connections evokes other-effects to come, that would be neglected in normally, including current spreading at bond-wire contacts, electro-acoustic coupling in the semiconductor crystal, and mutual coupling between bond-wire.

Even a basic I-V measurement can pose serious difficulties for an RF power transistor. Mary I-V curve tracers work at speeds several slower than the RF signal for

which the model is require and can be slow enough that transient junction heating effects, which will not occur to any significant extent during an RF cycle, intrude into the measurement. Accurate I-V curve are difficult to obtain for RF power transistors; that has led many to develop custom-built teat rigs, usually incorporating a pulsed measurement scheme [13]. An alternative approach is to build a curve tracer that sweeps through the I-V characteristics at rates in RF range [14].

Reference [11], [12], [15-17] provides starter bibliography, but the research continues.

2.1.4 Gain match and Power match

We can get the maximum gain when input and output of circuits was conjugate match. It is well known by circuit theorem that we can deliver maximum power into load component when load impedance is equal to real part of the generator impedance, and the reactive part should be resonated out. This is the concept of conjugate match or gain match. However, the practical devices have physical limited such as Vmax and Imax, the maximum supply voltage and the maximum generated current. Vmax could be maximum DC supply voltage or breakdown voltage of devices; and Imax could be saturation current of devices. By referring Figure 2.1, this seen the gain match cannot used the full capacity of transistor. If we want to utilize the maximum current and voltage swing of the transistor, a lower value of load resistance would need to be

selected; the value is commonly referred to as the load-line match, Ropt, and in its simplest form simply would be the ratio

$$Ropt = Vmax / Imax, \qquad (2.1)$$

Where we assume the generator's resistance is high and is not taken into account. This Ropt is so called the load-line match or power match. The power match represents a real compromise that is necessary to extract the maximum power from RF transistors and at the same time keep the RF voltage swing within specified limits and the available dc supply.

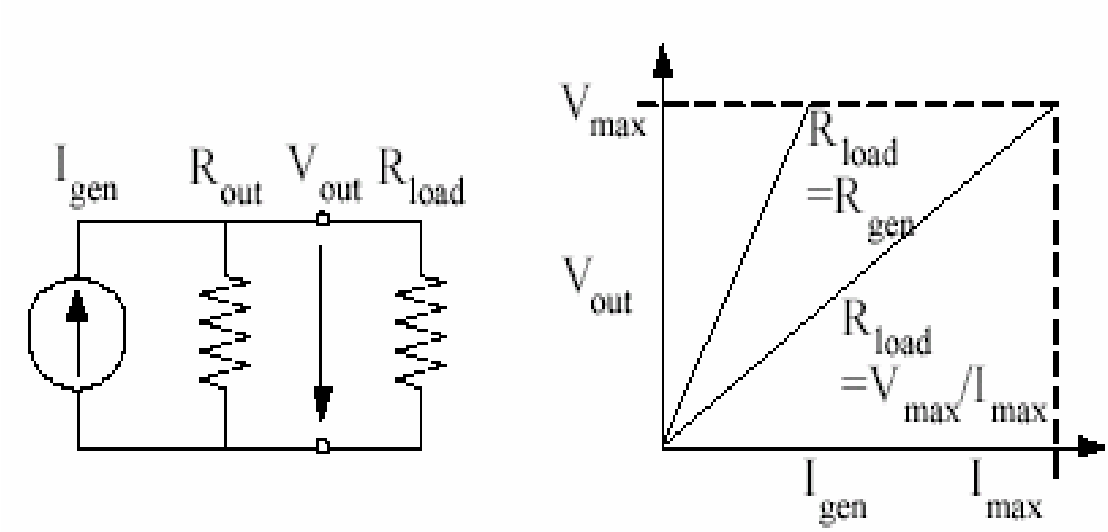


***Figure2.1*:** conjugate match and load-line match

2.1.5 Knee voltage effect

The knee voltage (pinch-off voltage) divides the saturation and the linear region of the transistor and can be defined as, for example, Vds at the 95% of Imax point. As shown in Figure 2.2[18]. And the optimum load resistance become

Ropt = (Vmax-Vknee) / Imax, (2.2)

For sub-micron CMOS transistors, Vknee is only about 10% to 15% of the supply voltage for typical power transistors, while it can be as high as 50% of the supply for deep sub-micron technologies as shown in Figure 2.2. A large portion of the RF cycle could be in linear region. Accordingly, both saturation and linear region must be considered when determining the optimum of operation [18] or relying on balance simulations of circuits.

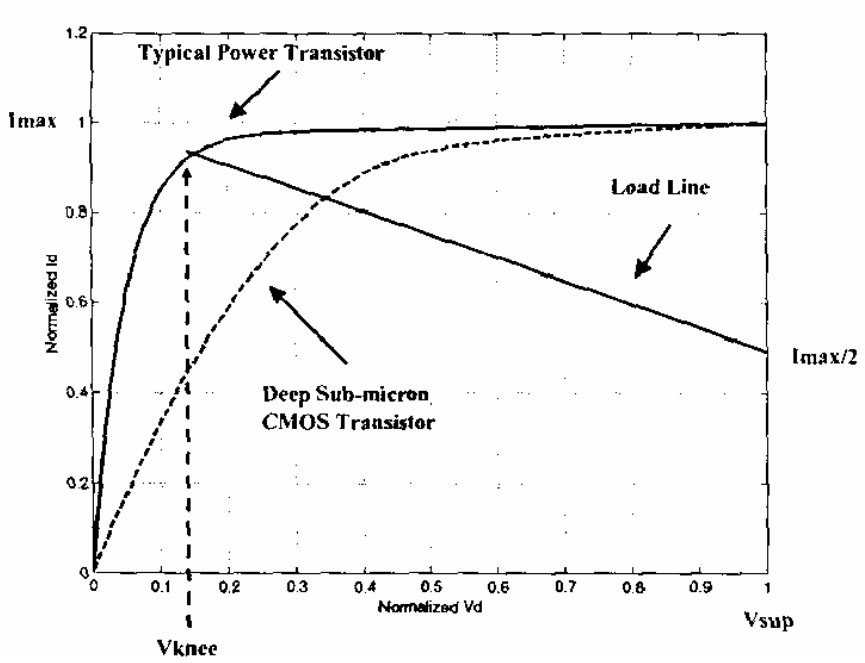


Figure2.2: knee voltage of deep sub-micron CMOS transistor is larger than typical power transistor

2.1.6 Load-Pull Measurement

A load-pull test setup consists of the device under test with some form of calibrated tuning device on its output. The input probably also will be tunable, but this is mainly

to boots the power gain of the device, and the input match typically be fixed close to a good match at each frequency. A typical block diagram is shown in Figure 2.3.

Load-pull measurement can find the practical Ropt of PA, and also the maximum output power.

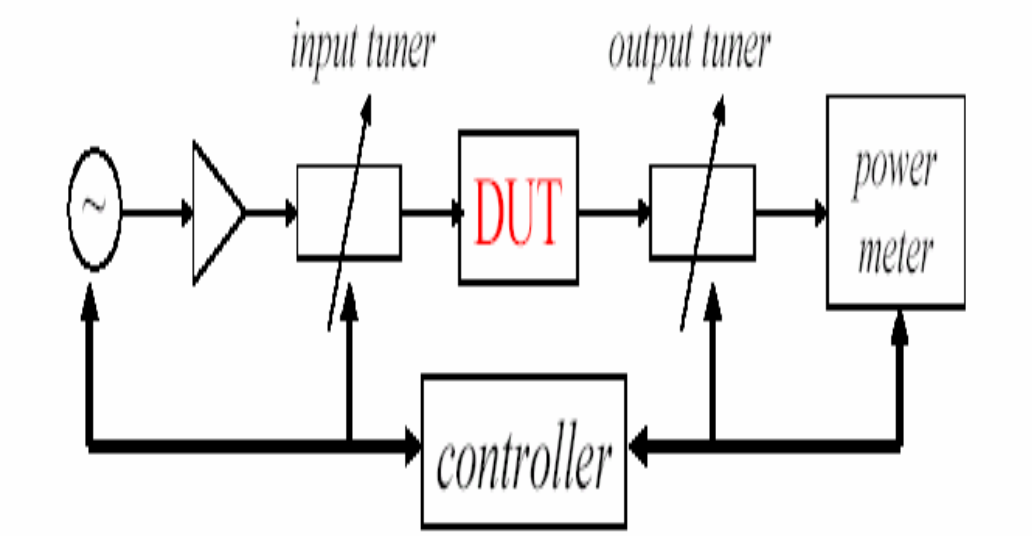


Figure 2.3: Typical configuration of load-pull

2.1.7 Input and output VSWR

VSWR are measured at small-signal conditions as well as at large-signal conditions. There come some problems with power match, It will cause reflections and VSWR at output, the reflected power is entirely a function of the degree of match between the antenna and the 50-Ohm system. The PA does not present a mismatched reverse termination, which could be a problem in some situation. A questionable concept of large signal impedance, once a device starts to operate in a significantly nonlinear fashion, the apparent value of the impedance will change, but the whole concept of

impedance starts to break down as well, because the waveforms no longer are sinusoidal.

2.1.8 Power gain

The power amplifiers are characterized by transducer power gain defined as the ratio of the power delivered to the load (Po) to the power available from the source (Pin) to the amplifier, i.e.,

G=Po/Pin, (2.3)

2.1.9 Output power and P1dB

Power delivered to the load (Po) is known as the output power, which is a strong function of the input power. The output power when the gain is compressed by 1 dB is defined as P1dB, which is normally used as a figure of merit to characterize nonlinearity in amplifiers.

2.1.10 Power added efficiency (PAE), Drain efficiency (ηd),and Power utilization factor

The PAE is defined as

$$PAE = \frac{output\_signal\_power - input\_signal\_power}{dc\_power} = \frac{Po - Pin}{Pdc}$$

$$PAE = \frac{Po}{Pdc}(1 - \frac{1}{G}) = \eta d(1 - \frac{1}{G}). \quad , \qquad (2.4)$$

where ηd is known as the drain efficiency. For high-efficiency amplifiers, single-stage gain is required to be on the order of 10 dB or higher. If the RF power gain is less than

10 dB, the drive power requirement will start to take a serious bite out of output efficiency of a PA stage, and the higher the efficiency, the more serious the effect. Sometimes, it is just as well to keep gain and output efficiency as separate stage, it is noted that at system level or even multistage PA level they will behave interactively on the overall efficiency.

One of the most importance concepts in comparing different PA configurations is the power utilization factor (PUF). PUF is the ratio of the power it would deliver as a simple class A amplifier.

$$PUF = \frac{P\_rf}{Plin}, \tag{2.5}$$

$$Plin = \frac{Vdc * Ipk}{4}, \tag{2.6}$$

where P*lin* is known as the output power of class A having the same dc supply voltage and peak RF current.

2.1.11 Spectral Regrowth

In a digitally modulated waveform, for example, QPSK, need a low-pass filter precede the modulator to limit the bandwidth of the signal, there by suppressing spectral leakage into adjacency channels. We expect limiting the bandwidth tends to smooth out the abrupt transitions in the time domain. And after filtering, exhibiting variation in its envelope as the filter bandwidth decreases. If the power amplifier is to maintain the spectrum to the limited bandwidth, then it must also amplify the

envelope variations linearly. However, if the PA exhibits significant nonlinearity, then shape signals, it is not preserved and the spectrum is not limited to the desired bandwidth. This effect is called "spectral regrowth" [19], [20] and can be quantified by the relative adjacent channel power [20]. Generally, nonlinear PA has better efficiency than linear PA. Therefore, digital modulation schemes exhibit a trade-off between spectral efficiency and power efficiency.

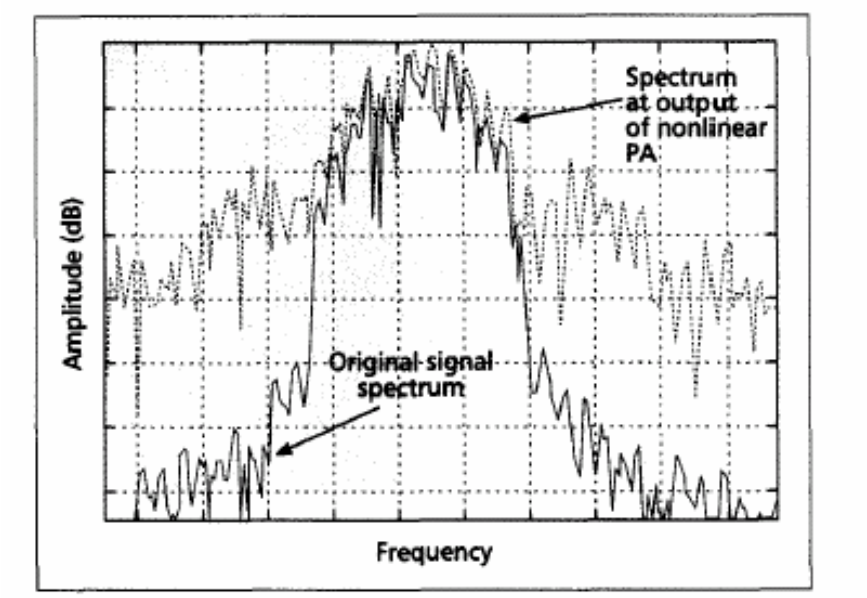


Figure2.4: Spectral regrowth due to amplifier nonlinearity

2.1.12 Adjacent channel power ratio (ACPR) [21]

ACPR is a commonly used figure of merit to evaluate the inter-modulation performance of RF power amplifiers designed for CDMA wireless communication systems, ACPR is a measure of spectral regrowth, appears in the signal sidebands, and is analogous to IM3/IM5 for an analog RF amplifier.

$$ACPR = \frac{power\_spectral\_density\_in\_the\_main\_channel\_1}{power\_spectral\_density\_in\_the\_offset\_channel\_2or3}, \qquad (2.7)$$

There offset frequencies and measurement bandwidths vary with system application.

2.1.13 Peak-to-Average Ratio (PAR) [22]

All single or multi-carrier (modulated or un-modulated) have a peak-to-average ratio. The ratio between the peak power (Pp) and the average power (Pa) of a signal is called the peak-to-average ratio, i.e.,

$$\chi = \frac{Pp}{Pa}, 10\log\frac{Pp}{Pa}(dB) \quad . \tag{2.8}$$

The peak-to-average ratio ΔPs of an input signal consisting of N carriers, each having a average power Pí is defined as

$$\Delta Ps = \frac{(\sum_{i=1}^{n}\sqrt{P_i\chi_i})^2}{\sum_{i=1}^{n}P_i} \quad . \tag{2.9}$$

Here *Xi* is the peak-to-average ratio of the *i*th carrier. If there are n carriers in a given operating bandwidth, it is easy to see that the theoretical maximum peak-to-average power ratio will be $\sqrt{n}$. Gaussian noise has a peak-to-power ratio of about 9 dB, so very dense multi-carrier systems might require about 6 dB more power backoff to achieve a similar level of IM distortion compared to a two-carrier signal having the same power.

2.1.14 Nonlinearity effect in power amplifier use two-tone analysis

There many different ways to measure the nonlinearity behavior of an amplifier. The simplest method is the measurement of the 1dB compression power level P1dB.

Another method that uses two closely spaced frequencies:

$$Vi(t) = v\cos(\omega_1 t) + v\cos(\omega_2 t) \quad (2.10)$$

Vi input to amplifier and measure the output frequencies component, this is so-call the inter-modulation (IM) products. The third-order products are at frequencies 2ω2-ω1 and 2ω1-ω2, and the fifth-order IM products are at frequencies 3ω2-2ω1 and 3ω1-2ω2. The third-order Intercept point (IP3) is a concept that represents the intersection between the extrapolated 1:1 slope of fundamental gain, and the 3:1 slope of the third-order IM (IM3) products. IM3 is given by [23]:

$$IM3(dBc) = \frac{P_{2\omega_1-\omega_2}}{P_{\omega_1}} = \frac{P_{2\omega_2-\omega_1}}{P_{\omega_2}} = 2(IP3 - P_f) \quad (2.11)$$

where Pf (dBm) is the average value of $P_{\omega 1}$ and $P_{\omega 2}$.

Another "softness" of the compression characteristic can be varied by choosing two tangible parameters, PCOMP and PSAT. PCOMP represent, in decibels, the different between the P1dB compression point and the maximum linear power point; PSAT represent, in decibels, the different between the saturated power point and the maximum linear power point, about this value, the characteristic is defined to be ideally flat, or saturated. The detail discuss of nonlinear effect can be studied at [24].

2.1.15 AM-to-PM Effect

Any amplifier, when driven into a strongly nonlinear condition, will exhibit phase as well as amplitude distortion. This usually is characterize in terms of AM-to-PM

conversion and represents a change in the phase of the transfer characteristic as the drive level is increased toward and beyond the compression. The most common manifestation of AM-to-PM effects is an irritating asymmetrical slewing of the inter-modulation (IM) or spectral regrowth display. The detail discuss of AM-to-PM effect can be studied at [24].

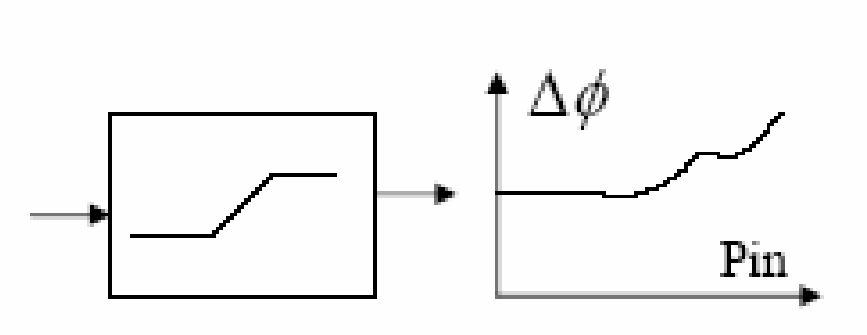


***Figure 2.5*: phase-shift distortion with input power increases**

2.2 Class of power amplifiers

What determine the class of operation of power amplifier is conduction angle of amplifier, input signal overdrive, and the output load network. Figure 2.6 shows how the PA relates to conduction angle and the input signal over-drive. For a small RF input signal V*in,* the amplifier can operate in class A, AB, B, or C depending on the conduction angle (bias voltage relative to the transistor's threshold voltage). The PA efficiency can be improved by reducing its conduction angle by moving the design into class C operation, but at the expense of lower output power. An alternative approach to increasing efficiency without sacrificing output power is to increase the input over-drive such that the transistor acts as a switch.

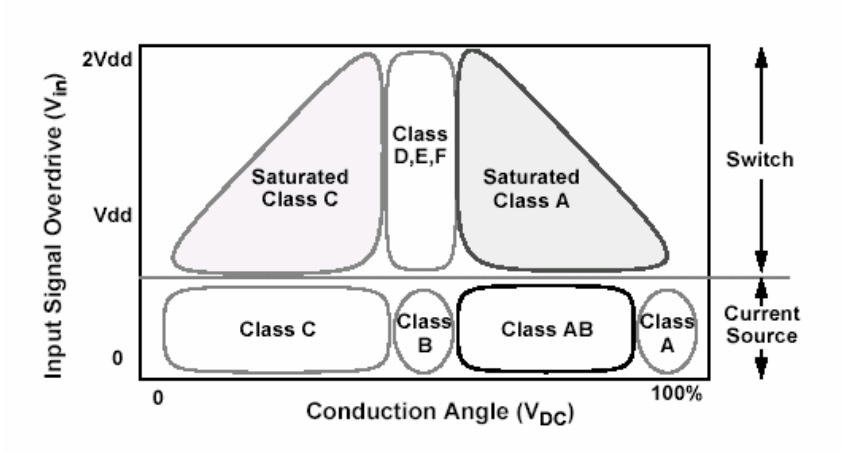


***Figure 2.6*: classification of Power amplifier**

2.2.1 Class A, AB, B, and C power amplifiers

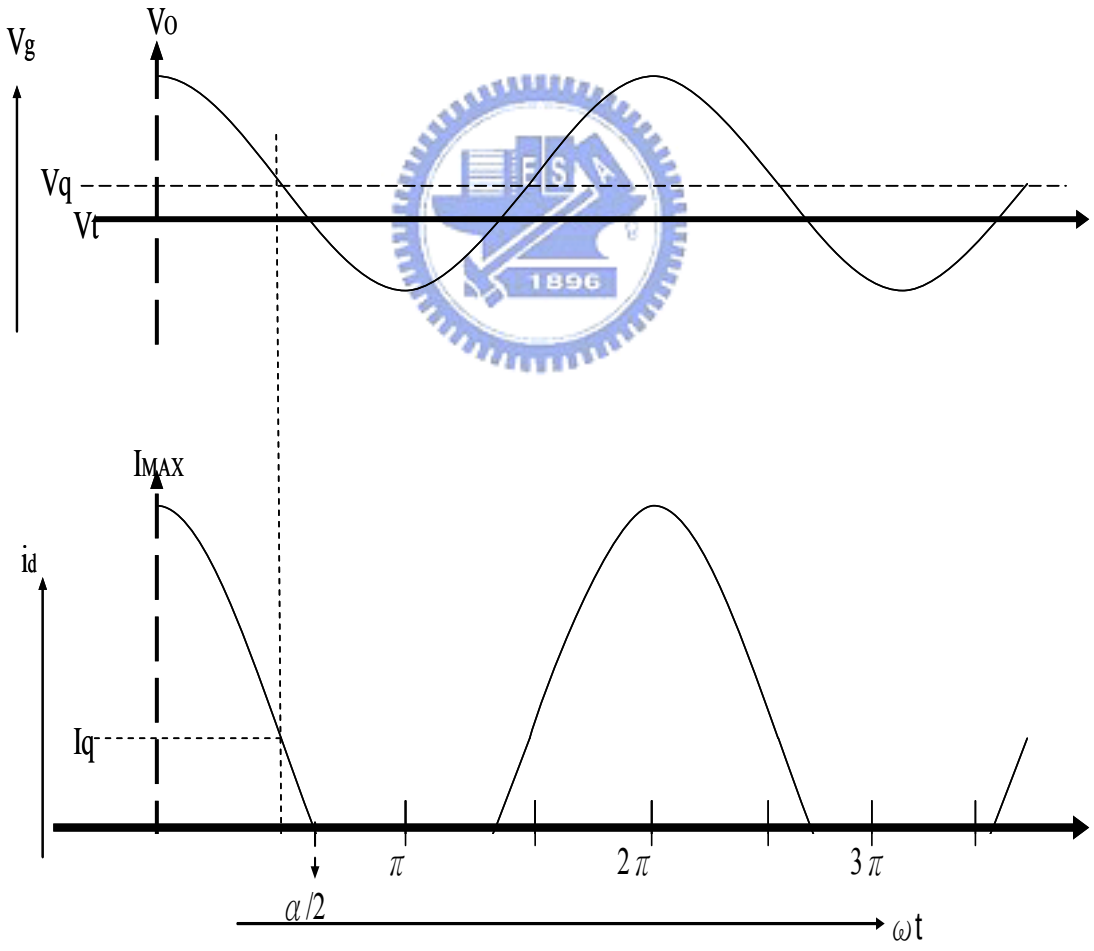


Figure 2.7: Reduced conduction angle current waveform

The simple process of reducing the conduction angle is illustrated in Figure 2.7, where Vt is the threshold voltage of Vgs for transistors. The required signal voltage amplitude will be

$$Vs = (1\text{-}Vq), \tag{2.12}$$

Where Vq is the normalized quiescent bias point, defined according to Vt=0, Vo=1. The current in the device has the familiar looking, truncated sine-wave appearance. The conduction angle, α, indicates the proportion of the RF cycle for which conduction occurs, the current cutoff points point are at ±α/2. So the drain current waveform can be written as

$$\begin{aligned} i_d &= I_q + I_{pk}\cos\theta \quad -\alpha/2 < \theta < \alpha/2 \\ i_d &= 0 \quad -\pi < \theta < -\alpha/2; -\alpha/2 < \theta < \pi \end{aligned}, \tag{2.13}$$

By Fourier analysis of the waveforms, the results can be written:

$$In = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)}[\cos\theta - \cos(\alpha/2)]\cos n\theta d\theta \quad , \tag{2.14}$$

then it is clear that

$$Idc = \frac{I_{\max}}{2\pi}\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}$$

$$I_{fundamental} = \frac{I_{\max}}{2\pi}\frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \quad ,. \tag{2.15), (2.16}$$

We use the conduction angle to define the class of power amplifier, for class A condition, α=0; for class B condition, α=π; for class AB condition, 0<α<π; and for the condition of class C, α>π. The harmonics amplitude is plotted in Figure 2.8. We can

see the odd harmonics be seen to pass through zero at the class B point, but in AB mode, the third harmonic is not negligible.

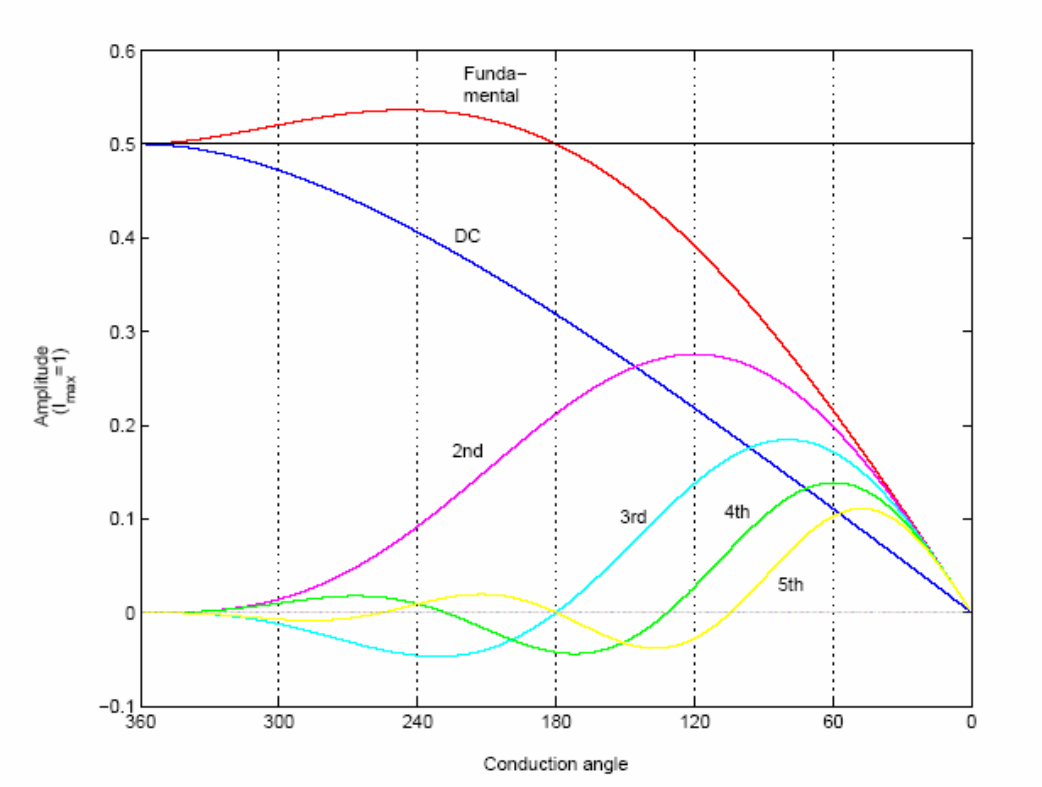


***Figure 2.8*:** Fourier component of power amplifier relate to conduction angle

Then, the RF fundamental output power is given by

$$P1 = \frac{Vdc}{\sqrt{2}}\frac{I1}{\sqrt{2}}$$
$$Pdc = VdcIdc \quad , \qquad (2.17),\ (2.18)$$

the output efficiency is defined by:

$$\eta = \frac{P1}{Pdc} \quad , \qquad (2.19)$$

then we can plot the result on Figure 2.9. From this Figure the main features of class A, AB, B and C can be determined.

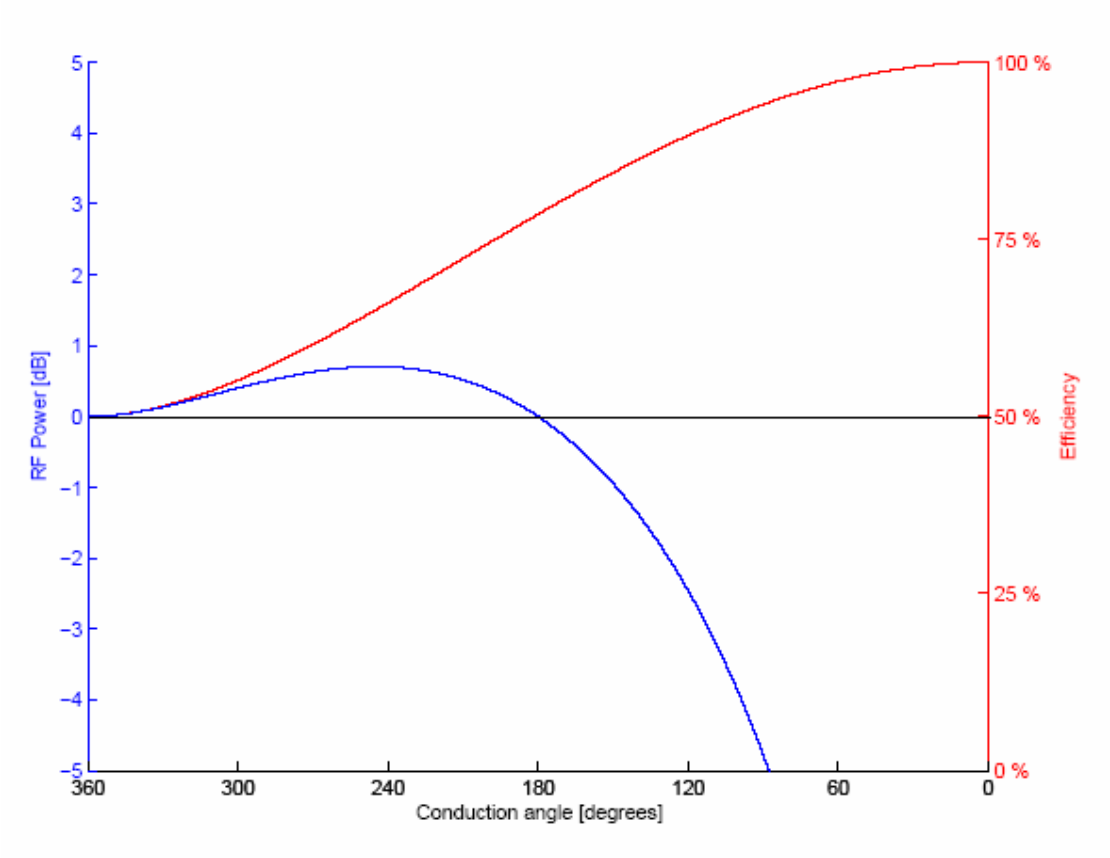


***Figure 2.9*:** RF power and efficiency with conduction angle sweep; assume optimum load and harmonic short.

2.2.2 Class D, E and F power amplifier

In this class the active device works as a switch; with very low resistance in the "ON" state and very high impedance in the "OFF" state, and respect to the load impedance. If the "ON" resistance is negligible, no power dissipation in the device and if the "OFF" impedance is very large, no current flows through the device. Therefore, in an ideal switching amplifier one can achieve 100% drain efficiency. The different between a class D and a class E is that a class E amplifier has a high Q-tuned circuit at the output of the device provide desired reactive load at the fundamental frequency

and open to other higher harmonics.

A class F amplifier is designed in the same manner as a class AB/B amplifier, except that the output circuit is designed to present a short circuit to the second harmonic and an open circuit to the third harmonic. The output waveform could become a square, such as a switch, and the theoretical efficiency approaches 100%.

Switch mode power amplifier in practice, efficiency could be degraded because the finite ON resistance and also there is significant transition time from the ON state to the OFF state and vice versa.

2.2.3 Power Amplifier Stability Issues

General speaking, k-factor analysis is useful to a linear two-port devices, it is usually a satisfactory assumption to assume that RF oscillations in power amplifiers will more likely occur when the amplifiers is backed off into its linear region, where the k-factor analysis is valid. At the condition of class AB or B operation, it is necessary to increase the quiescent current to perform the stability analysis with a represent amount of gain.

Stability of multi-stage amplifier is usually used k-factor analysis of individual stages. Any single stage must be designed with k-factor greater than unity from the low-frequency bias circuit range all the way up to the frequency at the gain rolls off to lower than unity. The use of resistive element will affect the efficiency of the PA, and

is an effective way to obtain good stability performance.

$$k = \frac{1 - |S11|^2 - |S22|^2 + D^2}{2|S11||S12|}, D = S11 * S22 - S12 * S21 \quad ,. \qquad (2.20)$$

2.3 Challenges of RF power amplifiers in CMOS technology

CMOS technology is not friendly towards design of power amplifiers. We simple list some issues that affected the PA performance.

2.3.1 Low breakdown voltage of deep sub-micron technologies.

This limits the maximum gate-drain voltage and delivering lower power. Unfortunately, COMS technology has lower current drive, the single stage gain is very low, and multiple stages would be used but affect the linearity and efficiency of amplifiers.

2.3.2 Substrates coupling effects

In contrast to semi-insulating substrates, a highly doped substrate is common in CMOS technology. This results in substrate interaction in a highly integrated CMOS IC. The leakage from an integrated power amplifier might affect the stability of other circuits, for example the VCO or LNA.

2.3.3 Large signal CMOS RF models

Conventional transistor models for CMOS devices have been found to be moderately accurate for RFIC. And need to be improved for analog operation at radio frequencies. Large signal CMOS RF models and substrate modeling are critical to the successful

design and operation of integrated CMOS radio frequency power amplifiers, owing to the large currents and voltage changes that the output transistors experience [16]. So that, traditional PA design relies heavily on data measured from single transistors, such as load-pull measurement. It is noted that the RF model of TSMC 0.18μm is not sufficient accurate to support the large signal, because the RF devices only have one width with 5μm*(number of finger), and the source wire line would not sufficient width to supply the large current of large transistor. As the result, some un-expectably effect might cause the RF model un-accurate.

2.3.4 Low-Q passive element at the output matching network

Since the inherent output device impedance in the power amplifier case is very low, impedance matching require higher impedance transformation ratios, it becomes very difficult. The output matching elements require lower loss, and good thermal properties since there are usually significant RF currents flowing in these elements. However, in CMOS technology, the losses in the substrate will decrease the quality factor (Q) of the passive element in the matching network, this great reduce the efficiency of circuits.

2.3.5 Electro-migration and reliability of CMOS devices

The power amplifier operation at a high output power state, large current and high voltage swing, this can be cause electro-migration and parasitic effect in the circuit

may cause performance degradation [16] and reliability problems. After a long time, the output power of PA should be degrade [25].

How long a CMOS PA can work? The recommended voltage to avoid hot carrier degradation is usually based on DC/transient reliability tests, and designer bias at the level below the result of tests [25].

Chapter3

Simulation of 5.2GHz Power Amplifier for 802.11a Application by using cascade

3.1 overview of 802.11a WLAN standard

The 802.11a standard operates as illustrated in Figure 3.1[26], in the 5-GHz unlicensed national information infrastructure (UNII) band, which provides a total available signal bandwidth of 300 MHz, and the bandwidth is larger than 802.11b which provides 85 MHz total bandwidth. As indicated in Figure3.1, the 802.11a standard has each channel bandwidths of 20 MHz with a data rate up to 54 Mb/s. The 802.11a standard use orthogonal frequency division multiplexing (OFDM) with 52 subcarriers, which can be either a BPSK (6 & 9Mb/s), QPSK (12 & 18Mb/s), 16-QAM (24 & 36Mb/s), or 64-QAM (48 & 54Mb/s) signals [27]. 802.11a standard allows the use of direct conversion transceivers [28], which have the disadvantage of DC offset or carrier leakage.

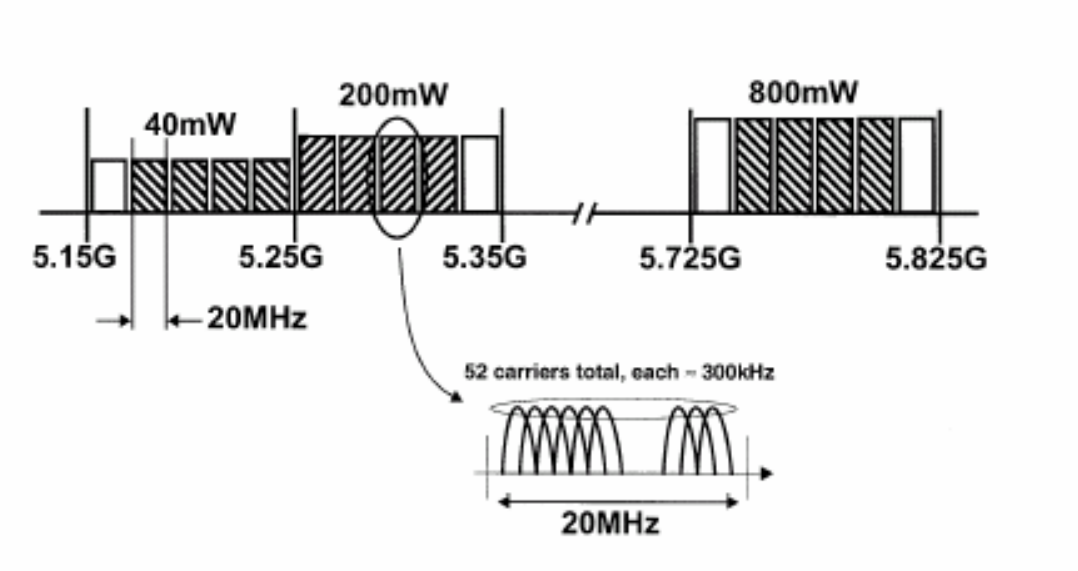


***Figure 3.1*:** Channel of EEE802.11a wireless WLAN

3.2 The PA issues of 802.11a transmitter

We continually to discuss with OFDM, which provides resistance to narrow band fading and interference, and reduced computational complexity compared to other modulations that require a time domain equalizer, and OFDM is well to against phase variation (group delay) across the channel. However, the peak to average power ratio of the OFDM signal is large. By theorem, 52 carriers have peak to average ratio as high as √52 or 17dB, it means that to obtain 40mW (16dBm) output power requires Psat of ~33dBm or 2W. If we use 16-QAM to reduce PAR to 6dB, it also requires Past of ~22dBm or 160mW output. Fortunately, in practical OFDM transceivers, it is not necessary to preserve extreme peaks in order to demodulate the signal correctly. Used the Rapp model [27]:

$$Vout = \frac{Vin}{\left(1+Vin^{2R}\right)^{\frac{1}{2R}}} \quad , \qquad (3.1)$$

where R is the Rapp coefficient and R infinite is an ideal PA with perfectly linear transfer characteristic to a hard saturation at Psat. This model can be approximated in a PA using pre-distortion or other linearization techniques. In the case, R is infinity of 54Mb/s data rates, requires 5.4 backoff dB from Psat. It means that to obtain 40mW (16dBm) output power requires Psat of ~22dBm or 160mW output power. And such a large backoff of PA could result in poor efficiency, as shown in Figure 3.2[27]:

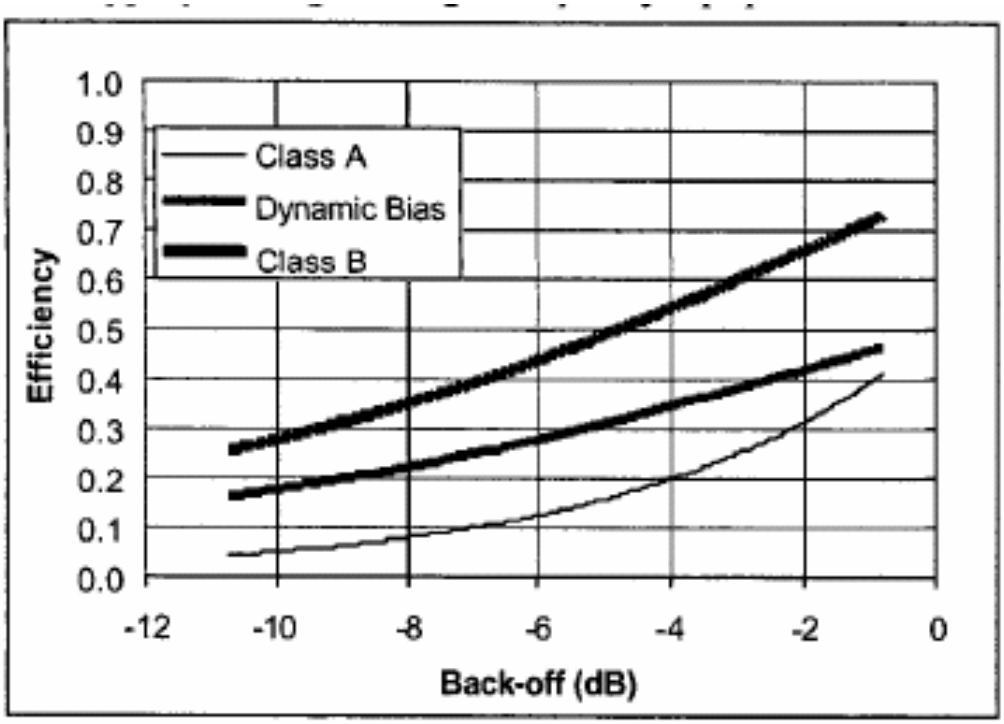


***Figure 3.2*:** Efficiency vs. Back-off in PA for OFDM

When PA operation at high output power, such as 22dBm or higher, another problem comes in deep-submicron CMOS devices. The breakdown of oxide or drain-to-source, which worsen as the technology scales down. Figure 3.3 show breakdown current flow in n-channel MOSFET. In MOS devices, one may identify four primary limits to allowable applied voltage in PAs. These are drain (or source) diode zener breakdown,

drain-source punch through, time-dependent dielectric breakdown, and gate oxide rupture.

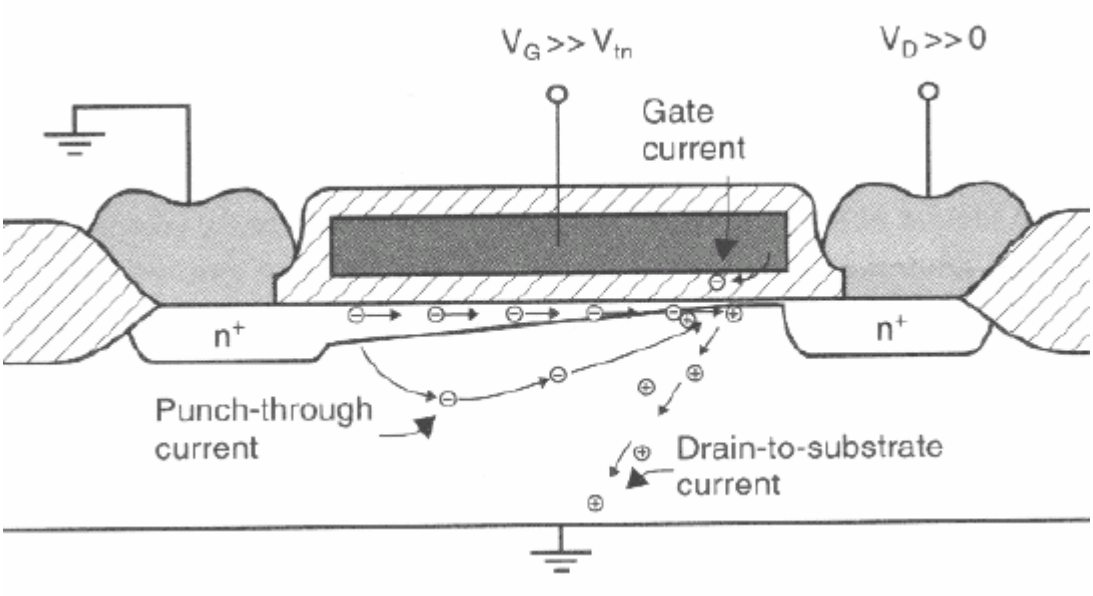


***Figure 3.3*:** Breakdown current of NMOS device

For example, in TSMC 0.18 μm process, typical breakdown voltage is Vgs 1.8V, and Vds 1.8V. Depending on the Class of operation Vds can swing 2 time the DC supply voltage, and even higher, oxide breakdown should occur when the difference between Vg-to-Vs or Vg-to-Vd are large than 1.8V. Also, when Vds is larger than 1.8V. This effect dominates the PA performance of CMOS, if we assume that 2VDD is 1.8V, and use 1Ω to load, we should have 400mA DC current and 180mW (22.5dBm) output power in Class A condition. Such 400mA current is huge and can cause electro-migration, and low output impedance have a high sensitivity to parasitic resistance in the matching network.

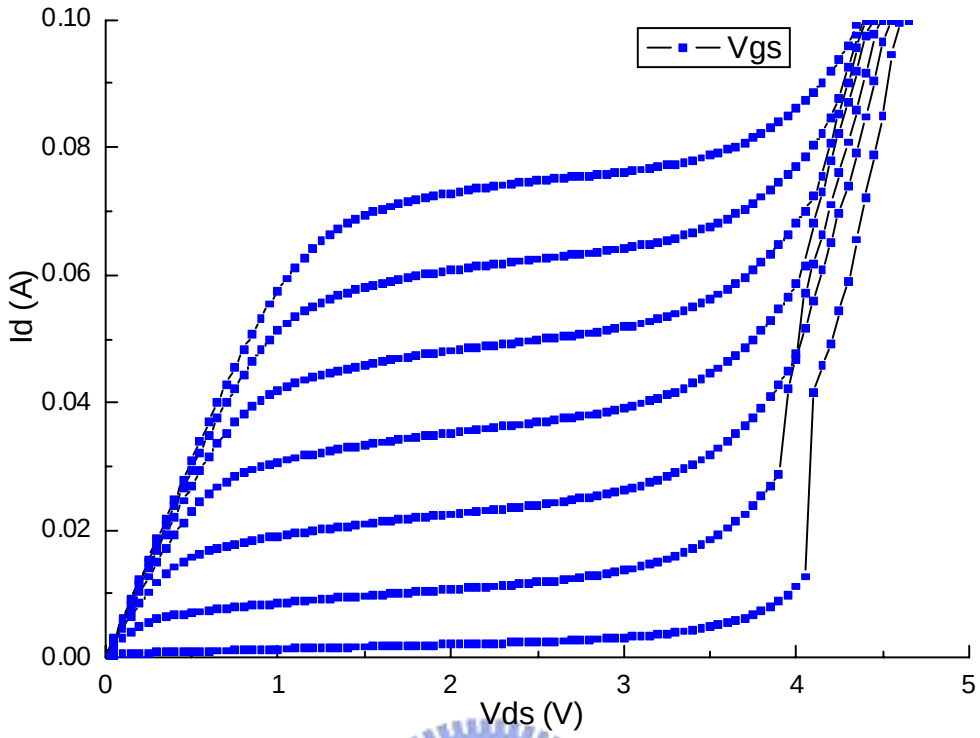


***Figure 3.4*:** Practical measurement of I-V curve in NMOS

Figure 3.4 show the practical I-V measure data of 0.18 μm n-MOSFET, Vd sweep from 0V to 4.5V and Vg sweep from 0.6V to 1.8V with 0.2 voltage step. It is clear that drain-source breakdown voltage is larger than 1.8 V and even up to 3V. We adjust the 2VDD to 3.0V, and use 1Ω to load, we should have 240mA DC current and 180mW (22.5dBm) output power in Class A condition, it large reduce the DC current. If we use cascade configuration to eliminate the oxide breakdown, VDD can be relaxed to 3.3V. The cascade configuration was used to increase the maximum available supply voltage [25] [13], and also increase the stability of circuit. So far, in cascode power amplifiers, the common-gate transistor has had a constant DC voltage with an RF ground. With large-signal operation, the voltage swing on gate-drain of

the common-gate transistor becomes larger than that of the common-source transistors, which becomes the bottleneck in terms of breakdown or hot carrier degradation [25].

3.3 Simulation of Power Amplifier for 802.11a application

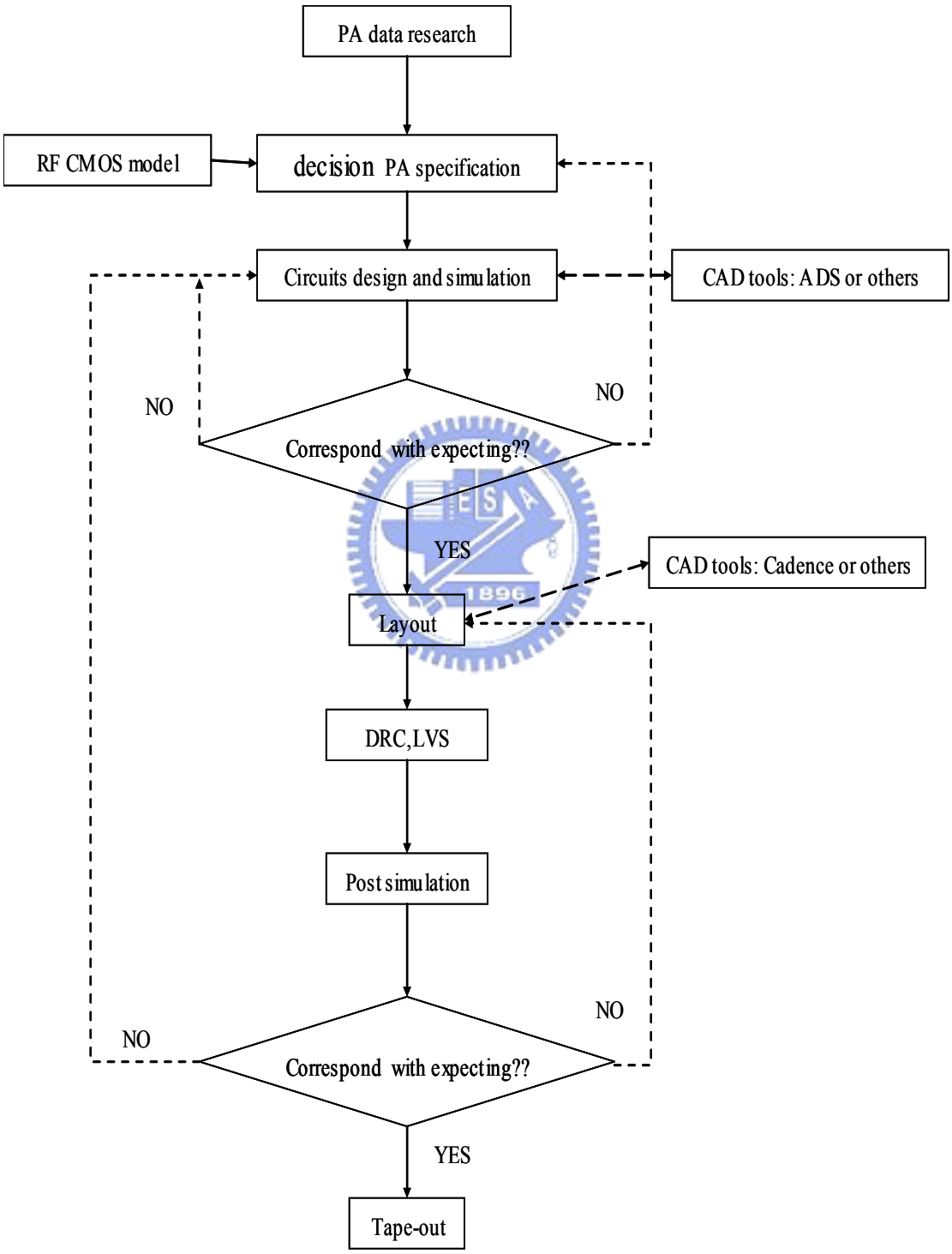


***Figure 3.5*:** Typical amplifier design flow

We start to design a two stage power amplifier, typical design flow is shown on Figure 3.5. The simulation tools are ADS, which can supports load-pull and large signal simulation. TSMC 0.18 μm process is used in this work, and small signal model and large signal model are supported by TSMC. Now, begin to design a power amplifier by following temps.

1. Simulation of Cascode configuration

We start to design output stage with I-V curve simulation. And decide the NMOS sizes and bias voltage to insure that the maximum output power delivered to load and the PAE proper to the design goal. It is shown the NMOS of 5 μm unit gate width has good performance compare to other size [29].

2. Simulation of output matching network

The detail of load line matching network is discussed by Steve C. Cripps "RF Power Amplifiers for Wireless Communications", and if we want to filter out the harmonics distortion, we select the band-pass type. Band-pass type also provide against low frequency oscillation.

3. Simulation of driver stage

Two stage power amplifier is popular, because it increases the total gain and isolation, engineers are easy to design output matching network and input matching network, however, inter-stage matching network become a issue. The driver stage

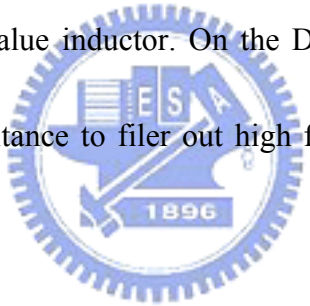
would be used to driver the power stage, and provide the input power of power stage is on the maximum PAE condition.

4. Simulation of input matching network

Input matching is designed by small signal theorem.

5. Design the bias circuit

We use the resister to bias the gate voltage, it increases stability of circuit but resister value variation by process must be considered. We use the RF choke at output drain, RF choke is typical a large value inductor. On the condition of this work, we use bias-tee instead of a large value inductor. On the DC supply nodes that no signal translates, we shunt a capacitance to filer out high frequency noise and insure AC ground.



3.4 Simulation results of 5.2GHz Power Amplifier

- Figure 3.6 shows the cascode configuration schematic and I-V curve simulation.
- Figure 3.7 shows the output matching network simulation.
- Figure 3.8 shows the schematic of two stage power amplifier.
- Figure 3.9 shows the Stability from 1 GHz to 10 GHz (Mu & MuPrime).
- Figure 3.10 shows the P1dB is -3dBm.
- Figure 3.11 shows the OIP3 is 29.7dBm.
- Figure 3.12 shows the maximum PAE is 17%.

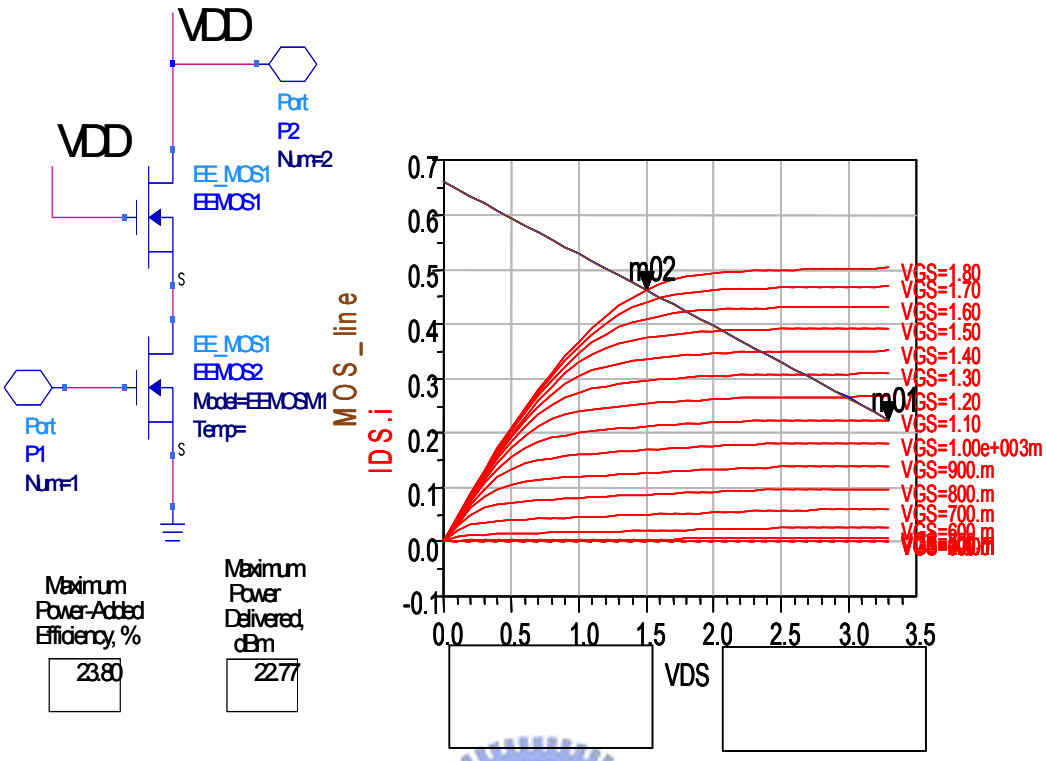


***Figure 3.6*:** Cascode configuration I-V curve and load-line simulation

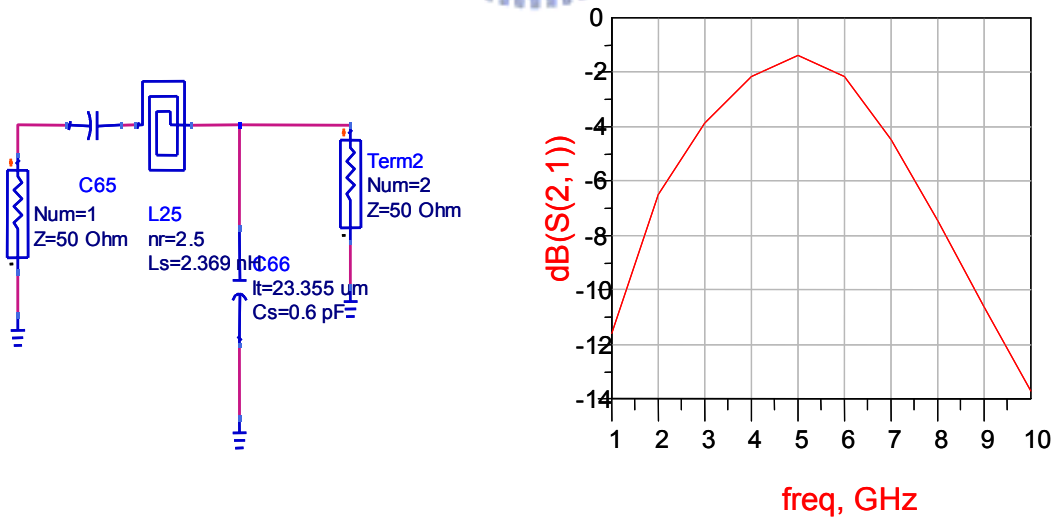


***Figure 3.7*:** Simulation of output band-pass filter

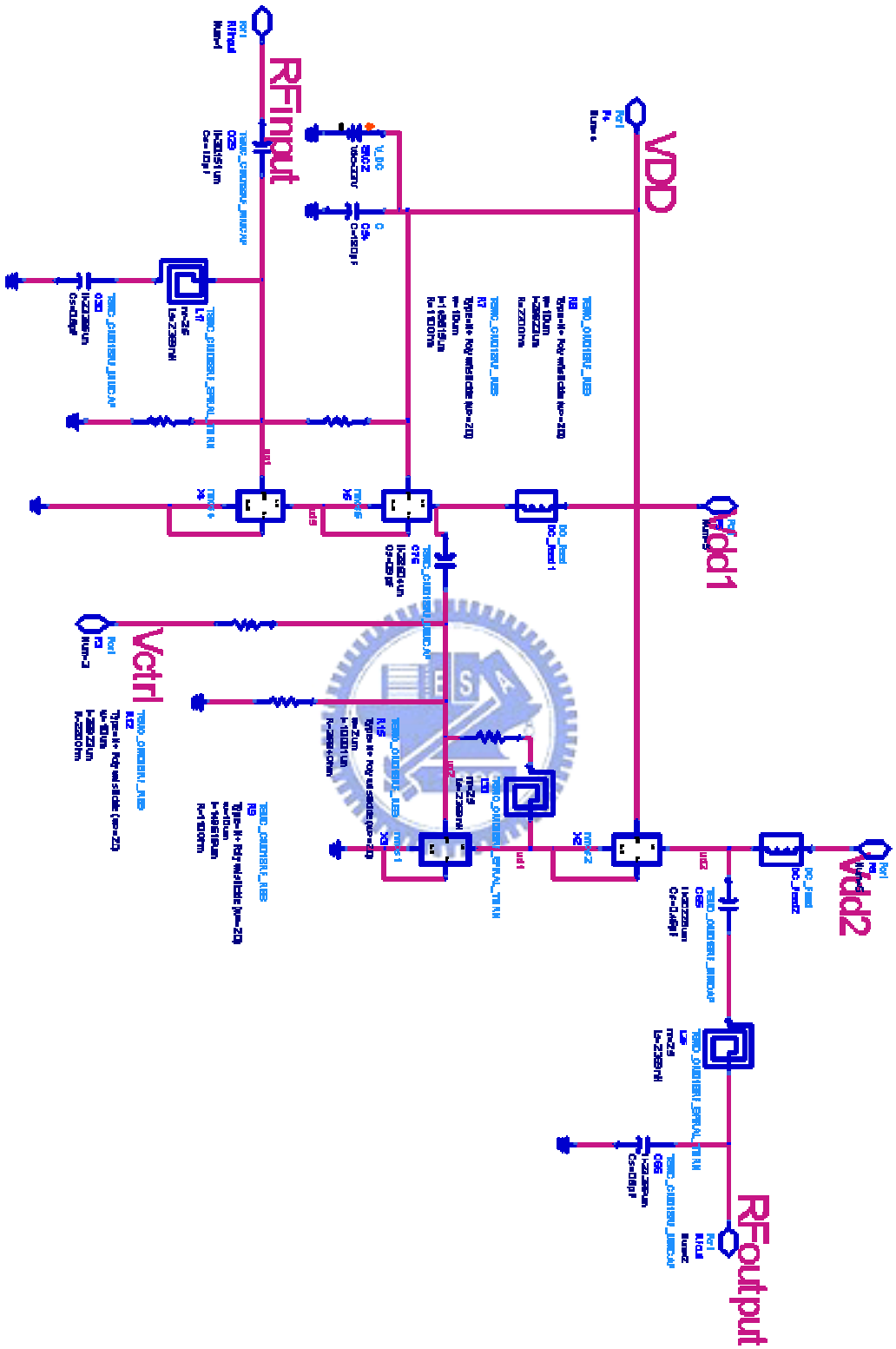


***Figure 3.8*:** schematic of 5.2GHz PA

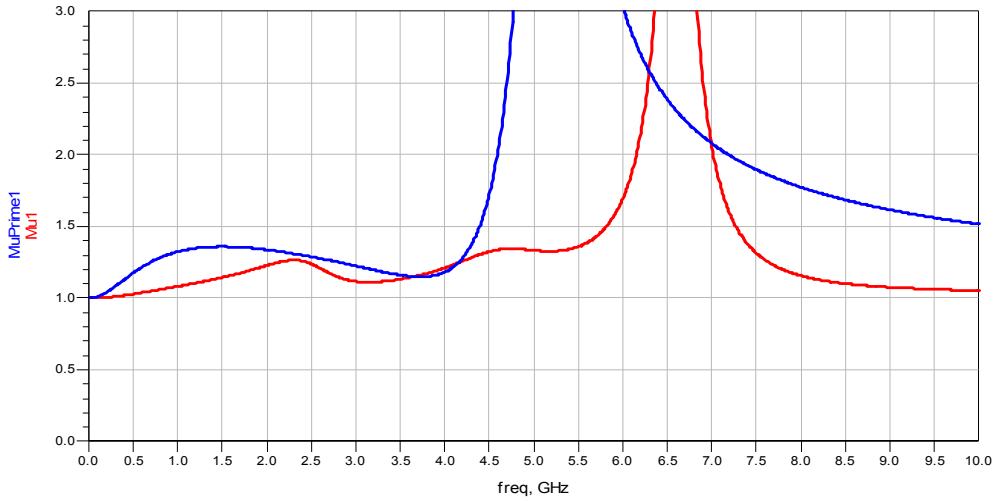


***Figure 3.9*:** The stability of 5.2GHz PA

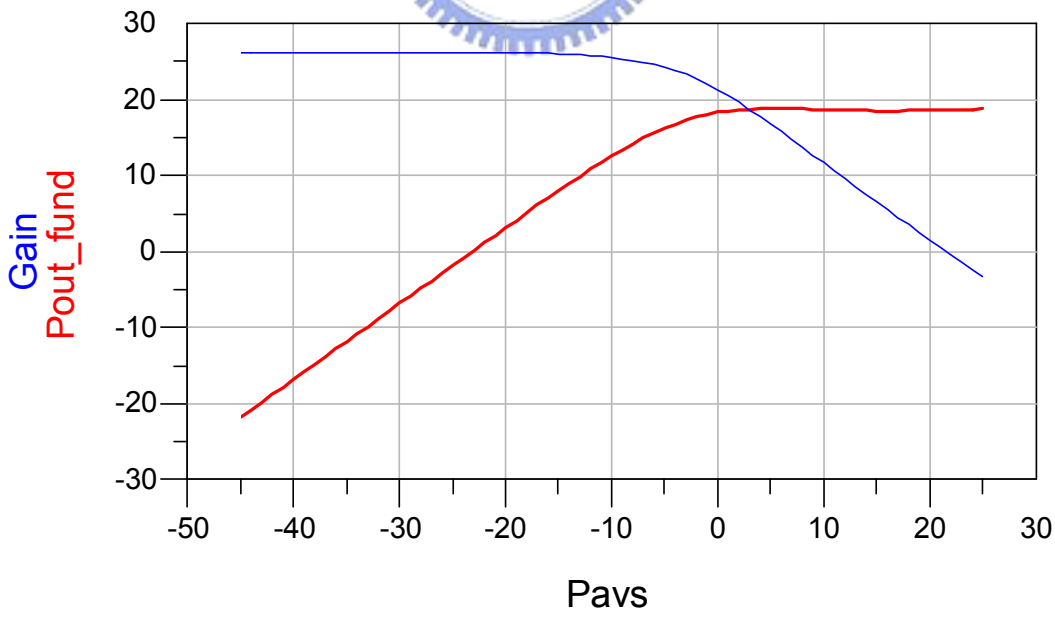


***Figure 3.10*:** Gain and output power of 5.2GHz PA

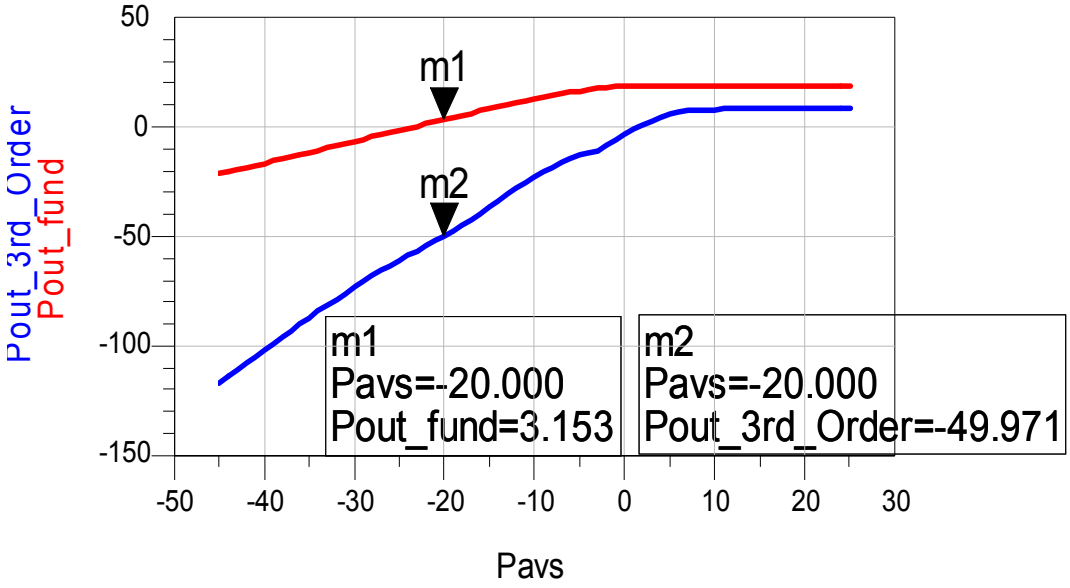


***Figure 3.11*:** IM3 of 5.2GHz PA

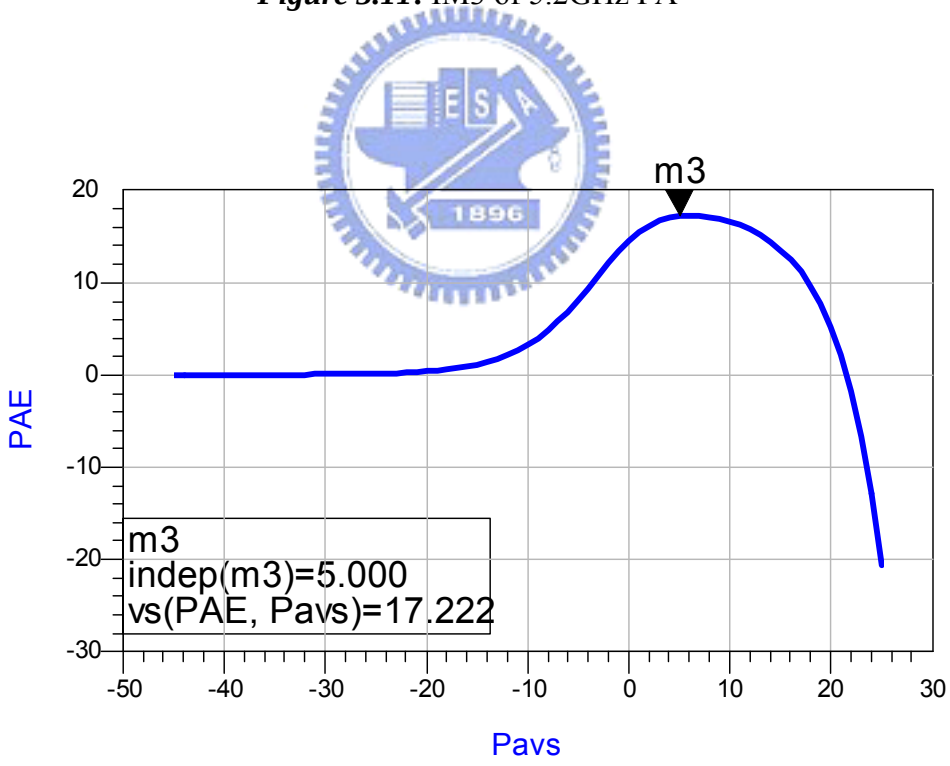


***Figure 3.11*:** Input power vs. PAE in 5.2GHz PA

***Table 3.1*:** Simulation results of 5.2GHz PA

B.W.(GHz)	Gain(dB)	P-1dB(dBm)	IP3(dBm)	PAEmax(%)	Current consumption (mA)
5.2	26	-3	29.715	17.222	204

3.5 layout consideration

The power amplifier was layout using CADENCE layout tool. The layout of RF power line requires special attention. The output transistor carries 160mA of DC current, plus the RF current, and has metal line width about 200μm to ensure against electro-migration. The transistor is arranged in 2 groups of transistors, each have 128 fingers with 5μm width and 0.18μm gate length. The source of NMOS must be careful, because the 5μm width of each finger, regardless of fingers number, the width of source metal line is about 10μm~15μm. This replies that we should increase width of source and avoid gate-source overlap. The capacitance is used metal-insulator-metal (MIM) capacitance supported by TSMC, the resister is used with P+ w/o silicide resister supported by TSMC.

Considerate bond-wire inductance effect and large current of NMOS source or drain, the PAD which are connected to the NMOS source or drain must use as many as design can tolerate. We also pay attention to symmetry of layout, the transistors were all arranged on center line of the layout. The practice layout is shown on Figure 3.13.

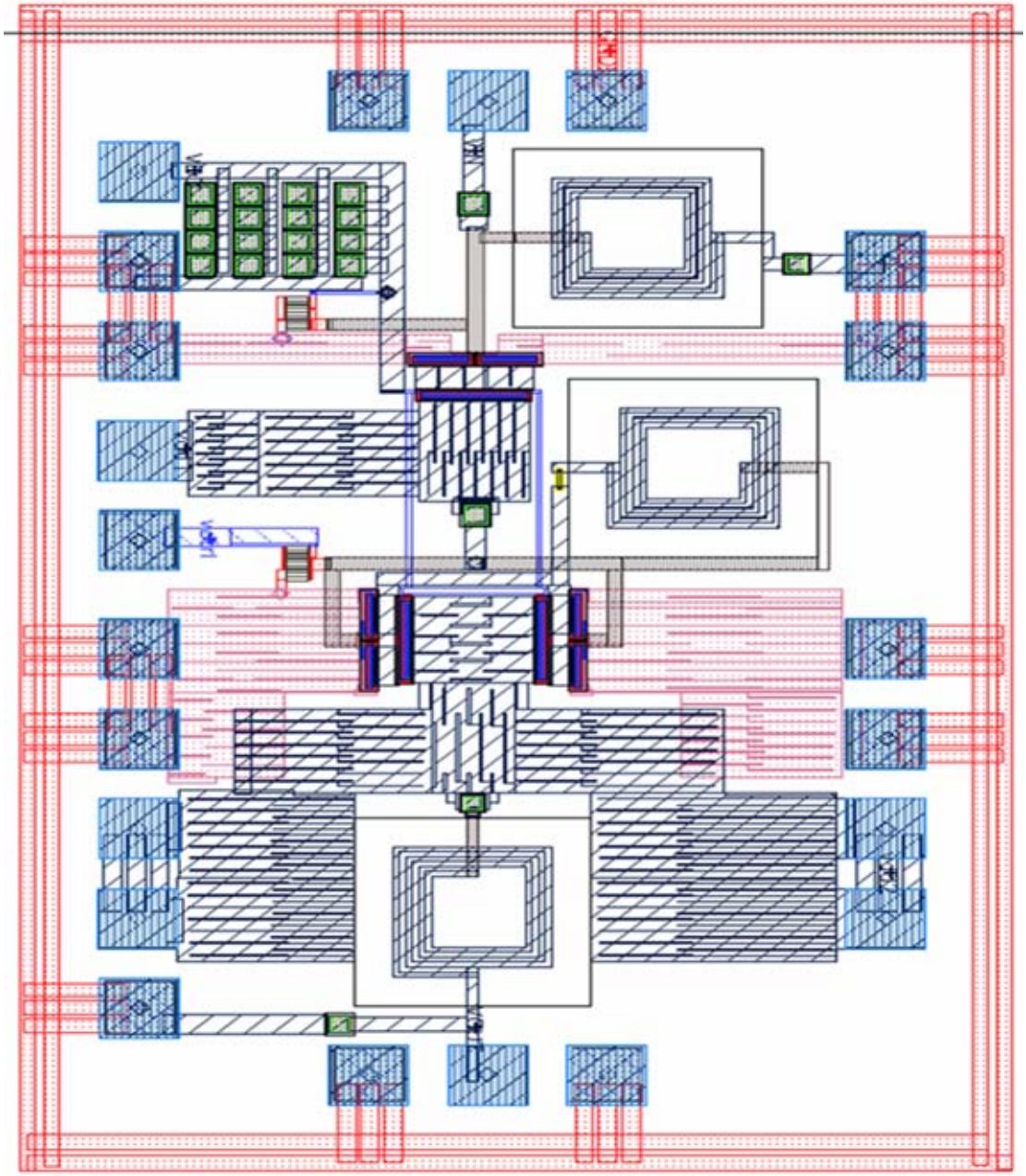


***Figure 3.13*: layout of PA**

3.6 Discussion

The 5.2GHz Power Amplifier did not tape-out because the die size, 1.955 x 1.258 (mm^2), is too large. The grade of CIC deliberation is C, and because of the total area of CIC is not enough the power amplifier did not tape-out. So there is no practical measurement date.

Chapter4

UWB CMOS Power Amplifier

4.1 Introduction of IEEE802.15.3a and UWB

The purpose of IEEE802.15.3 standard is to provide a specification for a low complexity, low cost, low-power consumption and high data rate wireless connectivity among devices within or entering the personal operating space. The data rate must be high enough (greater than 110Mbps) to satisfy a set of consumer multimedia industry needs for WPAN (Wireless Personal Area Networks) communications. The standard also addresses the quality of service (QoS) capabilities required to support multimedia data types. Devices included in the definition of Personal Area Networks are those that are carried, worn, or located near the body. Specific examples of devices include those that are thought of as traditionally being networked, such as computers, personal digital assistants (PDA), handhelds personal computers (HPC), and printers. It also includes other devices such as digital imaging systems. Study group 802.15.3a has been working for the past year with strong involvement of leading UWB companies. Strong support from Consumer Electronics companies in 802.15.3 will ensure the standard results in products delivered to the

market. The technical requirements developed by the study group are summarized in Table 4.1[30]. The system must be able to operate effectively in the presence of other 802.15.3a systems and in presence of other IEEE systems such as 802.11a. It is also important that the power consumption be low, to enable wireless connectivity on battery operated portable devices.

Table4.1: IEEE 802.15.3a Requirements

Parameter	Value
Bit rate	110 , 200,480 Mb/s
Range	30 and 12 ft
Power Consumption	100 and 250 mW
Bit error rate	1e-5
Colocated piconets	4
Interference capability	Robust to IEEE systems
Co-existence capability	Reduced interference to IEEE systems

UWB is the most likely technology to be adopted for IEEE 802.15.3a standard [31]. Much of the increased attention on UWB technology is due to the landmark ruling by the Federal Communications Commission (FCC). In February 2002, the FCC opened up 7500 MHz of spectrum (from 3.1GHz to 10.6 GHz) for use by UWB devices. The traditional design approach for a UWB communication system involved using narrow time-domain pulses that occupy a very wide spectrum. The main disadvantage of such

systems is that building RF and analog circuits as well as high speed analog-to-digital converters (ADCs) to process this extremely wideband signal is a challenging problem and results in a higher power consumption. The pulsed multi-band approach eliminates the disadvantage associated with a large front-end processing bandwidth. In this approach, the spectrum is divided into several sub-bands, whose bandwidth is approximately 500 MHz. By interleaving the symbols across sub-bands, UWB systems can still maintain the same transmit power as if they were using the entire bandwidth. The advantage of this approach is that the information can now be processed over a much smaller bandwidth, thereby reducing the complexity of the design, reducing the power consumption, lowering the cost, and improving spectral flexibility and worldwide compliance. The primary disadvantage of a pulsed multi-band system is the difficulty in collecting significant multi-path energy using a single RF chain. With a single RF chain, the amount of multi-path energy collected is limited by the dwell time on each sub-band [30].

The multi-band orthogonal frequency division multiplexing (OFDM) system inherits all the strengths of the multi-band system. An OFDM technique is used to transmit the information on each of the sub-bands. The multi-band OFDM system has several good properties, including the ability to efficiently capture multi-path energy with a single RF chain, as shown at Figure4.1, and insensitivity to deal with

narrowband interferers at the receiver without having to sacrifice either sub-band of data rate. The only drawback of this type of system is that the transmitter is slightly more complex because it requires an IFFT and the peak-to-average ratio maybe slightly higher than that of the pulse-based multi-band approaches.

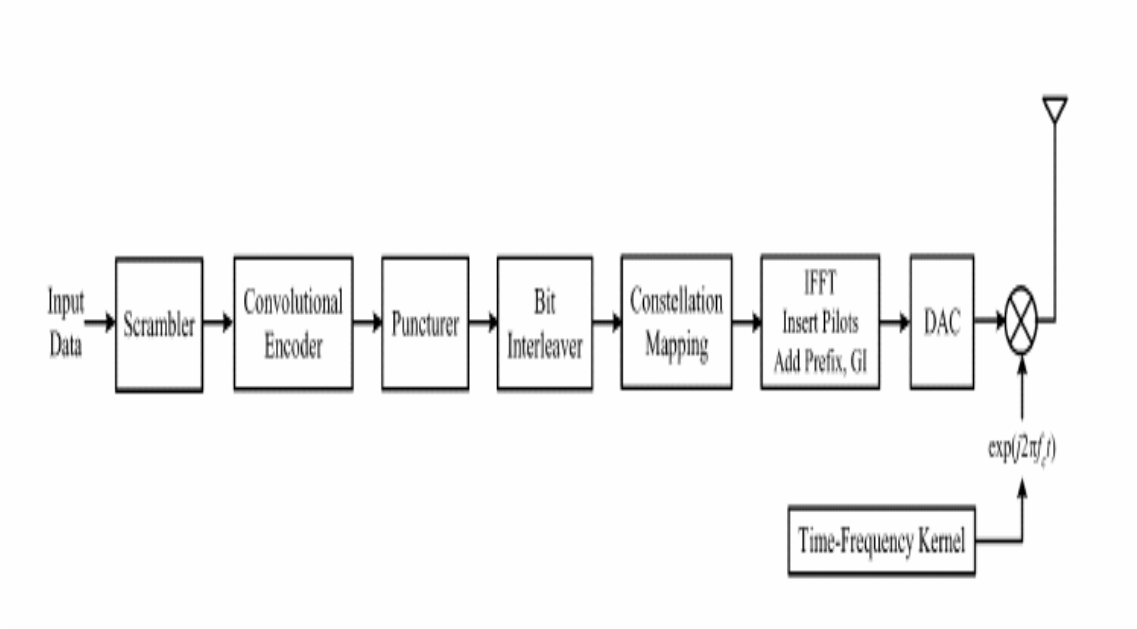


Figure4.1: Example TX architecture for a multi-band OFDM system

Two popular proposals, DS-CDMA and MB-OFDM, contend for 802.15.3a standards. The DS-CDMA proposal divides the entire allocated spectrum into two bands but excludes the 802.11a WLAN band. The frequency ranges for this proposal are from 3.2-5.15 GHz and 5.825-10.6 GHz. The DS-CDMA scheme uses traditional impulse UWB with M-ary Bi-Orthogonal Keying and a CDMA encoding scheme for multiplexing. The waveforms are shown Figure 4.2 [32].The DS-CDMA have supporters of companies such as Xtreme Spectrum, Motorola etc,.

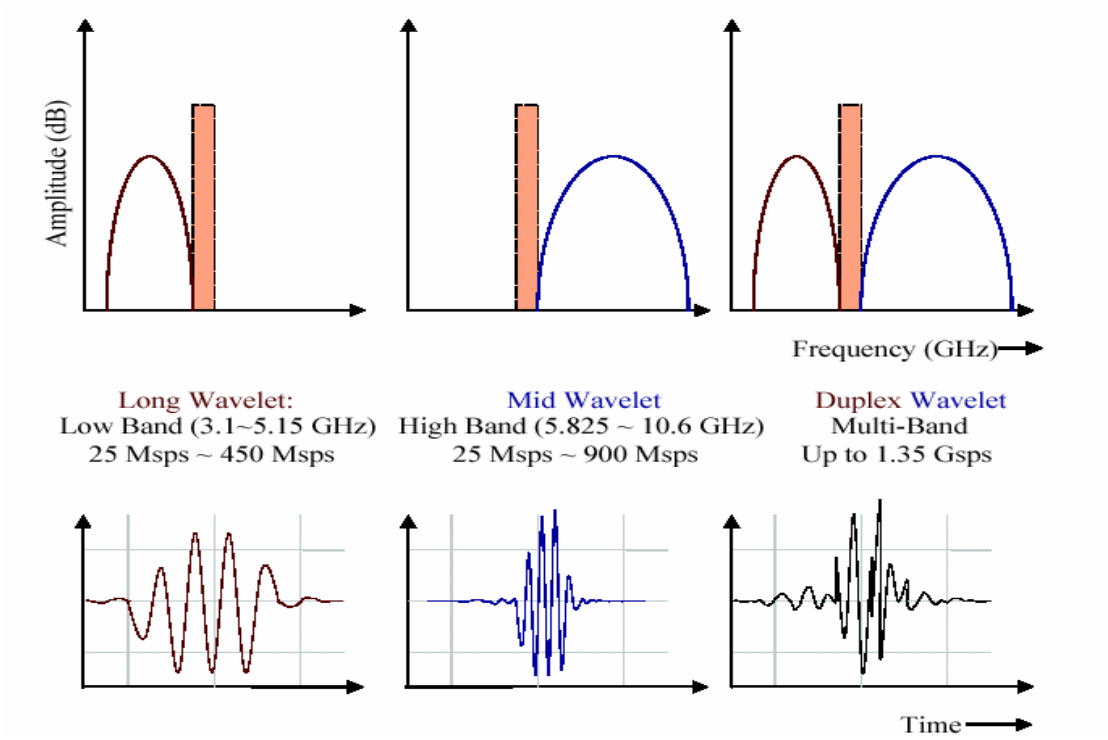


Figure4.2: The waveforms of DS-CDMA proposal

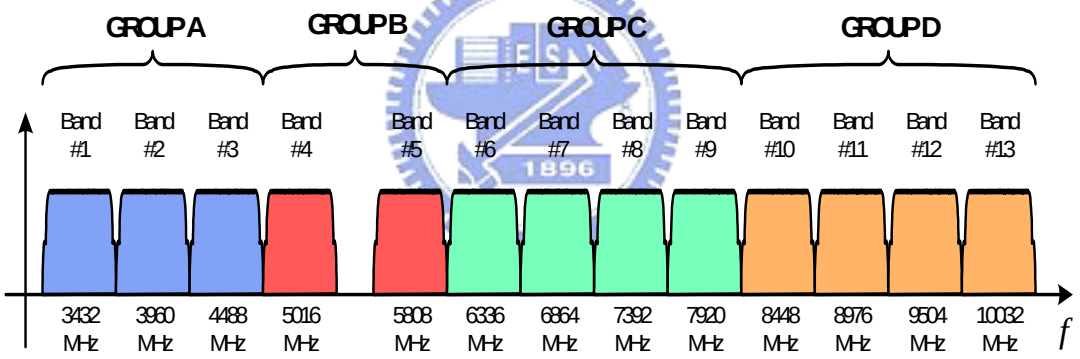


Figure4.3:13 bands and 4 groups are divided by MB-OFDM

The MB-OFDM spectrum is divided into 14 bands with 528 MHz bandwidth, and devices are allowed to statically or dynamically select which bands to use for transmission. The entire spectrum is divided into 4 distinct groups, as shown in Figure4.3.Group A: Intended for 1st generation devices (3.1 – 4.9 GHz); Group B: Reserved for future use (4.9 – 6.0 GHz); Group C: Intended for devices with

improved SOP performance (6.0 – 8.1 GHz) and Group D: Reserved for future use (8.1 – 10.6 GHz). .The MB-OFDM have supporters of companies such as Intel, TI etc,.

4.2 Design of CMOS Power Amplifier for UWB

4.2.1 The PA issues of UWB transmitter

In UWB systems, the power level from the UWB transmitter should be low enough not to interfere with the already existing communication systems, for example 802.11a. As shown in Figure 4.4[33], the low output levels that specified by the FCC is less than -41.3 dBm/MHz. Therefore, for a 7 GHz bandwidth, the peak output power is approximately-3 dBm or 500 μW. UWB systems need not require large transistors, and greatly lighten the difficult of CMOS technology. The main challenging task becomes to achieve a high gain and good impedance match over the entire frequency band.

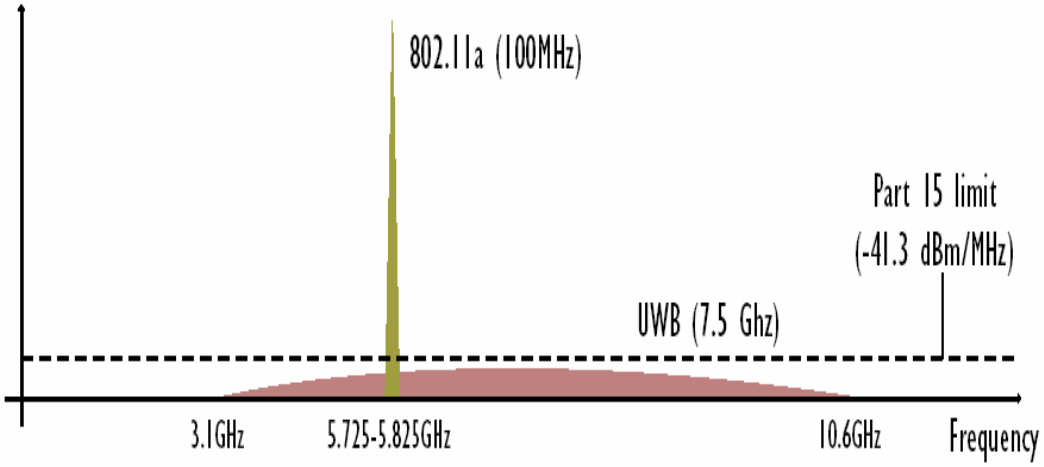


Figure4.4: The power level of UWB

Linearity is another issue in UWB systems. For constant envelope modulation schemes like GMSK, FSK, the amplitude remains constant and non-linear high efficiency power amplifier is used. However, non-constant envelope modulation schemes like CDMA, the amplitude of the signal also carries some data information and hence it is important to maintain the exact shape of the signal without introducing any distortion through the power amplifier. It is noted that because the bandwidth of MB-OFDM is less than DS-CDMA, the linearity requirements is more relaxed.

4.2.2 Wide Bandwidth Matching with Inductor-Resister Feedback

To design a UWB PA, the first consideration is to achieve wide bandwidth matching network. There are many methods for wide bandwidth matching network, such as distributed amplifier (DA) and balance amplifier etc,.

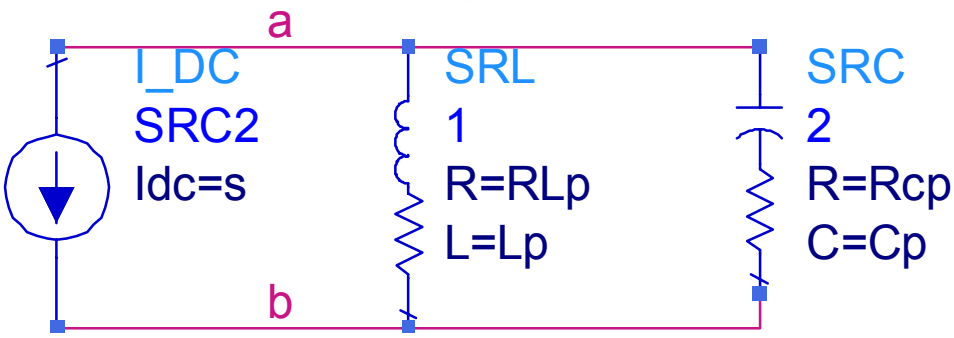


Figure4.5: Parallel resonance circuits

We consider with a parallel low Q LC circuit, as shown in Figure 4-5, and can write a admittances formula:

$$Y_{ab} = \frac{1}{r_{LP} + jX_{LP}} + \frac{1}{r_{LP} - jX_{cp}} = \frac{r_{LP}}{r_{LP}^2 + X_{LP}^2} + \frac{r_{CP}}{R_{CP}^2 + X_{CP}^2} + j\left(\frac{X_{CP}}{r_{CP}^2 + X_{CP}^2} - \frac{X_{LP}}{r_{LP}^2 + X_{LP}^2}\right), \quad (4\text{-}1)$$

When the imaginary part is zero, it indicates that the parallel circuit is at resonance, and we get

$$\frac{X_{CP}}{r_{CP}^2 + X_{CP}^2} = \frac{X_{LP}}{r_{LP}^2 + X_{LP}^2} \quad . \quad (4\text{-}2)$$

There we use $X_{cp} = \frac{1}{\omega C_P}$ and $\omega L_P = X_{LP}$, then (4-2) become

$$\omega^2 = \frac{L_P - C_P r_{LP}^2}{L_P C_P (L_P - C_P r_{CP}^2)} \quad . \quad (4\text{-}3)$$

From (4-3), if we choose

$$r_{LP} = r_{CP} = \sqrt{\frac{L_P}{C_P}}, \quad (4\text{-}4)$$

then the tank circuit should be pure resistance at any frequency.

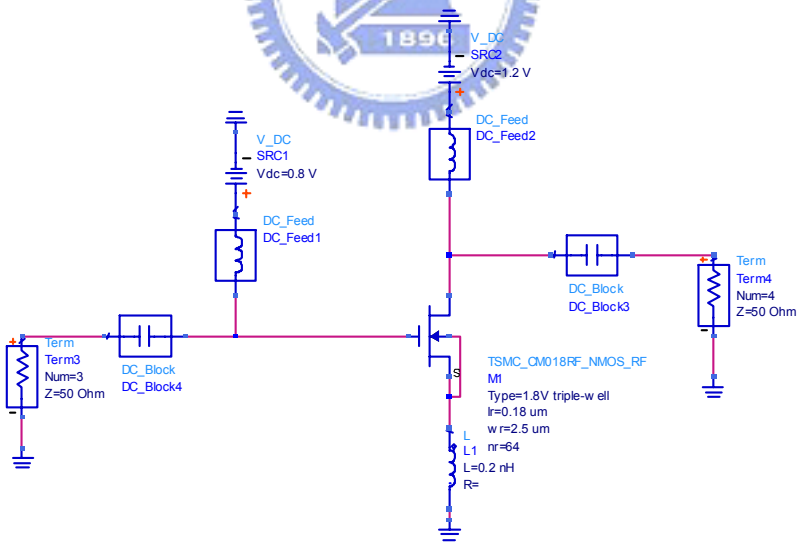


Figure4.6: A CS amplifier with inductor degeneration

Figure 4-6 show a common-source amplifier with inductor degeneration, it is not hard to show that input impedance has the following form:

$$Z_{in} = \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_S \approx \frac{1}{sC_{gs}} + \omega_T L_S \,. \tag{4-5}$$

And we consider an inductor-resistor feedback amplifier which is shown at Figure 4-7, the feedback circuit can be analysis by Miller approximation. It is result that an equivalent circuit is shown at Figure 4-8, where Lf= (L2/Av) and Rf= (R2/Av), Av is noted as voltage gain. Figure4-8 is similar to Figure 4-5, if we set $Cgs = C_P, Lf = L_P$ and $r_{CP} = \omega_T L_S$. And from (4-4) we can get the formula

$$Lf = (\frac{g_m}{C_{gs}} L_S)^2 \times C_{gs} = (g_m L_S)^2 / C_{gs}\,, \tag{4-6}$$

and

L2=Av*Lf. (4-7)

From (4-6) and (4-7), feedback inductor can be decided.

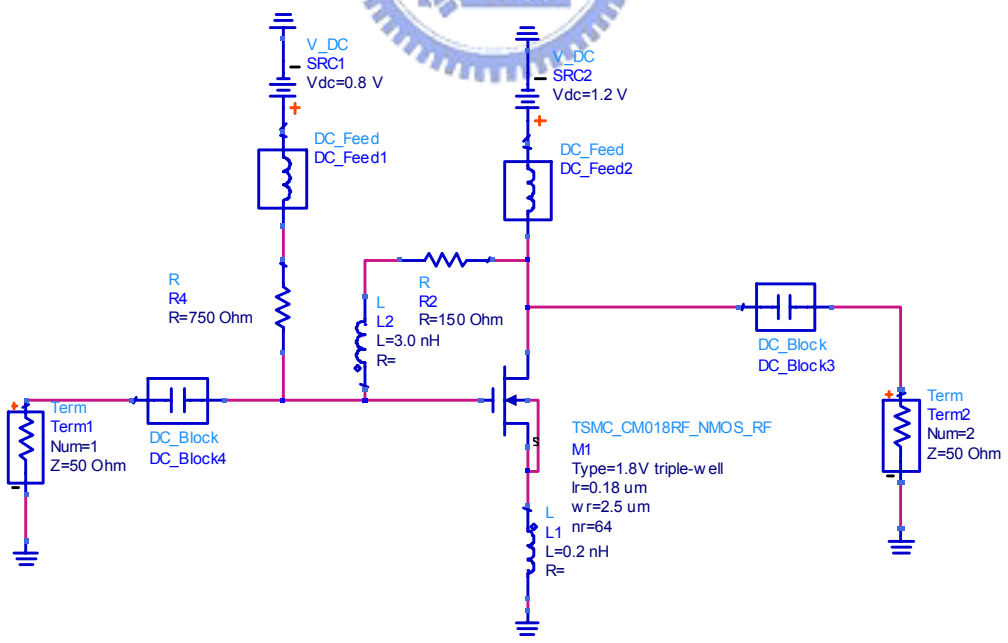


Figure4.7: A source degeneration amplifier with inductor-resistor feedback

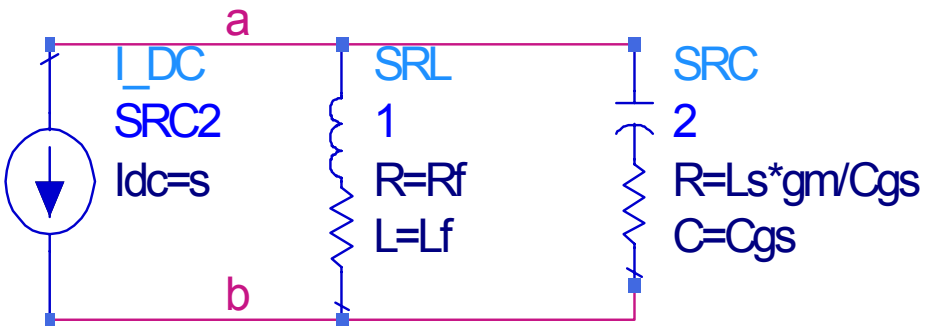


Figure4.8: The equivalent circuit of a source degeneration amplifier with inductor-resistor feedback

4.2.3 Gain flatness of amplifier with inductor-resistor feedback

This is the measurement of uniformity of the gain across the wide frequency range of interest. This parameter commonly used for wideband systems can impact pulse distortion in impulse-based UWB. It is desired that the gain be flat over the frequency band, typically a tolerance of ±0.5 dB.

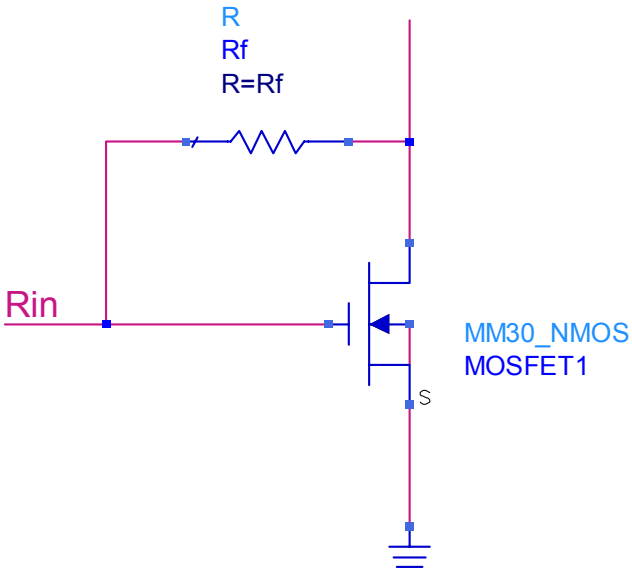


Figure4.9: NMOS with resistor feedback

Typically, it is to use a shunt feedback network, as shown at Figure 4-9, usually contains a resistor [34]. The resistor feedback can be design in such a way that it can provide the require match at both the input and output ends. Figure 4-10 show the characteristic of resistor feedback. Clearly, the low frequency gain drops due to small feedback resistor, and large feedback resistor provide good gain but have large gain variation. Since input impedance is usually on 50Ω, small resistor can get better matching. Therefore, good matching should due to low gain but flatness.

We use inductor-resistor feedback to improve the gain at matching consideration. Inductor-resistor feedback impedance can be written as:

$$Z_f = Rf + X_{Lf} = Rf + j\omega Lf \ , \qquad (4\text{-}8)$$

from (4-8), it is clear that Zf is small at low frequency and increase with the frequency raise. Therefore, the high frequency gain can slight increase. By cascading two stages, it should get flatness over the wide bandwidth. The concept is shown at Figure 4-11.

Inductor-resistor feedback improves the gain flatness and input matching, and make engineer easy to design a wideband amplifier.

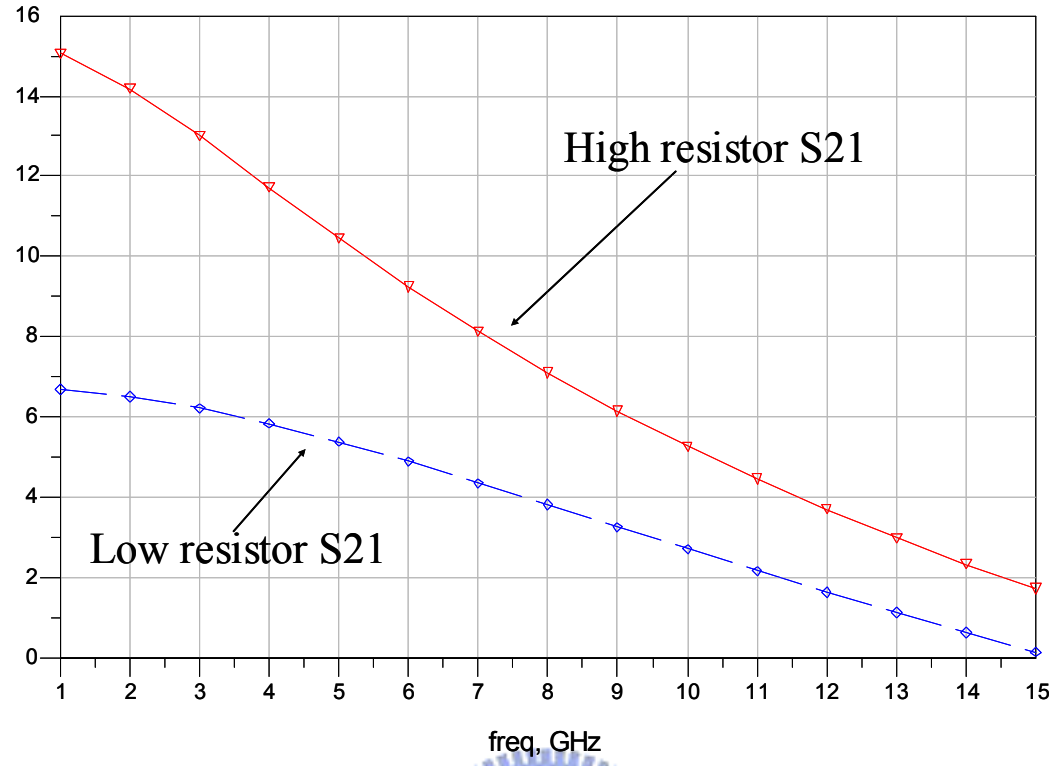


Figure4.10: Gain characteristic of resistor feedback

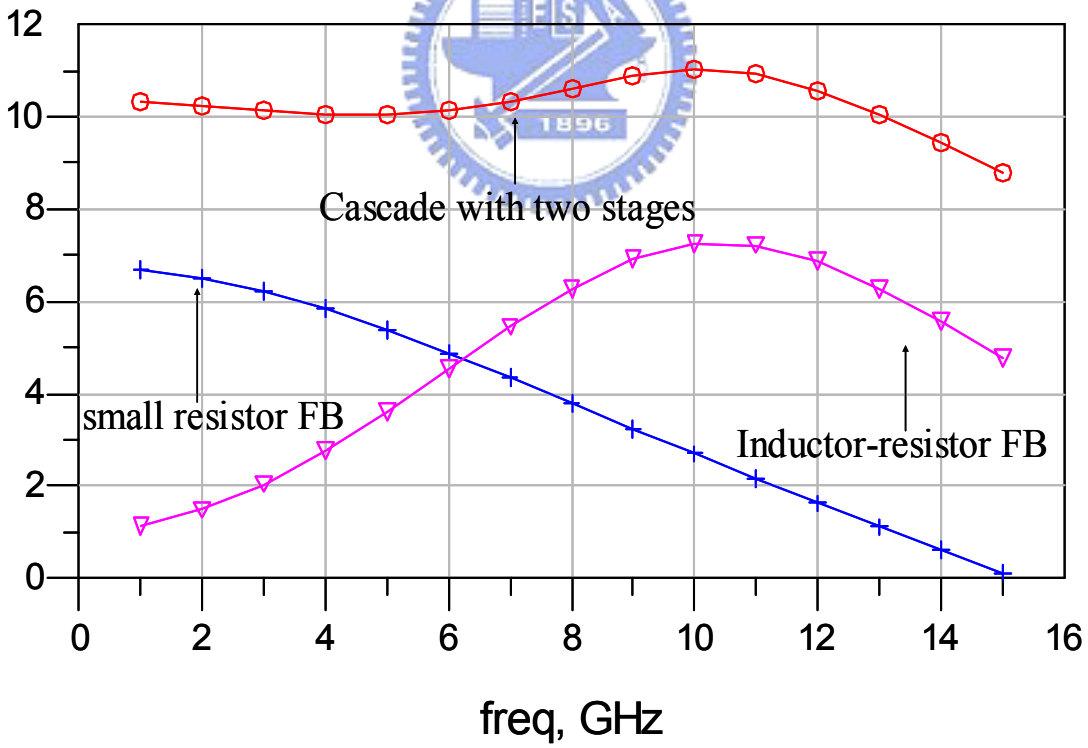


Figure4.11: Gain flatness of cascading two feedback

4.2.4 Output matching with inductor-resistor feedback

Output matching networks are also a problem to UWB PA. Since, antenna connect to the output of PA, the matching networks of PA must transfer to 50Ω for wideband. As the components of matching network are increasing, the parasitic effects are also increasing. This comes some bad performance, such as power loss and efficiency down, and increase the output noise.

In this work, we simplify output matching network by load-line theorem. The basic concept is selecting an optimum device it has optimum output load at 50Ω. By simulation of I-V curve, inductor-resistor feedback configuration also has good performance.

4.3 Simulation of Power Amplifier for UWB application

We start to design a two stage power amplifier, typical design flow is shown on Figure 3.5. The simulation tools are ADS, which can supports load-pull and large signal simulation. TSMC 0.18μm process is used in this work, and small signal model and large signal model are supported by TSMC. Now, begin to design a power amplifier by following steps.

1. **Simulation of output stage without feedback**

   We start to design output stage with I-V curve simulation. And decide the NMOS sizes and bias voltage to insure that the optimum output power delivered to load is 50Ω and the output power proper to the design goal.

2. Simulation of wideband matching with inductor-resistor feedback

According to the (4-5), we first decide Ls by setting $\omega_T Ls$=50, then use (4-6), (4-7) to decide the feedback inductor L2. Since, the feedback resistor also be set to 50Ω, the gain could be low, we need to tune the value of inductor and resistor to optimum the gain flatness and wideband matching with 50Ω.

3. Simulation of output stage with inductor-resistor feedback

After step1 and step2, we return to I-V curve simulation with inductor-resistor feedback, and insure that the optimum output power delivered to load is 50Ω and the output power proper to the design goal. If the performance is not good, we can tune the value of resistor or inductor and return to step2, otherwise retune to step1 and select a new device sizes or bias voltage.

4. Simulation of gain flatness with cascading two stage

Two stage power amplifier is popular, because it increases the total gain and isolation, engineers are easy to design output matching network and input matching network, however, inter-stage matching network become a issue. In this work, we tuned the first stage to insure input matching at 50Ω, and slightly increase the gain by inter-stage matching. the total gain variation from 3~10GHz is 4dB.

5. Design the bias circuit

We use the resister to bias the gate voltage, it increases stability of circuit but resister value variation by process must be considered. We use the RF choke at output drain, RF choke is typical a large value inductor. On the condition of this work, we use bias-tee instead of a large value inductor. On the DC supply nodes that no signal translates, we shunt a capacitance to filer out high frequency noise and insure AC ground. It is noted that wideband RF choke is a problem of design, large inductor value changes with frequency and the same with Q value.

4.4 Simulation results of UWB power amplifier

- Figure 4-12 shows that schematic and simulation result of I-V curve, the optimum load is 42Ω.and the fingers number of NMOS are 64. Output power at this bias is 8.8dBm.DC-to-RF efficiency is 40%, and optimum VDS is 1.0V, DC current 18.8mA.

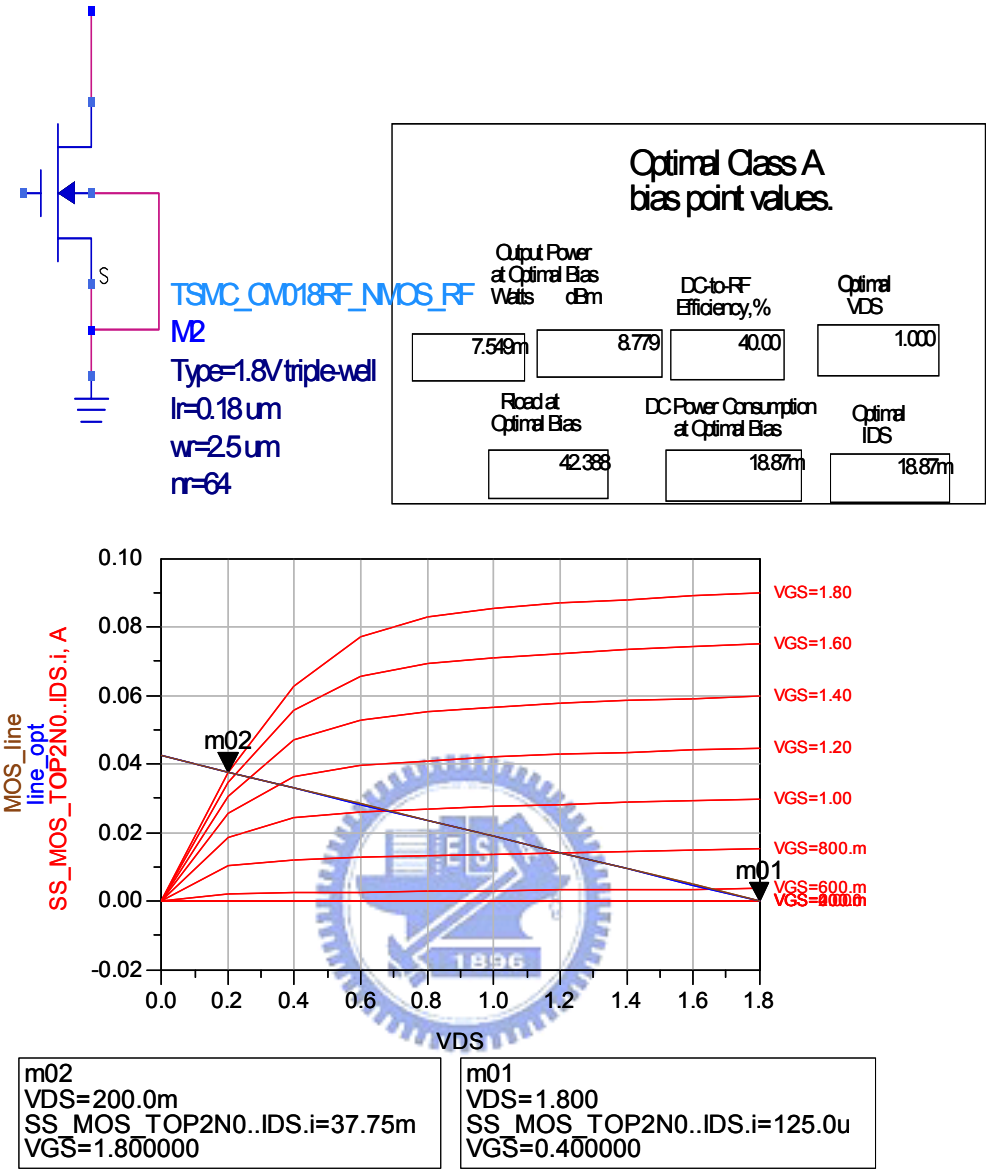


Figure4.12: Schematic and simulation result of I-V curve

➢ Figure 4-13 shows the input impedance of a source degeneration amplifier compare to equivalent circuits. The source inductor is 0.2nH with calculation by (4-5).

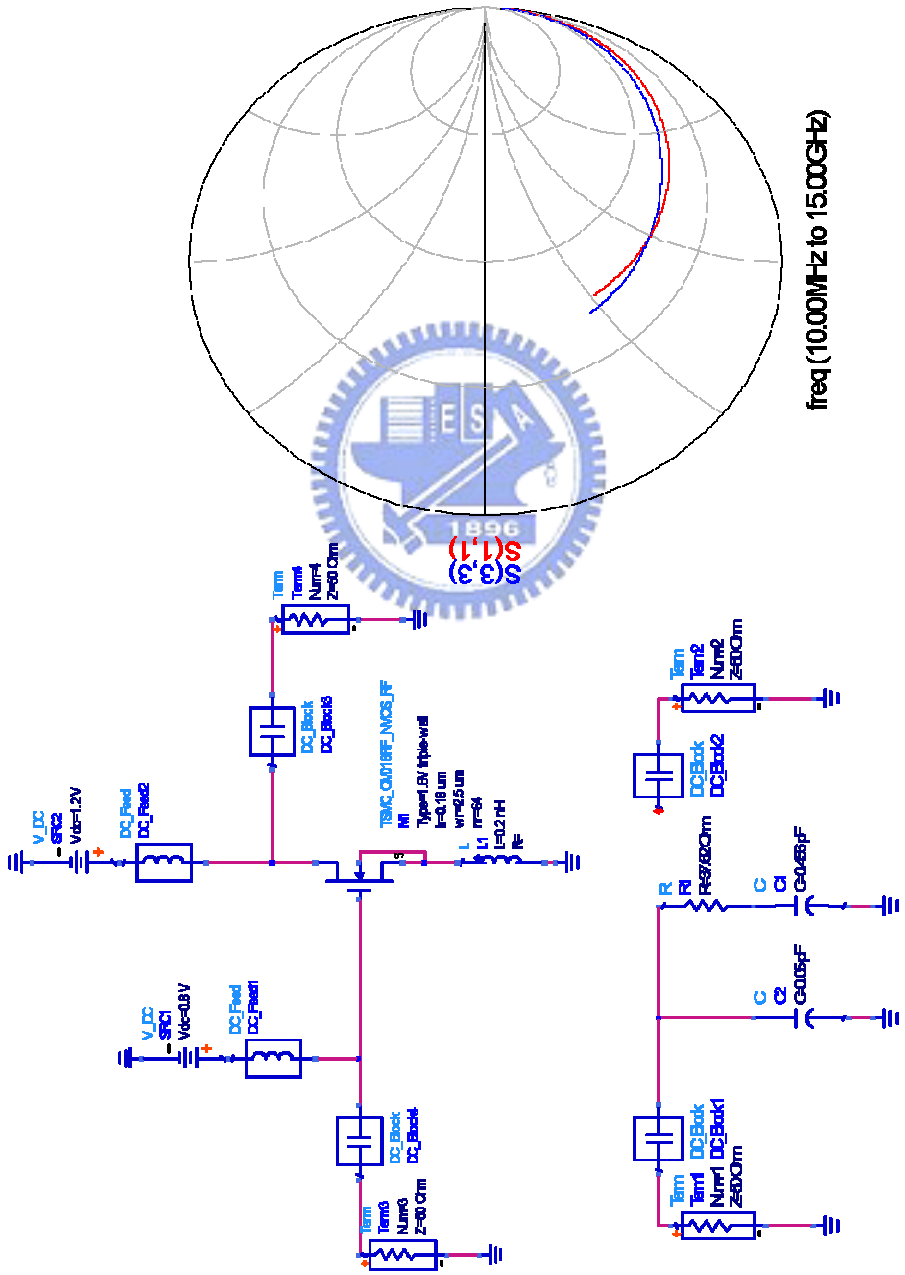


Figure4.13: Simulation of input impedance of a source degeneration amplifier

➢ Figure 4-14 shows the input impedance of inductor-resistor feedback amplifier compare to equivalent circuits, the feedback inductor is 3nH and resister is 150Ω.

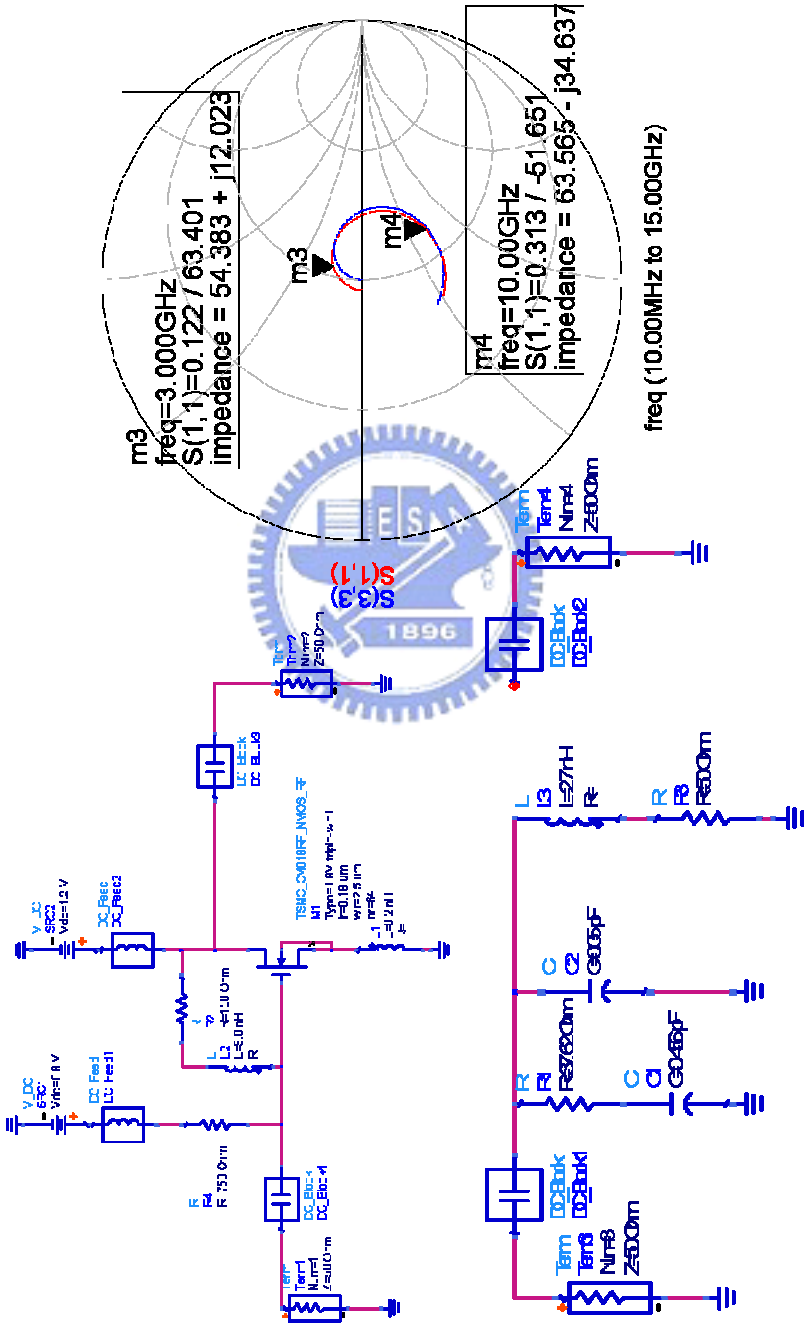


Figure4.14: Input impedance of inductor-resistor feedback amplifier compare to equivalent

➢ Figure 4.15 shows the gain and stability simulations of single stage inductor-resister feedback amplifier. From 3~10GHz, the gain variation is less than 1dB and stability from 0~15GHz.

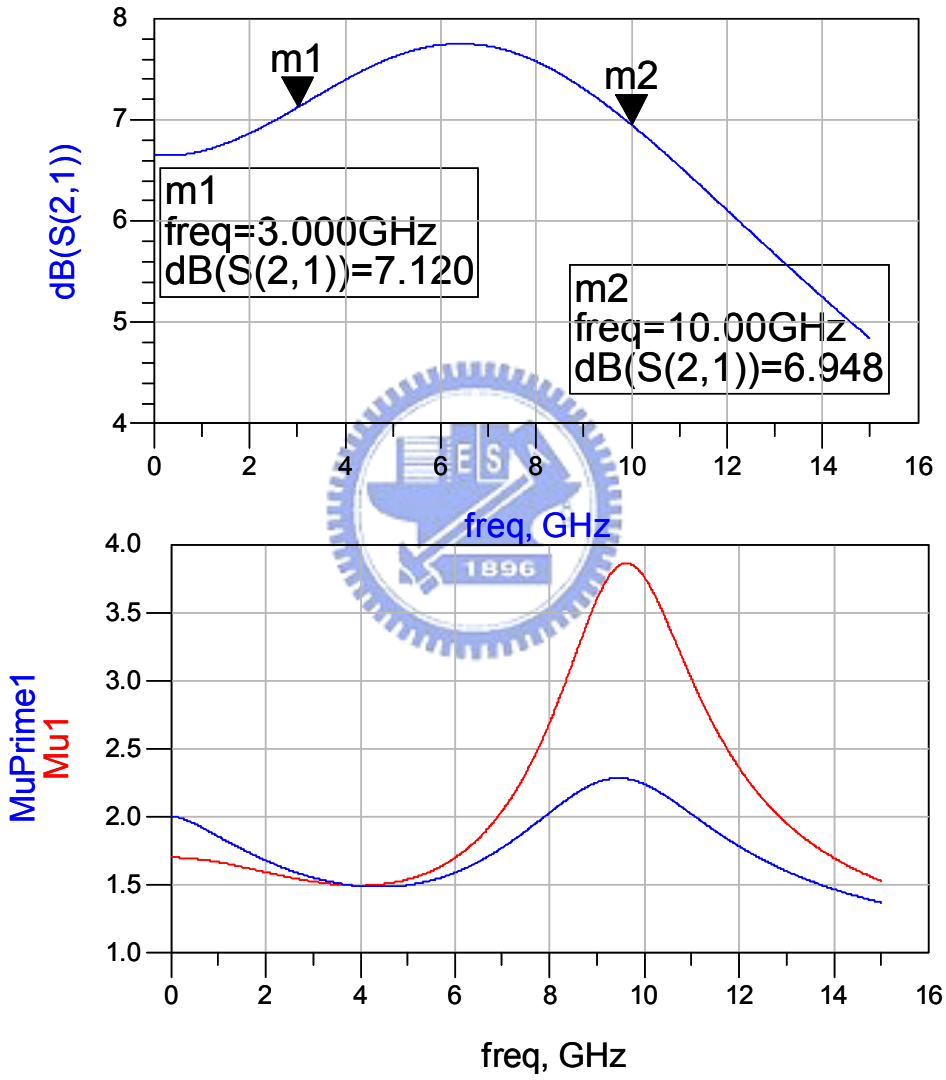


Figure4.15: The gain and stability simulations of single stage inductor-resister feedback amplifier

➢ Figure 4.16 shows the schematic and simulation result of I-V curve with inductor-resistor feedback. The optimum load is 50Ω.and the fingers number of NMOS are 64. Output power at this bias is 7.5dBm.DC-to-RF efficiency is 35%, and optimum VDS is 1.0V, DC current 15.0mA.

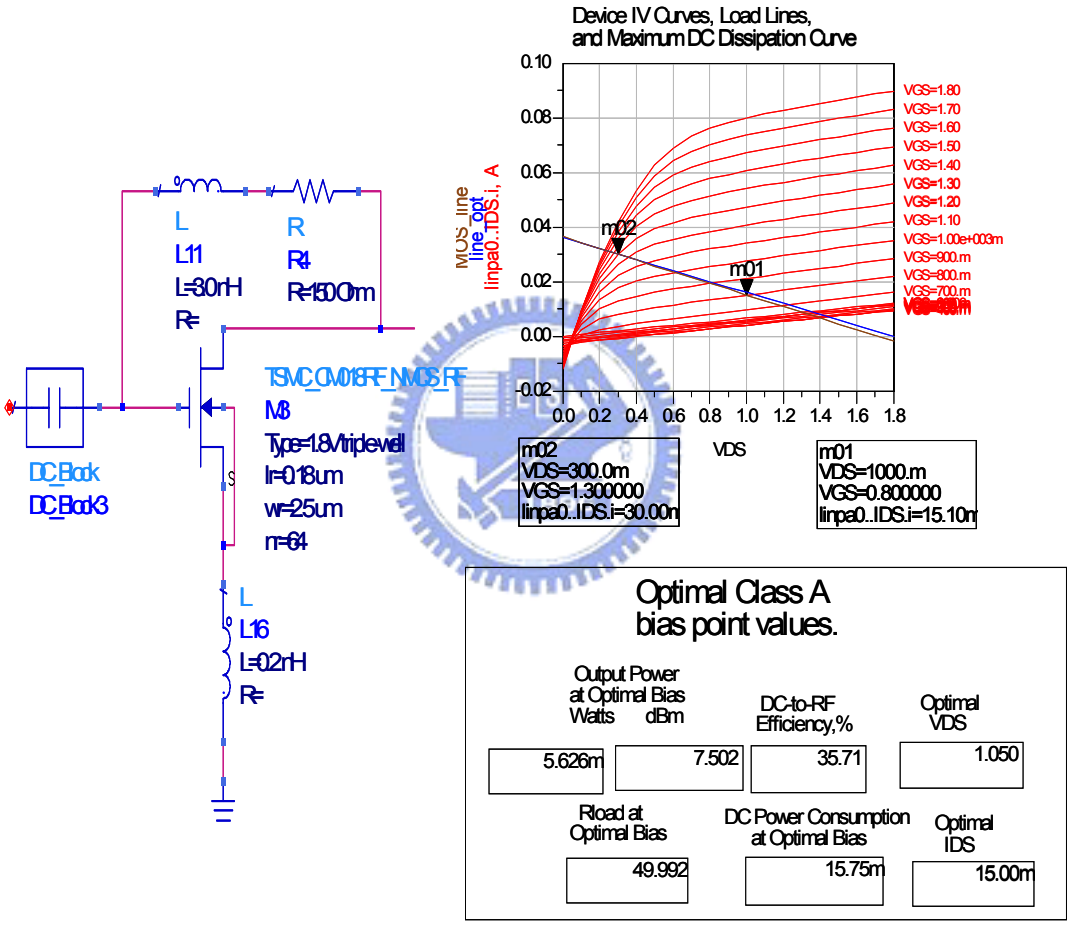


Figure4.16: Schematic and simulation result of I-V curve with inductor-resistor feedback.

➢ Figure 4.17 shows the schematic of the two stage amplifier. Inter-stage used L-C series tank that slightly increase total gain. The second stage bias with resistor to increase the stability of circuits. Output used a 10pF large capacitance to deliver signals without influencing matching.

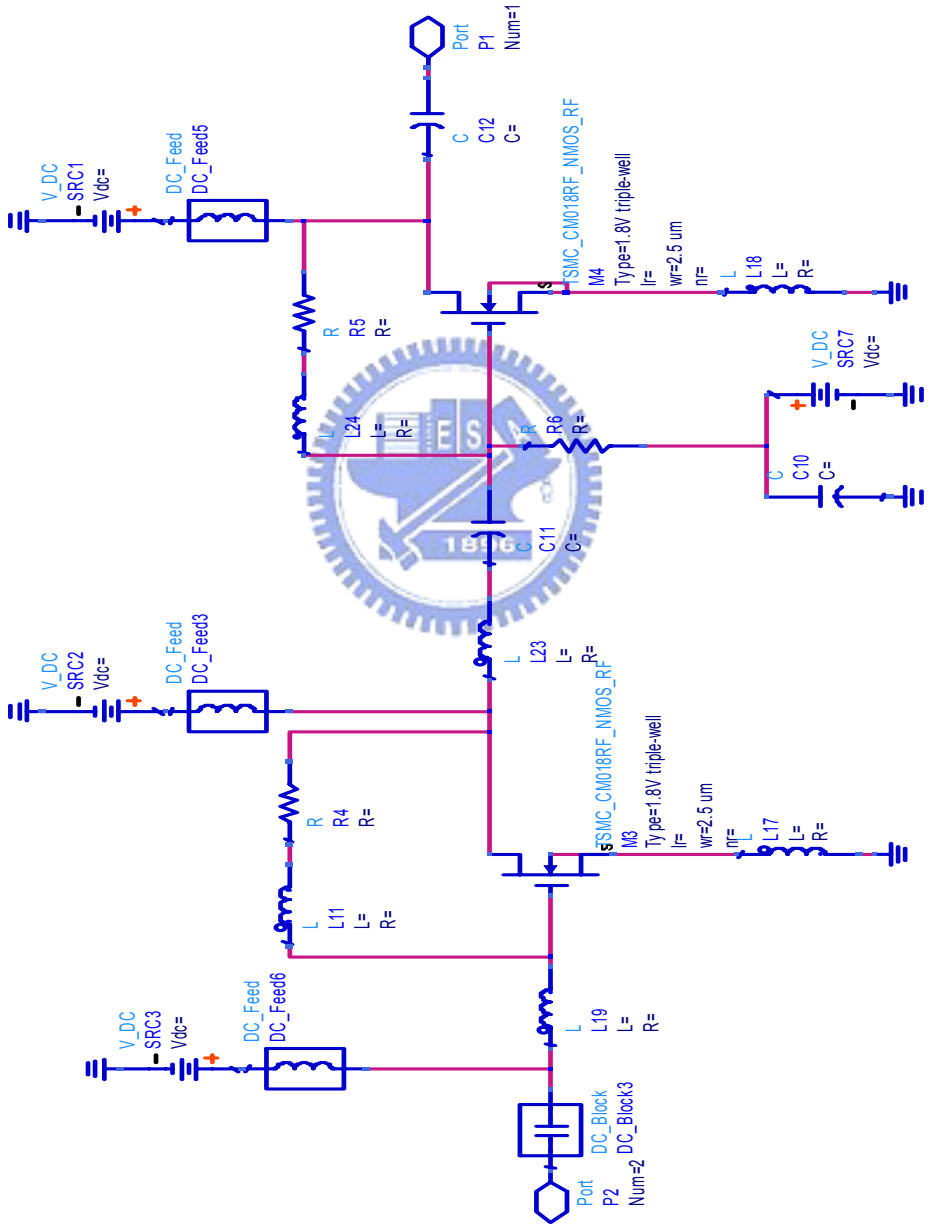


Figure4.17: Schematic of the two stage inductor-resistor feedback amplifier.

➢ Figure 4.18 shows the simulation of second stage with resistor FB compare to inductor-resistor FB. The gain of inductor-resistor feedback is flatter than resistor feedback and S22 of inductor-resistor is better than resistor feedback.

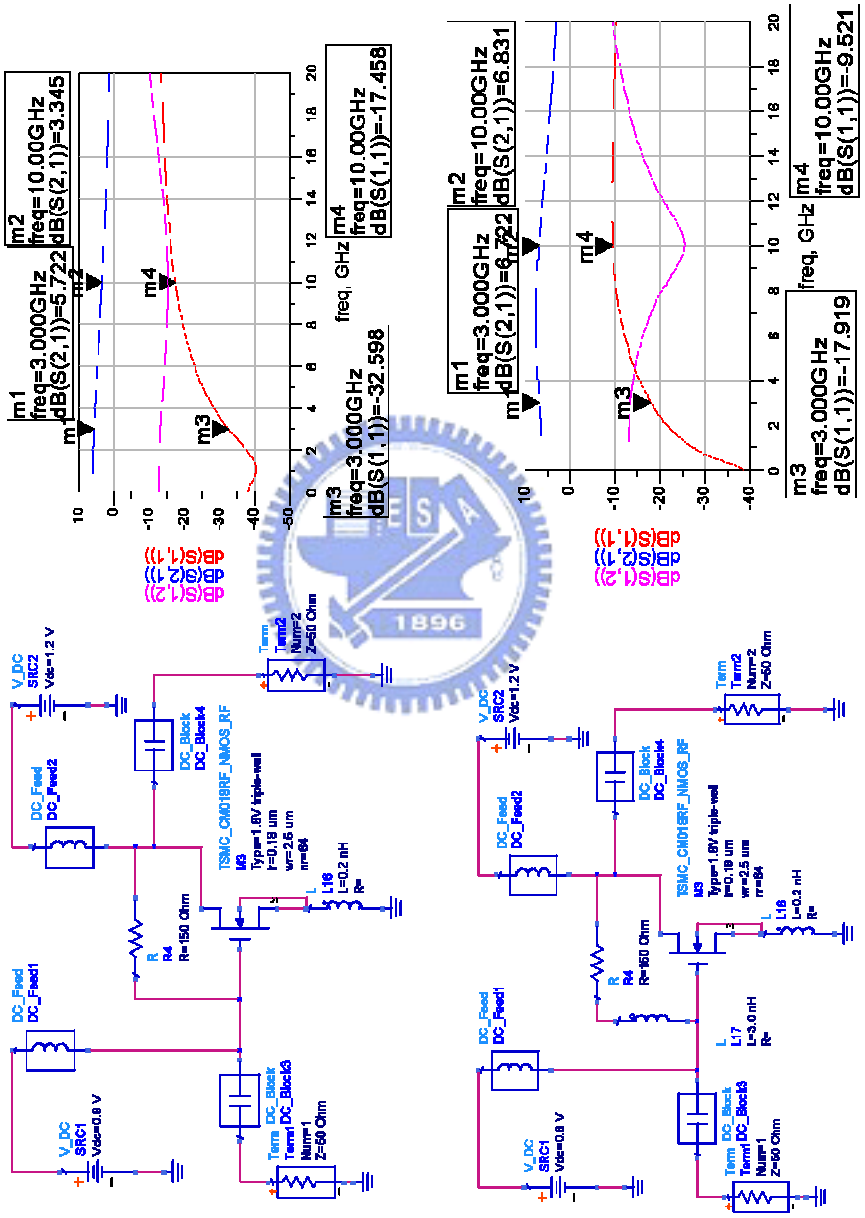


Figure4.18: Simulation of second stage with resistor feedback compare to inductor-resistor feedback

➢ Figure 4.19 shows the simulation of first stage with resistor FB compare to inductor-resistor FB. There are small different between inductor-resistor and resistor feedback because of small inductor.

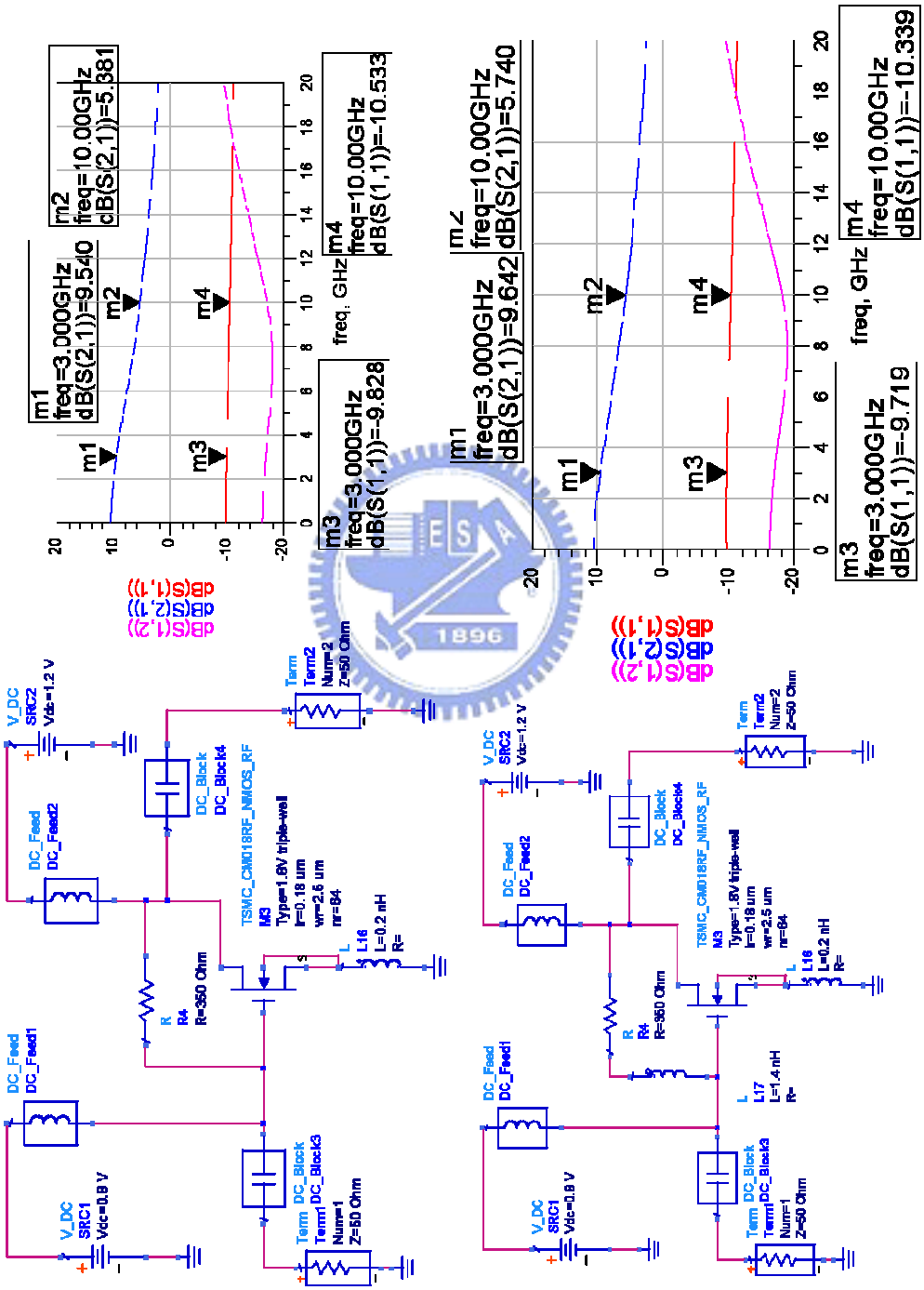


Figure 4.19: Simulation of first stage with resistor feedback compare to inductor-resistor feedback.

➢ Figure 4.20 shows the simulation of inter-stage stability. The stability of two stage from 0~10GHz.

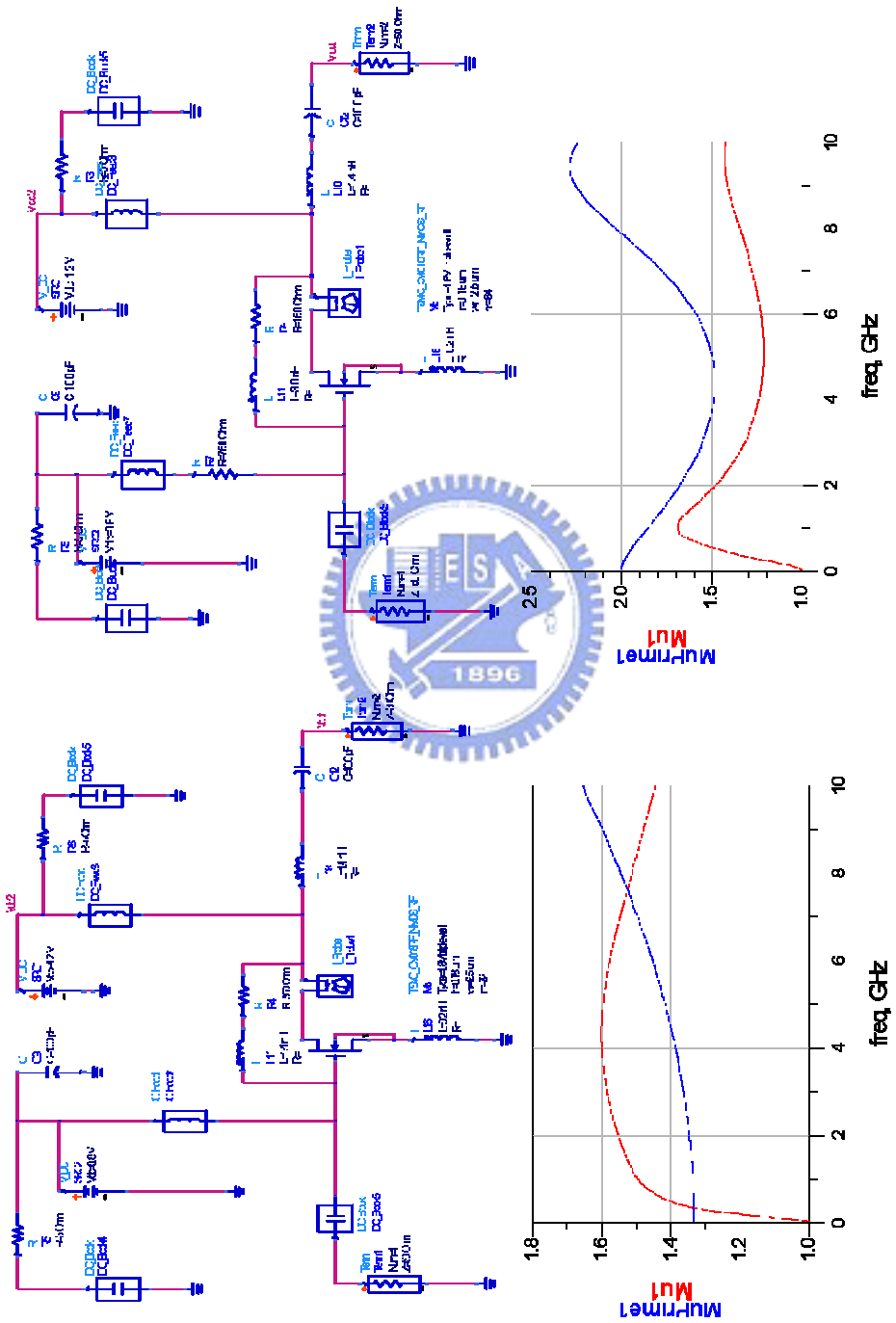


Figure4.20: Simulation of inter-stage stability

➢ Figure 4.21 shows the stability simulation from 0~20GHz of two stage inductor-resistor FB amplifier with μ value.

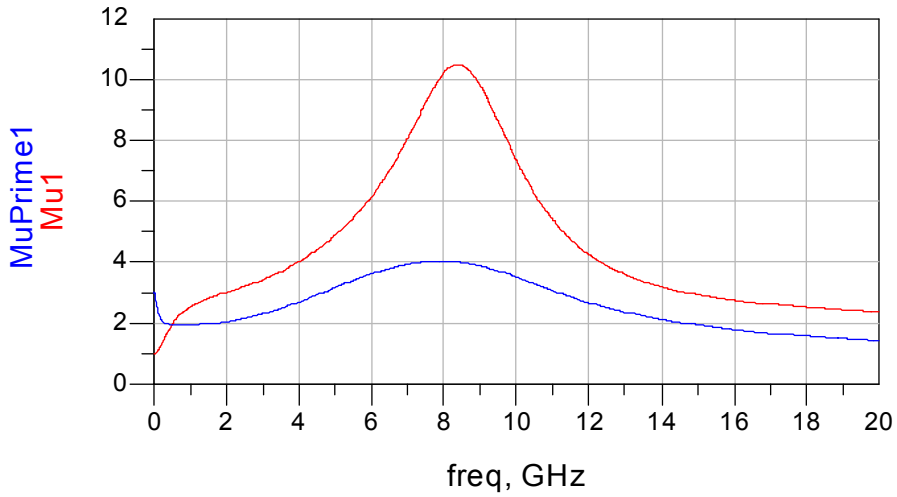


Figure4.21: Stability simulation from 0~20GHz of UWB power amplifier

➢ Figure 4.22 shows the S parameters simulation of two stage inductor-resistor FB amplifier.

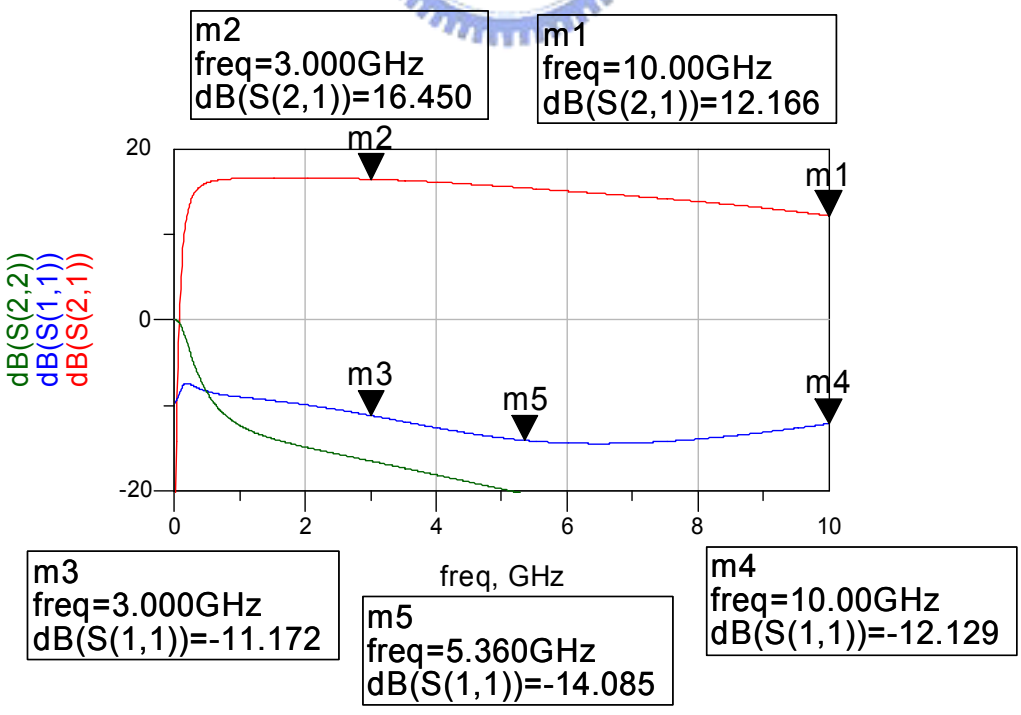


Figure4.22: S parameters simulation of UWB power amplifier

➢ Figure 4.23 shows the power gain and PAE simulation of two stage inductor-resistor FB amplifier. The PAE is 13% over the 3~10GHz and power gain is not flatness comparing to the S21.

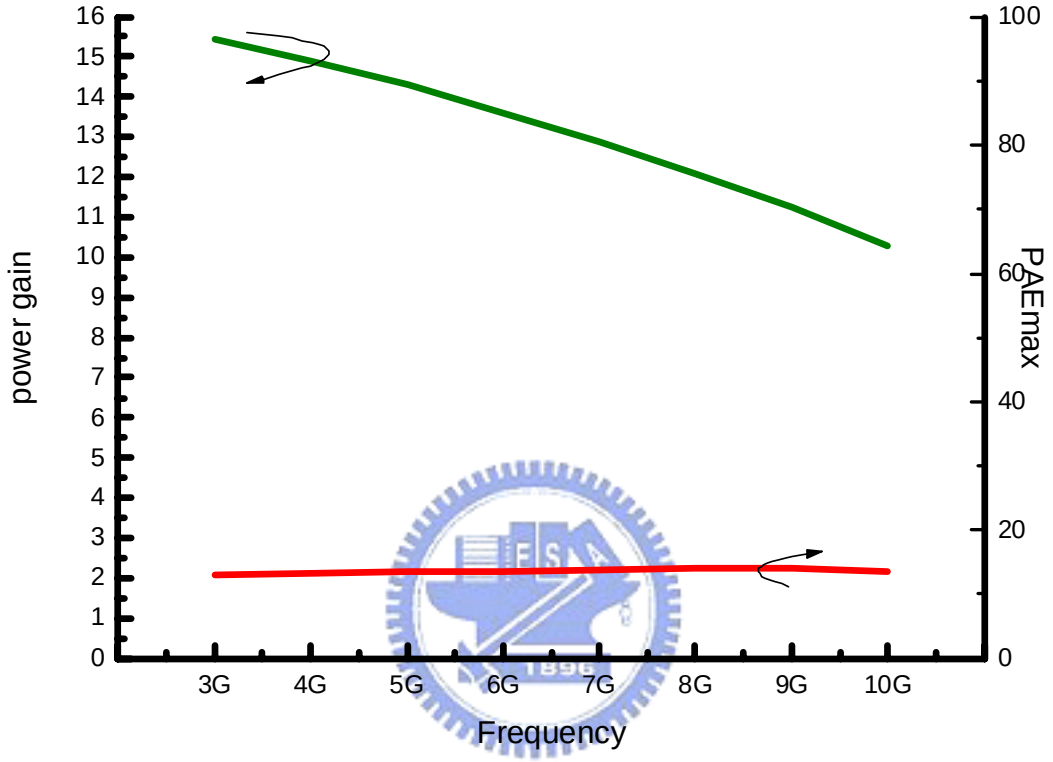


Figure4.23: Power gain and PAE simulation of UWB power amplifier

➢ Figure 4.24 shows the P1dB and IIP3 simulation of two stage inductor-resistor FB amplifiers. The IIP3 increase as the frequency rise and P1dB has a peak value at 7GHz.

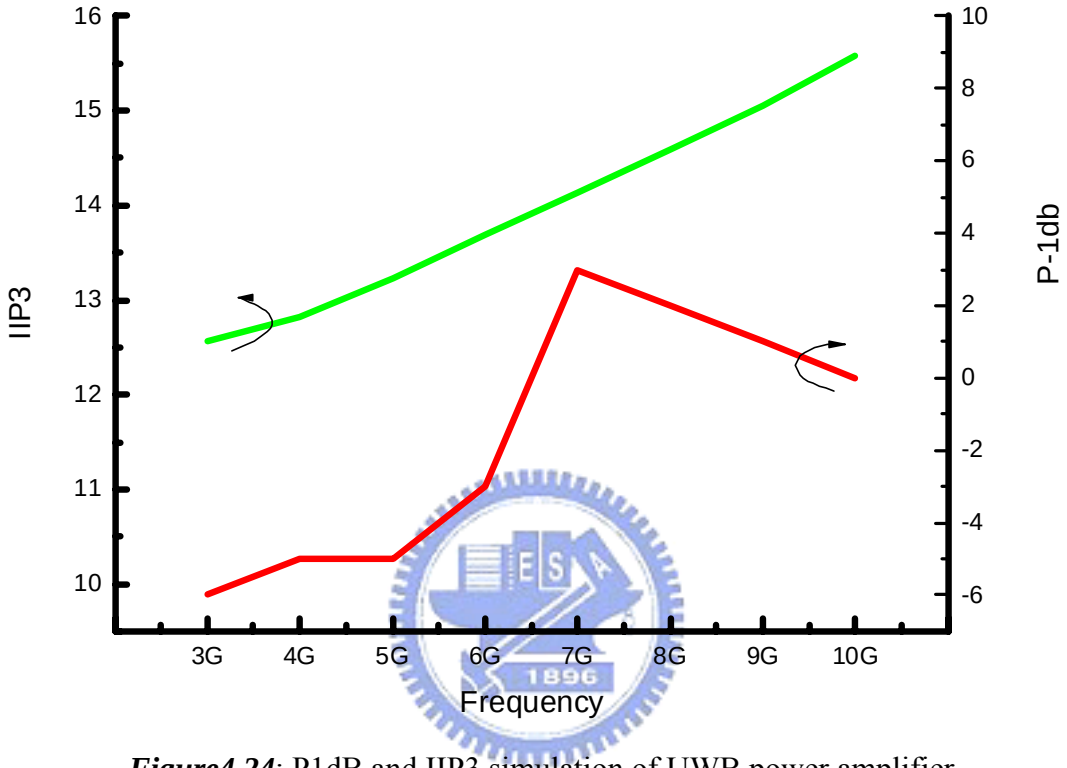


Figure4.24: P1dB and IIP3 simulation of UWB power amplifier

➢ Figure 4.25~Figure4.33 show the RF corner and temperate simulation of UWB power amplifier.

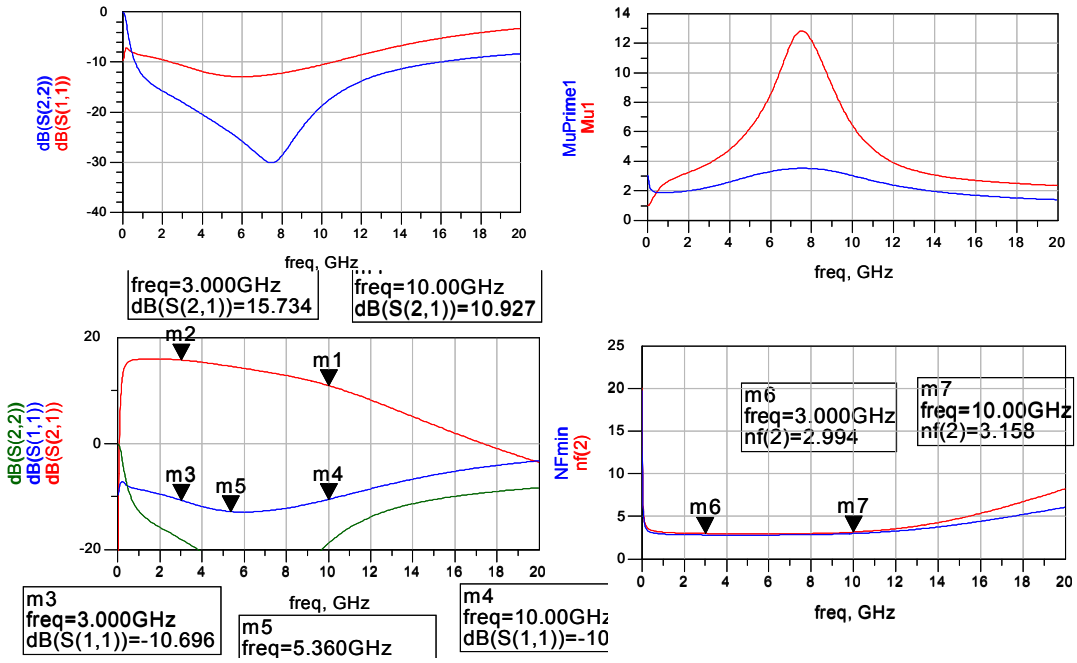


Figure4.25: RF corner SS at 16.8˚C simulation of UWB power amplifier

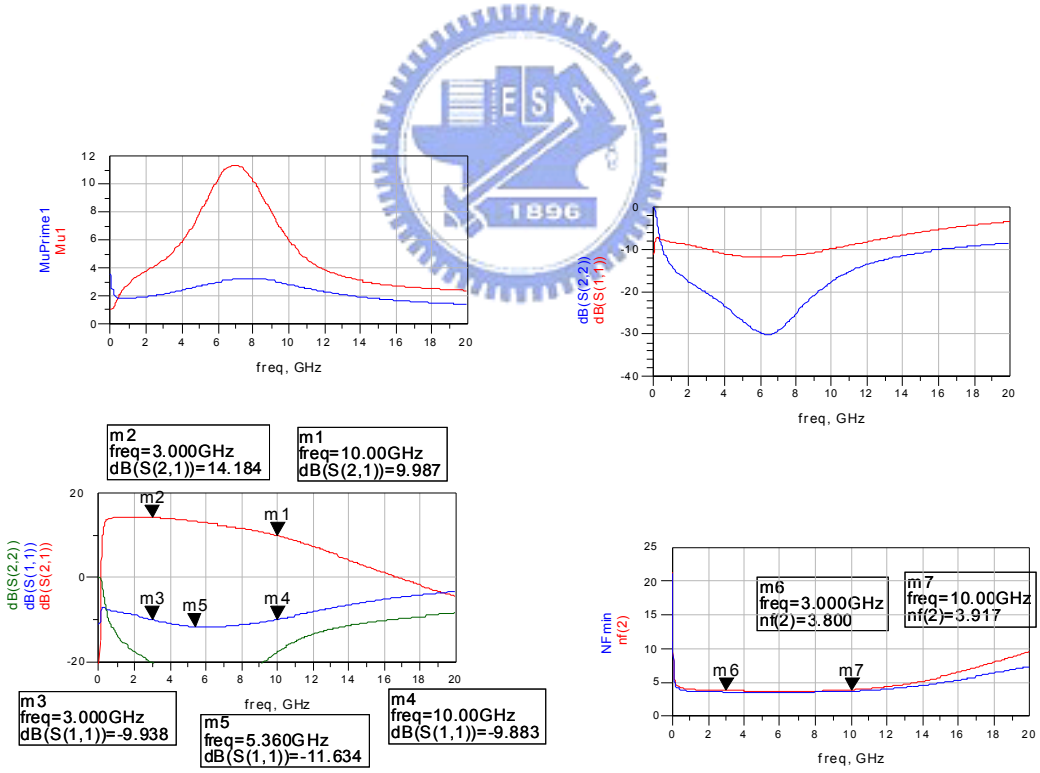


Figure4.26: RF corner-SS at 85˚C simulation of UWB power amplifier

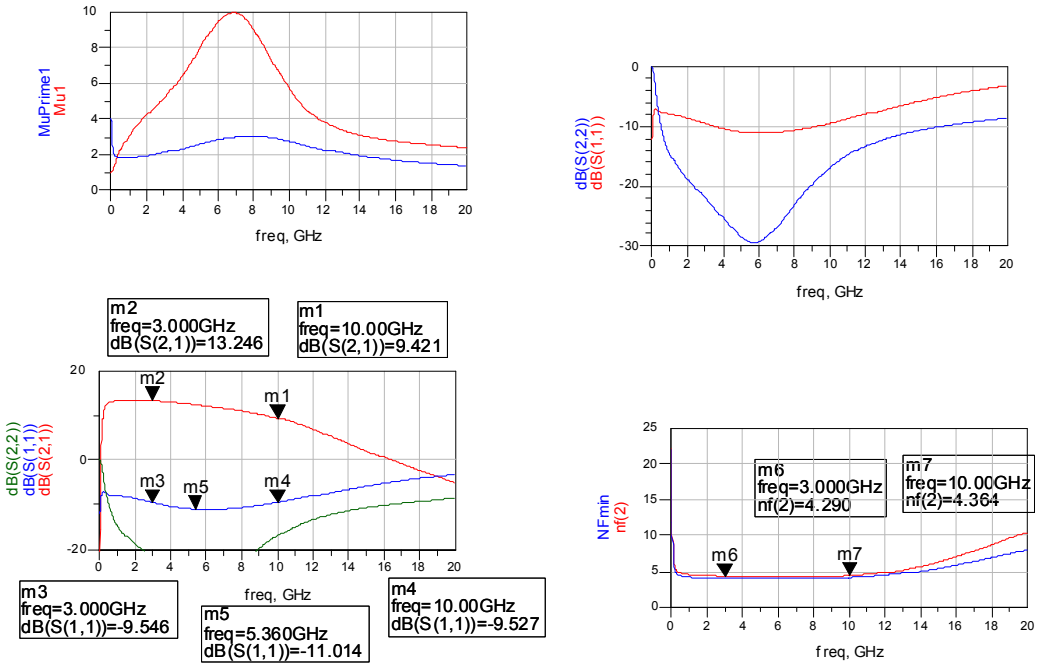


Figure4.27: RF corner-SS at 125.0˚C simulation of UWB power amplifier

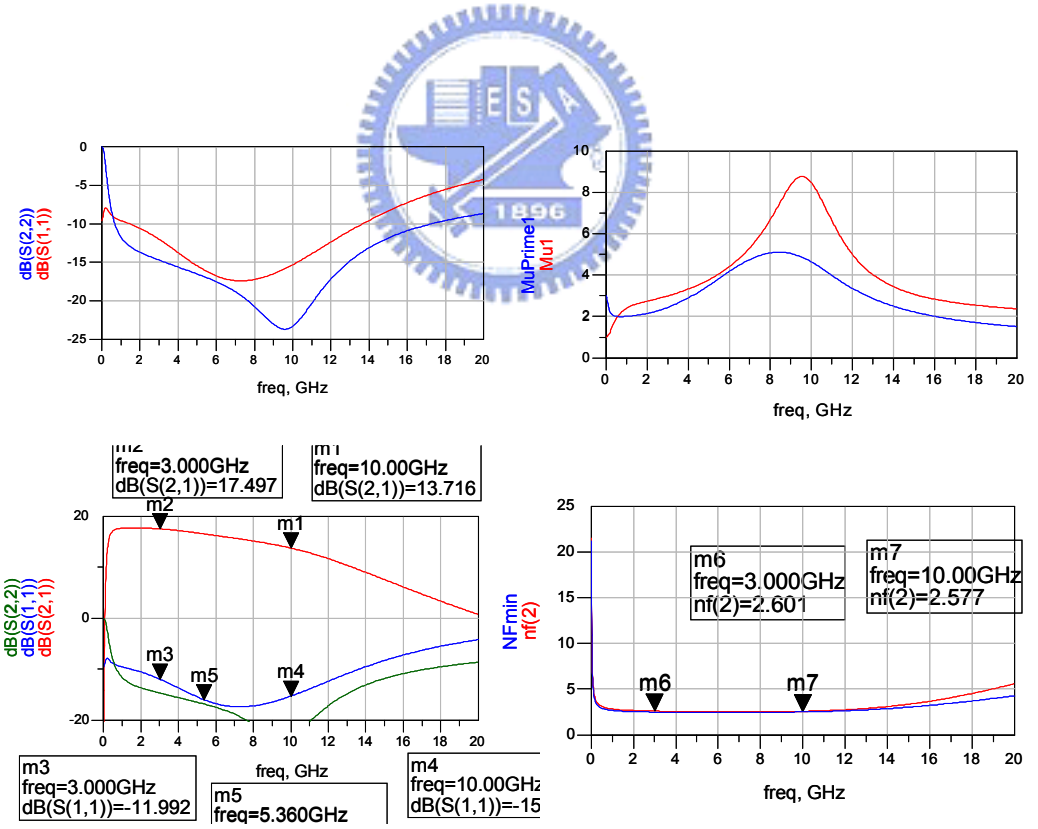


Figure4.28: RF corner-FF at 16.8˚C simulation of UWB power amplifier

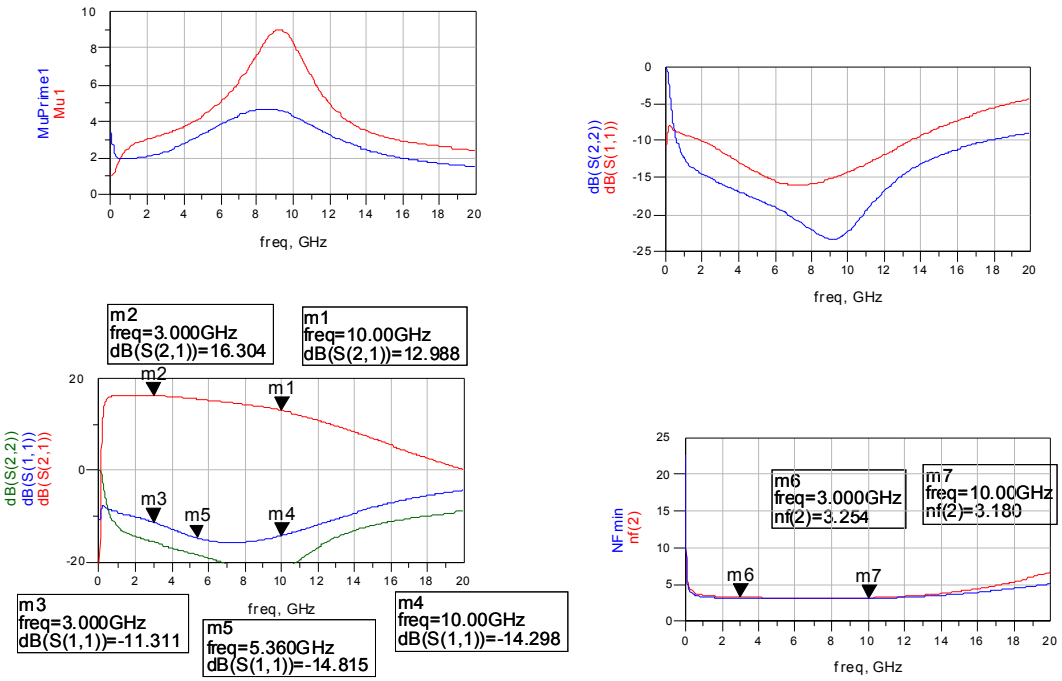


Figure4.29: RF corner-FF at 85.0°C simulation of UWB power amplifier

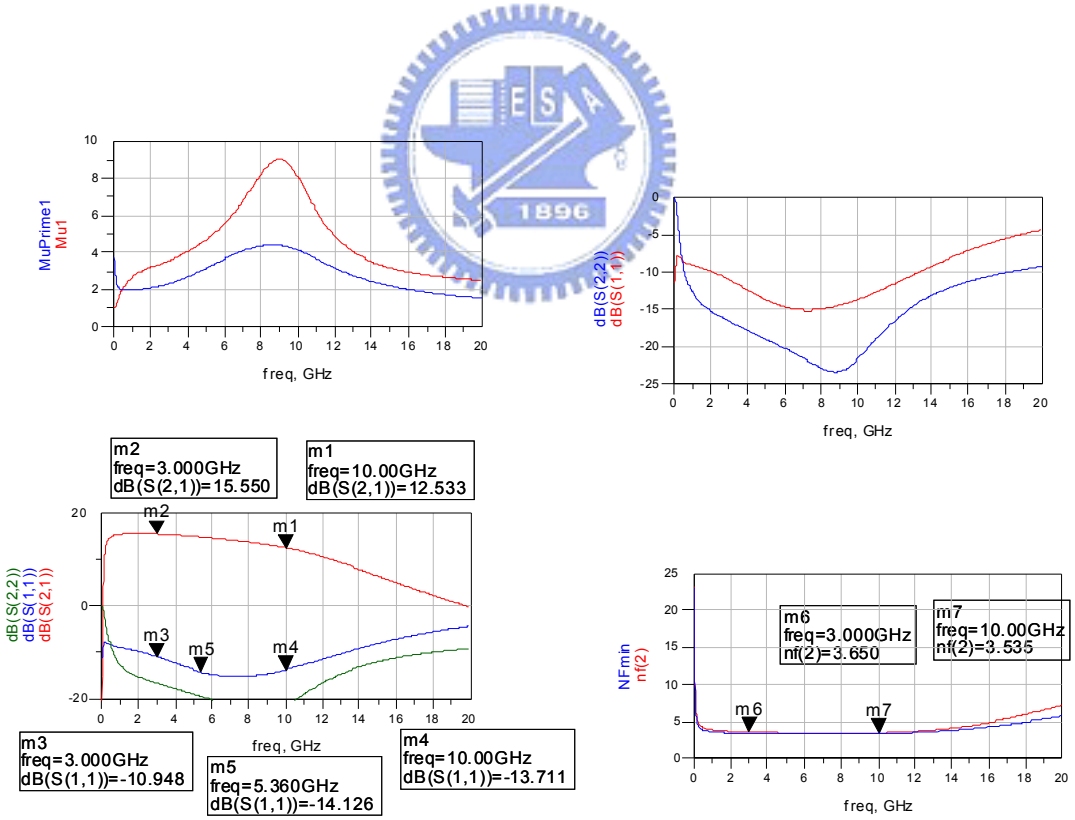


Figure4.30: RF corner-FF at 125.0°C simulation of UWB power amplifier

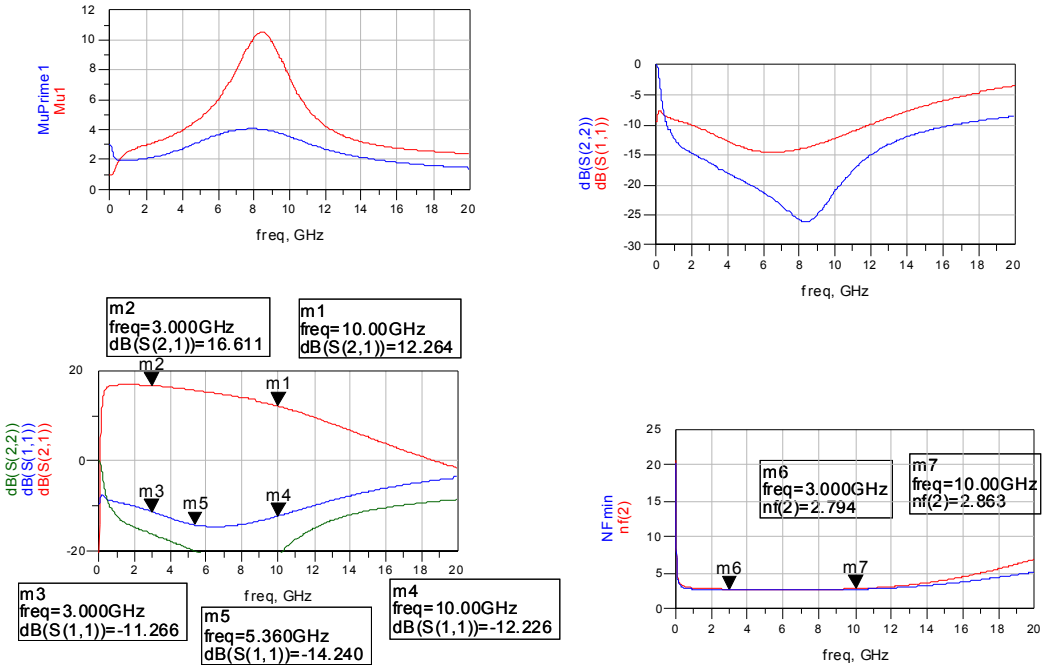


Figure4.31: RF corner-TT at 16.8°C simulation of UWB power amplifier

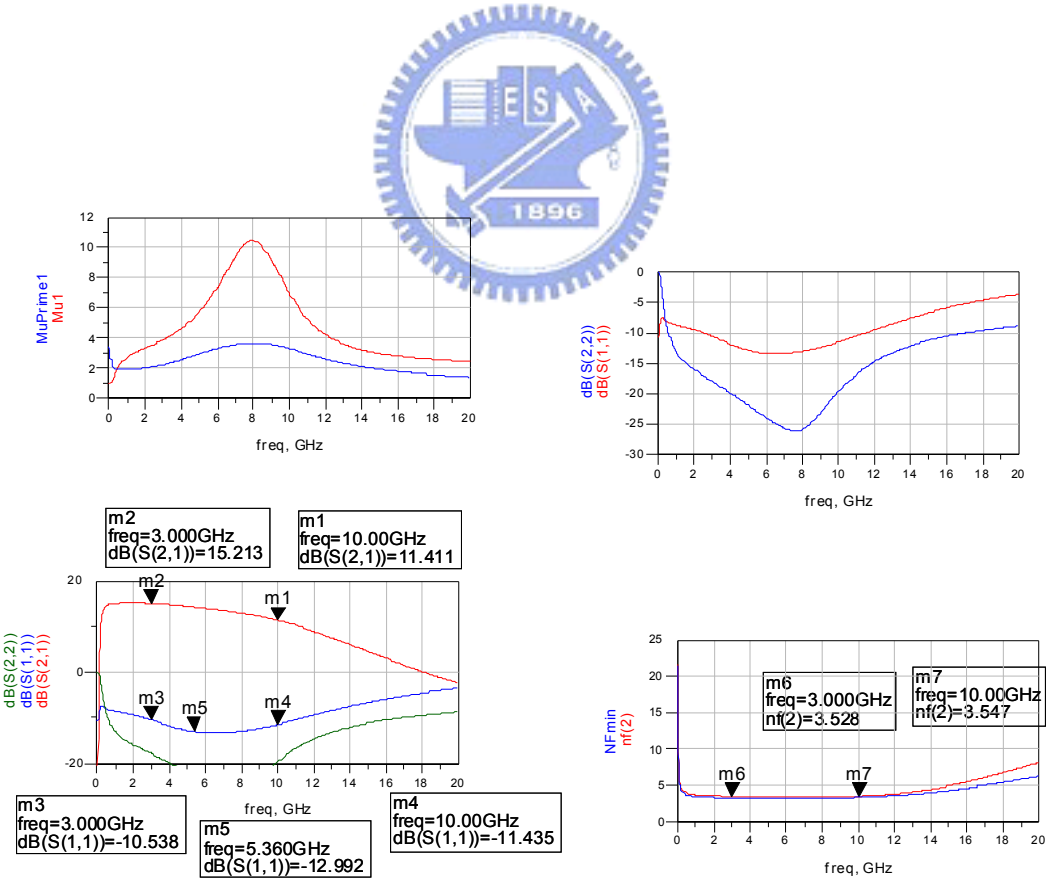


Figure4.32: RF corner-TT at 85.0°C simulation of UWB power amplifier

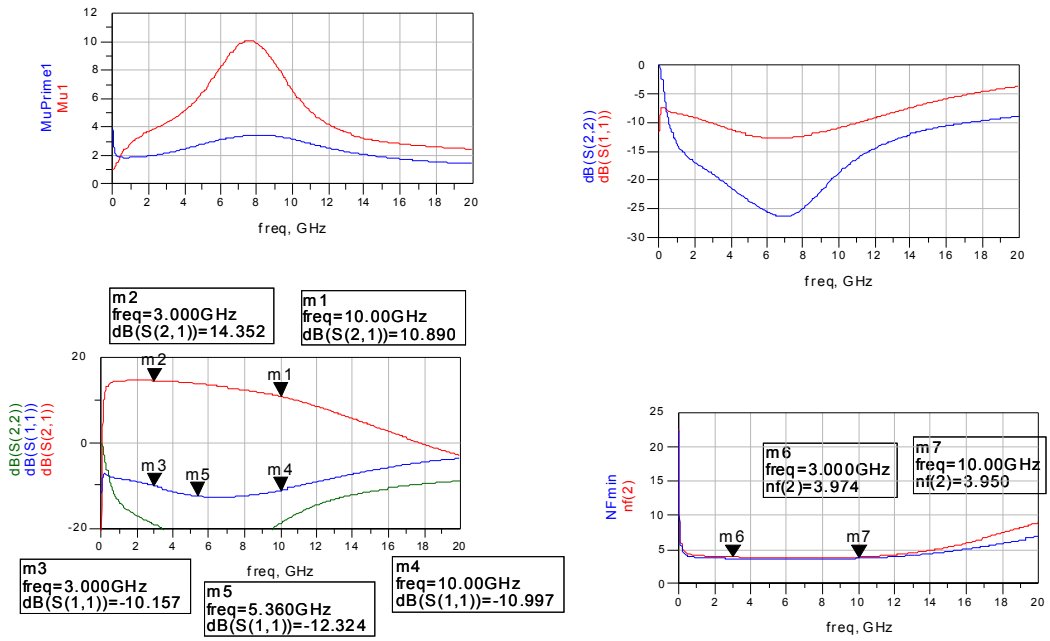


Figure4.33: RF corner-TT at 125.0°C simulation of UWB amplifier

➢ Figure 4.34 shows the resistor variation by +50% simulation of two stage inductor-resistor FB amplifier.

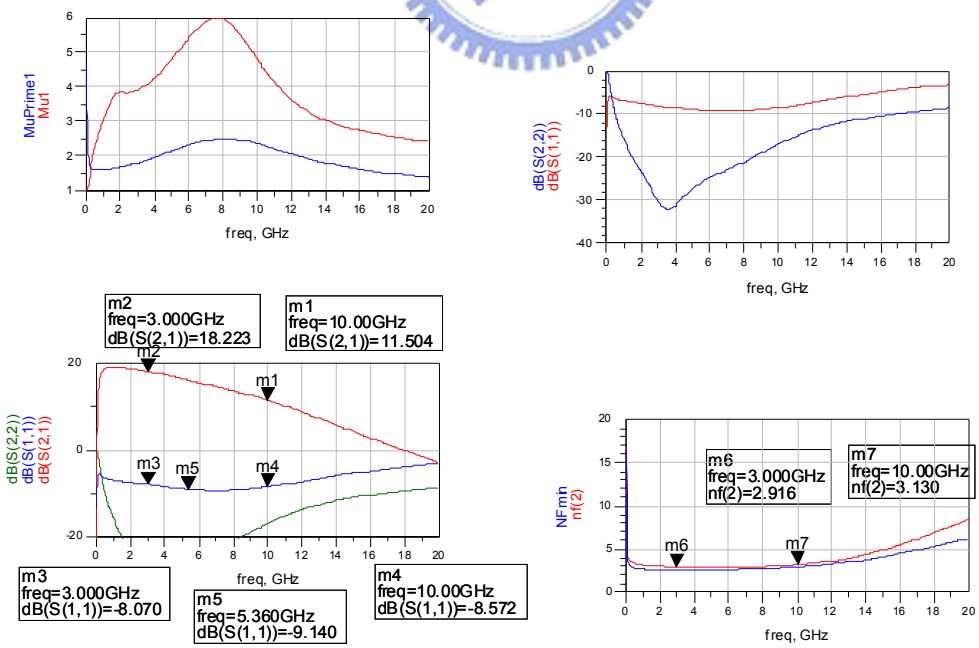


Figure4.34: resistor variation by +50% simulation of UWB power amplifier

➢ Figure 4.35 shows the resistor variation by -50% simulation of two stage inductor-resistor FB amplifier.

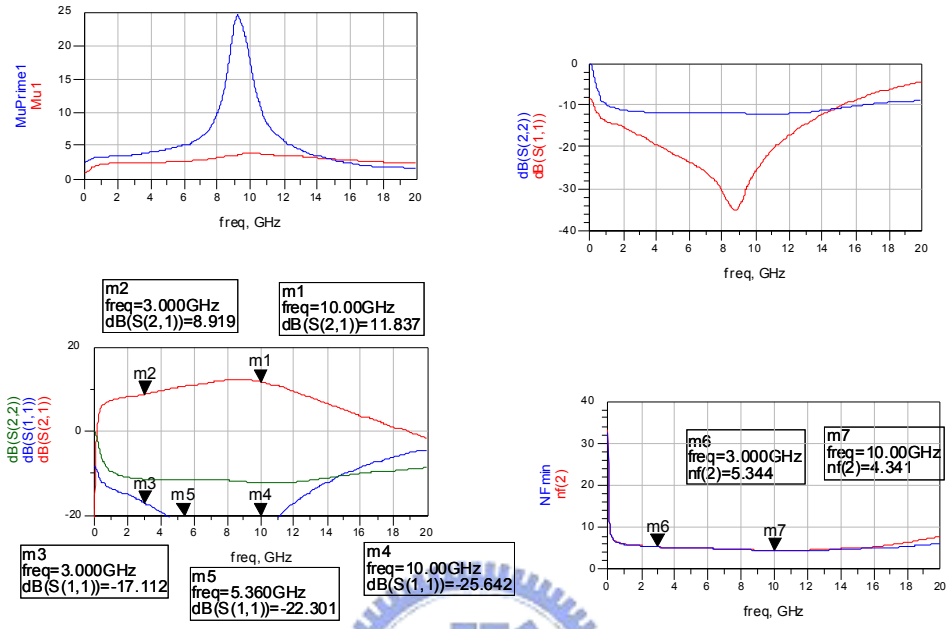


Figure4.35: resistor variation by -50% simulation of UWB power amplifier

Table4.2: The simulation specification of UWB power amplifier

B.W.(GHz)	Power Gain(dB)	P-1db(dBm)	IP3(dBm)	PAEmax(%)	Power consumption (mW)
3~10Ghz	15.15~10	-5~2~0	16.169~19.254	13.04~13.6	72~68

4.5 Layout and measurement consideration

The layout is shown in Figure 4.36, the total size occupied by the PA is 1.01x0.77 mm^2, The capacitance is used metal-insulator-metal (MIM) capacitance supported by TSMC, the resister is used with P+ w/o silicide resister supported by TSMC. Inductors is simulated by IE3D, the metal width is decided according to the capacity

of current flow and AC signal power. Input and output pads use GSG with 50Ω, and bias-tee is used on drain of each NMOS. Bias-tee replaces by the RF chock. Each NMOS are biased at the same voltage, vg is 0.8V and vd is 1.2V.

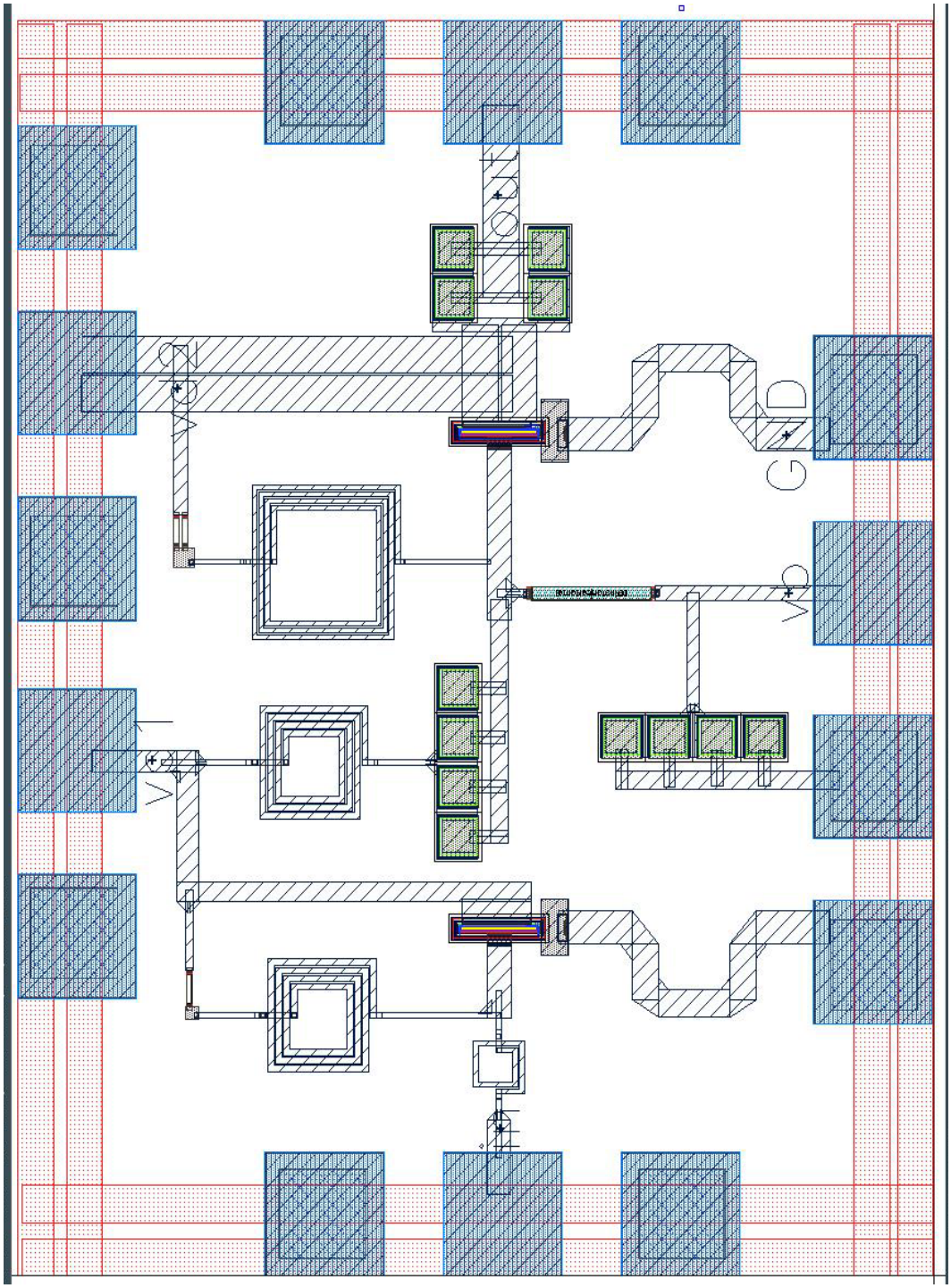


Figure4.36: layout of UWB PA

4.6 Experiment results

The measurement is in National Nano Device Laboratories (NDL), and used RFIC measurement system. RFIC measurement system include HP 8753D Network Analyzer, 8564E spectrum analyzer, HP 89441A Vector signal analyzer, HP6623A DC power supply and 3 automatic DC Bias. The measurement is shown at Figure 4.37, Figure 4.38, and Figure4.39. Figure 4.37 show the S parameter measurement of UWB PA, the S21 has 13dB at 3GHz but reduce as the frequency increase, the S11 is below the -10dB from 3~10 GHz, and the S22 is the same to S11 but have a peak at 9GHz. Figure 4.38 show the power gain and noise measurement of UWB PA, the power gain is the same with S21 in Figure4.37, and the noise figure is 4~7dB from 3~9GHz. beyond 9GHz, there is no gain and noise is rise. It is noted here we ignore the measurement results at 4.5GHz, it seen have some problem happened by something we had not take care.

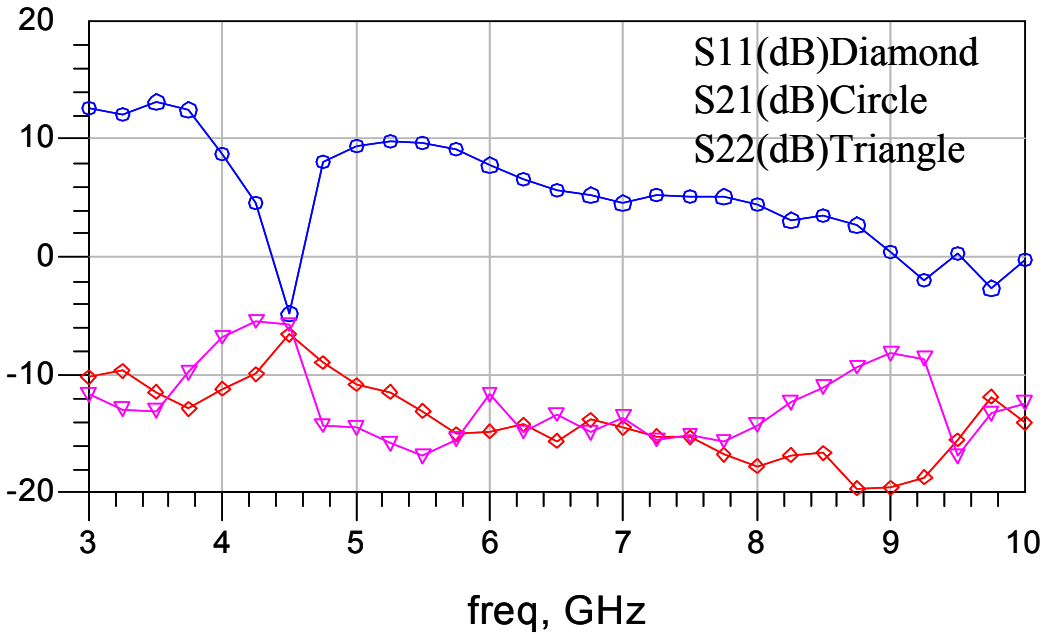


Figure4.37: S parameter measurement of UWB PA

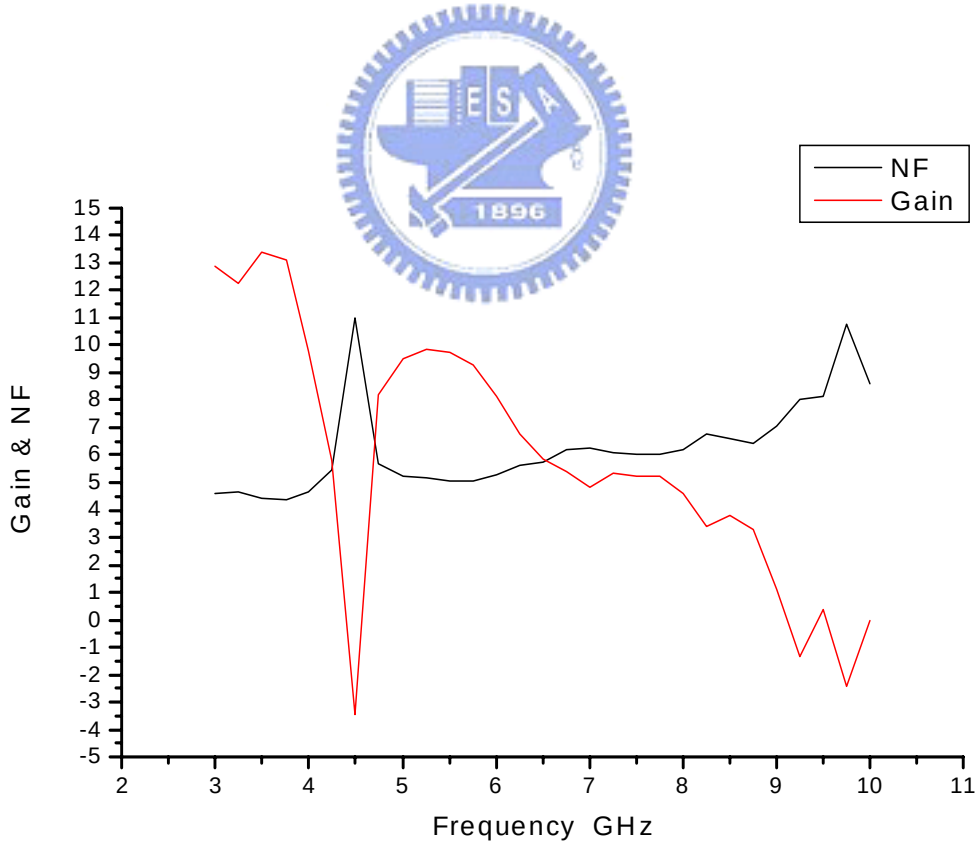


Figure4.38: power gain and NF measurement of UWB PA

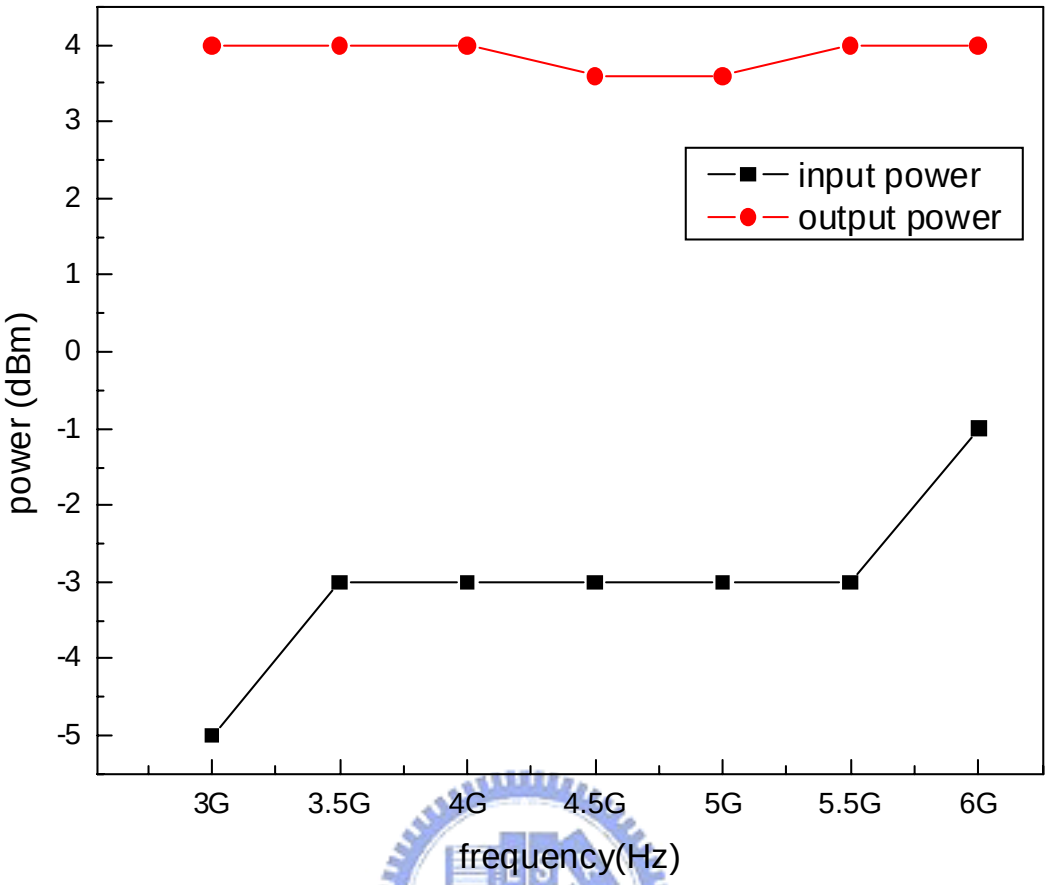


Figure4.39: P1dB measurement of UWB PA

Table4.3: Measurement compare to simulation of UWB power amplifier.

B.W.(GHz) 3~10GHz	Simulation	Measurement
Power Gain(dB)	**15.15~10**	**13~0**
P-1db(dBm)	**-5~2~0**	**4(3~6GHz)**
IP3(dBm)	**16.169~19.254**	**N/A**
PAEmax(%)	**13.04~13.6**	**3~2(3~6GHz)**
Noise figure	**3.9@125°C**	**4~7**
Power consumption (mW)	**72~68**	**74.4**

4.7 Remark

The performance of UWB PA with inductor-resistor feedback is not good by measurement, and there is a band-stop effect on 4.5GHz, the true reason is not clear, it is believed that layout or machine cause problems. Therefore, we ignore the measurement data at 4.5GHz and discuss the result. The inductor-resistor feedback has good performance for input and output matching and total power consumption is 74.4mW with vg 1.2V and vd 1.2V condition. The linearity measurement has no data beyond 6GHz, because of NDL machine limited. From 3~6G, the P1dB is large than -8dBm and fits the specification of UWB. The noise is not bad comparing to other UWB amplifier even LNA at recently days. It shows the potential to design low noise amplifier with inductor-resistor feedback configuration.

Chapter5

Conclusion

Advantage CMOS technology have two main drawbacks, one is low breakdown voltage and one is small bandwidth. However, modern wireless standards need high power or wideband of application. In this thesis, we have presented the design of RF CMOS power amplifier.

One is 5.2GHz power amplifier for 802.11a application, by using cascode configuration. According to the simulation result, the PA allows the maximum output power 22dBm, and has power gain 26dB, P1dB at -3dBm, and total current consumption 204mA at DC supply 3.3V. Since, cascode configuration can increase the output power, the electro-migration and parasitic effect in the circuit may cause performance degradation and reliability problems. However, there are no practical measurement results in this thesis. The LDMOS could be the key element to improve the PA performance in CMOS RF technology.

One is 3~10GHz power amplifier for UWB application, by use inductor-resistor feedback configuration. According to the practical measurement results, we have power gain 13~0dB, and noise figure 4~7 from 3~10GHz. The P1dB is 4dBm and

PAE is lower than 3% from 3~6GHz. Total power consumption is 74.4mW with vg 1.2V and vd 1.2V condition. The noise figure the noise is not bad comparing to other UWB amplifier even LNA at recently days. From 3~6G, the P1dB is large than -8dBm and fits the specification of UWB. The UWB power amplifier can be used for MB-OFDM and DS-CDMA. As the 130nm and 90nm CMOS technologies using in future, the gain will increase and should be able to cover the entire spectrum from 3.1 GHz to 10.6 GHz. The inductor-resistor feedback configuration provides a process to design a wideband matching network, with good performance of noise and gain flatness.

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