

MILC-TFT With High- κ Dielectrics for One-Time-Programmable Memory Application

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Abstract—In this letter, for the first time, one-time-programmable (OTP) memory fabricated on the low-temperature poly-Si p-channel thin-film transistor (TFT) with metal-induced lateral-crystallization channel layer and high- κ dielectrics is demonstrated. The state of this OTP memory can be identified by the scheme of gate-induced drain leakage current measurement. The OTP-TFT memory has good electrical characteristics in terms of low threshold voltage $V_{th} \sim -0.78$ V, excellent subthreshold swing ~ 105 mV/dec, low operation voltage, faster programming speeds, and excellent reliability characteristics.

Index Terms—Gate-induced drain leakage (GIDL), metal-induced lateral crystallization (MILC), one-time programmable (OTP), thin-film transistor (TFT).

I. INTRODUCTION

RECENTLY, nonvolatile memories have become very popular for the applications of portable electronics, in which high density of nonvolatile memory is inevitable. The scaling down of traditional memories has met physical limits due to the aggressive scaling down of the photolithography and tunneling oxide thickness [1], [2]. However, low-temperature poly-Si thin-film transistors (LTPS-TFT) have been widely used for the application of system on panel (SOP) [3] and 3-D circuit-integration elements such as SRAMs, DRAMs, and nonvolatile memories [4]–[6]. Ultrahigh density memories have also been completed using 3-D multilayer stack LTPS-TFT memories. Unfortunately, it is difficult to fabricate nonvolatile memories without any extra mask and processing. Furthermore, many defects occur among the polysilicon channel films because of the large number of grain boundaries, resulting in much poor subthreshold swing (SS) and high threshold voltage (V_{th}) [7], [8]. In this letter, for the first time, the LTPS p-channel TFT with metal-induced lateral-crystallization (MILC) channel layer for the dual application of high-performance device and excellent reliable one-time-programmable (OTP) memory is successfully

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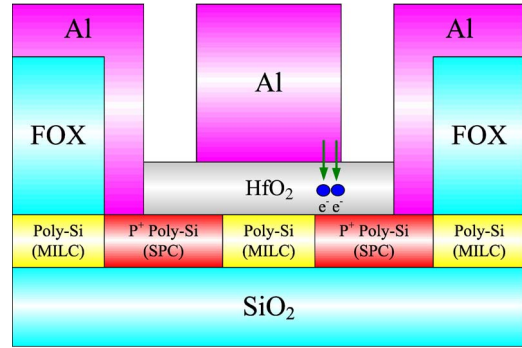


Fig. 1. Cross-sectional scheme of the OTP-TFT memory with MILC polycrystalline silicon channel film and illustration of electron trapping for program state.

proposed. The performance of the LTPS-TFT device, which is demonstrated using the MILC method and HfO_2 gate dielectric, is improved. Moreover, the OTP-TFT memory has been fabricated without any extra mask and processing. This process is simple and fully compatible with standard LTPS-TFT. The MILC-TFT with HfO_2 gate dielectric can be used as OTP memories by measuring the change of gate-induced drain leakage (GIDL) current [9], [10]. The OTP-TFT memory with lower V_{th} , excellent SS, lower operation voltage, longer retention time, and good read disturbance can be obtained, highly promising for the realization of SOP and 3-D circuit integration.

II. EXPERIMENTAL PROCEDURE

The device cross section of the OTP-TFT memory with HfO_2 dielectric and MILC polycrystalline silicon channel film is shown in Fig. 1. First, 500-nm thermal oxide was grown on the Si wafer by furnace system. Undoped amorphous Si (α -Si) layer with a thickness of 50-nm was deposited by low-pressure chemical vapor deposition at 550 °C. A 5-nm Ni layer was deposited by an electron-beam evaporation system at room temperature and patterned by liftoff process as a seed layer to crystallize the α -Si. Then, the 50-nm α -Si layer was crystallized by the MILC process at 550 °C for 24 h in a N_2 ambient. To reduce Ni contamination, the residual Ni was removed by $H_2SO_4 + H_2O_2$. The source and drain (S/D) regions in the device active region were implanted with boron (10 keV at $5 \times 10^{15} \text{ cm}^{-2}$) and activated at 600 °C for 24 h annealing in a N_2 ambient. A 500-nm plasma-enhanced chemical-vapor-deposition oxide was deposited at 300 °C for device isolation. The device active region was formed by patterning and etching isolation oxide. Next, a 50-nm HfO_2 with effective oxide thickness EOT

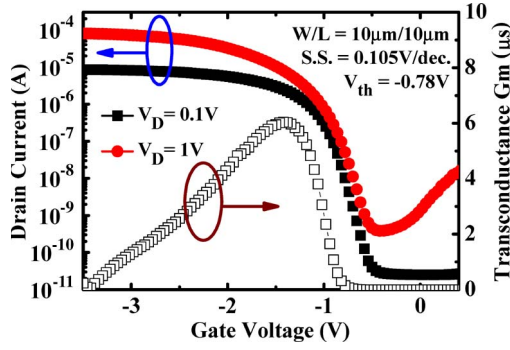


Fig. 2. Room temperature transfer characteristics (I_D - V_G and transconductance G_m) of the OTP-TFT memory with MILC polycrystalline silicon channel film ($V_D = |V_{DS}|$).

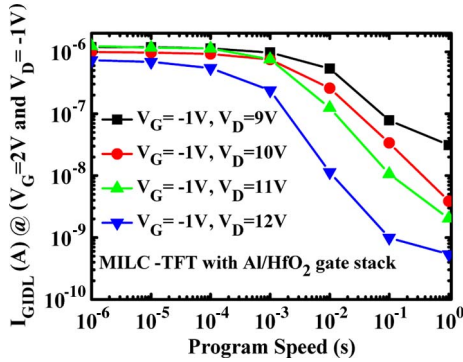


Fig. 3. Program speed characteristics of the OTP-TFT memory with MILC polycrystalline silicon channel film at different operating voltages.

~ 12.3 nm was deposited by electron-beam evaporation system at room temperature. Then, after the patterning of S/D contact holes, a 500-nm Al was deposited by electron-beam system evaporation at room temperature and patterned as Al gate and S/D contact pads. There was no other treatment during fabrication. The standard MILC LTPS-TFT and OTP memory can be fabricated simultaneously. This process is simple and fully compatible with standard LTPS-TFT.

III. RESULTS AND DISCUSSION

Fig. 2 shows the transfer characteristics (I_D - V_G and G_m) of the OTP-TFT memory with MILC polycrystalline silicon channel film. The device with gate length (L) and width (W) of 10 and 10 μm , respectively, was measured. The threshold voltage (V_{th}) of the device was defined as the V_G at which the normalized drain-current reaches $W/L \times 10$ nA for $V_D = -0.1$ V. The OTP device has superior performance, with smaller V_{th} (~ -0.78 V), excellent subthreshold swing (~ 105 mV/dec) and higher drain current. A high gate-capacitance density, which corresponds to low EOT ~ 12.3 -nm, is obtained from the capacitance-voltage curve of Al/HfO₂ on a P-type substrate to extract the gate-capacitance density of OTP-TFT memory (not shown).

In addition, this high-performance MILC-TFT device can also be used as an OTP memory device at sufficient gate voltage and drain voltage operation. The program speed characteristics of OTP-TFT devices with different operating voltages are shown in Fig. 3. The OTP-TFT device is programmed

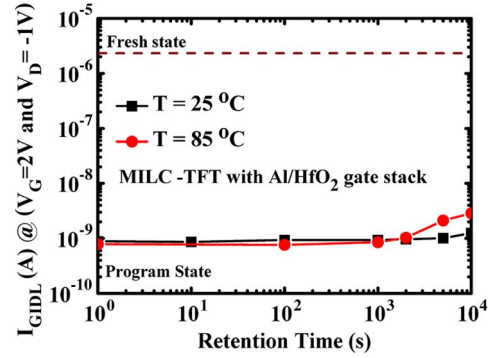


Fig. 4. Data retention characteristics of OTP-TFT memory for the different bake temperatures. After 10k s at 25 °C, no significant GIDL current shift occurred.

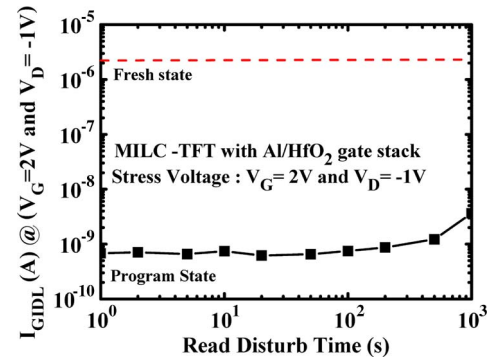


Fig. 5. Read disturbance characteristics obtained for the OTP-TFT memory (stress voltage on $V_G = 2$ V and $V_D = -1$ V).

using electron gate injection mechanism for OTP memory application. The program conditions are follows: $V_G = -1$ V and $V_D = 9, 10, 11,$ and 12 V. The change of GIDL current (I_{GIDL}) may be read from Fig. 3. The I_{GIDL} was measured from the OTP-TFT device with $V_G = 2$ V and $V_D = -1$ V. The higher current (1 μA) and lower current (500 pA) of I_{GIDL} were defined as the erased state (“0” state) and programmed state (“1” state), respectively. The memory states of MILC-TFT memory can be determined from the GIDL current under forward read operation [9], [10]. In the trapping location, the electrons have been trapped in the HfO₂ layer at the gate and drain overlap region (in Fig. 1). Furthermore, the GIDL current is reduced owing to the electron trapping at the gate and drain overlap region. The lower GIDL current can be attributed to the decrease of vertical electric field. A higher voltage for V_D trends to result in larger I_{GIDL} change and faster programming speed owing to the higher local electric field near the drain side. Comparing OTP-TFT memory with other LTPS-TFT memory devices, the programming voltage and read voltage are relatively smaller [12].

Fig. 4 shows the data retention performance which is measured at room temperature and 85 °C. At room temperature, charge loss can be barely observed up to 10⁴ s. The OTP-TFT device with HfO₂ gate dielectric exhibits good retention characteristics at room temperature and high temperature due to the deep-trapping level in the HfO₂ layer. The results indicate that the I_{GIDL} change is still retained about three orders after 10⁴ s at 85 °C. Hence, the trapped electrons in the OTP-TFT memory with the HfO₂ dielectric are not easily

detrapped. In addition, the measured read-disturb characteristic is shown in Fig. 5. The stress voltage was set at $V_G = 2$ V and $V_D = -1$ V. The I_{GIDL} is slightly increased after 10^3 s, due to the electron detrapping by the stress voltage. Consequently, the I_{GIDL} change is maintained about three orders after 10^3 s read disturb. Compare with other TFT-memory devices [12]–[14], OTP-TFT devices can be operated at lower voltages and higher program/erasing speeds with better charge retention over the same period of time.

IV. CONCLUSION

For the first time, a high-performance LTPS p-channel TFT with MILC channel layer with HfO_2 gate dielectric used for OTP memory is successfully fabricated. This novel structure has excellent characteristics: low threshold voltage, excellent subthreshold swing, low operation voltage, faster programming speeds, and excellent reliability characteristics. OTP-TFT memory offers a very promising solution for the application of SOP and 3-D circuit integration.

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