國立交通大學

電子工程學系　電子研究所碩士班

碩士論文

應用於無線區域網路的 0.7-V 5-GHz 互補式金氧半導體直接降頻式射頻前端接收器

THE DESIGN OF SUB-0.7V 5-GHz CMOS DIRECT-CONVERSION RECEIVER FRONT-END FOR WIRELESS LAN APPLICATIONS

研 究 生：粘家熒

指導教授：吳重雨 博士

中華民國 九十四 年 十一 月

應用於無線區域網路的 0.7-V 5-GHz 互補式金氧半導體直接降頻式射頻前端接收器

The Design of Sub-0.7V 5-GHz CMOS Direct-Conversion Receiver Front-End for Wireless LAN Applications

研 究 生：粘家熒　　Student: Chia-Ying Nien

指導教授：吳重雨 博士　　Advisor: Dr. Chung-Yu Wu

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronic Engineering

November 2005

Hsin-Chu, Taiwan, Republic of China

中華民國 九十四 年 十一 月

應用於無線區域網路的 0.7-V 5-GHz 互補式金氧半導體直接降頻式射頻前端接收器

研究生：粘家熒　　指導教授：吳重雨　博士

國立交通大學

電子工程學系　電子研究所碩士班

摘　要

本論文提出一個操作電壓低於 0.7 伏特應用於無線區域網路的 5-GHz 低功率直接降頻式射頻前端接收器。此射頻接收器包含的電路有低雜訊放大器，可補償直流偏差的降頻器和正交壓控振盪器，透過國家晶片系統設計中心委託台灣積體電路製造股份有限公司以 0.18 微米互補式金氧半導體的製程製造。整個射頻接收器已經被完整地設計、製造與量測完成。

量測結果顯示，此射頻接收器可在低於 0.7 伏特的操作電壓下正常運作，但由於對寄生效應的疏忽，量測得到的效能不如預期。其中，射頻接收器的轉換增益為 12.6 dB，雜訊指數為 24 dB，1 dB增益壓縮點為-24 dBm，此外，當輸入一個頻率與正交壓控振盪器的頻率相同且強度為-50 dBm的訊號至接收器的輸入端時，自身混波後產生的直流偏差小於 3 毫伏。此射頻接收器的消耗功率為 8.14 毫瓦，晶片面積為 4.4 mm^2。經過分析因寄生效應而產生頻率偏移的問題之後，修正過的射頻接收器即可符合IEEE 802.11a的規格。

The Design of Sub-0.7V 5-GHz CMOS Direct-Conversion Receiver Front-End for Wireless LAN Applications

Student: Chia-Ying Nien Advisor: Dr. Chung-Yu Wu

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

Abstract

A sub-0.7V 5-GHz direct-conversion receiver for low-power and wireless applications is proposed in this thesis. The receiver composed of a low-noise amplifier, a set of I/Q downconverters with a DC compensation circuit, and a quadrature voltage-controlled oscillator is realized in a 0.18-μm CMOS technology supported by Taiwan Semiconductor Manufacturing Company via Chip Implementation Center. The proposed receiver is completely designed, fabricated and tested.

Measured results exhibit that the receiver can operate well under supply voltages of 0.65 V and 0.7 V even though it doesn't achieve adequate performance due to an oversight of parasitic effects. The receiver performs a conversion gain of 12.6 dB, a noise figure of 24 dB, a 1-dB compression point of -24 dBm, and a DC offset of less than 3 mV with an injected input power of -50 dBm, while draining 8.14 mW and covering 4.4 mm^2. The problem of frequency shift in measurement is discussed and modified, and a re-designed receiver, which is able to fit the IEEE 802.11a specification, is completed.

誌　謝

能夠順利完成碩士論文，首先要感謝我的指導教授吳重雨老師；在研究所的這兩年裡，老師提供我一個良好的學習環境，並且在學習與研究上適時的給予我指導與啟發，更教導我許多研究的方法，讓我學會了作研究應有的態度。其次要感謝論文口試的評審委員，柯明道教授、柏振球教授與高宏鑫博士對我的論文提出了許多建議，讓我獲益良多，並且使我的論文內容更加完整。

再來要感謝實驗室的學長們，周宗昀、王文傑、虞繼堯、蘇烜毅、陳旻珓、林韋霆、Ismail、Fadi、丁彥、謝致遠、張秦豪、鄭建祥、許德賢、歐欣華，學長們給予我的幫助與指點和研究上的經驗傳承，讓我可以順利完成論文。接著要感謝這兩年一起在實驗室打拼的夥伴們，岱原、吳諭、煒明、靖驊、鍵樺、建樺、弼嘉、台祐、宗熙、建文、進元、竣帆、志朋、傑忠、啟祐、宗信、文芩、豪傑、怡凱、必超、晏維、柏宏…等，由於他們的鼓勵與幫忙，陪伴我度過這段研究生活，也增添了許多歡笑與回憶。

還有要感謝這兩年來一直陪著我的女朋友勤穎，當我面臨壓力時鼓勵我，給我繼續前進的動力，當我研究繁忙時體諒我，讓我可以全心衝刺；感謝她陪我經歷這段成長歷程，一起分享生活中的心情點滴。最後要感謝我的爸媽和妹妹，感謝爸媽不辭辛勞的養育我、栽培我，讓我在求學的過程沒有後顧之憂，而且不斷的支持我，讓我可以朝著自己的目標努力前進。

感謝每個人的參與，讓我度過這段精彩的研究生活，順利獲得碩士學位。

粘家熒

于 風城交大

乙酉・秋

CONTENTS

Chinese Abstract i

English Abstract ii

Acknowledgement iii

Contents iv

Table Captions vi

Figure Captions vii

CHAPTER 1 INTRODUCTION 1

1.1 Background 1

1.2 A Review of CMOS RF Receiver Front-End 2

1.2.1 Receiver Architectures 3

1.2.2 Issues in Direct-Downconversion 7

1.2.3 Low-Voltage Receivers 14

1.3 Motivation 14

1.4 Thesis Organization 15

CHAPTER 2 SUB-0.7V 5-GHz DIRECT-CONVERSION RECEIVER FRONT-END 16

2.1 IEEE 802.11a PHY Specification and Link Budget 16

2.2 Downconverter with DC-Offset Compensation 20

2.2.1 Operational Principle 20
2.2.2 DC-Offset Compensation 24
2.2.3 Circuit Implementation 27
2.3 Folded-Cascode Low-Noise Amplifier 30
2.3.1 Design Considerations 31
2.3.2 Circuit Implementation 35
2.4 Quadrature Voltage-Controlled Oscillator 37
2.5 Receiver Realization 39
2.6 Simulation Results 42

CHAPTER 3 EXPERIMENTAL RESULTS 53

3.1 Layout Description 53
3.2 Measurement Considerations and Setup 54
3.3 Experimental Results 60
3.4 Discussions and Comparisons 69

CHAPTER 4 CONCLUSIONS AND FUTURE WORKS 80

4.1 Conclusions 80
4.2 Future Works 80

REFERENCES 82

Table Captions

Table I	Comparison on DC-Offset Cancellation Methods	11
Table II	IEEE 802.11a Receiver Requirements	18
Table III	Design Target Set of Receiver	20
Table IV	Detailed Parameters of the Downconverter	30
Table V	Detailed Parameters of the LNA	37
Table VI	Detailed Parameters of the Quadrature VCO	39
Table VII	Detailed Parameters of the Output Buffer	41
Table VIII	Simulated Bias Statuses of Positive-Substrate-Biased MOS Transistors	45
Table IX	Detailed Simulated Results of DC Offset at Each Stage	51
Table X	Post-Simulation Summary of the Receiver	52
Table XI	Comparison on Bias Status between Post-Simulation and Measurement	68
Table XII	Summary of the Tested Receiver	69
Table XIII	Summary of Revised Post-Simulation	73
Table XIV	Summary of the Re-Designed Receiver	75
Table XV	Comparison of Performance with Other Proposed 5-GHz Receivers	78
Table XVI	Comparison of Performance with IEEE 802.11a Specification	79

Figure Captions

Fig. 1	General receiver architecture.	3
Fig. 2	Heterodyne downconversion.	4
Fig. 3	Simple homodyne receiver.	5
Fig. 4	Hartley architecture.	6
Fig. 5	Weaver architecture.	7
Fig. 6	Self-mixing of (a) LO signal, (b) a strong interferer [6].	8
Fig. 7	Quadrature generation in (a) RF path, (b) LO path [24].	13
Fig. 8	Receiver architecture.	16
Fig. 9	Channel allocation of the IEEE 802.11a standard within the UNII band.	17
Fig. 10	Block diagram of modulator.	21
Fig. 11	Realization of combiner.	22
Fig. 12	Modulator circuit realized by two-input combiners.	23
Fig. 13	Simple example of DC-offset generation.	24
Fig. 14	DC-offset compensation circuit [15].	25
Fig. 15	A band-pass filter as the load of downconverter.	27
Fig. 16	Impedance of band-pass filter.	27
Fig. 17	(a) I-channel and (b) Q-channel downconverter with DC-offset compensation circuits.	30
Fig. 18	Input impedance of common-source with inductive source degeneration.	31
Fig. 19	Revised model of input impedance.	32
Fig. 20	Noise model of input stage.	33
Fig. 21	Minimum NF curves related to channel width and power consumption.	35
Fig. 22	Intermodulation phenomenon [3].	35

Fig. 23 Folded-cascode LNA. 37
Fig. 24 General resonator. 38
Fig. 25 Conceptual diagram of quadrature VCO. 38
Fig. 26 Quadrature VCO. 39
Fig. 27 I-channel output buffer. 41
Fig. 28 Frequency response of the output buffer. 41
Fig. 29 Simulated S11 of the LNA. 43
Fig. 30 Simulated voltage gain of the LNA. 43
Fig. 31 Simulated noise figure of the LNA. 43
Fig. 32 Two-tone test plot of simulated IIP3 of the LNA. 44
Fig. 33 Simulated DC transfer characteristics of the downconverter. 45
Fig. 34 Simulated quadrature IF waveforms (solid-line: I-channel, dot-line: Q-channel). 45
Fig. 35 Simulated LO spectrum. 46
Fig. 36 Simulated quadrature LO waveforms (solid-line: I-channel, dot-line: Q-channel). 46
Fig. 37 Simulated tuning range of the quadrature VCO. 47
Fig. 38 Simulated phase noise of the quadrature VCO. 47
Fig. 39 Simulated conversion gain of the receiver. 48
Fig. 40 Simulated noise figure of the receiver. 49
Fig. 41 Two-tone test plot of simulated IIP3 of the receiver. 49
Fig. 42 Two-tone test plot of simulated IIP2 of the receiver. 50
Fig. 43 Simulated DC offset at each stage. 50
Fig. 44 Layout configuration of the receiver. 54
Fig. 45 Chip microphotograph. 55
Fig. 46 Bonding board for the receiver. 55
Fig. 47 Half circuit of input matching network. 56
Fig. 48 DC board for the receiver. 57

Fig. 49 Adjustable voltage module. 57

Fig. 50 Measurement setup for the receiver. 58

Fig. 51 Measurement setup for DC offset. 59

Fig. 52 Test platform for the receiver. 59

Fig. 53 S11 of the receiver. 60

Fig. 54 Measured spectrum of the QVCO. 62

Fig. 55 Microphotograph of the QVCO after laser-cut. 62

Fig. 56 Measured tuning range of the QVCO. 63

Fig. 57 Measured IF spectrum. 64

Fig. 58 Measured conversion gain of the receiver. 64

Fig. 59 Measurement setup for noise figure. 66

Fig. 60 Measured noise figure of the receiver. 66

Fig. 61 Measured 1-dB compression point of the receiver. 67

Fig. 62 Measured DC offset of the receiver. 67

Fig. 63 Equivalent inductances of spiral inductors in the QVCO. 70

Fig. 64 Equivalent quality factors of spiral inductors in the QVCO. 70

Fig. 65 Revised post-simulation of conversion gain. 71

Fig. 66 Revised post-simulation of SSB noise figure. 72

Fig. 67 Revised post-simulation of 1-dB compression point. 72

Fig. 68 Revised post-simulation of DC offset. 72

Fig. 69 Layout configuration of the re-designed QVCO. 74

Fig. 70 Equivalent inductances of re-designed center-tap inductor. 74

Fig. 71 Simulated tuning range of the re-designed QVCO. 75

Fig. 72 Simulated DC voltage with device variations on *Mi3* and *Mi5*. 76

Fig. 73 Modified downconverter. 76

CHAPTER 1
INTRODUCTION

1.1 Background

In the last two decades, the demand for wireless communication technologies has grown significantly. Wireless communication systems have made great progress from bulky to handy as well as from costly to widespread. The main driving force behind the trends is the evolution of integrated-circuits (IC) techniques. As the developments of semiconductor fabrication, in addition to perform the best performance, they are requested to achieve low cost, low power and short time-to-market. Therefore, wireless communication technologies are going to advance more rapidly in company with the progress of IC techniques.

Radio-frequency integrated circuits (RFIC) play the leading roles in wireless communication systems. In the past, high-frequency circuits, such as low-noise amplifiers, mixers and power amplifiers, are usually implemented in III-V or bipolar processes due to their superior device characteristics in high frequency range. However, these processes are usually high-priced and cannot be integrated with general silicon processes that are adopted to fabricate digital integrated circuits. For this reason, over recent years, CMOS technology is gradually in widespread use to implement an entire communication system, including RF front-end and baseband circuits.

Besides, wireless equipments with high performance depend on proper-designed circuits. Each kind of applications is created for a specific use, such as GSM and GPRS for mobile communication; Bluetooth for wireless personal area network (WPAN), and IEEE 802.11 family for wireless local area network (WLAN). Actually, the extreme performance that circuits can reach affects the establishment of specifications. RF circuits are usually a main bottleneck even if they occupy only a little part in a communication system. The complexity

on the characteristics of analog and high-frequency causes difficulties in design methodology. In order to overcome the obstacles, researchers are devoted to investigations on materials, lithography techniques and architectures to improve existent drawbacks. As plenty studies bring lots of efficient developments, more and more wireless equipments have become commercial and popular products.

Nowadays, electric products with embedded wireless devices have been available; for example, most people have their own cellular phones. Undoubtedly, emerging circuits and sophisticated processes are coming to existence without an end. Owing to cord-free convenience, wireless communication will go deep into everyone's daily life in the future.

1.2 A Review of CMOS RF Receiver Front-End

A RF receiver front-end generally consists of several main components: a low-noise amplifier (LNA), downconverters and filters. LNA amplifies the desired RF signal received from antenna with low-noise distribution. Downconverters perform frequency translation by multiplying a RF signal and an LO signal generated by a voltage-controlled oscillator and output a lower-frequency signal to feed subsequent stages. Filters suppress the undesired signals for baseband circuits receiving messages with sufficiently low error rate. Fig. 1 enumerates a general receiver architecture for example. However, in practical applications, receivers can be implemented with different architectures for various system requirements. Every existent architecture has superiority and inferiority of itself; therefore, an appropriate choice should depend on the specific necessity.

There are several practical issues affecting a receiver. First, because most wireless communication systems are narrow-band systems, for instance, the IEEE 802.11a standard regulates an operating band from 5.15 GHz to 5.35 GHz and a channel bandwidth of 20 MHz [1], they usually suffer from nonlinearity issues. While signals with various frequencies are received simultaneously, intermodulation phenomenon corrupts the adjacent-channel signals

[2]. It is hard to suppress the undesired intermodulated signals by any additional filters. Furthermore, sensitivity and maximum dynamic range are issues of signal power level [2]. The former is limited by noise floor. It is not detectable while signal power is lower than noise floor. Operating range of the transistors in circuits confines the later. Besides, due to all circuit blocks fabricated on an identical wafer, signals in one component may leak to another via substrate. Other special issues on different architectures are discussed in the following subsection.

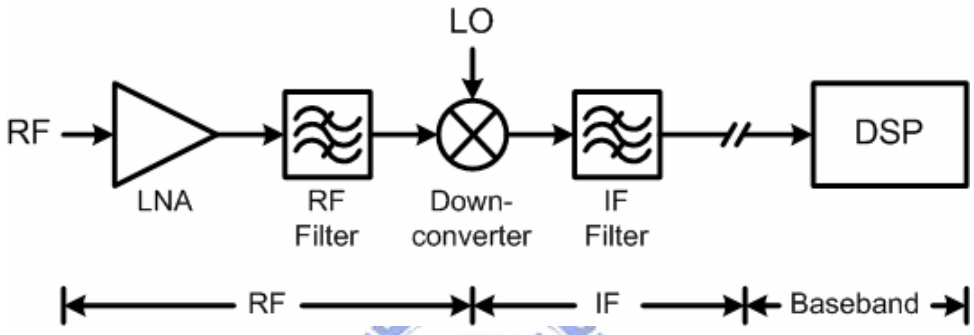


Fig. 1 General receiver architecture.

1.2.1 Receiver Architectures

As RF receivers evolve continuously, several main architectures in recent years can be generalized. They are heterodyne receivers, homodyne receivers and image-reject receivers [3].

■ **Heterodyne Receivers**

In a heterodyne architecture, the received RF signal is downconverted to an intermediate-frequency (IF) signal with its frequency range between RF and baseband; that is, $\omega_{IF} = \omega_{RF} - \omega_{LO}$. Illustrated in Fig. 2, the downconverter mixes RF and LO signals and generates IF signal.

This architecture has a serious problem of image. If image signal and the desired signal are received simultaneously, they are downconverted to an identical IF. Since the system is for narrow-band communication, the image must be out of the desired band. The most common

approach to suppressing the image is through the use of an image-reject filter placed before the downconverter, as depicted in Fig. 2. The filter is designed to have a relatively small loss in the desired band and a large attenuation in the image band. Nevertheless, the image-reject filter is usually implemented with external passive components because it is difficult to design an on-chip filter with a sufficiently high quality factor. Even if an integrated image-reject filter has been proposed [4], the large power dissipation seems to be an unworthy sacrifice for low-power applications.

In addition, the heterodyne receiver exhibits a trade-off between image rejection and channel selection when deciding an IF [3]. A low-IF choice leads to inferior rejection of image whereas a high-IF choice needs a high-Q channel-select filter. Since the image degrades the sensitivity of the receiver, the choice of IF entails a trade-off between sensitivity and selectivity. In order to relax the trade-off, dual-IF topology is applied [5]; however, it has the power-consumption issue due to more circuit stages for multi-downconversion procedure. In conclusion, compared with other receiver topologies, heterodyne receiver can achieve better performance, but at the same time it is more complicated, difficult to be integrated, and not appropriate to realize the last wireless communication standards.

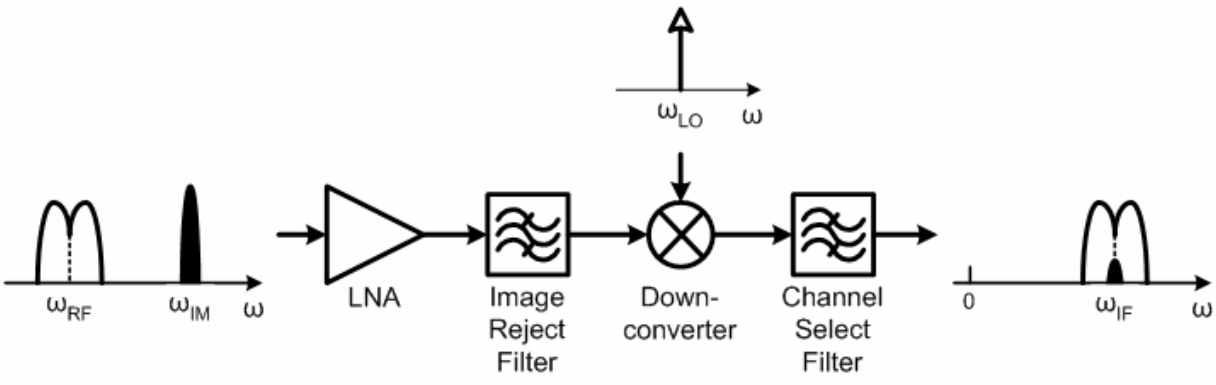


Fig. 2 Heterodyne downconversion.

■ **Homodyne Receivers**

Also called “direct-conversion” or “zero-IF” receiver, homodyne receiver converts RF signal directly to baseband by mixing once. Illustrated in Fig. 3 is a simple homodyne receiver, where the LO frequency is equal to the carrier frequency of the interested channel. Note that a low-pass filter is also required to perform channel selection.

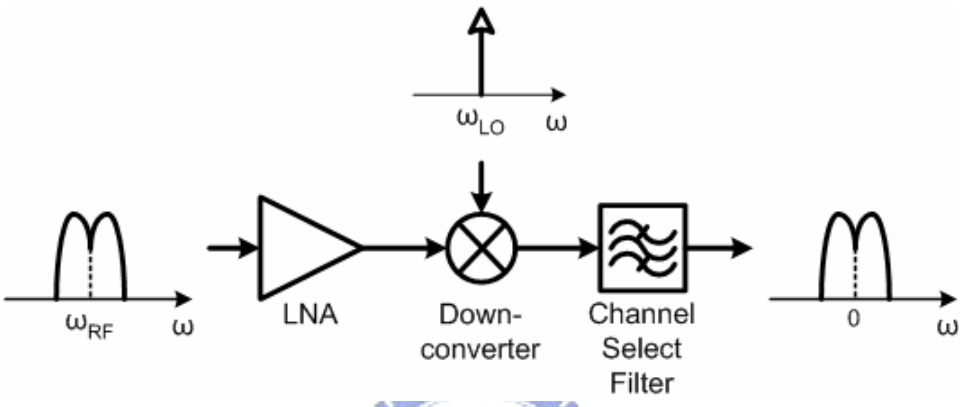


Fig. 3 Simple homodyne receiver.

The simplicity of the homodyne architecture causes high integration, low cost and low power. Moreover, the most important advantage is that the problem of image is circumvented because the IF frequency is zero. As a result, no image filter is required. This may also simplify the LNA design because there is no need for the LNA to drive a 50-Ω load, which is often necessary when dealing with image reject filters.

On the other hand, the homodyne receiver topology incorporates a number of issues that do not play roles in a heterodyne receiver like flicker noise, I/Q mismatch, even-order distortion and, above all, DC offsets [2], [6]. All of them are challenges to designers so that a multitude of solutions have been proposed. They are discussed in detail in the next subsection.

■ **Image-Reject Receivers**

To resolve the trade-offs governing the use of image-reject filters in heterodyne architecture, several innovative techniques of suppressing images have been proposed. We

enumerate two representative techniques in this section.

An image-reject architecture originating from a single-sideband (SSB) modulator is introduced by Hartley in 1928 [7]. Illustrated in Fig. 4, Hartley's circuit mixes the RF signal with the quadrature outputs of the local oscillator, low-pass filters the resulting signals, and then shifts one by 90° before adding them together. It is apparent that the IF output is free from the image after this process. However, the principal drawback of this architecture is its sensitivity to mismatches due to the phase and gain deviations of the two LO quadrature outputs; therefore, incomplete image cancellations come about. Also, the Hartley topology suffers from the loss and noise of the shift-by-90° stage and the linearity of the adder.

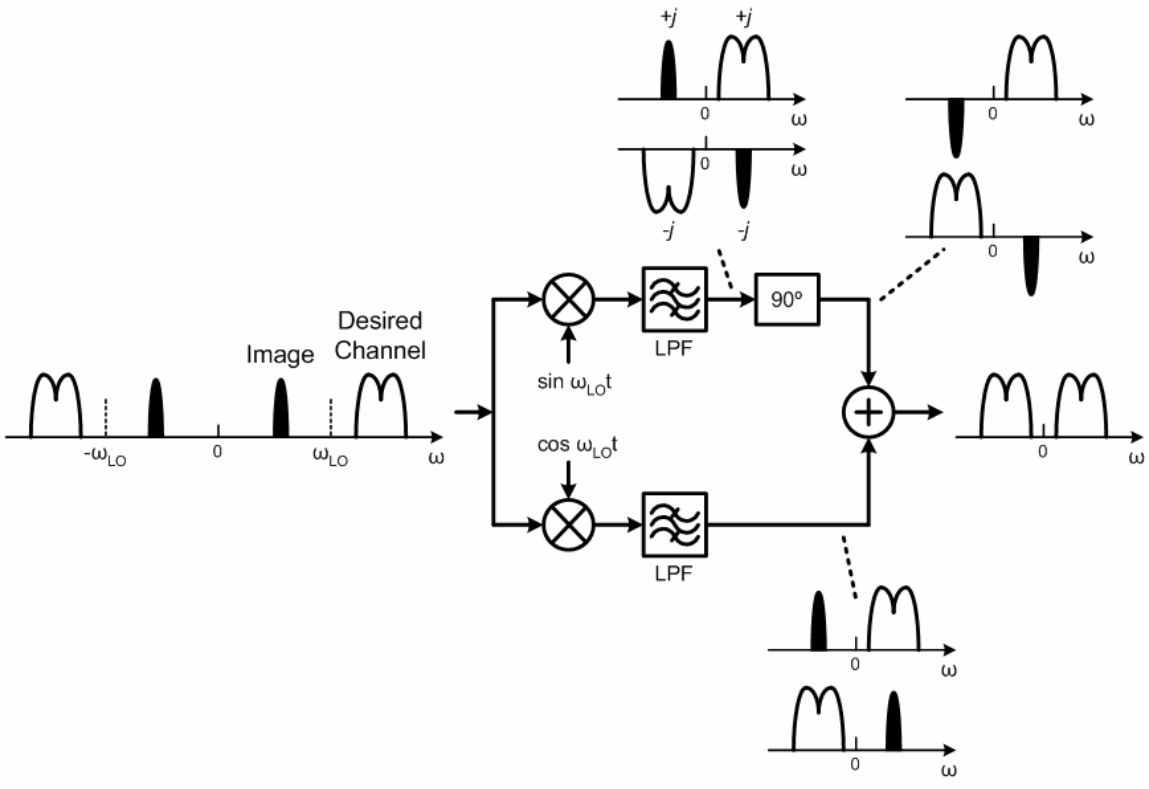


Fig. 4 Hartley architecture.

Another technique is the Weaver architecture [8], which allows an arbitrary translation of the signal band without image interference, originally invented as an alternative to Hartley's single-side band modulator. Illustrated in Fig. 5, this circuit performs two consecutive

quadrature downconversion operations on the signal and the image such that if the final outputs are subtracted, the signal is obtained and the image is suppressed. The Weaver approach is also sensitive to mismatches, but is avoid the use of an *RC*-*CR* network that is used to realize the shift-by-90° circuit, thereby achieving greater image rejection despite process and temperature variation. Moreover, an important issue in the Weaver architecture is the secondary image [3]. If the secondary downconversion translates the signal spectrum to a nonzero center frequency, an unwanted band may fall into the desired channel. This effect constrains the choice of the second LO frequency.

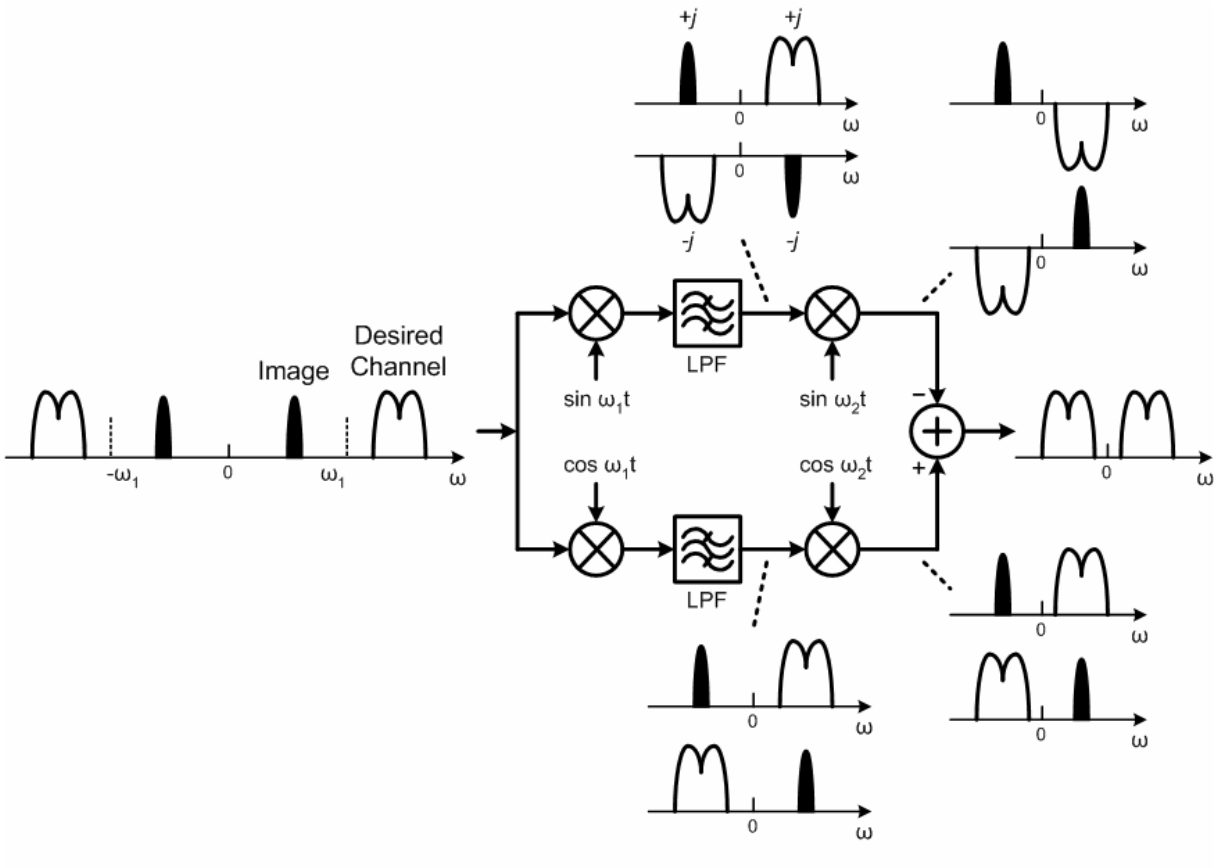


Fig. 5 Weaver architecture.

1.2.2 Issues in Direct-Downconversion

- **DC Offsets**

In a homodyne topology, because of the downconverted band extending to the vicinity of zero frequency, extraneous offset voltages can corrupt the signal and even saturate the following stages. Illustrated in Fig. 6, DC offset can be generated by the mixing of the LO leakage signal and LO signal [Fig. 6(a)] because the isolation between the LO port and the inputs of the mixer and the LNA is finite. Similarly, a self-mixing occurs if a strong interferer leaks from the LNA or mixer input to the LO port [Fig. 6(b)]. These effects arise from capacitive and substrate coupling in chief. Besides, the transistor mismatch in the signal path and the demodulation of a large amplitude modulation (AM) signal via second-order nonlinearity of the mixer also generate DC offset [9].

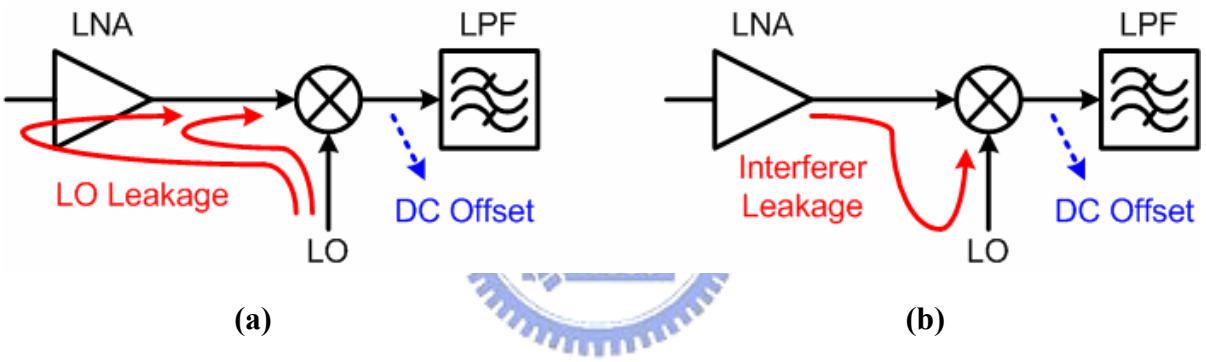


Fig. 6 Self-mixing of (a) LO signal, (b) a strong interferer [6].

The DC offset resulting from self-mixing is estimated roughly as follows. In general, the total gain of a receiver front-end from antenna to ADC is typically around 80 to 100 dB so as to amplify the microvolt input signal to a level that can be digitalized by an ADC [3]. Of this gain, typically 20 to 25 dB is contributed by the LNA/mixer combination and residues are provided by the baseband amplifier. Suppose an LO signal has a power of 0 dBm and experiences an attenuation of 60 dB as it couples to the input of the LNA. If the gain of the LNA/mixer combination is around 25 dB, then the offset produced at the output of the mixer is on the order of 6 mV. When directly amplified by the baseband amplifier, the offset voltage saturates the following circuits, thereby prohibiting the amplification of the desired signal.

From the above discussion, we infer that homodyne receivers require some means of offset cancellation. A natural solution is ac-coupling, i.e. high-pass filtering, after downconversion [10]. Unfortunately, this solution also removes the DC energy of the desired signal. In addition, it requires large capacitors or resistors and thus brings unavoidable in-band loss. When high-pass filters (HPF's) are applied, it has to be noted that the poles of these HPF's cannot be too low as they would result in long transient settling during gain changes or Tx-to-Rx switching [11]. Another alternative method of offset cancellation is the DC-coupled stage with a feedback configuration [12], [13]. That is, a negative feedback scheme is around the baseband amplifier. The low-frequency content at the output of the baseband amplifier is fed back through a g_m-C filter to the mixer in order to cancel DC offset and flicker noise. Compared with the ac-coupling, it employs only grounded capacitors and can therefore utilize MOS capacitors which need several times smaller than the floating counterpart [14]. Nevertheless, an extra g_m-C filter has to be integrated into the baseband amplifier, resulting in a constraint on stability. Based on the concept of filters to remove the DC offsets, we infer that the filter can be integrated into the mixer to economize on power consumption. The downconverter in this thesis integrates the DC-offset compensation circuit with band-pass filter, which is proposed in [15], is discussed in detail in the next chapter.

In addition to the preceding methods of utilizing filters, in the multiphase reduced frequency conversion receiver architecture [16], the VCO frequency is far below the carrier frequency; as a result, the main power of LO leakage is not located at the carrier frequency and then the amount of DC offset can be reduced. However, it not only brings about complexity and symmetrization in circuit design but also consumes extra power due to multiphase VCO and mixer. Also, offset can be alleviated effectively in the architecture which comprises a balanced harmonic mixer [17]. Instead of LO signal and RF carrier running at the same frequency, the second harmonic of the LO signal takes part in the mixing process. Therefore, the LO leakage generates no DC component but an output which is still situated at

the LO frequency can be easily filtered out [18]. On the other hand, the main issues of this architecture are its weakness in linearity and higher LO power due to the use of second harmonic signal.

Besides the above-mentioned static DC offset, time-varying DC offsets can be the result of self-mixing due to leakage of single-tone (CW) or frequency-modulated (FM) interference to the LO port. Similarly, second-order distortion applied to CW or FM interference results in DC offset, which varies with the frequency and the power level of the received signal [19]. At 5-GHz carrier frequency, on account of high attenuation and absorbance of the reflected signals, such time-varying DC offsets are small compared to the static DC offsets and the dynamic range of the receiver, thus they can be tracked and removed by digital signal processing (DSP) after analog-to-digital conversion.

Recently, dynamic calibration with DSP techniques is in widespread use to solve the offset problems. In general, it has to be achieved with DAC's. Furthermore, if the LNA is gain-variable, a lookup table (LUT) can be incorporated in the receiver and the pre-calibrated compensation values can be selected based on gain control [20]. An algorithm has been implemented in the baseband circuits to automatically calibrate the LUT whenever the receiver is in the idle mode and no signal is detected, which is adequate for stationary offset. Nonetheless, when there is a jump change in the value of the offset, it is no longer a good estimator for the offset [21]. A practicable method for this situation is proposed by utilizing IIR filters to produce more than one pre-designated threshold [22].

Table I lists the features of the above methods of DC-offset cancellation. In brief, the offset cancellation circuits should be easily-integrated, power-saving, and eliminate offsets as completely as possible.

Table I Comparison on DC-Offset Cancellation Methods

Reference	[11]	[13]	[15]	[16]	[18]	[20]	[21]
Large C or R	V	V					
Long settling and in-band loss	V						
Constraint on stability		V	V				
Complex structure				V		V	
Sensitive to layout symmetrization				V			
Weakness in linearity					V		
No dynamic calibration	V	V	V	V	V		
Require DAC's						V	V
Require CMFB circuits							V
Extra power consumption	V	V	V	V	V	V	V

■ **Flicker Noise**

Also known as "1 / f" noise, flicker noise is an intrinsic noise in semiconductor devices, and most prominent in surface-transport devices such as the CMOS due to random trapping/de-trapping of charge carriers at the oxide-silicon interface [23]. In typical submicron MOS technologies, minimum-channel MOSFET with a width of a few hundred microns and bias current of a few hundred microamperes exhibit a flicker-noise corner frequency in the vicinity of 1 MHz [24]. Thus, the baseband signal below the flicker-noise corner frequency is overwhelmed by the noise. The flicker noise in CMOS technology might exceed the white noise up to several megahertz [25], which corrupts the signal bandwidth seriously in various communication systems.

In the main, flicker noise is roughly proportional to the channel current and inversely proportional to the dimensions of transistor. For this reason, it can be mitigate by reducing the channel current, thus trading linearity and transconductance with the flicker noise. Another

approach is that adopting the transistors with large dimensions in flicker-noise-sensitive areas, such as the tail current source and the input transistors, which, however, degrades the transconductance and slows the circuit operation. It is usually believed that PMOS transistors exhibit less flicker noise than NMOS transistors since the former carry holes in a buried channel; nevertheless, this difference between PMOS and NMOS transistors is not consistently observed [26]. All of these approaches are useless in the RF mixer design, where both low parasitics and high transconductance are crucial to the circuit performance; hence, an improved passive mixer based on active mixer is proposed to alleviate noise while maintaining an adequate transconductance [27], [28]. The two-stage mixer separates into the *V-I* converter and the current-steering switches to obtain optimal performance respectively.

■ **I/Q mismatch**

For most phase and frequency modulation schemes, a homodyne receiver must incorporate quadrature downconversion. This requires the quadrature generation either in RF path or in LO path (Fig. 7). In either case, the errors arising from the inaccurate 90° phase shift and mismatches between amplitudes of the *I* and *Q* signals distort the constellation of the downconverted signal, resulting in an enhanced bit error rate (BER). The tolerance to gain and phase error usually depends on different modulation schemes. For example, the use of 64-QAM modulation requires a signal-to-noise ratio (SNR) of 30 dB, which is substantially greater than that required by the FSK modulation in Bluetooth and the QPSK modulation in 802.11b. This high SNR translates to stringent phase noise requirements for the frequency synthesizer and tight I/Q matching constraints for the receiver [29].

The problem of I/Q mismatch tends to decrease with higher levels of integration. For instance, the I/Q mismatch is much less troublesome in homodyne receivers than in image-reject architectures [24]. In analog IC design, the lower frequency allows the use of large devices to improve the matching without excessive power dissipation. Besides, I/Q mismatch should be less sensitive to process variation and temperature. The self-calibrated

circuits integrated into either the ring oscillator [30] or the LC oscillator with a tunable poly-phase filter [31] can overcome these phenomena adequately.

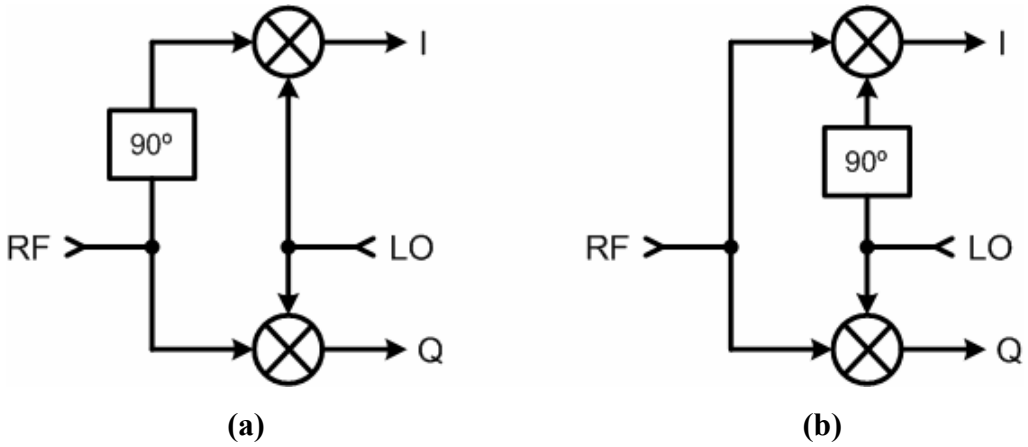


Fig. 7 Quadrature generation in (a) RF path, (b) LO path [24].

■ **Even-Order Distortion**

Typical RF receivers are susceptible to only odd-order intermodulation effects. In direct conversion, on the other hand, even-order distortion, especially second-order nonlinearity, also becomes problematic [3]. Suppose two strong interferers close to the channel of interest experience nonlinearity in the LNA, they can generate a low-frequency beat in the presence of even-order distortion. If mismatches between differential pairs or other asymmetry occur in the mixer, the RF signal feedthrough directly to the IF output, thus the low-frequency beat corrupts the baseband signal.

Even-order distortion can be suppressed by adopting differential circuits or high-pass filters. Differential LNA's and double-balanced mixers are much less susceptible to distortion on account of the inherent cancellation of even-order products. However, the phenomenon is critical for balanced topologies as well due to unavoidable asymmetry between the differential signal paths [32].

1.2.3 Low-Voltage Receivers

Low power has become a significant trend in circuit design. Reducing the supply voltage is a familiar way to save power; however, it degrades the performance of circuits because the operational range decreases inevitably. Low supply voltage constrains the numbers of cascoded MOS devices. Each MOS transistor occupies a DC-voltage drop to sustain operation in saturation region. Voltage swing margin is also an essential consideration in analog circuit design, including RF receivers. Moreover, maintaining linearity and noise performance are challenges in low-voltage design.

Several innovations on design methodology are proposed to achieve low-voltage design. There are two 5-GHz CMOS receivers realized with 1.1-V and 0.8-V supply, respectively [15], [33]. The first receiver, which comprises a differential LNA, a set of I/Q downconversion mixers with DC-offset compensation circuits and a quadrature voltage-controlled oscillator (VCO), performs low power consumption. The other comprising a differential LNA, a set of active mixers and a quadrature VCO exhibits high linearity. In addition, adopting MOS devices with positive substrate bias is a feasible scheme in low-voltage design [34].

1.3 Motivation

In the previous section, we review several receiver architectures and mention that the problem of image is circumvented in homodyne architecture. Besides, in the IEEE 802.11a standard, no subcarriers are in the center frequency of each channel, resulting in an empty spectrum of ±156.25 kHz after downconverted to baseband. For this reason, the direct-conversion architecture is appropriate to realize the receivers for the 802.11a applications since the DC offset is no longer a critical problem. It is also mentioned that low-voltage design can satisfy the demand of low power. Thus, a sub-0.7V 5-GHz direct-conversion receiver front-end based on the IEEE 802.11a specification is realized in this thesis, and it is implemented in 0.18-μm CMOS technology supported by TSMC. In

addition to no image problems, direct-conversion receivers perform high integration and low cost while low-voltage design reduces the total power consumption for entire receiver front-end.

The receiver in this thesis comprises a folded-cascode LNA for low-voltage operation, a DC-offset compensation circuit with band-pass filter integrated with the downconverter to suppress the DC offset voltages and achieve simple channel selection, and a quadrature VCO to drive the I/Q downconverters. Large devices are adopted in flicker-noise-sensitive and low-frequency, i.e. after downconversion, areas to mitigate flicker noise. Furthermore, all of the circuits in the receiver are differential topologies to reduce even-order distortion. For low-voltage operation, a few MOS devices with positive substrate bias are used to decrease the threshold voltage, resulting in adequate linearity.

1.4 Thesis Organization

Chapter 2 reviews the IEEE 802.11a standard and pertinent requirements of each stage in the receiver and describes the design issues of the building blocks. The circuit implementation and post-simulation results are also depicted. Chapter 3 summarizes the experimental results and discussions. Finally, conclusions and future works are described in Chapter 4.

CHAPTER 2

SUB-0.7V 5-GHz DIRECT-CONVERSION RECEIVER FRONT-END

This chapter describes the sub-0.7V direct-conversion receiver front-end, with a differential low-noise amplifier connected to a set of I/Q downconversion mixers, which are driven by a VCO with quadrature outputs. Fig. 8 shows the complete architecture of the receiver. With a DC-offset compensation circuit integrated into each downconverter, it is able to mitigate the effect of DC offsets, resulting from LO leakage and signal feedthrough.

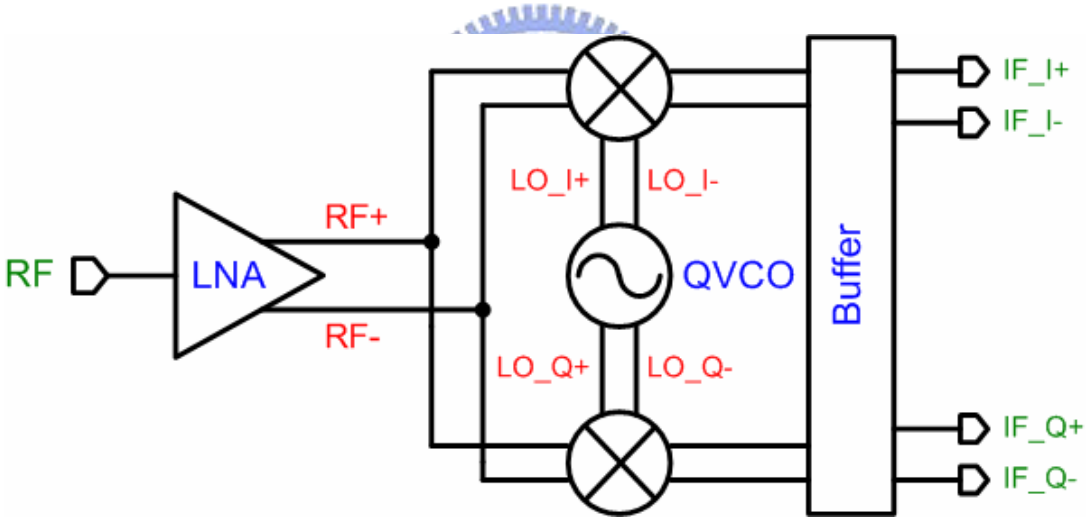


Fig. 8 Receiver architecture.

2.1 IEEE 802.11a PHY Specification and Link Budget

The 802.11a standard specifies operation over a generous 300-MHz allocation of spectrum in the 5-GHz unlicensed national information infrastructure (UNII) band. Over the 300-MHz allowance, there is a contiguous 200-MHz portion extending from 5.15 to 5.35 GHz, and a separate 100-MHz segment from 5.725 to 5.825 GHz. These allocations are further split

into three equal domains distinguished by allowable transmit powers. The bottom 100-MHz domain is restricted to a maximum output power of 40 mW, the next 100 MHz to 200 mW, and the top 100 MHz to a maximum of 800 mW, as indicated in Fig. 9. Furthermore, unlike 802.11b using DSSS modulation, 802.11a employs orthogonal frequency division multiplexing (OFDM) modulation, a technique that uses multiple carriers to mitigate the effect of multipath. Illustrated in Fig. 9, the 802.11a standard supports a channel bandwidth of 20 MHz, with each channel being an OFDM modulated signal consisting of 52 subcarriers. Each of the subcarriers can be a BPSK, QPSK, 16-QAM, or 64-QAM signal [1]. Therefore, the 802.11a standard provides nearly 5 times the data rate and as much as 10 times the overall system capacity as 802.11b WLAN system.

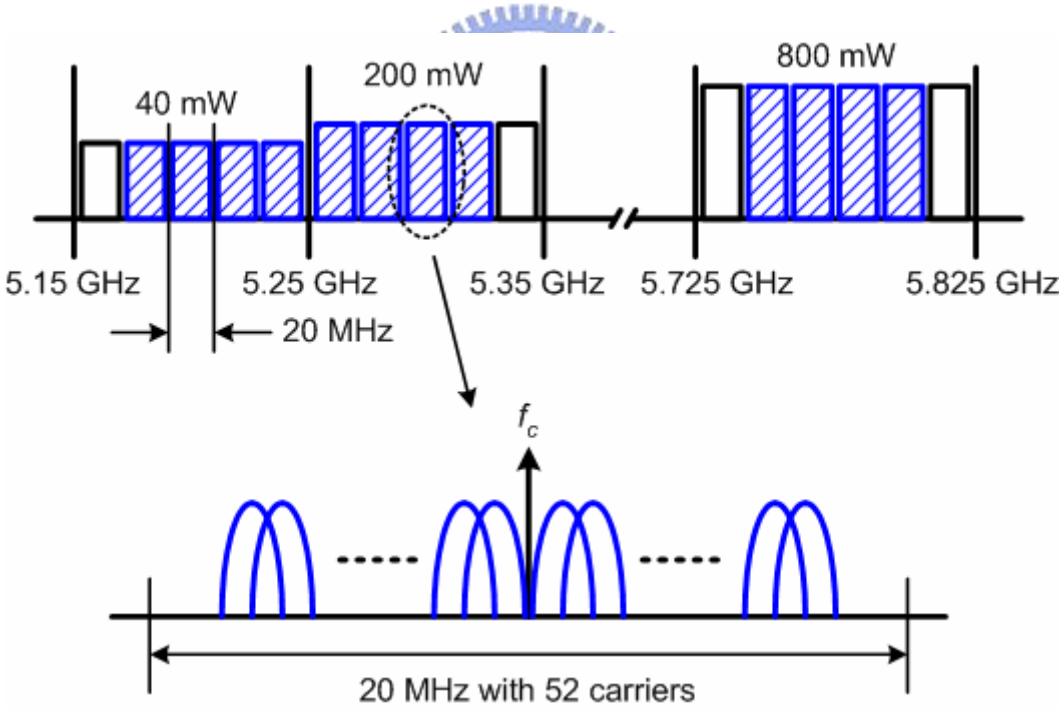


Fig. 9 Channel allocation of the IEEE 802.11a standard within the UNII band.

In order to determine the precise target values of performance requirements for an 802.11a WLAN receiver, we reduce the specification set to frequency range, noise figure (NF), and maximum input signal level (or input-referred 1-dB compression point). For frequency

range, it is often acceptable to cover only the lower 200-MHz band because the upper 100-MHz domain is not contiguous with the allocation and universally unavailable; consequently, we choose 5.15-5.35 GHz as the frequency band of receiver. About noise figure, strictly speaking, it is a function of data rate; however, it would be cumbersome to specify individual noise figures for each possible data rate. As a result, the 802.11a specification simply recommends a noise figure of 10 dB with 5-dB implementation margin to accommodate the worst-case situation [1]. Besides, the specification also specifies -30 dBm as the maximum input signal that a receiver must accommodate (for a 10% packet error rate). Based on this approximation, we target a worse-case input-referred 1-dB compression point of -30 dBm. In conclusion, the summary of performance requirements of a receiver front-end for 802.11a standard is listed in Table II.

Table II IEEE 802.11a Receiver Requirements

Frequency band	5.15-5.35 GHz
Channel bandwidth	20 MHz
Channel number	8
Sensitivity	-65 dBm (for 54 Mbits/s)
Max. RX input power	-30 dBm
Noise Figure	15 dB

When designing a radio receiver, it is often desirable to specify the performance of individual blocks (amplifiers, mixers, and filters) separately to simplify the design task. The system performance is then determined by the cascade connection of these individual blocks; therefore, it is significant to understand the effects of cascading on figure-of-merit, such as noise figure and linearity. It is known as Friis's Equation [35] that the noise figure of a

cascade of signal blocks can easily be shown to be

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \cdots A_{p(m-1)}}, \tag{2.1}$$

where NF_m is the noise figure of the mth stage evaluated with respect to the driving impedance of the preceding stage and A_{pm} is the power gain of the mth stage. Similarly, we can evaluate the linearity of a cascade of signal blocks. The production of intermodulation distortion in each stage is complicated; hence, with some simplifying assumption, we can obtain the following equation [3]

$$\frac{1}{A_{IP3}^2} \approx \frac{1}{A_{IP3,1}^2} + \frac{A_{p1}^2}{A_{IP3,2}^2} + \frac{A_{p1}^2 A_{p2}^2}{A_{IP3,3}^2} + \cdots, \tag{2.2}$$

where $A_{IP3,n}$ denotes the input-referred third-order intercept point of the nth stage and A_{pn} is the power gain of the nth stage.

Based on the preceding analysis, the design target of each stage in receiver front-end would be evaluated entirely, and the overall design target set is summarized in Table III.

Table III Design Target Set of Receiver

Receiver	Supply voltage	0.6 V
	Gain	20 dB
	Noise figure	< 15 dB
	$P_{1\text{-}dB}$	> -30 dBm
	DC offset	< 10 mV
	Power Consumption	< 10 mW
LNA	Gain	20 dB
	Noise figure	< 5 dB
	$P_{1\text{-}dB}$	> -15 dBm
Downconverter	Gain	0 dB
	Noise figure	< 24 dB
	$P_{1\text{-}dB}$	> -8 dBm
VCO	Tuning range	5.15-5.35 GHz

2.2 Downconverter with DC-Offset Compensation

In a radio receiver, downconverters perform frequency translation by multiplying a RF signal and an LO signal. The downconverter proposed in this thesis is available to be applied to direct-conversion receivers; furthermore, it improves DC offsets and LO leakage problems effectively due to a DC-offset compensation circuit integrated. It downconverts the differential RF signal from 5.25 GHz to an IF signal of around 10 MHz.

2.2.1 Operational Principle

The block diagram of the modulator, which forms the modulation function, is shown in Fig. 10. The single-stage modulator is modified from a conventional two-stage modulator [36].

There are four combiners, two adders and one subtracter in the modulator. Suppose the output signal C_i is expressed as

$$C_i = h_0\left(h_1 A_i + h_2 B_i + h_3\right)^2. \tag{2.3}$$

In this equation, C_i is the output of the combiner $COMB_i$ ($i = 1 \sim 4$), A_i and B_i are the inputs to $COMB_i$, and h_0 to h_3 are constants. In addition, the input signals (V_1+v_1, V_1-v_1, V_2+v_2, V_2-v_2, where V_1 and V_2 are input common-mode DC voltage; v_1 and v_2 are input AC signals.) are introduced into these four combiners and the output is taken as the difference of the outputs of two adders (ADD_1 and ADD_2) by using subtracter (SUB_1). It can be shown that

$$V_o = 8h_0h_1h_2v_1v_2. \tag{2.4}$$

From Eq. (2.4), it is indicated that the circuit structure in Fig. 10 performs the function of modulation.

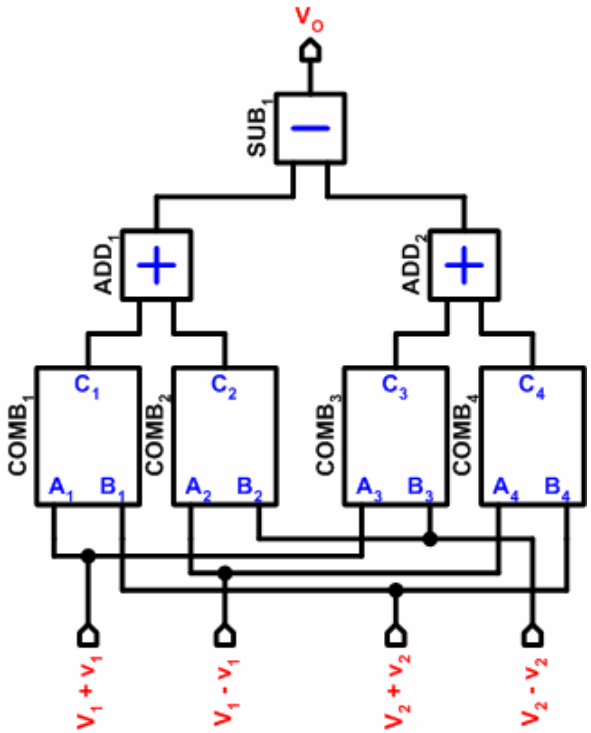


Fig. 10 Block diagram of modulator.

Since MOS transistor is basically a square-law device, the second-order transfer function in Eq. (2.3) can be easily implemented with the MOS transistors [37], [38]. Fig. 11 shows the combiner circuit which is cascoded by the two MOS transistors M_a and M_b. The two input signals V_1 and V_2 are introduced to the gate of the MOS transistors M_a and M_b, respectively. The MOS transistor M_b, which is operated in triode region, provides source degeneration of the MOS transistor M_a so that the linearity of M_a is improved. Therefore, the transfer characteristic of the combiner in Fig. 11 can be derived by the drain current equations of M_a and M_b, which are operated in saturation region and triode region, respectively. Neglect the terms with smaller value, the output current I_o can be expressed as

$$I_o \approx K_a\left[\left(1-K_a\right)V_1-\frac{1}{2}K_bV_2+\left(K_a-1\right)V_{Ta}+\frac{1}{2}K_bV_{Tb}\right]^2, \tag{2.5}$$

where $K_a=\mu_0\left(C_{ox}/2\right)\left(W/L\right)_a$ ($K_b=\mu_0\left(C_{ox}/2\right)\left(W/L\right)_b$) is the transconductance parameter of M_a (M_b), μ_0 is the effective surface carrier mobility, C_{ox} is the gate oxide capacitance per unit area, $(W/L)_a$ ($(W/L)_b$) is the ratio of the channel width and length of M_a (M_b), and V_{Ta} (V_{Tb}) is the threshold voltage of M_a (M_b). Hence, it is obvious that Eq. (2.5) can perform the function of Eq. (2.3).

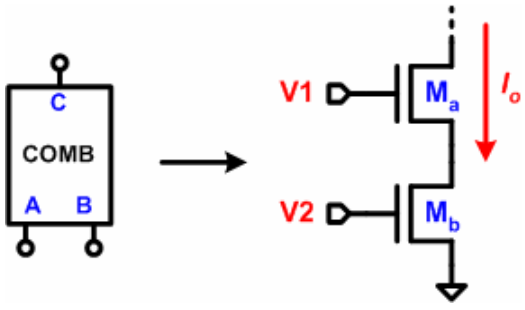


Fig. 11 Realization of combiner.

The complete modulator shown in Fig. 10 can be formed by connecting the combiners presented in Fig. 11. The resultant circuit diagram is indicated in Fig. 12, where Z_1 and Z_2 are

impedance elements. Assume that the value of the impedance Z_1 and Z_2 is Z; the MOS transistors M_{ai} (M_{bi}) (i = 1 ~ 4) are identical with the same K_a (K_b), also, the threshold voltage of all MOS transistors are identical. Thus, it is derived that

$$V_o = 4ZK_aK_b\left(K_a - 1\right)V_1V_2\,. \tag{2.6}$$

As exhibited in this equation, the function of modulator is realized. If substitution is introduced as

$$V_1 = \cos\omega_{RF}t, \text{ and } V_2 = \cos\omega_{LO}t\,,$$

the input/output relation becomes

$$V_o = 4ZK_aK_b\left(K_a - 1\right)\left(\cos\omega_{RF}t \times \cos\omega_{LO}t\right). \tag{2.7}$$

The result corresponds to the IF output of I channel. By the same token, the Q-channel IF output is obtained if

$$V_1 = \cos\omega_{RF}t, \text{ and } V_2 = \sin\omega_{LO}t\,.$$

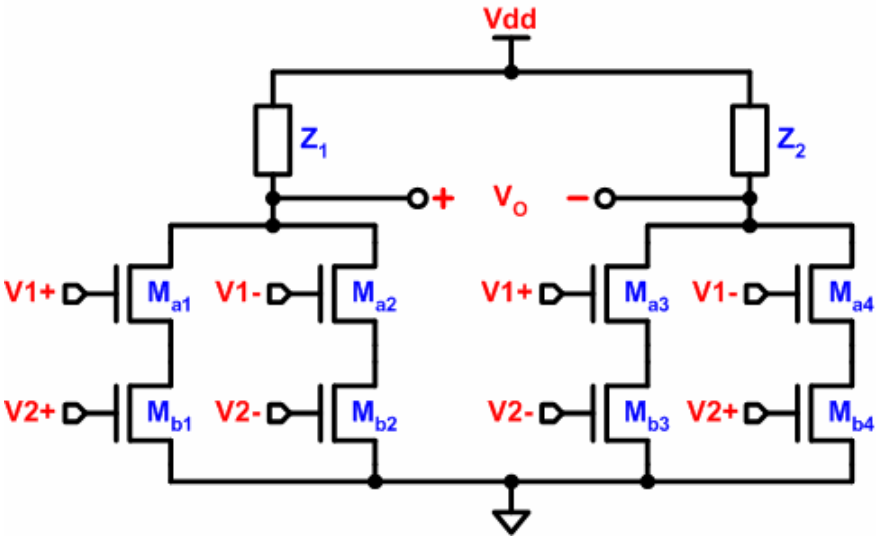


Fig. 12 Modulator circuit realized by two-input combiners.

2.2.2 DC-Offset Compensation

In the above-mentioned modulator, an extra current appears at the output terminal when self-mixing occurs. Illustrated in Fig. 13, the current flows into the load and bring a redundant voltage. The extra voltage affects the initial biased point of the modulator. For this reason, we infer that the modulator applied to direct-conversion receivers requires some means of offset cancellation. A feasible approach to moderate the offsets is applied [15]. Illustrated in Fig. 14, the PMOS transistor M_X, which is self-biased, acts the load of the modulator. The output voltage of the modulator is fed back to M_X through a large resistor R_m. When an additional current due to self-mixing appears and flows into M_X, since the V_{GS} of M_X is equal to V_{DS}, the drain current can be written based on the square-law that

$$I_D = K\left(V_{DS_X} - V_T\right)^2\left(1+\lambda V_{DS_X}\right), \tag{2.8}$$

where λ is the channel-length modulation parameter. With the same amount of offset current, V_{DS} is suppressed in cubic degree. As a result, the offset voltage of the output terminal of the modulator is reduced to few millivolts.

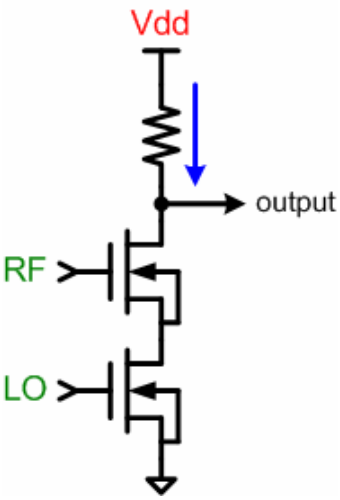


Fig. 13 Simple example of DC-offset generation.

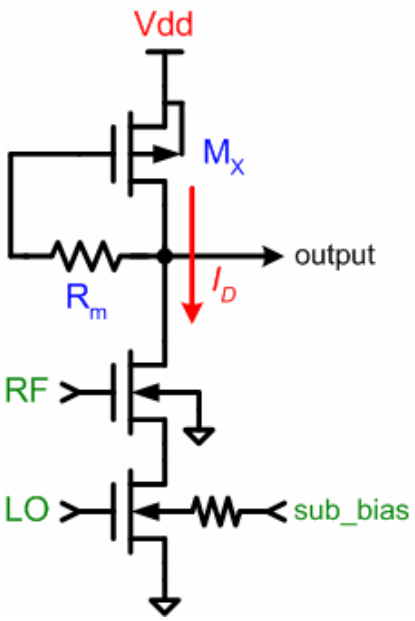


Fig. 14 DC-offset compensation circuit [15].

In most receivers, downconverters are usually connected to channel select filters in order to filter out unwanted bands because there are harmonic signals and a number of interferers in these bands. Besides, the 802.11a standard specifies no subcarriers in the center frequency of each channel, resulting in an empty spectrum of ±156.25 kHz after downconverted to baseband. If the low-corner frequency of band-pass filter falls below this value, the carried information of a whole channel remains intact. Thus, a band-pass filter with a low-corner frequency of 150 kHz and a bandwidth of 10 MHz is required. Nevertheless, a second-order LC band-pass filter whose low-corner frequency is around 150 kHz requires a very high quality factor. Also, there is a trade-off between loss and quality factor in typical filters. Therefore, a band-pass filter load integrated into the downconverter is applied [15].

Fig. 15 shows the band-pass filter load evolved from the DC-offset compensation load in Fig. 14. With the capacitor C_m connected to the gate of the PMOS transistor M_X, a second-order band-pass filter load is formed. Owing to the PMOS transistor biased in saturation region, the small-signal model is applied to derive the input impedance of the load as follows,

$$Z_{in} = \frac{R_m\left(C_m + C_{gd}\right)s + 1}{\left(R_m C_m C_{gd}\right)s^2 + \left(C_m + g_m R_m C_{gd}\right)s + g_m} \| r_o$$

$$\approx \frac{R_m C_m s + 1}{\left(R_m C_m C_{gd}\right)s^2 + \left(C_m + g_m R_m C_{gd}\right)s + g_m} \tag{2.9}$$

where C_{gd} is the gate-drain capacitance, C_{db} is the drain-body capacitance, r_o is the output resistance, and C_{gs} is combined with C_m. The second order band-pass filter load has two poles and one zero, which $\omega_{pole1} = \frac{g_m}{C_m}$, $\omega_{pole2} = \frac{1}{R_m C_{gd}}$, and $\omega_{zero} = \frac{1}{R_m C_m}$. It is obvious that R_m and C_m have to be much larger than $1/g_m$ and C_{gd}, respectively, to obtain a zero preceding two poles. For example, suppose a transconductance of 2 *mA/V* and a gate-drain capacitance of 120 *fF*, capacitor C_m and resistor R_m can be designed a value of 100 *pF* and 100 kΩ, respectively; thus, a zero is at 16 kHz and two poles are at 3.18 MHz and 13.26 MHz. After deciding the proper values of passive elements and the dimension of M_X, the pass bands of the band-pass filter load are able to fit the baseband spectrum specified by the 802.11a standard, shown in Fig. 16. In brief, a band-pass filter load integrated into the downconverter performs a simple channel selection in baseband. Without any g_m-C filters or complex multi-phase architecture, it adopts a few passive components to achieve DC-offset compensation and channel selection; also, it does not increase numerous power consumption compared with an extra channel select filter.

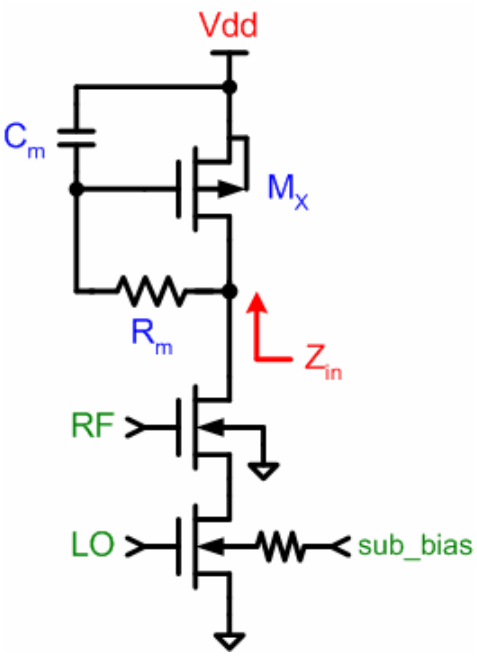


Fig. 15 A band-pass filter as the load of downconverter.

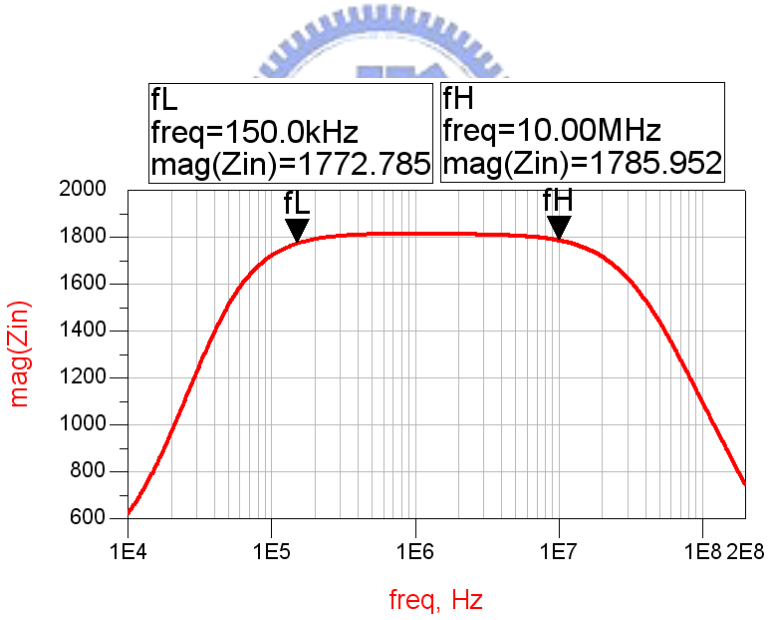


Fig. 16 Impedance of band-pass filter.

2.2.3 Circuit Implementation

The derivation of modulation function of the modulator in the previous subsection is based on the assumptions of ideal square-law. However, there are some nonideal effects in MOS transistors, such as channel-length modulation, velocity saturation and mobility

degradation. In a short-channel device, the drain current of MOS transistor can be represented as

$$I_D = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\frac{(V_{GS}-V_T)^2}{1+\left(\frac{\mu_0}{2v_{sat}L}+\theta\right)(V_{GS}-V_T)}$$

$$\approx \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\left[1-\left(\frac{\mu_0}{2v_{sat}L}+\theta\right)(V_{GS}-V_T)\right](V_{GS}-V_T)^2, \quad (2.10)$$

where v_{sat} denotes the saturation velocity, μ_0 denotes the low-filed mobility, and θ is a fitting parameter being approximately equal to $(10^{-7}/t_{ox})\text{V}^{-1}$ [39]. Therefore, according to Eq. (2.10), Eq. (2.6) is revised to the following form:

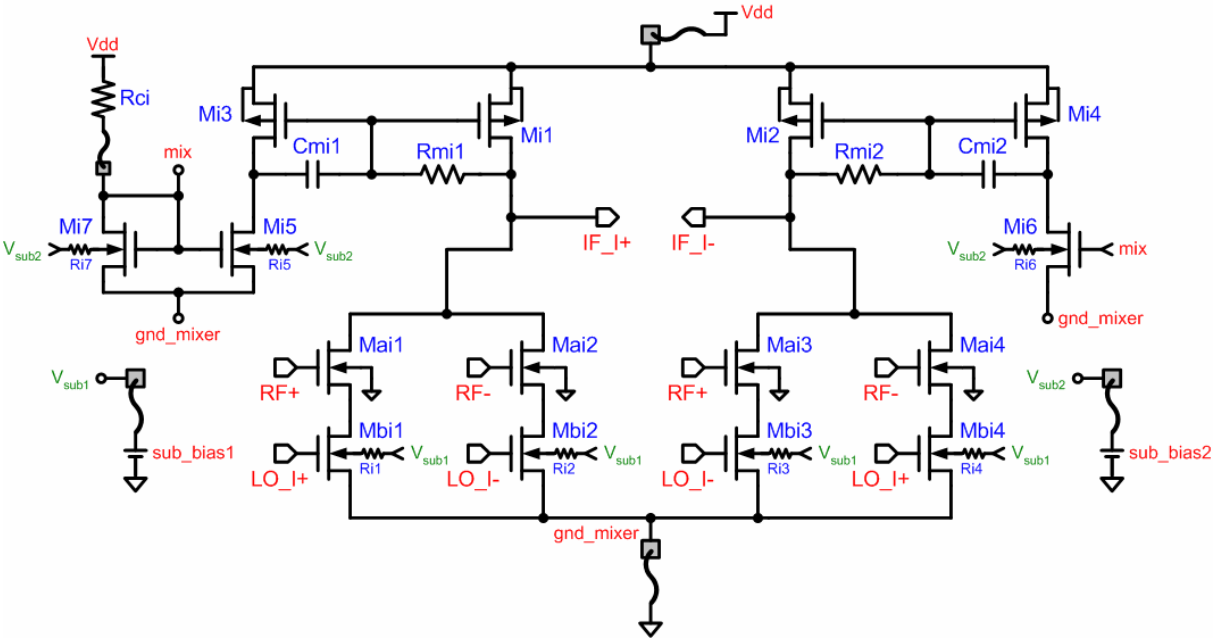
$$V_o = 4ZK_a'K_b'\left(K_a'-1\right)V_1V_2 \quad (2.11)$$

with $K_a' = 1-\left(\mu_0/2v_{sat}L_a+\theta\right)\left(V_{GS_a}-V_{T_a}\right)$, and $K_b' = 1-\left(\mu_0/2v_{sat}L_b+\theta\right)\left(V_{GS_b}-V_{T_b}\right)$. From Eq. (2.11), it is verified that if overdrive voltage is sufficiently small, the combiner realizes the modulation function even though short-channel devices are adopted.

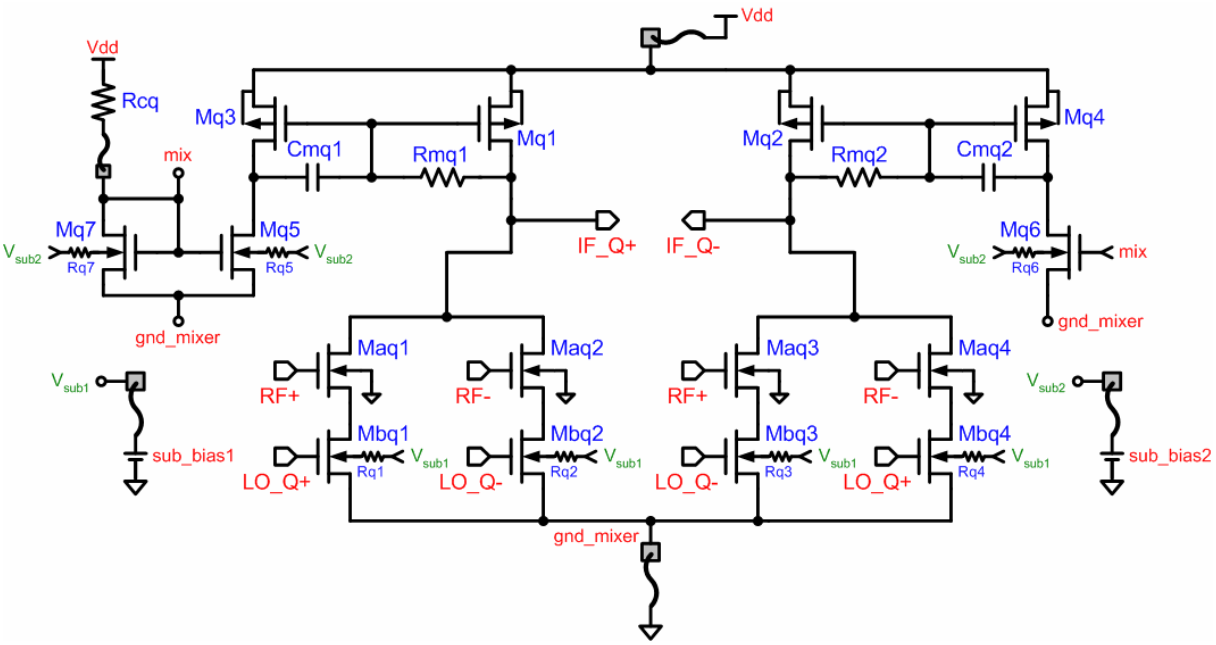
Fig. 17 presents the designed downconverter, which is divided into *I*-channel and *Q*-channel implementations, and Table IV lists the relative parameters. RF signal and LO signal are introduced into the gate of the MOS transistors *Mai#* and *Mbi#* (*Maq#* and *Mbq#*), respectively, after re-biased. In order to ensure *Mbi#* (*Mbq#*) in triode region, positive substrate bias is adopted to reduce the threshold voltage. The DC-drop of a combiner is around 100 mV; therefore, the downconverter is achievable under 0.6-V supply voltage. To allow an adequate swing in the downconverter, a conversion gain of about 0 dB is designed for better linearity.

Because the low-corner frequency of the band-pass filter shown in Fig. 15 is approximately decided by R_m and C_m product, C_m would cost a large area if R_m is small, and

vice versa. In order to economize on chip area, C_m is replaced with, for example, *Cmi1*, *Rmi1* and *Mi3* in Fig. 17(a). Based on Miller effect, *Cmi1* can be magnified and thus decreasing the area. The resultant value of capacitance increases around 5 times compared to original capacitor. *Rmi#* (*Rmq#*) is implemented by HRI (high resistor implant) resistor due to higher resistance. The current source composed of *Mi5, Mi6* and *Mi7* (*Mq5, Mq6* and *Mq7*) provides DC bias current for the band-pass filter load, and all of these NMOS transistors are also positive-substrate-biased in order to decrease their threshold voltages. It is noted that the bulk-source and bulk-drain junctions of a positive-substrate-biased MOS transistor have to be always off in order to ensure that no large currents flow into these junctions or else extra power dissipation is generated. Besides, larger-dimensioned devices are adopted in low-frequency, i.e. after downconversion, areas to mitigate flicker noise and alleviate the effect of device mismatch.



(a)



(b)

Fig. 17 (a) I-channel and (b) Q-channel downconverter with DC-offset compensation circuits.

Table IV Detailed Parameters of the Downconverter

Mai1-Mai4, Maq5-Maq4	10 μm / 0.25 μm	Ri1-Ri7, Rq1-Rq7	10 kΩ
Mbi1-Mbi4, Mbq5-Mbq4	10 μm / 0.25 μm	Rmi1, Rmi2, Rmq1, Rmq2	200 kΩ
Mi1, Mi2, Mq1, Mq2	300 μm / 0.5 μm	Cmi1, Cmi2, Cmq1, Cmq2	20 pF
Mi3, Mi4, Mq3, Mq4	115 μm / 0.5 μm	Rci, Rcq	2 kΩ
Mi5-Mi7, Mq5-Mq7	15 μm / 0.5 μm		

2.3 Folded-Cascode Low-Noise Amplifier

In a communication system, LNA, one of receiver front-end circuits, is located on the receiving path of transceiver. The main functions are amplifying the RF signal received from antenna, providing input impedance matching, and contributing so minimum noise that the system can operate well.

2.3.1 Design Considerations

Input matching is an important consideration for connection with external components. Described in microwave theory, signal is partially reflected as soon as passing through an interface between two different mediums. In other words, in circuits, two stages with unequal input/output impedances stand for two different mediums. Hence, to minimize signal reflection, input impedance of a LNA has to be designed to 50 Ω (the characteristic impedance in wireless communication system).

A feasible method of creating an input resistance of 50 Ω in a common-source amplifier is inductive source degeneration, which is illustrated in Fig. 18. To simplify the analysis, consider a MOS model that includes only a transconductance and a gate-source capacitance. In the case, it is not hard to show that the input impedance has the following form:

$$Z_{in} \approx \frac{g_m}{C_{gs}} L_s + j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right). \tag{2.12}$$

From Eq. (2.12), it is realized that source inductor can efficiently eliminate the imaginary part; therefore, proper choice of g_m, L_s, and C_{gs} yields a 50-Ω resistance.

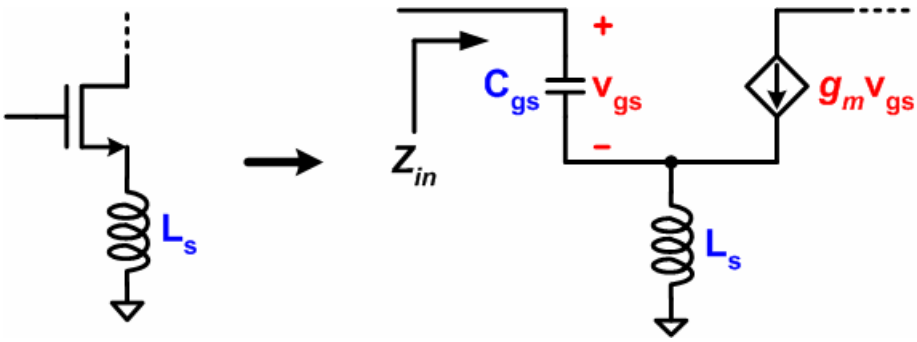


Fig. 18 Input impedance of common-source with inductive source degeneration.

Practically, input matching is also affected by other inevitable factors. In general, there are parasitical capacitances existing on I/O pads, furthermore, if a chip under test is bonded on

a printed circuit board for measurement, bond-wires contribute parasitical inductance. Take these parasitics into account, a revised model with parasitics of a pad and a bond-wire is shown in Fig. 19. It is convenient to use Smith chart to decide proper value of C_{pad} and L_{bw} so that the input impedance Z_{in} can achieve 50 Ω.

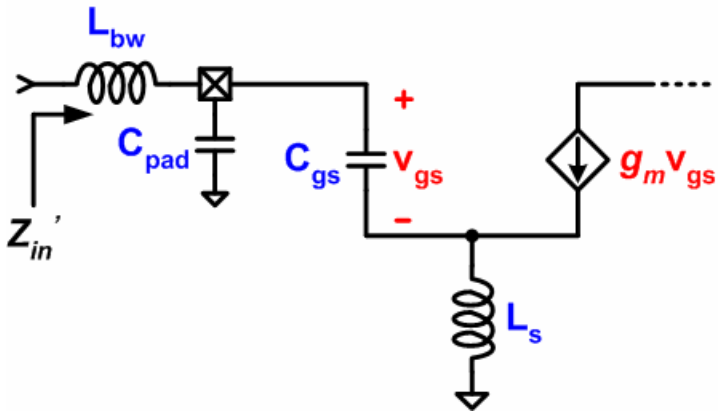


Fig. 19 Revised model of input impedance.

Another important issue to LNA is noise performance. We are going to analyze the noise performance of the LNA, which is common-source topology with inductive source degeneration, and design an optimum dimension of the MOS transistor to obtain minimum noise contribution.

The noise figure of the LNA can be computed by analyzing the circuit shown in Fig. 20. In this circuit, R_s and R_g represent the resistance of voltage source and gate resistance, respectively; $\overline{i_d^2}$ represents the channel thermal noise of the device. Besides, if the device is biased so that the channel is inverted, fluctuations in the channel charge will induce a physical current in the gate due to capacitive couple [40]. It is called "induced gate noise" and represented $\overline{i_g^2}$ in Fig. 20.

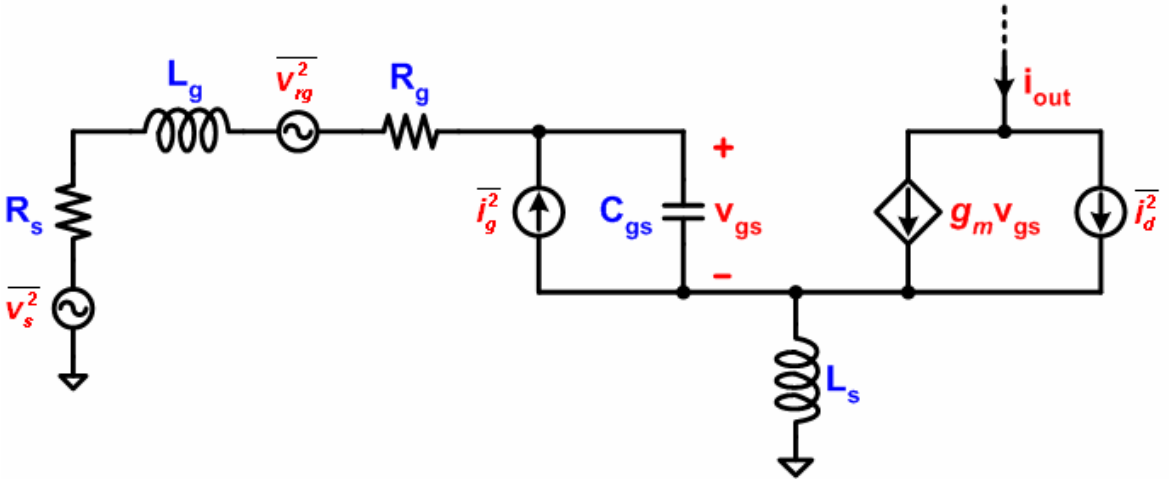


Fig. 20 Noise model of input stage.

Analysis based on this circuit neglects the noise contribution of subsequent stages to the amplifier; thus, the noise figure formulates as [41]:

$$NF = 1 + \frac{\gamma \omega_0 L}{3 v_{sat}} P(\rho, P_D) \tag{2.13}$$

with

$$\rho = \frac{V_{od}}{L \varepsilon_{sat}}. \tag{2.14}$$

In this equation, γ is the coefficient of channel thermal noise, L is the channel length, v_{sat} and ε_{sat} are the saturation velocity and the velocity saturation field strength, respectively, V_{od} is the overdrive voltage, and P_D is the power consumption. Moreover, $P(\rho, P_D)$ denotes a high-order polynomial. The detailed contents are derived in [41]. Besides, consider a simple second-order model of the MOSFET transconductance can be employed which accounts for high-field effects in short-channel devices. Assume that I_d has the form [42]

$$I_d = W C_{ox} v_{sat} \frac{V_{od}^2}{V_{od} + L \varepsilon_{sat}}. \tag{2.15}$$

Having established an expression for I_d, we can formulate the power consumption of the

amplifier as follows,

$$P_D = V_{dd} I_d = V_{dd} W C_{ox} v_{sat} \frac{V_{od}^2}{V_{od} + L\varepsilon_{sat}}. \tag{2.16}$$

As Eq. (2.13) and (2.16) expressed, they reveal that channel width is an implicit function of noise figure.

Consequently, the decidable parameters are V_{dd}, P_D, W and L. An alternative method of optimization fixes the power consumption and adjusts ρ to find the minimum noise figure; also, minimum channel length and 0.6-V supply voltage are chosen in 0.18-μm CMOS technology. In conclusion, Fig. 21 indicates the relation between channel width and noise figure with fixed power consumption each curve. It is convenient to decide proper channel width with restricted power consumption so that the optimum noise figure is obtained.

Transconductance of input-stage MOS transistor and load impedance dominate the voltage gain in common-source amplifier. The transconductance is fixed while the dimension of MOS transistors and bias condition has been decided for input matching and noise optimization. Hence, sufficiently high load impedance or other advanced circuit structure with identical input stage is then expected. Besides, in RF circuits, LC-tank is a common choice for load if fabrication technology is able to provide inductors with adequate quality factors because loads with higher quality factor cause higher gain. On the other hand, although high-Q load increases gain effectively, linearity is contrarily degraded. An LNA operating nonlinearly causes intermodulation while signals with various frequencies are received simultaneously; as a result, the frequencies of other undesired signals output from LNA are close to that of received signals. Here is an illustration in Fig. 22 for example. The LNA receives two signals at ω_1 and ω_2, respectively, and then outputs signals at ω_1, ω_2, $2\omega_1$-ω_2 and $2\omega_2$-ω_1. If the difference between ω_1 and ω_2 is small, the signals at $2\omega_1$-ω_2 and $2\omega_2$-ω_1 appear in the vicinity of ω_1 and ω_2. As the power of ω_1 and ω_2 increases, the power of $2\omega_1$-ω_2 and

$2\omega_2$-ω_1 grows up in cube. Thus, the additional signals may fall in adjacent channels and corrupt normal receiving.

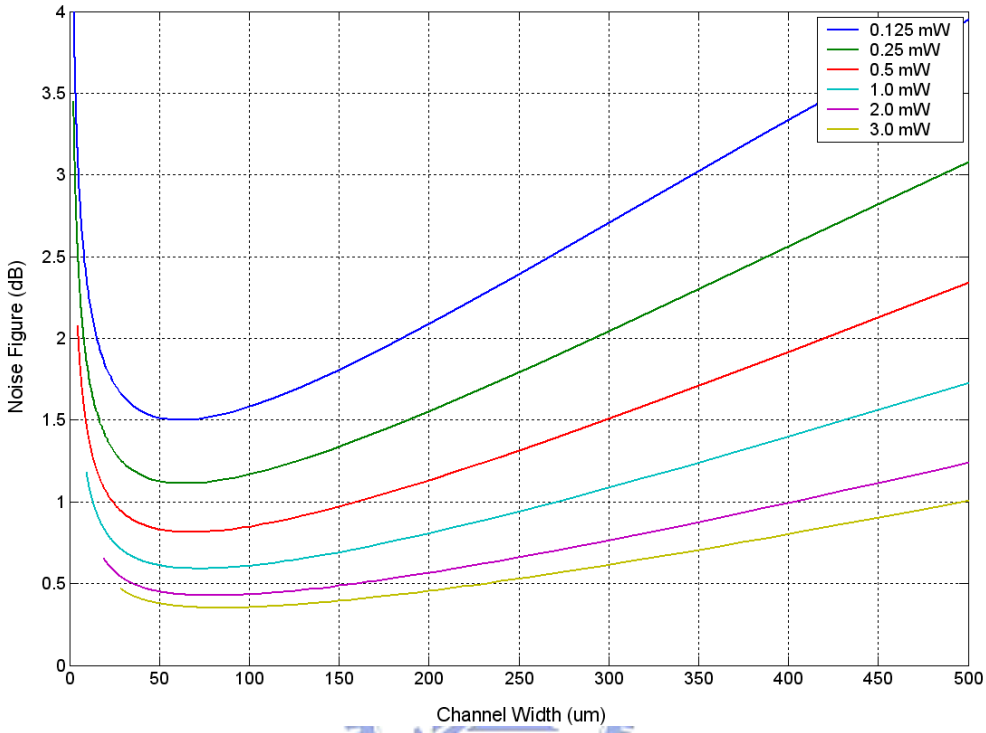


Fig. 21 Minimum NF curves related to channel width and power consumption.

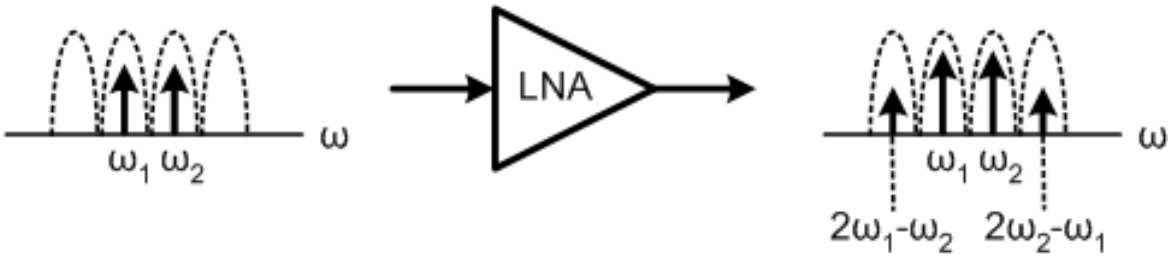


Fig. 22 Intermodulation phenomenon [3].

2.3.2 Circuit Implementation

In addition to the considerations mentioned in the previous subsection, the most important issue in this thesis is low-voltage operation. With the targeted supply voltage down

to 0.6 V, there are limited numbers of suitable LNA topologies. Conventional cascode amplifiers require high supply voltage headroom, while single transistor amplifiers are prone to instability problem. In order to operate under a very low supply voltage, a folded cascode structure is adopted since it eliminates one level of transistor stacking [43].

Fig. 23 shows the schematic of differential LNA in the receiver, and Table V lists the detailed parameters of each device. In this schematic, MOS transistors *Mn1* and *Mn2*, whose dimensions are decided by the illustration in Fig. 21 for low-noise consideration, act as common-source amplifiers; *Mp1* and *Mp2*, which are common-gate amplifiers, perform current buffers with load inductors *Ld1* and *Ld2*. As a result of this circuit topology, more voltage headroom can be used to bias the MOS transistors in saturation region, leading to an improved linearity. Also, reverse isolation is enhanced as conventional cascode structure behaves. Inductors *Lc1* and *Lc2* behave as DC current sources. They provide the necessary DC bias current without requiring extra voltage headroom, while presenting high impedances to the RF signals when resonating with the parasitic capacitances of the MOS transistors. Besides, an additional advantage is to nullify the parasitic capacitances of the MOS transistors, resulting in an improvement of the noise figure [44]. Due to a specific quality factor of on-chip spiral inductor, the impedance of the inductor is limited at resonance compared to the impedance seen at the sources of the PMOS transistors *Mp1* and *Mp2*. Thus, a portion of RF signals will be lost to the tank on account of current division. Finally, inductors *Ls1* and *Ls2* are used for matching the input resistance as mentioned in the previous subsection.

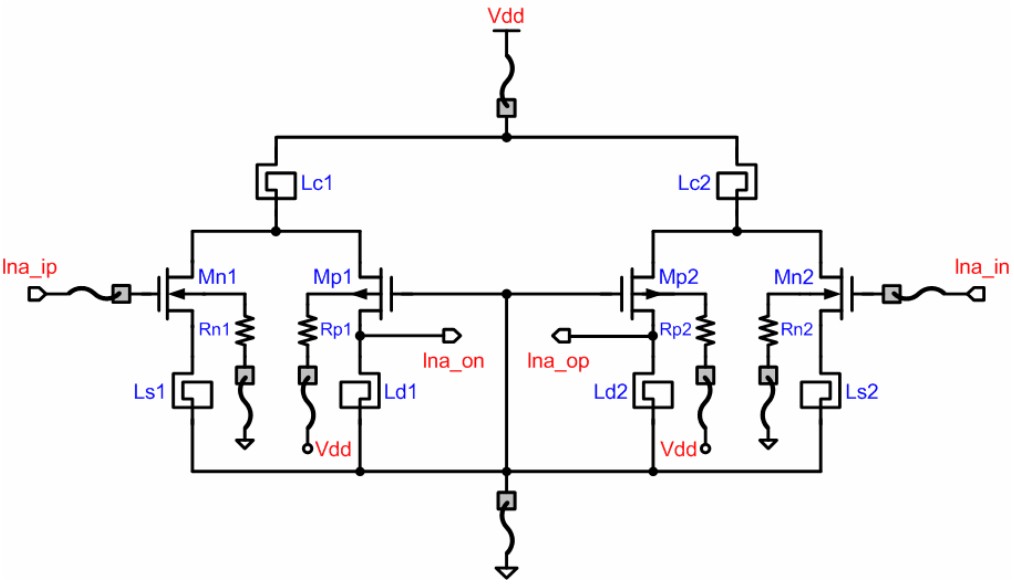


Fig. 23 Folded-cascode LNA.

Table V Detailed Parameters of the LNA

Mn1, Mn2	50 μm / 0.18 μm
Mp1, Mp2	115 μm / 0.18 μm
Ls1, Ls2	1 nr (0.805 nH)
Lc1, Lc2	5.5 nr (14.5 nH)
Ld1, Ld2	2 nr (2.04 nH)
Rn1, Rn2, Rp1, Rp2	10 kΩ

2.4 Quadrature Voltage-Controlled Oscillator

A basic LC oscillator usually comprises a resonator which includes an inductor, a capacitor and a negative resistance, shown in Fig. 24. Following this design concept, except a spiral inductor, we introduce a varactor and a cross-coupled pair into the resonator to tune the oscillated frequency and form a negative resistance, respectively. Moreover, in order to generate quadrature-phase signals, a circuit structure based on even-stage ring oscillator is introduced [45]. Combining two resonators and two inverters, a quadrature VCO is

implemented. The conceptual diagram of quadrature VCO is presented in Fig. 25, where INV_I and INV_Q are two identical inverters which are common-source topology. Finally, the realization of whole quadrature VCO circuit is shown in Fig. 26 and its parameters are listed in Table VI.

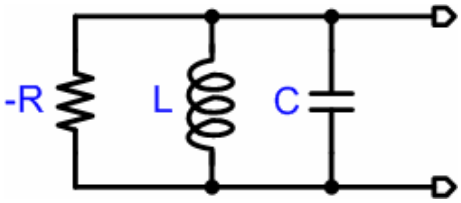


Fig. 24 General resonator.

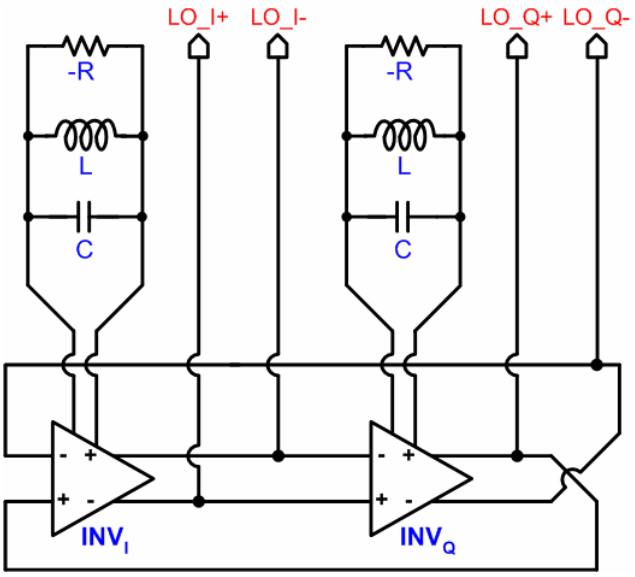


Fig. 25 Conceptual diagram of quadrature VCO.

For low-voltage consideration, the two LC-tanks perform not only resonators but also loads. Thus, the output voltage swing can exceed supply voltage to achieve sufficiently large amplitude and keep sinusoidal waveform. Besides, there are four output buffers, i.e. *Mx1-Mx4*, which are open-drain topologies, following each quadrature output in order to measure the performance of the quadrature VCO individually.

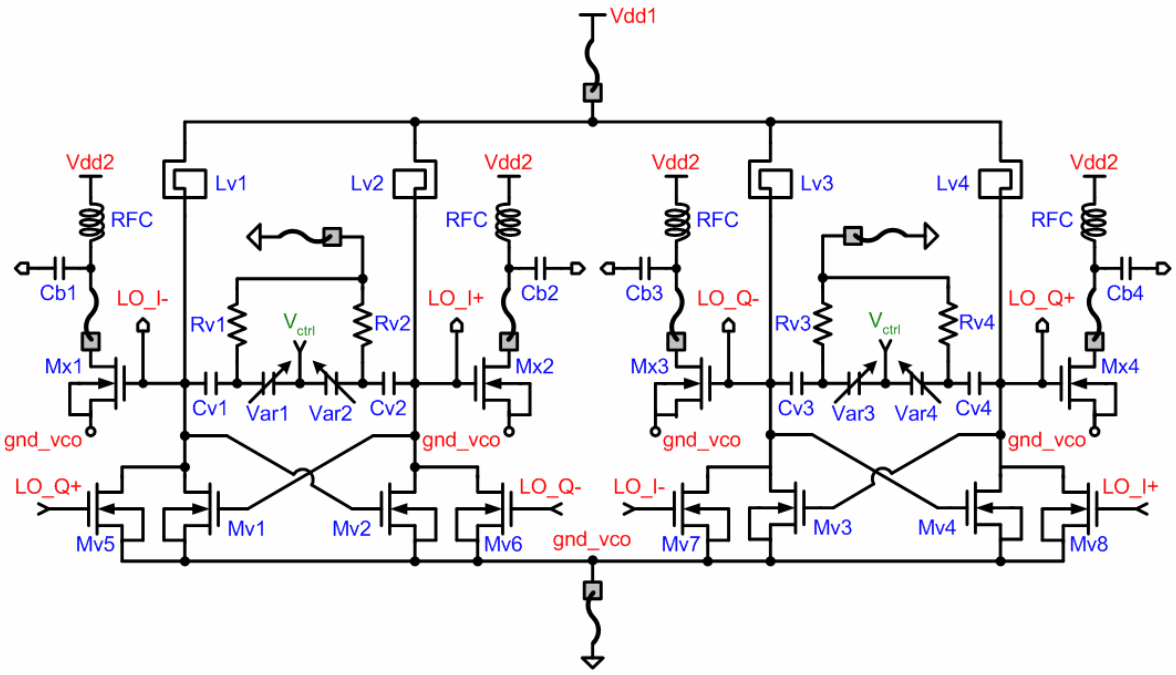


Fig. 26 Quadrature VCO.

Table VI Detailed Parameters of the Quadrature VCO

Mv1-Mv8	32.5 μm / 0.18 μm
Mx1-Mx4	50 μm / 0.18 μm
Rv1-Rv4	5.4 kΩ
Cv1-Cv4	0.6 pF
Lv1-Lv4	1.25 nr (1.1 nH)
Cb1-Cb4	5 pF

2.5 Receiver Realization

0.6-V power supply is no doubt a challenge in 0.18-μm technology in many conventional circuit structures. The numbers of cascoded MOS devices, in practice, have to be kept less than two, i.e. a NMOS cascoded with a PMOS. However, it only confirms that all MOS devices are able to operate normally under required DC status. Another obstacle is voltage

swing. Fortunately, a character of inductor can be applied to overcome the swing restriction. RF circuits usually apply inductor in order to acquire proper loads. An inductor provides sufficiently high load impedance while resonating with an equivalent parallel capacitor. In addition, even if one terminal is connected to power supply, voltage swing of the other terminal can exceed the supply voltage.

A buffer as output stage follows the downconverter for measurement. It comprises four common-source amplifiers with complementary loads, following the four output terminals of the downconverter respectively. Fig. 27 presents the buffer of the *I*-channel, which is identical to the *Q*-channel, and Table VII lists the relative parameters. According to Eq. (2.1) and (2.2), the performance of receiver is affected by each stage in the cascade. In order to reduce the injury to linearity, class-A topology is adopted to implement the output buffer with its power supply are 1.25 V and -0.55 V. Moreover, the downconverted signals applying to the input terminals of the output buffers are not re-biased in order to measure the exact DC offset voltage. Similarly, the output terminals of the output buffers are not connected to DC-blocking capacitors. The measurement for DC offset is installed by connecting the output terminals to off-chip resistors. Finally, the frequency response of the output buffer is shown in Fig. 28, where a voltage gain of 0 dB and a bandwidth of 10 MHz are exhibited.

All inductors employed are spiral inductors made of top thick metal, varactors are NMOS varactors, resistors are HRI resistors, and capacitors are MIM (metal-insulator-metal) capacitors. To avoid body effect, all NMOS devices contain deep n-wells for equal voltage potential between respective source terminals and bulk terminals. All device models are supported by TSMC.

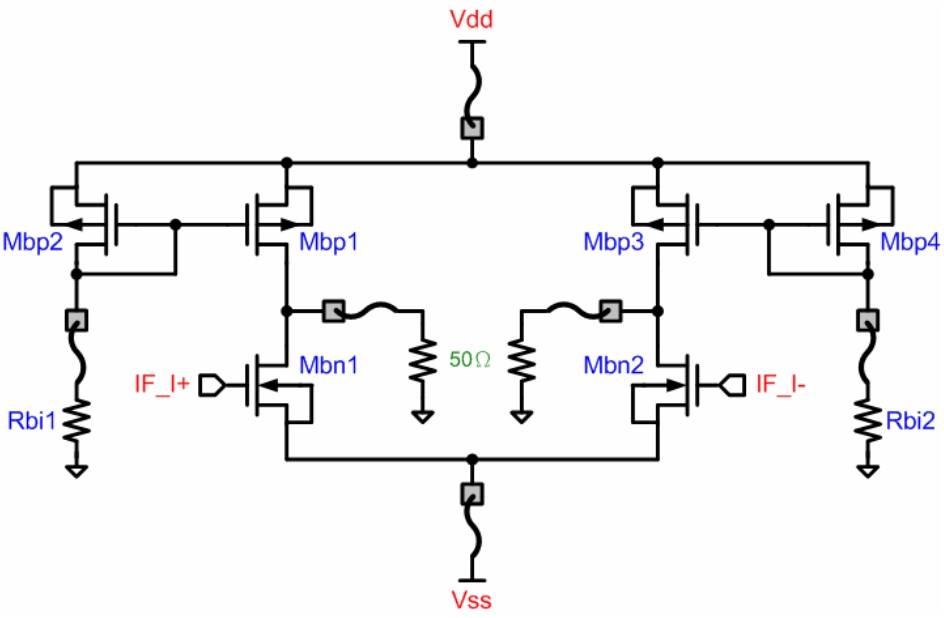


Fig. 27 I-channel output buffer.

Table VII Detailed Parameters of the Output Buffer

Mbn1, Mbn2	140 μm / 0.35 μm
Mbp1, Mbp3	180 μm / 0.18 μm
Mbp2, Mbp4	75 μm / 0.18 μm
Rbi1, Rbi2	600 Ω

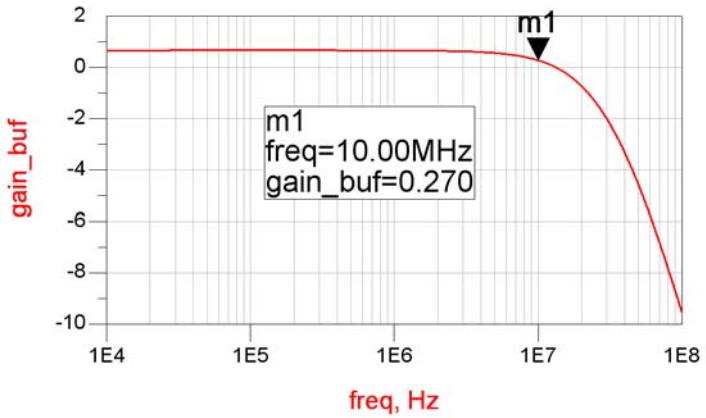


Fig. 28 Frequency response of the output buffer.

2.6 Simulation Results

Post-simulation is completed by HPICE for transient analysis and ADS simulator for other simulations with process parameters of TSMC 0.18-μm mixed signal 1P6M salicide 1.8V/3.3V RF SPICE models. The following are the post-simulation results of all circuits constructing the receiver.

- **LNA**

LNA, locating on the first stage of the receiver, provides input matching, voltage gain and low-noise contribution for the receiver in a specific frequency band. Fig. 29 presents the simulated input matching (S11) of lower than -10 dB in a frequency range of 5.05 GHz to 5.45 GHz. Fig. 30 exhibits that the voltage gain is larger than 20.5 dB in the desired band. Fig. 31 is the simulation result of noise figure related to frequency. If the dimensions of the input MOS device are optimized for noise, the resultant noise figure is close to the minimum noise figure. To evaluate the linearity performance, two-tone test is introduced [3]. Two near-frequencyed signals are introduced into the LNA and then the LNA outputs signals of first order and third order, which is mentioned in subsection 2.3.1. Fig. 32 plots the power relation of the two terms on a logarithmic scale. The horizontal coordinate of the two-curved intersection point, called IIP3 (input third intercept point), is a parameter for linearity estimation. Also, 1-dB compression point ($P_{1\text{-dB}}$), another parameter for linearity estimation, is obtained from Fig. 32.

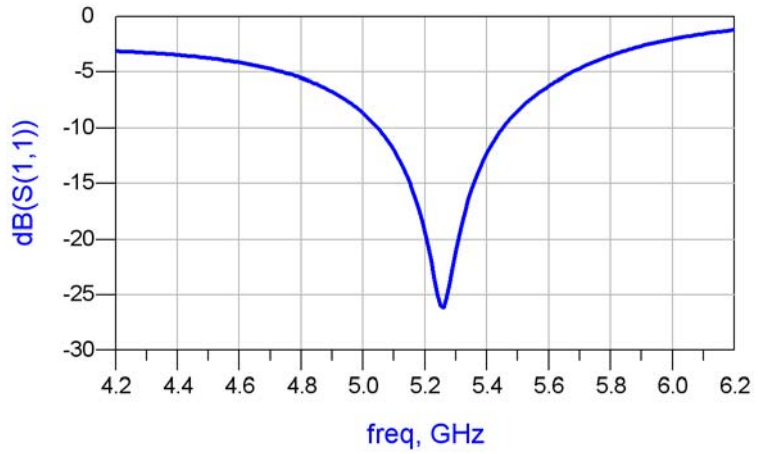


Fig. 29 Simulated S11 of the LNA.

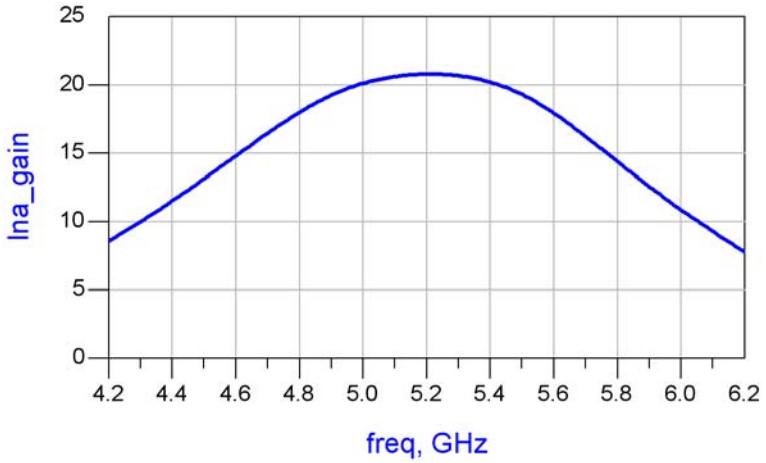


Fig. 30 Simulated voltage gain of the LNA.

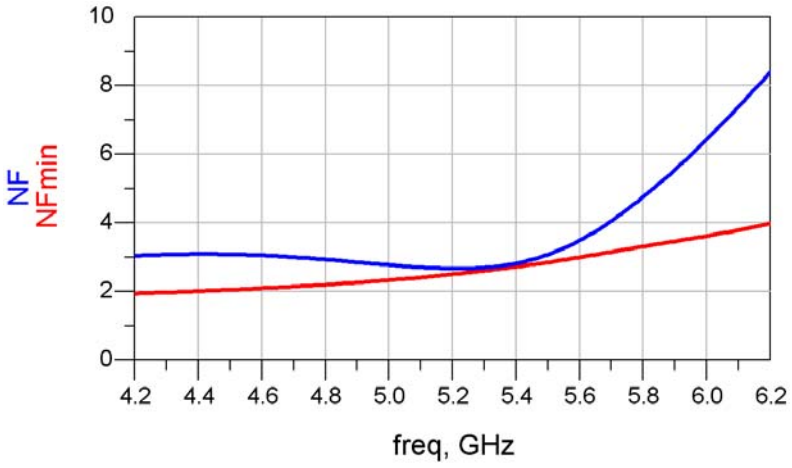


Fig. 31 Simulated noise figure of the LNA.

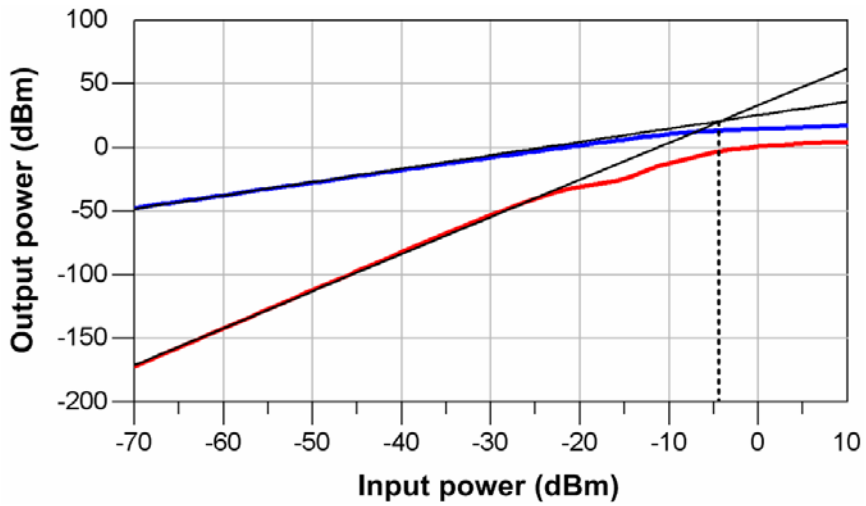


Fig. 32 Two-tone test plot of simulated IIP3 of the LNA.

■ **Downconverter**

Fig. 33 shows the DC transfer characteristics of the downconverter with input voltages v_{RF} and v_{LO} between ±200 mV and ±300 mV, respectively, and the corresponding maximum differential output swing is ±174 mV. In practice, the IEEE 802.11a standard regulates a maximum input power of -30 dBm, after amplified by the designed LNA, signal power increases to -10 dBm, i.e. ±100 mV, so the maximum input amplitude fed into the downconverter is around ±100 mV; therefore, the corresponding maximum differential output swing is ±93 mV with a maximum-scaled linearity error of 7% (7 mV/100 mV = 7%). An output buffer stage follows the downconverter. Fig. 34 is the results probed at the output of the buffer. The quadrature downconverted IF signals are at a frequency of about 10 MHz. For partial positive-substrate-biased MOS transistors, an issue of power dissipation resulting from bulk current is considered. The bias statuses of positive-substrate-biased MOS transistors are listed in Table VIII.

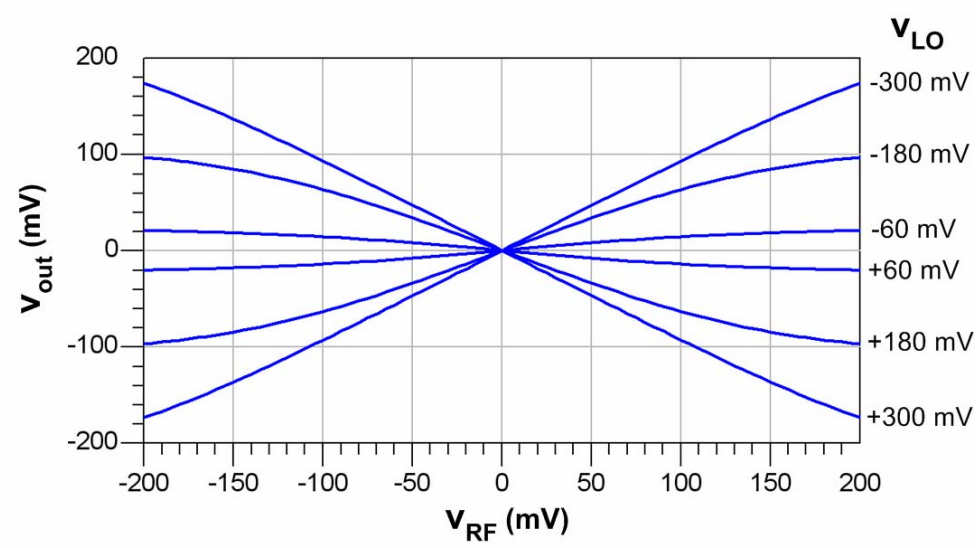


Fig. 33 Simulated DC transfer characteristics of the downconverter.

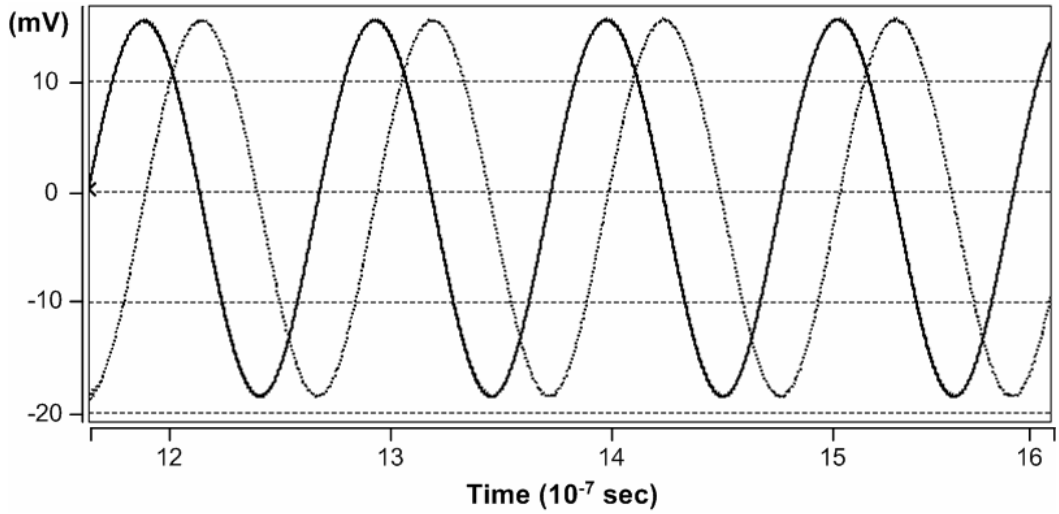


Fig. 34 Simulated quadrature IF waveforms (solid-line: I-channel, dot-line: Q-channel).

Table VIII Simulated Bias Statuses of Positive-Substrate-Biased MOS Transistors

	Bulk-biased voltage	Bulk-biased current
Mbi1-Mbi4, Mbq1-Mbq4	0.35 V	45.6 nA
Mi5, Mi6, Mq5, Mq6	0.3 V	9.38 pA
Mi7, Mq7	0.3 V	6.84 pA

■ **Quadrature voltage-controlled oscillator**

Fig. 35 presents the LO spectrum, where a desired tone at 5.25 GHz is observed. Fig. 36 and Fig. 37 are sequentially quadrature LO waveforms and the plot of tuning range, respectively. The quadrature VCO oscillates from 5.14 GHz to 5.36 GHz with under a tuning voltage of 0 V to 1 V. When the oscillation frequency is 5.25 GHz, the phase noise is -106.4 dBc at 1-MHz offset, shown in Fig. 38.

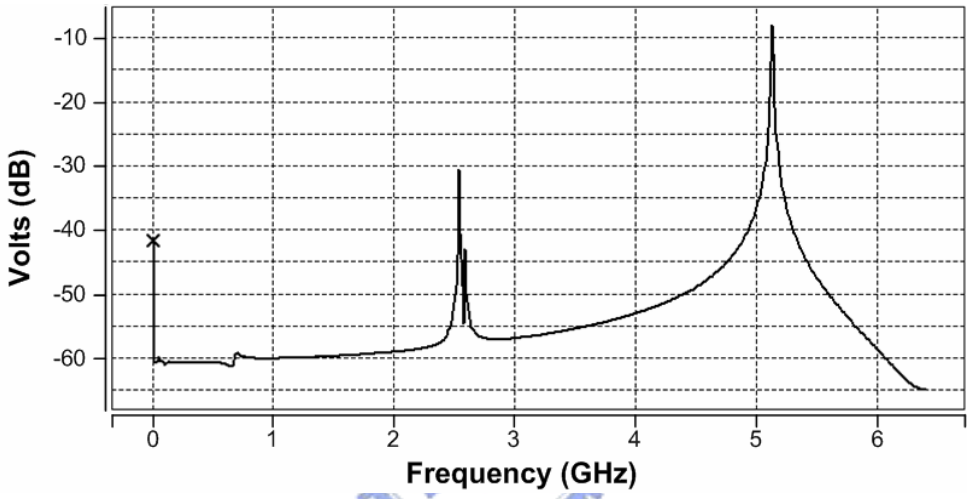


Fig. 35 Simulated LO spectrum.

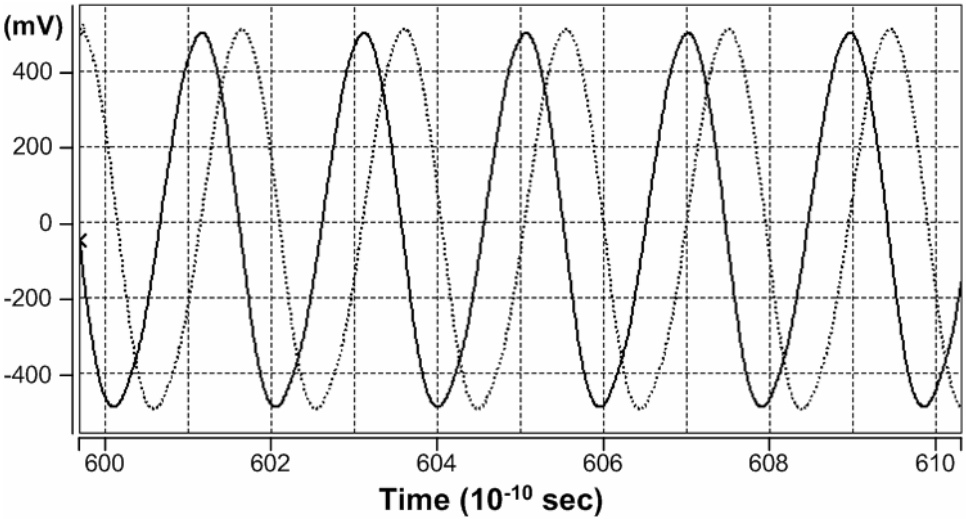


Fig. 36 Simulated quadrature LO waveforms (solid-line: I-channel, dot-line: Q-channel).

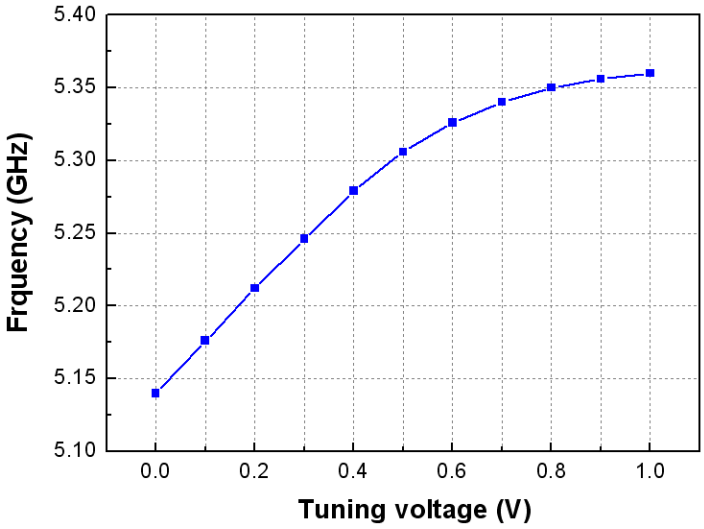


Fig. 37 Simulated tuning range of the quadrature VCO.

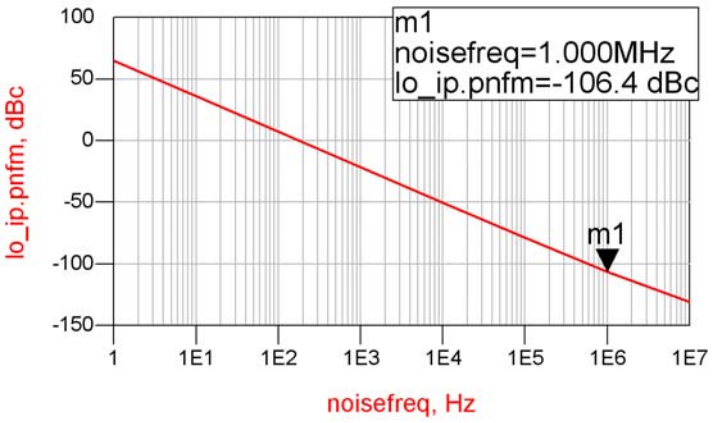


Fig. 38 Simulated phase noise of the quadrature VCO.

■ **Overall**

Fig. 39 plots the simulated conversion gain of the receiver. By sweeping the frequency of RF signal with an LO frequency of 5.24 GHz, the conversion is about 21.7 dB in the desired band, and the corner frequencies at 150 kHz and 10 MHz are observed. Noise performance of the receiver is presented in Fig. 40. Selecting the noise bandwidth from 150 kHz to 10 MHz, the SSB noise figure is 13.5 dB after calculation. Two-tone test is applied to simulate the linearity of the receiver. Two RF signals at 5.245 GHz and 5.255 GHz are fed into the receiver

and downconverted by a LO frequency of 5.24 GHz and then the receiver outputs IF signals of first order and third order. Fig. 41 plots the output power of the two terms relative to RF input power on a logarithmic scale. The input third order intercept point (IIP3) and 1-dB compression point are acquired. The output buffer is taken into account in this simulation, and the 1-dB compression point would increase a value of 4.2 dB if the output buffer is excluded. For second-order distortion, the input second order intercept point (IIP2) is also simulated and plotted in Fig. 42.

As a result of a DC-offset compensation circuit applied to the receiver, DC offset voltage is also simulated. A RF signal with an identical frequency to LO signal is fed into the receiver to simulate self-mixing phenomenon. After self-mixing, a DC offset voltage is appeared at the output terminals of the downconverter and thus influences bias status. By sweeping the power levels of input RF signal, the DC offset voltages at differential IF output terminals are plotted in Fig. 43. With an injected input power of -50 dBm, the DC offset voltage is about 4 mV. Besides, the DC offset voltages at the outputs of each stage are listed in Table IX. In conclusion, a simulation summary of the receiver is listed in Table X.

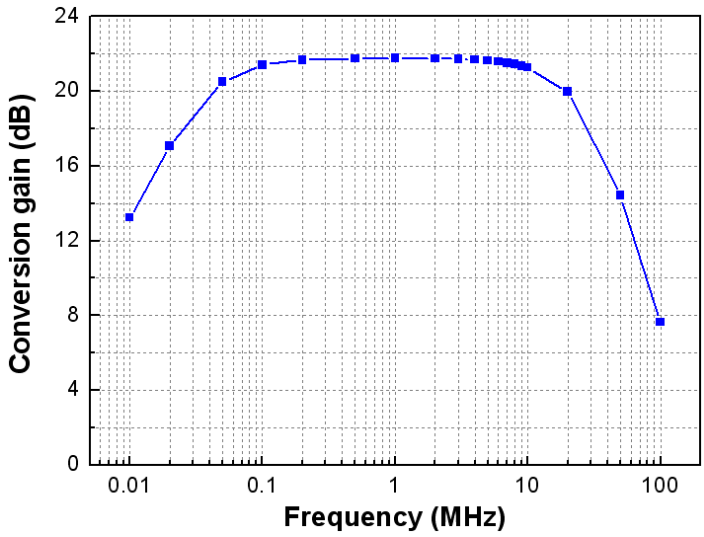


Fig. 39 Simulated conversion gain of the receiver.

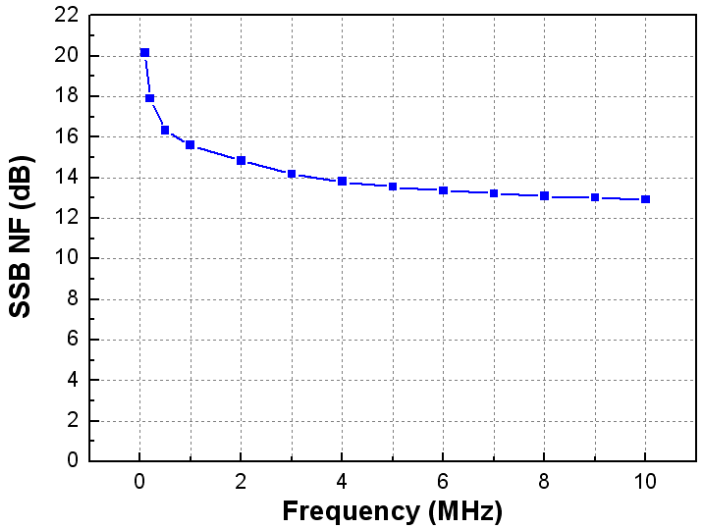


Fig. 40 Simulated noise figure of the receiver.

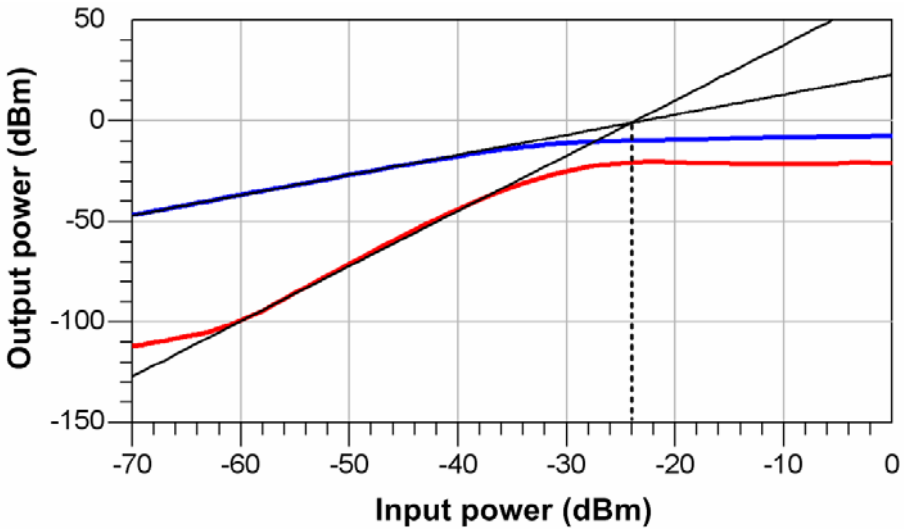


Fig. 41 Two-tone test plot of simulated IIP3 of the receiver.

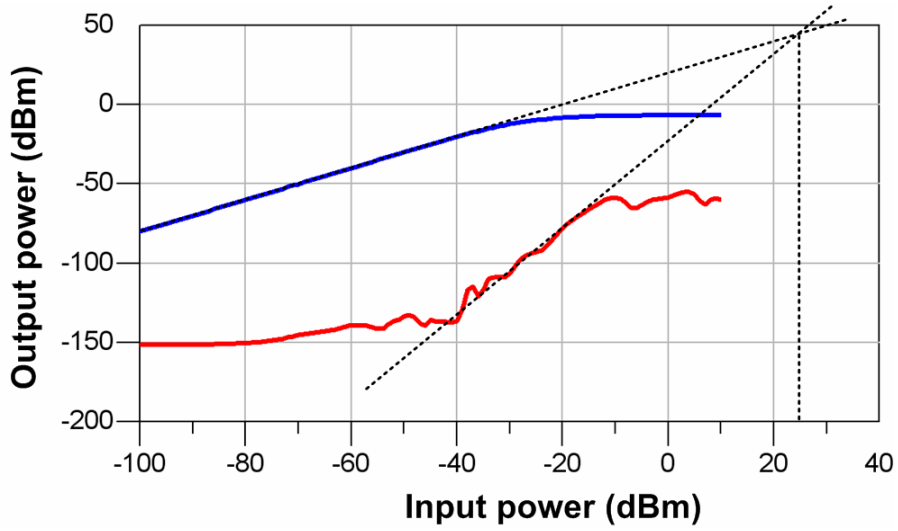


Fig. 42 Two-tone test plot of simulated IIP2 of the receiver.

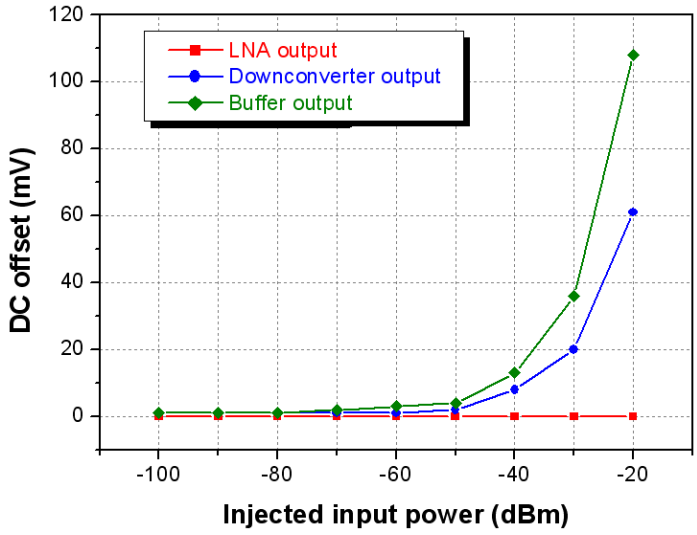


Fig. 43 Simulated DC offset at each stage.

Table IX Detailed Simulated Results of DC Offset at Each Stage

Injected input power	LNA output	Downconverter output	Buffer output
-60 dBm	0.36 μV	1 mV	3 mV
-50 dBm	0.93 μV	2 mV	4 mV
-40 dBm	1.69 μV	8 mV	13 mV
-30 dBm	2.97 μV	20 mV	36 mV
-20 dBm	24.1 μV	61 mV	108 mV

Table X Post-Simulation Summary of the Receiver

Technology	TSMC 0.18-μm CMOS 1P6M	
Supply voltage	0.6 V	
Frequency band	5.15-5.35 GHz	
LNA	S11 (< -10 dB)	5.05-5.45 GHz
	Gain	20.5 dB
	Noise figure	2.7 dB
	P_{-1dB}	-13.3 dBm
	IIP3	-4 dBm
	Power consumption	1.45 mW
Downconverter	Conversion gain	1 dB
	Noise figure	21 dB
	Power consumption	0.48 mW
Quadrature VCO	Tuning range	5.14-5.36 GHz
	K_{VCO}	220 MHz/V
	Output power	3 dBm
	Power consumption	2.5 mW
Overall	Conversion gain	21.7 dB
	SSB noise figure	13.5 dB
	P_{-1dB}	-29.4 dBm (without buffer)
		-33.6 dBm (with buffer)
	IIP3	-24 dBm (with buffer)
	DC offset (with an injected power of -50 dBm at receiver input)	4 mV
	Power consumption	4.4 mW

CHAPTER 3
EXPERIMENTAL RESULTS

The receiver front-end are designed and fabricated. This chapter describes layout, measurement setup and experimental results. The measured results are taken into discussions and compared with post-simulation results.

3.1 Layout Description

The receiver is implemented in 0.18-μm 1P6M CMOS technology supported by TSMC. All NMOS devices are arranged with deep n-well technique, which allows source and bulk of an individual NMOS transistor to be connected to avoid body effect. Because of fully differential configuration applied to all circuits, the components are disposed as symmetrically as possible. Dummy gates and dummy resistors are introduced to the margins of each MOS device and resistor, respectively, to cope with process variation. The LNA and downconverter of the receiver are complicated in implementation and suffer from process variation easily. Mismatches between two identical devices originally in layout may occur due to regional locations, material gradient and temperature gradient during fabricating process. The MOS devices are disposed with uniform separation for process-variation tolerance and symmetrical signal routes. Besides, an additional guard ring surrounds each channel of the downconverter to alleviate LO affection due to substrate coupling. Similarly, the quadrature VCO and the output buffers are surrounded with double guard rings for suppression of substrate-coupling LO and stable electric potential on substrate, respectively.

Furthermore, every spiral inductor keeps proper distances from the others and the core circuit to prevent mutual inductances and disturbance, and signal paths should be as short as possible in metal routes to alleviate the transmission line effect. Each gate-biased pad is fed

with a DC voltage via a kΩ-order resistor for gate reliability. Any DC pad is recommended not to locate between two differential-signaled pads so that the signal routes on the external board, connected to signal pads via bond-wires, are not restricted by DC lines. For the input matching consideration, the differential RF input pads are designed individually. Fig. 44 shows the receiver layout, covering an area of 4.4 mm^2.

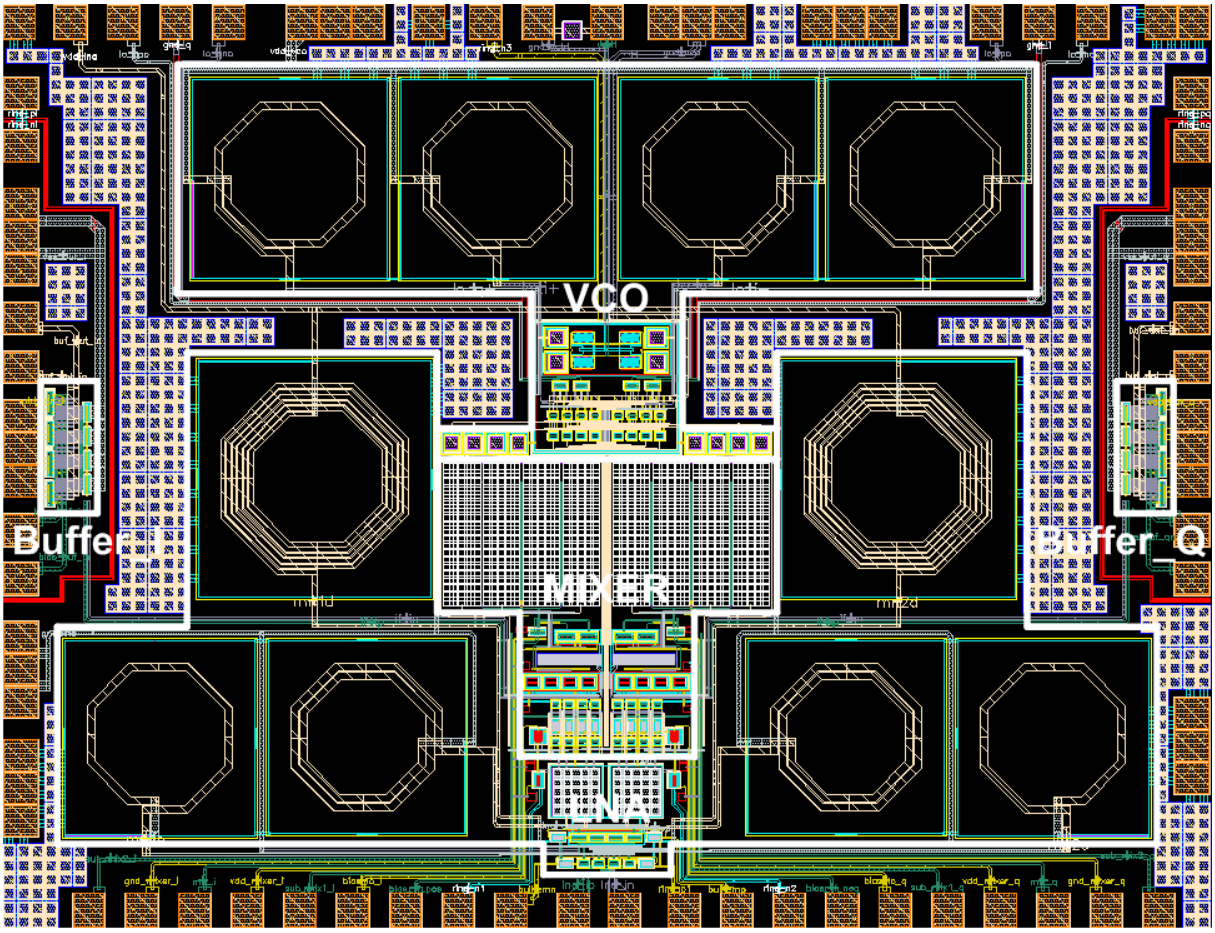


Fig. 44 Layout configuration of the receiver.

3.2 Measurement Considerations and Setup

The receiver chip is a bare die and needs to be bonded on board. Packaged chips are excluded due to more complicated parasitics. The chip microphotograph and the bonding board are shown in Fig. 45 and Fig. 46, respectively.

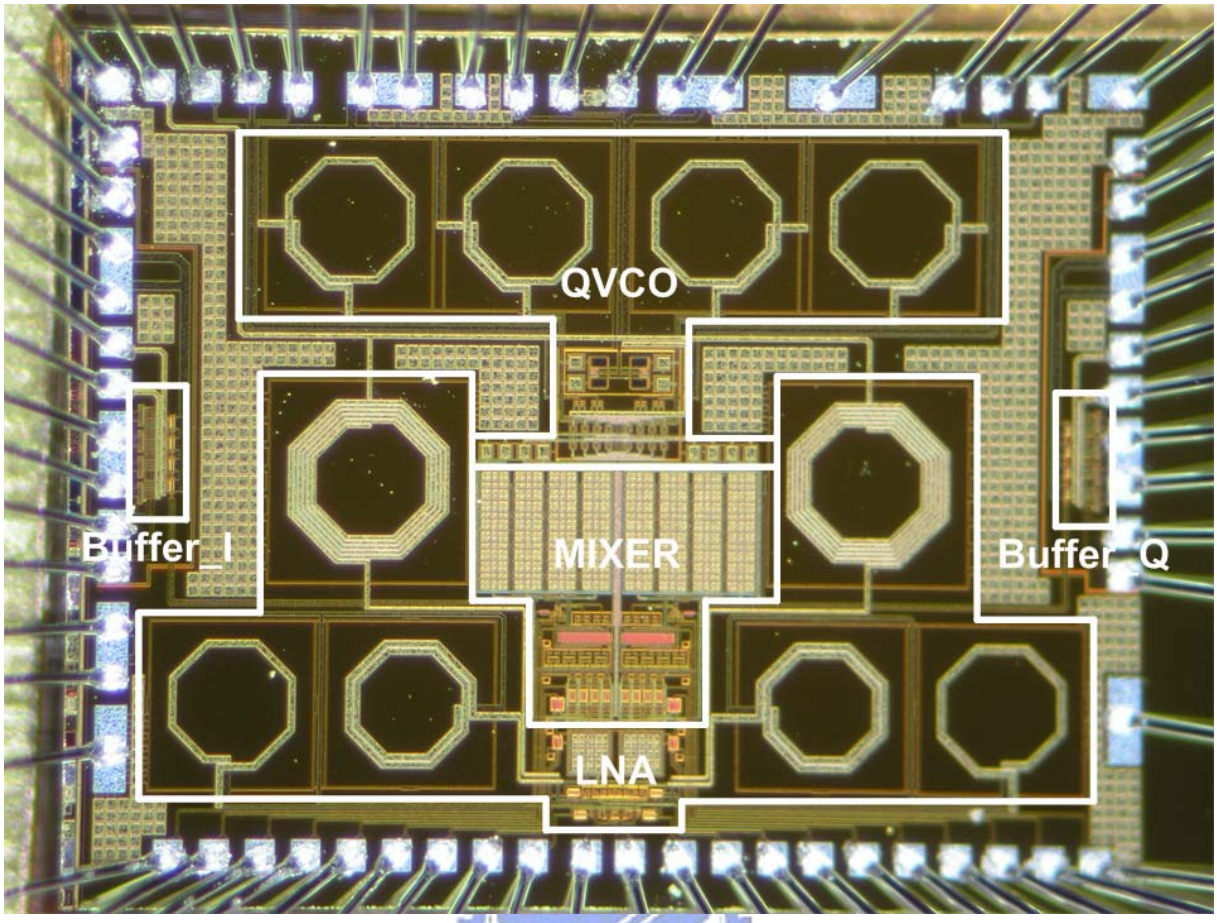


Fig. 45 Chip microphotograph.

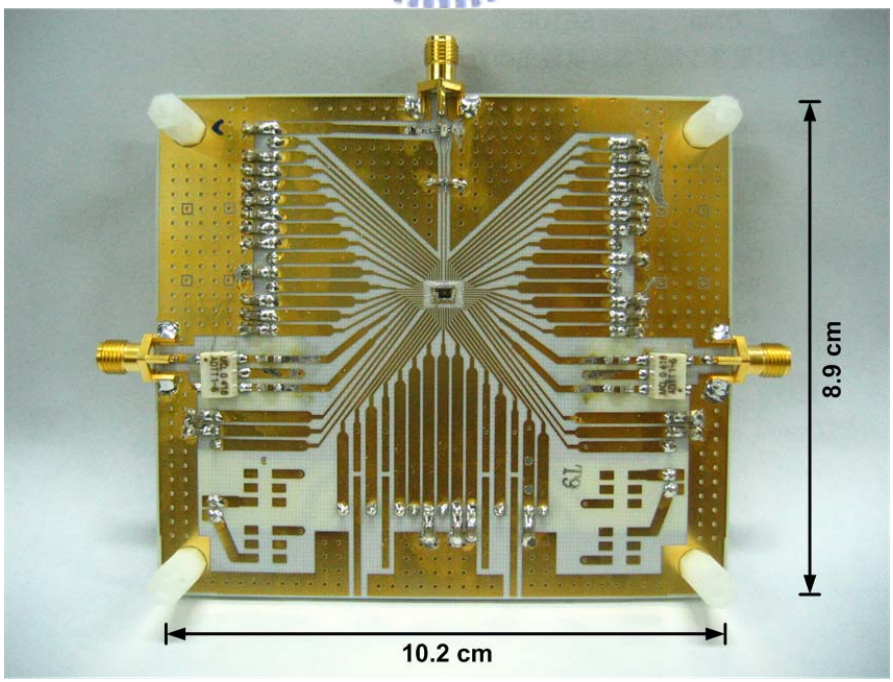


Fig. 46 Bonding board for the receiver.

Fully differential topology is adopted in the chip so a balun and two transformers are necessary for RF and IF terminals, respectively, in measurement. The balun with part number BL2012-10B5388 are made by Advanced Ceramic X Corporation. The transformers with model index ADTT1-6 are made by Mini-Circuits. Signal attenuation caused by the balun and transformers are measured for compensating back to relative apparent performance. Besides, inductance variation of bond-wire may affect input matching. A matching network, composed of microstrip transmission lines and discrete capacitors, is employed to compensate the input matching. Fig. 47 illustrates the half circuit of the input matching network. In this figure, L_{bw} represents the equivalent inductance of the bond-wire. Discrete capacitor C_s, is made by YAGEO with product number CC0603CRNPO9BN1R0, connects to the microstrip transmission line and divides it into two parts, *TL1* and *TL2*. The microstrip transmission line is made by the top layer of PCB, whose dielectric material is RO4003 with a dielectric constant of 3.38.

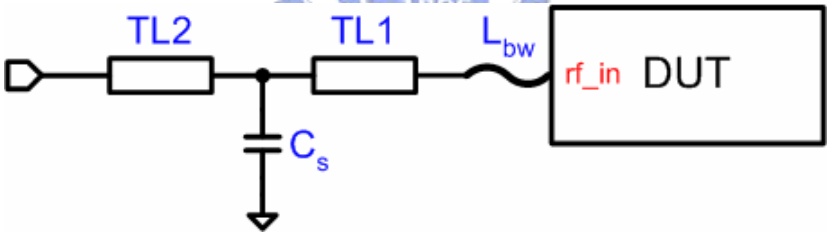


Fig. 47 Half circuit of input matching network.

The receiver chip under test needs a lot of discrete modules. As shown in Fig. 48, the modules are integrated in an individual DC board for this chip. In addition, every bias terminal is fed externally for flexible adjustment. A tunable resistor can provide an adjustable voltage source. Two parallel capacitors of 100 μF and 1000 μF connect to each power supply and ground, and another two capacitors of 0.47 μF and 4.7 μF connect to every bias terminal and ground in order to filter out noise from power supply. Fig. 49 presents the scheme. For

this scheme, a stable LO signal is obtained, resulting in smoother downconverted IF signals.

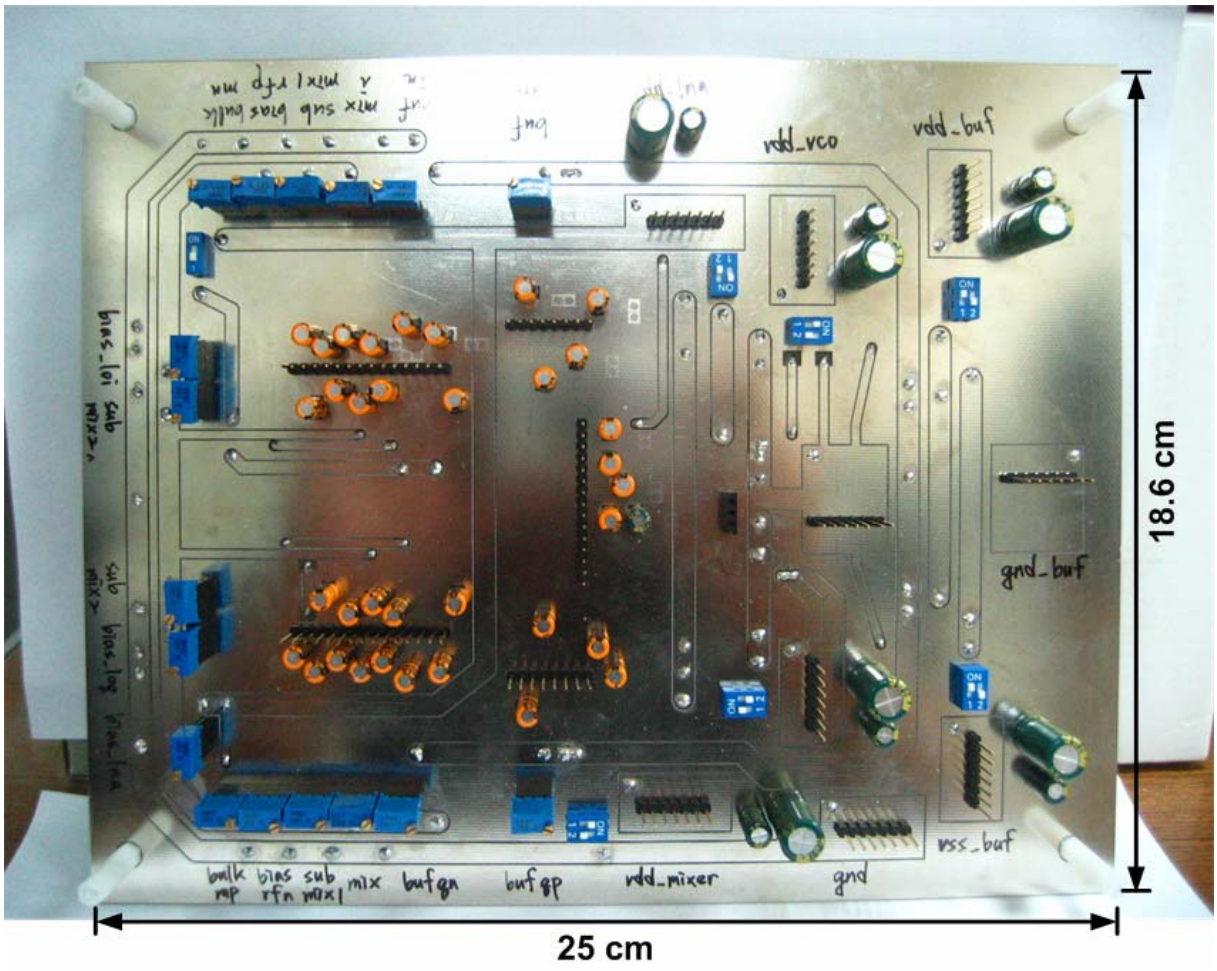


Fig. 48 DC board for the receiver.

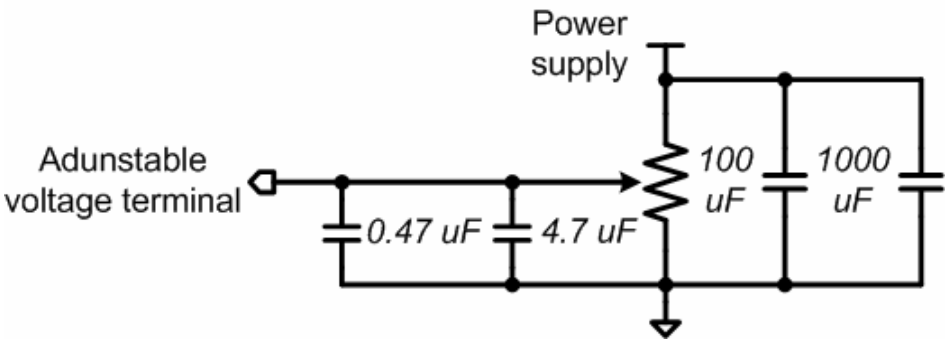


Fig. 49 Adjustable voltage module.

The complete measurement setup with other accessories for the receiver is depicted in Fig. 50. This setup is adequate to measure the most parameters of the receiver, such as conversion gain, noise figure and linearity. Besides, to measure DC offset voltage, extra external resistors are connected directly to the IF output terminals of the receiver. The method of DC-offset measurement is illustrated in Fig. 51. In this figure, a signal at f_1 is inputted to the receiver, and the quadrature VCO oscillates at f_2. If the two signals are identical frequency, i.e. $f_1 = f_2$, a DC offset voltage is generated after downconverted. The DC offset voltage is appeared at the output terminals of the buffers, and it is more conspicuous as the input power is larger.

Combing the bonding board with the DC board and then the test platform, shown in Fig. 52, is completed. Besides, all kinds of measurements depend on various instruments. S-parameter analysis requires a network analyzer; spectrum analysis requires a signal generator and a spectrum analyzer; noise analysis requires a noise source and a noise figure meter; waveform analysis requires a signal generator and an oscilloscope.

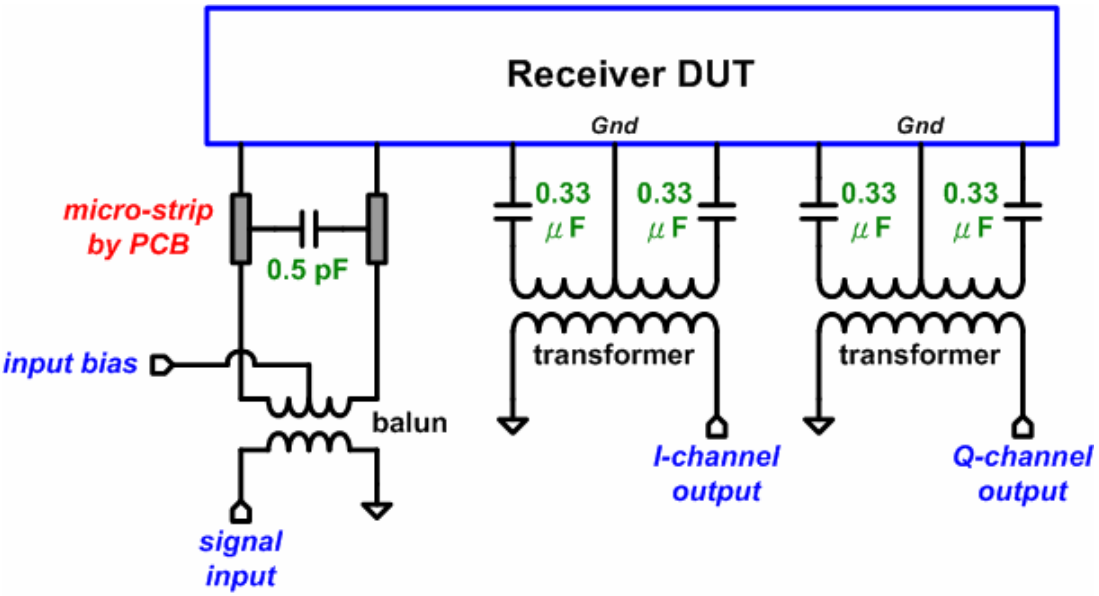


Fig. 50 Measurement setup for the receiver.

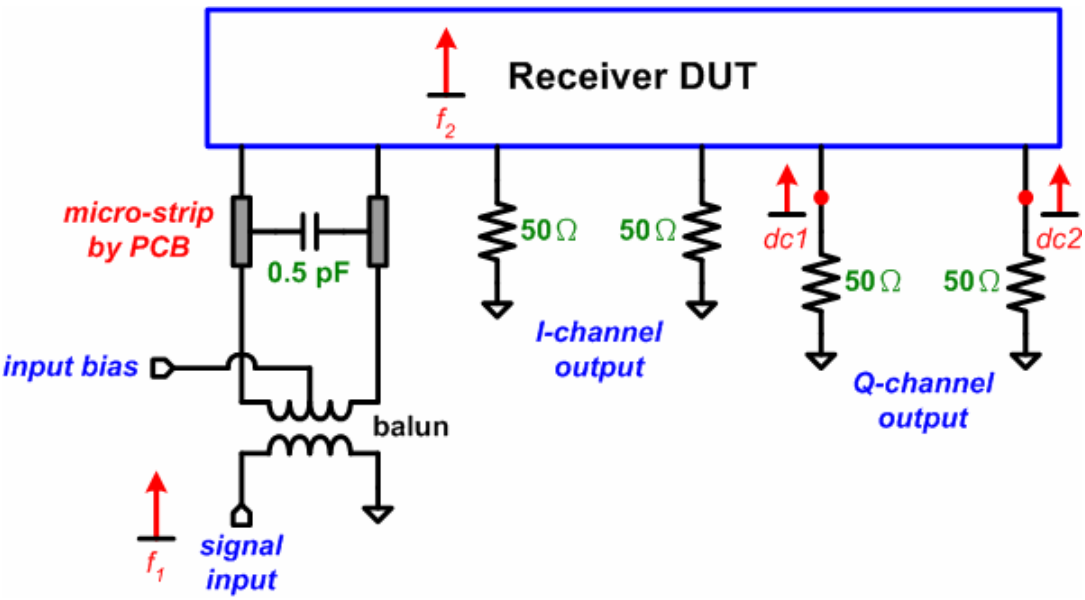


Fig. 51 Measurement setup for DC offset.

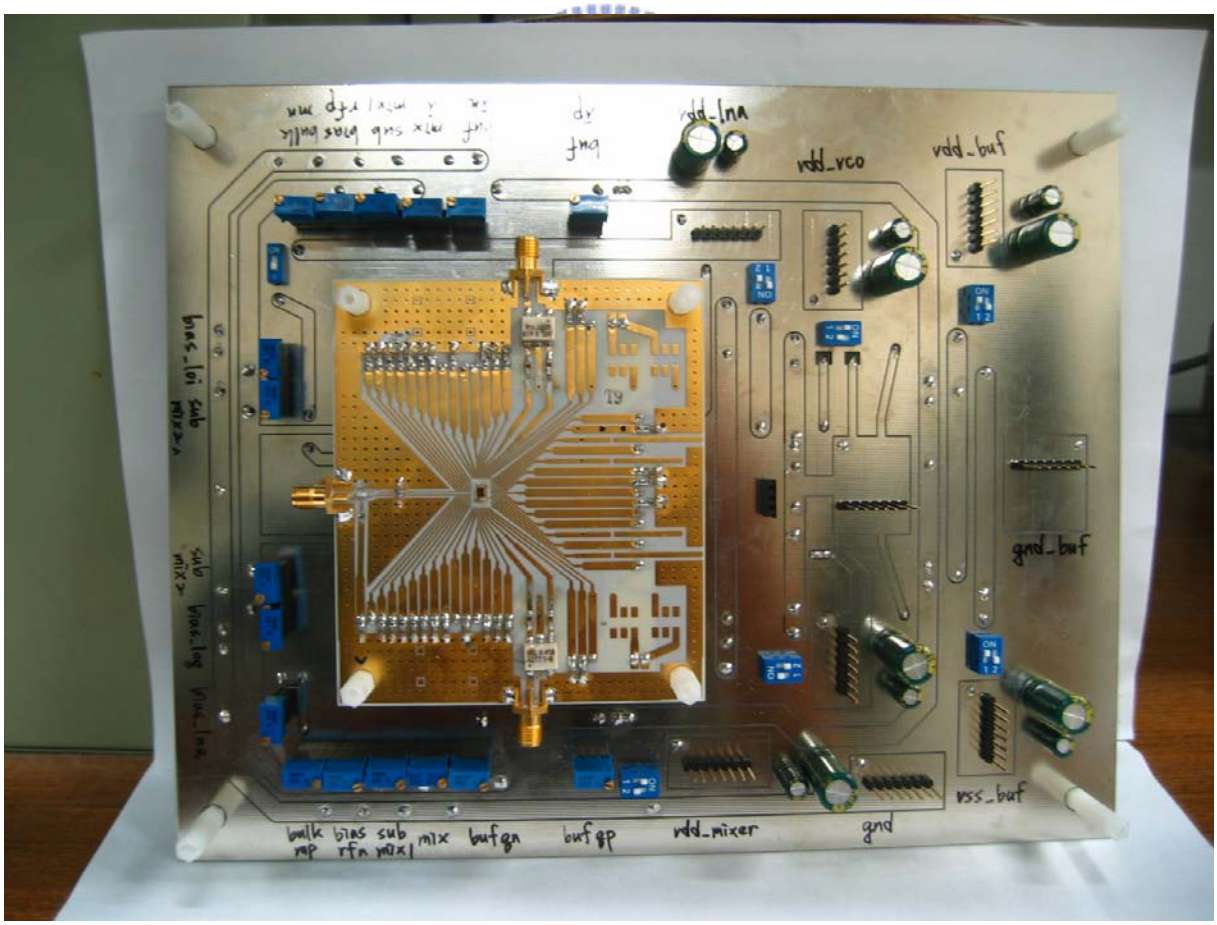


Fig. 52 Test platform for the receiver.

3.3 Experimental Results

Before measuring the receiver, the loss of passive components should be measured in the first place. The loss of external input matching network, output transformers and DC blocking capacitors are measured by network analyzer. The loss of the input matching network is about 1.7 dB in the desired band. The loss of the output transformer and DC blocking capacitors of each channel is about 0.2 dB in the desired band. The cable loss is about 2.7 dB. Besides, the parasitic resistances of metal lines on the bonding board are so little that the loss of them is neglected in measurement.

Including the input matching network, composed of external capacitors and microstrip transmission lines, the receiver performs an S11 of lower than -10 dB in a frequency range of 5.07 GHz to 5.3 GHz, exhibited in Fig. 53. It is found by several tested chips that the optimum input matching can be achieved by moving the capacitor to a certain location on the microstrip transmission line. The equivalent inductance of bond-wire is estimated with an approximate value of 2 *nH*.

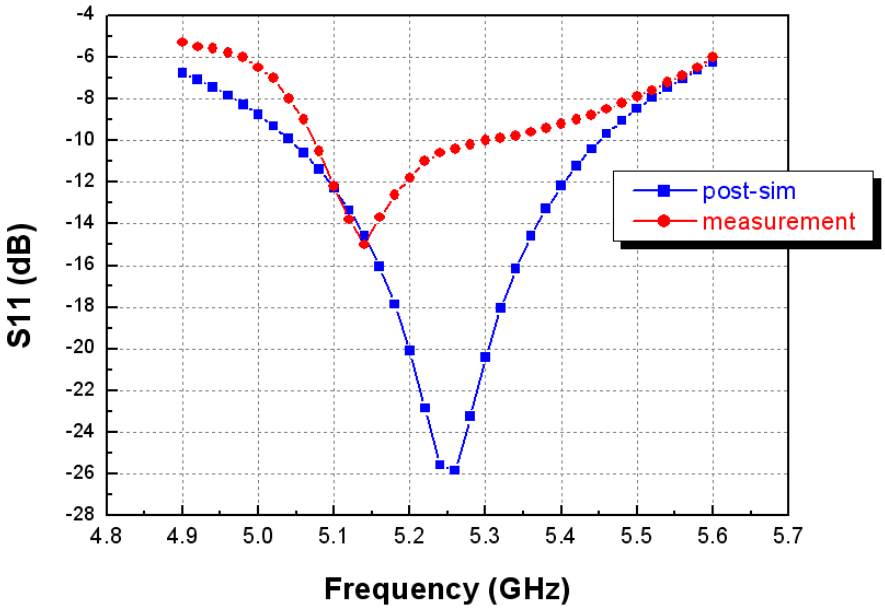


Fig. 53 S11 of the receiver.

The spectrum of the QVCO (quadrature VCO) can be analyzed by the QVCO buffer. The measured spectrum is presented in Fig. 54, where the power is only -48.67 dBm under a supply voltage of 0.7 V because the output terminals of the QVCO buffer are not impedance matching. The oscillation frequency can be tuned from 3.617 GHz to 3.797 GHz under a tuning voltage of 0 V to 1 V, and the K_{VCO} is 180 MHz/V. The oscillation frequency shifts downward by 1.5 GHz compared with post-simulation results due to parasitic inductances of the interconnections connected to the inductors and the core of the QVCO. The parasitic inductances are not extracted by Calibre, a verification tool used to extract parasitics. In order to measure the receiver in the desired band, laser-cut technique is adopted to cut off the connection between the buffer and the core of the QVCO and a part of varactors. Thus, the capacitances at each output terminals of the QVCO are reduced so that the oscillation frequency of the QVCO shifts upward. After coping with several tested chips with this procedure, a resultant oscillation frequency tuned from 4.564 GHz to 4.684 GHz under a tuning voltage of 0 V to 1 V is obtained by measuring the LO leakage at the IF output, and the K_{VCO} is reduced to 120 MHz/V. Fig. 55 shows the microphotograph of the QVCO after laser-cut, and Fig. 56 plots the resultant tuning range compared to the original measurement. In conclusion, the resultant frequency range is applied to measure the performance of the tested receiver.

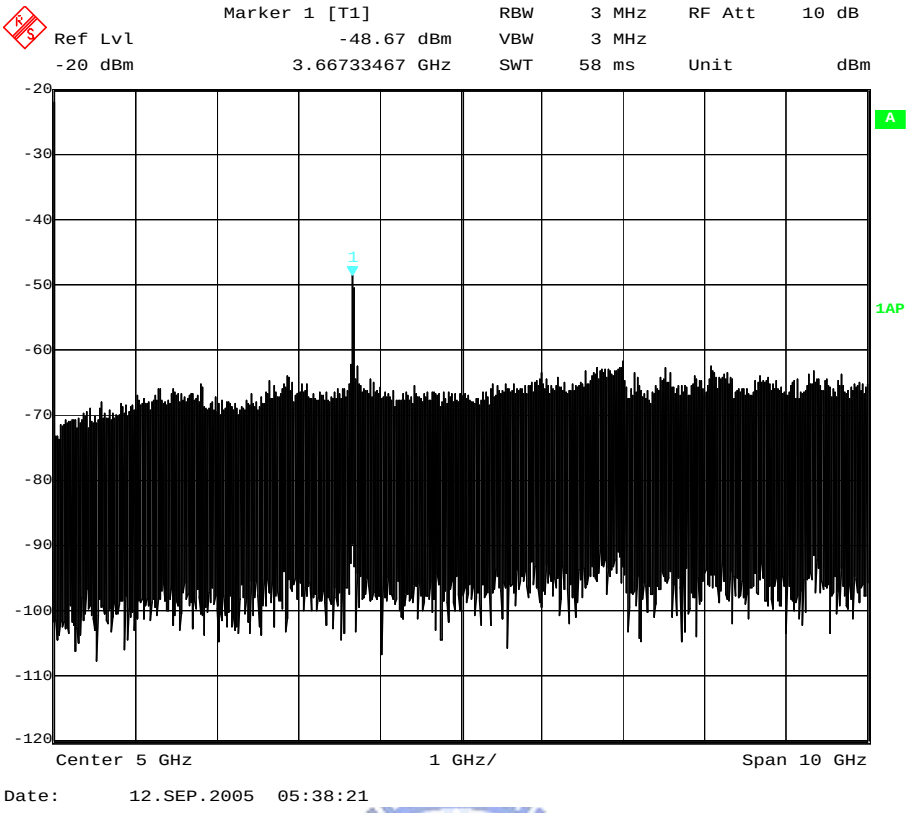


Fig. 54 Measured spectrum of the QVCO.

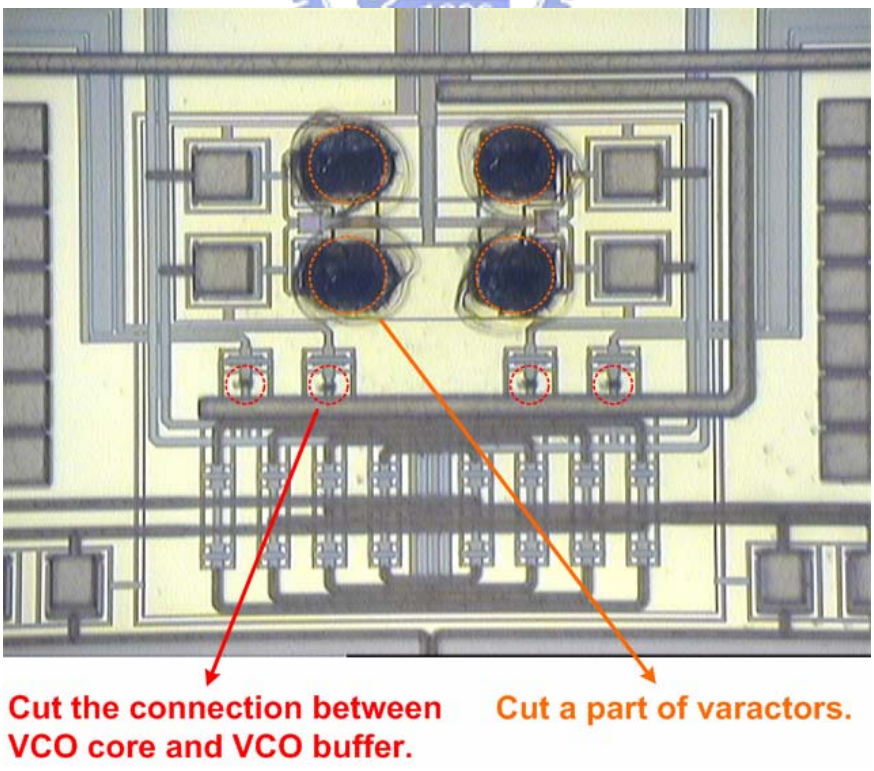


Fig. 55 Microphotograph of the QVCO after laser-cut.

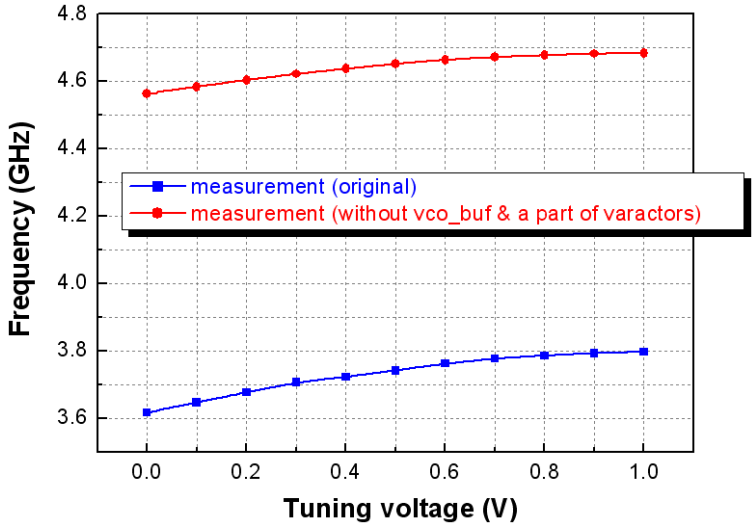


Fig. 56 Measured tuning range of the QVCO.

Two-port network of S-parameter analysis cannot be applied for gain estimation because the frequencies of input and output terminals are different. Spectrum observation is a substitutive way. Fig. 57 presents an IF output spectrum of the receiver while a RF signal with a frequency of 4.65 GHz and a power of -65 dBm is introduced and the oscillation frequency of the QVCO is 4.65 GHz. Compensating back with the loss of cable and external components, the receiver performs a conversion gain of 12.6 dB under a supply voltage of 0.65 V. The measured conversion gain is too low because the frequency of RF signal is not located at the desired band of the LNA, which is a gain stage in chief. To measure the conversion gain at the lower frequency, a RF signal with larger power is introduced to the receiver. Fig. 58 displays the measured conversion gain of the receiver by sweeping the frequency of RF signal with an LO frequency of 4.65 GHz. The corner frequencies at 150 kHz and 10 MHz are also observed.

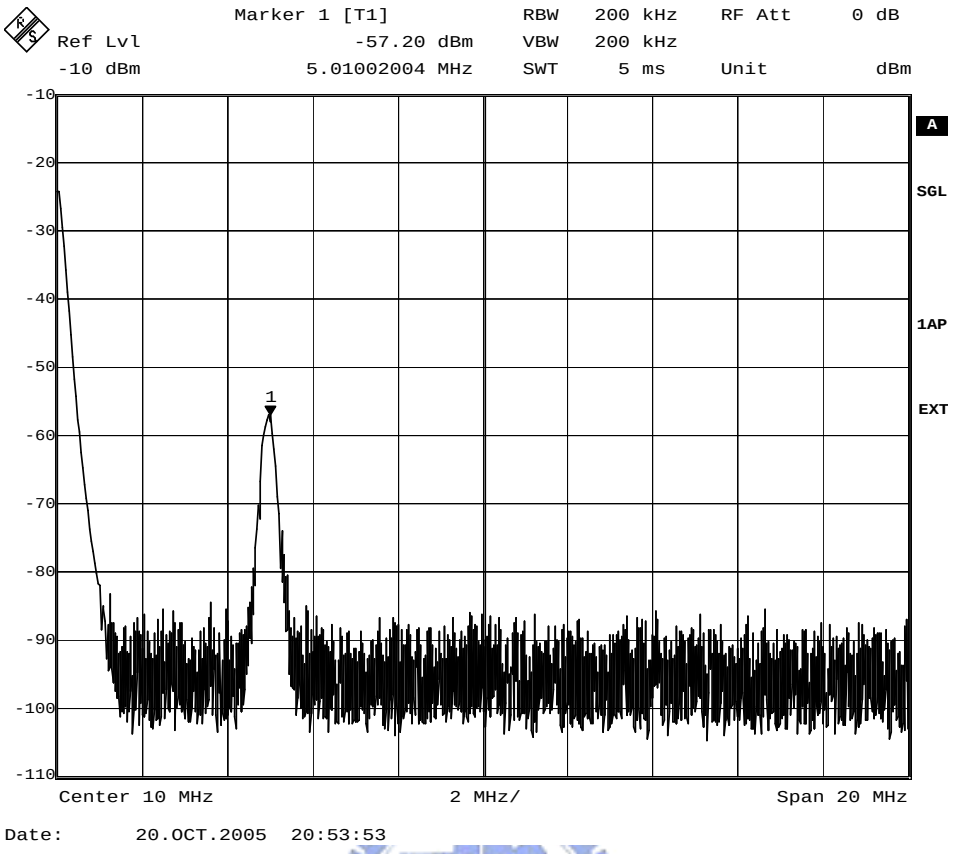


Fig. 57 Measured IF spectrum.

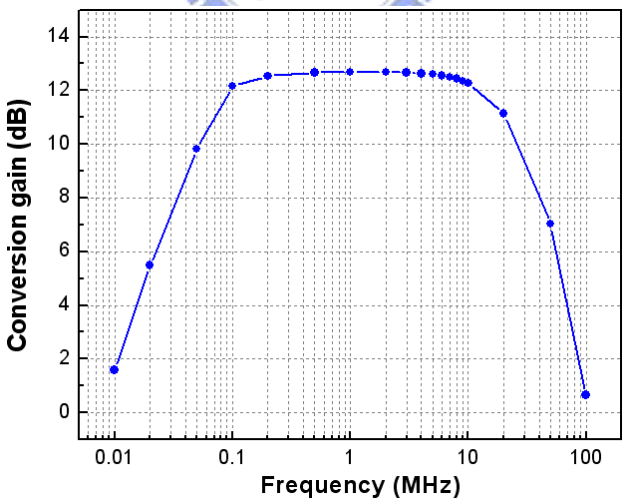


Fig. 58 Measured conversion gain of the receiver.

The measurement setup for noise figure is shown in Fig. 59. The signal analyzer with product number FSIQ26 is made by Rhode & Schwarz. The noise source with product

number 346B, having a SNR of 15.2 dB, is made by HP. Software for noise measurement named FS-K3, having a start frequency of 100 kHz, is utilized to calculate the noise figure. Fig. 60 presents the noise performance of the tested receiver. Selecting the noise bandwidth from 150 kHz to 10 MHz, the SSB noise figure is 24 dB after calculation. Similarity, the measured noise performance is terrible since the frequency of RF signal is not located at the desired band of the LNA, which dominates total noise performance. Fig. 61 plots the IF output power related to RF input power, and the 1-dB compression point is obtained with a value of -24 dBm. The measured result is better than post-simulation due to the measured low conversion gain of the receiver. Also, DC offset is measured, and the results are presented in Fig. 62. After measuring several tested chips, the DC offset voltage at the differential outputs is less than 3 mV and 25 mV with an injected input power of -50 dBm and -30 dBm, respectively.

The values of fine-tuned supply voltages, gate biases and bias resistors are listed and compared with post-simulation in Table XI. The power consumption of the tested receiver is 8.14 mW due to a raise of the supply voltages of each sub-circuit. Table XII lists a summary of the tested receiver, including a comparison between post-simulation and measurement. The measured performance differs from the post-simulation and thus it is discussed in detail in the next section.

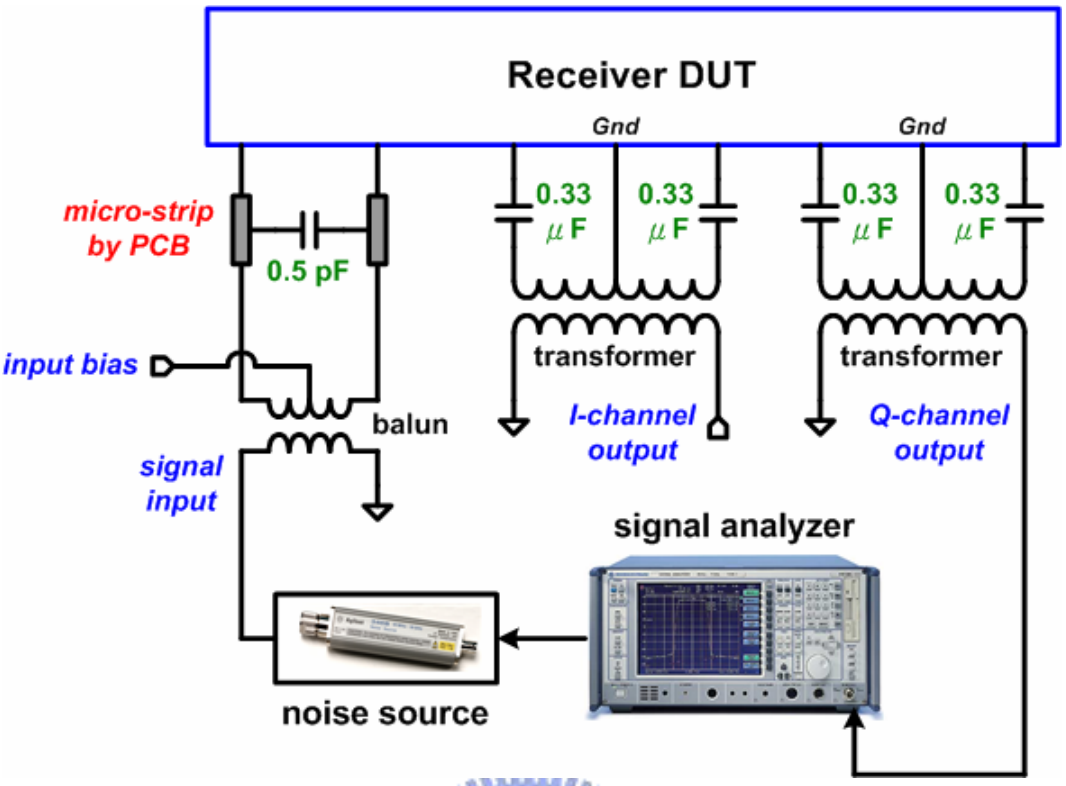


Fig. 59 Measurement setup for noise figure.

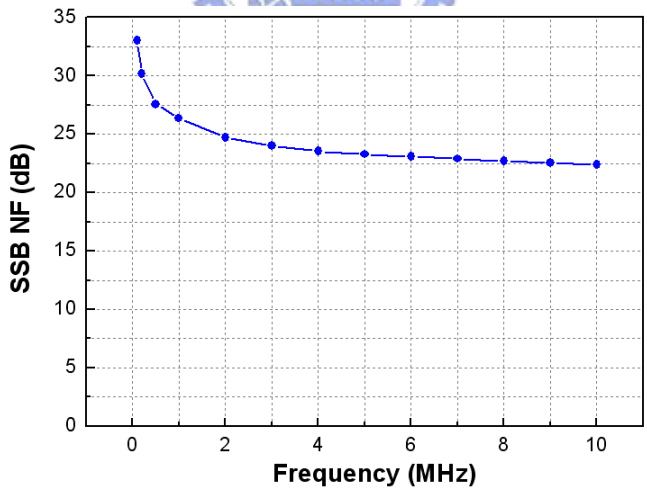


Fig. 60 Measured noise figure of the receiver.

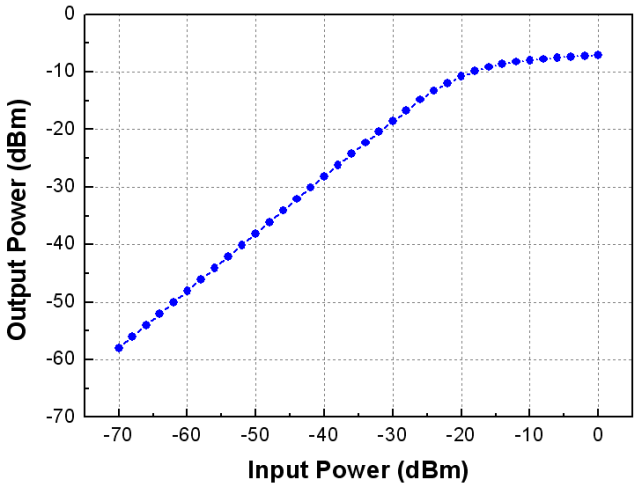


Fig. 61 Measured 1-dB compression point of the receiver.

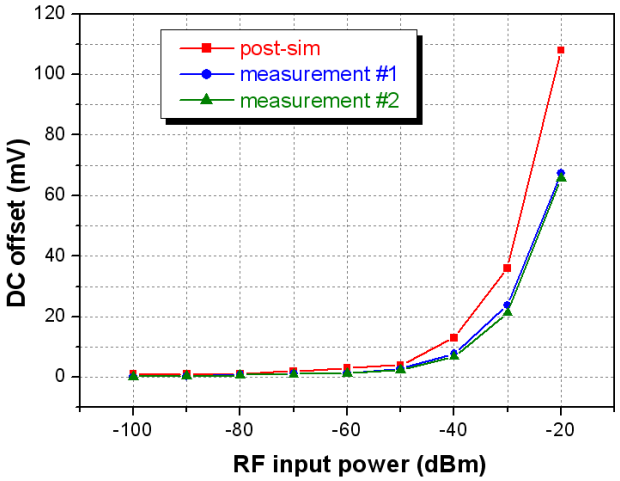


Fig. 62 Measured DC offset of the receiver.

Table XI Comparison on Bias Status between Post-Simulation and Measurement

Supply voltage	Post-simulation	Measurement
LNA and downconverter	0.6 V	0.65 V
Quadrature VCO	0.6 V	0.7 V
Gate bias	Post-simulation	Measurement
Mn1, Mn2	0.6 V	0.63 V
Mai1-Mai4, Maq1-Maq4	0.6 V	0.65 V
Mbi1-Mbi4, Mbq1-Mbq4	0.6 V	0.65 V
Bulk bias	Post-simulation	Measurement
Mbi1-Mbi4, Mbq1-Mbq4	0.35 V	0.38 V
Mi5-Mi7, Mq5-Mq7	0.3 V	0.33 V
Bias resistor	Post-simulation	Measurement
Rci, Rcq	2 kΩ	1.8 kΩ
Rbi1, Rbi2	600 Ω	582 Ω
Rbq1, Rbq2		554 Ω

Table XII Summary of the Tested Receiver

	Design target	Post-simulation	Measurement
Technology	TSMC 0.18-μm CMOS 1P6M		
Supply voltage	0.6 V	0.6 V	0.65 V/0.7 V
Power consumption	< 10 mW	4.4 mW	8.14 mW
QVCO tuning range	5.15-5.35 GHz	5.14-5.36 GHz	4.56-4.68 GHz (after laser-cut)
S11 (< -10 dB)	5.15-5.35 GHz	5.05-5.45 GHz	5.07-5.3 GHz
Conversion gain	> 20 dB	21.7 dB	12.6 dB
SSB noise figure	< 15 dB	13.5 dB	24 dB
P_{-1dB}	> -30 dBm (without buffer)	-29.4 dB (without buffer)	-24 dBm
DC offset	< 10 mV	4 mV	< 3 mV

3.4 Discussions and Comparisons

First, the problem of frequency shift in the QVCO circuit is discussed. By reviewing the layout, it is found that the interconnections between the spiral inductors and the QVCO core are too long to increase equivalent inductances due to parasitic effects. Except parasitic capacitances and resistors, the parasitic inductances of metal routes are not extracted by Calibre. Hence, a complete analysis of parasitics has to be adopted to obtain an accurate simulation results. The layout of spiral inductors including metal routes in the QVCO is simulated by ADS Momentum simulator. Each spiral inductor is analyzed by a method of two-port S-parameter network. Fig. 63 and Fig. 64 present the equivalent inductances and quality factors of each spiral inductor. An average inductance is 2.43 *nH* at 5 GHz, increasing 1.24 *nH* compared to the inductor model provided by TSMC. The quality factor is down to an

average value of 3.85. For the low quality factors, the output power of QVCO also reduces, resulting in a low conversion gain of receiver. Applying the analysis results of these spiral inductors with metal routes to the QVCO circuit, the revised simulated oscillation frequency of the QVCO can be tuned from 3.62 GHz to 3.8 GHz under a tuning voltage of 0 V to 1 V, and the output power decreases to -1 dBm. The revised simulation of oscillation frequency is close to the measured results.

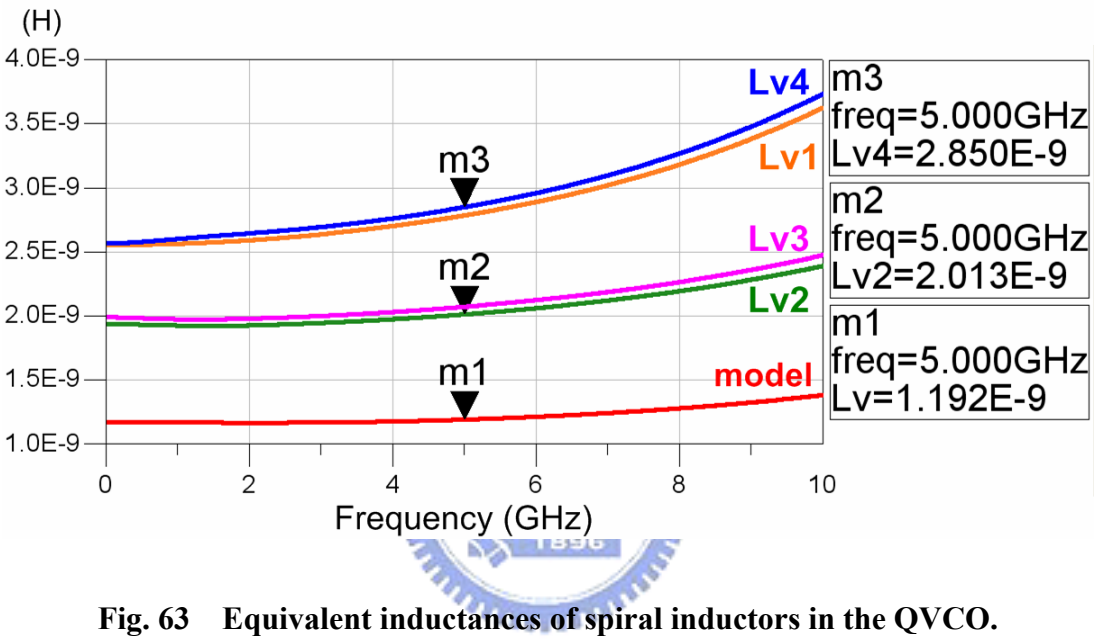


Fig. 63 Equivalent inductances of spiral inductors in the QVCO.

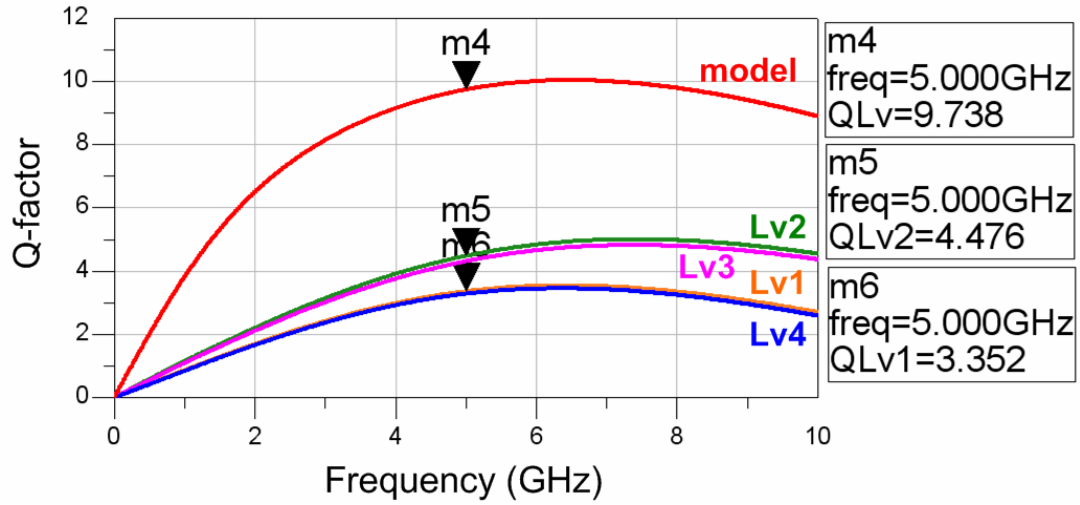


Fig. 64 Equivalent quality factors of spiral inductors in the QVCO.

In addition, the receiver is re-simulated to verify measurement results. The oscillation signal of the QVCO is set to a frequency of 4.65 GHz, which is identical to the measured oscillation frequency. Fig. 65 plots the revised simulated conversion gain of the receiver, which is down to 14.2 dB. Revised simulated noise performance of the receiver is presented in Fig. 66. The SSB noise figure is 21.5 dB. Fig. 67 plots the IF output power related to RF input power, and the revised simulated 1-dB compression point is obtained with a value of -26.2 dBm. DC offset voltage is 3 mV with an injected input power of -50 dBm, shown in Fig. 68. Table XIII lists a summary of comparing the revised simulation with measurement, and it is observed that the revised post-simulation results are close to measurement.

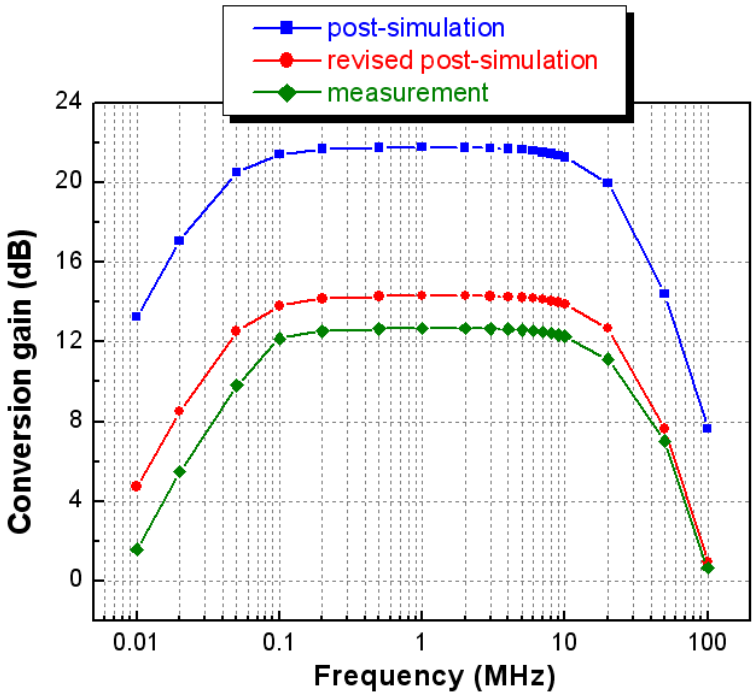


Fig. 65 Revised post-simulation of conversion gain.

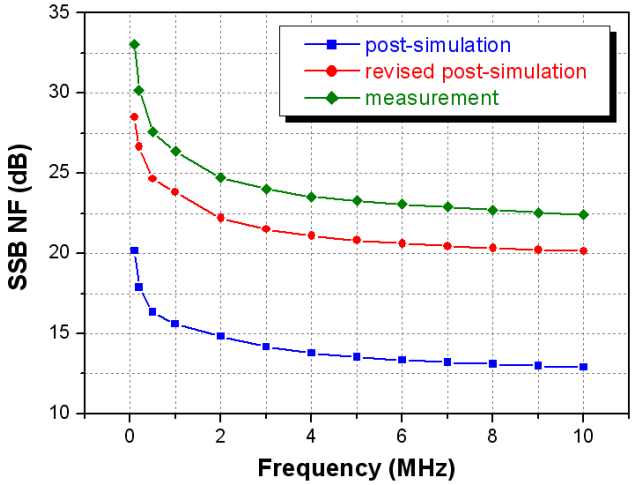


Fig. 66 Revised post-simulation of SSB noise figure.

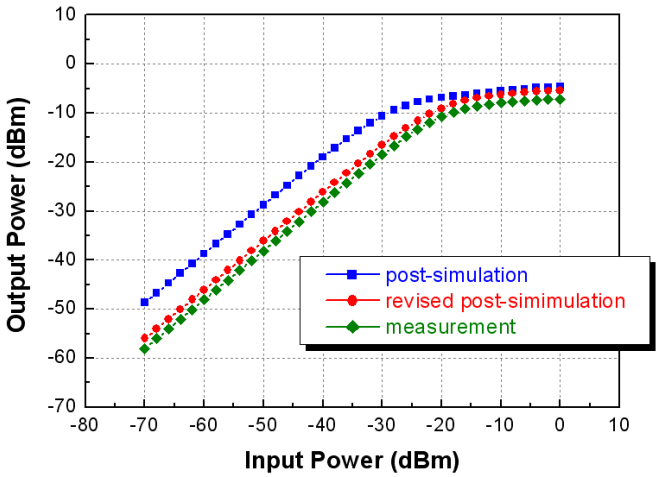


Fig. 67 Revised post-simulation of 1-dB compression point.

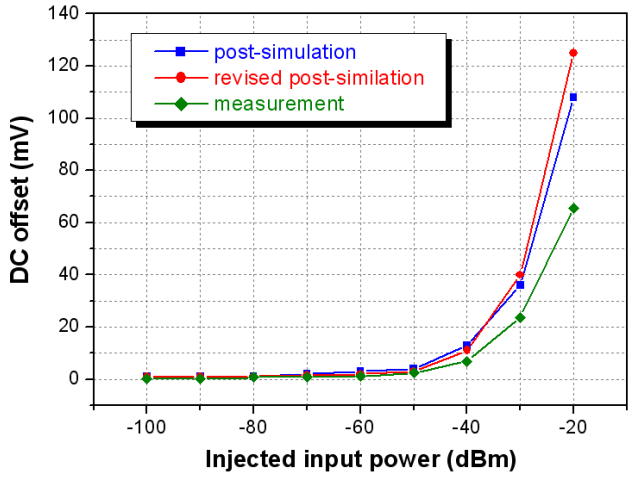


Fig. 68 Revised post-simulation of DC offset.

Table XIII Summary of Revised Post-Simulation

	Post-simulation	Revised Post-simulation	Measurement
Technology	TSMC 0.18-μm CMOS 1P6M		
Supply voltage	0.6 V	0.6 V	0.65 V/0.7 V
Power consumption	4.4 mW	4.4 mW	8.14 mW
VCO tuning range	5.14-5.36 GHz	3.624-3.806 GHz	3.617-3.797 GHz
Conversion gain	21.7 dB	14.2 dB	12.6 dB
SSB noise figure	13.5 dB	21.5 dB	24 dB
P_{-1dB}	-33.6 dBm	-26.2 dBm	-24 dBm
DC offset	4 mV	3 mV	< 3 mV

In order to alleviate the injury to circuit performance due to parasitic effects, the signal paths should be as short as possible in metal routes. A spiral inductor of center-tap type is applied to substitute the original spiral inductor of standard type. With two spiral inductors combined together, a center-tap spiral inductor can be connected to a differential circuit and thus shortens the interconnections between the inductor and core circuit while chip area is saved. Two center-tap spiral inductors are introduced into the original QVCO, shown in Fig. 69, and their equivalent inductances are 798 *pH* at 5 GHz, shown in Fig. 70. With a changed channel width of MOS transistors *Mv1-Mv8*, from 32.5 μm to 25 μm, a re-designed QVCO can be integrated with the designed receiver. Fig. 71 plots the tuning range of the re-designed QVCO compared with the original design. Besides, a summary of the re-designed receiver is listed in Table XIV.

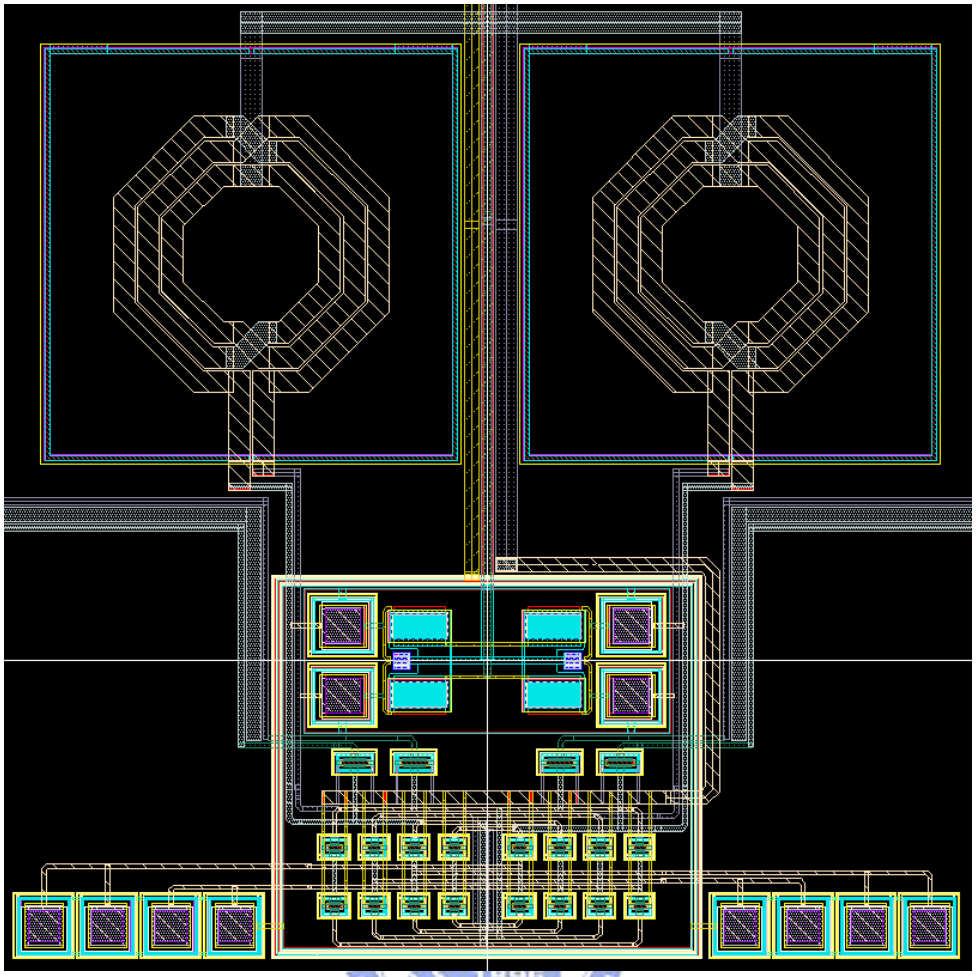


Fig. 69 Layout configuration of the re-designed QVCO.

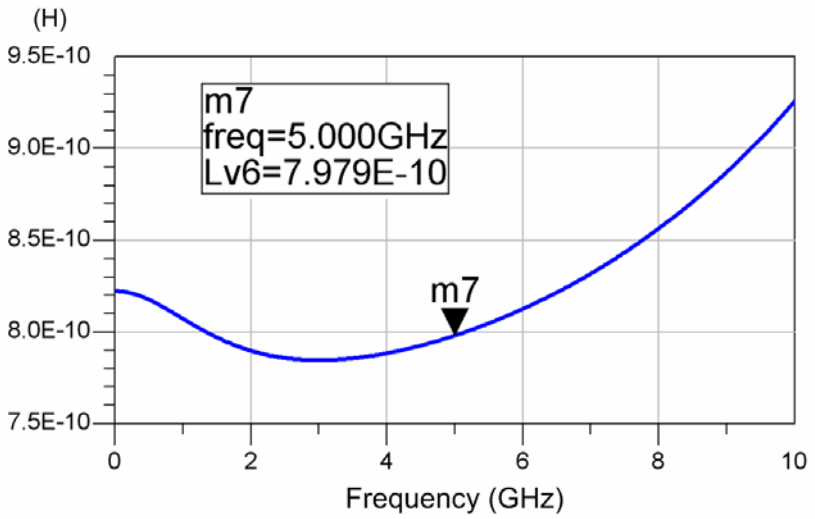


Fig. 70 Equivalent inductances of re-designed center-tap inductor.

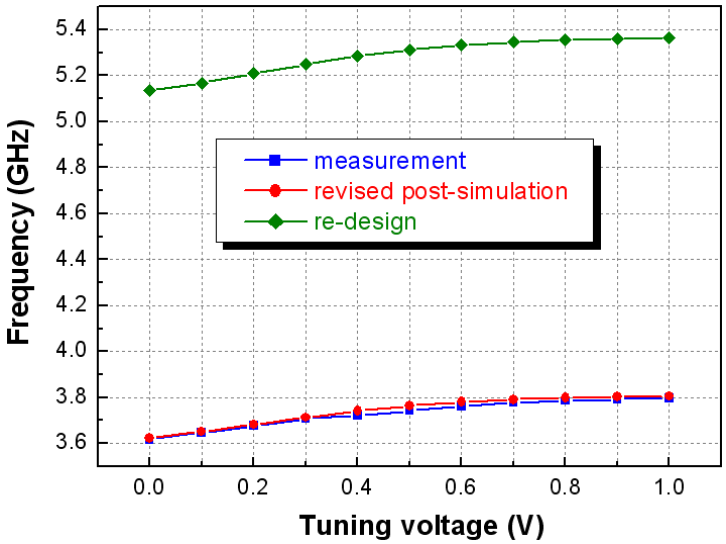


Fig. 71 Simulated tuning range of the re-designed QVCO.

Table XIV Summary of the Re-Designed Receiver

	Post-simulation	Measurement	Post-simulation of re-designed receiver
Technology	TSMC 0.18-μm CMOS 1P6M		
Supply voltage	0.6 V	0.65 V/0.7 V	0.6 V
Power consumption	4.4 mW	8.14 mW	3.8 mW
VCO tuning range	5.14-5.36 GHz	5.07-5.3 GHz	5.134-5.366 GHz
Conversion gain	21.7 dB	12.6 dB	21.2 dB
SSB noise figure	13.5 dB	24 dB	13.7 dB
P_{-1dB}	-33.6 dBm	-24 dBm	-32.5 dBm
DC offset	4 mV	< 3 mV	4 mV

Another critical issue in measurement is to confirm the DC voltage of the net between *Mi3* and *Mi5* (*Mi4* and *Mi6*) in the I-channel downconverter, which has to be adequate to ensure that *Mi3* and *Mi5* (*Mi4* and *Mi6*) are in saturation region. A simulation including

device mismatches is utilized to simulate process variation on devices. Suppose a variation in the dimensions of MOS transistors is 10%, the DC voltage of the net between *Mi3* and *Mi5* varies in a range of 74 mV to 125 mV; in this range, *Mi3* and *Mi5* are also in saturation region, shown in Fig. 72. To avoid this problem, a modified circuit is proposed and presented in Fig. 73, where *Mi5* and *Mi6* are used to substitute for the original current source so that *Mi3* and *Mi4* are confirmed in saturation region.

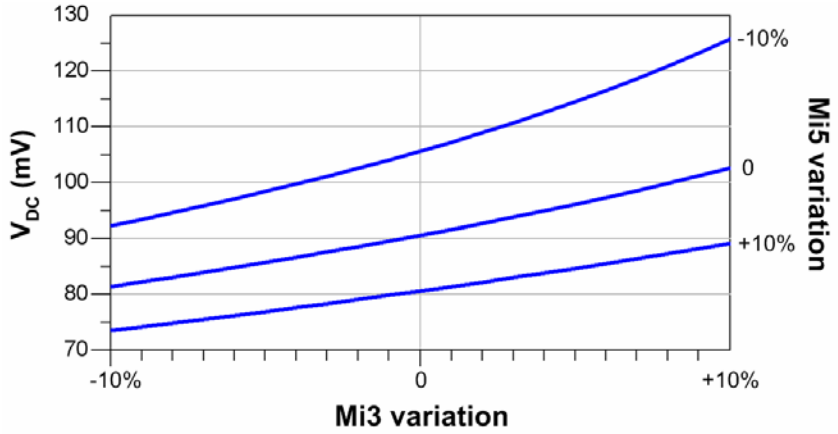


Fig. 72 Simulated DC voltage with device variations on *Mi3* and *Mi5*.

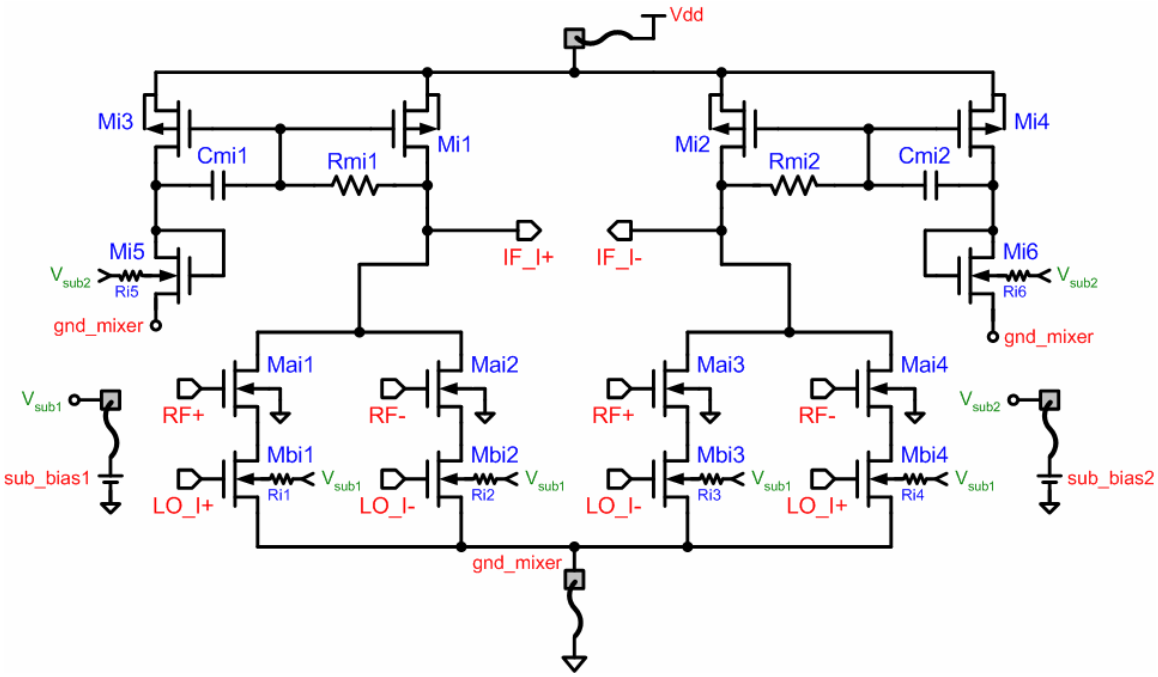


Fig. 73 Modified downconverter.

Table XV compares the designed receiver with three similar arts [12], [15] and [33]. A regular supply voltage of 2.5 V is applied to the first design, realized in 0.25-μm digital CMOS technology. It employs a double downconversion heterodyne architecture with a LO frequency of 2.6 GHz and applies offset cancellation to the baseband amplifiers. Placing the image around the zero frequency, the receiver achieves an image rejection ratio of 62 dB with no external components while minimizing the flicker noise upconversion in the first mixing operation. The design exhibits a low noise figure of 6.4 dB but an output offset voltage of 25 mV. The second design adopts a direct-conversion architecture and proposes a novel offset compensation circuit as the loads of mixer, which is introduced into this thesis. Under a low supply voltage of 1.1 V, this receiver fits the IEEE 802.11a specification and performs a low DC offset of less than 3 mV. The last design under a lower supply voltage of 0.8 V introduces a heterodyne architecture. Although this design performs a low noise figure of 7 dB and a good IIP3 of -1 dBm, it uses numerous inductors to achieve adequate conversion gain under a low supply voltage but covers a lot of chip area. Also, for a conventional double-balanced mixer operating well under such low supply, MOS devices with relatively large widths are adopted. Image-reject capability, a critical issue in heterodyne architecture, should be taken into consideration in this receiver.

Finally, a comparison of performance between the designed receiver and the IEEE 802.11a specification is listed in Table XVI. It is indicated that the re-designed receiver is able to fit the specification.

Table XV Comparison of Performance with Other Proposed 5-GHz Receivers

	This work		[12]	[15]	[33]
	Measurement	Post-simulation of re-design			
Technology	0.18-μm CMOS		0.25-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Architecture	Homodyne		Heterodyne	Homodyne	Heterodyne
Supply voltage	0.6 V/0.7 V	0.6 V	2.5 V	1.1 V	0.8 V
Chip area	4.4 mm^2	—	0.42 mm^2	2.09 mm^2	5.44 mm^2
Power consumption	8.14 mW	3.8 mW	29 mW	37.56 mW	56 mW
Frequency band	4.56-4.68 GHz	5.15-5.35 GHz	5.15-5.35 GHz	5.15-5.35 GHz	5.15-5.35 GHz
VCO tuning range	120 MHz	232 MHz	—	220 MHz	200 MHz
IF frequency	10 MHz	10 MHz	10 MHz	10 MHz	75 MHz
S11	-15 dB	-26 dB	—	-26 dB	-20 dB
Conversion gain	12.6 dB	21.2 dB	43 dB	17.8 dB	6 dB
SSB NF	24 dB	13.7 dB	6.4 dB	14.9 dB	7 dB
P_{-1dB}	-24 dBm	-32.5 dBm	-26.5 dBm	-23 dBm	-10.3 dBm
DC offset	< 3 mV	4 mV	25 mV	1-3 mV	—
Injected input power	-50 dBm	-50 dBm	-64 dBm	-50 dBm	—
Corner frequency	50 kHz	50 kHz	1.5 kHz	150 kHz	—

Table XVI Comparison of Performance with IEEE 802.11a Specification

	Post-simulation	Measurement	Post-simulation of re-design	Requirement
Frequency band	5.14-5.36 GHz	4.56-4.68 GHz	5.134-5.366 GHz	5.15-5.35 GHz
P_{-1dB}	-29.4 dBm (without buffer)	-24 dBm	-28.3 dBm (without buffer)	> -30 dBm
SSB noise figure	13.5 dB	24 dB	13.7 dB	< 15 dB

CHAPTER 4
CONCLUSIONS AND FUTRUE WORKS

4.1 Conclusions

A sub-0.7V 5-GHz direct-conversion receiver front-end composed of a LNA, a set of I/Q downconverters and a quadrature VCO for low-power and wireless applications is designed, fabricated and measured. Under low supply voltages of 0.65 V and 0.7 V, the direct-conversion receiver is proven working well even though it doesn't achieve adequate performance due to an oversight of parasitic effect. Also, the receiver, which consumes only 8.14 mW and covers an area of 4.4 mm^2, performs less power and smaller area than current sub-1V designs [33]. A DC-offset compensation circuit with band-pass filter is applied, and the measured DC offset voltage is less than 3 mV with an input injected power of -50 dBm. The DC-offset compensation circuit is a simple structure and consumes less than 0.5 mW.

In analog/RF circuit design, parasitic effects on metal lines are critical issues. The parasitics of interconnections affect seriously the performance of circuits so that signal paths should be as short as possible in metal routes. To make sure of measurement results being as close as possible to post-simulation results, parasitic effects should be taken completely into considerations during post-simulation while designing circuits next time.

4.2 Future Works

The re-designed circuits with modified spiral inductors should be fabricated to verify their functionalities. For more practicability, an automatic gain control (AGC) circuit, a channel select filter, and an ADC can be included to test the received packet error rate (PER), which is able to indicate linearity, noise and DC offset completely.

For time-varying DC-offset cancellation, a dynamic offset calibration scheme should be

adopted to cancel the DC offsets entirely. Besides, an additional circuit to introduce external LO signal to a receiver can make the measurement of other circuits in a receiver more convenient. Further, a frequency synthesizer can be included to acquire a stable LO signal.

REFERENCES

[1] IEEE Std. 802.11a, Part 11, *Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: High-speed Physical Layer in the 5 GHz Band*, Sep. 1999.

[2] B. Razavi, "Challenges in Portable RF Transceiver Design," *IEEE Mag. Circuit and Devices*, vol. 12, pp. 12-25, Sep. 1996.

[3] B. Razavi, *RF Microelectronics*, Upper Saddle River, NJ: Prentice Hall, 1998.

[4] C. B. Guo *et al.*, "A Fully Integrated 900-Mhz CMOS Wireless Receiver with On-Chip RF and IF Filters and 79-dB Image Rejection," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1084-1089, Aug. 2002.

[5] J. C. Rudell *et al.*, "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2071-2088, Dec. 1997.

[6] A. A. Abidi, "Direct-Conversion Radio Transceivers for Digital Communications," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1399-1410, Dec. 1995.

[7] R. Hartley, "Modulation System," U.S. Patent No.1666206, Apr. 1928.

[8] D. K. Weaver, "A Third Method of Generation and Detection of Single-Sideband Signals," in *Proc. IRE*, vol. 44, Dec. 1956, pp. 1703-1705.

[9] A. Springer, L. Maurer, and R. Weigel, "RF System Concepts for Highly Integrated RFICs for W-CDMA Mobile Radio Terminals," *IEEE Trans. Microwave Theory and Techniques*, vol. 50, pp. 254-267, Jan. 2002.

[10] B. Razavi, "A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LAN's," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1382-1385, Oct. 1999.

[11] A. R. Behzad *et al.*, "A 5-GHz Direct-Conversion CMOS Transceiver Utilizing Automatic Frequency Control for the IEEE 802.11a Wireless LAN Standard," *IEEE J.*

Solid-State Circuits, vol. 38, pp. 2209-2220, Dec. 2003.

[12] B. Razavi, "A 5.2-GHz CMOS Receiver with 62-dB Image Rejection," *IEEE J. Solid-State Circuits*, vol. 36, pp. 810-815, May 2001.

[13] R. Harjani, J. Kim, and J. Harvey, "DC-Coupled IF Stage Design for a 900-MHz ISM Receiver," *IEEE J. Solid-State Circuits*, vol. 38, pp. 126-134, Jan. 2003.

[14] Y. J. Jung *et al.*, "A Dual-Mode Direct-Conversion CMOS Transceiver for Bluetooth and 802.11b," in *Proc.* 29*th ESSCIRC*, Sep. 16-18, 2003, pp. 225-228.

[15] Y. Ding, *Design of Low Voltage 5-GHz CMOS Direct-Conversion Front-End Receiver*, M. thesis, Coll. of Electrical Engineering and Computer Science, National Chiao-Tung University, Hsinchu, Taiwan, Jul. 2004.

[16] K. Y. Lee *et al.*, "Full-CMOS 2-GHz WCDMA Direct Conversion Transmitter and Receiver," *IEEE J. Solid-State Circuits*, vol. 38, pp. 43-53, Jan. 2003.

[17] T. Yamaji and H. Tanimoto, "A 2GHz Balanced Harmonic Mixer for Direct-Conversion Receivers," in *Proc. CICC*, May 5-8, 1997, pp. 193-196.

[18] Z. Zhang, Z. Zhiheng, and J. Lau, "A 900 MHz CMOS Balanced Harmonic Mixer for Direct-Conversion Receivers," in *RAWCON 2000*, Sep. 10-13, 2000, pp. 219-222.

[19] I. Vassiliou *et al.*, "A Single-Chip Digitally Calibrated 5.15-5.825-GHz 0.18-μm CMOS Transceiver for 802.11a Wireless LAN," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2221-2231, Dec. 2003.

[20] P. Zhang *et al.*, "A 5-GHz Direct-Conversion CMOS Transceiver," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2232-2238, Dec. 2003.

[21] M. Lehne, J. T. Stronick, and U. Moon, "An Adaptive Offset Cancellation Mixer for Direct Conversion Receivers in 2.4GHz CMOS," in *Proc. ISCAS*, vol. 1, May 28-31, 2000, pp. 319-322.

[22] J. Stonick *et al.*, "Adaptive DSP Compensation for Analog Distortions in 2.4 and 5.8 GHz Transceivers," *CDADIC Technical Report*, Jul. 1999.

[23] B. Razavi, *Design of Analog CMOS Integrated Circuits*, Boston, MA: McGraw-Hill, 1999.

[24] B. Razavi, "Design Considerations for Direct-Conversion Receivers," *IEEE Trans. Circuits and Systems II*, vol. 44, pp. 428-435, Jun. 1997.

[25] T. Melly *et al.*, "A 1.3V Low-Power 430 MHz Front-End Using a Standard Digital CMOS Process," in *Proc. CICC*, May 11-14, 1998, pp. 503-506.

[26] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd Ed., Boston, MA: McGraw-Hill, 1999.

[27] B. Ravazi, "A 900-MHz CMOS Direct Conversion Receiver," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 12-14, 1997, pp. 113-114.

[28] S. Zhou and M. C. Chang, "A CMOS Passive Mixer with Low Flicker Noise for Low-Power Direct-Conversion Receiver," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1084-1093, May 2005.

[29] M. Zargari, "A 5-GHz CMOS Transceiver for IEEE 802.11a Wireless LAN Systems," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1688-1693, Dec. 2002.

[30] C. H. Park, O. Kim, and B. Kim, "A 1.8-GHz Self-Calibrated Phase-Locked Loop with Precise I/Q Matching." *IEEE J. Solid-State Circuits*, vol. 36, pp.777-783, May 2001.

[31] S. H. Wang *et al.*, "A 5-GHz Band I/Q Clock Generator Using a Self-Calibration Technique," in *Proc.* 28*th ESSCIRC*, Sep. 24-26, 2002, pp. 807-810.

[32] A. Parssinen, "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1893-1903, Dec. 1999.

[33] M. N. El-Gamal, K. H. Lee, and T. K. Tsang, "Very low-voltage (0.8 V) CMOS receiver frontend for 5 GHz RF applications," in *Proc. IEE Circuits Devices Syst.*, vol. 149, Oct.-Dec. 2002, pp. 355-362.

[34] C. H. Chang, *The Design of High-Output-Power RF Power Amplifier Using MOS Devices with Positive Substrate Bias*, M. thesis, Coll. of Electrical Engineering and

Computer Science, National Chiao-Tung University, Hsinchu, Taiwan, Jul. 2004.

[35] H. T. Friis, "Noise Figure of Radio Receivers," in *Proc. IRE*, vol. 32, Jul. 1944, pp. 419-422.

[36] H. S. Kao and C. Y. Wu, "An Improved Low-Power CMOS Direct-Conversion Transmitter for GHz Wireless Communication Applications," in *APCCAS 2002*, vol. 1, Oct. 28-31, 2002, pp. 5-8.

[37] S. Y. Hsiao and C. Y. Wu, "A Parallel Structure for CMOS Four-Quadrant Analog Multipliers and Its Application to a 2-GHz RF Downconversion Mixer," *IEEE J. Solid-State Circuits*, vol. 33, pp. 859-869, Jun. 1998.

[38] C. Y. Wu and H. S. Kao, "A 2-V Low-Power CMOS Direct-Conversion Quadrature Modulator with Integrated Quadrature Voltage-Controlled Oscillator and RF Amplifier for GHz RF Transmitter Applications," *IEEE Trans. Circuits and Systems II*, vol. 49, pp. 123-134, Feb. 2002.

[39] C. Y. Wu and C. Y. Chou, "A 5-GHz CMOS Double-Quadrature Receiver for IEEE 802.11a Applications," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 12-14, 2003, pp. 149-152.

[40] A. V. Ziel, "Gate Noise in Field Effect Transistors at Moderately High Frequencies," in *Proc. IEEE*, vol. 51, pp. 461-467, Mar. 1963.

[41] D. K. Shaeffer and T. H. Lee, *The Design and Implementation of Low-Power CMOS Radio Receivers*, Norwell, MA: Kluwer Academic, 1999.

[42] N. G. Einspruch, Ed., *VLSI Electronics: Microstructure Science*, vol. 18, chap. 1, pp. 1-37, Academic Press, NY, 1989.

[43] E. Abou-Allam and T. Manku, "A Low Voltage Design Technique for Low Noise RF Integrated Circuits," in *Proc. ISCAS*, vol. 4, May 31-Jun. 3, 1998, pp. 373-377.

[44] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz CMOS Wireless LAN Receiver Front End," *IEEE J. Solid-State Circuits*, vol. 35, pp. 765-772, May 2000.

[45] C. Y. Wu and H. S. Kao, “A 1.8 GHz CMOS Quadrature Voltage-Controlled Oscillator (VCO) Using the Constant-Current LC Ring Oscillator Structure,” in *Proc. ISCAS*, vol. 4, May 31-Jun. 3, 1998, pp. 378-381.