Low-Threshold-Voltage TaN/LaTiO n-MOSFETs With Small EOT

S. H. Lin, C. H. Cheng, W. B. Chen, F. S. Yeh, and Albert Chin

***Abstract*—In this letter, we report a low threshold voltage (V_t) of 0.12 V in self-aligned gate-first TaN/LaTiO n-MOSFETs, at an equivalent oxide thickness of only 0.63 nm. This was achieved by using Ni-induced solid-phase diffusion of SiO_2-covered Ni/Sb that reduced the high-κ dielectric interfacial reactions.**

***Index Terms*—LaTiO, low V_t, solid-phase diffusion (SPD).**

I. Introduction

A DIFFICULT challenge for metal-gate/high-κ CMOS [1]–[13] is to suppress the undesirable large flatband voltage ($V_{\rm fb}$) rolloff [7], [8] at smaller equivalent oxide thickness (EOT), which leads to an unwanted high threshold voltage (V_t). To address this issue, an ultrathin SiO_2 layer can be inserted between the high-κ dielectric and Si as used in the 45-nm-node technology with a 1-nm EOT [9]. However, this may not work when the EOT is scaled down to ~0.6 nm. Previously, we have shown that the $V_{\rm fb}$ rolloff and the high V_t are related to charged-oxygen vacancies in the nonstoichiometric oxides (HfO_{2-x} and SiO_x) [7], [8]. This occurs via an inevitable interfacial reaction and interdiffusion [7] due to the close bond enthalpies of the high-κ HfO_2 (802 kJ/mol) and the SiO_2 (800 kJ/mol) [3]. Since this reaction follows an Arrhenius temperature dependence, it can be reduced by using low-temperature processing. This has been verified by the low $|V_t|$ obtained in metal-gate/high-κ CMOS with EOT of 1.05–1.2 nm, using $< 900\ ^\circ$C solid-phase-diffusion (SPD)-formed ultrashallow junctions [7] and laser annealing [8]. In this letter, we report a low V_t of 0.12 V in TaN/LaTiO n-MOSFETs with an EOT of only 0.63 nm. This was achieved by using higher κ LaTiO to decrease the gate leakage current and low-temperature Ni-induced SPD for source-drain to lower high-κ/Si interface reaction exponentially.

Manuscript received May 15, 2009; revised June 21, 2009. First published August 19, 2009; current version published August 27, 2009. This work was supported in part by the National Science Council of Taiwan under Grant NSC 97-2120-M-009-008. The review of this letter was arranged by Editor M. Ostling.

S. H. Lin and F. S. Yeh are with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: d9563815@oz.nthu.edu.tw; fsyeh@ee.nthu.edu.tw).

C. H. Cheng is with the Department of Mechanical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, and also with Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu 300, Taiwan (e-mail: feldcheng@hotmail.com).

W. B. Chen is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: barn.ee95g@nctu.edu.tw).

A. Chin is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, and also with Nano-Electronics Consortium of Taiwan, Hsinchu 300, Taiwan (e-mail: albert_achin@hotmail.com).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2009.2027723

II. Experimental Procedure

Standard p-type Si wafers were used in this letter. The self-aligned gate-first TaN/LaTiO n-MOSFETs were made by depositing TiO_2-doped La_2O_3 (LaTiO with ~25% TiO concentration) on Si substrate using physical-vapor deposition, followed by a postdeposition anneal (PDA). The addition of TiO_2 in LaTiO increases the κ value, which allows the using of a thicker layer to decrease the leakage current and still maintains the small EOT. After TaN deposition and patterning, self-aligned 20-nm Sb and thin Ni were deposited. This was covered with 100-nm-thick SiO_2 followed by a 650 °C RTA [13]. A low sheet resistance of 125 Ω/sq was measured using SiO_2-covered Ni/Sb SPD at 650 °C. After etching nonreacted metal, Al contact metal was added on source-drain to form the n-MOSFETs with 10 μm × 100 μm size. The interface reaction was investigated by secondary ion-mass spectroscopy (SIMS) and transmission electron microscopy (TEM). The fabricated n-MOSFETs were characterized by capacitance–voltage (C–V) and current–voltage (I–V) measurements.

III. Results and Discussion

Fig. 1(a) and (b) shows the C–V and $J-V$ curves of TaN/LaTiO n-MOS devices at various RTA temperatures. High capacitance density of 3.4 μF/cm^2, leakage current of 5×10^{-2} A/cm^2 at -1 V, and proper $V_{\rm fb}$ of -0.52 V were obtained after a 600 °C RTA. This gives an EOT of 0.63 nm by CVC quantum–mechanical C–V simulation, which can be used for 25-nm-node technology with 10-nm gate length at year 2015 according to ITRS [14]. The negative $V_{\rm fb}$ is a unique property of La_2O_3 even with the TaN gate [6]. However, both unwanted EOT degradation and $V_{\rm fb}$ rolloff from -0.52 to -0.27 V were found with increasing RTA temperature from 600 °C to 900 °C. The TEM images of 600 °C and 900 °C RTA samples were also inserted in Fig. 1(a) and (b), respectively. The thickness of the interfacial layer increases with increasing RTA temperature from 600 °C to 900 °C, which matches well the decreasing capacitance density. Such interfacial-layer formation is unavoidable because of the strong bond enthalpy of Si–O (800 kJ/mol) close to La–O (799 kJ/mol) but higher than Ti–O (672 kJ/mol) [3].

$$\mathrm{Si} + \mathrm{LaTiO}_m \xrightarrow[\Delta]{} \mathrm{SiO}_x + \mathrm{LaTiO}_{m-x} \qquad (1)$$

We further used SIMS to study these phenomena. Fig. 2 shows the SIMS profile of the earlier MOS structure after 600 °C and 800 °C RTA. The interdiffusion of the Ti and Si was

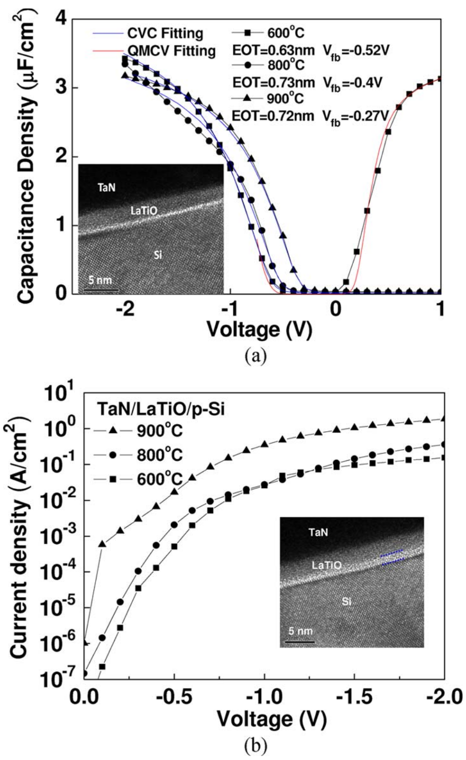

Fig. 1. PDA temperature dependence of (a) C–V and (b) $J-V$ characteristics of TaN/LaTiO/p-Si n-MOS devices. The 600 °C data were measured in a MOSFET from accumulation to inversion, while the 800 °C and 900 °C data were measured in MOS capacitors from accumulation to depletion. The inserted TEM images in (a) and (b) are the samples after 600 °C and 900 °C RTA.

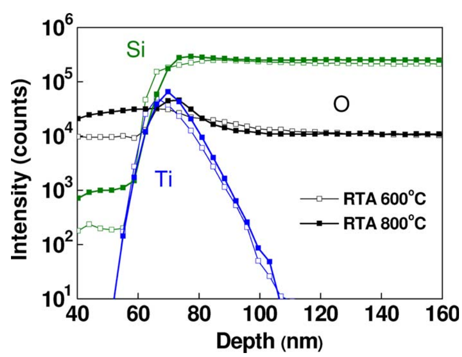

Fig. 2. SIMS profile of LaTiO after 600 °C and 800 °C RTA treatments.

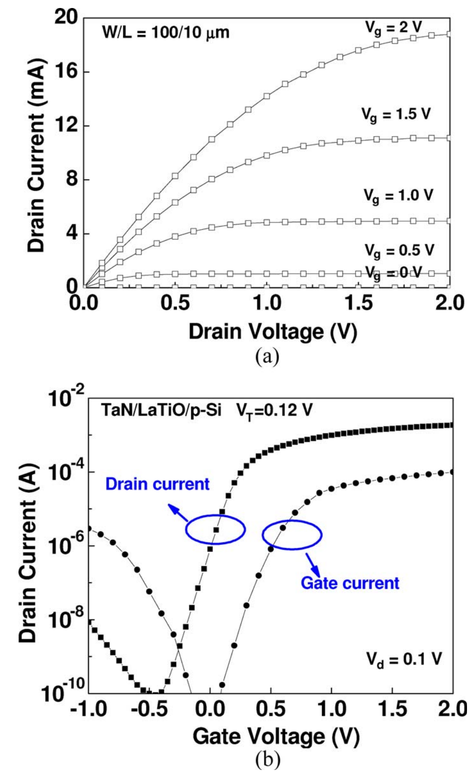

Fig. 3. (a) I_d–V_d and (b) I_d–V_g and I_g–V_g characteristics of self-aligned gate-first n-MOSFETs, where the LaTiO gate dielectric is treated with a 600 °C RTA.

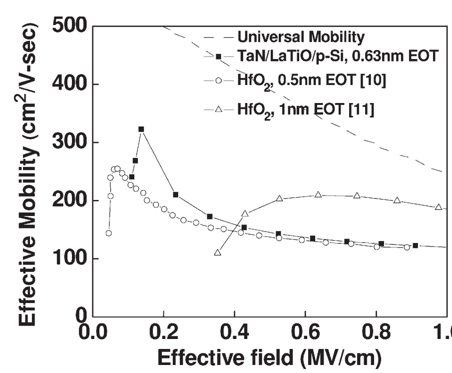

Fig. 4. Electron mobility of the n-MOSFETs extracted from the I_d–V_g curves shown in Fig. 3(b).

found with increasing the RTA temperature. The oxygen peak in the high-κ dielectric shifts toward the Si, suggesting the formation of interfacial silicate from thermal-dynamic considerations [7]. This interface layer is further observed by cross-sectional TEM, which is unavoidable unless a thick enough interfacial SiO_2 is inserted between high-κ and Si to decrease the interface reaction and interdiffusion.

This additional interfacial layer cannot explain the unexpected leakage-current increase after 900 °C RTA. We have used X-ray diffraction to measure the crystallinity of the LaTiO after various RTA. The amorphous LaTiO becomes crystallized at 900 °C RTA. Therefore, the higher leakage current after the 900 °C RTA may be related to the formation of polycrystals that provide extra leakage paths through highly defective grain boundaries [15]. This further emphasizes the importance of the proposed low-temperature processing.

To lower the interfacial reaction, we have used Ni-induced SPD for source-drain regions of TaN/LaTiO n-MOSFET. Fig. 3(a) and (b) shows the I_d–V_d and I_d–V_g characteristics. Besides the good transistor characteristics, a low V_t of 0.12 V was measured at 0.63-nm EOT. Fig. 4 shows the effective mobility derived directly from the I_d–V_g curves. The mobility data of 0.5-nm EOT $NiSi/HfO_2/HfSiO_x$ and 1.0-nm EOT TiN/HfO_2 n-MOSFETs were also plotted for comparison [10], [11]. A mobility of 126 $cm^2/V \cdot s$ was obtained in TaN/LaTiO n-MOSFET at 0.8 MV/cm with a 0.63-nm EOT. This value is slightly higher that for $NiSi/HfO_2/HfSiO_x$ device at 0.5-nm EOT [10], along with a very low V_t of 0.12 V. Such low V_t is due to the unique negative $V_{\rm fb}$ of La_2O_3 dielectric. However, the mobility is significantly smaller than the TiN/HfO_2 n-MOSFET at 1.0-nm EOT [11]. Similar mobility decrease with decreasing EOT was also reported in the literature [10], [12]. Such mobility degradation at small EOT is unavoidable due to the less interfacial SiO_x allowed at thinner EOT. This further increases the interface charged-oxygen vacancies in (1) formed by interface reaction and interdiffusion after standard 1000 °C RTA. Further mobility improvement can be reached by adding an ultrathin SiON, although this is traded off by the EOT scaling.

IV. Conclusion

Using a simple process, we have fabricated metal-gate/high-κ TaN/LaTiO n-MOSFET with a low V_t of 0.12 V at 0.63-nm EOT. Besides, this device has the advantages of simple self-aligned and gate-first process compatible with current VLSI.

References

[1] H.-H. Tseng, C. C. Capasso, J. K. Schaeffer, E. A. Hebert, P. J. Tobin, D. C. Gilmer, D. Triyoso, M. E. Ramón, S. Kalpat, E. Luckowski, W. J. Taylor, Y. Jeon, O. Adetutu, R. I. Hegde, R. Noble, M. Jahanbani, C. El Chemali, and B. E. White, "Improved short channel device characteristics with stress relieved pre-oxide (SRPO) and a novel tantalum carbon alloy metal gate/HfO2 stack," in *IEDM Tech. Dig.*, 2004, pp. 821–824.

[2] T. Nabatame, M. Kadoshima, K. Iwamoto, N. Mise, S. Migita, M. Ohno, H. Ota, N. Yasuda, A. Ogawa, K. Tominaga, H. Satake, and A. Toriumi, "Partial silicides technology for tunable work function electrodes on high-k gate dielectrics—Fermi level pinning controlled $PtSi_x$ for $HfO_x(N)$ pMOSFET," in *IEDM Tech. Dig.*, 2004, pp. 83–86.

[3] D. S. Yu, A. Chin, C. H. Wu, M.-F. Li, C. Zhu, S. J. Wang, W. J. Yoo, B. F. Hung, and S. P. McAlister, "Lanthanide and Ir-based dual metal-gate/HfAlON CMOS with large work-function difference," in *IEDM Tech. Dig.*, 2005, pp. 649–652.

[4] C. H. Wu, D. S. Yu, A. Chin, S. J. Wang, M.-F. Li, C. Zhu, B. F. Hung, and S. P. McAlister, "High work function Ir_xSi gates on HfAlON p-MOSFETs," *IEEE Electron Device Lett.*, vol. 27, no. 2, pp. 90–92, Feb. 2006.

[5] X. P. Wang, C. Shen, M.-F. Li, H. Y. Yu, Y. Sun, Y. P. Feng, A. Lim, H. W. Sik, A. Chin, Y. C. Yeo, P. Lo, and D. L. Kwong, "Dual metal gates with band-edge work functions on novel HfLaO high-κ gate dielectric," in *VLSI Symp. Tech. Dig.*, 2006, pp. 12–13.

[6] C. H. Wu, B. F. Hung, A. Chin, S. J. Wang, X. P. Wang, M.-F. Li, C. Zhu, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang, "High temperature stable $[Ir_3Si\text{-}TaN]/HfLaON$ CMOS with large work-function difference," in *IEDM Tech. Dig.*, 2006, pp. 617–620.

[7] C. F. Cheng, C. H. Wu, N. C. Su, S. J. Wang, S. P. McAlister, and A. Chin, "Very low V_t [Ir–Hf]/HfLaO CMOS using novel self-aligned low temperature shallow junctions," in *IEDM Tech. Dig.*, 2007, pp. 333–336.

[8] C. C. Liao, A. Chin, N. C. Su, M.-F. Li, and S. J. Wang, "Low V_t gate-first $Al/TaN/[Ir_3Si\text{-}HfSi_{2-x}]/HfLaON$ CMOS using simple process," in *VLSI Symp. Tech. Dig.*, 2008, pp. 190–191.

[9] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging," in *IEDM Tech. Dig.*, 2007, pp. 247–250.

[10] M. Takahashi, A. Ogawa, A. Hirano, Y. Kamimuta, Y. Watanabe, K. Iwamoto, S. Migita, N. Yasuda, H. Ota, T. Nabatame, and A. Toriumi, "Gate-first processed $FUSI/HfO_2/HfSiO_x/Si$ MOSFETs with EOT = 0.5 nm—Interfacial layer formation by cycle-by-cycle deposition and annealing," in *IEDM Tech. Dig.*, 2007, pp. 523–526.

[11] S. Datta, G. Dewey, M. Doczy, B. S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick, and R. Chau, "High mobility Si/SiGe strained channel MOS transistors with HfO_2/TiN gate stack," in *IEDM Tech. Dig.*, 2003, pp. 653–656.

[12] W. Tsai, L.-Å. Ragnarsson, L. Pantisano, P. J. Chen, B. Onsia, T. Schram, E. Cartier, A. Kerber, E. Young, M. Caymax, S. De Gendt, and M. Heyns, "Performance comparison of sub 1 nm sputtered TiN/HfO_2 nMOS and pMOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 311–314.

[13] S. H. Lin, S. L. Liu, F. S. Yeh, and A. Chin, "Low V_t TaN/HfLaO n-MOSFETs using low temperature formed source-drain junctions," *IEEE Electron Device Lett.*, vol. 30, no. 1, pp. 75–77, Jan. 2009.

[14] International Technology Roadmap for Semiconductors, Process Integration, Devices, and Structures Chapter, p. 11. [Online]. Available: www.itrs.net/Links/2007ITRS/2007_Chapters/2007_PIDS.pdf

[15] K. C. Chiang, A. Chin, C. H. Lai, W. J. Chen, C. F. Cheng, B. F. Hung, and C. C. Liao, "Very high κ and high density TiTaO MIM capacitors for analog and RF applications," in *VLSI Symp. Tech. Dig.*, 2005, pp. 62–63.