1.25 億位元/每秒資料回復電路設計與實現

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摘要

隨著互補式金氧半製程技術的發展，以及處理器運算能力的快速提昇，提示著用以傳輸資訊的寬頻資料連結越來越顯得需要。在許多的應用中，比如說電腦內部、電腦與電腦間和電腦與週邊間的介面，這樣的連結通常是一個很重要的部分。為了克服在資料傳輸過程中由各種雜訊源所導致的訊號完整性問題，接收器在整個高速連結效能的表現中扮演了一個重要的角色，而其中最複雜的部分就是資料回復電路的設計。傳統上，GaAs 和Si bipolar 等製程都較常被使用在這樣高速電路，然而，由於互補式金氧半製程本身低成本、低功率、高度整合的優勢，目前深次微米互補式金氧半製程也已經被考慮使用在這些高速電路。

論文主題在於使用標準互補式金氧半製程實現一個雙回路系統1.25Gb/s時脈資料回復電路。內容可分為五章，第一章為簡介，第二章以時脈資料回復電路的基本原理作為開始。然後，在設計系統參數的複雜取捨將被討論並且也討論所建議的架構工作原理，第三章描述使用一些電路可支援高效能、低成本、短的設計時間和可量測的設計與應用，此方法可符合1.25Gb/s 的輸入資料速率。第四章介紹超大型積體電路實行的注意事項，第五章總結此論文。

Design and Realization of a 1.25 Gb/s Clock and Data Recovery Circuit

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Abstract

The scaling of CMOS process technologies and the increasing computational capability of processors, indicate that high bandwidth links to communicate the information are needed. Such high speed links are often important parts of innercomputer, computer-to-computer or computer-to-peripheral interfaces. To overcome the signal integrity problems induced by various noise sources during data transmission period, the receiver design plays an important role in the overall performance of high speed links. The design of clock and data recovery circuits is the most complicated part of implementation. transceiver. Traditionally, such high-speed circuits used for multi-Gb/s data communication were implemented with either GaAs MESFET or Si bipolar technology. However, the deep sub-micron CMOS technology is now being considered in these high-speed circuits because of its low cost, low power dissipation, and highly integrated capability.

The goal of this work is to use a standard CMOS process to implement a 1.25 Gb/s dual-loop clock and data recovery (CDR) circuit. This thesis could be divided into five chapters. The chapter 1 is introduction. The chapter 2 starts with the basics

of the CDR. Then, the trade-off involving in several design parameters of the system will be discussed. Chapter 3 discusses the circuit design for high performance, low cost, short design time and testable design. The methodology could be applied for a 1.25 Gb/s CDR circuit. In chapter 4, we present matters needing attention about VLSI implementation. Chapter 5 summarizes this work.

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