Chapter 1

Introduction

1.1 Motivation

The clock and data recovery (CDR) has become so important in electronics over the past ten years. The volume of data transported over the telecommunications network increased mainly due to increased internet traffic [1]. The call for technologies, such as Local Area and Wide Area Network (LAN, WAN), Fiber To The Home [2] and the board-to-board interconnections between computers [3], which expand the capacity of fiber-based transport links to Gb/s degree has risen in response to this explosion in data traffic.

The design of clock and data recovery circuits is the most complicated part of implementing an optical transceiver. Traditionally, such high-speed circuits used for multi-Gb/s data communication were implemented with either GaAs MESFET or Si bipolar technology. However, the deep sub-micron CMOS technology is now being considered in these high-speed circuits because of its low cost, low power dissipation, and highly integrated capability.

1.2 Fiber-Optic Transceiver

Figure 1-1 shows a common fiber-optic data communication system consisting of a transmitter and a receiver. At transmitter side, a line multiplexer that manages several parallel signals and interleaves them into a serial output. The output stream is sent to a laser driver and turned into optical signal through a laser diode. The optical signal travels through a fiber to the receiver side.

At the receiver side, it uses a photodiode to convert the incoming non-return to zero (NRZ) optical pulses from a fiber channel to a current. These current pulses are then converted by the transimpedance (TZ) amplifier into a voltage. The pulses are low-pass filtered to remove out-of-band noise, thereby improving the received signal-to-noise ratio (SNR). An automatic gain control amplifier (AGC) provides additional amplification while compensating for variations in the received signal power. One of the important blocks is the CDR block in the receiver end. This block recovered the timing information that is lost at the input to the fiber channel. This means that if the clock signal is used to retime the data, the sampling occurs at the optimum position, improving the bit error rate (BER) of the receiver. Finally, it is applied to a 1:N time-division demultiplexer (DEMUX) to separate several low-speed outputs.

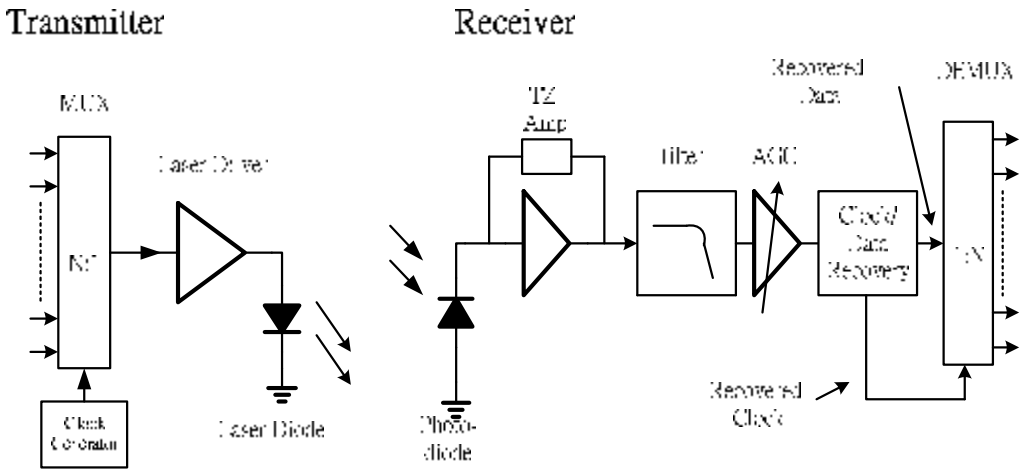

Fig. 1-1 Typical Fiber-Optic Transceiver

1.3 Data Format

The way to transmit digital signals is to use two different voltage levels for the binary digits. Codes that follow this strategy share the property that the voltage level is constant during a bit interval. As shown in Figure 1-2, in this format each bit has a duration of Tb (“bit period”), is equally likely to be ZERO or ONE, and is statistically independent of other bits. A NRZ data allows arbitrarily long sequences of “1” or “0”. Since the transition between “1” and “0” or vice versa provides all the frequency information in the data stream, there is an absence of clocking information during the consecutive identical digits. In this work, the NRZ data is used as the input of the CDR circuit.

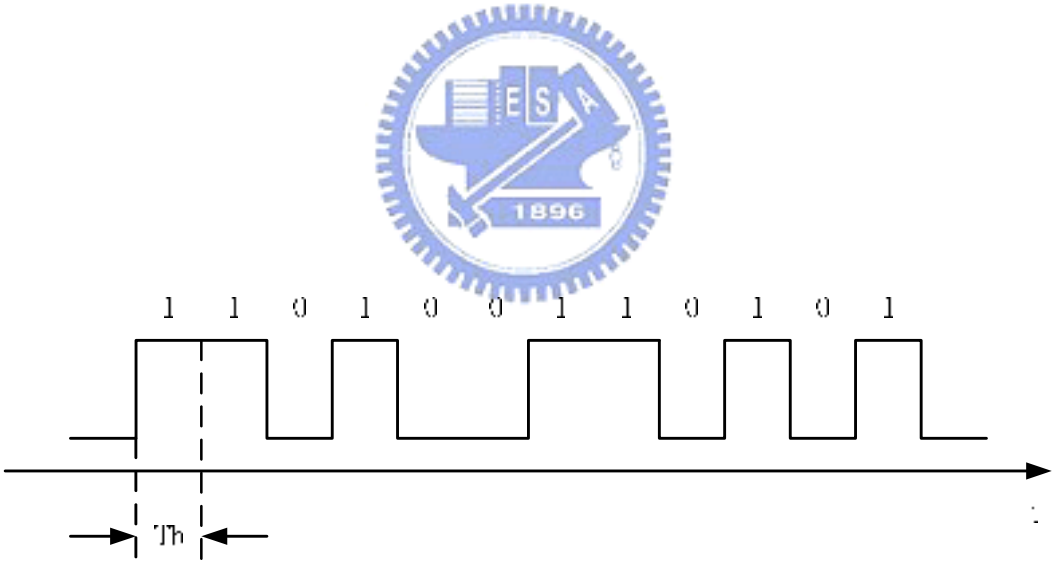

Fig. 1-2 NRZ data

1.4 Timing Margin Analysis

The synchronization issue is usually illustrated using a data eye in the receiver end. It offers the key to the understanding of a good estimation. Figure 1-3 shows the eye diagram of the received data. The best point to sample data is at the center of the eye, which minimizes the timing margin for data reception. The maximum data transfer rate is determined by the following parameters, as shown in the following[4] :

(1)$T_{\text{tx jitter}}$**:** the transmitter's clock jitter. It is introduced by the noise and the clock jitter on the transmitter side.

(2)T_{ISI}**:** the inter-symbol-interference. This is the sum of the rise/fall time of the signal plus the uncertainty in the total signal delay.

(3)$T_{\text{rx sh}}$**:** the sample-and-hold time of the sampler, i.e., the time zone around the sampling time during which a changing input signal can result in an undefined receiver output.

(4)$T_{\text{rx jitter}}$**:** the receiver's clock jitter. It is caused by power supply and substrate noise resulting from the switching of digital logics or output buffers to introduce timing error on the receiver side.

(5)T_{OS}**:** the static sampling error. The static sampling offset typically resulting from the systematic clock skew deviate the average position of the sampling points from the center of the data eye.

(6)T_{B}**:** the time for the bit cell.

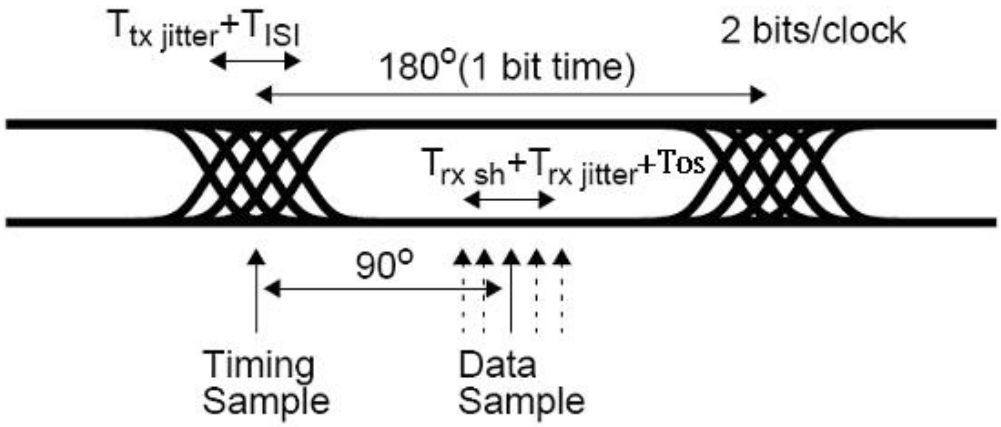

Fig. 1-3 Received Data Eye

Therefore, the timing margin of the clocking scheme, which can be viewed as the tolerance to additional delay uncertainty, is given by:

$$T_{margin} = T_B - (T_{tx\ jitter} + T_{ISI}) - (T_{rx\ sh} + T_{rx\ jitter} + T_{OS}) \quad (1.1)$$

1.5 Thesis Overview

The thesis comprises five chapters of which this introduction is the first. The chapter 2 starts with the basics of the CDR. Then, the trade-off involving in several design parameters of the system would be discussed. Chapter 3 discusses the circuit design more detailed in transistor level. In chapter 4, we present the VLSI implementation and several physical design strategies used to minimize noise coupling and facilitate testing. Chapter 5 summarizes this work.