Chapter 2

Clock and Data Recovery Architectures

2.1 Principle of Operation

This chapter discusses the design issues related to the CDR architectures. The bang-bang CDR architectures have recently found wide usage in high-speed applications [5], [6]. The most common bang-bang CDR is based on Alexander phase detector [7], which works at a full-rate clock frequency. To achieve higher operational speed in a technology with a low transistor cutoff frequency, a half-rate phase detector is necessary to increase the throughput of the system [8]. In this work, the CDR contains several major building blocks.

(1) Phase detector: A digital circuit senses the phase difference between the input data and the half-rate clock only on data transitions.

(2) Frequency detector: The digital quadricorrelator technique is adopted [9]. At initial state, a fundamental property of the digital quadricorrelator frequency detector (DQFD) is to produce output signals, which control charging and discharging currents according to the frequency difference between incoming NRZ data and recovered clock. After the frequency detector's operation, pulls in the VCO frequency to a certain range compared with the data rate. The frequency detector is automatically disabled itself and doesn't disturb the loop.

(3) Voltage-controlled oscillator: A local clock generator which is aligned to the incoming NRZ data and provides half-quadrature phases for the half-rate frequency detector. Recovered clock from the VCO is used to sample the incoming NRZ data.

The proposed half-rate CDR circuit consisting of the half-rate DQFD, a voltage-controlled oscillator, a half-rate phase detector, and two charge pumps, as shown in figure 2-1. At first, both the DQFD and the PD compare the incoming NRZ data and recovery at the same time. Secondly, the frequency-locked loop, which is constructed from Loop2, detects the frequency difference between the incoming NRZ data and the recovered clock. This DQFD pulls the VCO output frequency to the data rate. Thirdly, the DQFD automatically disables itself while the frequency is locked. This means that the whole loop is dominated by Loop1 and the Loop2 doesn't disturb the whole loop. Finally, the operation is completed and the CDR can achieve fast locking and wide pull-in range due to DQFD.

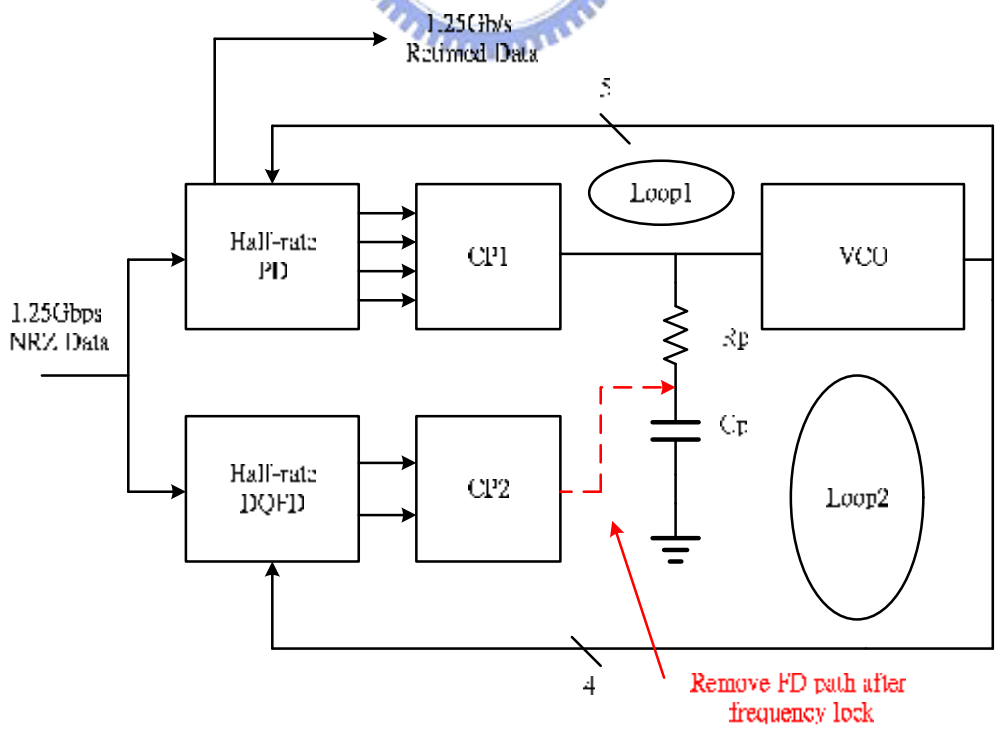


Fig. 2-1 Half-rate CDR architecture

2.2 CDR Fundamental

Generally, the task of the CDR architecture is to recovery the phase-and-frequency information from the input by extracting the clock from the rising edges of the data stream. Figure 2-2 shows a common half-rate CDR to regenerate the data stream in locked state. We can see the CDR sample the data stream with rising/falling edges of Clock1 and extract the correct data from the outputs of two decision circuits with Clock2. We can discuss the building block in detail in the following subsections.

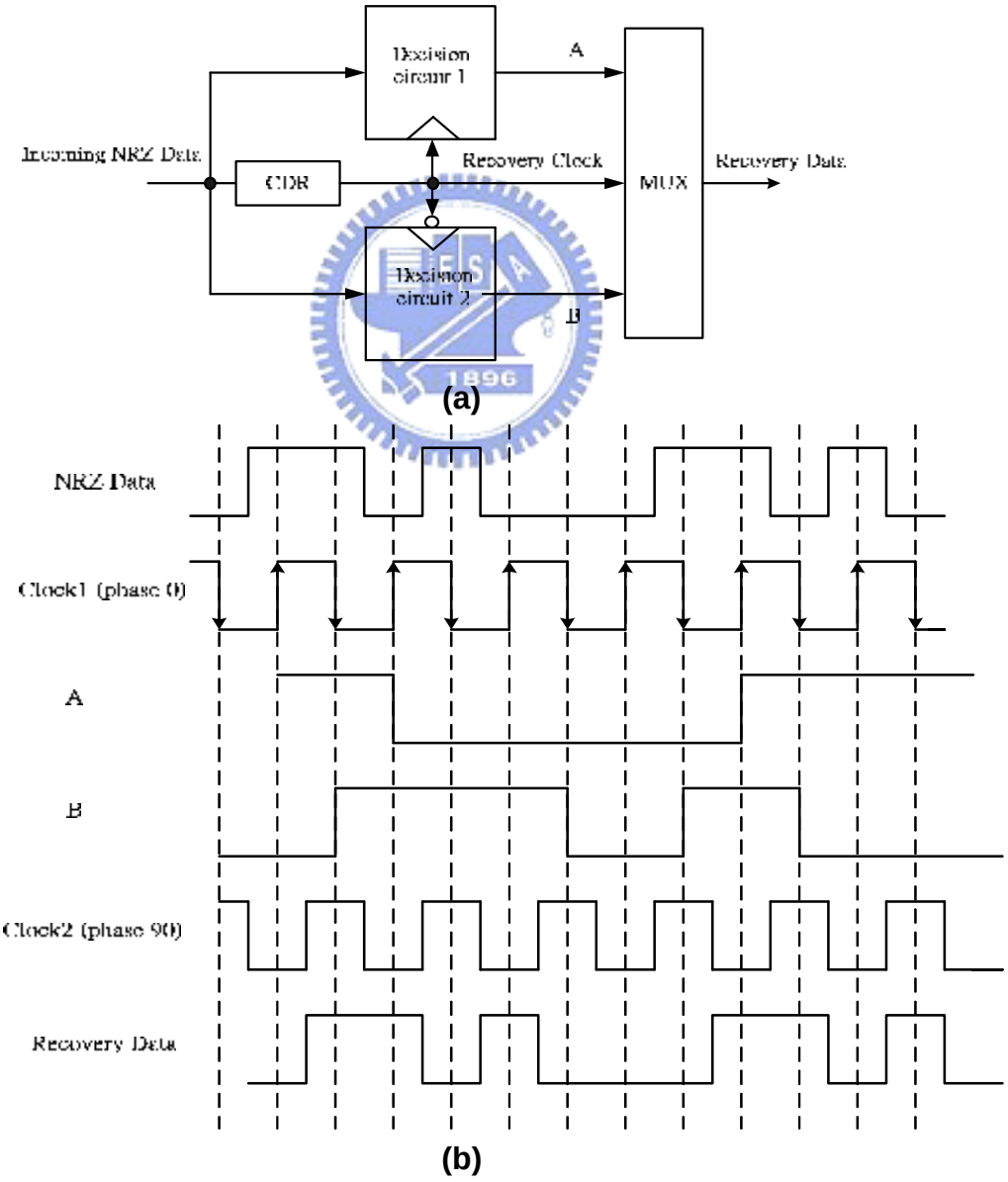
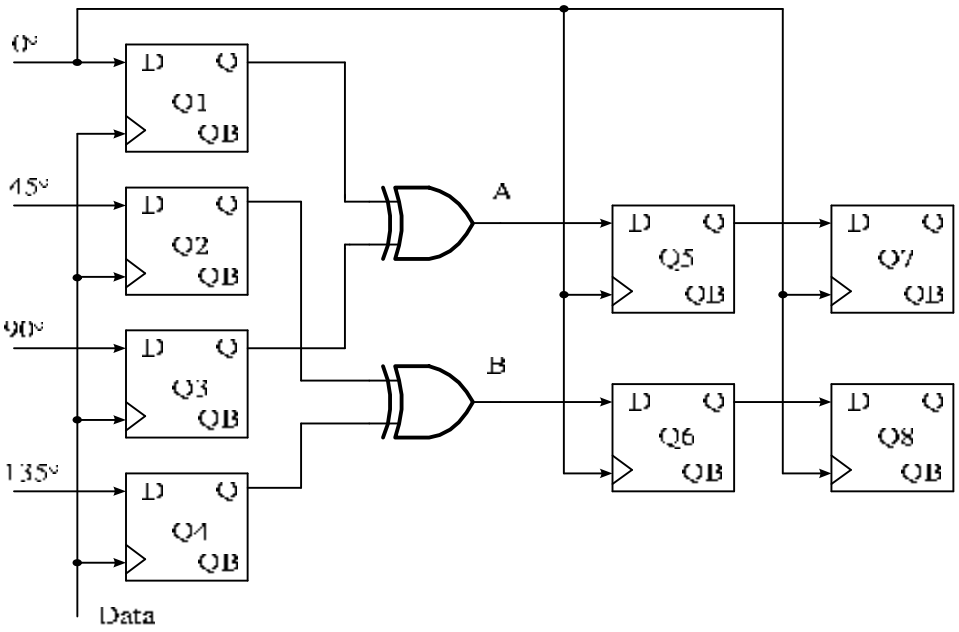


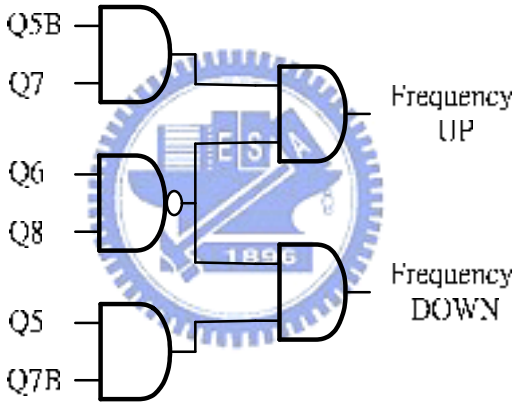
Fig. 2-2 A Data Regeneration (a) scheme, (b) timing diagram

2.2.1 Frequency Detector

The loop bandwidth of CDRs [5], [10]-[12] should be small to improve noise performance. However, it will result in small capture and pull-in ranges. CDRs without frequency acquisition loops might need either additional reference clock [11] or off-chip tuning [12]. Digital quadricorrelator [13], [14] have been widely used in frequency acquisition. However, the conventional digital quadricorrelator frequency detector [14] could be suitable for CDRs with full-rate clocks. To reduce the power consumption, clock relaxing techniques [5]-[6], [10]-[12] have been applied to achieve higher transmission rate with lower clock rate. For the half-rate CDR, we employ a half-rate frequency detector to improve the capability of frequency acquisition [9]. In the initial state, the CDR is out of lock. The digital quadricorrelator frequency detector should produce a useful output signal to pull the frequency of VCO to the half data rate. When the frequency lock is achieved, the digital quadricorrelator frequency detector will disable itself. As shown in Figure 2-3, the digital quadricorrelator frequency detector can be realized by eight DFFs, two XOR gates, and combinational logics.



(a)



(b)

Fig. 2-3 (a) Schematic of half-rate DQFD (b)Combinational logics

According to the results of 0°, 45°, 90°, and 135°are sampled by input data, each half of clock period can be divided in to four states, I, II, III, and IV, as shown in figure 2-4. In this quadricorrelator frequency detector, four DFFs (Q5-Q8) triggered by clock of 0° will store the sampled values and record the states. There is a rising edge of clock of 0° to ensure this state to have been recorded. In other words, all valid state transitions have to rotate counterclockwise and cross the arrow in figure 2-4. The arrow represents the edge of clock of 0° to rise at the boundary between state IV and state I.

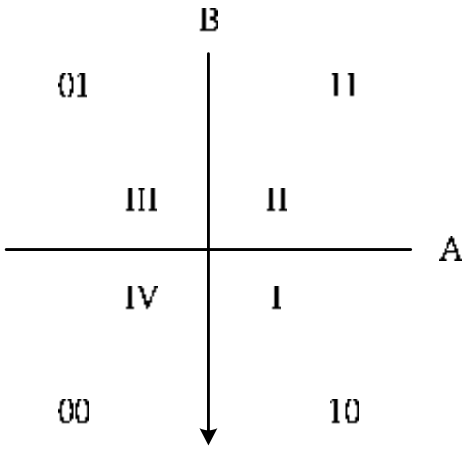


Fig. 2-4 State representation

The operational principle of the half-rate quadricorrelator frequency detector will be discussed in the following. For a slow periodic data as shown in figure 2-5(a), suppose that the first rising edge of data appears at the boundary between state III and state IV. Then the second rising edge appears ate the boundary between state IV and state I. The state transition rotated from state IV to state I would be detected. This state transition would indicate that the clock rate is faster than the half data rate; i.e., frequency DOWN should be active. For a fast periodic data in figure 2-5(b), the first rising edge appears at the boundary between state I and state II. The second one appears at the boundary between state IV and state I. Then the third one appears at the boundary between state III and state IV. We should consider two cases related to the operation in fast periodic data. Case 1, the data leads a little; i.e., the first rising edge appears at the state I. The state transition rotated from state I to state IV would be detected. Case 2, the data lags a little; i.e., the first rising edge appears at the state II. We can find the state transition rotated from state I to state IV occur due to the second one and third one. This state transition would indicate that the clock rate is slower than the half data rate; i.e., frequency UP should be active. Two additional state

transitions, such as state transition from state I to state III and state transition from state II to state IV, are chosen to aid the speed-up process. Similarly, two additional state transitions, such as state transition from state III to state I and state transition from state IV to state II, are chosen for the slow-down process.

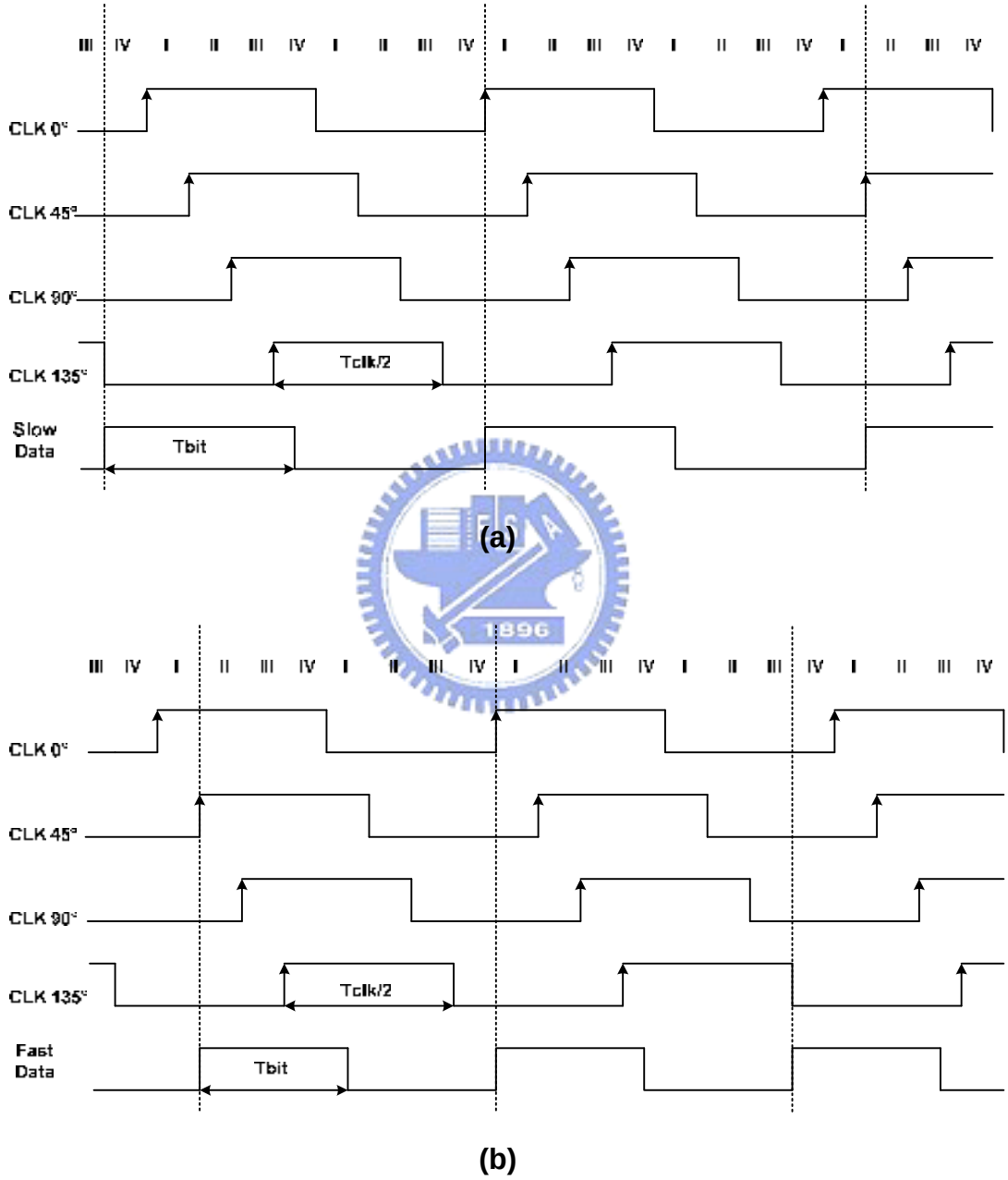


Fig. 2-5 Timing diagram for (a) slow periodic data (b) fast periodic data

Since the state varies with the input data and four different phase of the VCO output, the following state will be any possible state. In order to analyze these state conveniently, we define a three-state logic. As shown in figure 2-6. It contains three states: Frequency UP, Frequency DOWN, and Don't care. When state I rotates to state III or state IV and state II rotates to state IV, the VCO output frequency goes up. When state IV rotates to state I or state II and state III rotates to state I, the VCO output frequency goes down. Other cases are "Don't care".

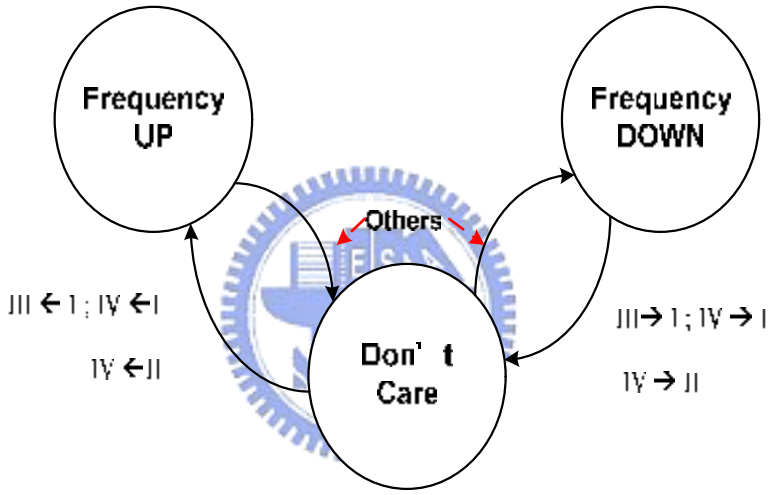


Fig. 2-6 A three-state logic of the half-rate DQFD

We have to deal with the diagram of the three-state logic, which decide the operations of the half-rate digital quadricorrelator due to the state changes, see in Table 2-1. According to the logic table, we can obtain the combinational circuit in detail. This type of frequency detector has two major advantages. One is that the synchronous processing guarantees the frequency detector automatically disabled when the VCO output frequency is equal to the half data rate and there is no need additional circuit to turn off the frequency detector in the lock state. It means the frequency detector does not disturb the system in the lock state and we can achieve

low jitter performance. The other, the half-rate digital quadricorrelator frequency detector can detect the frequency difference between the input data stream and the VCO clock. There is a considerable issue related to the mismatch between the quadrature clocks. The mismatch will affect the operation of the half-rate quadricorrelator frequency detector. To improve this issue, additional dummy cells should be necessary.

Table 2-1 Logic table of the half-rate DQFD

current state Q7Q8 \ Q5Q6 Previous state	State I	State II	State III	State IV
	10	11	01	00
State I 10	X	X	DOWN	DOWN
State II 11	X	X	X	DOWN
State III 01	UP	X	X	X
State IV 00	UP	UP	X	X

2.2.2 Phase Detector

The phase detector plays a critical role in determining the purity of the clock data recovery from the received data. The phase detector must be able to cope with random NRZ data and recover the clock that is associated with the data stream. We usually use a linear phase detector or a digital bang-bang phase detector. A linear phase detector exhibits low jitter performance in the lock condition, but suffers from nonlinearity for non-uniform data patterns and requires an external loop filter. In addition, it is difficult to design and is highly sensitive to mismatch. A previously proposed linear phase detector [15] uses an unconventional 2.6V supply for a 0.18 μm CMOS process, and requires an precise signal comparison to generate the phase error signal. An alternative phase detector [16] is sensitive to the clock and data duty cycle. A digital bang-bang phase detector is less sensitive to data patterns and can be fully integrated in a CMOS process. The main problem with such a detector is the generation of a high ripple over the control line of the oscillator during the lock condition resulting in high jitter [8]. It provides simplicity in design and better phase adjustment at high speed in spite of higher jitter [17].

In this work, we will employ a four-step digital bang-bang phase detector to replace the conventional two-step one to improve the performance of the system [18]. The detailed implementation, which was raised earlier in this chapter, will be discussed further more in the next chapter.

2.2.3 Voltage-Controlled Oscillator

Generally, the ring oscillator generate a square output waveform with its frequency controlled by the control voltage, as shown in figure 2-7(a).Figure 2-7(b) shows the characteristic of VCOs, where f1 and f2 are the output frequencies corresponding to the control voltages of V1 and V2 respectively, and the slope Kvco is the gain of the VCOs. Gain and linearity are most important to CDR systems. We will define some specifications of VCO are [18]

(1) Tuning linearity: An ideal VCO has a constant VCO gain, Kvco, at the entire frequency range, as shown in figure 2-7(b).

(2) Tuning range: the range between the minimum and maximum values of the VCO frequency

(3) Power supply sensitivity: Some VCOs with relatively low sensitivity to noise on the power supply. In 1.25 Gbps clock recovery applications with multiple channels on the same die. The power supply Vdd will be lower than the nominal value when switching activities are frequent [19]. Beside, the switching noise introduced by digital circuits will also couple to Vdd of a VCO and influence its output waveform. Therefore, this effect must be reduced as low as possible.

(4) Phase stability: An ideal spectrum of the VCO output should be looked like the Dirac-impulse. In other words, the phase noise of the VCO output must be as low as possible.

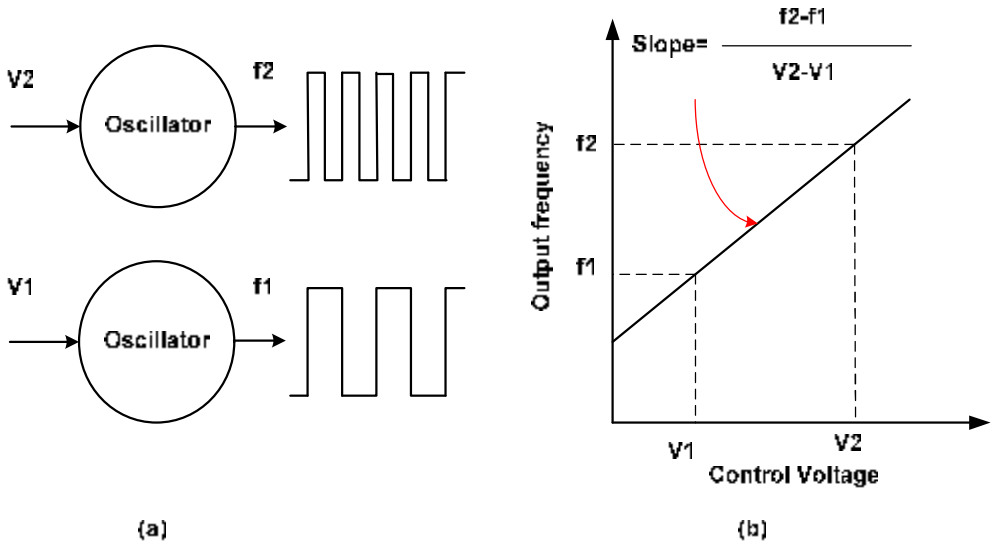


Fig. 2-7 Illustration of the VCO (a) model of the oscillator (b) characteristic

2.2.4 Loop Filter

The low-pass filter lies between the phase detector output and the voltage control line of the VCO. It has a lead-network consisting of a resistor Rp in series with capacitor Cp and a capacitor Cs in parallel. The lead-network filter provides a pole in the original to provide an infinite DC gain to get the zero static phase error, and a zero in the open loop response in order to improve the phase margin to ensure overall stability of the loop. The transfer function of the filter is given by

$$F(s) = \frac{Kh \times (S + w_z)}{S} \tag{2.1}$$

Where

$$\omega z = \frac{1}{RpCp},\ Kh = Rp \tag{2.2}$$

Capacitor C2 is used to provide higher-order roll off for reducing the ripple noise to mitigate frequency jump. The total transfer function of the loop filter is

$$F(s) = \frac{Kh \times (s + w_z)}{s \times (1 + \frac{s}{w_p})} \tag{2.3}$$

Where

$$w_z = \frac{1}{RpCp}, w_p = w_z \times (1 + \frac{Cp}{Cs}), Kh = \frac{Rp \times Cp}{Cp + Cs} \qquad F(s) = \frac{Kh \times (S + w_z)}{S} \qquad (2.4)$$

But the adding of the capacitor Cs will make the overall system become third-order one and affect the stability of the loop. In general, by setting Cp>20×Cs, the third-order can be approximated to second-order loop.

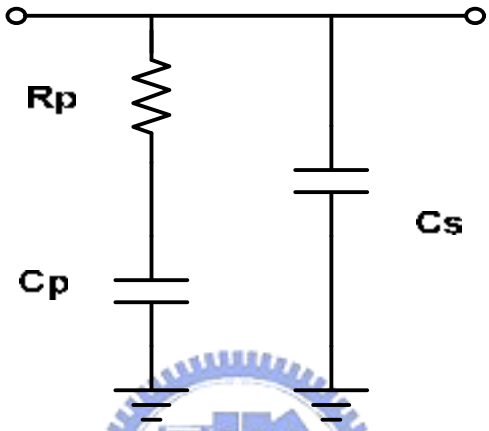


Fig. 2-8 A second-order low-pass filter

2.3 Loop Performance Analysis

Since the digital bang-bang phase detector is a nonlinear circuit, it is different from the linear phase detector [5], [20], which can be analyzed more effectively and directly. Recent years, there are some technical literatures which have provided the analysis of a PLL-based CDR with a bang-bang phase detector [21]-[25]. In this work, we imitate the analysis of a linear PLL-based CDR since we use the four-step bang-bang phase detector, which provides less quantization error than conventional bang-bang phase detector [21]. In the loop performance analysis, the frequency detector can be neglected because it dose not affect the system as soon as the lock is acquired. The approximate model of the CDR with a four-step bang-bang phase detector is shown in figure 2-9, where Kpd is the gain of the phase detector , Kvco is

the gain of the VCO, an F(s) is the transfer function of the loop filter. We can observe the model is similar to the one in the CDR with a linear phase detector.

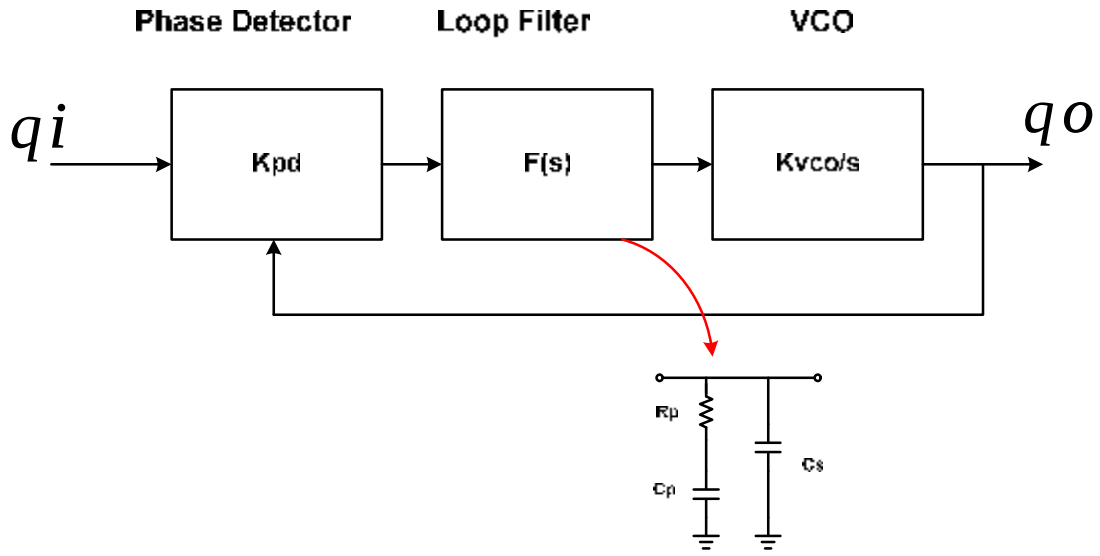


Fig. 2-9 Model of the CDR

Considerable insight can be obtained into the design of the CDR by first considering its open-loop response. This response can be derived by breaking the loop at the feedback input of the phase detector. The output phase, θ o(s), is related to the input phase, θ i(s), by

$$qo(s) = qi(s) \times Kpd \times F(s) \times \frac{Kvco}{s} \tag{2.5}$$

The open-loop transfer function of the system is therefore equal to

$$H_o(s) = \frac{qo(s)}{qi(s)} = Kpd \times F(s) \times \frac{Kvco}{s} \tag{2.6}$$

When the loop filter in figure 2-8 is used, Eq. (2.6) becomes

$$H_o(s) = \frac{Kpd \times Kvco}{Cs + Cp} \cdot \frac{1 + s \cdot Rp \cdot Cp}{s^2 \left(1 + s \cdot \frac{Rp \cdot Cs \cdot Cp}{Cs + Cp}\right)} = K \cdot \frac{s + w_z}{s^2 \left(1 + s \cdot \frac{1}{w_p}\right)} \tag{2.7}$$

where $K = Kpd \times Kvco \times Kh$ is the loop bandwidth of the CDR

Figure 2-10 shows the bode plot of the transfer function. We can see the phase of Ho(s) is 180° at ω=0, and the zero ω_z, and the pole ω_p, introduce the phase shift of +90° and -90°, respectively. The phase margin could be described as follows

$$PM = \tan^{-1}(\frac{K}{w_z}) - \tan^{-1}(\frac{K}{w_p}) \tag{2.8}$$

Another way to approximate this parameter is to ignore the shunt capacitor Cs. Since Cp >> Cs, the zero $\omega_z=\frac{1}{RpCp}$, is much smaller than the pole $\omega_p=\frac{Cs+Cp}{RpCsCp}$. Therefore, Eq. (2.7) can be re-written as

$$H_o(s) = \frac{Kpd \times Kvco}{Cp} \cdot \frac{1 + s \cdot Rp \cdot Cp}{s^2} \tag{2.9}$$

where $F(s)=Rp+\frac{1}{sCp}$.

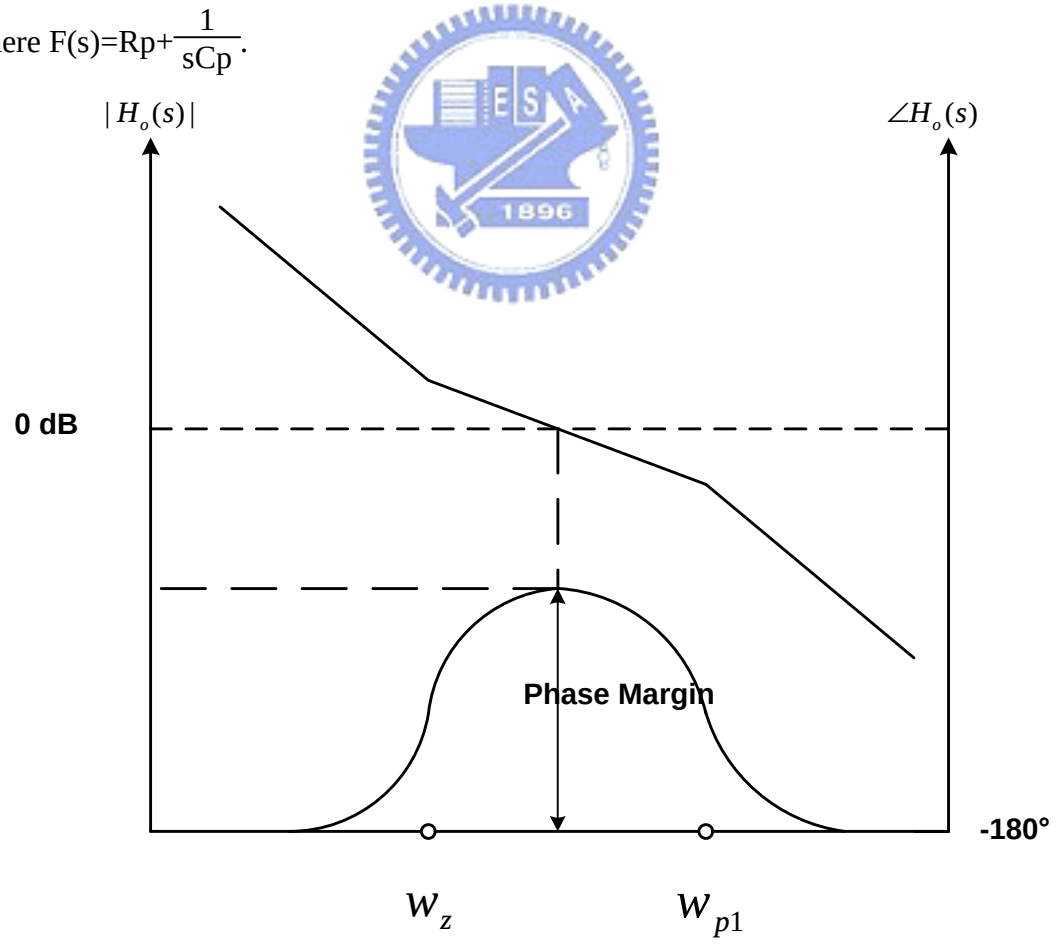


Fig. 2-10 Bode plot of the open-loop transfer function

In the following, we will discuss the stability factor related to the CDR with a bang-bang phase detector [24], [25]. The stability factor determines whether the system is stable or not. We ignore the shunt capacitor Cs to analyze the loop. Figure 2-11 shows the second order bang-bang loop schematic. These are loops labeled "proportional path" and "integral path". The first loop includes the connection of the phase detector to the VCO input through the proportional branch of the loop filter, while the second loop includes the integral branch of the loop filter. The binary control, or "bang-bang" loop, can be considered a phase tracking loop, while the integral branch can be viewed as a frequency tracking loop. It is important the two branched of the loop should be noninteracting. For this to be true, the phase wall-off of the bang-bang branch of the loop, $\Phi_{bb}(t)$, must dominate over the phase walk-off of the integral branch, $\Phi_{int}(t)$. Taking the ratio of $\Phi_{bb}(t)$ and $\Phi_{int}(t)$ at the end of one frame update time gives a figure of merit ξ for the loop stability:

$$\Phi_{bb} = Icp \cdot Rp \cdot Kvco \cdot T_{update} \tag{2.10}$$

$$\Phi_{\text{int}} = \frac{Icp \cdot T_{update}^{2}}{2Cp} \cdot Kvco \tag{2.11}$$

$$x = \frac{2Rp \cdot Cp}{T_{update}} \tag{2.12}$$

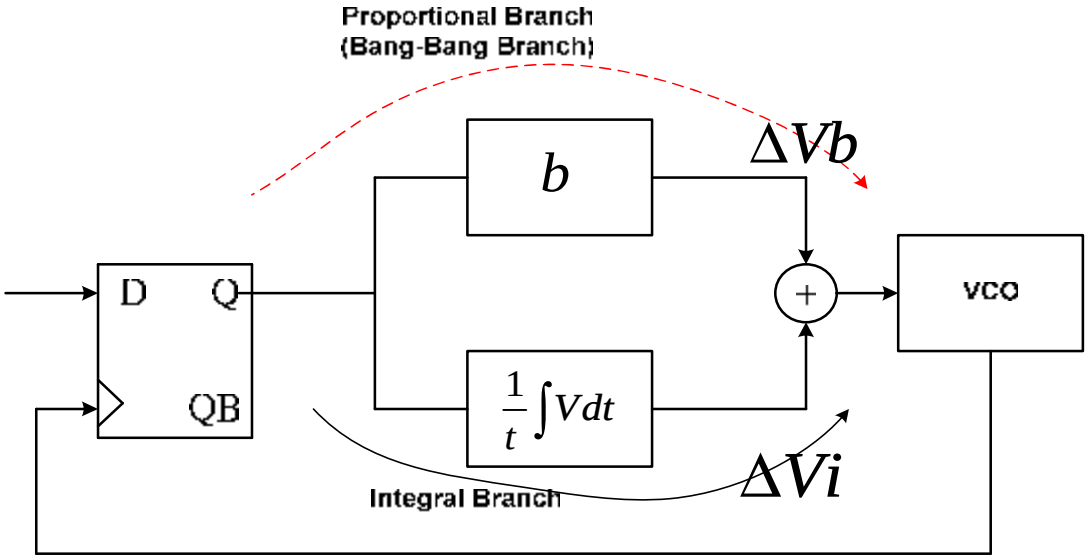


Fig. 2-11 Second-order bang-bang loop schematic

ξ must be greater than one for the two branched to be considered noninteracting. In fact, if ξ becomes significantly less than 1, the "bang-bang" portion of loop will no longer stabilize the system.

2.3.1 Approximated Frequency Response with 1st-order RC lowpass filter

In contrast to the approximated analysis above, the other popular method to analysis a CDR is by the closed-loop transfer function which is written in Eq. (2.13) and the loop filter transfer function is $F(s) = R + \frac{1}{s \cdot Cp}$

$$G(s) = \frac{q_o(s)}{q_i(s)} = \frac{H_o(s)}{1 + H_o(s)} = \frac{Kpd \cdot F(s) \cdot Kvco}{s + Kpd \cdot F(s) \cdot Kvco} \tag{2.13}$$

or, equivalently, by

$$G(s) = \frac{q_o(s)}{q_i(s)} = \frac{H_o(s)}{1 + H_o(s)} = \frac{2 \cdot z \cdot \left(\frac{s}{w_n}\right) + 1}{\left(\frac{s}{w_n}\right)^2 + 2 \cdot z \cdot \left(\frac{s}{w_n}\right) + 1} \tag{2.14}$$

where ζ, define as the damping factor, is given by

$$z = \frac{1}{2}\sqrt{\frac{K}{w_z}} \tag{2.15}$$

and w_n, define as the natural frequency (rad/s), is given by

$$w_n = \sqrt{K \cdot w_z} \tag{2.16}$$

The damping factor and natural frequency characterize the close-loop response. The close-loop frequency response of the CDR for different values of damping factor are normalized to natural frequency as shown in figure 2-12. This figure shows that the CDR is a low-pass filter to the phase noise at frequency below ω_n. For small value of ζ, the curve is shaper than those of large value of ζ. In the CDR design, the loop is designed to be over-damping (ζ>1) to avoid the jitter peaking effect. This also helps increase the phase margin of the open-loop transfer function [26].

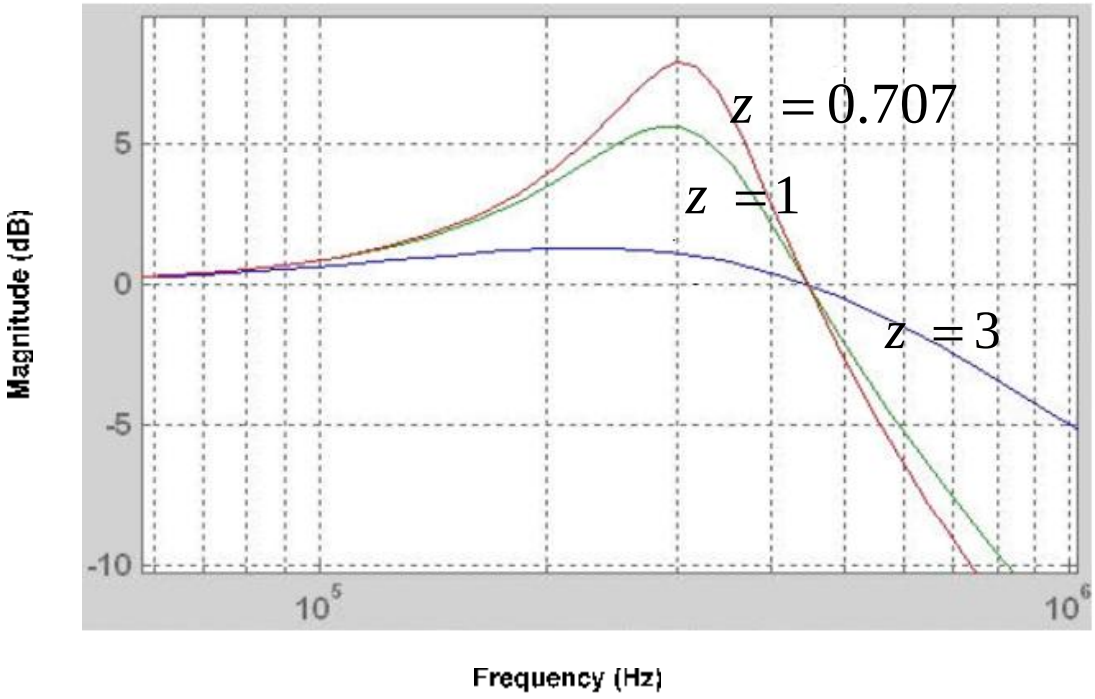


Fig. 2-12 The close-loop frequency response of the CDR

Figure 2-13 shows the transient step response of the CDR for different value of damping factor and for time normalized to $\frac{1}{w_n}$. The step response is generated by instantaneously advancing the phase of the input by one radian and observing the output for different damping levels in the time domain. The CDR output initially responses rapidly but takes a long time to the steady state for the damping factor larger than one; i.e., the system is over-damped. We can find that the rate of the initial

response increase and the rate of the final response decrease. That is a tradeoff in the CDR design.

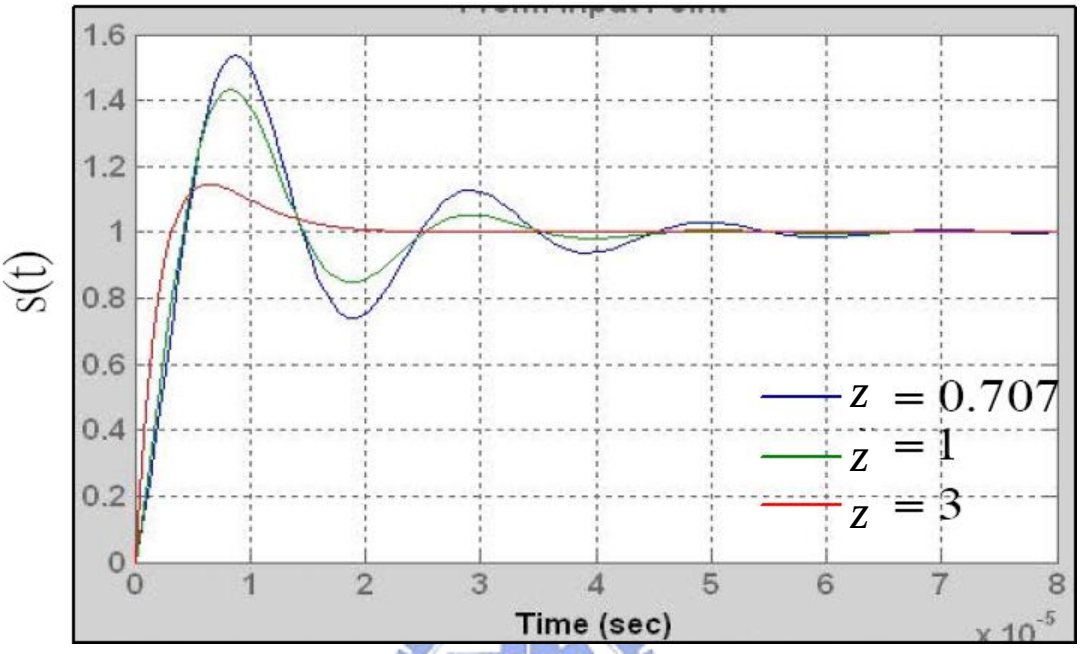


Fig. 2-13 The close-loop transient step response of a CDR

2.4 CDR Parameter Design

Recall our discussion in which loop performance is analyzed. The design of the CDR should be set up the loop parameter for the desirable control dynamics. The value of the loop parameter must be somehow reasonable for the device parameter Kpd, Kvco, Rp, Cp, Cs. In this work, since the capacitor Cp is implemented on-chip, to minimize jitter, its size had better be limited within 100pF. The problem of selecting device parameter is made more difficult by a number of constraining factor. First, loop bandwidth (K) and damping factor (ζ) both depend on all other the parameter. Secondly, the maximum value for Cp leads to the minimum current for charge pump circuits. Furthermore, all worst case of the parameters due to process and temperature variation must lead to acceptable loop performance. A suggested

design flow of the CDR is shown as follow:

(1)Determine Kvco: the gain of the VCO can be found from simulation result, and experimental results or data sheets when a commercial VCO is used. In general, the VCO gain should be too high to avoid the additional jitter introduced by the disturbance on the control line.

(2)Determine Kpd: the gain of the phase detector can be decided according to the current for charge pump circuits [21].

(3)Determine K: the loop bandwidth is then determined depending on the required noise and transient characteristics.

(4)Determine Rp: according to the selected K to determine the Rp.

(5)Determine Cp: the decision for Cp primarily depends on the stability factor, phase margin, and the damping factor (ζ).

(6)Determine Cs: define the maximum possible phase margin. Setting Cp>20×Cs is a general case.