Chapter 4

VLSI Implementation

4.1 Layout

In a high-speed, mixed-mode circuit design, significant attention must be paid to physical layout both to avoid speed degradation and to minimize noise coupling. In addition, testing issues must be considered in conjunction with layout floorplanning and pad placement.

The whole chip layout of the CDR is shown in figure 4.1. It can be seen that a large area is occupied by the on-chip loop filter capacitor. The capacitor is created by a 7×11 array of 77-pF square MOS capacitors. In the middle left areas of figure 4.1, the phase detector and frequency detector can be seen, while the middle right shows the VCO block. The I/O blocks such as input preamplifier and the output buffer are located in the left area of figure 4.1.

Several physical design strategies used to minimize noise coupling and facilitate testing are discussed and listed below:

1. In order to avoid the substrate noise coupling form digital circuit block to sensitive analog circuit block, the ground used by digital circuits is separate from the analog ground.
2. Three sets of supply voltage are adopted. One is for I/O circuits such as the input preamplifier and the output buffer, one is for VCO and another is for digital circuits. The purpose is not only to reduce the noise coupling between each

building block but also to monitor individual current sank easily by each block.

3. The biasing circuit for each main block is also separated. The allocation of biasing circuits is the same as that of supply voltage.

The proposed CDR circuit has been implemented in TSMC 0.35 μm 2P4M CMOS process with a supply voltage of 3.3V. The total area of the chip is 1.8mm×1.8mm. The performance summary of the proposed CDR circuits is given in table 4.1.

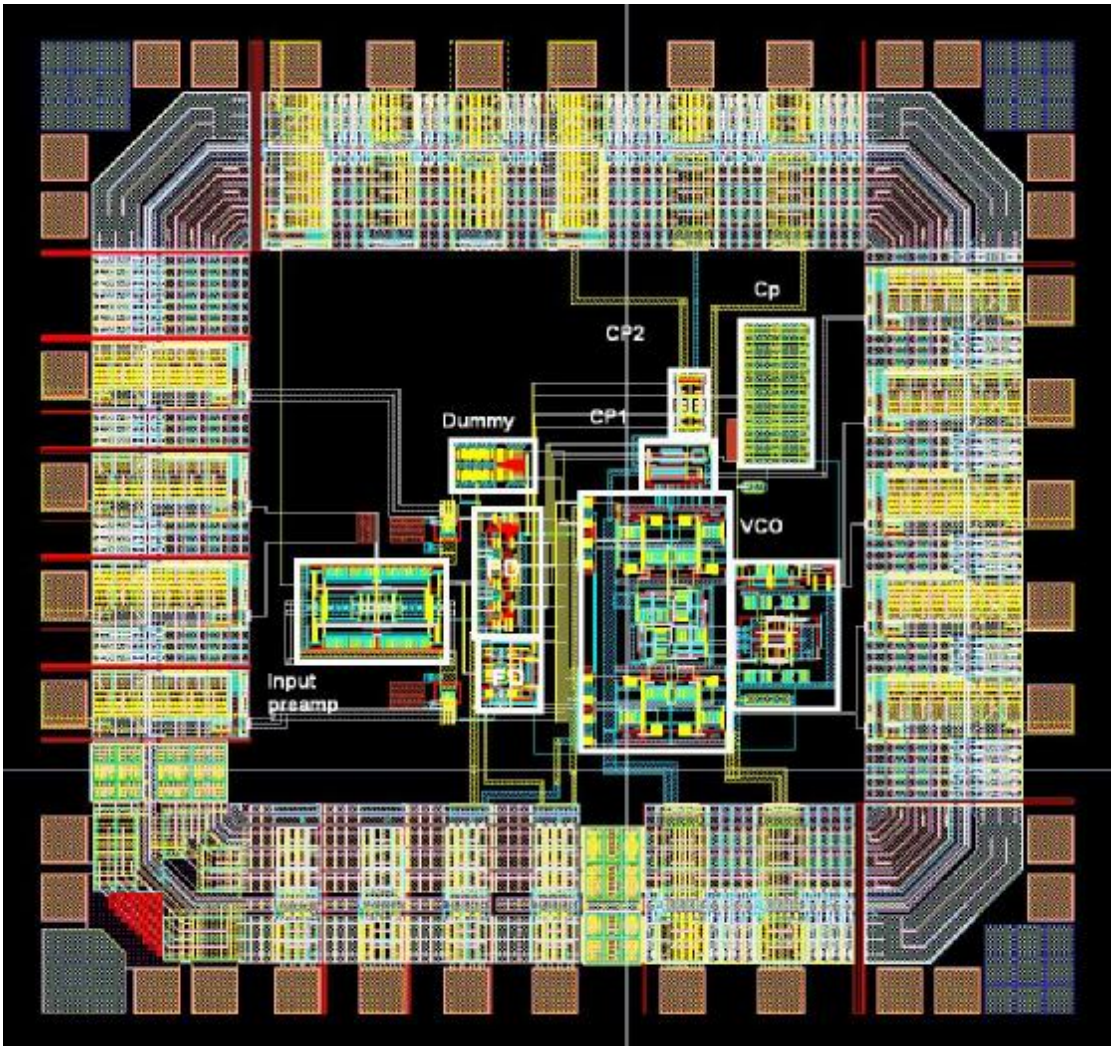

Fig. 4-1 Chip layout of the CDR

Table 4-1 Performance Summary

CDR Spec.	Bit Rate	1.25 Gb/s
	VCO Center Frequency	625 MHz
	Loop Bandwidth	≈ 3MHz
	Acquisition Time	< 3.5 μ s
	Kpd	34 $\frac{uA}{rad}$
	Kvco	65 MHz/V
	Phase Margin	62.4°
	Loop Filter	Cs=2 pf
		Cp=77 pf
		Rp=1.4KΩ
Power Supply	3.3 V	
Power Consumption	≈ 250 mW (two output buffers included)	
Chip Size	1.8mm × 1.8mm	
Technology	TSMC 0.35 μ m 2P4M CMOS	