Chapter 5

Conclusion

A clock and data recovery circuit was successfully presented in this thesis. The CDR incorporates a Dual-loop control mechanism to achieve better jitter performance. These two tracking paths coexist to control the loop behavior and have quite different features to enhance frequency acquisition and reduce the VCO output jitter.

In chapter 2, the approximate second-order model, which imitates the analytical method in linear PLL model, was derived to validate the stability and to facilitate the system parameters design. Furthermore, the appropriate noise sources can also be introduced in the model to see their effect on output jitter. Finally, the proposed half-rate digital quadricorrelator frequency detector significantly increases acquisition range and locking time of CDR system.

In chapter 3, a 1.25 Gb/s CMOS CDR circuit has been fabricated in 0.35 μm standard CMOS process technology. The first important point lies in the input and output interface. In order to recovery the high-speed signals in the Gb/s range reliably, the circuit at the receiving front end must resolve the small-swing input at very high rates, and gives the sampling strobe correctly. Even more important is phase detector, we proposed a half-rate four-stage bang-bang detection method for a phase tracking state. The outputs of phase detector drive a charge-pump and the loop filter. Furthermore, the ring oscillator consists of four stages delay cells for multi-phase clocks.

In chapter 4, there are some discussions on the layout techniques. The common centroid layout structure is used to reduce layout mismatch. Finally, the CDR circuit as presented in this thesis occupies a 1.8mm × 1.8mm chip area in TSMC 0.35 μm 2P4M technology. The total power consumption of this chip is about 250 mW under a 3.3V supply voltage (two output buffers included).