The effect of the geometry aspect ratio on the silicon ellipse-shaped surrounding- gate field-effect transistor and circuit

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Abstract

The silicon (Si) surrounding-gate metal-oxide-semiconductor field-effect transistor (MOSFET) has ultimate gate structures and is a potential candidate for use in next-generation high-performance nano-devices. However, because of limitations of the fabrication process, theoretically ideally round shape of the surrounding gate may not always guarantee. These limitations may lead to the formation of an ellipse-shaped surrounding gate with major (a) and minor (b) axes of different lengths. In this study, the effect of the geometry aspect ratio, a/b, on the dc and ac characteristics of the 16 nm gate ellipse-shaped surrounding-gate MOSFETs and circuits is examined by using a three-dimensional coupled device-circuit simulation technique. The dependences of electrical characteristics on the geometry aspect ratio are evaluated with reference to various device characteristics and the circuit properties, including the circuit gain, the 3 dB bandwidth, the unity-gain bandwidth, the rise/fall time and the delay time. In analog circuits, the device with an aspect ratio of less than 1 is promising because the short-channel effect is suppressed. However, for a digital circuit configuration, the transient response of the circuit relies on the charge/discharge capability of the transistor. Thus, a device with a large aspect ratio, such as 2, will be more suitable for digital applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Silicon-based field-effect transistors (FETs) with vertical channels present fascinating scaling-down properties, unlike conventional bulk metal-oxide-semiconductor FETs (MOSFETs) [1–9]. For example, double-, triple- and surrounding-gate MOSFETs with vertical channels have more attractive electrical and physical characteristics than do single-gate devices [10, 11]. They inherently offer good suppression of short-channel effects (SCEs), have high transconductance (g_m) and exhibit ideal subthreshold swing (S.S.). Among the aforementioned multiple-gate devices, the round-shaped surrounding-gate MOSFET is the structure for use in next-generation high-performance nano-devices as well as in analog and digital circuits [12–18]. As well as offering perfect channel controllability because of the complete 100% gate coverage, the surrounding-gate MOSFET tolerates a thicker silicon fin than with double- and triple-gate devices [19–22]. Unfortunately, limitations of manufacturability prevent some surrounding-gate MOSFETs from exhibiting their theoretically ideal round shape of channel; in contrast, the process obstruction may yield elliptical shaped surrounding-gate MOSFETs with different major and minor axes lengths [23]. The geometry aspect ratio (AR) which is defined by the ratio of the length of the major axis to that of the minor axis of the ellipse-shaped surrounding-gate device affects the electrical characteristics of nano-MOSFETs. However, the effects of the geometry aspect ratio of ellipse-shaped surrounding-gate MOSFETs on the properties of analog and digital circuits have not yet been clearly investigated. Notably, the theoretically ideal round shape of surrounding-gate devices may not exhibit the best circuit performance.

In this study, the effects of the geometry aspect ratio of ellipse-shaped surrounding-gate MOSFETs on analog and digital circuits are examined by performing a three-dimensional (3D) quantum-corrected coupled device-and-circuit simulation technique [24–26] on a parallel computing system [27–29]. The explored 16 nm gate ellipse-shaped surrounding-gate MOSFETs of interest have various geometric aspect ratios, from 0.5 to 2; an aspect ratio of 1 represents the ideally round surrounding-gate transistor. The effects of the geometry aspect ratio of the device on the electrical characteristics of analog and digital circuits are intensively evaluated in terms of the circuit gain, 3 dB bandwidth, unity-gain bandwidth, rise/fall time and delay time. The results of this study demonstrate that in the analog applications, a device with an aspect ratio smaller than 1 has promising characteristics because the short-channel effect is suppressed. However, the transconductance of a device with a smaller aspect ratio is lower because the device is narrower. In the digital circuit design, the significant increase in the length of the interconnect has made the load capacitance seriously affect the device driving capability. Therefore, the lower transconductance of a device with a smaller aspect ratio may reduce the current driving capability and increase the delay of digital circuits. Hence, devices with a larger aspect ratio are more suitable for digital applications than those with a small aspect ratio. This study clarifies the geometric effects of the device channel on the characteristics of surrounding-gate MOSFETs in analog and digital applications. It is useful for developing new fabrication viewpoints for fabricating ultrasmall ellipse-shaped surrounding-gate MOSFETs and applications thereof in circuits.

This paper is organized as follows. Section 2 elucidates the investigated device structures, the circuit topologies and the simulation approach. Section 3 analyzes the effect of geometry on various important electrical characteristics of various circuits. This section discusses and compares different device structures with various aspect ratios. Finally, conclusions are drawn and future work suggested.

2. The device structure and simulation methodology

Figure 1(a) presents the explored device structure. The simulated ellipse-shaped surrounding-gate MOSFETs have major (a) and minor (b) axes of different lengths: the geometric aspect ratio is defined as the ratio of the length of the major axis to that of the minor axis (a/b). The aspect ratio (AR) in this work ranges from 0.5 to 2. To simplify the investigated problem and to clarify the effect of the geometric aspect ratio on the electrical characteristics of the circuit of the ellipse-shaped surrounding-gate MOSFETs, the simulated devices have a gate length of 16 nm, an oxide thickness of 1 nm and a mid-gap material, such as TiN, as the gate material. The minor axis of the ellipse-shaped channel is fixed at 5 nm and the major axis varies with the aspect ratio. The channel and source/drain doping concentrations of the designed device are 2×10^{17} cm^{-3} and 3×10^{20} cm^{-3}, respectively. Notably, to sustain favorable operating characteristics, the ratio of channel

a	2.5	3.75	5	6.25	7.5	8.75	10
b	5	5	5	5	5	5	5
Geometry Aspect Ratio (AR = a/b)	0.5	0.75	1.0	1.25	1.5	1.75	2.0
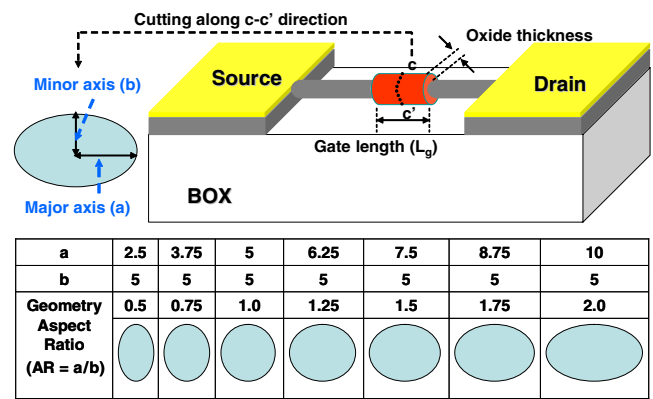
(a)
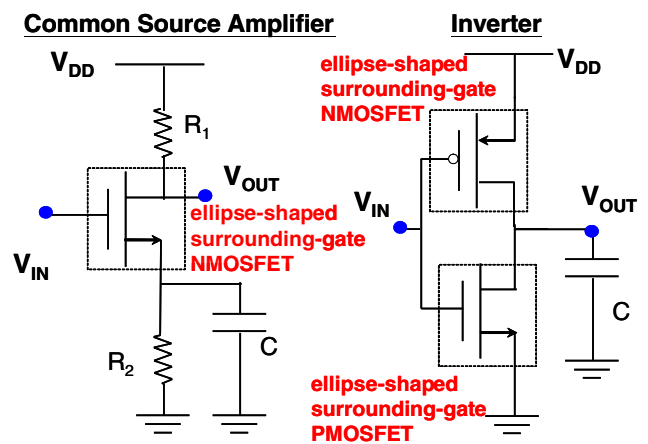
(b)

Figure 1. (a) The studied ellipse-shaped surrounding-gate MOSFETs with the major and minor axes. The geometry aspect ratio varies from 0.5 to 2. (b) The studied circuit topologies for analog and digital application. The circuit characteristics are obtained from the coupled device-circuit simulation.

length (L_g) to the thickness (T_{si}) of the surrounding-gate device should exceed 1 [19, 21]. In this investigation, the ratio of the channel length to the thickness is fixed at 1.6, satisfying the design criteria for silicon surrounding-gate transistors.

The dc characteristics of the investigated surrounding-gate devices are simulated by solving, on our established parallel computing system [27–29], a set of 3D quantum-mechanically-corrected transport equations, which are the electron–hole current continuity equations, the Poisson equation and the density-gradient equation [30–32]. Notably, in the simulation of nanodevices, a model based on full quantum mechanical physics [33, 34] will definitely provide a better estimate than quantum-mechanically-corrected transport equations, but at a cost of the need for the computer-aided device design and simulation. Therefore, an experimentally calibrated density-gradient model [30–32] based on a first-order quantum approximation has been validated for the efficient modeling of quantum mechanical effects in the simulation of nano-devices. This simulation quantitatively can predict the electrical and physical properties of the examined transistors accurately and thus the simulation

herein will not be significantly altered. The developed simulation prototype has been carefully calibrated and validated in various semiconductor scenarios, with reference to the effect of grain boundaries on surrounding-gate polysilicon thin film transistors [24], the effect of discrete impurities on nano-MOSFETs [10, 11, 26, 35–39] and surrounding-gate transistor simulation [18–21, 23, 36]. Our recent work has also studied the effects of randomness and geometry variation on surrounding-gate transistors. The employed physical model of a simulated silicon surrounding-gate device has been calibrated using the measured results of surrounding-gate MOSFETs [21] to maximize the accuracy.

Figure 1(b) presents the tested circuits, a common source amplifier and an inverter for studying analog and digital circuits using the explored ellipse-shaped surrounding-gate transistors. The input offset voltage of the common-source amplifier is 0.5 V; the frequency is swept from 1×10^8 Hz to 1×10^{14} Hz. Since no device-equivalent circuit model has been properly established for such ultrasmall nano-devices, the aforementioned device equations are directly coupled with the circuit voltage and current conservation equations, and simultaneously solved to evaluate the circuit performance [24–26]. The coupled device-and-circuit simulation scheme directly incorporates the quantum mechanical effect into the simulation of ellipse-shaped surrounding-gate MOSFETs circuits.

3. Results and discussion

This section discusses the dc characteristics of ellipse-shaped transistors. The simulation results will be used in an analysis of variations in the characteristics of the circuit level. The coupled device-and-circuit simulation is adopted to calculate the characteristic responses of the circuits of interest in both the frequency and the time domains.

3.1. Device characteristics

Figures 2(a) and (b) plot the electrical characteristics of the simulated surrounding-gate MOSFETs with ellipse-shaped channels. The calculated threshold voltage (V_{th}) and the on/off current ratio increase as the aspect ratio (AR) declines. Additionally, these characteristics indicate that a device with a lower aspect ratio may have greater channel controllability. A smaller aspect ratio device may suffer from less short-channel effects, including drain induced barrier lowering (DIBL) and subthreshold swing (S.S.). The insets in figure 2(b) define DIBL and S.S., and the threshold voltage is determined from the current criterion that drain current $\geqslant 10^{-7}$ (W/L) A. The decrease in the aspect ratio of the device seems to improve dc characteristics; however, because of an increase in the threshold voltage and a decrease in the channel width, a device with a smaller aspect ratio may have a lower transconductance (g_m). To evaluate the impact of the variations of these dc characteristics on analog and digital circuits, the device transport equations are coupled with the circuit conservation equations and solved self-consistently to evaluate circuit performance [24–26].
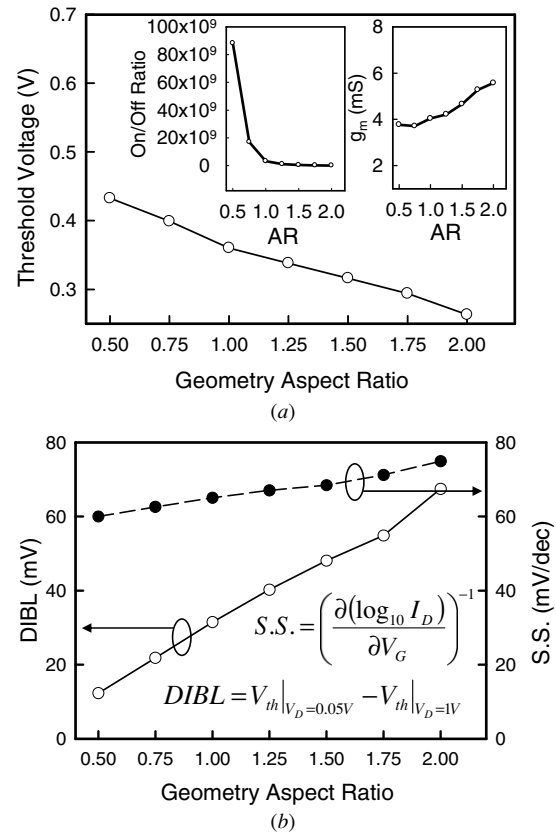

Figure 2. The (a) threshold voltage and (b) short-channel effects (DIBL and S.S.) for the studied device with respect to different geometry aspect ratio.

3.2. Analog circuit performance

Figure 3(a) plots the voltage-transfer characteristics of the studied common-source amplifier; the inset presents the operation point, V_{IL}. Since a device with a smaller aspect ratio has a higher threshold voltage, V_{IL} is increased, as plotted in figure 3(b). The input offset voltage, V_{IN}, of the common-source amplifier is 0.5 V. The margin $V_{IN}-V_{IL}$ is lower, limiting the voltage gain of the amplifier. Figure 4(a) plots the slopes of the voltage-transfer curves. The device with AR = 0.5 has the highest voltage gain, as presented in figure 4(b); however, the corresponding optimal input voltage to obtain maximum voltage gain is near 0.6 V. For the given 0.5 V input voltage, the voltage gains of circuits are as plotted in figure 4(b); the device with AR = 1 yields the highest voltage gain of the circuit. The results reveal that a device with an aspect ratio of 1 may have the highest voltage gain; however, the decline in the voltage gain as the aspect ratio of the device decreases is caused mainly by the change of the threshold voltage. The characteristics of the device with a fixed threshold voltage will be discussed later. The 16 nm gate common-source amplifier circuit in the high-frequency regime is then quantitatively studied to determine its high-frequency circuit gain, 3 dB bandwidth and unity-gain bandwidth. Figure 5 presents the output resistance (r_0) and gate capacitance (C_g) of the studied ellipse-shaped surrounding-gate transistors, which are strongly correlated with the high-frequency characteristics. As the aspect ratio of the device decreases, its output resistance
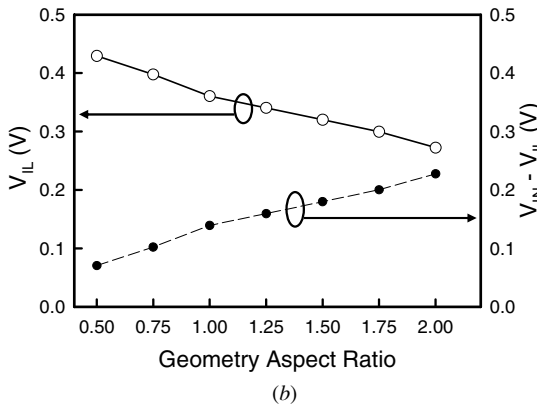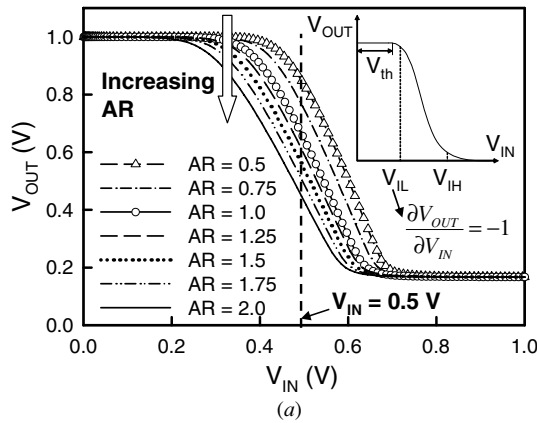
Figure 3. (*a*) The voltage transfer curve, for the studied devices with different geometry aspect ratios. The inset shows the definition of V_{IL}. (*b*) The dependence of V_{IL} and $V_{IN} - V_{IL}$ on the device's geometry aspect ratio.

Figure 4. (*a*) The slope of the voltage transfer curve for the studied device with different geometry aspect ratios. (*b*) The maximum voltage gain and voltage gain at 0.5 V input voltage for the studied ellipse-shaped surrounding-gate MOSFETs' circuit.

is increased and the gate capacitance is decreased. A change of the threshold voltage of the transistors alters the operating conditions of the circuit, such as the nodal voltages at the source and drain sides of the transistors. Hence, the output resistance and the gate capacitance of the transistors are obtained from the nodal voltage of the tested circuit to determine the corresponding characteristics of the devices in the circuit.

The high-frequency responses of the studied circuits are investigated in figure 6(*a*), by extracting the high-frequency circuit gain, the 3dB bandwidth and the unity-gain bandwidth. As displayed in the inset of figure 6(*b*), the high-frequency circuit varies in a manner similar to the dc voltage gain of the circuit. Figure 6(*b*) plots the 3 dB bandwidth of the studied circuits. According to the inset in figure 6(*b*), the 3 dB bandwidth is proportional to the reciprocal of both the output resistance of the circuit and the capacitance of the transistor. The intrinsic resistance of the transistor is of the order of 10^6 Ω, which is significantly larger than the load resistance, R_1 (5 kΩ), between V_{DD} and V_{OUT}, as presented in figure 1(*b*). Thus, the output resistance of the circuit is dominated by the load resistance, and the circuit output resistances of the ellipse-shaped MOSFET circuits are similar. Accordingly, the 3 dB bandwidth is dominated by the change in the gate capacitance. Since the gate capacitance decreases as the aspect ratio increases, the 3 dB bandwidth increases as the aspect ratio increases. Figure 6(*c*) plots
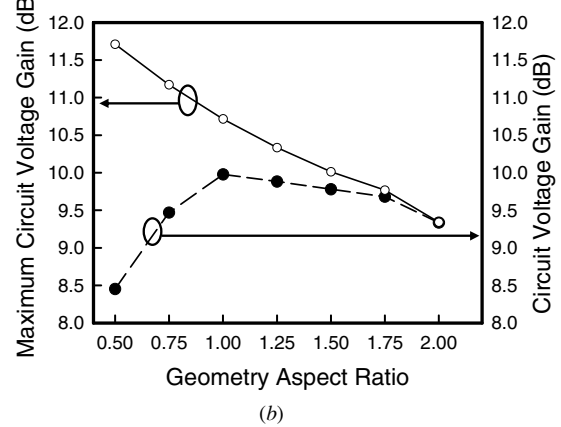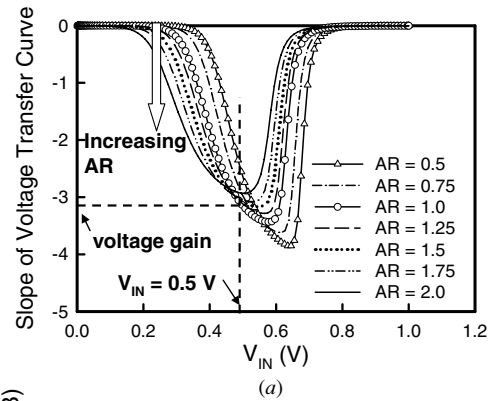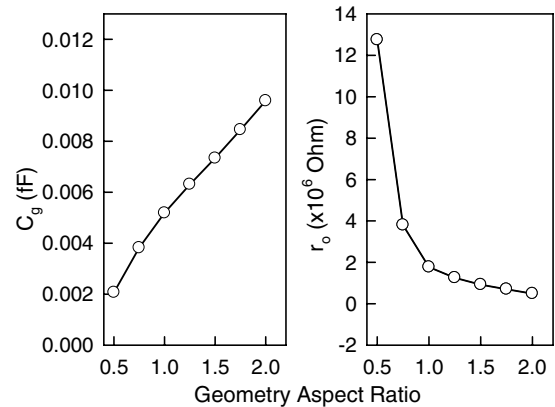

Figure 5. The gate capacitance (C_g) and output resistance (r_0) of the studied ellipse-shaped surrounding-gate MOSFETs' circuit with different geometry aspect ratios.

the unity-gain bandwidth of the studied devices. The unity-gain bandwidth is proportional to the transconductance and inversely proportional to the gate capacitance. Although both these characteristics affect the unity-gain bandwidth, the variation of the gate capacitance is three times larger than the variation of the transconductance. The unity-gain bandwidth is therefore dominated by the gate capacitance, and increases as the aspect ratio decreases.

To compare various surrounding-gate devices with different aspect ratios on the same basis, the threshold voltage
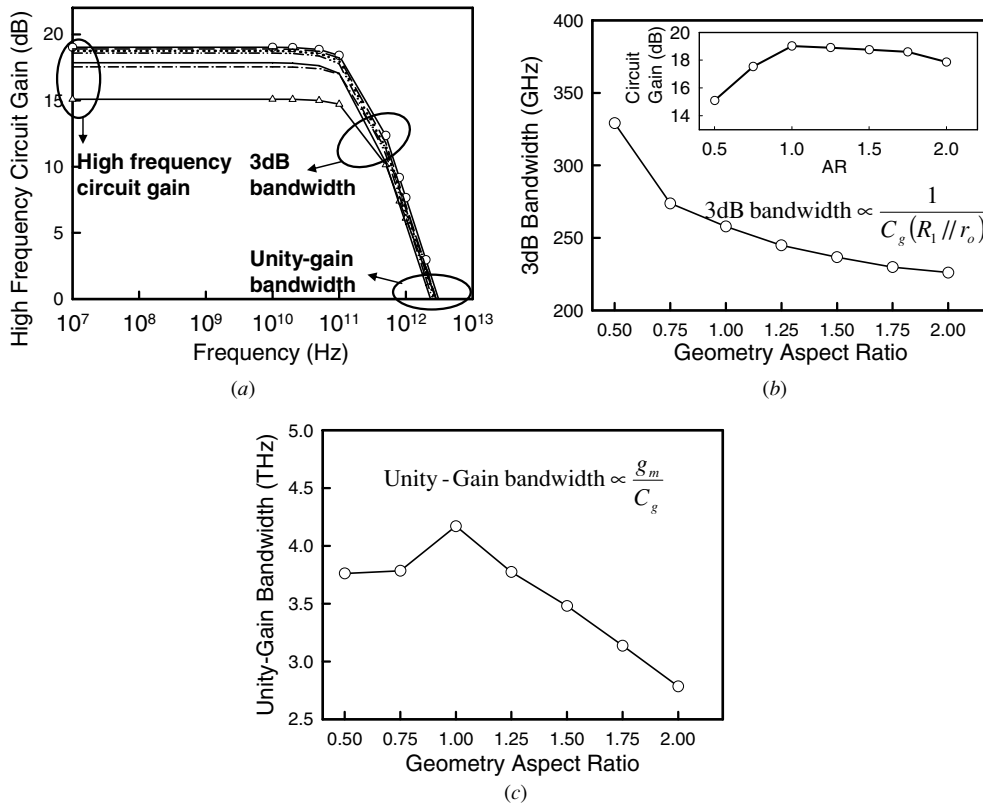
Figure 6. The high-frequency responds and the corresponding high-frequency characteristics circuit gain (*a*), 3 dB bandwidth (*b*) and unity-gain bandwidth (*c*) of the studied ellipse-shaped surrounding-gate MOSFETs' circuit are explored.
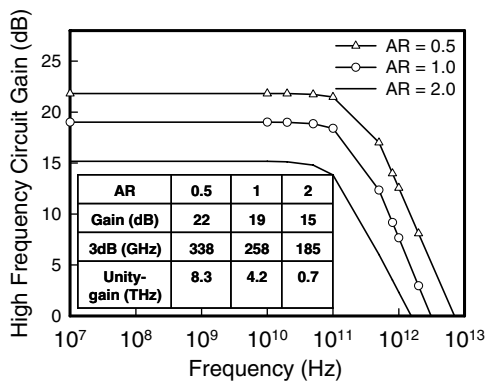

Figure 7. The high-frequency response of the studied ellipse-shaped surrounding-gate MOSFETs' circuit with different geometry aspect ratios, where the threshold voltage of device is calibrated to 360 mV.

of the devices with aspect ratios of 0.5, 1 and 2 are calibrated to 360 mV. Figure 7 plots the high-frequency responses of the calibrated devices; the inset plots the estimated high-frequency circuit gain, the 3 dB bandwidth and the unity-gain bandwidth. The results show that a device with a smaller aspect ratio has significantly better high-frequency characteristics. The high-frequency circuit gain, the 3 dB bandwidth and the unity-gain bandwidth of AR = 0.5 are 2.65, 4.52 and 21.4 times larger than those of the devices with AR = 2. An ellipse-shaped surrounding-gate device with a smaller aspect ratio has better dc characteristics, and is preferred in analog circuit applications.

3.3. Digital circuit performance

The inverter acts as a primary logic gate in a digital system; therefore, without loss of generality, it is used as the test circuit to evaluate the effect of the aspect ratio on timing characteristics. We believe that the simulation results can be applied to other logic gates, such as NAND, NOR and others. The loading capacitance of the inverter is 10 fF, which is 1000 times larger than the capacitance of a transistor. To simplify the problem of interest and clarify the effect of the aspect ratio on the timing of the studied surrounding-gate MOSFET circuit, the aspect ratio of the simulated 16 nm gate PMOS surrounding-gate MOSFETs is initially fixed at 1.

Figure 8(*a*) plots the calculated transient input and output characteristics of the studied inverter circuit. Figures 8(*b*) and (*c*) show the signal transitions of the output signal; the insets present the operation of the circuit during the fall and rise of the output signal, respectively. As displayed in figure 8(*b*), when the input signal transits from logic state '0' to '1', the NMOS is turned on and the load capacitance of the circuit begins to be discharged. Therefore, an NMOS transistor with a higher transconductance has a shorter transient characteristic. In the rise transition of the output signal, the input signal transits from logical '1' to '0', the NMOS is off, and the PMOS begins to charge the load capacitance. Since the load capacitance is 1000 times larger than the capacitance of the transistors, the influence of the variation in the gate capacitance of the device is negligibly small enough to be neglected. The rise transition characteristic
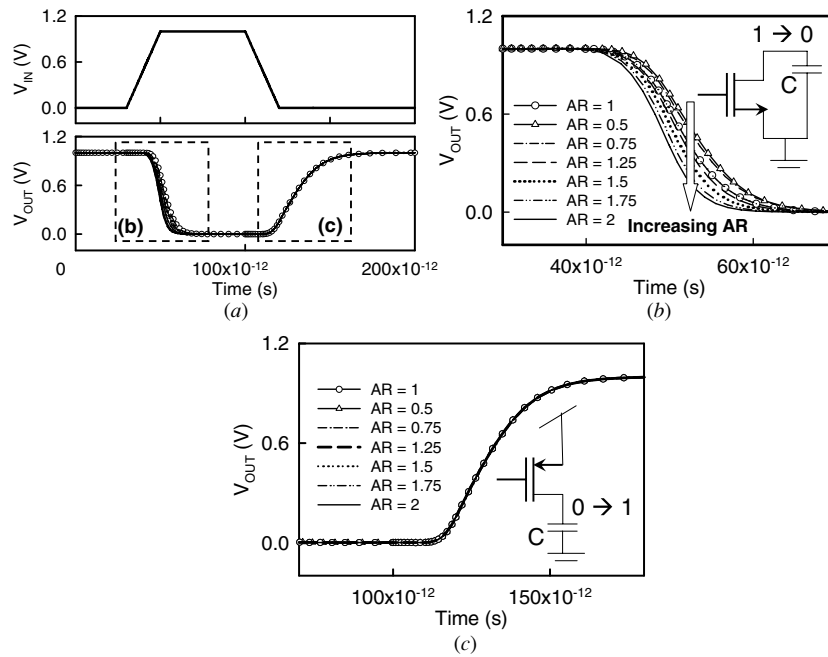
Figure 8. (*a*) The input and output signals for the studied ellipse-shaped surrounding-gate MOSFETs' inverter circuits. Zoom-in plots of the fall and rise transitions are further explored in (*b*) and (*c*).
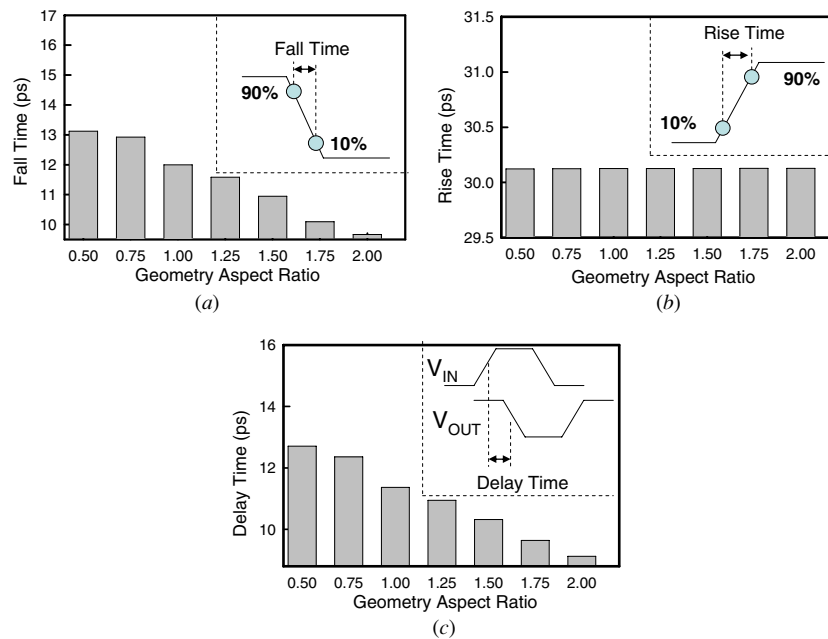

Figure 9. The (*a*) fall time, (*b*) rise time and (*c*) delay time of the studied ellipse-shaped surrounding-gate MOSFETs' inverter circuits.

of the explored inverter circuits is similar because the aspect ratio of the simulated 16 nm gate PMOS surrounding-gate MOSFETs is fixed, as displayed in figure 8(*c*). The fall time, the rise time and the delay time of the transient characteristics are further estimated, and plotted in figures 9(*a*)–(*c*). The fall time is the time required for the output voltage to vary from 90% of the logical '1' level to 10% of the logical '1' level, while the rise time is the time required for the output voltage to vary from 10% of the logical '1' level to 90% of the logical '1' level, as presented in insets of figures 9(*a*) and (*b*). A device with a higher aspect ratio exhibits a faster falling

transition. However, the aspect ratio does not affect the rise time transition. Both the fall time and the delay time of a device with AR = 0.5 are approximately 1.4 times longer than those of a device with AR = 2. To compare surrounding-gate devices with various aspect ratios on a fair basis, the threshold voltage of the device is calibrated to 360 mV to evaluate the timing characteristics, as presented in figure 10. Even though the difference between the transconductance of the device with AR = 0.5 and that of the device with AR = 2 is reduced by the adjustment in the threshold voltage, the device with AR = 2 still has more promising timing characteristics than that
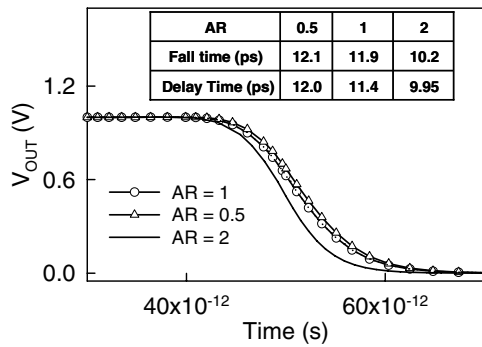
AR	0.5	1	2
Fall time (ps)	12.1	11.9	10.2
Delay Time (ps)	12.0	11.4	9.95

Figure 10. The timing characteristics of the studied ellipse-shaped surrounding-gate MOSFETs' circuit with different geometry aspect ratios, where the threshold voltage of device is calibrated to 360 mV.

with AR = 0.5. The device with the larger aspect ratio may be suitable for digital applications because it has the larger transconductance and driving current.

4. Conclusions

This work studied the effects of the aspect ratio on the ellipse-shaped surrounding-gate transistor on analog and digital applications, using 3D coupled device-and-circuit simulations. The adopted physical model of the device was calibrated with the measurements of fabricated surrounding-gate MOSFETs to maximize accuracy. A theoretical investigation indicated that a device with a low aspect ratio exhibits good channel controllability and is suitable for analog applications. However, the transistor that is preferred for analog applications may not be suitable for digital applications. A device with a smaller aspect ratio may have a smaller transconductance. A small transconductance limits the driving ability of the inverter. Therefore, a device with a larger aspect ratio is preferred for short signal propagation. The results of this work are useful in the fabrication of surrounding-gate MOSFETs in various circuit applications. We are now working on the experimental design of simulated surrounding-gate FET circuits and studying the intrinsic characteristic fluctuations in surrounding-gate transistor circuits.

Acknowledgments

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