國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

1.2Gbps 更小擺幅差動訊號傳輸模式收發器
A 1.2Gbps RSDS Serial-link transceiver

研 究 生　：　邱啟祐

指導教授　：　吳錦川　教授

中華民國九十四年八月


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碩士論文

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摘要

由於積體電路製程上技術的進展,在晶片間的資料傳輸所要求的速度與傳輸資料量也因應的提升,但如何在達到高速傳輸的目的下卻不造成空間與功率的浪費，而在現今以高速序列傳輸方式為主流中，具有高速、低功率、低雜訊干擾特性的(RSDS)更小擺幅差動訊號傳輸方式的技術是頗受歡迎的。

本篇論文在研究 RSDS 傳輸模式下以 1.2Gbps 的傳輸速度運作的收發器架構，當中分為傳輸與接收兩個部份，並以 tsmc 0.352P4M CMOS 的製程技術在電壓電源為 3.3V 的情況下進行模擬。

傳輸器利用一個鎖相迴路來提供時脈和多工器將資料由並列轉為序列輸出。鎖相迴路的輸入頻率為 75MHz，輸出頻率鎖在 150MHz 並提供八個相位的時脈給多工器使用，並在時脈與資料間先進行預先位準調整，再經由八對一多工器輸出可得 1.2Gbs 的資料頻率輸出，該接收器的消耗功率為 134mW。

接收器使用一具磁滯現象比較器將接收訊號放大為數位訊號。再利用一操作在輸入資料一半頻率、且具有頻率、相位雙向追蹤的時脈資料回復電路來將資料與時脈對準，最後由一對八解多工器將資料轉回並列。該接收器的功率消耗為 164mW。

A 1.2Gbps RSDS Serial-link transceiver

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Abstract

Due to the improvement of IC fabrication technology, the speed and amount of inter-chip data transmission has also been required more. The problem is how to make high speed transmission without wasting space and power. Among the main stream, high speed serial ports, RSDS technology with high speed, low power and low EMI character is popular now.

This thesis describes the design of a high-speed RSDS transmission interface with 1.2Gbps rate. The transceiver includes transmitter and receiver and is simulated in a TSMC 0.35μm 2P4M process and at 3.3V supply voltage.

The transmitter makes use of a PLL to provide the 8-phase, 150MHz clock for the multiplexer and translate the parallel data to be serial and the input frequency of PLL is 75MHz.The data and clock is pre-skewed to adjust the accuracy .Then with the 8-phase clock and 8 to 1 multiplexer, the output data can be transmitted at 1.2Gbps data rate. And the total power of the transmitter is 134mW.

The receiver uses the comparator with hysteresis to amplify the incoming data to full swing, and uses (CDR) clock and data recovery with phase and frequency

detectors to lock the clock with better jitter performance. Finally, the 1 to 8 de-multiplexer converts the CDR output to 8 parallel data channels. The total power of receiver is 164mW.

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謹以此篇論文獻給所有關心我的人與我所關心的朋友。

邱啟祐

國立交通大學

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Introduction

1.1 Motivation

Recently, the advances of IC fabrication technology have led to an great growth of the integration levels of digital IC's. For perfect performance, all high-speed components of a system should be integrated into a signal die. However, some technological obstacles forbid the implementation of System-On-a-Chip (SOC). Therefore, high speed links will be the key of the connection between different modules and chips. While improving the I/O speed, we also need to keep the circuit are a small and power consumption low so that we can make sure that integrating transmitter, receiver, and protocol control into a single chip will have the good performance[1].

The basic data link consists of the components such as transmitter, receiver, and channel. The transmitter translates the incoming digital data to analog level and converts the data into a serial data stream on the channel to receiver. A high-level and a low-level are the logical value in the analog system as 0 and 1 are the logical value to the digital system. In order to detect the logic level of analog waveform from the channel, the analog waveform needs to be amplified in the front of receiver. The timing recovery circuit is additional part in receiver to resolve the input into the needed clock. Finally, the receiver converts the serial data to the parallel data.

In this thesis, the achievement is to design a CMOS serial link transceiver based on the RSDS interface and meet the specification for delay, cost, data mapping, power consumption and logic threshold variation. RSDS means Reduced Swing Differential Signaling. It's a way to transmit data with very low differential swing (200mv) over two printed circuit board (PCB) traces or a balance cable. The following section will show RSDS in more detail.

1.2 Introduction of RSDS

1.2.1 RSDS/LVDS

Reduced Swing Differential Signaling, like it's predecessor LVDS (Low Voltage Differential Signal), originated from the LCD Manufacture's unique need for on glass interface with high speed, reduced interconnection, lower power, and a lower EMI.

The following figure indicates the difference between RSDS/LVDS

Characteristic	RSDS	LVDS
V_{OD}, output voltage swing	+/- 200mV	+/- 350mV
R_{TERM}, Termination	100Ω	100Ω
I_{OD}, output drive current	2mA	3.5mA
Data MUX	2:1	7:1
Content	RGB Data	RGB Data and control
Application	Intra-system interface	System-system interface

Table 1-1 RSDS/LVDS comparison [2]

1.2.2 Applications RSDS/LVDS

Because of the benefits of the RSDS and LVDS low signal swing, the RSDS and LVDS are widely used standards of flat panel interfaces. The chart below shows some applications based on RSDS/LVDS interface.

PC/Computing	Telecom/Datacom	Consumer
Flat panel displays	Switches	Home/office
Monitor link	Add/drop multiplexers	Set op boxes
Printer engine link	Box-to-Box	
System clustering	Routers	Game displays/controls
SCI processor interconnect	Hubs	In-flight entertainment

Table 1-2 RSDS/LVDS applications

1.2.3 The Trend of RSDS

The tendency of the TFT industry toward higher resolution displays requires a new low noise digital interface. The open RSDS technology offers us an industry leading technology platform. Combining the TFT display-related technology with a low power consumption, low noise interface like RSDS will accelerate developing new TFT driver families to achieve next-generation, high-performance TFT LCD modules.

Fig 1-1 illustrates a typical application block diagram of the LCD module. The RSDS bus is located between the Panel timing Controller (TCON) and the Colum Drivers. This bus is typical nine pair wide plus clock and is a multidrop bus configuration.

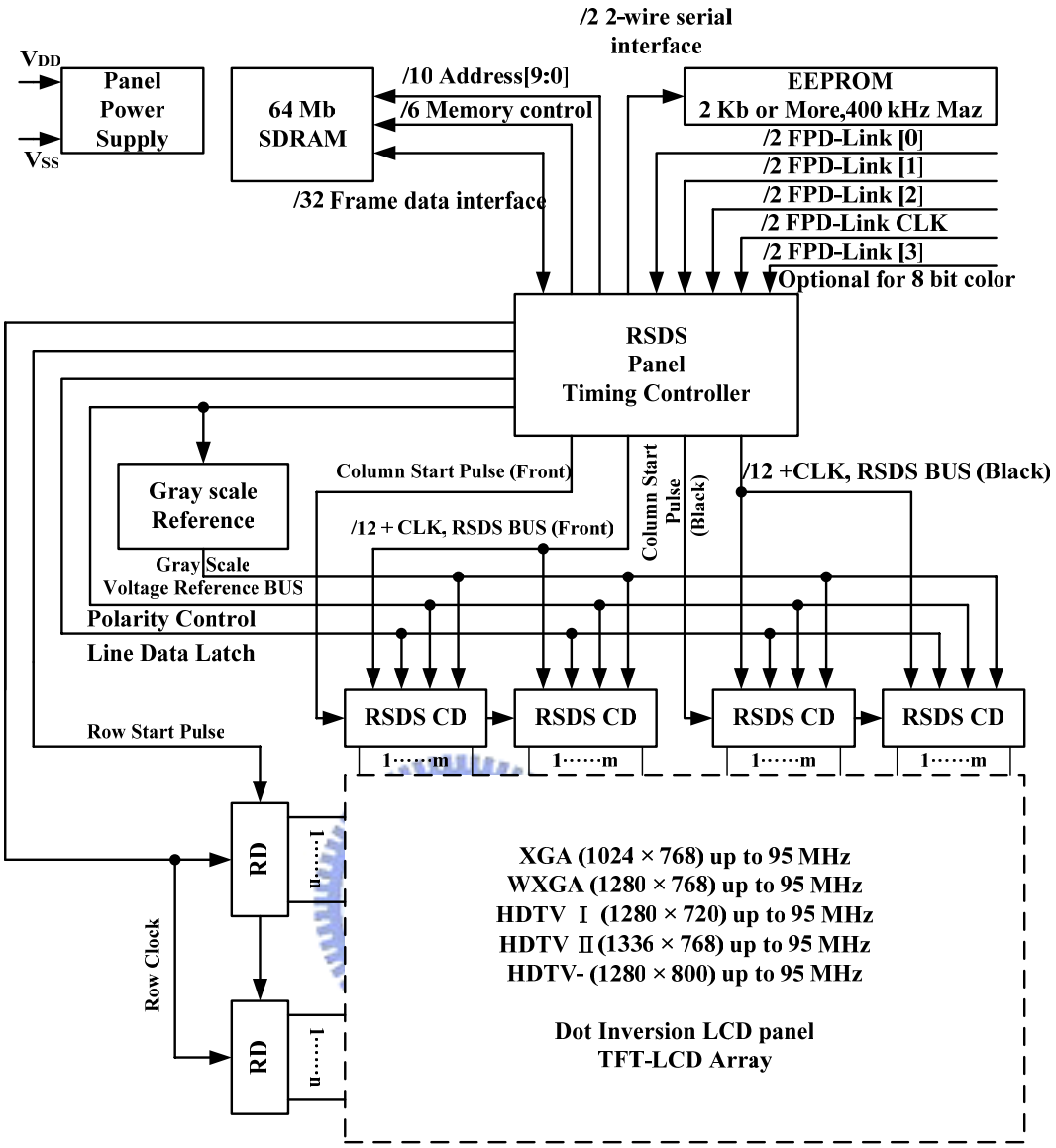


Figure 1-1 Block diagram of the LCD nodule [3]

1.2.4 The Benefits of RSDS

With RSDS technology, designers are able to reduce the size of circuit boards and the bus interconnect, and eliminate discrete components typically used in TFT LCD modules. The XGA (eXtended Graphics Adapter) panel timing controller combined with a partner's RSDS-enabled XGA column driver form a powerful solution to reduce size, weight and cost.

The use of RSDS Technology also enables several other key features and benefits in these new display designs. Substantial power savings, critical in battery-operated and mobile applications can be realized without sacrificing performance and resolution. Significantly reduced EMI-radiated (electro-magnetic interference) noise can be achieved, lowering production costs by eliminating EMI shielding.[3]

1.3 Thesis Organization

This thesis is organized into six chapters and the first one is the introduction of the RSDS interface. Chapter 2 introduces more specification and background of RSDS interface transmission and shows the basic design of serial link. In Chapter3, the conception and architecture of Phase-Locked Loop (PLL) will be described. Chapter 4 shows the discussion of the transmitter architecture. High speed parallel to serial data conversion is achieved by means of time-division multiplexer toggled by a low jitter and 8-phases phase-locked loop. The transmitter simulation result is shown in the end. Chapter5 presents the building block of receiver. The clock and data recovery circuit will be introduced and the architecture with improved jitter performance is proposed. The frequency acquisition part design is also introduced .The whole simulation performance (including transmitter, cable and receiver) will be shown in the end of this Chapter. Chapter 6 is the conclusion of this thesis and shows the future work.

Chapter 2

Background

Chapter 2 describes the detail of RSDS specification, some terminologies and conceptions for transmission environment, some basic design architectures and some opinions for performance enhancement.

2.1 RSDS Specification [5]

Reduced Swing Differential Signaling (RSDS) is a signaling standard that defines the output characteristics of a transmitter and inputs of a receiver along with the protocol for a chip-to-chip interface between Flat Panel timing Controllers and Column Drivers. RSDS which is a differential interface with a nominal signal swing tend to be used in display applications. It retains the many benefits of the LVDS interface commonly used between host and the panel for high bandwidth, robust digital interface. The RSDS provides many benefits to the applications which include:

- Reduced bus width – enables smaller thinner column driver boards
- Low power dissipation – extends system run time
- Low EMI generation – eliminates EMI suppression components and shielding
- High noise rejection – maintains signal image
- High throughput – enables high resolution displays

The **Fig 2-1** below show the RSDS transmitter output swing level in single end and differential end. The RSDS has the waveform with low signal swing of 200mV. And the **Table 2-1** below presents the electrical specification for a transmitter (TX) and receiver (RX).

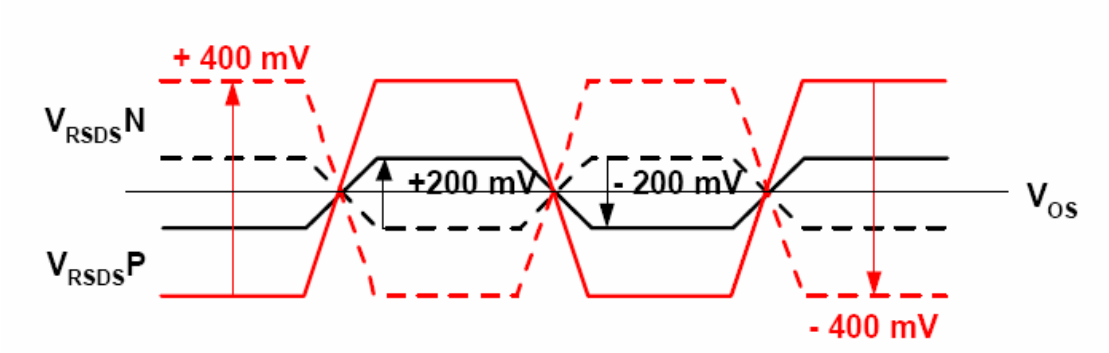


Figure 2-1 RSDS swing level

Tx/Rx	Parameter	Definition	Condition	MIN	TYP	MAX	Units
Tx	V_{OD}	Differential output voltage	R_L=100Ω	100	200	600	|mv|
Tx	V_{OS}	Offset voltage	--	0.5	1.2	1.5	V
Tx	I_{RSDS}	RSDS driver current	--	1	2	6	ma
Tx	T_R/T_F	Transition	20%to80%, V_{OD}=200mV C_L=5pf	--	500	--	ps
Tx	--	RSDS clock duty cycle	--	45	50	55	%
Rx	V_{TH}	Differential threshold	--			+/-100	mV
Rx	V_{CM}	Input common mode voltage	--	0.3		1.5	V
Rx	I_L	RSDS Rx input leakage	--	-10		10	μA

Table 2-1 Electrical specification of RSDS transmitters and receiver

2.2 Basic Serial Link

As shown in the below **Fig 2-2**, the common components of the basic serial link are transmitter, channel and receiver. In order to increase the bandwidth of the link, the data are usually parallel before being sent by the transmitter. The transmitter converts the digital information to analog level on the transmission medium. The driver makes the analog signal be differential. The medium on which the signal travels, e.g. coaxial cable or twisted pair, are commonly called the communication channel. The receiver in the end of channel recovers the incoming signal to the original digital information by amplifying and sampling the signal. The termination resistor which matches the impedance of the channel could minimize the signal reflection. The circuit at receiver, the clock and data recovery adjusts the receiver clock based on the received data to let the sampling point fix the center of the data eye. Finally, the serial to parallel interface converts the serial data back to N parallel bits data.

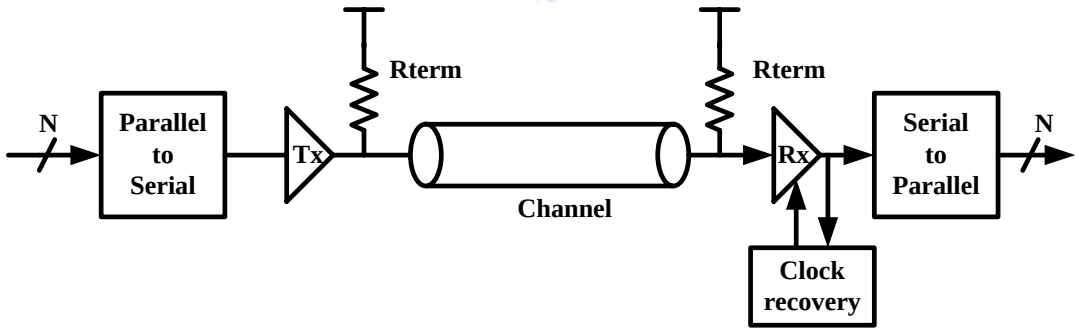


Figure 2-2 Block diagram of the basic serial link

The performance of a link is mainly characterized by the data bandwidth. The another important parameter of link performance is the bit error rate (BER) , a measure of how many bit errors are made per second. A link's maximum data rate is specified at the specific BER to guarantee the robustness of the overall system. BER

is important not only because it reduces the effectiveness of a system's bandwidth, but also because in many systems, applications of error correction techniques can prohibitively increase the system cost. The errors are caused by the noise from each part of the system. The intrinsic sources of noise are the random fluctuation due to the thermal vibration and shot noise of the positive and active system components. In VLSI applications, other non-fundamental sources of noise also limit the performance of link. The noise sources include coupling effect from other channel, the mutual inductance, switching activity from other circuits integrated with the link circuit, and the reflections induced from the link imperfections. These types of noise typically have non-white frequency spectrum, and exhibit with the strong data correction. Moreover, the overall power is often proportional to the power of the signals. Therefore, there are two main issues in designing high-speed serial link interface circuit: signaling and clock.[6]

2.3 Noise Issue

When selecting a particular signaling or a clocking scheme, the primary goal is to transmit data between system components with the maximum bandwidth, while keeping the low associated cost low. These costs include the power consumption and the area occupied by the signaling and synchronization circuits, as well as the cost of the required external component. Unfortunately, the noises in the digital system make it difficult to achieve the objective. The noises influence the amplitude and timing of transmitted signal, thus the impact impels the correct reception. These noises are either relative to, or independent of the original transmitted signal amplitude. The problem of independent noise can be easily overcome by reinforce the amplitude of

the transmitted signals. But it is more arduous to solve the problem of the proportional noise source. This type noise only can be minimized or erased by designing the signaling circuit and transmitting environment carefully. The most critical proportional noise sources are cross-talk, reflection and self-induced power supply noise. In this section, these types of noise sources and the methods commonly used to deal with them will be discussed.

2.3.1 Cross-talk [7]

The problem of cross-talk and how to deal with it is becoming more important as system performance and board densities increase. Our discussion on cable-to-cable coupling described cross-talk as appearing due to the distributed capacitive coupling and the distributed inductive coupling between two signal lines. When the cross-talk is measured on an undriven senses line to a driven line (both terminated at their characteristic impedance), the near end cross-talk and far end cross-talk have quite distinct features, as shown in the **Fig 2-3**. It should be noted that the near end component reduces to zero at the far end and vice versa. At any point in between, the cross-talk is a fractional sum of the near and far end cross-talk waveforms as shown in the figure. It also can be noted that the far end cross-talk can have either polarity whereas the near end cross-talk always has the same polarity as the signal causing it.

The amplitude of the noise generated on the undriven senses line is directly related to the edge rates of the signal on the driven line. The amplitude is also directly related to proximity of the two lines. This is factored into the coupling constants K_{NE} and K_{FE} by terms that include the distributed capacitance per unit length, and the length of the line. The lead to lead capacitance and mutual inductance thus created

causes “noise” voltages to appear when adjacent signal paths switch.

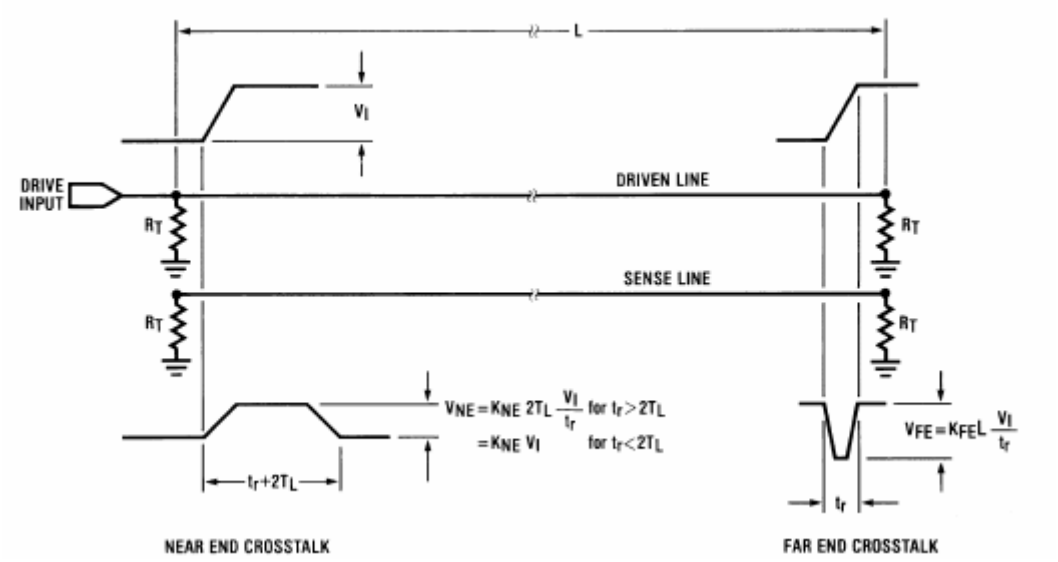


Figure 2-3 Cross-talk

Several useful observations that apply to a general case can be made:

- The cross-talk always scales with the signal amplitude V_I.
- Absolute cross-talk amplitude is proportional to skew rate V_I / t_r, not just $1/ t_r$.
- Far end cross-talk width is always t_r.
- For $t_r < 2T_L$, when tr is the transition time of the signal on the driven line and T_L is the propagation or bus delay down the line, the near end cross-talk amplitude V_{NE} expressed as a fraction of signal V_I is K_{NE} which is a function of physical layout only.
- The higher the value of “t_r” (slower transition times) the lower percentage of cross-talk (relative to signal amplitude).

From these above points, the goal of serial link, high-speed transmission, makes the effect of cross-talk worse and more significant. The methods to reduce the amplitude of the cross-talk include: diminishing the amplitude of transmission data, arranging the layout carefully to reduce the coefficient K_{NE} (the value of mutual capacitance and

mutual inductance), lessening the times of the signal transition by coding the data and techniques like slew-rate control of driver output signals.

2.3.2 Reflection

Reflection-induced inter-symbol interference is the most common type of proportional noise on the serial link. Like the **Fig 2-2**, signal lines must be terminated. This can be accomplished by setting termination circuits on either the transmitter or the receiver end of line. The use of the termination circuit is to absorb the transmitted signal energy, and avoid it reflected back into transmission medium.

The reflection of signal is given by [8]

$$V_{reflected} = \rho V_{incident} \quad (2\text{-}1)$$

$$\rho_L = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad \rho_S = \frac{Z_S - Z_0}{Z_S + Z_0} \quad (2\text{-}2)$$

Where: ρ_L =load reflection coefficient, ρ_S =source reflection coefficient, Z_L=load resistance, Z_S=source driving-point resistance, Z_0=transmission line impedance

Terminating both at source and destination ends of the transmission medium can be used to alleviate this problem at the expense of increased power dissipation. Automatic impedance control can also be used to reduce reflection noise by dynamically adjusting the termination resistor to match the interconnection characteristic impedance [9].

2.3.3 Power Supply Noise

Self-induced power supply noise is a result of the finite supply pin impedances in the semiconductor package. Power supply noise is perhaps the most important contributor to system noise. When any element switches logic state, the current drawn from the external supply of the chip changes at a rate equal to dI/dt .The inductance L of the supply voltage bonding wire will then cause the on-chip power supply voltage drop by a voltage $\Delta V = L\frac{di}{dx}$ .If the drop becomes too large; it can cause the internal logic error. Even a supply spike on one circuit's output could feed an extraneous noise voltage into the next device's input. It is a problem in almost every digital system. However, power supply noise is generally not a dominant voltage noise in the differential links. Sending complementary signals allow the total current draw from (and discharged to) each power supply to be constant, eliminating large current spikes across the power pin inductors or power distribution inductance. Moreover, since the differential pairs are nicely balanced, to the first order, any power supply noise coupled to the signal pair at both the transmitter and the receiver are common-mode.

Although power supply noise affects different systems by different degree, its presence in digital systems has stimulated enormous research efforts in techniques to reduce the dI/dt noise. Such techniques include minimizing the inductance of power distribution networks, employing constant-current drivers or more generally keeping the total current drawn from each supply constant, increasing the bypass capacitance both on the chip and on the board, using separate power supplies for noise-sensitive circuit, generating on-chip supplies using voltage regulators, slowing down signal transition using slew rate control [10], and using coding schemes that reduce switching frequency of signals [11].

2.4 Signaling Circuits

The noise sources mentioned in Section 2.2 all are proportional to transmitted signal amplitude and hence cannot be overcome by simply increasing the signal swing. Therefore, these noise sources are the primary types of noise that the transmitter and receiver must deal with.

The transmitter drives a HIGH or LOW analog voltage onto the channel and is designed for a particular output-voltage swing based on the system specification. The design issues are to maintain small voltage noise and timing noise on the signal. There are two types of output drivers to drive the output: voltage-mode drivers and current-mode drivers. Voltage-mode drivers, as shown in **Fig 2-4 (a)**, are switches that switch the line voltage. Because the switches are implemented with transistors, the driver appears as a switched resistance. To switch the voltage fully, a small resistance is needed which typically requires a large switching device. In contrast, current-mode drivers, as illustrated in **Fig 2-4 (b)**, are switching current sources. The output impedance of the driver is much higher than the line impedance. It is also called high impedance signaling. Therefore, the transmitter bandwidth is typically not an issue even with significant output capacitance. The voltage to be transmitted on the line is determined by the switched current and the line impedance or an explicit load resistor. The driver can be simply implemented by biasing the MOS transistor in its saturation region. Current-mode drivers are slightly better in terms of insensitivity to supply-power noise because they have high output impedance and hence the signal is tightly coupled only to V_{OH}, the signal return path. The output current does not vary with ground noise as long as the current source bias signal is tightly coupled to the

ground signal. The disadvantage with current-mode drivers is that, in order to keep the current sources in saturation, the transmitted voltage range must be well above ground that increases power dissipation.

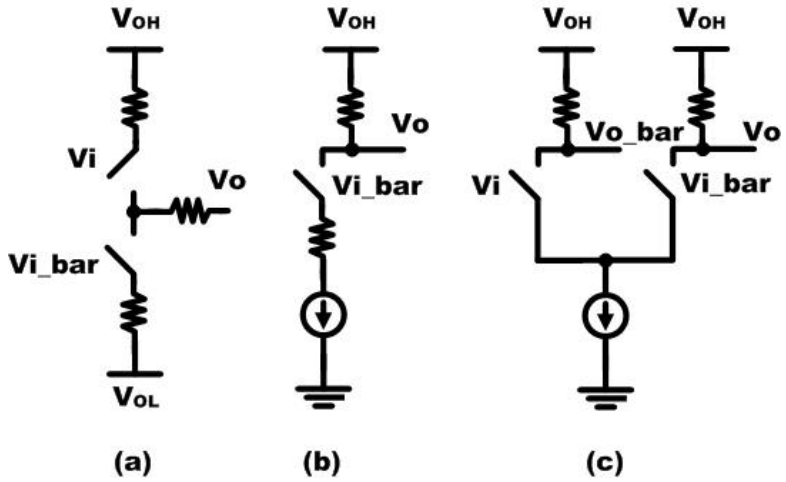


Figure 2-4 Transmitter timing diagram with different transmitter architectures: (a) voltage-mode, (b) current mode, and (c) differential.

For better supply-noise rejection, the differential mode can be adopted, as shown in **Fig 2-4 (c)**, because the supply noise is now common-mode. Since the current remains roughly constant, the transmitter induces less switching noise on the supply voltage that could benefit other transmitted or received signals on the same die. To reduce reflections at the end of the transmission line, the transmitter needs to be terminated. An off-chip termination resistor could introduce significant impedance mismatches because of the package parasitic components. To incorporate the resistor, with current-mode drivers, an explicit on-chip resistor at the driver can act as the termination resistor. If a resistive layer is not available, a transistor in its linear region can be used as the resistor. With voltage-mode drivers, the design is slightly more complex because the switch resistance should match the line impedance Z_0. This may be done either through proper sizing of the driver or by over-sizing the driver and

compensating with an external series resistor, as shown in the **Fig 2-4 (a)**.

2.5 Timing Recovery Architecture

2.5.1 PLL-based Architecture

The task of the timing recovery circuit is to recover the phase and frequency information from the transition in the received data stream. The optimal sample point is midway between the possible data-transition times. Noise and mismatches inherent to the timing recovery circuit produce jitter in the sampling clocks, which degrade the timing margin. Moreover, the transmitter jitter causes uncertainty in the transition points makes clock extraction more difficult. As shown in **Fig 2-5**, two types of timing recovery architectures have been used in links. One is the PLL-based (data-recovery PLL) [12] and the other is the oversampling phase-picking [13].

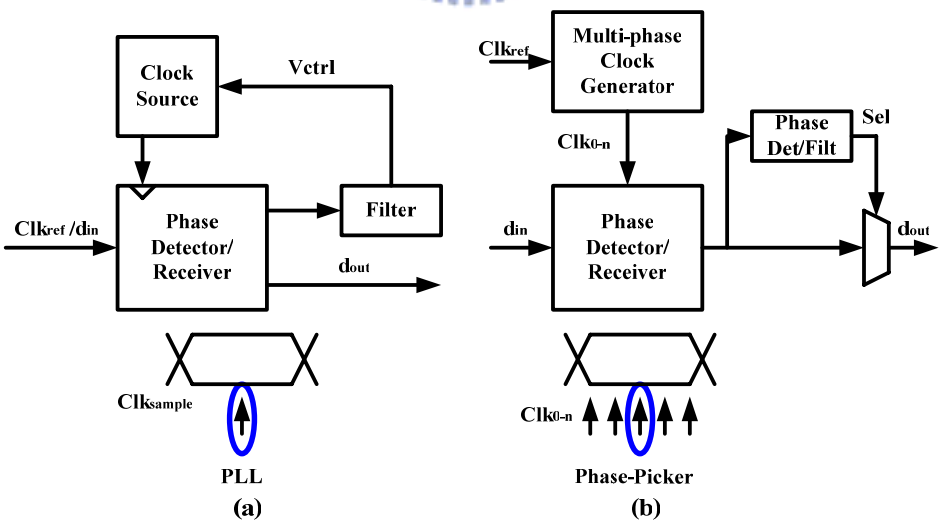


Figure 2-5 Timing recovery architecture

(a) PLL-based (b) oversampling phase-picking

In PLL-based architecture, as shown in **Fig 2-5(a)**, the negative feedback loop

controls the internal phase by adjusting the frequency of the voltage controlled oscillator (VCO) with Vctrl signal until the frequency matches that of an external reference. A phase detector detects the phase difference between the sampling clock and the external input data signal, and adjusts the VCO control voltage. A phase detector generally drives a charge pump that converts the phase difference into a charge. A filtered version of this charge becomes the VCO control voltage. Based on the phase information of the data, the best sample is chosen as the data bit by some decision logic. To maintain good phase relationship between the sampling clock and the data transitions, the PLL should detect the input phase accurately and track any input jitter with a high loop bandwidth. Unfortunately, the stability limits the loop bandwidth of the system. Because the timing information is embedded in the data system, coding of the data is used to ensure a minimum and maximum transition density. High data transition density in the data stream is preferred since it could maintain the stability of the system.

PLL-based timing recovery architectures can be categorized into full-rate and half-rate architectures. In a full-rate circuit the position of the data transition is compared to the falling edge or rising edge of the clock and clock frequency is equal to the data rate as shown in **Fig 2-6 (a)**. Single edge triggered flip flop can be used to retime the data. On the other hand, the location of the data transition is compared to both rising and falling edges of the clock in a half-rate circuit and the clock frequency is equal to one half of the data rate as shown in **Fig 2-6(b)**. Due to the one half of the clock frequency, double edge triggered flip flop is needed to perform the data retiming.

The most important advantage of half-rate architectures is the reduction of the circuit speed by a factor of two. This often means the reduction of the total power dissipation. In fact, as the operation speed of circuits approaches the maximum

operating frequency of a particular technology, the required power consumption grows exponentially. In addition, the de-multiplexing performed simultaneously by half-rate architecture is another attractive feature that makes them suitable for serial link architecture. It can reduce the complexity, hardware, and power dissipation of the deserializer.

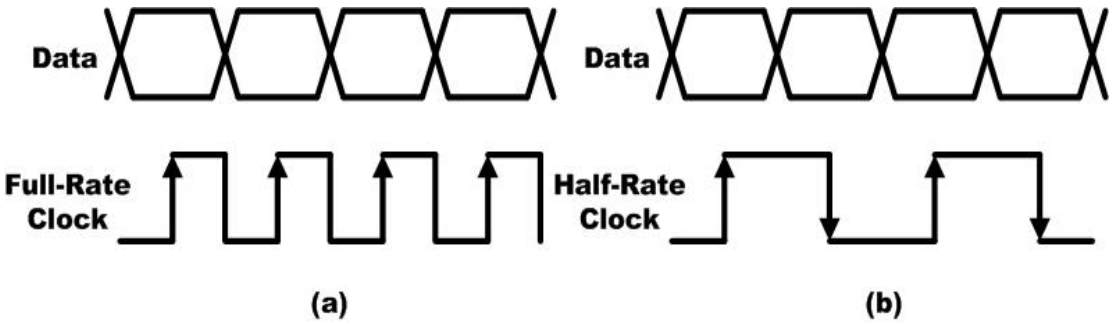


Figure 2-6 (a) Full-rate data and clock (b) Half-rate data and clock

The duty cycle mismatch is a major concern in employing half-rate timing recovery architecture. If the spacing between the rising and falling edges of the clock signal is different from half to the clock period, the width of the data eye sampled by the rising edge is different from that sampled by the falling edge, resulting in bimodal jitter. So the duty cycle of the clock signal must be considered carefully in the design of half-rate timing recovery architecture.

	Full-Rate	Half-Rate
Circuit Operation Speed	**Symbol Rate**	**Half of the Symbol Rate**
Number of Clock Phase	**Single Clock Phase**	**Dual Clock Phase**
DeMux	**None**	**Can do 1:2 DeMux**
Clock Duty Cycle	**Not Important**	**Important**
Jitter Tolerance Margin	**Larger**	**Lower**

Table 2-2 Comparison between full-rate and half-rate timing recovery

architectures[14][15]

2.5.2 Oversampling Phase-picking Architecture

The second timing recovery scheme is the oversampling phase-picking as shown in **Fig 2-5 (b)**. Instead of using feedback loop to control the sampling phases, the data stream is sampled at multiple phase positions per bit creating an oversampling representation of the data stream. It does not require data coding or frequency acquisition since the system clock is readily available through the clock channel. What has to be handled is to adjust the skew between the clock and received data streams. Transitions in the data can be extracted from the sampled data. Based on the data transitions, the sample position nearest the center can be chosen as the data bit. The way to choose data is determined by different digital algorithms, like majority voting [16]. The phase-picking architecture has several advantages. First, it replaces the feedback loop with a feed-forward loop, allowing the selected sample to track phase movements of the data with respect to the clock without an intrinsic bandwidth limitation. The maximum tracking rate is limited by the transition information present. This fast tracking can potentially track the transmit PLL's jitter accumulation. A second advantage of the phase-picking architecture is that long PLL phase-locking time is not needed. Phase decisions are made whenever input transitions are present. The primary disadvantage of the architecture is that there is an inherent static phase error due to the phase quantization. Higher oversampling ratios could reduces the static phase error but add significant complexity to the design. Furthermore, inherent sampler uncertainty limits the minimum quantization error. More significantly, the increased number of samplers increases the input capacitance, hence limiting the input bandwidth. Therefore, the architecture has a trade-off between the input bandwidths

and static phase offsets. For high input bandwidths, the tradeoff favors a low oversampling ratio with the penalty of higher static phase offsets due to the coarse quantization. Besides, due to the open loop mechanism, an error may occurs when sampling point just stands on the data edges, which is not a good position for sampling time, This condition is usually introduced by the static phase error between clock and signal, i.e. the timing skew. However, the feed-forward loop could not offer a mechanism to eliminate the effect of timing skew, which may cause the design complexity of the decision algorithm.

Chapter 3

Phase-Locked-Loop

3.1 Introduction

A phase-locked loop (PLL) is basically an oscillator whose phase and frequency is locked to certain times of input, reference frequency. PLL is a widely used analog circuit. It can be used to recover a clock from the input data, perform synchronization, frequency synthesizer, and generate multiple phases with equal phase resolution. Recently, the PLL designs play a key role in the link performance due to the demand of higher bandwidth in high-speed link. In this chapter, a charge-pump type PLL will be introduced. This circuit with 75MHz reference frequency input generates a clock signal at 150MHz. By adopting four differential stages in voltage controlled oscillator, it generates eight clock phases for the use of the eight-to-one multiplexer.

3.2 Phase-Locked Loop Architecture

The block diagram of a typical PLL circuit is shown as the **Fig 3-1**. The structure consists of the following circuit: a Phase-Frequency Detector (PFD), a Charge Pump, a Loop Filter, a Voltage-Controlled Oscillator and a Divider. The PLL output frequency is twice as fast as the input frequency. Therefore, a divided-by-2 circuit is needed. The internal signal generated by PLL system is called Fback and the external

signal given from outside is called by Fref. These two signal is compared by using the PFD and the PFD generates the adjusting signals, Up and Down to charge pump. The adjusting signals will control the current to charge or discharge the Loop Filter. The VCO is a circuit to generate a clock signal with the adjustable frequency. The frequency depends on the voltage Vctrl and the relationship is an inverse ratio. The Loop Filter is commonly a low-pass filter and provides extra poles and zeros to suppress the high-frequency signal from the PFD. After series of comparison, while the phase difference between Fback and Fref will be constant and the frequencies of Fback and Fref will be nearly the same, this means the PLL is "locked".

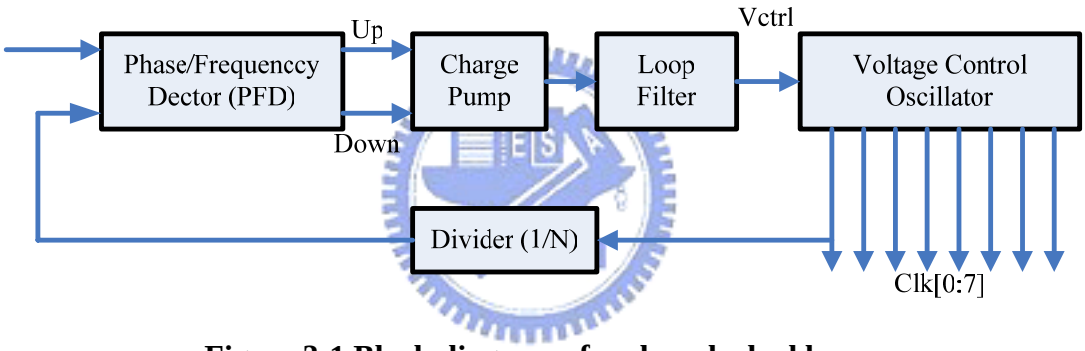


Figure 3-1 Block diagram of a phase locked loop

3.3 Circuit Implementation

3.3.1 Phase Frequency Detector (PFD)

The PFD is a digital sequential circuit to detect the input phase difference between Fref and Fback. It generates two logic signals "Up" and "Down". According to the logic signals, the PLL system works at the tri-state operation as shown in **Fig 3-2**. The tri-state operation allows a wide range of detection for $\Delta\phi = \pm 2\pi$. It detects both phase error and frequency difference.

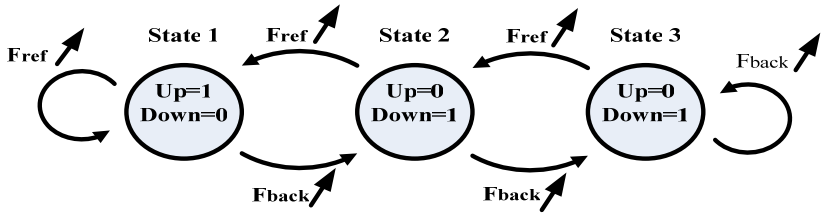


Figure 3-2 tri-state diagram of the phase detector

In the **Fig 3-2**, the state Up=1 and Down=1 never occurs. The UP and Down have individual usage. UP is used to increase the frequency of the signal Fback. In contrast, Down is used to decrease the frequency of Fback. In the case that the reference signal lags the feedback signal as shown in **Fig 3-3**, Down will be set high from low, and on the rising edge of reference signal, the Up will be set high. Thus, the reset is set to high at almost the same time to pull both Up and Down low. In the opposite case that the reference signal leads the feedback signal, the Up will be set high first and the Down and reset will be set high while the rising edge of feedback signal arrivals. Repeating these operations for a long time, the PLL will synchronize the reference signal and feedback signal. Therefore, the PLL is "locked" and both Up and Down will keep low.

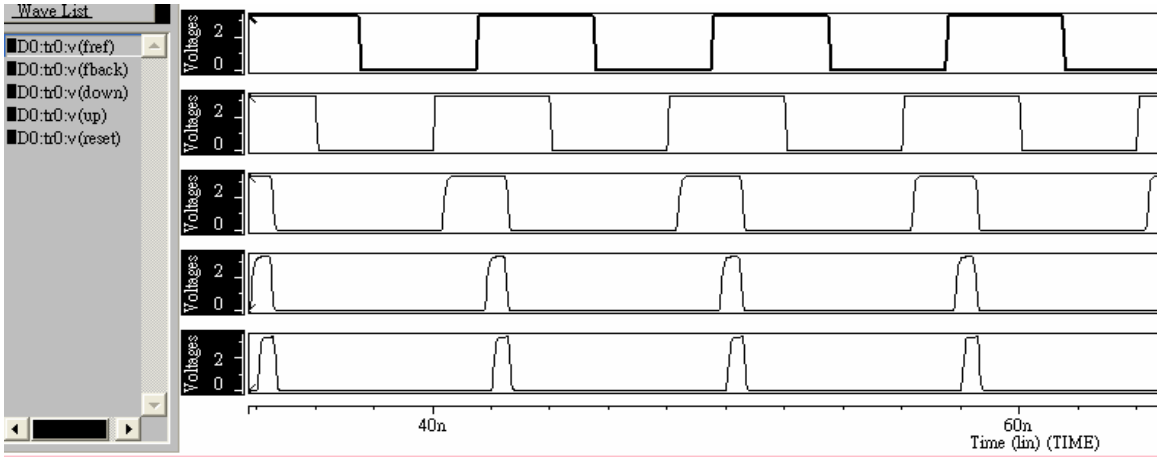


Figure 3-3 reference signal comes after feed back signal

Generally, the framework of PFD consists of two D-flip-flops, one NOR gate and one delay circuit as shown in **Fig 3-4**. In this part, the True-Single Phase Circuit (TSPC) type D flip-flop is used; **Fig 3-5** shows the architecture of the PFD.

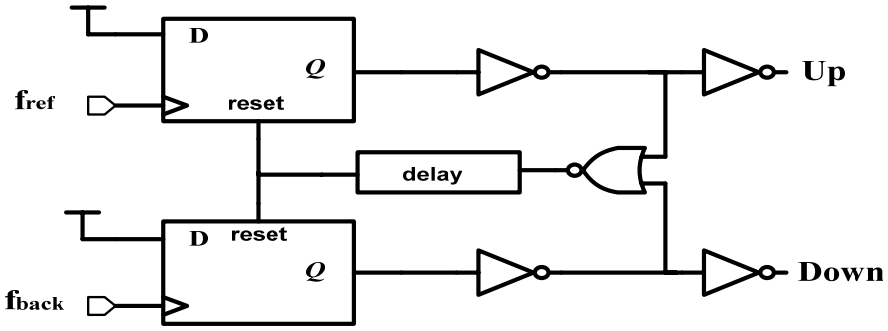


Figure 3-4 structure of PFD

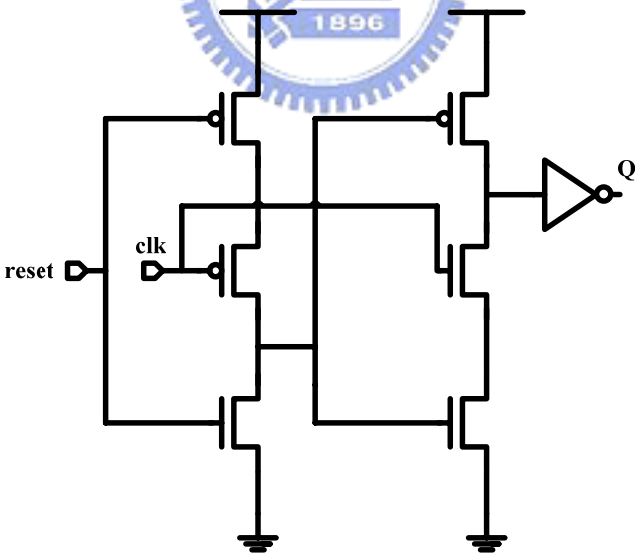


Figure 3-5 Dynamic D Flip-Flop TSPC[17]

According to the PFD transfer characteristic curve as shown in the **Fig 3-6**, we can find that when the phase difference is small, the reset will be generated in a short

time. This condition causes that Up and Down signals may not reach the full swing and it is difficult to identify the logic signal for charge pump. Thus the loop filter will not be charged or discharged due to the very narrow pulse of the Up and Down signal. This occurrence is called dead zone. The dead zone is one kind of source of the output jitter. Because it allows the VCO to accumulate as much random phase error as the extent of the dead zone while receiving no corrective feedback to change the control voltage[18]. The dead zone problem is shown as **Fig 3-7**. In order to cancel the discrete part of the transfer curve, a delay circuit is added. If the delay time is precisely matched, the dead zone can be reduced. However, the PFD will have the limit on the maximum operation frequency that is proportion to total reset path delay [19]. Therefore, the delay time should be kept minimal.

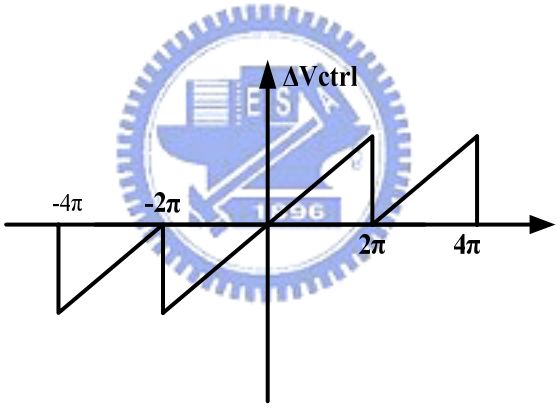


Figure 3-6 PFD transfer characteristic curve

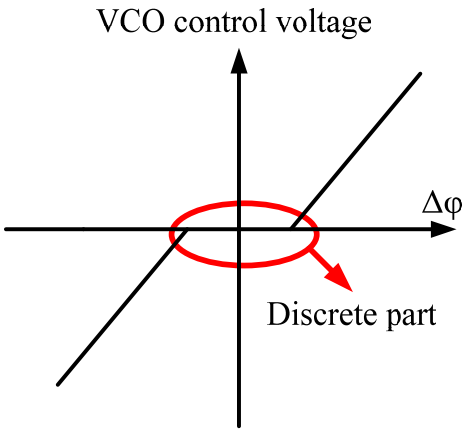


Figure 3-7 PFD transfer character curve with dead zone

3.3.2 Charge Pump

The charge pump is a circuit that supplies current to the loop filter to adjust the control voltage of the VCO. However, the charge injection is an undesirable feature of charge pump. The injection effect is caused by the overlap capacitance of the switch devices and by the capacitance at the intermediate node between the current source and the switch devices.

Fig 3-8 shows a simple pump circuit, and the output is directly affected by the switching noise from the overlap capacitance of the switch deices. In addition, the intermediate nodes between the current source and switch devices will charge toward the supplies while the switch devices are off.

The charge injection effect will result in a phase offset at the input of the phase detector when PLL is in locked mode. Thus, the jitter will increase. When the charge pump current is diminished, the effect is comparatively in big scale, and the phase offset increases. In order to solve the problem, the control voltage must be isolated from the switch noise resulted from the overlap capacitance of the switch devices. Moreover, in order to fix the charge-sharing problem, an operation at amplifier can be adopted to buffer the output voltage to let the intermediate nodes switch to the output of the amplifier while the switches are off[20].

To combat the injection problem, a charge pump circuit is designed as shown as **Fig 3-9**. In this circuit, the switch devices M13 and M18 are isolated from the sensitive output Vctrl by inserting devices M17 and M18. When switching devices are off, the intermediate nodes between M13, M14, M17 and M18 will be charged toward the Vctrl by the gate overdrive of the current source devices. In order to make sure the matching between I_p and I_n, the cascade current mirror circuit is used. In addition, the

gate node of devices M16 and M11 are always connected to VDD and VSS directly. So, there are always constant currents flowing through M16, M11. Because of the full-swing signals Up and Down, the architecture makes sure that the output current can match the current on M11 and M16 precisely and quickly.

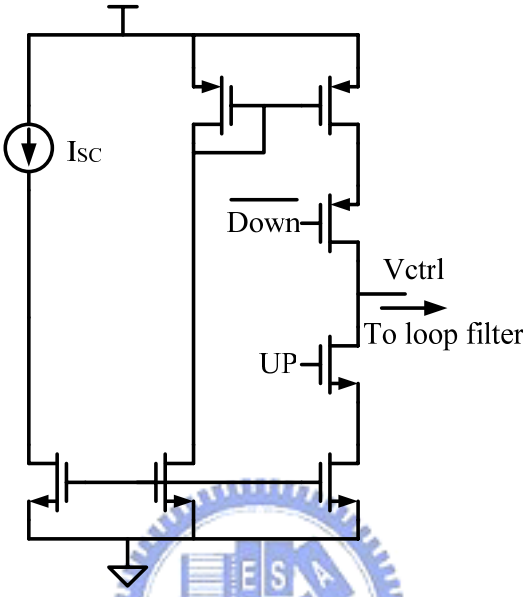


Figure 3-8 Charge pump with charge injection effect

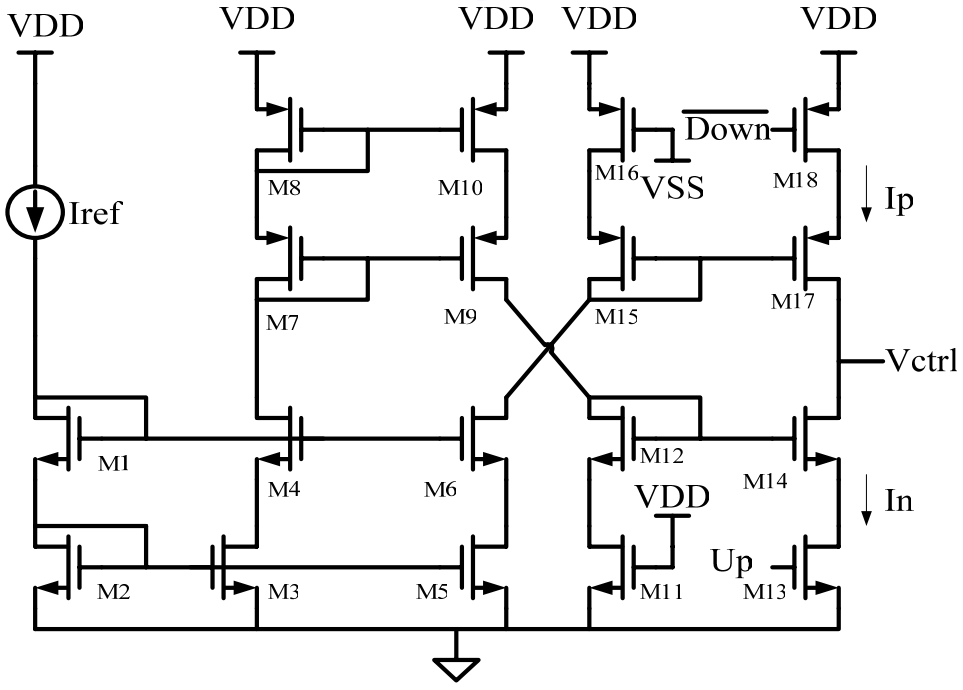


Figure 3-9 Schematic of charge pump

3.3.3 Voltage Control Oscillator (VCO)

The building blocks of the VCO include a four stages ring oscillator and a self-biased replica-feedback bias generator. **Fig 3-10** and **Fig 3-11** shows the schematic of the four stages VCO and the delay cell.

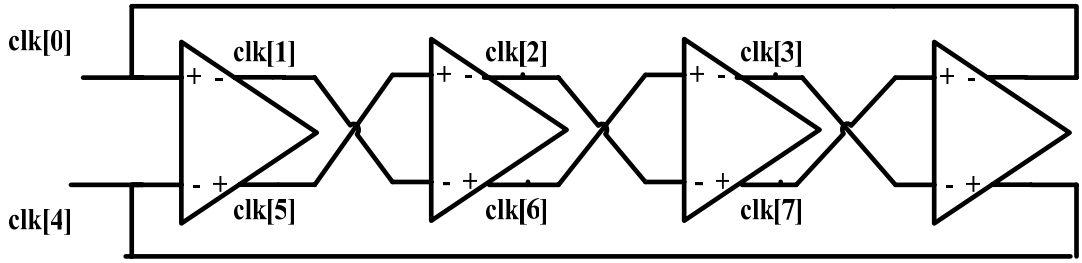


Figure 3-10 Schematic of the four stages VCO

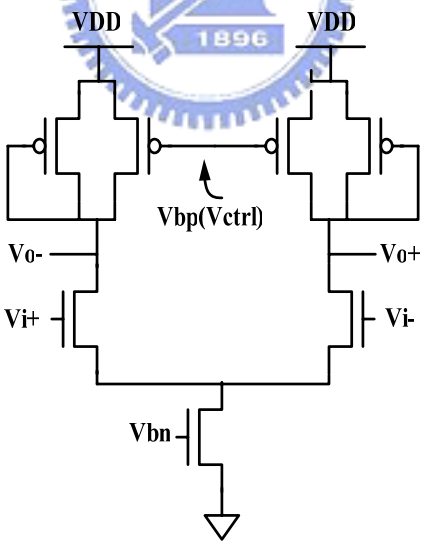


Figure 3-11 Schematic of VCO delay cell with symmetric load elements

The voltage control oscillator is critical and sensitive block in the PLL system. In order to have the low jitter characteristic performance of the output clock signal. In the mixed mode circuit, the delay buffer used in the section should have the low

sensitivity to the noise of the supply and substrate voltage. Therefore, the basic building block of the VCO used in this thesis is based on the differential delay stages with symmetric loads[21]. I-V curve of the delay stage with symmetric load is shown as **Fig 3-12**[22]. Although the I-V curve is nonlinear but is symmetrical to the center of the output voltage swing, and the delay stage has high noise immunity.

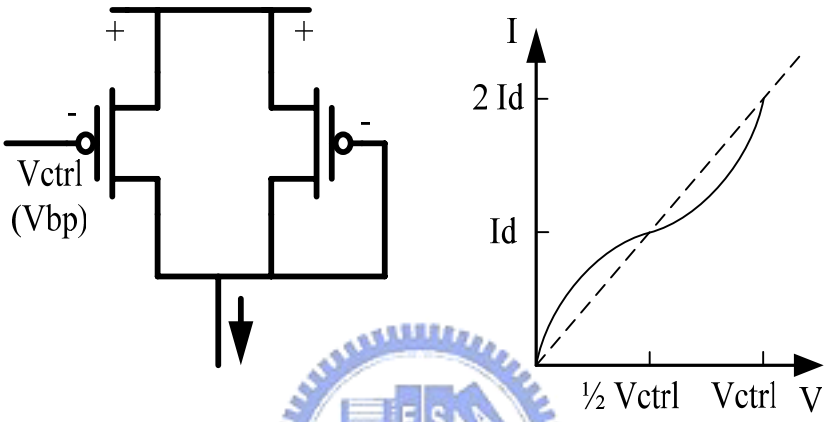


Figure 3-12 The symmetric load I-V curve

Based on the scheme as shown as **Fig 3-11**, the effective resistance of the symmetric load, R_{eff} is directly proportion to the small signal resistance at the end of the swing range that is one over the transconductance (gm) for one of the two equally sized devices when biased at control voltage. Thus, the delay per stage can be expressed by the equation:

$$t_d = R_{eff} \times C_{eff} = \frac{1}{gm} \times C_{eff} \qquad \textbf{(3-1)}$$

where C_{eff} is the effective delay cell output capacitance, R_{eff} is the effective resistance of delay cell. The drain current for one of the two equally sized devices at Vctrl is given by

$$I_d = \frac{k}{2}[(Vdd - Vctrl) - |Vtp|]^2 \quad \textbf{(3-2)}$$

where k is the device transconductance of the PMOS device. Taking the derivative with respect to (Vdd-Vctrl), the transconductance is given by

$$gm = k[(Vdd - Vctrl) - |Vtp|] \quad \textbf{(3-3)}$$

Combining (3-1) with(3-3), the delay of each stage can be written as

$$t_d = \frac{C_{eff}}{k[\{Vdd - Vctrl) - |Vtp|} \quad \textbf{(3-4)}$$

The period of a ring oscillator with N delay stages is approximately 2N times the delay per stage. This translates to a center frequency of

$$f_{vco} = \frac{1}{2Nt_d} = \frac{k[(Vdd - Vctrl) - |Vtp|]}{2NC_{eff}} \quad \textbf{(3-5)}$$

The gain of the VCO is defined as the absolute value of the slope on the frequency-Vctrl curve. Thus, K_{vco} can be expressed as

$$K_{vco} = \left| \frac{\partial f_{vco}}{\partial Vctrl} \right| \quad \textbf{(3-6)}$$

As a result, the center frequency of the VCO is in direct proportion to (Vdd-Vctrl) and has no relationship to supply voltage. K_{vco} is independent of buffer bias current and the VCO has the first order linearity.

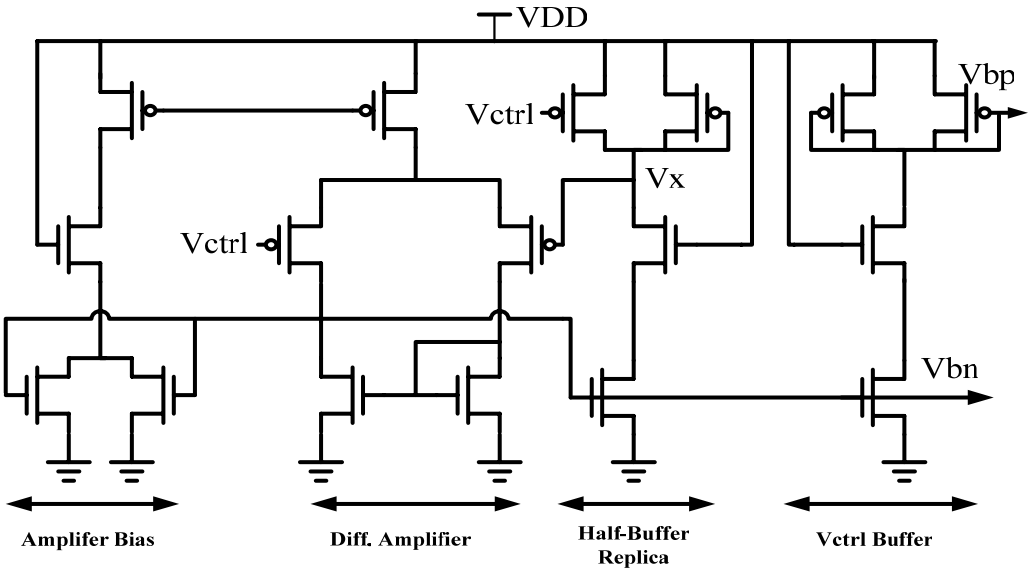


Figure 3-12 Replica-feedback current source bias circuit

The VCO bias generator providing the bias voltage Vbn and Vbp is shown as **Fig3-12**. It is composed of an amplifier bias, a differential amplifier, a half-buffer replica and a control voltage buffer. The task of the framework is to adjust the bias buffer current and provide the correct Vctrl with lower swing limit for the buffer stage. In order to accomplish the target, the differential amplifier and the half-buffer replica form a negative feedback, and the voltage Vx equals the voltage Vctrl so that the output swings vary with the control voltage rather than is fixed. In order to track all variations at frequency for the PLL design, the bandwidth of the bias generator is typically set at least equal to the center frequency of the delay stages.

The bias generator also provides a buffered version of Vctrl at the Vbp output using an additional half-buffer replica. This output isolates the Vctrl from the potential capacitance coupling in the buffer stages. There is an important issue. The noticeable the supply-independent bias exists on the “degeneration” bias point. If all the transistors carry no current at beginning, they may remain indefinitely while the supply turning on. The reason is that the loop can get balance when all devices carry

no current. Therefore, an additional start-up circuit is necessary to propel the loop circuit out of the degenerate bias point.

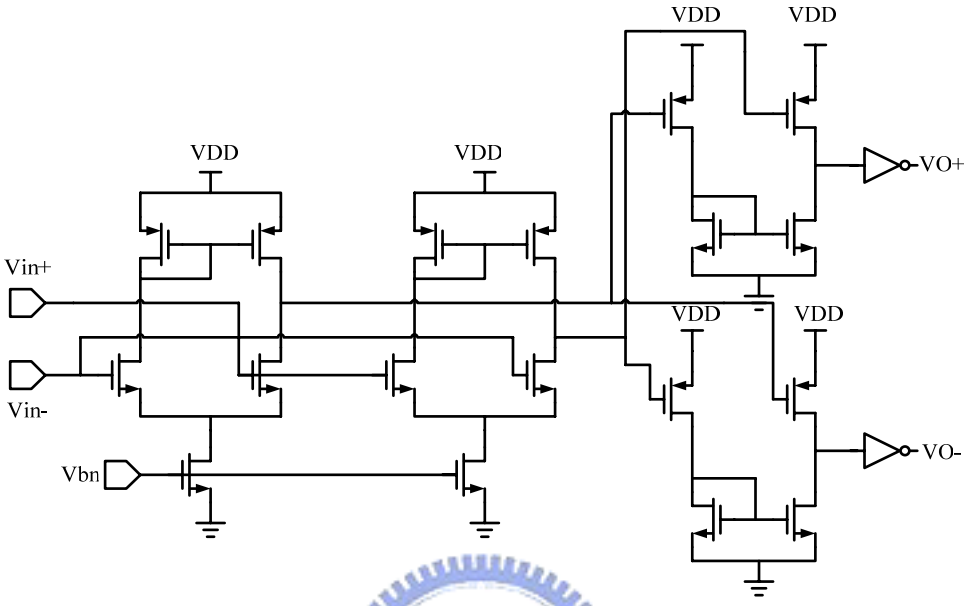


Figure 3-13 Schematic of differential-to-single-ended converter

The differential-to-single-ended converter is shown in **Fig 3-13**. It consists of two opposite phase NMOS differential amplifier driving two PMOS common-source amplifier connected by NMOS current mirror. The first level NMOS differential amplifier amplifies the input differential-small signal to drive the next level PMOS amplifier and a single-ended full-swing signal is generated. The two differential amplifiers use the same current source bias voltage, Vbn, generated by the self-biased generator for the VCO. According to Vbn, the circuit corrects the input common-mode voltage level and provides signal amplification. The inverters are added at the output to improve the driving ability.

The duty-cycle corrector is connected behind the differential-to-single-ended converter to ensure that the duty-cycle of the VCO will be 50% and shown as **Fig3-14**[23]. This duty-cycle correction circuit consists of only two transmission

gates and two inverters, the area is minimal and the power consumption is negligible. The signal Vin+ selected from the multiphase signals turn on M3 and M4, and charges the output node Vout of the duty-cycle corrector almost instantaneously. Because the discharge path of the node Vin+ is already off due to the signal Vin-. The signal Vin-, which is also selected from the multiphase signals, is the one whose rising edge is shifted by 180° in phase from that of Vin+. Similarly, the signal Vin- rapidly discharges the node Vout and delivers the desired 50% duty-cycle signal. The advantage of duty-cycle corrector can apply to many aspects in this thesis, that will be described in the later section.

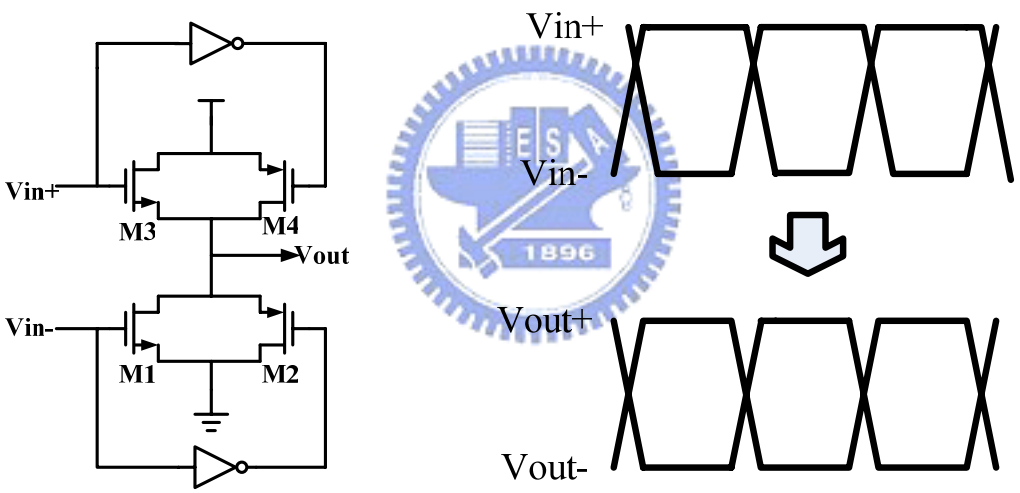


Figure 3-14 Schematic of duty-cycle corrector and its timing diagram

3.3.4 Loop Filter

The loop filter configuration used in this thesis is typically a low pass filter to suppress the high-frequency signal generated from PFD and the circuit is shown as **Fig 3-15**. The capacitance C0 in series with R1 provides a zero in the open loop

response. The additional zero can improve the phase margin and overall stability of the loop. The shunt capacitance C1 can suppress the discrete voltage pulse which disturbs the VCO operation. However, a large C1 can adversely affect the overall stability of the loop.

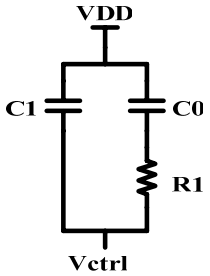
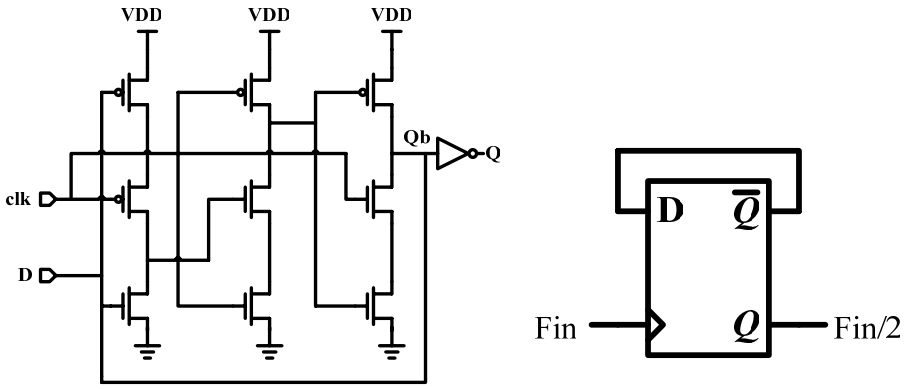


Figure 3-15 2nd order passive loop filter

3.3.5 Divider

In our PLL, we need a divided-by-2 circuit to double input reference frequency. We use a TSPC D-Flip-Flop and connect its inverted output to D input, and the circuit connection is shown as **Fig 3-16(a)**[24]. In this circuit we need to check input clock driving capability to make this circuit have correct operation. The scheme of the divider is shown as the **Fig 3-16(b)**.



(a) **(b)**

Figure 3-16 (a) TSPC asynchronous divided-by-two circuit (b) divider scheme

3.4 Fundamentals of PLL

3.4.1 PLL Linear Model

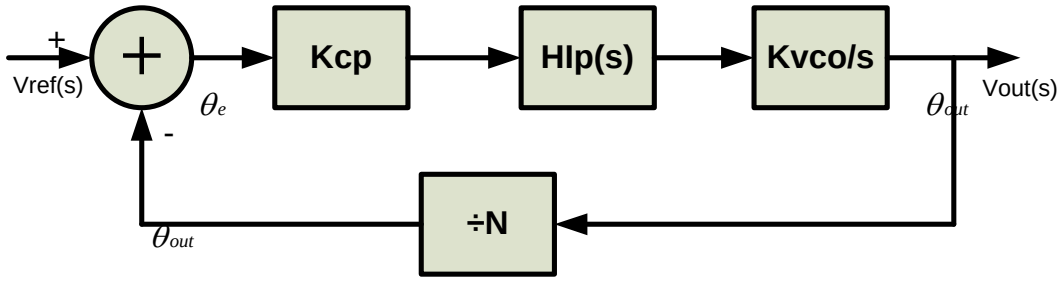


Figure 3-17 PLL linear model

The phased-locked loop is a highly-nonlinear system. However, when the system in the lock mode. Its dynamic response to input-signal phase and frequency changes can be approximated by a linear model. **Fig 3-17** shows the linear mathematical model representing the PLL is in the locked stage.

When the PLL is locked, the PFD as a provider produces a error phase difference defined as $\frac{I_p}{2\pi}$. The output voltage difference is proportional to the error phase difference. The average of the error current within a cycle is $i_d = I_p \frac{\theta_e}{2\pi}$, so that the ratio of the output current to the input phase differential, Kcp is $\frac{I_p}{2\pi}$(A/rad). The loop fliter has a transfer function Hlp(s) (V/A). in order to keep the mathematics simple, the parasitic shunting capacitance, C_1 may be omitted. Then the Hlp(s) can be simplified as $R_1 + \frac{1}{sC_0}$. Kv(Hz/V) is the ratio of the VCO frequency to the control voltage variation. Since the phase is the integral of frequency over time, Kv(Hz/V)

should be changed to $\frac{2\pi K_v}{s} = \frac{K_{vco}}{s}$ (rad/sec V). N is the divider parameter, the ration of the output frequency to reference input frequency.

The open-loop transfer function of the PLL can be represented as

$$G(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{IpKvHlp(s)}{sN} \quad \textbf{(3-7)}$$

From the feedback theory, the close-loop transfer function of the PLL can be found as

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = N\frac{G(s)}{1+G(s)} \quad \textbf{(3-8)}$$

Then, the function **3-7** and **3-8** can be combined and the Hlp(s)= $R_1 + \frac{1}{sC_0}$ is substituted into **3-7**, then the combined function is shown as

$$H(s) = N\frac{(\frac{IpKv}{NC_0})(1+sR_1C_0)}{s^2 + s(\frac{IpKv}{N})R_1 + \frac{IpKv}{NC_0}} \quad \textbf{(3-9)}$$

This can be compared with the classical two-pole system transfer function

$$H(s) = N\frac{\omega_n^2(1+\frac{s}{\omega_z})}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \textbf{(3-10)}$$

Then, the parameters natural frequency ω_n, zero of the LP ω_z and damping factor ζ can be derived as

$$\omega_n = \sqrt{\frac{IpKv}{NC_0}} = \sqrt{\frac{KcpKvco}{NC_0}} \quad \textbf{(3-11)}$$

$$\omega_z = \frac{1}{R_1C_0} \quad \textbf{(3-12)}$$

$$\zeta = \frac{\omega_n}{2\omega_z} = \frac{R_1}{2}\sqrt{\frac{KcpKvcoC_0}{N}} = \frac{R_1}{2}\sqrt{\frac{IpKvC_0}{N}} \quad \textbf{(3-13)}$$

In a 2nd –order system, the loop bandwidth of the PLL is determined by ω_n. But the -3dB bandwidth should be $K = \frac{IpKvcoC_0}{N}$(Hz). As for the value chosen for damping

factor, a large one will bring about response sluggishness and longer time for locking. To the other end, if the value is too small, oscillation for step response will make the system unstable. For the compromise between the two end, ζ =1.414 is adopted for this work.

3.4.2 PLL Noise Analysis and Stability

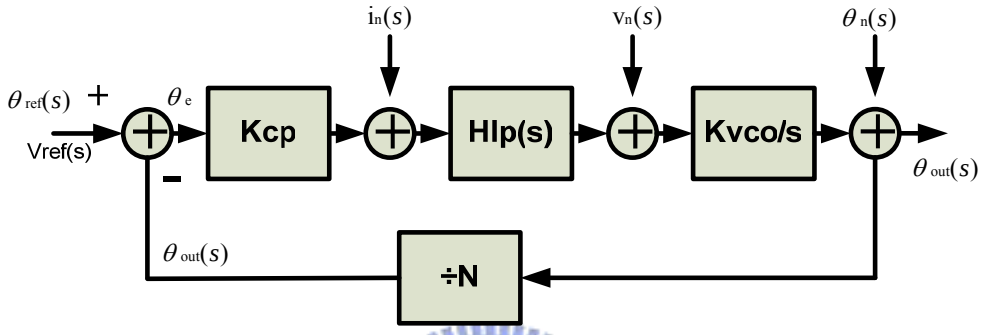


Figure 3-18 PLL linear model with various equivalent noise sources

The transfer function can be derived for disturbances injected at various points in PLL as shown as in **Fig 3-18**. There are three interference sources, $i_n(s)$, $v_n(s)$ and $\theta_n(s)$. The first one is that the current variation injected at the output of the charge pump and the phase detector. The second one is that voltage noise injected at the output of the filter. The third one is that the phase errors injected by the VCO. The table 3-1 shows the response equations of the three interference sources.

source	Noise transfer function	
$i_n(s)$	$H_i(s)=\frac{\theta_{out}(s)}{i_n(s)}=\frac{(\frac{Kvco}{C})(1+sRC)}{s^2+2\zeta\omega_n s+\omega_n^2}$	**(3-14)**
$v_n(s)$	$H_v(s)=\frac{\theta_{out}(s)}{v_n(s)}=\frac{sKvco}{s^2+2\zeta\omega_n s+\omega_n^2}$	**(3-15)**
$\theta_n(s)$	$H_\theta(s)=\frac{\theta_{out}(s)}{\theta_n(s)}=\frac{s^2}{s^2+2\zeta\omega_n s+\omega_n^2}$	**(3-16)**

Table 3-1 Noise transfer function

From the observation of the above equation, the transfer function, $H_\theta(s)$, $H_v(s)$ and $H_\theta(s)$ are respectively low-pass, band-pass and high pass[25][26]. In order to reduce the noise impact, there is one way to increase the loop bandwidth ω_n by increasing the factor Kcp. However, the maximum ω_n is restricted by the update frequency ω_{ref} of the phase detector. From the analysis of the research [19], the criteria of the stability limit can be derived as:

$$\omega_n^2 < \frac{\omega_{ref}^2}{\pi(RC\omega_{ref} + \pi)} \qquad \textbf{(3-17)}$$

In general, ω_n is approximately less than $1/10$ of phase detector update frequency ω_{ref} to avoid the instability. So the restriction of the maximum frequency of loop filter is $\omega_n < \frac{1}{10}\omega_{ref}$.

3.5 Loop Parameters Consideration

After describing each building block in detail, it is noticed that the set of the loop parameters is highly relative to the system performance and is needed to be considered carefully. Refer to the derivation of the transfer function and the noise analysis just mentioned. There are two terms needed to be satisfied for the stability of the PLL system, and for the simplification of the system order from third order to second order to be accurate. First, the capacitor in the loop filter shunt on control voltage for suppression purpose must be much smaller than the filtering capacitance. This is can be explained by the function 3-18 as shown below:

$$\omega_z = \frac{1}{C_0 R_1};\quad \omega_p = \frac{1}{R_1}\cdot\frac{C_0 + C_1}{C_0 C_1} = \omega_z\left(\frac{C_0}{C_1}+1\right) \qquad \textbf{(3-18)}$$

If $C_0 > 20C_1$, the higher frequency pole induced by C_1 can be ignored. Second, as proposed in [27], the (3-16) must be satisfied for the system stability. As a rule, it is true that by keeping $\omega_{ref} > 10\omega_n$, stability in discrete-time model as well as in continuous-time model can be assumed. Under such premise, the remaining loop parameters are be taken into consideration, specifically, natural frequency ω_n, damping factor ζ and the most one, the phase margin of the open loop system.

Fig 3-19 shows the curve for the open loop PLL frequency response. This curve gives the phase margin of approximate 70°. The total parameters of the PLL are listed in the **Table 3-2**. The simulation Vctrl timing diagram and transfer characteristic are shown as the **Fig 3-20 and Fig 3-21**. The supply voltage used is 3.3V and the Vctrl is in the region of 1.0V to 2.0V. The gain of the VCO, Kvco is 130 MHz/V.

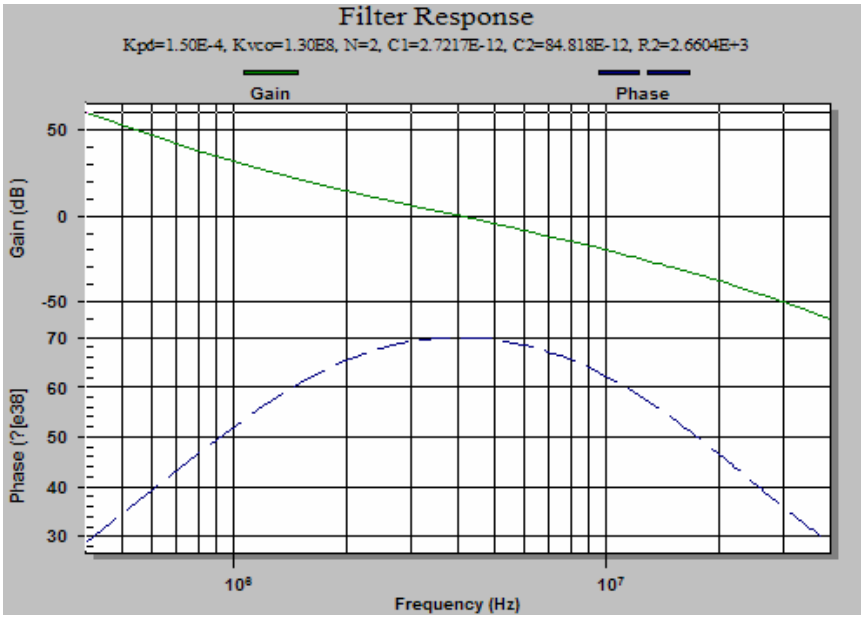


Figure 3-19 open loop PLL frequency response

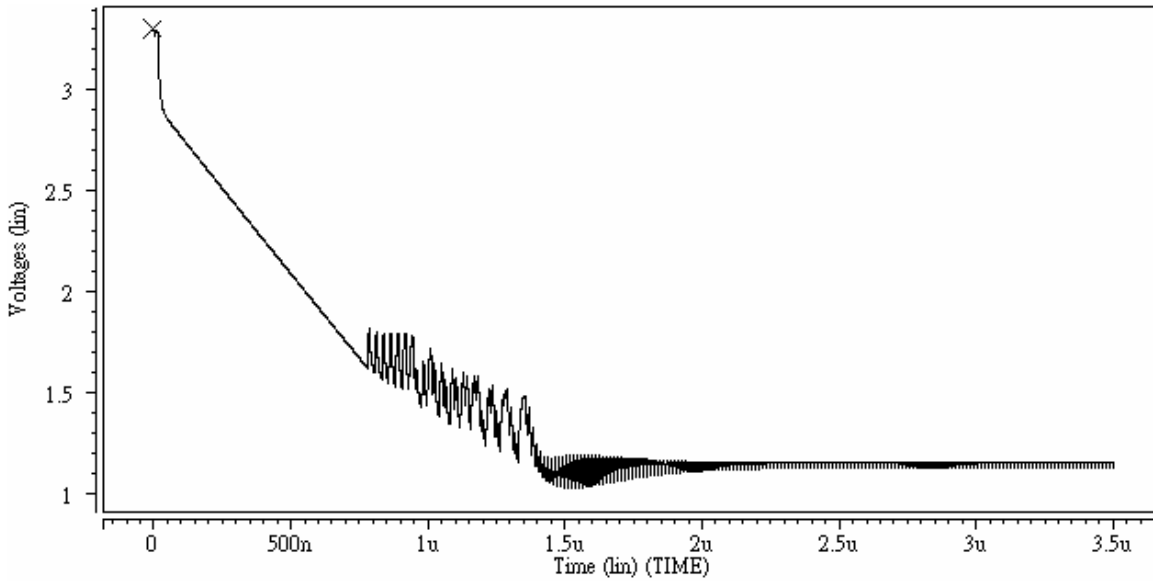


Figure 3-20 Vctrl timing diagram

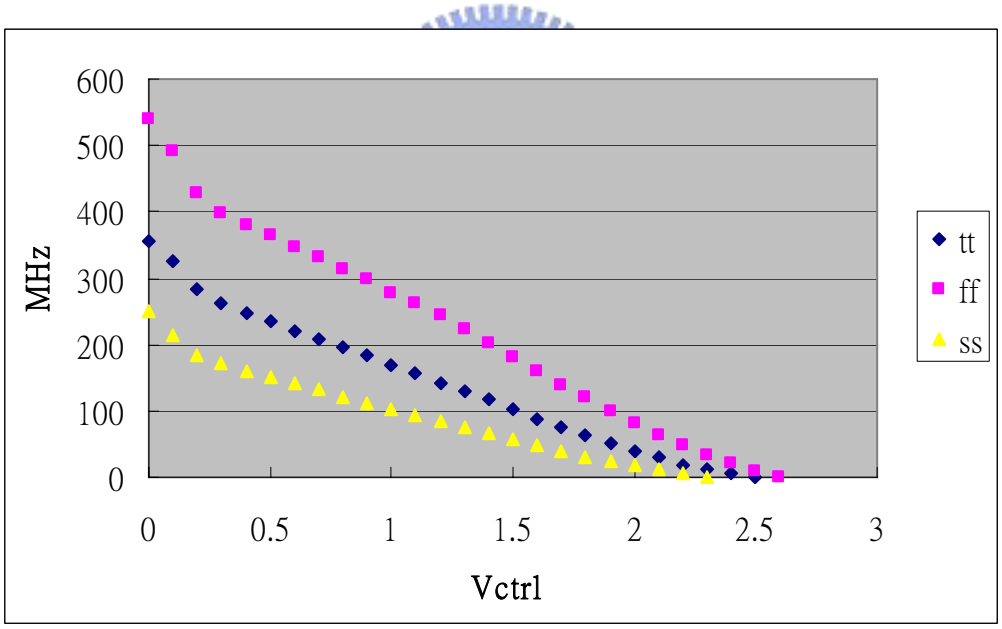


Figure 3-21 Kvco curve

Charge Pump Current (I_{cp})	120uA
VCO Center Frequency (Fvco)	130MHz
K_{VCO}	130MHz/V
Divided by N	2
Loop Bandwidth	4000kHz
Phase Margin	70 degrees
Parameter of Loop Filter	C0=84.81p F
	C1=2.72p F
	R1=2.66k ohm

Table 3-2 Parameter of the transmitter PLL

Chapter 4

Transmitter

4.1 Architecture of Transmitter

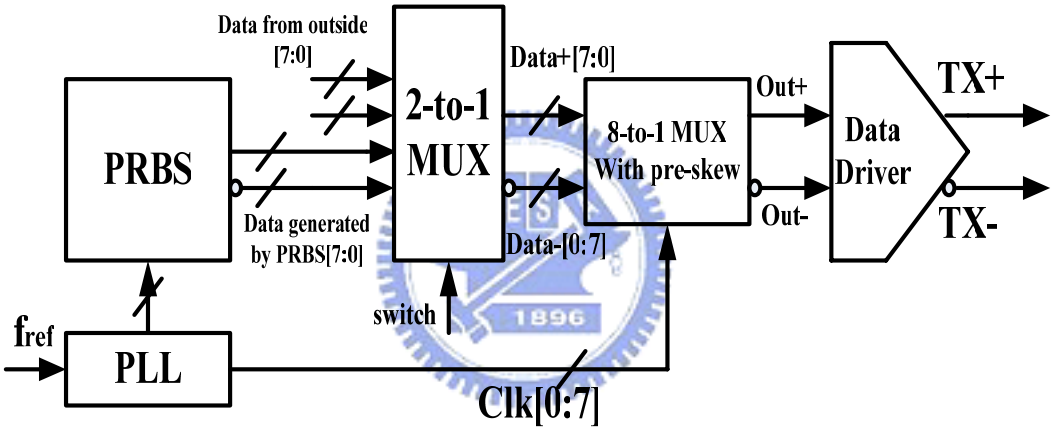


Figure 4-1 Block diagram of the transmitter

Fig 4-1 shows the components of the transmitter. The transmitter is built up by a PRBS circuit, a PLL, a multiplexer, a 8 to 1 multiplexer with pre-skew circuit and a data driver. The purpose of the Pseudo Random Bit Sequence circuit (PRBS) circuit is to generate series of testing data. There is a 2 to 1 multiplexer to select the input data from the testing data or actual channel data. With the 8 to 1 multiplexer, we can reduce the frequency requirement of the timing circuit and we can serialize the parallel and low-speed data to be a 1.2Gbs, high speed, serial transmission data by the eight-phase, 150MHz clock signals generated by PLL. A pre-skew circuit is needed to avoid that the multiplexer samples the data at the transient. Finally, through the data

driver, the data stream is transmitted out with a nominal swing of 200mV. In the following section, we will introduce the circuit and the function of each block in the transmitter architecture in detail.

4.2 Pseudo Random Bit Sequence (PRBS)

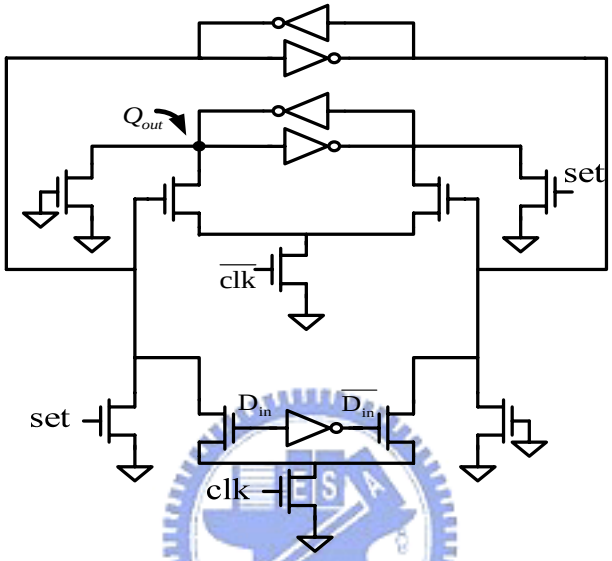


Figure 4-2 PRBS delay cell circuit

The Pseudo Random Bit Sequence is designed for generating a sequential data in random for testing. The delay cell of PRBS is shown as **Fig 4-2**. With a series delay cell, each delay cell can supply a signal for next delay cell and so on. The signal from the XOR can renew the cycle and delay cells will generate the new data. Thus, PRBS can generate a random pattern. In fact, repetition of the pattern exists and the pattern repeats every 2^7-1=127 clock cycles. We also note that if the initial condition of each delay cell is zero, PRBS remains in the degenerate state. Therefore, a signal SET is needed to start up the PRBS. Then we use the outputs of the seven delay cells and XOR gate to form eight parallel input data of transmitter. And the architecture is shown in **Fig 4-3**.

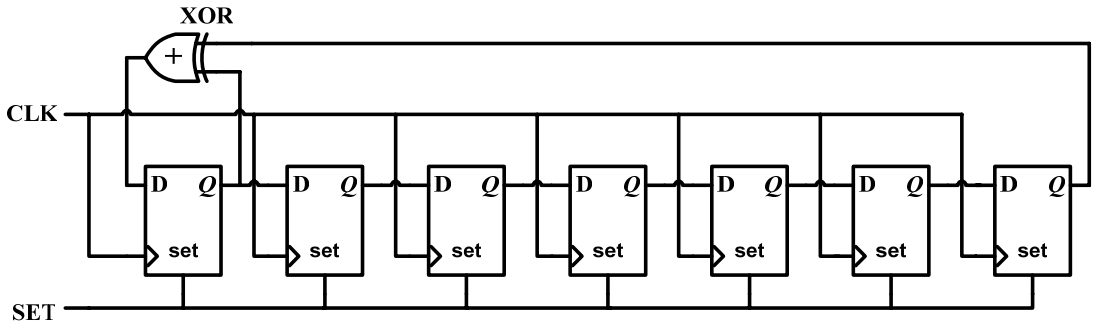


Figure 4-3 Scheme of Pseudo Random Bit Sequence (PRBS)

4.3 Multiplexer (8 to 1)

4.3.1 The Algorithm for Parallel to Serial

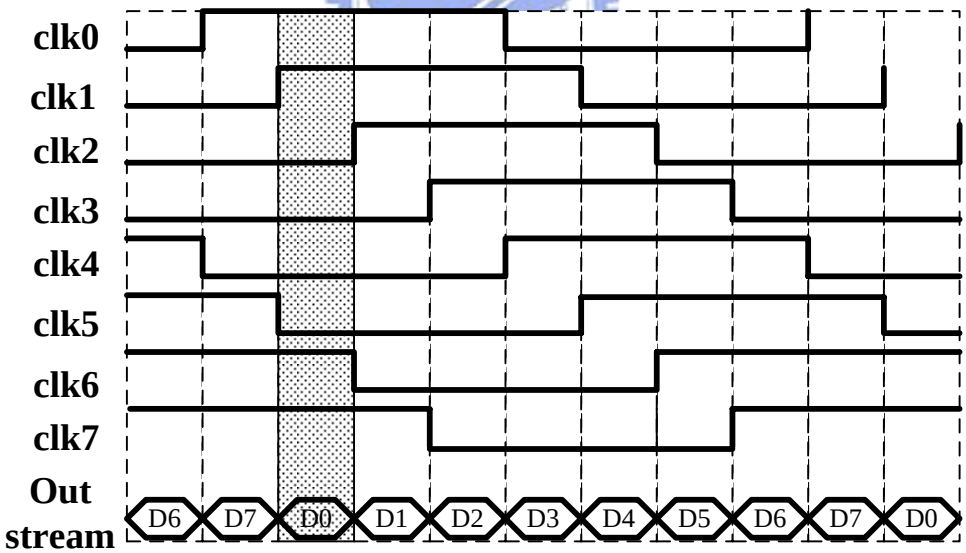


Figure 4-4 Timing diagram of 8:1 multiplexer

When the PLL produces eight-phases 150MHz clock signal, we can make the serial data stream with 1.2Gbps and the relationship between clk0~clk7 and output data stream is shown in **Fig 4-4**. In this thesis, a 3-levels MUX is used to realize

8-parallel data to one serial data and it is shown in **Fig 4-6**. Therefore, the algorithm for the timing schedule and function of each MUX cell is necessary to be considered. As the shaded area in the **Fig 4-4**, when the clk(1,2,6,7) is on, the D0 is given to out stream. It is similar to D1, D2 ….D7. We list the total relationship in a **table4-1** that can help to understand the logic function of the 3-levels MUX.

<table>
<tr><th></th><th>Clock on (level 1)</th><th>Critical clock</th><th>Clock on (level 2)</th><th>Critical clock</th><th>Clock on (level 3)</th><th>Critical clock</th></tr>
<tr><td>D0</td><td>(0,1,6,7)</td><td rowspan="2">(6,2)</td><td>D0 (0,1,6,7)</td><td rowspan="4">(7,3)</td><td>D0 (0,1,6,7)</td><td rowspan="8">(1,5)</td></tr>
<tr><td>D1</td><td>(0,1,2,7)</td><td>D1 (0,1,2,7)</td><td>D1 (0,1,2,7)</td></tr>
<tr><td>D2</td><td>(0,1,2,3)</td><td rowspan="2">(0,4)</td><td>D2 (0,1,2,3)</td><td>D2 (0,1,2,3)</td></tr>
<tr><td>D3</td><td>(1,2,3,4)</td><td>D3 (1,2,3,4)</td><td>D3 (1,2,3,4)</td></tr>
<tr><td>D4</td><td>(2,3,4,5)</td><td rowspan="2">(2,6)</td><td>D4 (2,3,4,5)</td><td rowspan="4">(3,7)</td><td>D4 (2,3,4,5)</td></tr>
<tr><td>D5</td><td>(3,4,5,6)</td><td>D5 (3,4,5,6)</td><td>D5 (3,4,5,6)</td></tr>
<tr><td>D6</td><td>(4,5,6,7)</td><td rowspan="2">(4,0)</td><td>D6 (4,5,6,7)</td><td>D6 (4,5,6,7)</td></tr>
<tr><td>D7</td><td>(5,6,7,0)</td><td>D7 (5,6,7,0)</td><td>D7 (5,6,7,0)</td></tr>
</table>

Table 4-1 the deductive logic of 3-levels multiplexer

As shown in above table, in the first MUX level, we need to separate the adjacent input data. For example, to observe the difference between D0 and D1, we can find that except the clk(6,2), the others are the same. So we can define clk(6,2) is significant to D0 and D1 and is critical to separate D0 and D1. In the second level, the D0 and D1 are classified as the same type and D2 and D3 are classified as the same type. Then, observing D0~D3, clk(7,3) is the critical clock in the second level MUX. Similarly, the D0~D3 and D4~D7 can be separated into two groups by the same way.

Table 4-1 shows the flowchart of how to deal with the data through the 3-levels MUX. The critical clocks of each level are marked. It is useful for us to infer the algorithm and construction of the 3-level MUX.

4.3.2 MUX Architecture

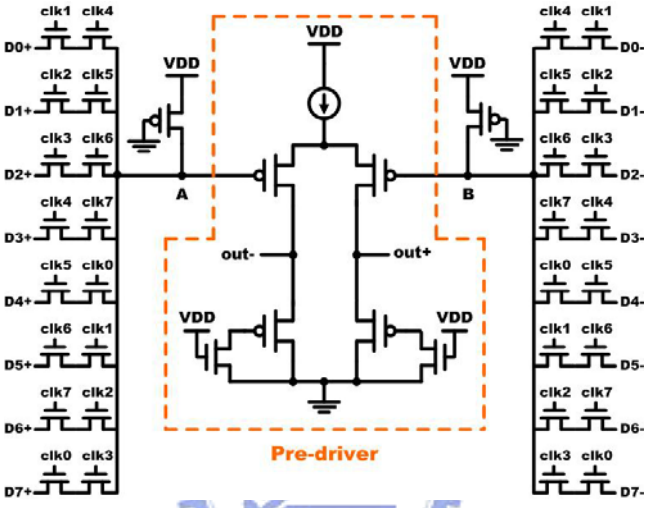


Figure 4-5 Multi-phase Type MUX

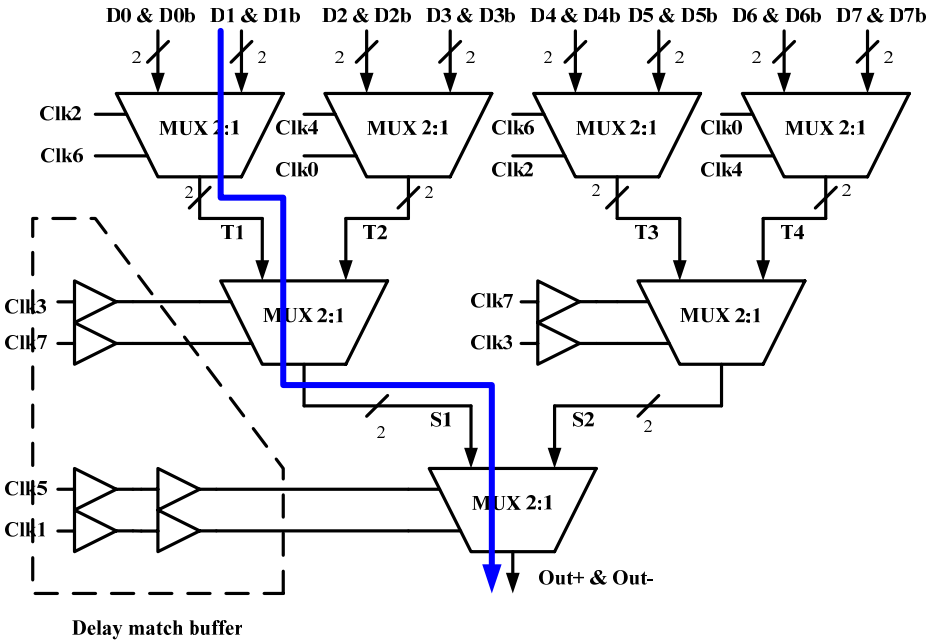


Figure 4-6 Architecture of the 3-levels multiplexer[29]

In the issue of transmitter, there are a lot of types multiplexer to serialize the input parallel data. In the conventional MUX design, a multi-phase type MUX is usually used and shown as **Fig 4-5**. This circuit uses low frequency clock with different-phases, so the power consumption is low. But there is a fatal drawback that the fan-in at the point A and B is high while there are many multiplexer inputs. The high fan-in causes the large parasitic capacitance and the large parasitic capacitance will limit the maximum operating speed. The speed limitation is not only an inherent property of the process technology but also of the circuit topology[28]. Therefore a proposed circuit, 3-levels MUX is introduced in this section to overcome the speed limitation problem.

Fig 4-6 shows the architecture of the 3-levels 8 to 1 MUX which is built with seven 2 to 1 MUX and some delay match butters. From the result of the **Table 4-1**, the input data signals and control clock signals are distributed in the design to achieve this algorithm. The 2:1 MUX cell is shown in **Fig 4-7** and the output capacitance is small, so it can operate at higher speed. The 3-levels MUX is more suitable for high-speed operations with low power consumption than the conventional one. However, the delay match buffer is needed that the clock timing can match the data timing while the data passed through a MUX with a certain delay. The delay match buffer is shown in **Fig 4-8** and the construction is the same to 2:1 MUX, so the circuit delay of these two circuits is almost the same.

This circuit, however, has some flaws. First, it converts serial data only into 2 bit parallel, which makes it unsuitable for some communication system such as 10-channel MUX needed in fiber channel designs. Second, it requires the distribution of precisely delay adjust for different phase clock signals to its respective 2:1 MUX.

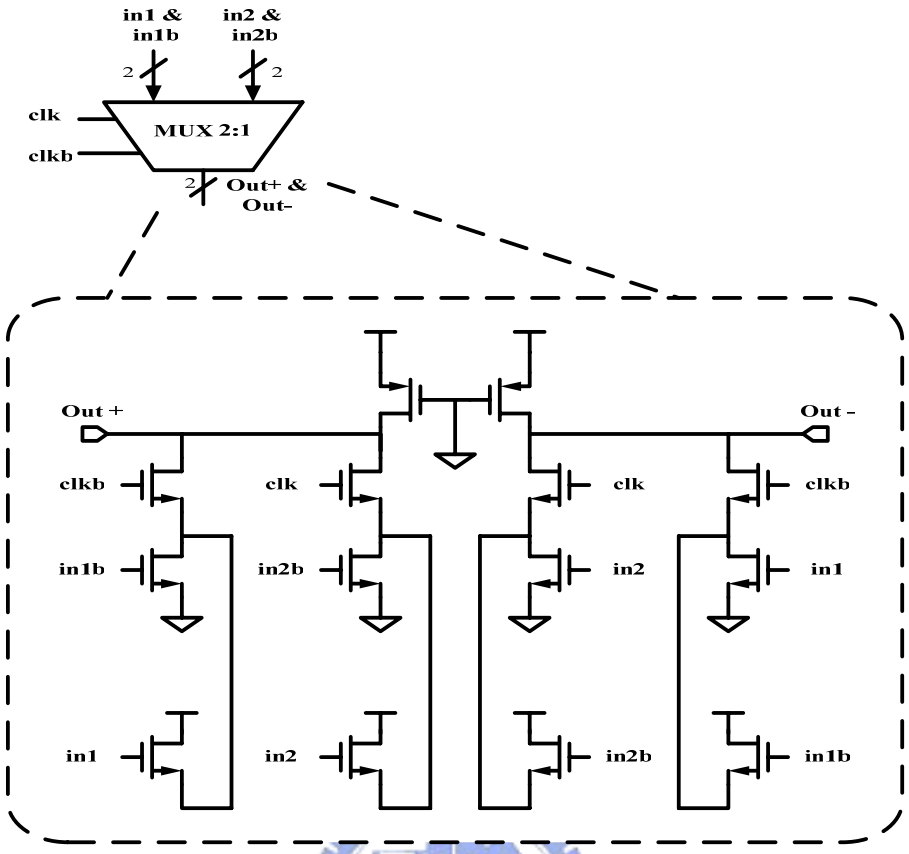


Figure 4-7 Scheme of 2:1MUX Cell

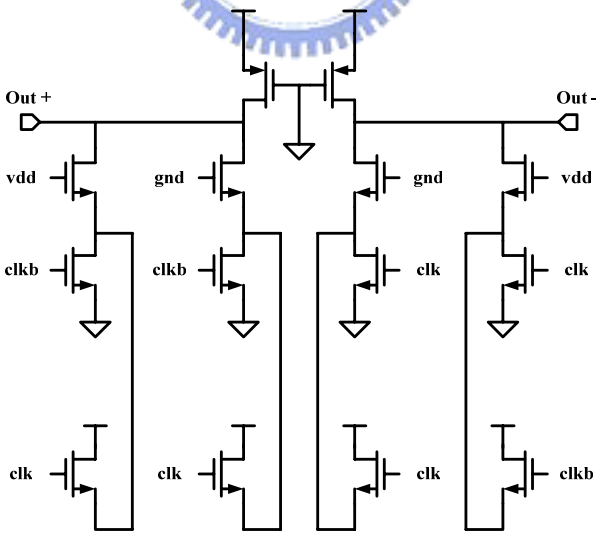


Figure 4-8 Delay Match Buffer

4.3.3 The 8:1MUX with pre-skew circuit

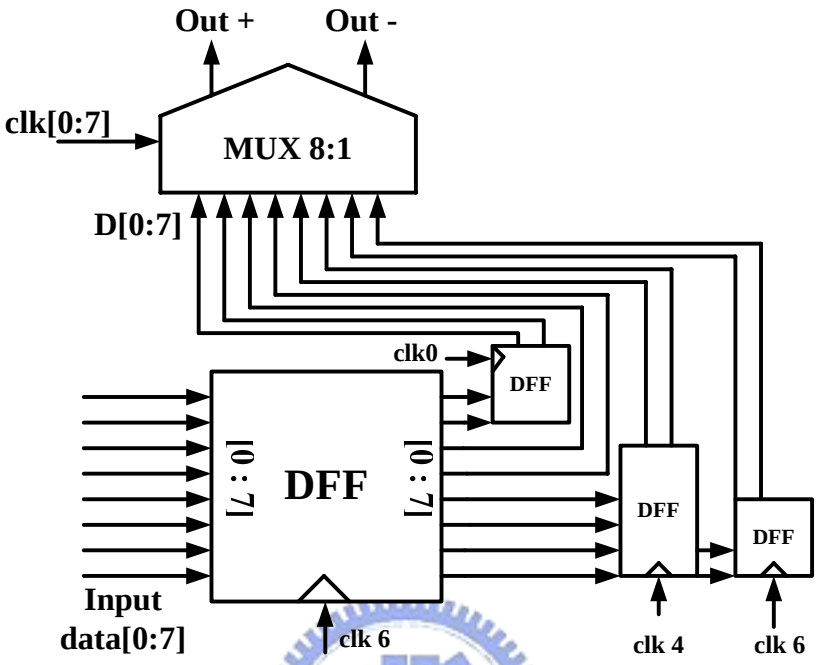


Figure 4-9 Pre-skew Circuit

The purpose of the pre-skew circuit is to make sure that each MUX of first level can select input data at the stable and correct state. If the transient edges of clock and input data rise at approximately the same time, the selected data is confused and costs some time to be stable. Thus, the output data jitter of the transmitter will increase. In order to achieve the target, some input data is needed to be shifted before given into the 3-level MUX. **Fig 4-9** shows the block diagram and design blueprint of the Pre-skew circuit. According to **Fig 4-6** and **Fig 4-9**,the following **Table 4-2 4-3 4-4** demonstrate that how the 3-level MUX serializes the shifted data and those tables are a flow diagram from level 1 to level 3. The number is the brackets of each data flow means the data generation timing. Finally, at the end of the 3-levels MUX , the 8 parallel to 1 serial data is produced.

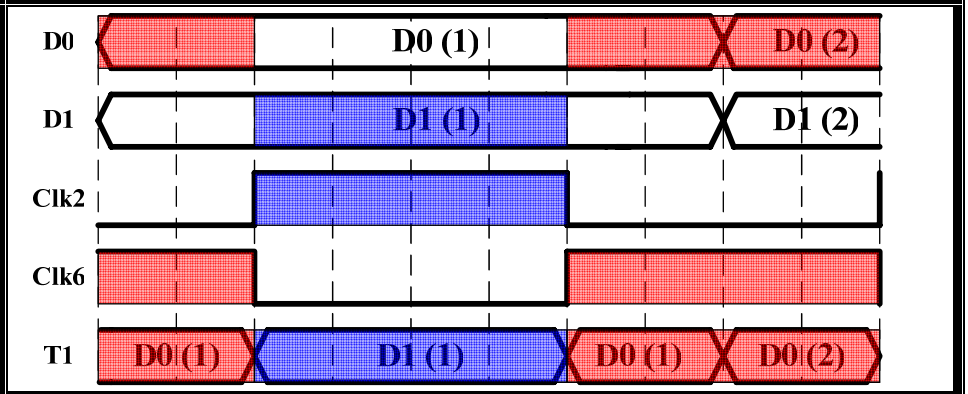
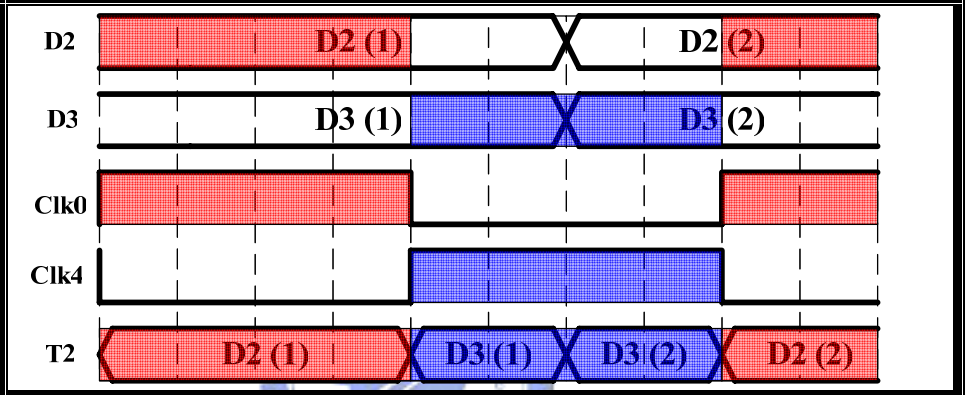
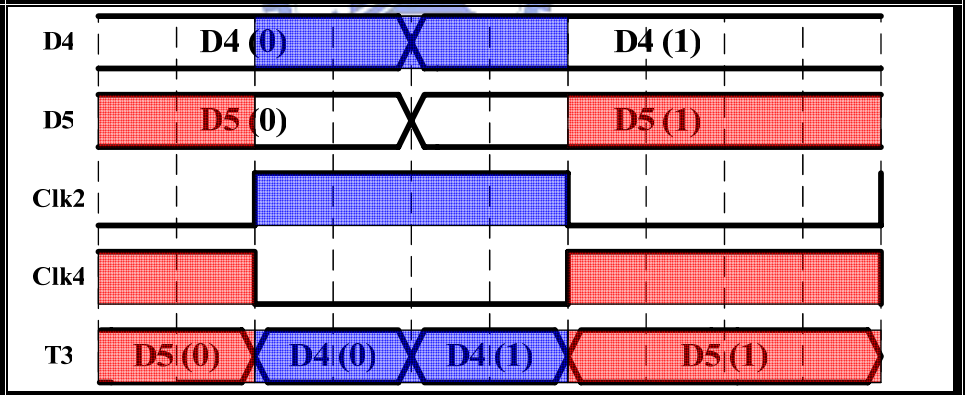
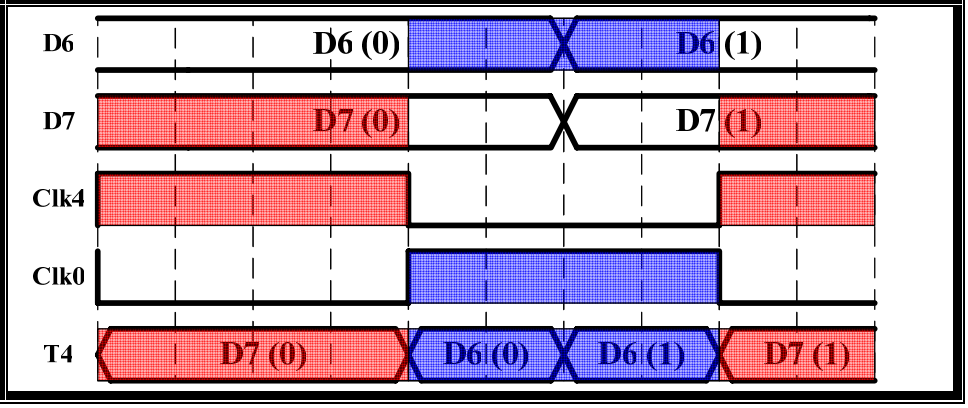
	Level 1
MUX 1	
MUX 2	
MUX 3	
MUX 4	

Table 4-2 Algorithm Result of the First Level

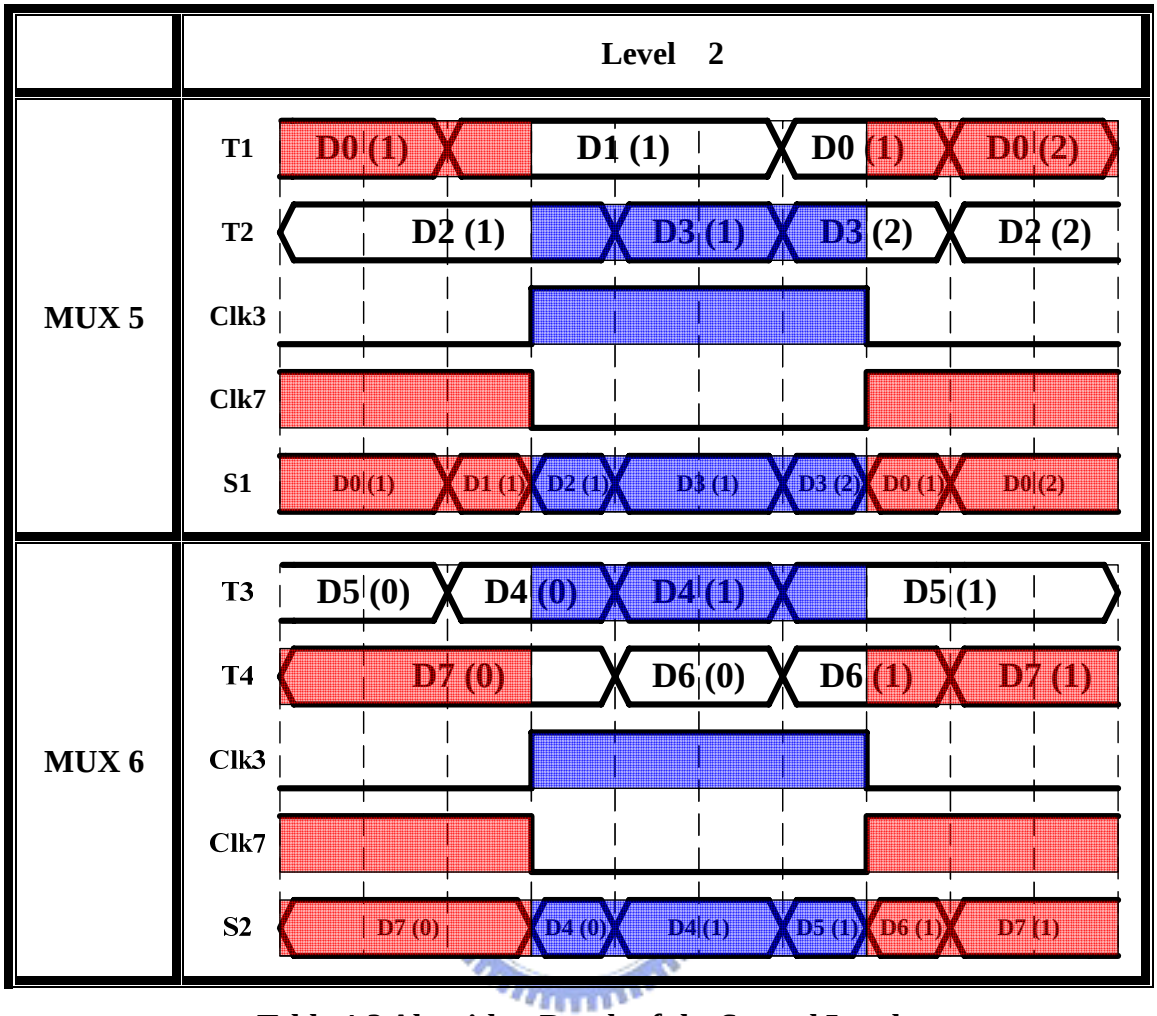


Table 4-3 Algorithm Result of the Second Level

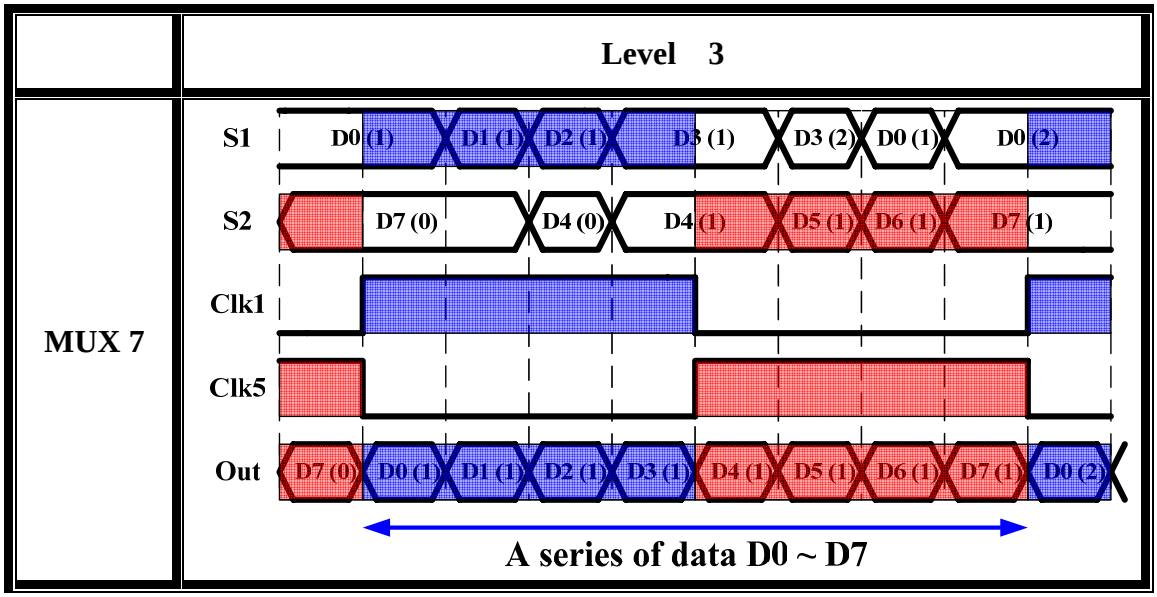


Table 4-3 Algorithm Result of the Third Level

4.4 Data driver

The simplified RSDS link diver consist of a current source which drives the differential pair line. Due to the high DC input impedance of the basic receiver, the majority of driver current flows across the termination resistor and generates a signal with about 200mV swing. When the drivers switches, it changes the direction of the current flowing across the resistor. Thereby, a valid “one” or “zero” logic state can be defined. An additional load resistor at the receiver end provides current-to-voltage conversion and optimum line matching at the same time. However, an additional resistor is usually placed at the source end to suppress reflected waves caused by crosstalk. The configuration of the data driver is shown in **Fig 4-10(a)**. A feedback loop across a replica of the transmitter circuit may be used to define the correct output level. But in this case, we should carefully ponder on the effect of component mismatches between the transmitters and the replica.

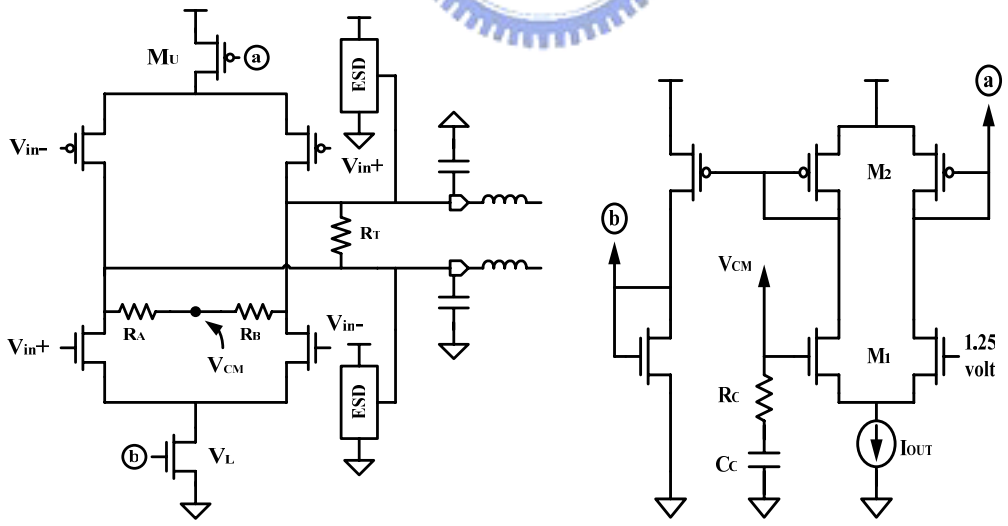


Figure 4-10 (a) RSDS transmitter data driver(b) Common mode feedback circuit

A simple low-power common-mode feedback circuit as shown in **Fig 4-10(b)** is

used to achieve higher precision and low circuit complexity. The common-mode feedback circuit provides a 1.25V as a reference voltage for the data driver. The fraction of the tail current I_{out} flowing across M1 and M2 is mirrored to M_U and M_L. with M_A and M_D switched on, the polarity of the output current is positive toghter with differential output voltage. On the contrast, with M_B and M_C switches on, the polarity of the output current and voltage is reversed. Thus, the logic state of the output voltage can be defined.

4.5 Simulation Result of Transmitter

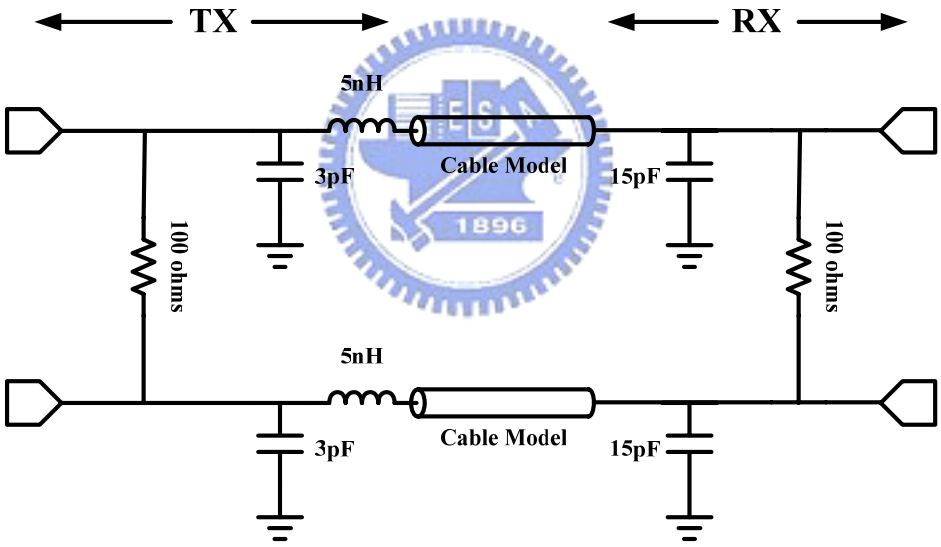


Figure 4-11 Simulation Environment

In real IC, the die is packaged by wire bonding so that the influences should be taken into consideration. During simulation, the package effects are added at Vdd, Gnd and I/O node. Besides, the output loading of the data driver through the cable also should be considered. The simulation environment is implemented as shown in **Fig 4-11**. In the following sections, the simulation results are respectively

demonstrated.

4.5.1 Simulation Result of PLL

Fig 4-12 shows the result of the eight-phase clock signal with 150MHz frequency of the PLL introduced in this chapter. **Fig 4-13** shows the eye-diagram of the clock generated by the PLL. And the jitter is about 26ps.

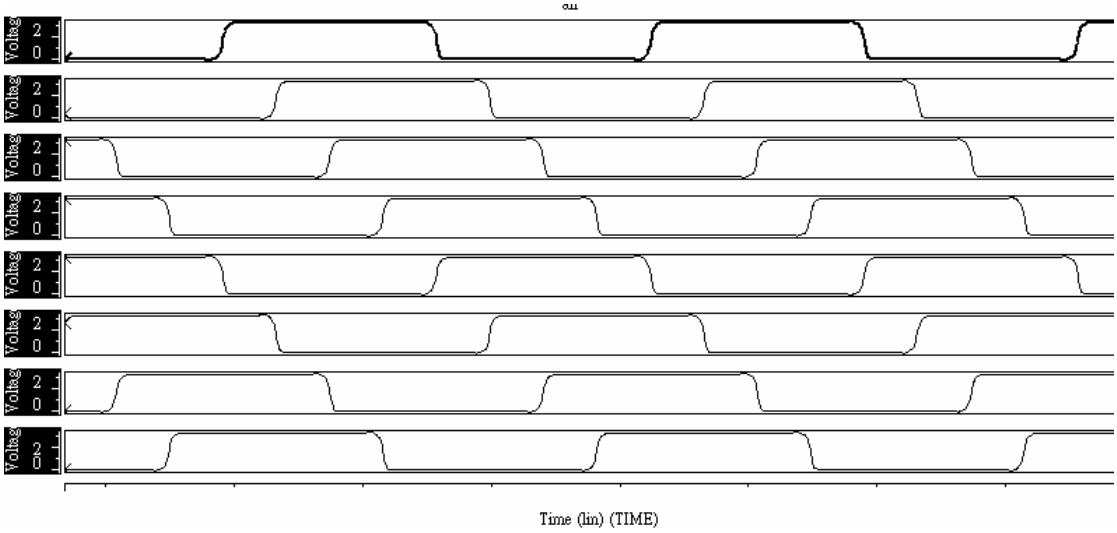


Figure 4-12 Eight-phase VCO clock

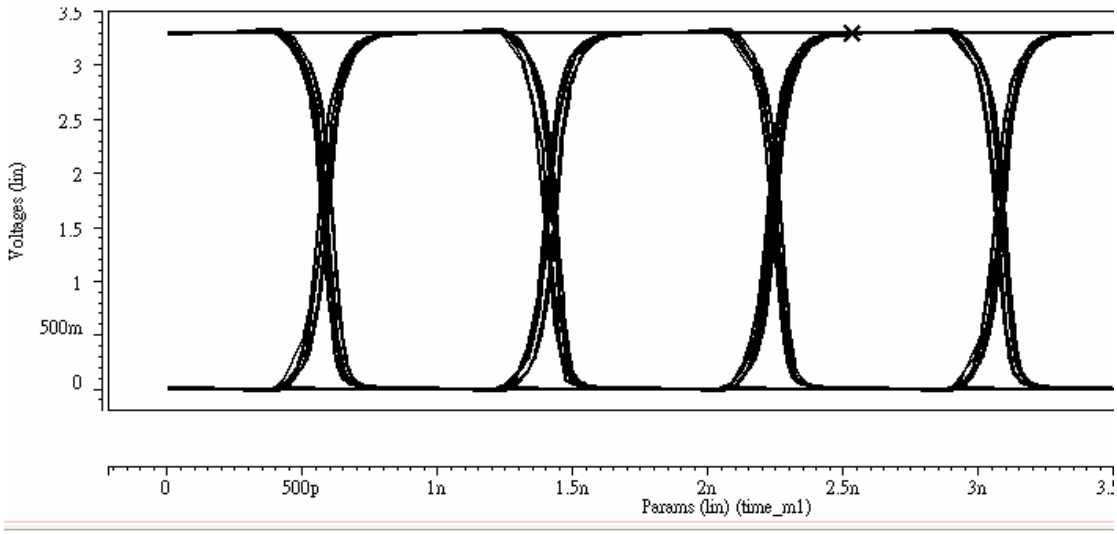


Figure 4-13 eye-diagram of VCO clock

4.5.2 Architecture Comparison

To look back the Section 4.3.2 and 4.3.3, the additional circuits “3-levels MUX” and “pre-skew circuit” are introduced. In this section, the simulation results will be shown and compared to proof the preferable property of the additional circuits.

◆ **Multi-phase Type MUX**

With the Multi-phase Type MUX architecture, because of the defect, the high capacitance, the performance of the high-speed data transmission is not very good. The simulation result is show as **Fig 4-14**. The amplitude of the data eye-diagram is about ±179mv and the width of the eye-diagram is about 718ps. If there is no jitter, the width of eye should be 1/1.2G = 883ps. Therefore, the figure shows 833-718=115ps jitter exists in the eye-diagram.

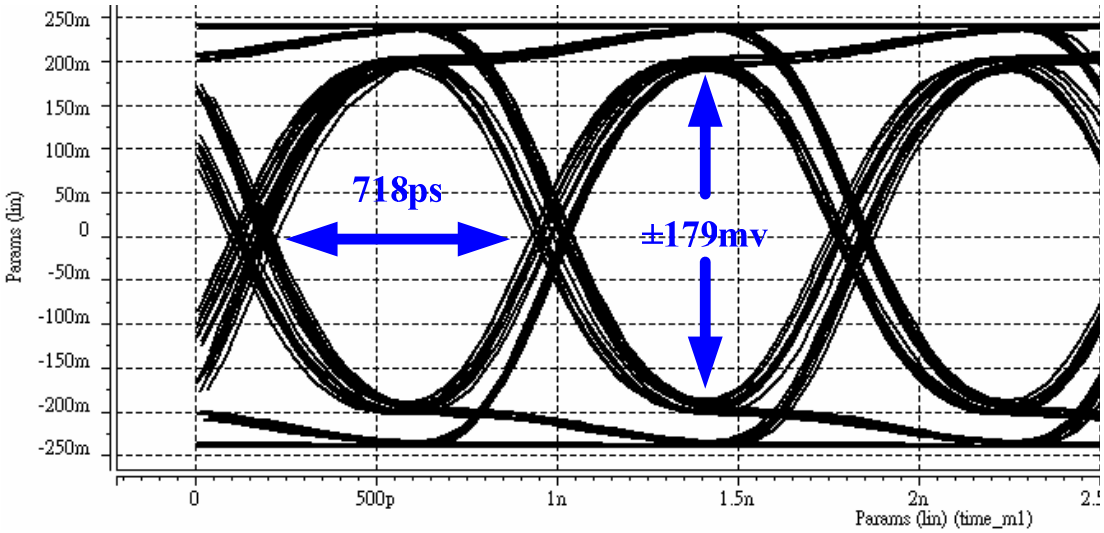


Figure 4-14 eye-diagram of output (Multi-phase Type MUX)

◆ **With 3-levels MUX (no pre-skew circuit)**

Fig 4-15 shows the simulation result with the 3-levels MUX architecture multiplexer. This structure provides a wider bandwidth for high-speed data transmission. The amplitude of the data eye-diagram is about ±187mv and the width of the eye-diagram is about 762ps with 71ps jitter. Both jitter and signal amplitude are improved. The jitter is reduced from 115ps to 71ps.

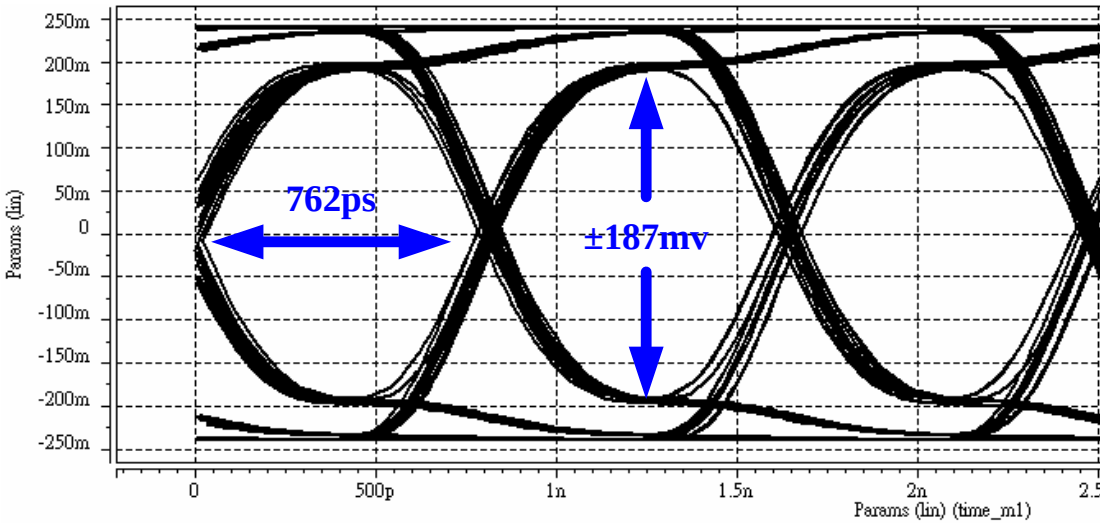


Figure 4-15 eye-diagram of output (3-levels MUX without pre-skew)

◆ **With 3-levels MUX and pre-skew circuit**

With the pre-skew circuit, the condition that the clock edge falls on the data transient state can be prevented. This makes the eye-diagram more open. The simulation result is shown in **Fig 4-16**. The amplitude of the data eye-diagram is increased to about ±200mv and the width of the eye-diagram is about 769ps with 64ps jitter. **Fig 4-17** shows the differential output data stream of the transmitter. The

sequential logic levels are labeled on the figure.

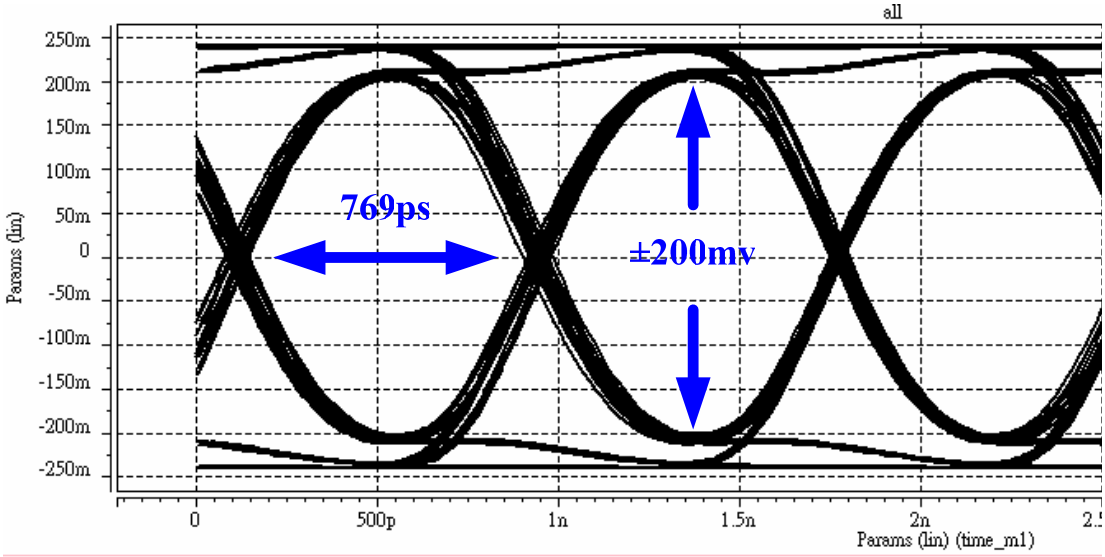


Figure 4-16 eye-diagram of output (3-levels MUX with pre-skew)

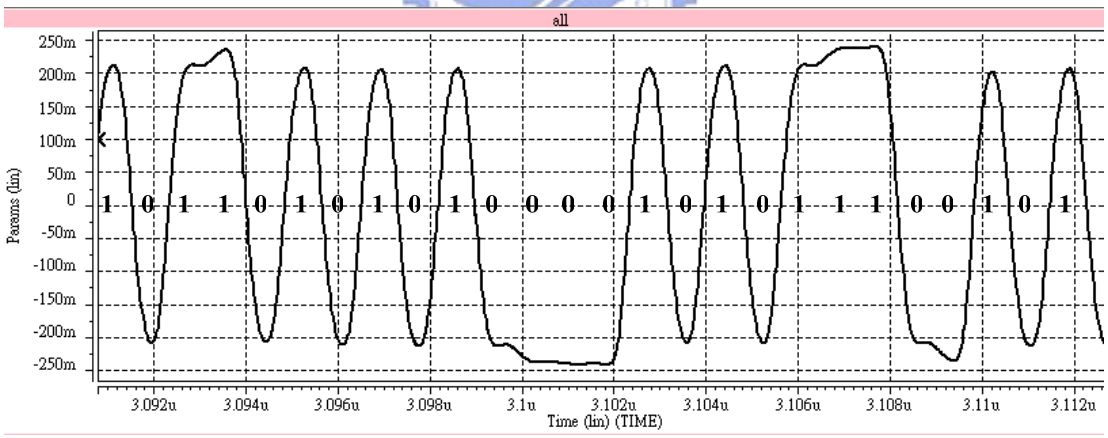


Figure 4-17 output waveform of TX

4.5.3 Layout of transmitter

Fig 4-18 shows the layout of the transmitter and each component is labeled. The post simulation result is shown in **Fig4-19**. The amplitude of the data eye-diagram is increased to about ±175mv and the width of the eye-diagram is about 730ps with

103ps jitter

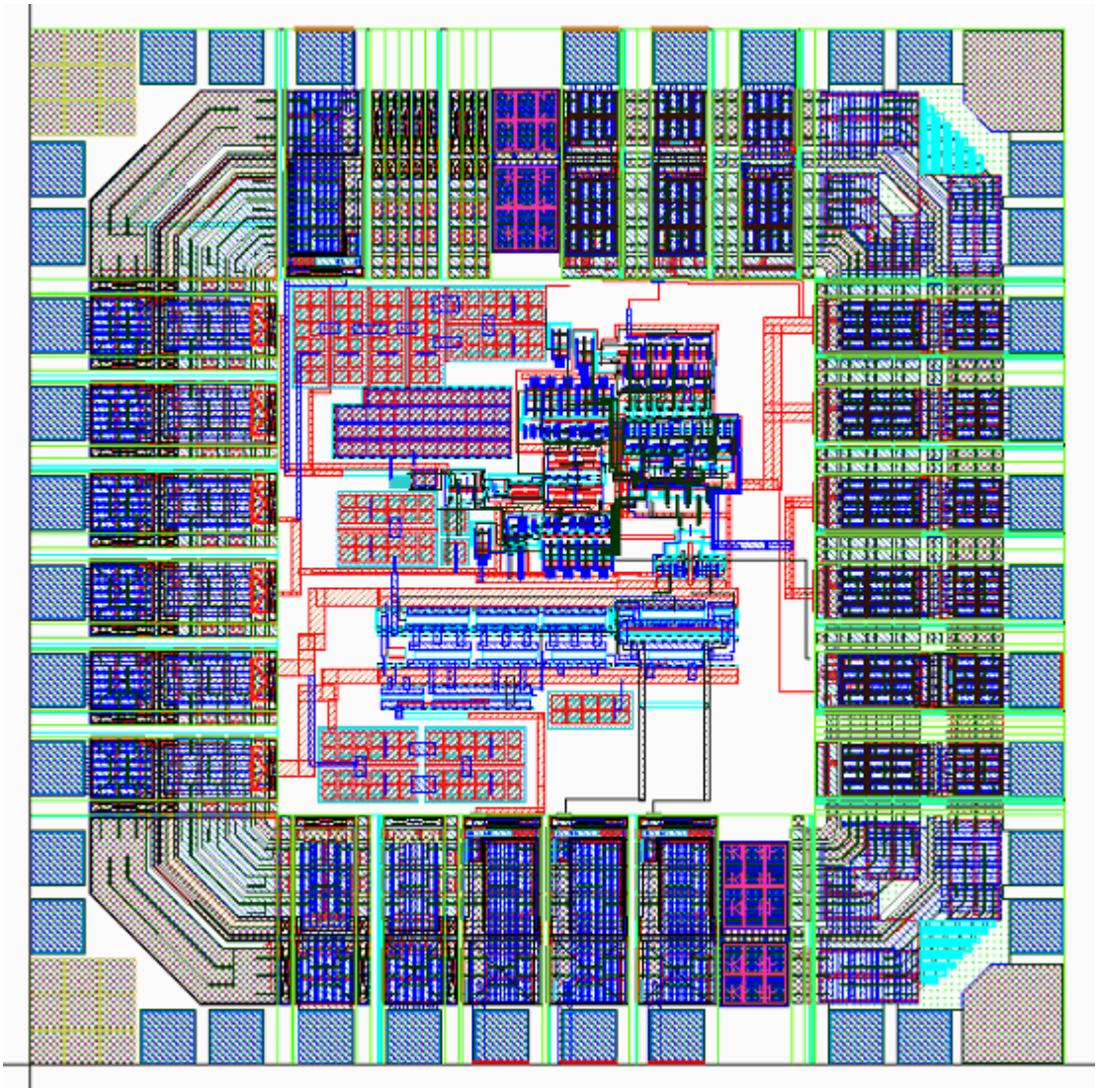


Figure 4-18 Layout of transmitter

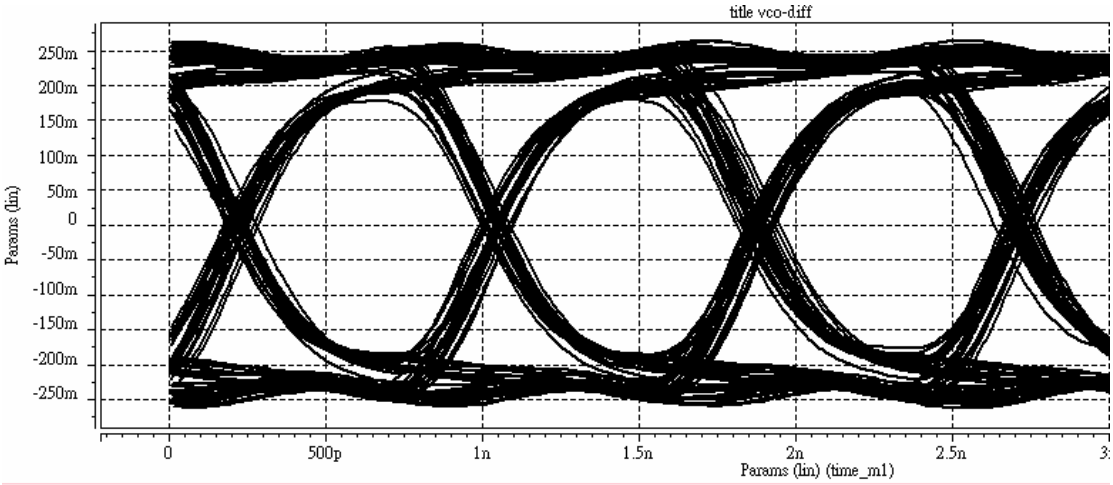


Figure 4-19 post simulation of transmitter

Chapter 5

Receiver

5.1 Architecture of Receiver

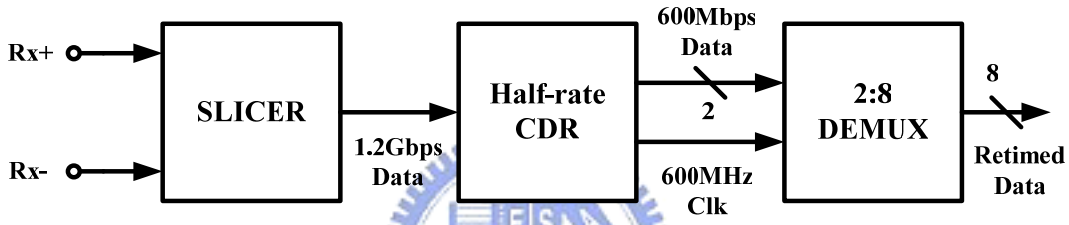


Figure 5-1 Block diagram of the receiver

This chapter introduces the architecture of the receiver design and the principle of the clock and data recovering circuit. The differential transmitted data signal is amplified to digital signals by the Slicer circuit. The purpose of the clock and data recovery circuit is to generate the receiver sampling clock based on the input data and adjust the sampling point on the center of the data eye. Then the de-multiplexer circuit makes the input serial data restoring to the eight-phase parallel data.

5.2 Slicer

When the differential data enter the receiver chip, due to the inductance and capacitance resonance caused by bonding wire and pad, data will be distorted. The

slicer circuit is used to recovery several hundred mV input signal to full swing. **Fig5-2** shows the circuit diagram of the slicer[30]. This circuit plays a key role to sense received signal in the receiver. It is actually an open-loop comparator. To meet the common mode voltage range, the circuit is implemented with PMOS input differential pair with a constant current source and NMOS crossed-coupled pairs are used as the load.

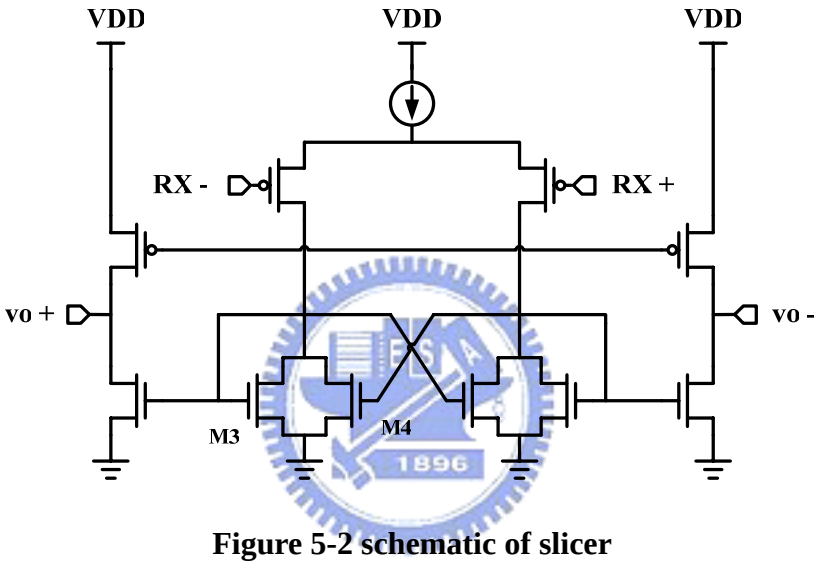


Figure 5-2 schematic of slicer

Because slicer needs to detect the received data which were noisy and swing limited and amplify the signal to get the full swing level. Therefore, the gain and bandwidth of the slicer should be designed carefully to achieve the requirement. Moreover, the important characteristic, offset voltage which affects the accuracy of receiver should be noticed. The offset voltage is not only due to the mismatches in the input devices but also mismatches (both device and capacitance mismatch) within the positive-feedback structure.

The advantage of this hysteresis comparator is noise immunity and noise is cut off by the threshold voltage as **Fig 5-3**. If the size ratio A= $(W/L)_4/(W/L)_3$ and

bias current through M1 is I_B, the threshold voltage is derived as

$$\pm Vth = \pm\sqrt{\frac{I_B}{K}}\frac{\left(\sqrt{A}-1\right)}{\sqrt{1+A}} \tag{5-1}$$

The threshold voltage depends on not only the bias current but also the size ratio of the lower two current mirrors. If A<1, there is no hysteresis in transfer function, when A>1, hysteresis will result as **Fig 5-3**. **Fig 5-4** shows the frequency response of the slicer.

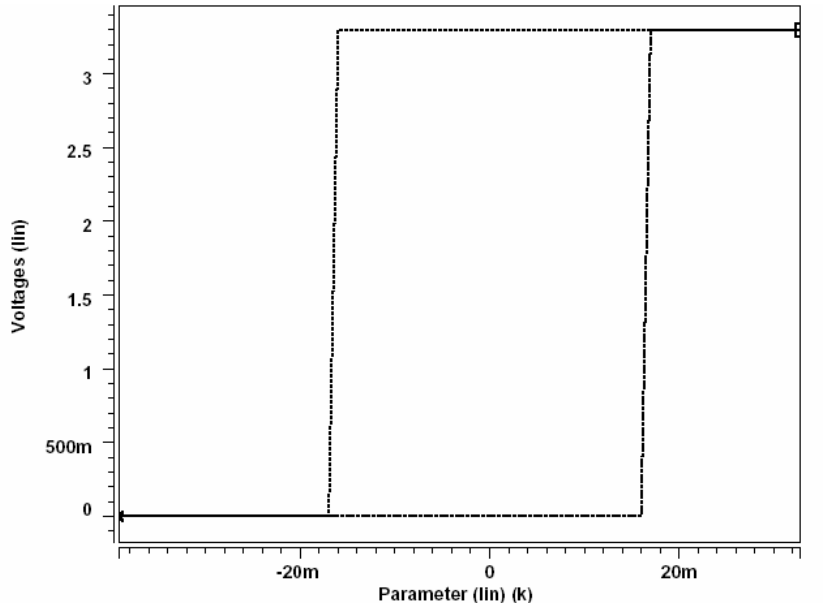


Figure 5-3 Simulation of Hysteresis comparator

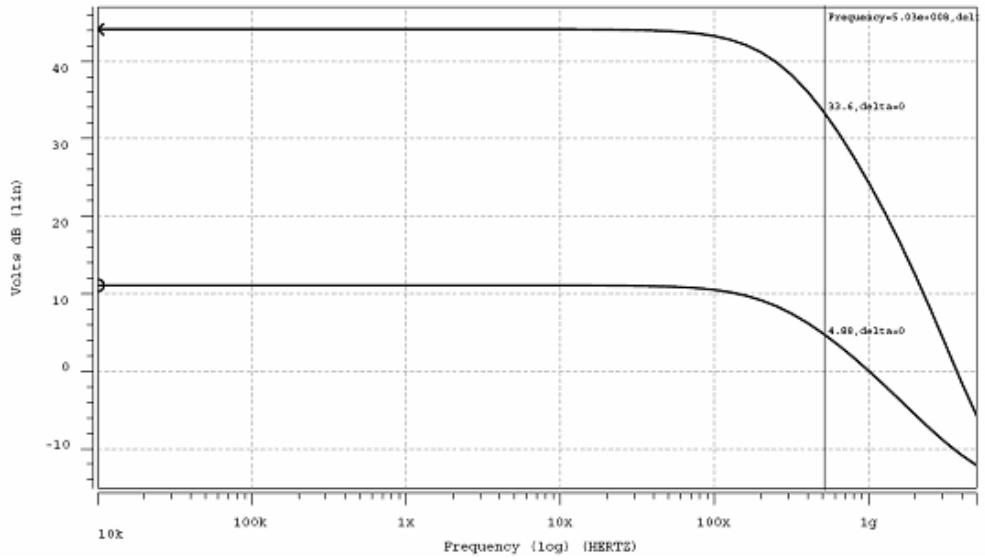


Figure 5-4 Frequency response of slicer

5.3 Clock and Data Recovery

5.3.1 Introduction

The data stream received and amplified by the slicer is asynchronous. the data jitter during transmission exists and an adjustable global clock is necessary to tune the timing based on the data. The clock is extracted from the random data so as to allow synchronous operation. The task of global clock generation is done by the clock and data recovery (CDR) circuit. Reviewing the issue introduced in Chapter2, the architecture is the PLL-based type CDR. The main idea of a PLL-based CDR is the detection of the data location with respect to the clock edge while the data entering receiver. If the data leads the clock, the UP signal will be generated to speed up the clock. In contrast, if data lags the clock, the Down generated makes the clock slow down. Finally, the clock edge will be located at the center of each bit by this feedback system.

5.3.2 Architecture of CDR

Fig 5-5 shows the CDR architecture used in this thesis, this is a half-rate dual-tracking loop design with improved jitter performance. Due to the temperature and process variations, the frequency drift in VCO exists. There are two circuits, FD (frequency detector) and PD (phase detector) to adjust the output frequency in VCO. The frequency detector detects the frequency difference to drive the charge pump to adjust the control voltage and then VCO frequency can be close to half of the data rate. Then, the half-rate phase detector produces error signal proportional to the phase

difference between the 600 MHz VCO clock and 1.2Gbps data stream. Moreover, when the half-rate phase detector executes the adjusting operation, it generates the two 600Mbps data sequence for the de-multiplexer. This will be discussed in the following section.

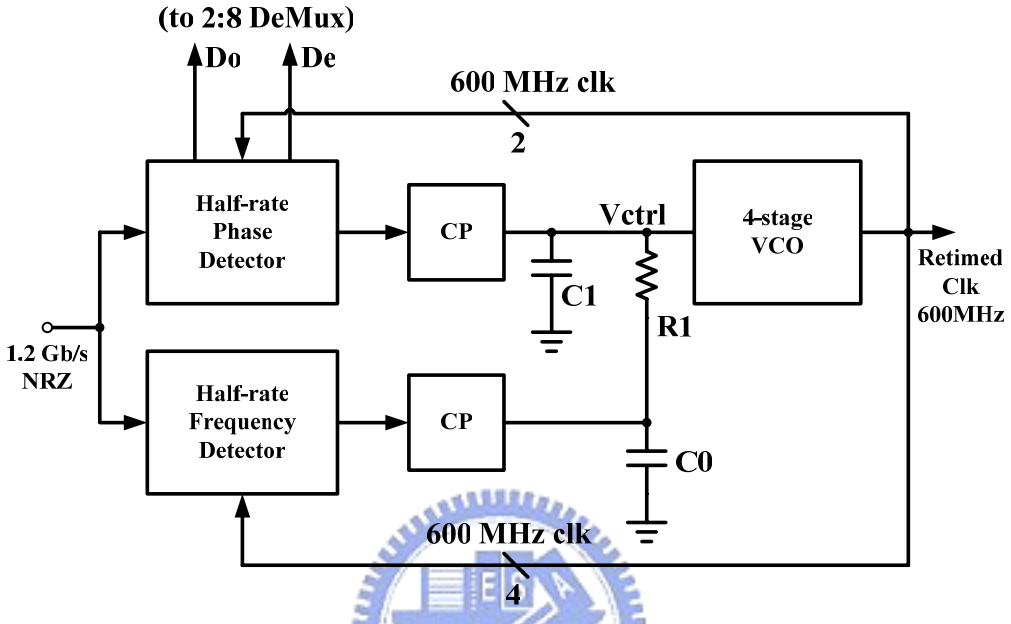


Figure 5-5 Half-rate CDR architecture

5.3.3 Half-rate Phase Detector

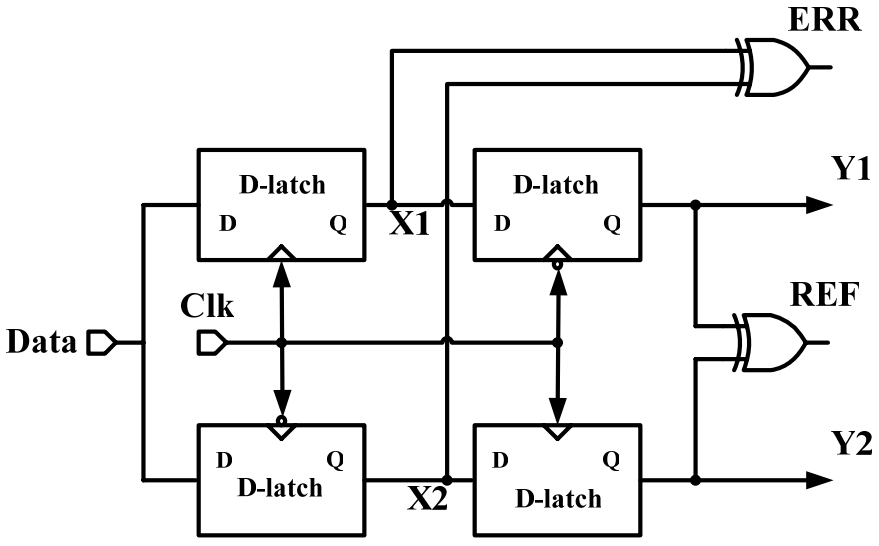


Figure 5-6 Half-rate phase detector

The half-rate phase detector is shown in the **Fig 5-6**[31]. Comparing to the phase detector used in the traditional PLL, it is more difficult to achieve the synchronous operation and requires more accuracy. Because the detecting signal in the half-rate phase detector is non-periodic random data, not like the periodic certain clock detected in traditional PLL. As a result, phase detectors used in CDR should exhibit several properties. First, due to its random nature, the data may exhibit long sequences of consecutive ONEs and ZEROs which might introduce the drift in oscillator. Hence, in the absence of data transitions in the input bit stream, the phase detector must not produce any false phase comparisons in order to tolerate consecutive ONEs of ZEROs. Second, because the comparison is operated at high speed rate, the symmetry of the rise time and fall time for each cell in the detector is significant. Whit the good symmetry, the sensitive circuit can produce the precise signal. Therefore, the size tuning is necessary to be considered carefully.

Furthermore, there are some useful advantages of the half-rate phase detector. First, because the detector can sense the input random data at full rate with only half of the data rate, the operation speed of other circuit (such as PLL) can be slowed down so that the total power dissipation can be reduced. Second, the low clock frequency requirement makes the PLL more easily designed.

Fig 5-7 is the timing scheme for the detector receiving an arbitrary data signal while the clock properly located at the center of the data bit interval. The two XOR gate generates the ERR and REF pulses only while the input data has transition. As shown in the **Fig 5-7**, the width of the REF is twice than the ERR. This means that the current in charge pump caused by the ERR must be scaled up by a factor of two with respect to the current caused by REF so that when the clock edge locates in the middle of the eye, the total current is zero. The Y1 and Y2 sequence are the de-multiplexed input signals extracted from the original input sequence.

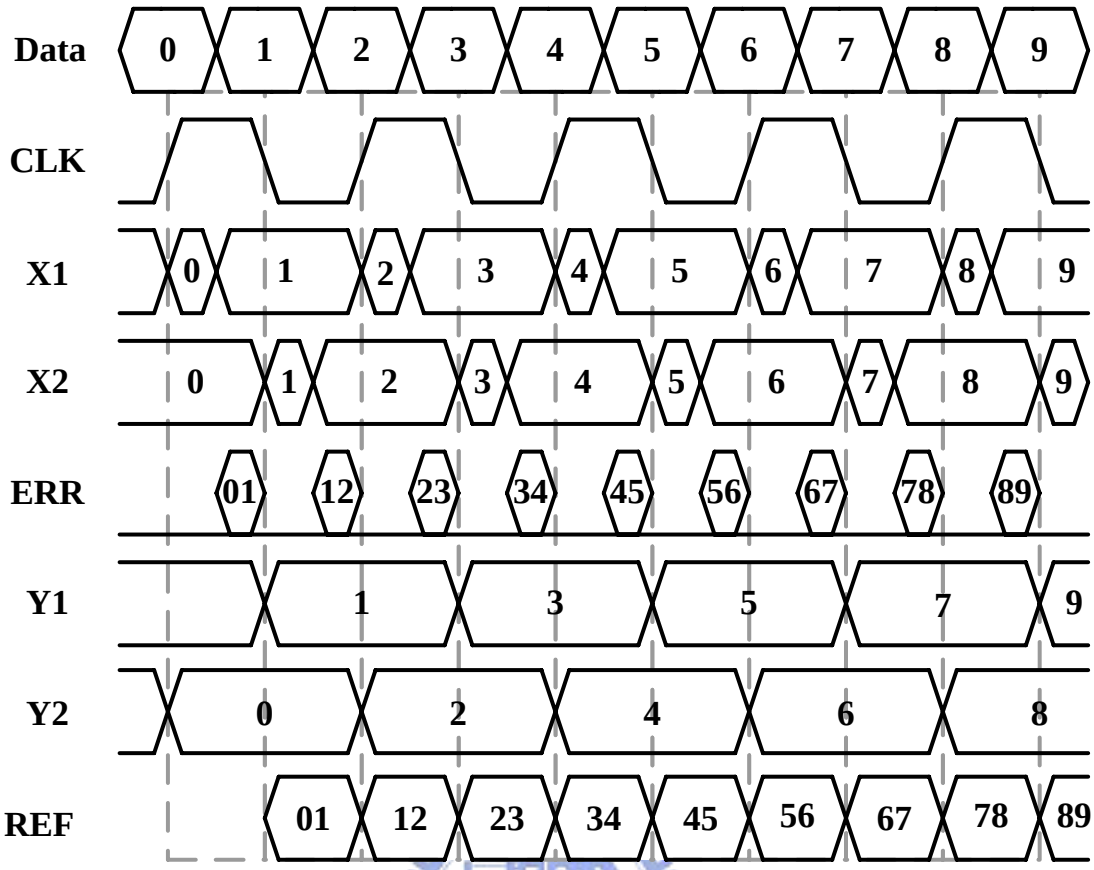


Figure 5-7 Timing scheme of the half-rate phase detector operation

Then, the REF and ERR signals are applied to the charge pump circuit similar to the circuit used in Section 3.3.2. In order to make the total current of charge pump zero when there is no phase difference between the clock and the data, the size of ERR part circuit should be scaled by a factor of two with respect to the size of REF part circuit and the discharge current and charge current will be the same.

The **Fig 5-8** shows the perfect locked condition. However, it is hard to design a circuit that can achieve this task so precisely. Shown in the **Fig 5-9**, is the simulation result of the relationship between phase difference and chare pump current. After a series of simulations and taking down the result point, we can find that when the phase difference is 430ps, the total current is zero. This indicates that the systematic offset between the data and the clock is very small.

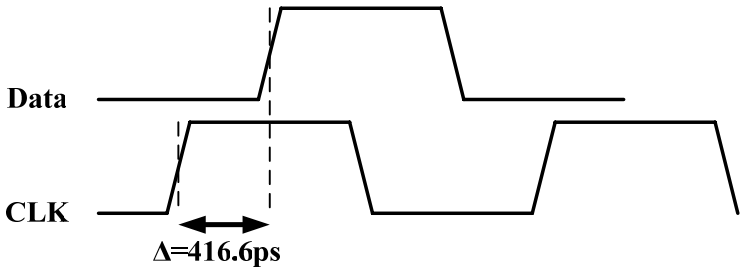


Figure 5-8 Perfect locked condition

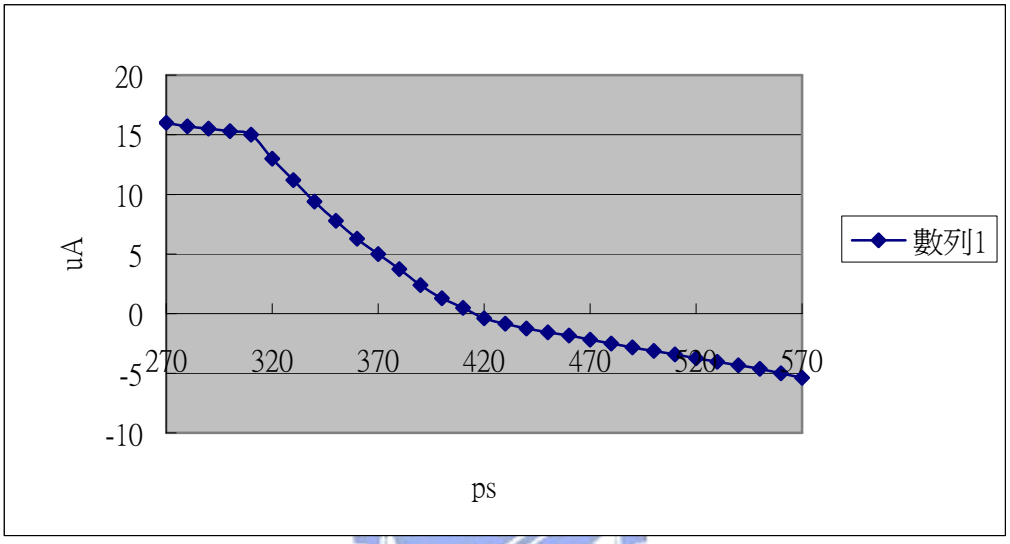


Figure 5-9 Transfer characteristic of phase detector

5.3.4 Half-rate Frequency Detector

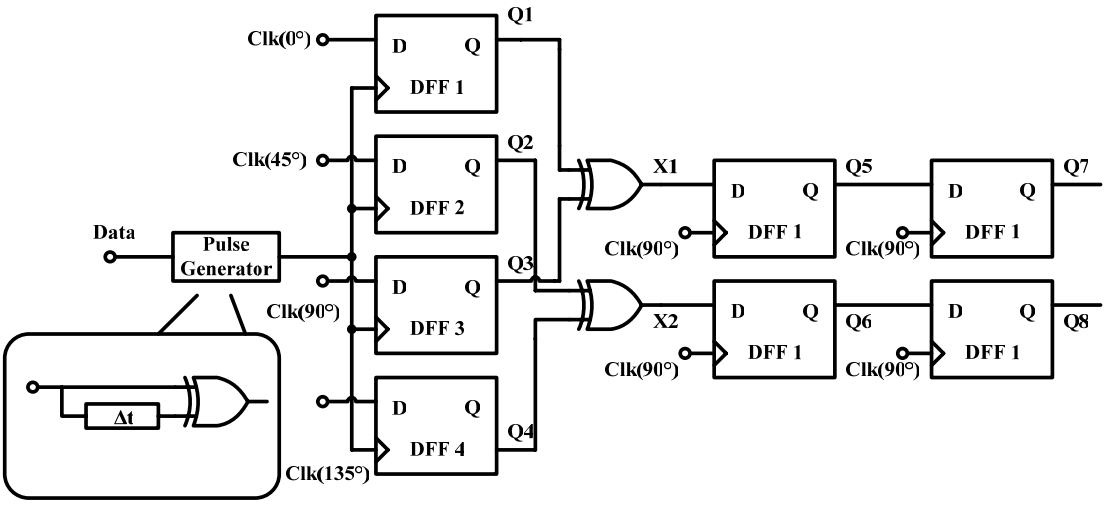
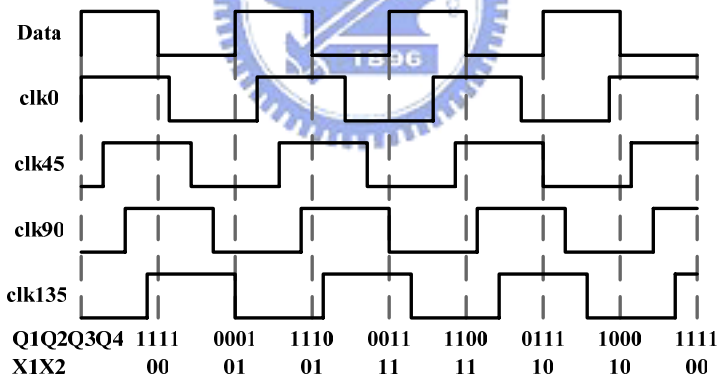


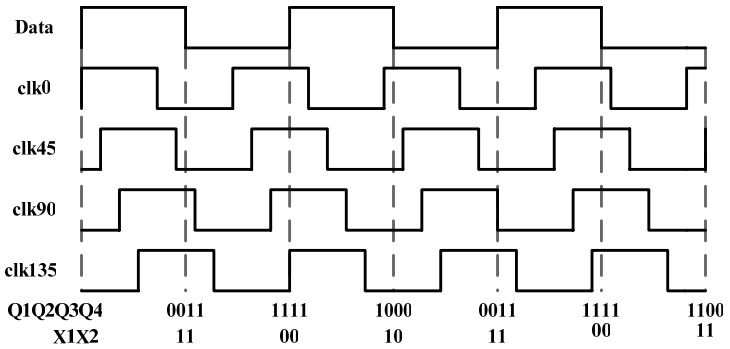
Figure 5-10 Half-rate frequency detector[32][33][34]

The block diagram of half-rate frequency detector is shown in **Fig 5-10**. It is constructed by the D flip-flop and XOR gate. The input data passes through the pulse generator and the generator produces a clock-pulse with the signal edge same to the input data. At every transition of the input data, the multiple clock phases with 45° disparty, clk0, clk45, clk90 and clk135 are sampled by the clock-pulse. The D flip- flops act as the register which save the X1, X2 generated at different time.

There are two sample of timing diagram for a period of data signal with the 4-phases clock in **Fig 5-11**. The nodes X1 and X2 are needed to define four quadrants of phase (0,0), then (0,1), then (1,1), then (1,0). When there is a frequency difference between input signal and clock data output, the sampled quadrant will rotate around the circular phase diagram as shown in **Fig 5-12**. The direction of the rotation is depended on whether half of the input signal frequency is faster or slower than the clock frequency.



Fcvo > 1/2 data rate



Fcvo > 1/2 data rate

Figure 5-11 timing diagram of FD

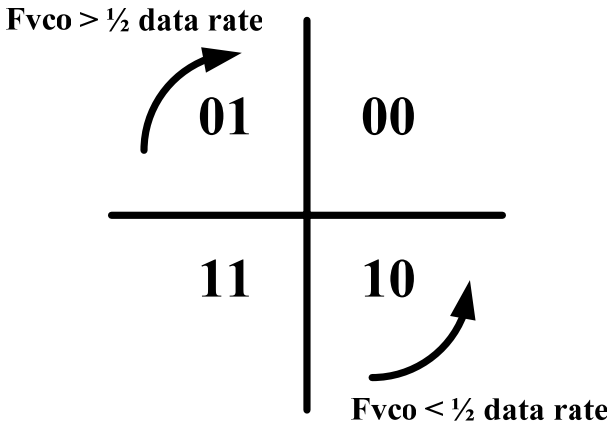


Figure 5-12 Circular phase diagram

It can be seen from **Fig 5-12**, when the clock frequency is lower than half of the input signal frequency, the sampled quadrant rotates counterclockwise and vice versa. The direction of rotation can be detected by monitoring the two consecutive quadrants like 1,0 and 0,0. If the sampled quadrant moves from the former to later, the clock is found to be slow and an UPp pulse is needed to speed up the clock. On the other hand, a transition from 0,0 to 1,0 quadrant denotes a fast clock and a DOWN pulse should be generated to slow down the frequency of the clock. The UP and DOWN signals can be implemented as Fig. 5-13.

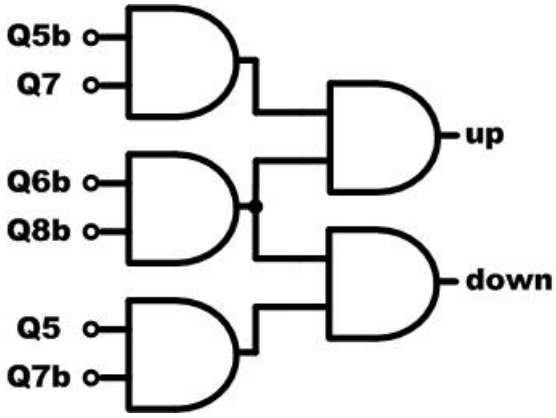


Figure 5-13 Up and down generator

The half-rate frequency detector has two features. First, it will turn off automatically when frequency of the VCO is close to half of the input data rate. When

the frequency detector turns off, the frequency error of the two signals is within a range between ±300ppm. Hence, the frequency detector does not affect the operation of the phase detector and there is no need to switch off the frequency detector in the lock state. It means that low jitter performance can be achieved. Second, the frequency detector has a large capture range for the NRZ input data. It can detect frequency derivation over ±30 percentage of the data rate. Thus, the tuning range of the VCO could be designed larger.

5.4 Linearization Circuit

Because the ring oscillator in receiver must oscillates at the much higher frequency than the one in transmitter, Kvco value in receiver is also higher than Kvco value in transmitter. However, the high value of Kvco is the significant source of jitter. An additional circuit, a linearization circuit is used in this work to suppress the Kvco value.

A linearization circuit is shown in **Fig 5-14**. The input controlled voltage, Vctrl, is not directly applied to the VCO, but is converted to another voltage, Vtun, with a scaling-linear characteristic. The product of this transfer curve with the VCO tuning sensitivity should be as constant as possible to achieve a linear overall tuning. The output voltage, Vtun, changes with the input voltage, Vctrl, which covers the linear gradation characteristic of the VCO. **Fig 5-15** shows the characteristic transfer curve of the linearization circuit[34].

Whit the additional circuit to suppress the sensitivity of the VCO, the transfer curve of VCO becomes gentler and is shown in **Fig 5-16**. The Kvco is 160MHz/V at the 600MHz oscillation frequency.

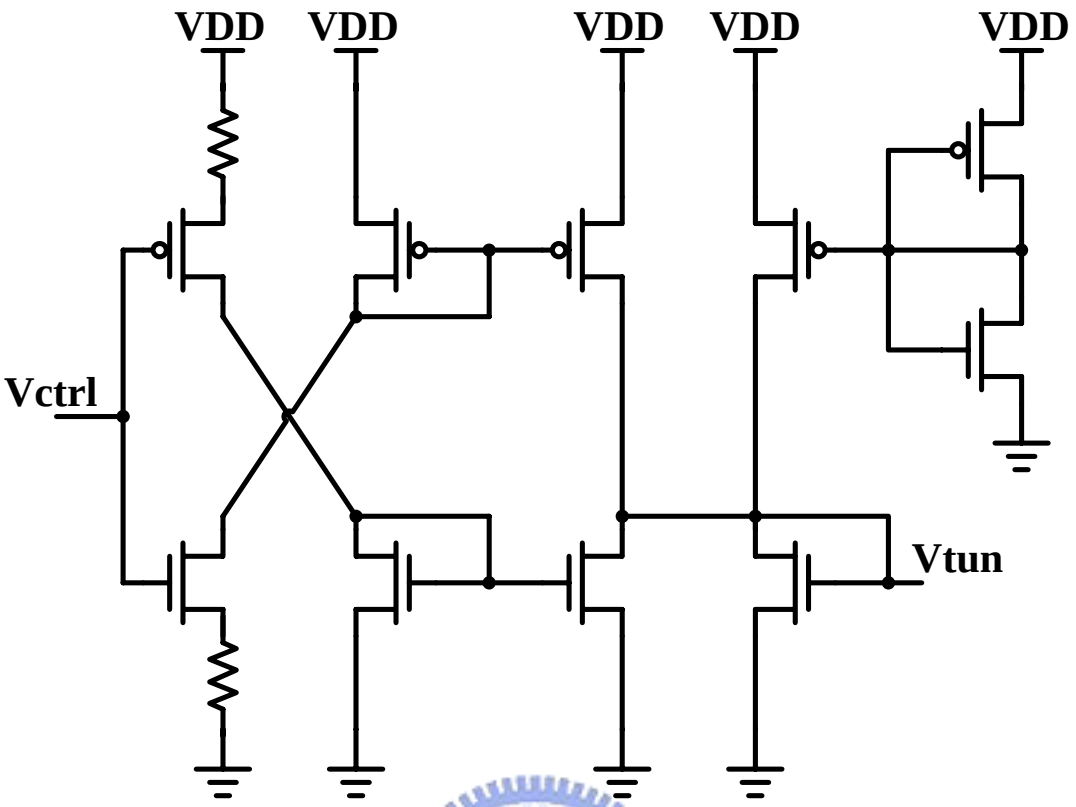


Figure 5-14 Schematic of the linearization circuit

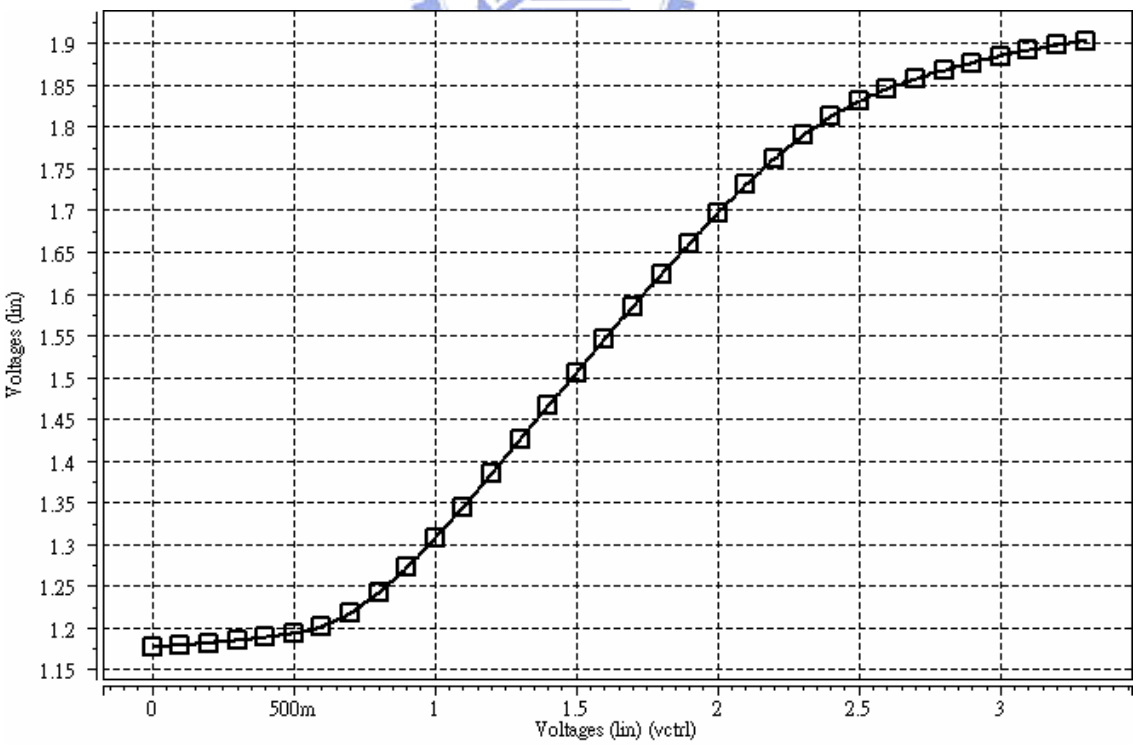


Figure 5-15 Transfer curve of the linearization circuit

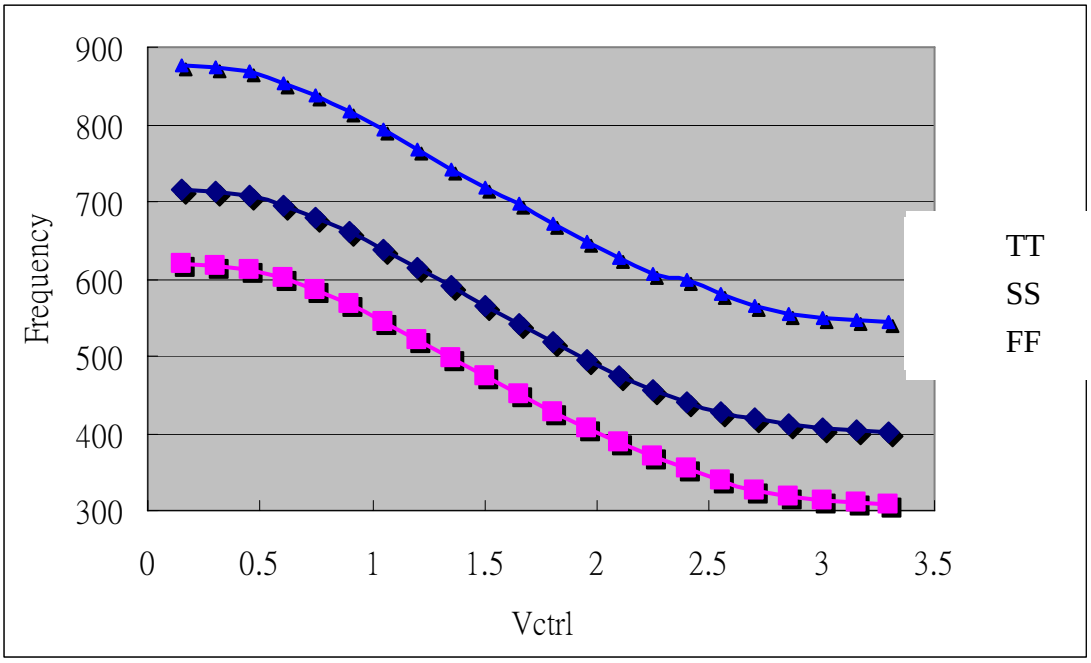


Figure 5-16 Transfer curve of VCO (Kvco=160MHZ/V - TT)

5.5 Parameters of CDR

VCO Frequency	600MHz
PDCP Current	50 μ A
FDCP Current	2mA
VCO gain	160MHz/V
Loop Bandwidth	2.5MHz
Parameter of Loop Filter	C0=178.16pF
	C1=5.717pF
	R1=2.0265k ohm
Phase Margin	70°
Power	164mW

Table 5-1 Parameters of CDR

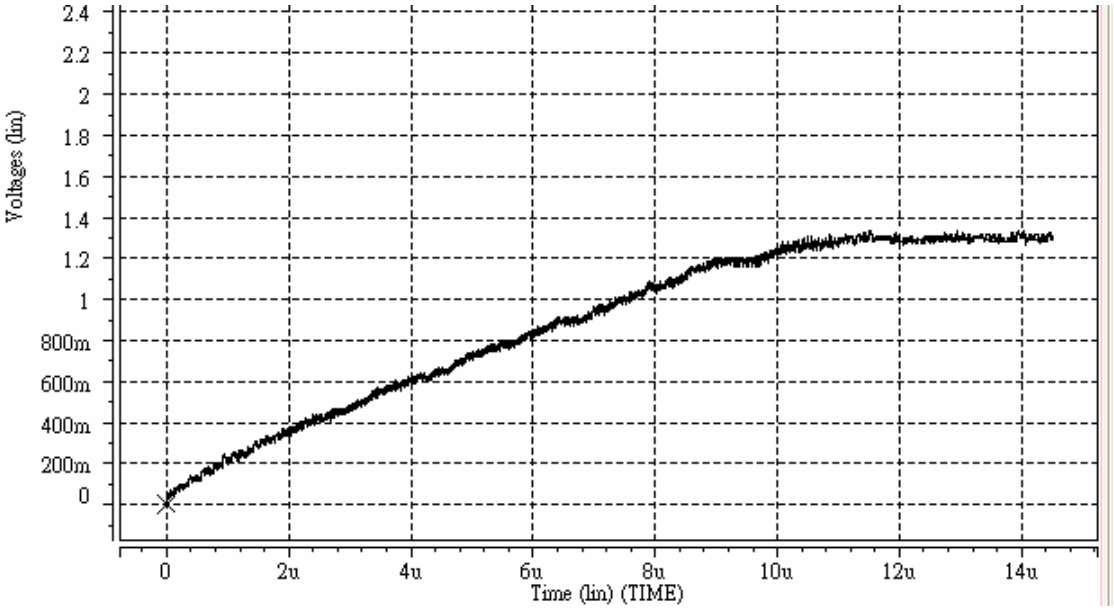


Figure 5-17 Control voltage of VCO

The total parameters of the CDR are listed in the **Table 5-1**. **Fig 5-17** shows the tracing of the control voltage of VCO. It takes about 11us to get to lock statement and the voltage is hold at about1.3V. The locking speed is not quick. In order to increase the locking speed, the larger current is needed. However, the large current will make the system unstable for locking. That is what is needed to improve in this thesis.

5.6 De-Multiplexer

The asynchronous tree-type de-multiplexer architecture can use both rising and falling clock edges to operate. Therefore, a tree-type de-multiplexer is able to operate at half the speed of the data rate. It is more suitable for high-speed work because of its simple construction and low power consumption. The architecture of 2:8 de-multiplexer is shown in the **Fig 5-18**[35].

The architecture of 1:2 DEMUX is shown in **Fig 5-19(a)**, and **Fig 5-19(b)**. The timing diagram indicates that the 1:2 DEMUX module dose not need precisely controlled clock distribution. If the delay for the clock in the circuit is suitable, a little

timing difference of clock distribution is tolerated. The 1:2 DEMUX modules not only generates the de-multiplexed output but also an optimized clock for the next stage. The asynchronous tree-type 2:8 de-multiplexer is obtained simply by connecting such 1:2 DEMUX modules.

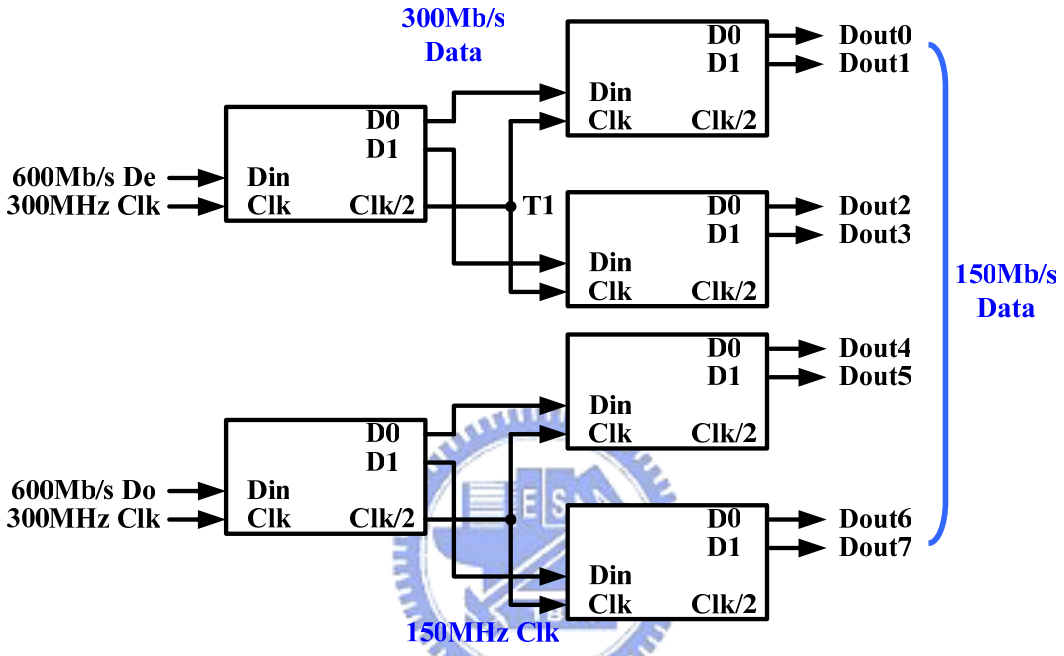


Figure 5-18 Asynchronous tree-type 2:8 de-multiplexer

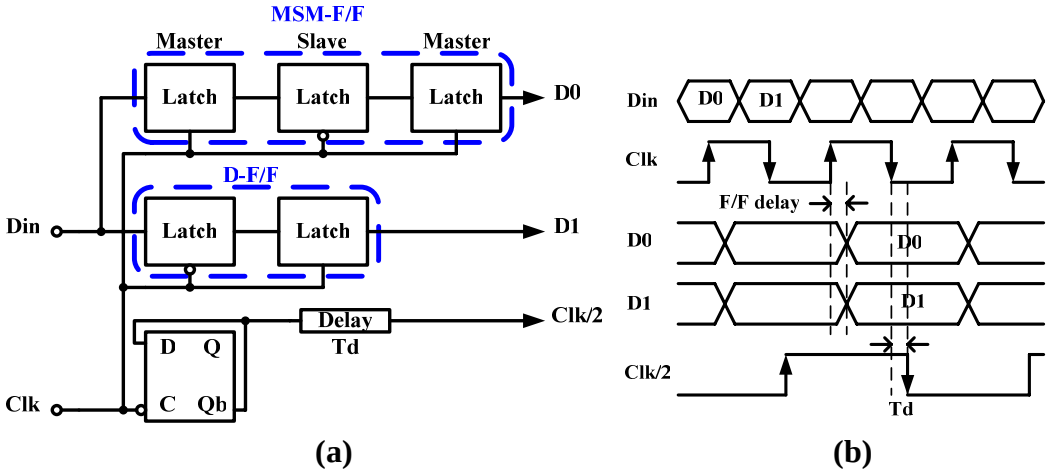


Figure 5-19 (a) 1:2 DEMUX (b) timing diagram

The module contains a clock divider for the next stage, as well as a D-flip-flop (D-F/F) and a master-slave-master type flip-flop (MSM-F/F) for data. The module

operates at half the clock speed of the input data rate. This is because this module operates using both rising and falling clock edges. The D-F/F outputs odd data streams at rising edges of the clock, and the master-slave latches in the MSM-F/F latch even data streams at falling edges of the clock. These latched data are output at rising edges of the clock by the second master latch in the MSM-F/F. In this way, two bit output data D0 and D1 are synchronized with the rising edges of the input clock. A divided clock Clk/2 is generated at the falling edges of the input clock. With the delay circuit, which adjusts the timing between D0/D1 and Clk/2, the timing of the Clk/2 for each next stage is set at the precise center of each D0/D1 eye.

Fig 5-20 is the illustration of the de-multiplexer operation and the De is the even parts of the input stream generated at Y2 as shown in **Fig 5-7**. The D0 of the data stream is finally de-multiplexed to 150MHz parallel data at the Dout0 channel.

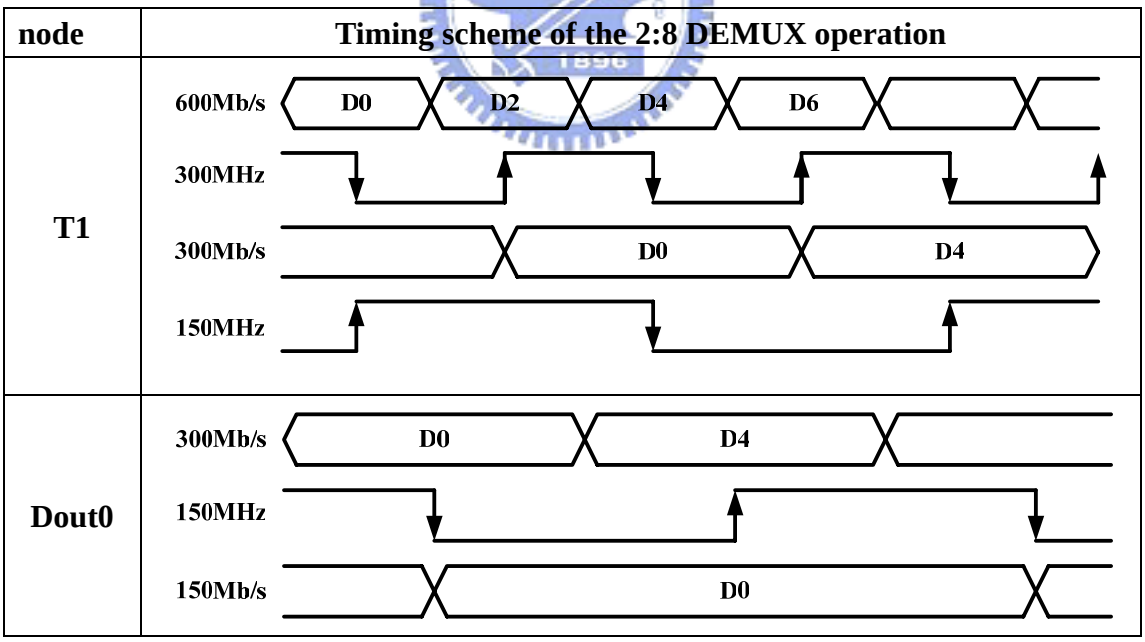


Figure 5-20 Illustration of 2:8 DEMUX paralleling the data (D0 is the example)

5.7 Receiver Simulation Result

The top part of **Fig 5-21** shows the received data from the transmitter and through the cable channel mentioned in chapter4 and the differential swing is about 400mv. The down part shows the corresponding output signal, and the input data with limited swing is amplified to full swing.

Fig 5-22 shows the ripple of the control voltage of the VCO when the CDR is in the lock state, and the control voltage is kept at about 1.305V. Since there are ripples on control voltage and the ripples would cause jitter on the retimed clock of CDR, reducing the amplitude of the ripple on control voltage is necessary. From this figure, the amplitude of control voltage is hold within about 35mV.

Fig 5-23 shows the input data of the CDR system and the retimed clock is almost located at the midpoint of the input data. **Fig 5-24** shows the retimed even and odd data (Y1 and Y2 in **Fig 5-7**) when the CDR is in lock state. After CDR is in the lock state, the input serial data stream at1.2Gbps rate is de-multiplexed to eight parallel channels at 150MHz rate. The outcome of the receiver is shown in the **Fig 5-25**. The Din is the input data of the receiver and Dout0 ~ Dout7 are the eight parallel output data.

In order to test the tracking ability of the receiver, we change the input data phase by 90° while the CRD is lock already. As shown in **Fig 5-26**, the phase of input data is changed at 1.81ns, the control voltage ripples and it takes the CDR about 110ns to regain the lock state.

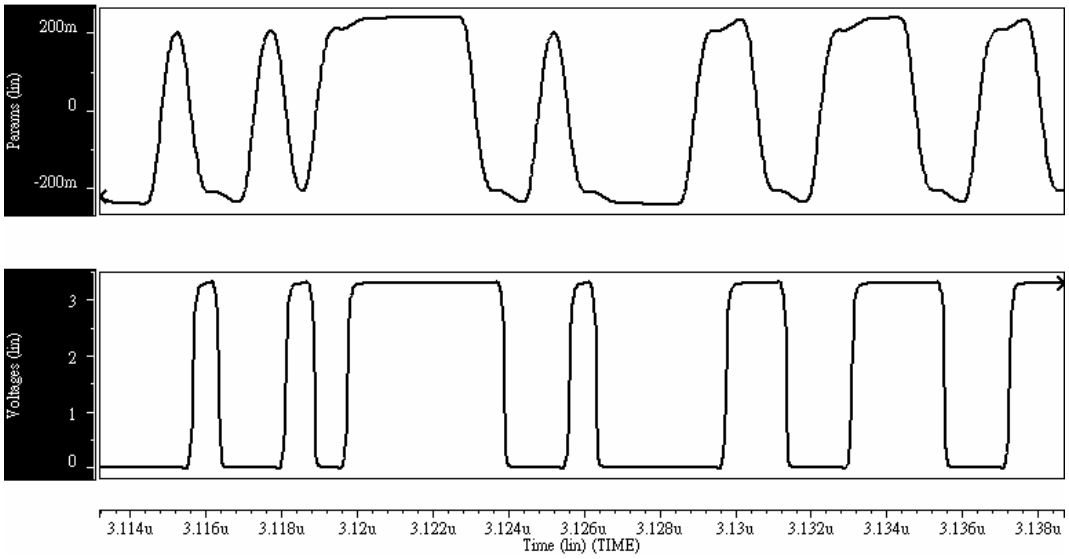


Figure 5-21 Waveforms of received data and output of the slicer

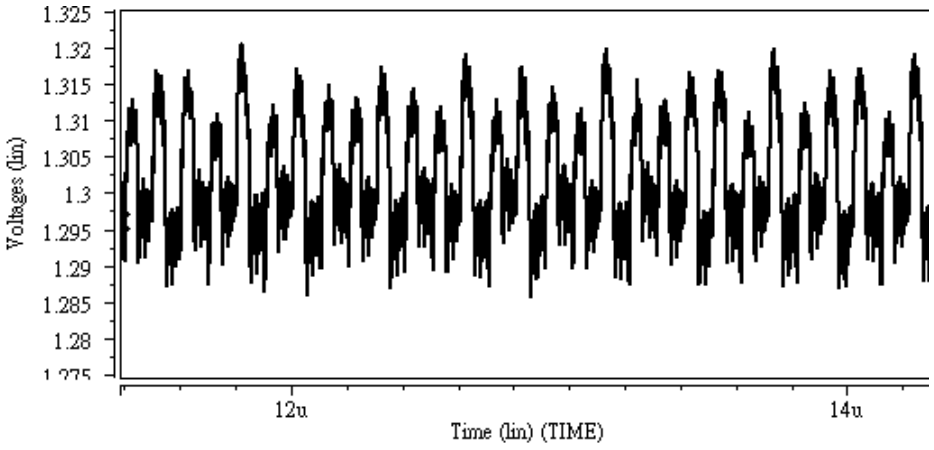


Figure 5-22 Control voltage of VCO when CDR is in lock state

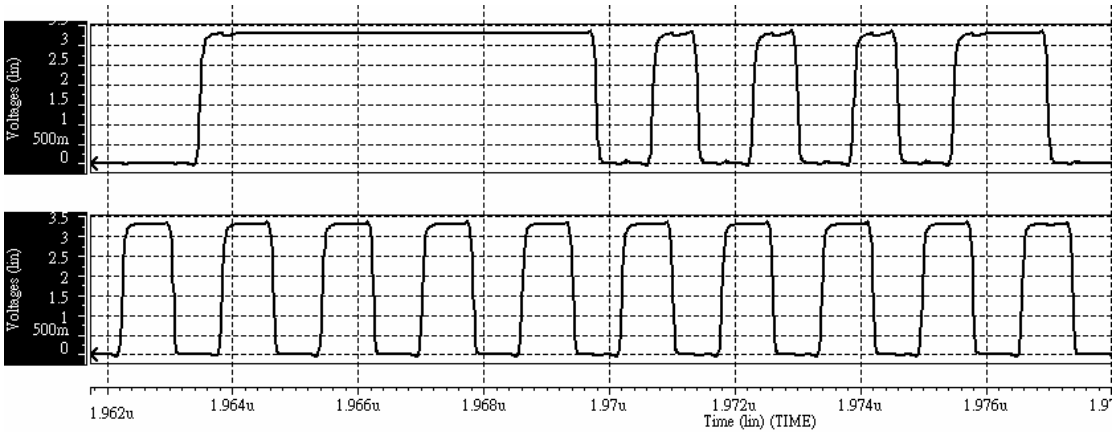


Figure 5-23 Input data and retimed clock while CDR in the lock state

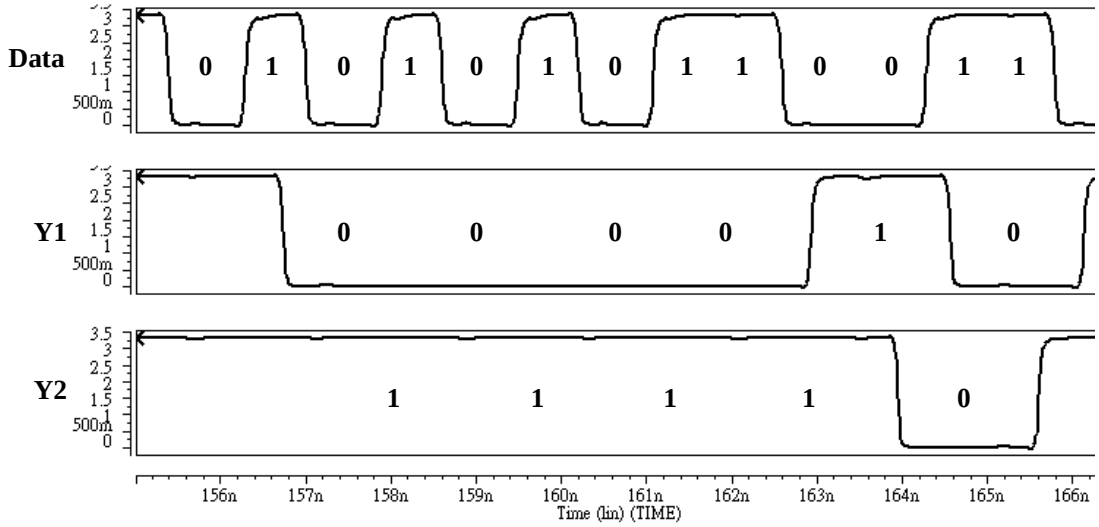


Figure 5-24 Retimed even and odd data and Retimed clock

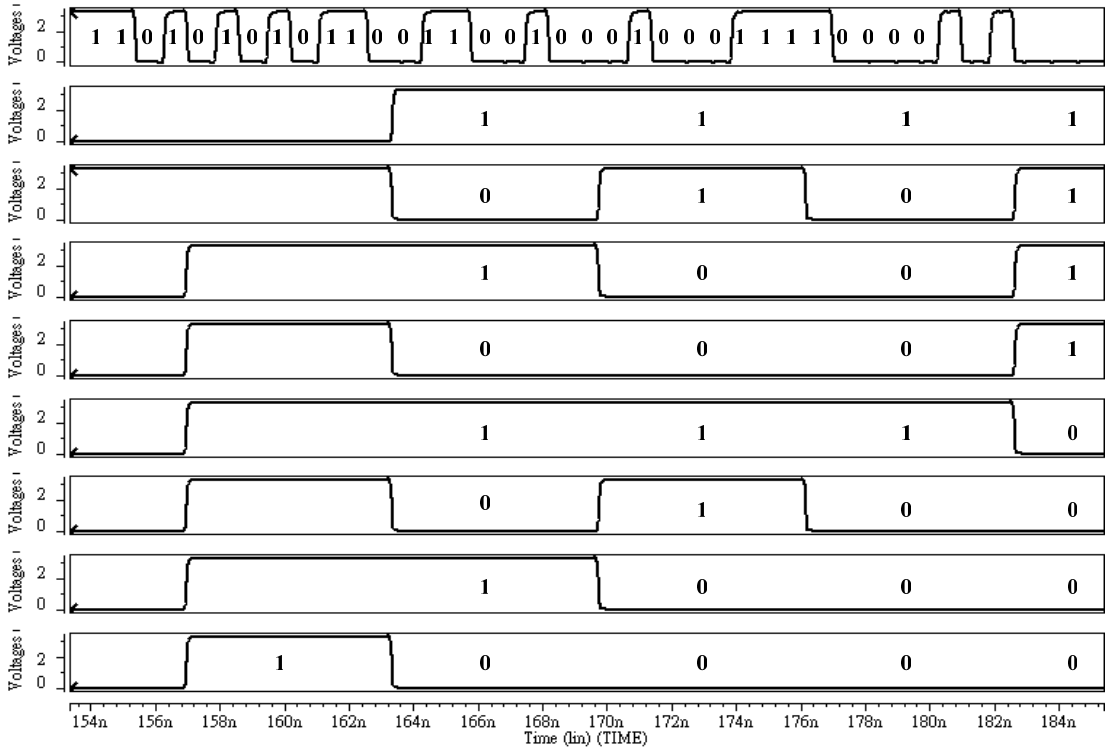


Figure 5-25 Serial input data and 8-parallel outputs of receiver

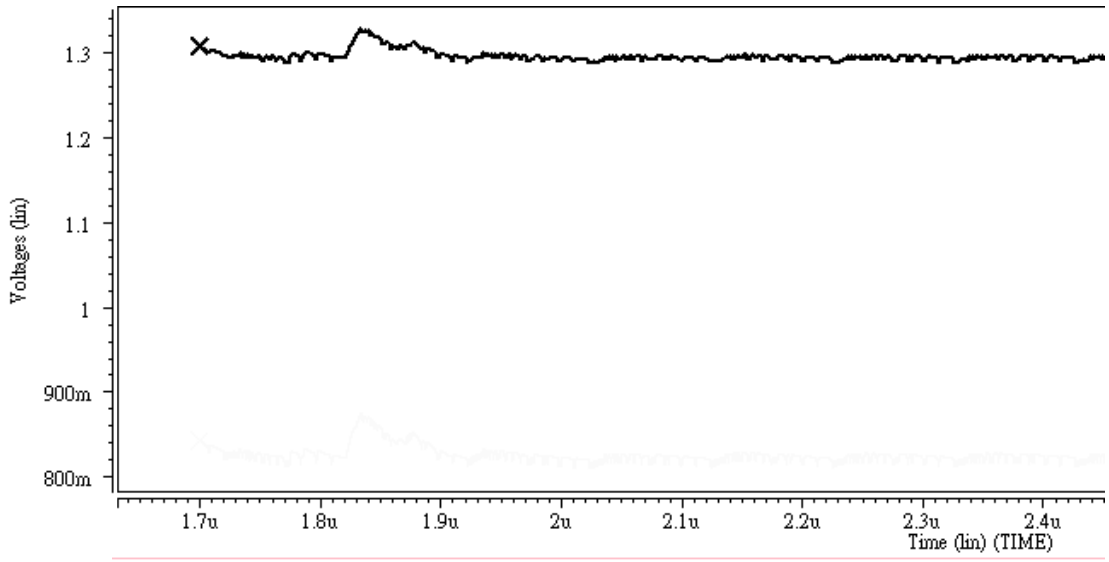


Figure 5-26 The variation of control voltage when the phase of input data is changed by 90°

Chapter 6

Conclusion and Future work

6.1 Conclusion

In this thesis, we have accomplished the design of the transceiver based on RSDS interface including a transmitter and a half-rate clock and data recovery receiver. It is a way to communicate data using the very low swing (about 200mV) differential over two printed circuit board (PCB) traces or cable. We design the circuit for operating at 1.2Gbps data rate. Transmitter consists of PRBS for generating test input data, eight-phase PLL, 8-to-1 multiplexer for transferring the parallel input data to serial data stream and data driver. With the 75MHz input reference clock, the PLL oscillates 8 phases at 150MHz rate. PLL is composed of Phase Detector for detecting the difference between the reference clock and output clock, Charge Pump for providing the current to charge or discharge the control voltage, Loop Filter, Voltage Control Ring-Oscillator for generating the eight-phase clock, and a divided by two circuit. The 8-to-1multiplexer is constructed with the 3-levels type MUX. This kind multiplexer provides a better bandwidth for high speed than the Multi-phase Type MUX. For the receiver part, the slicer at the receiver front-end resolves the small input at high data rates. The clock and data recovery (CDR) operates at half of the input data rate and uses a dual-tracking path control mechanism to achieve better jitter performance. Then, the de-multiplexer converts the CDR outputs to eight parallel data.

6.2 Future Work

The increasing demand for data bandwidth in communication system has driven the development of the high-speed and low-cost serial link technology. We can do the further work as below to achieve the high-speed operation destination.

- Reduce PLL output jitter
- Make the multiphase clock uniform more
- Use the current mode logic in Phase Detector of CDR to reduce the swing noise, power consumption and retimed clock jitter.

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