國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

互補式金氧半十位元 40MHz 取樣頻率導管式類比數位轉換器

A 3.3v 10-bit CMOS pipelined Analog-to-Digital Converter

研 究 生 ： 黃傑忠

指導教授 ： 吳錦川 教授

中華民國九十四年九月

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碩士論文

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摘要

由於導管式類比數位轉換器在達到低功率且高速的同時，也不會耗費太大的面積，因此時常被使用在許多必須兼顧高速以及高精確度的應用中。然而如果想要達到更高速以及更高精確度的同時，許多的問題就會產生，像是電容的不匹配效應，運算放大器的有限增益以及頻寬，比較器的參考電壓漂移等等的問題。在本篇論文中，我們提出了一個新的正回授放大器來解決因增益與頻寬不夠還有寄生電容所造成的一些誤差，非常適用於高效能的類比數位轉換器中。

在這篇論文中，使用了台積電 0.35um 雙氧化層以及四層金屬的製程來模擬一個全差動架構，3.3 伏特供應電壓，10 位元，40MHz 取樣頻率的類比數位轉換器，本設計採用了每級 1.5 位元的錯誤更正技術。這個類比數位轉換器中包含許多元件，其中有餘數放大器，比較器，正反器，加法器，時脈產生器和一個前端的取樣電路，此架構的差動輸入範圍是負 1 伏到正 1 伏。

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ABSTRACT

Among all architectures of analog-to-digital converter (ADC), the pipeline architecture was widely used in applications with high speed and high resolution, due to its small size and low power consumption. If we want to achieve higher speed and more accuracy, there are some errors to overcome. Such as capacitor mismatch, operational amplifier gain error, bandwidth limitation, comparator threshold offset and so on. In this thesis, we present a new operational amplifier with positive feedback technique to reduce its gain error and input parasitic capacitance, it is well suited to implement ADC with high performance.

In this thesis, a fully differential 3.3V, 10-bit, 40M sample/sec pipelined ADC with a 1.5-bit stage digital error correction has been designed with TSMC 0.35-μm double-poly four-metal CMOS process. The components in this ADC include residue amplifier, comparator, **C^{2}MOS** flip-flop, adder, clock generator and front-end sample-and-hold(S/H). The input range is -1V~+1V.

致謝

在碩士兩年的生涯中，學到了不少的東西，也體驗到了不少的東西。其中包括了在修課時所遇到的瓶頸，以及在不熟悉的環境中所感到的迷惑，剛開始時真的有種窒息的感覺，幸好在身邊有著志同道合的好朋友，彼此間的鼓勵與扶持，讓我們共同度過了辛苦卻收獲滿滿的兩年。

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接著要謝謝我的家人，無論在任何的艱苦下，他們總是給我最無私的援助，讓我能夠有動力能夠支撐下去。當然，還有在 307 實驗室的所有學長，阿瑞、權哲、史周、聖文、大師兄與一齊努力的同窗們，志朋、POLO、BUTTHEAD、小鍵、大建樺、弼嘉、紅毛、阿信、諭哥、岱原、粘哥、煒銘、宗熙、啟賓、建文、進元、台佑等，謝謝你們無論是在學業上以及非學業上所給予我的指導與歡樂，還有新進 307 的小碩一們，雖然跟你們相處的時間不多，但能有你們這樣的學弟，是我們學長們的福氣。最後要感謝我的女朋友呂芷瑩小姐，感謝她不管在任何的時候，都能給我打氣加油，雖然很多時候是叫我出去玩，不過也讓我能在工作與娛樂之中取得平衡，不至於被強大的壓力給擊倒，最後我僅以此篇論文獻給我身邊的所有人，沒有你們就不會有今天的我。

黃傑忠

九十四年九月

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FIGURE CAPTIONS


E
S
A
1896

Chapter 1

Introduction

1.1 MOTIVATION

The analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are required between analog signal and digital systems to take advantage from digital signal processing (DSP) as shown in Figure 1.1. There are several reasons why DSP of an analog signal may be preferable to processing the signal directly in analog domain. First, accuracy considerations play an important role in determining the form of the signal processor. Second, the digital signals are easily stored on magnetic media without loss signal fidelity. Third, in many case, a digital implementation of the signal processing system is cheaper than an analog one. As a consequence, more and more applications have replaced much analog circuits with their digital counterparts (such as digital audio). However, the signals in real world are analog signals, the need for analog circuit design remains strong.

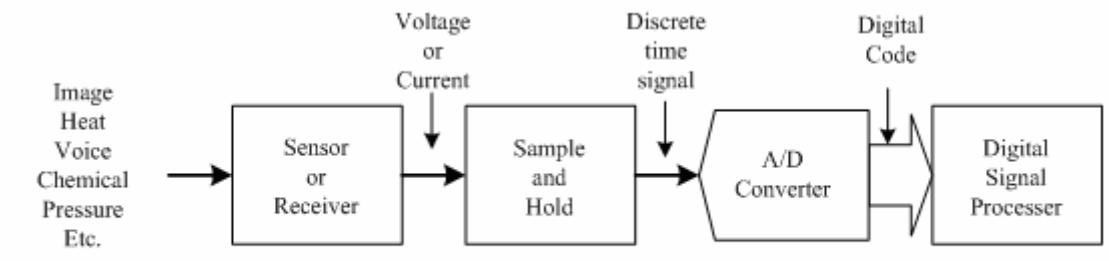


Figure 1.1 A typical block diagram of signal-processing system.

In recent years, the technologies of semiconductor were rapidly developed; digital circuits have achieved more accurate, reliable, storable, higher yield and fewer costs. This trend made a great impact on mixed-signal integrated circuits. The speed of the A/D and D/A interfaces must scale with the speed of the digital circuits in order to fully utilize advantages of advanced technologies. Furthermore, the ADC is implemented with a great deal of digital circuits. The noise immunity becomes an important issue in mixed-signal systems. Therefore, the design of ADC for high speed and high resolution with reasonable chip area and power consumption is one of many difficult challenges of analog design.

1.2 THESIS ORGANIZATION

In chapter 2, the basic concepts of performance metrics used to characterize ADCs is introduced. Then, the architectures of ADC are reviewed. We also summarized the characteristic of those ADCs at last. In chapter 3, the pipeline architecture is briefly introduced. Furthermore, the error sources of each stage of pipelined ADC are discussed. In chapter 4, the design and analysis of the building block will be presented. In chapter 5, we made conclusions for our design, and the future work is given.

Chapter 2

Fundamentals of Pipelined Analog-to-Digital Converter

2.1 OVERVIEW

The analog-to-digital converters are widely used in many applications. A high-speed ADC is usually applied to video system, and multi-media system, etc. Digital processing, storage, and transmission of video information require an ADC can be operated with a sample rate, range from 20MHz to 100MHz, and a resolution range from 8-bit to 12-bit.The summary of ADC in systems are shown in Table 2.1 [1]. For instance, the conventional NTSC TV system requires 8-bit resolution and a 20MHz sampling. However, recently proposed high definition television (HDTV) digital VTR in Japan requires 10-bit resolution and 75 MHz sampling for 1125 scanning lines, a 60Hz field rate with 30 MHz bandwidth luminance signal, and two 15MHz bandwidth color-difference signals [2].

Architectures for realizing ADC can be roughly divided into three categories—low-to-medium speed, medium speed, and high speed as shown in Table 2.2 [3]. Each of them is the different trade-off between resolution, speed, area and power. In this chapter, we first discuss performance specifications to characterize ADCs, and then describe the design details for these different Architectures. In the end of this chapter, we summarized and chose the suitable architecture to meet our target specification.

Table2.1 Summary of ADC in systems

Applications	Requirements
NTSC/PAL Decoder	8Bits, 14-17MHz
HDTV	8-10Bits, 50-75MHz
CATV Channel Modems	8-12Bits, 50-75MHz
ADSL/HDSL Transceivers	12-16Bits,3MHz
CDDI Transceivers, VG	8-10Bits, 30-60MHz
Mag Storage Read Channel	6-8Bits, 75-150MHz
High Performance Imager	12Bits, 75MHz
Scanner	10-16Bits, 6-40MHz
LCD Monitor	8Bits, 150MHz
APS CMOS Sensor	8-12Bits, 20MHz

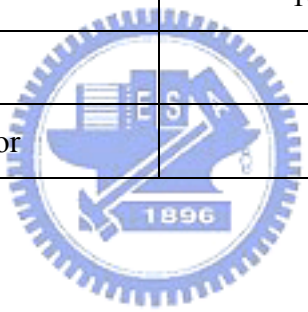


Table2.2 Different A/D converter architectures

Low-to-Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low-to-Medium Accuracy
Integrating	Successive approximation	Flash
Oversampling	Algorithmic	Two-step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

2.2 ADC PERFORMANCE SPECIFICATIONS

ADCs are characterized in a number of different ways to indicate the performance capability, cost, and ease of use. Some of the most important characteristics of ADCs are introduced below.

2.2.1 Resolution and LSB

Resolution describes the fineness of the quantization performed by the ADC. Sometimes it is called as effective number of bits (ENOB). A high resolution ADC divides the input range into a large number of sub-ranges than a low resolution converter. Resolution is usually defined as the base 2 logarithm of the number of sub-ranges which the ADC inputs range is divided into. This quantity is referred to the number of bits resolved by the ADC. Thus, for a fixed full scale input range, the high resolution ADC can resolve smaller signals than a low resolution ADC. Resolution is usually degraded by noise or nonlinearity. Therefore, most techniques for characterizing the true resolution of an ADC are to measure either noise, nonlinearity, or both [4].

LSB means least significant bit size, can be expressed by Equation (2.1).

$$LSB = \frac{V\max}{2^N} \tag{2.1}$$

Where Vmax is the full-scale voltage, N is the ADC's resolution. It is useful to define LSB to be the voltage change when one LSB changes, particularly in measure errors.

2.2.2 Nonlinearity

Most ADCs are intended to have a transfer characteristic approximating a straight line. As the resolution increases, the input-output characteristic of the ADC is

more close to a straight line. The transfer characteristic for ideal ADCs progresses from low to high in a series of uniform steps. Therefore, nonlinearity is present even in an ideal ADC. The transfer characteristic of a practical ADC contains steps which are not perfectly uniform, and this deviation generally contributes to further non-idealities. Such non-idealities can be expressed in several ways as shown in Figure 2.1. An error which causes all thresholds to shift from their ideal positions by an equal amount is called an offset error. Non-ideality which results in an erroneous quantizer step size is called gain error or scale factor error. Linearity error refers to the deviation of the actual threshold levels from their ideal values after offset and gain errors have been removed. Excessive linearity error results in missing codes.

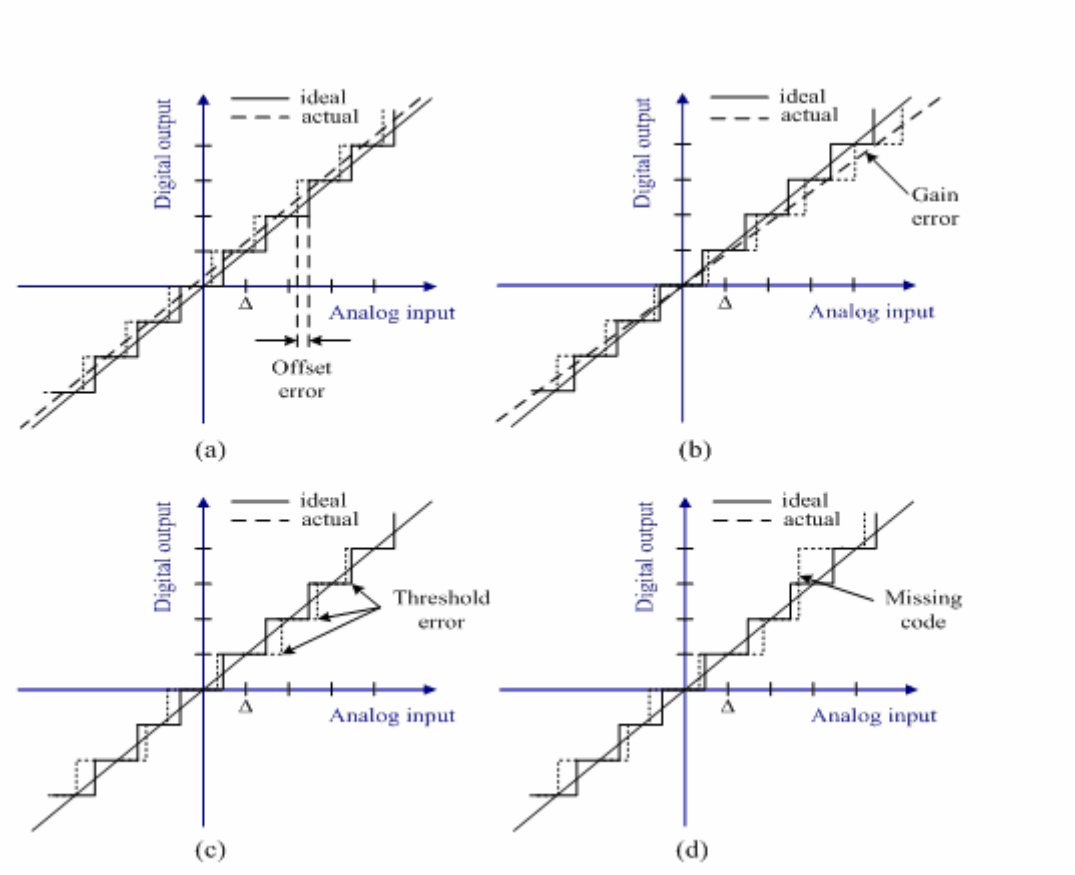


Figure 2.1 Quantization transfer functions including error sources (a) Offset error, (b) Gain error, (c) Linearity error, (d) Missing code.

Two types of nonlinearity are used to characterize this deviation. Differential nonlinearity (DNL) measures how far each of step sizes deviates from nominal value of the step size. Integral nonlinearity (INL) is the difference between the actual transfer characteristic and the straight line characteristic the ADC is intend to approximate. DNL and INL are both plotted as a function of code. DNL and INL are generally expressed in term of LSB of the converter input. Figure 2.2 shows INL and DNL, which can be expressed as Equation (2.2) and Equation (2.3).

$$DNL(i) = \frac{UB(i+1) - UN(i)}{LSB} - 1 \tag{2.2}$$

$$INL(i) = \frac{UB(i+1) - UN(i)_{ideal}}{LSB} - 1 \tag{2.3}$$

where UB(i) is transition level of i-th code [4] [5] [6] [7].

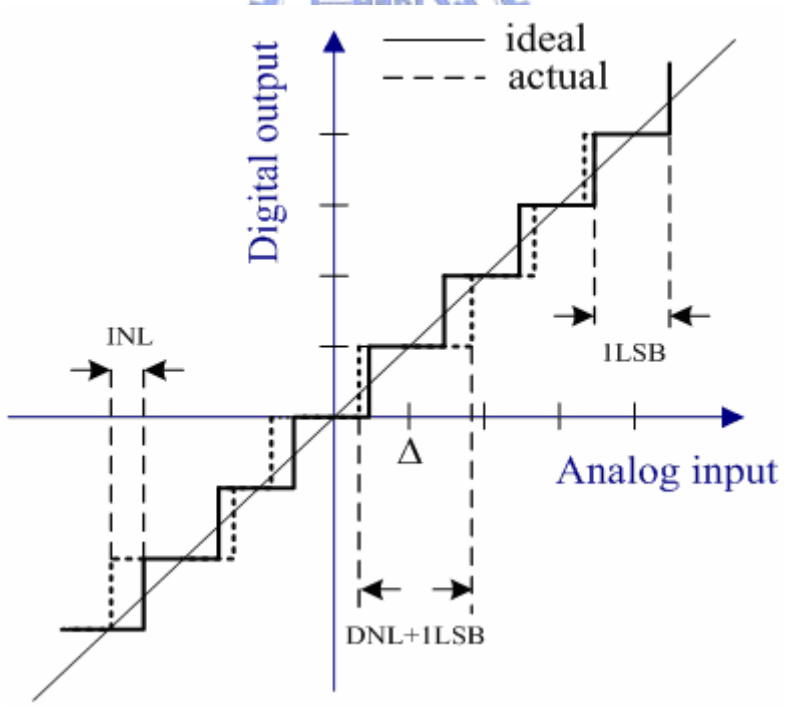


Figure 2.2 Transfer characteristic of ADC showing INL and DNL.

2.2.3 Signal to Noise Ratio

The signal to noise ratio (SNR) is the ratio of signal power to noise power in the output of ADC. One common way to measure SNR is plot the spectrum of the output of the ADC. The SNR is calculated by measuring the difference between signal peak and noise floor and including a factor to adjust for the number of samples used to generate the spectrum as shown below.

$$SNR(db) = signal\_peak(db) - noise\_floor(db) - 10\log N \qquad (2.4)$$

The last term in the Equation (2.4) can be understood as follows. To generate an N point Faster Fourier Transform (FFT) of a signal, N samples of the signal are taken. Sampling the signal N times increase signal power by a factor of N^2 and the noise power by a factor of N. Thus the SNR is increased by a factor of N and the SNR of the FFT is higher than SNR in one sample of the signal. The SNR improvement in db is 10logN, and the noise floor in the FFT becomes lower relative to the signal as more samples are taken. Figure 2.3 illustrated this idea [8].

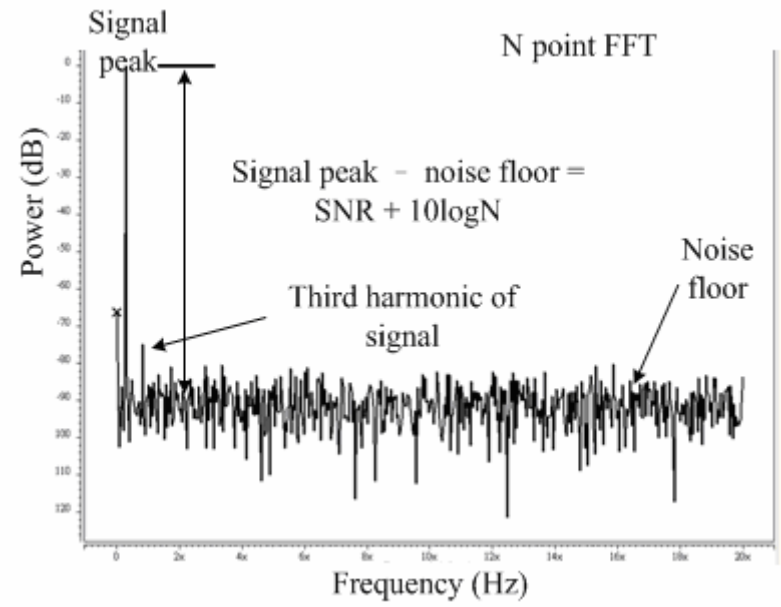
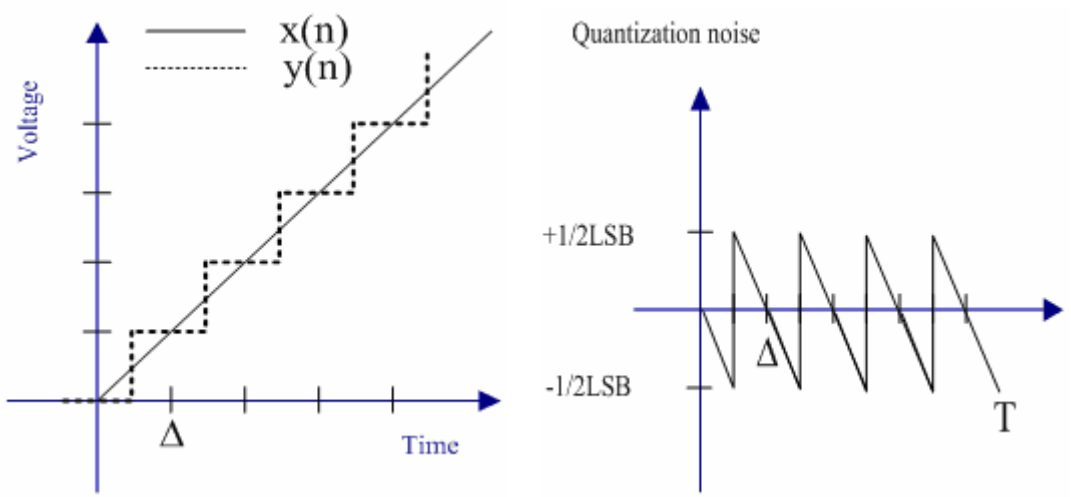


Figure 2.3 Procedure for computing SNR from an N point FFT

The use of quantization introduces an error, q(n), defined as the difference between input signal x(n) and the output y(n). The error is called quantization noise. We can build a model to calculate as shown in Figure 2.4



(a) (b)

Figure 2.4 (a) The difference between input signal x(n) and the output y(n). (b) Quantization error of an ADC.

It is assumed that the quantization error Q is a uniformly distributed random variable, and the interfering effect of the quantization noise on the quantizer input is similar to that of thermal noise. The probability density function for such an error signal will be a constant value, as shown in Figure 2.5.

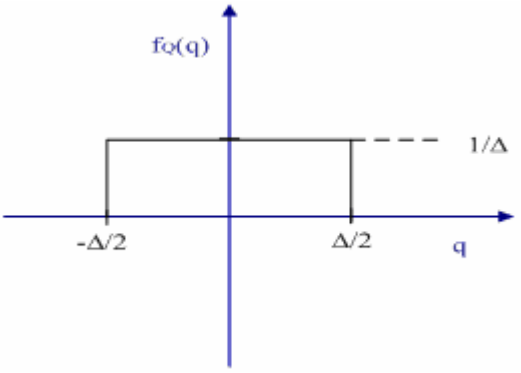


Figure 2.5 The probability density function of the quantization error.

The equation of the quantization error Q is expressed as Equation (2.5).

$$f_Q(q) = \begin{cases} \frac{1}{\triangle}, & -\frac{\triangle}{2} \le q(n) \le \frac{\triangle}{2} \\ 0, & \text{otherwise} \end{cases} \tag{2.5}$$

Therefore, the R.M.S value of the quantization error is

$$V_{Q,rms}^2 = \frac{1}{\triangle}\int_{\frac{-\triangle}{2}}^{\frac{\triangle}{2}} q^2 dq = \frac{\triangle^2}{12} \tag{2.6}$$

In general, when the quantization noise is uniformly distributed over the interval $\pm V_{LSB}/2$, the R.M.S quantization noise voltage equals $V_{LSB}/\sqrt{12}$ and is independent of the sampling frequency, fs, and input signal.

The SNR formula is to assume that V_{IN} is a sinusoidal waveform between -Vref and Vref. Thus, the AC R.M.S value of sinusoidal wave is

$$V_{IN,RMS} = \frac{V_{ref}}{\sqrt{2}} \tag{2.7}$$

Then, the SNR is given by

$$SNR = 20\log_{10}\left(\frac{V_{IN,RMS}}{V_{Q,RMS}}\right) = 20\log_{10}\left(\frac{\frac{V_{ref}}{\sqrt{2}}}{\frac{V_{LSB}}{\sqrt{2}}}\right) = 20\log_{10}\left(\sqrt{\frac{3}{2}}2^N\right) \tag{2.8}$$

It can be expressed in dB:

$$SNR = 6.02N + 1.76 \quad (\text{dB}) \tag{2.9}$$

Note that Equation (2.9) gives the best possible SNR for an N-bit ADC. However, the idealize SNR decreases from this best possible value for reduced input signal levels [4] [5].

2.2.4 Signal to Noise + Distortion Ratio

The signal to noise plus distortion ratio (SNDR) is also often used to measure the performance of an ADC. It measure degradation due to the combined effect of noise, quantization errors, and harmonic distortion. The SNDR of a system is usually measured for a sinusoidal input and is a function of the frequency and amplitude of the input signal. When a sinusoidal signal of a single frequency is applied to a system, the output of the system generally contains a signal component at input frequency. Due to distortion, the output also contains signal components at harmonics of the input frequency. An ADC usually samples an input signal at finite rate. As the result, some of the harmonic distortion products are aliased down to lower frequencies. Furthermore, the ADC adds noise to the output, and this noise is generally present to some degree at all frequencies. The SNDR of the ADC is defined as the ratio of the signal power in the fundamental to the sum of the power in all of the harmonics, all of the aliased harmonics, and all of the noises [8]. It can be expressed by Equation (2.10).

$$SNDR = 20\log_{10}\left(\frac{V_{IN,RMS}}{V_{tatol\_noise,RMS}}\right) \tag{2.10}$$

2.2.5 Dynamic Range

Dynamic range is another useful performance benchmark. Dynamic range is a measure of the range of input signal amplitudes for which useful output can be obtained from a system. Dynamic range can be defined in a number of different ways. One way to define dynamic range for a system is as follows. Apply a sinusoidal input of a single frequency to the system and vary the amplitude. Measure the maximum power obtainable from the system at the input frequency. The dynamic range could be

defined as the ratio of the maximum power at the fundamental frequency to the output power for a minimum detectable input signal. The minimum detectable input signal power is the value of the signal power when the signal to noise ratio is 0dB. If the noise power is independent of the size of the signal, the dynamic range is equal to the SNR at full scale. However, in some cases the noise power increases as the signal level increases. In these cases, the maximum SNR is less than the dynamic range [4] [5].

2.2.6 Spurious Free Dynamic Range

The spurious free dynamic range (SFDR) is the ratio of the largest spurious frequency and the fundamental frequency. This is the difference between the R.M.S input signal and highest frequency spur at the output of the ADC as showing in Figure 2.6.

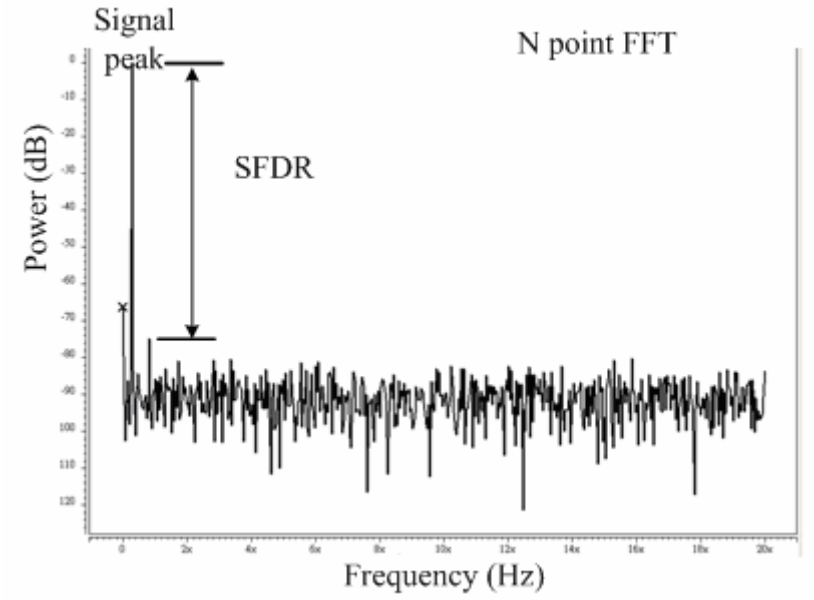


Figure 2.6 An example of how SFDR is measured in a FFT test.

2.2.7 Sampling Rate, Conversion Time and Latency

The sampling rate indicates the number times the input signal is sampled per second. Conversion time means converter data time from sample to data out, and latency is the clock cycle from sample edge to data out edge. Figure 2.7 shows examples above.

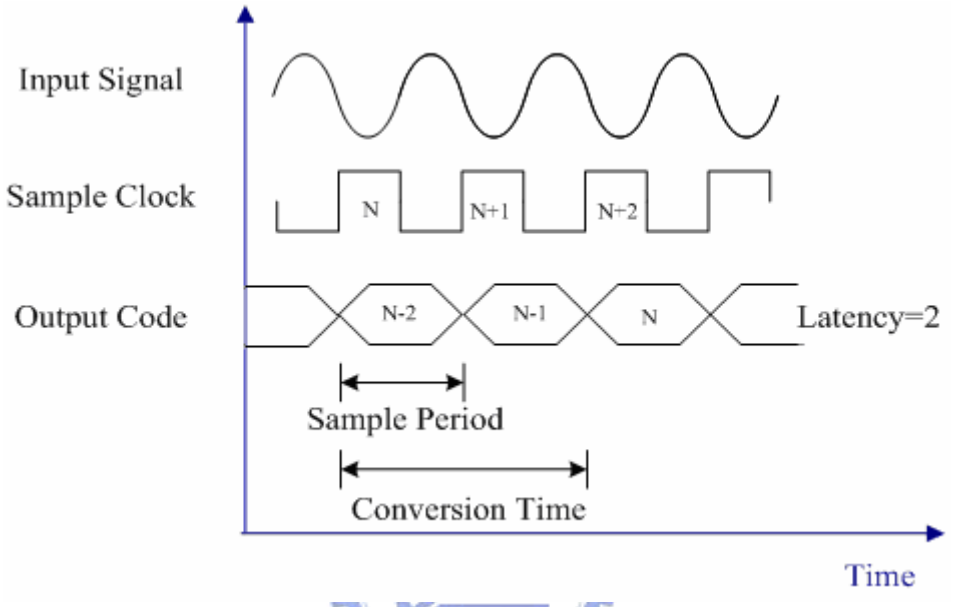


Figure 2.7 Definitions of sampling time, conversion time and latency

2.2.8 Input Bandwidth

ADC's resolution is a function of the frequency of the input signal. At high input frequencies, the SNDR of the ADC output can be reduced by a number of effects. The input bandwidth of the ADC is the input frequency at which the SNDR is 3dB below the maximum value.

2.2.9 Input Capacitance

Input capacitance is the capacitive load presented by the ADC to the circuit driving it. The input capacitance of an ADC is an important parameter because the input capacitance can load the circuit driving the ADC and degrade its performance.

2.2.10 Input Signal Swing

The input signal swing indicates the maximum and minimum values that the input signal may have without driving the ADC out of range or resulting in an unacceptable level of distortion.

2.2.11 Power Dissipation

Power dissipation is becoming an important ADC specification because many ADCs are being implemented in portable systems powered by a battery with limited energy. Reducing power dissipation can reduce system weight or improve battery life. Reducing power dissipation can also make it easier to keep the temperature of the ADC at a reasonable level.

2.3 ARCHITECTURES OF ADC

2.3.1 Flash ADC

Flash ADCs, also known as parallel ADCs, are the standard approach for realizing very-high-speed converters. Figure 2.8 shows a block diagram of an N-bit flash ADC. It consists of 2^n-1 comparators, are used to directly measure an analog signal to a resolution of n bits. The flash architecture has the advantage of being very fast, because the conversion occurs in a single ADC cycle. The disadvantage of this approach is that it requires a large number of comparators that are carefully matched and properly biased to ensure that the results are linear. Since the number of comparators needed for an N-bit resolution ADC is equal to 2^n-1, limits of physical integration and input loading keep the maximum resolution fairly low. For example, a 4-bit ADC requires 15 comparators, an 8-bit ADC requires 255 comparators, and a 10-bit ADC would require 1023 comparators.

The flash ADCs are suitable for applications requiring very large bandwidths. However, flash converters consume a lot of power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications that typically cannot be addressed any other way. Examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives [3] [9] [10].

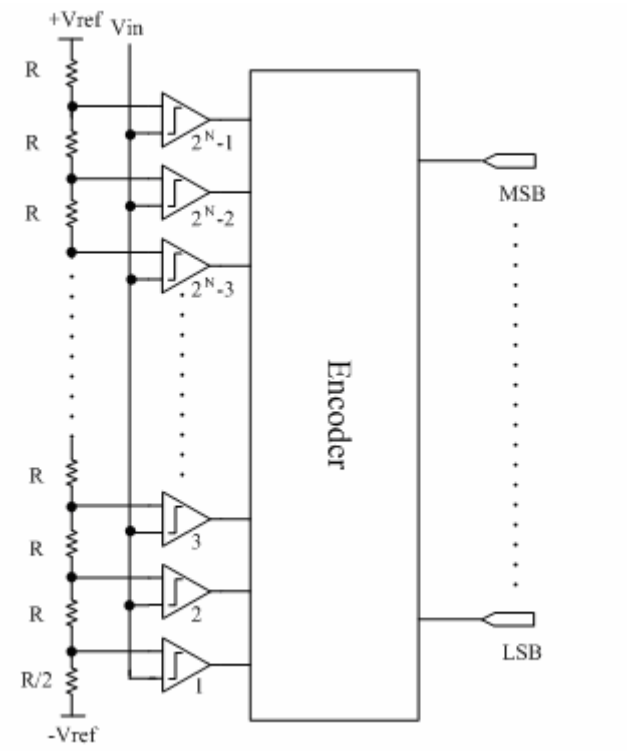


Figure 2.8 Block diagram of an N-bit flash ADC.

2.3.2 Sub-ranging ADC

In the field of high speed ADCs, the flash ADCs remain dominant due to their one-clock-cycle conversion; however, they suffer from large power consumption and area usage due to their 2^N comparators. For applications such as imaging, video and digital communication, where high resolution is required, the sub-ranging structures, first introduced by Dingwall and Zazzu [11], have gradually begun to replace the flash

ADC. Sub-ranging ADC uses fewer comparators than parallel flash ADCs. Instead of using one comparator per LSB like a flash converter does, a sub-ranging ADC uses fewer comparators, draws less power, has lower input capacitance, and can attain higher resolutions. Although not as fast as a parallel ADC, sub-ranging ADCs can digitize at speeds greater than 100 Ms/s at 8-bit resolution [12]. They can resolve signals to 16 bits at slower speeds. Figure 2.9 shows a block diagram of a 10-bit sub-ranging ADC that uses two 5-bit stages to digitize the analog input signal. The first ADC converts the upper 5 bits while the second stage converts the lower 5 bits. This design uses 62 comparators (31 for each ADC) rather than the 1023 comparators required by a 10-bit flash converter. Sub-ranging ADCs often find use in RF test equipment, lower-speed digitizing oscilloscopes, and high-end PC plug-in digitizer cards and PC-external data-acquisition systems.

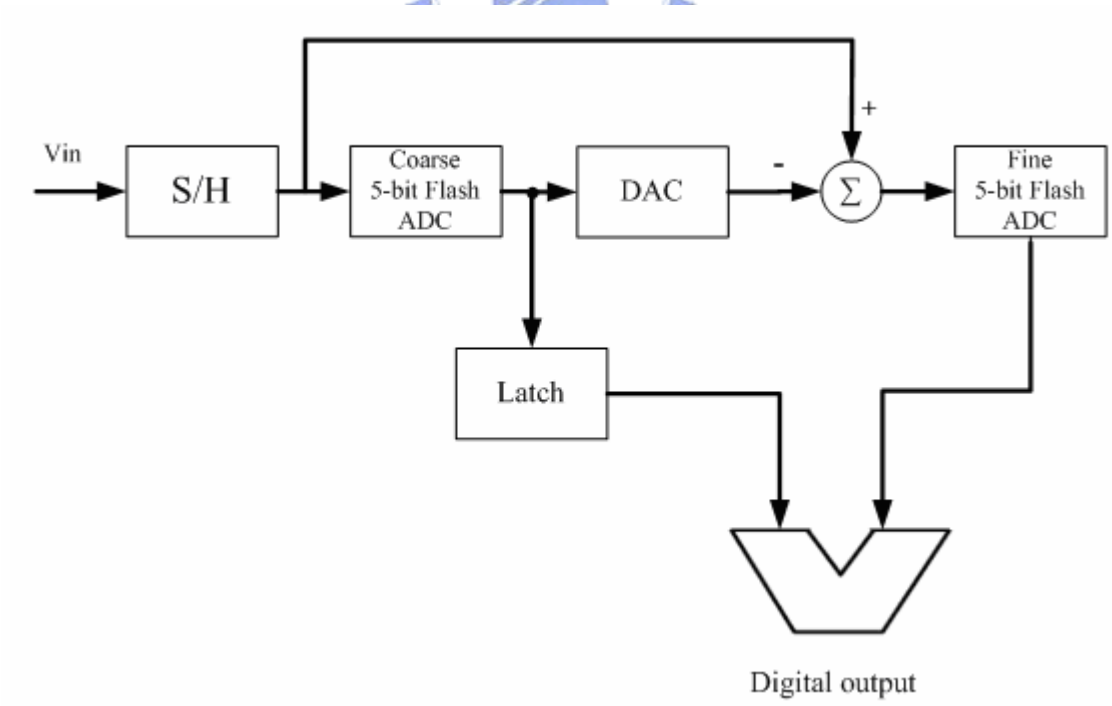


Figure 2.9 Conventional block diagram of a 10-bit sub-ranging ADC.

2.3.3 Successive Approximation ADC

The successive-approximation architecture can be thought of as the other end of the spectrum from the flash architecture. While a flash converter uses many comparators to converter in a single cycle; a successive-approximation-register (SAR) converter conceptually uses a single comparator to converter in many cycles. To understand the basic operation of SAR ADC, knowledge of the search algorithm referred to as a “binary search” is helpful [3]. Figure 2.10 shows block diagram of a SAR ADC. To implement the binary search algorithm, the N-bit register is first set to midscale (that is, 100... .00, where the MSB is set to '1'). This forces the DAC output (Vdac) to be Vref/2, where Vref is the reference voltage provided to the ADC. A comparison is then performed to determine if Vin is less than or greater than Vdac. If Vin is greater than Vdac, the comparator output is logic high or '1' and the MSB of the N-bit register remains at '1'. Conversely, if Vin is less than Vdac, the comparator output is logic low and the MSB of the register is cleared to logic '0'. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete, and the N-bit digital word is available in the register.

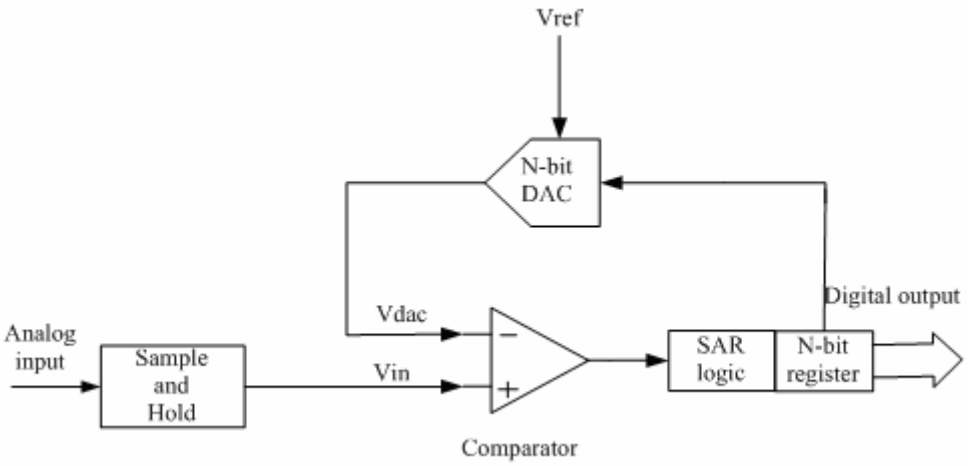


Figure 2.10 Block diagram of successive approximation architecture.

Figure 2.11 shows an example of a 4-bit conversion. The y-axis (and the bold line in the figure) represents the DAC output voltage. In the example, the first comparison shows that Vin < Vdac. Thus, bit 3 is set to '0'. The DAC is then set to 0100_2 and the second comparison is performed. As Vin > Vdac, bit 2 remains at '1'. The DAC is then set to 0110_2, and the third comparison is performed. Bit 1 is set to '0', and the DAC is then set to 0101_2 for the final comparison. Finally, bit 0 remains at '1' because Vin > Vdac.

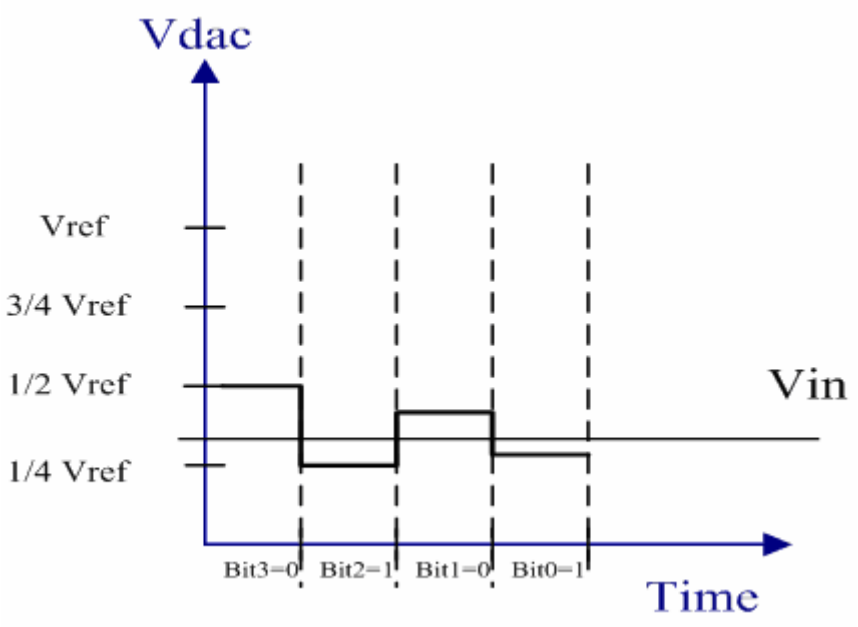


Figure 2.11 SAR operation (4 bits example).

SAR architectures are chosen frequently for medium-to-high-resolution applications, typically with sample rates fewer than 5 Ms/s. SAR ADCs most commonly range in resolution from 8 to 16 bits and provide low power consumption as well as a small form factor. This combination makes them ideal for a wide variety of applications, such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition.

2.3.4 Algorithmic (Cyclic) ADC

An algorithmic converter operates in much the same way as a SAR ADC. However, whereas a SAR ADC halves the reference voltage in each cycle, a cyclic ADC doubles the error voltage while leaving the reference voltage unchanged.

Figure 2.12 shows the block diagram for an algorithmic converter [3]. This converter requires a small mount of analog circuitry because it repeatedly uses the same circuitry to perform its conversion cyclically in time. This architecture has difficulties in building an accurate multiply-by-two gain amplifier. Besides, if we use the switch-capacitance circuits, the capacitor ratio mismatch and clock feed-through must be carefully considered also. For the audio applications, it could reach low-power and low-voltage operation.

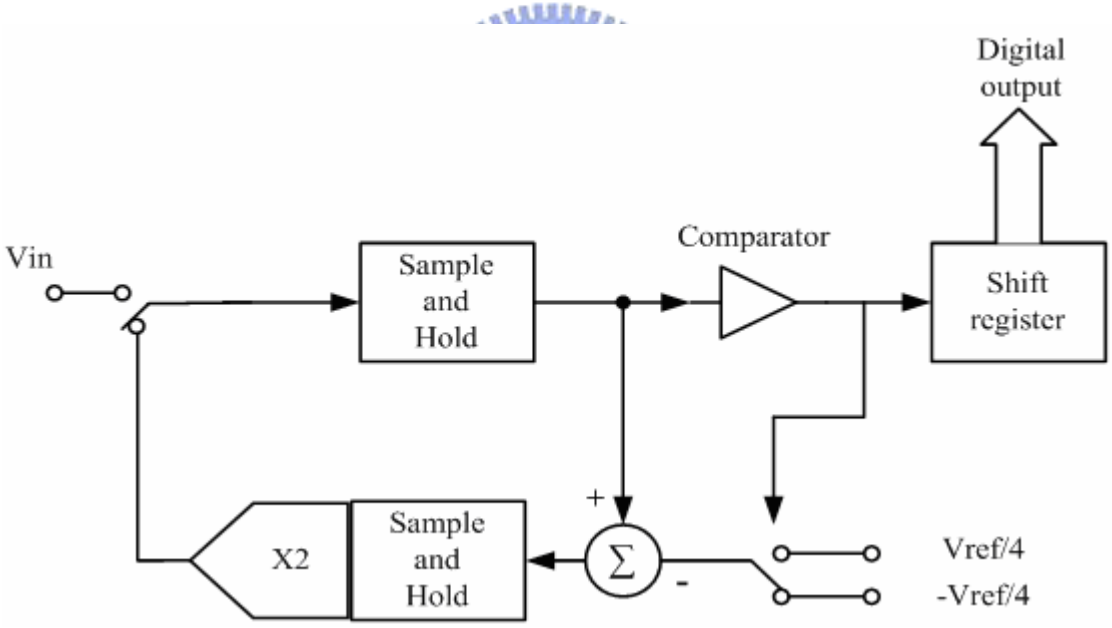


Figure 2.12 Block diagram of algorithmic converter.

2.3.5 Integrating (Dual Slope) ADC

The integrating converter architecture combines high resolution and excellent noise rejection, making it ideal for converting low-bandwidth analog signals [13]. Figure 2.13 shows the block diagram of an integrating ADC. It integrates the input

signal over a period of time so that fluctuations resulting from random noise contained in the signal are averaged together and thus largely eliminated. In its most basic form, the integrating ADC has two operational phases as shown in Figure 2.14. During the integration phase, the signal is converted to a stored charge on a capacitor. Once the integration period is completed, the reference phase begins. In this phase the capacitor is switched from the input signal to a fixed reference voltage which is opposite in sign to the input signal. The capacitor is discharged, and the time necessary to discharge the capacitor is measured. This time is directly related to the charge on the capacitor and is used to determine the binary output of the ADC.

The major disadvantage of integrating ADCs is that they are slow. Typical conversion rates are in the 1 to 10 samples per second range. For this reason integrating ADCs are typically used only in instruments where the signal level is expected to change rather slowly. This type of converters often include built-in drivers for LCD or LED displays and are found in many portable instrument applications, including digital panel meters and digital multi-meters.

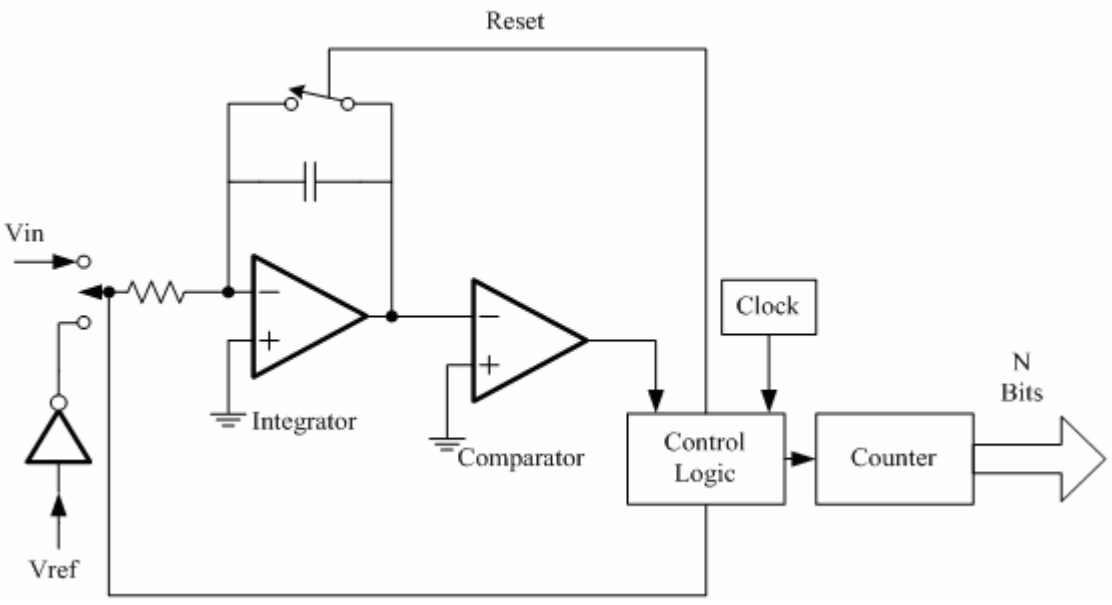


Figure 2.13 Block diagram of an integrating ADC.

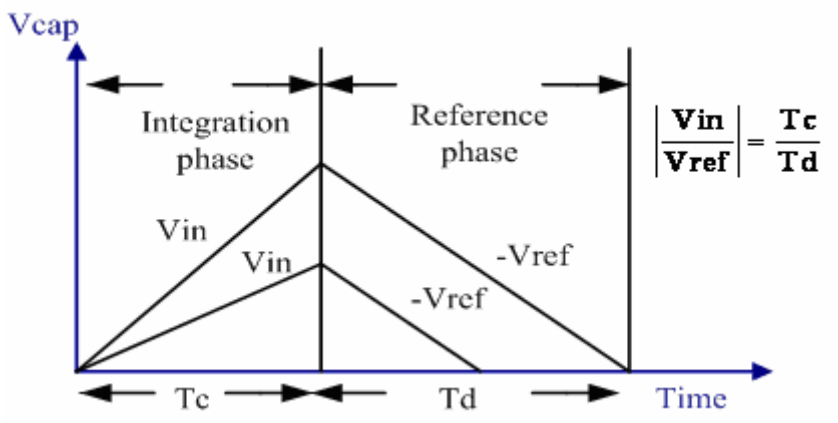


Figure 2.14 The operation of the integrating ADC.

2.3.6 Sigma-Delta (over-sampling) ADC

Sigma-delta converters, also called over-sampling converters, the basic concepts behind the sigma-delta ADC architecture originated at Bell Labs in the 1950s—in work done on experimental digital transmission systems utilizing delta modulation and differential PCM. By the end of the 1960s, the sigma-delta architecture was well understood. However, because digital filters (then a rarity) were an integral part of the architecture, practical IC implementations did not appear until the late 1980s, when signal processing in digital CMOS became widely available [14].

Figure 2.15 shows the sigma-delta ADC consists of 2 major blocks: modulator and digital filter. The modulator, whose architecture is similar to that of a dual-slope ADC, includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, transforming it to a serial bit stream with a frequency well above the required sampling rate. The output filter then converts the bit stream to a sequence of parallel digital words at the sampling rate.

Sigma-delta ADCs are used predominately in lower speed applications requiring a trade off of speed for resolution by over sampling, followed by filtering to reduce noise. 24-bit sigma-delta ADCs common used in Audio designs, instrumentation and Sonar. Bandwidths are typically less than 1MHz with a range of 12 to 18 true bits.

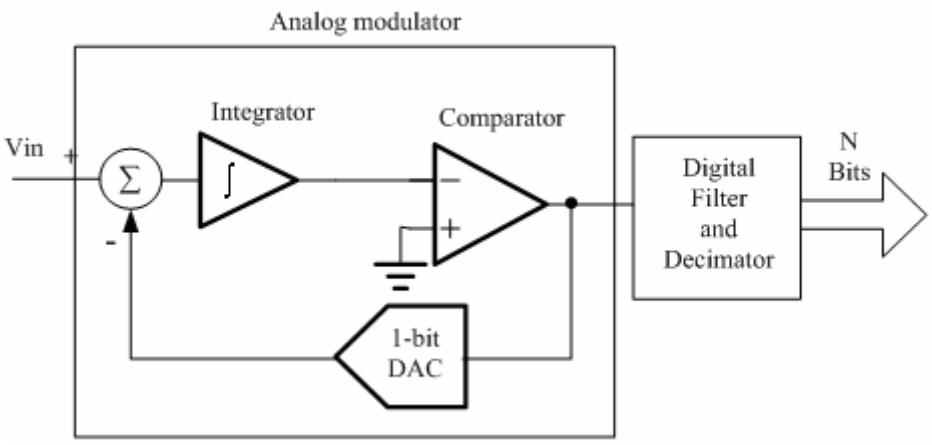


Figure 2.15 Block diagram of first-order sigma-delta ADC.

2.3.7 Folding and Interpolating ADC

Since the flash ADC uses many comparators costs a lot of power and area. It makes flash ADC not adequate for high resolution applications. In order to reduce the large number of comparators, the difference between analog input and each reference voltage can be quantized at the output of each comparator. This is possible because of the finite gain and nonzero linear input range of comparators in front of latches. Figure 2.16 shows example of a 4-bit interpolating ADC.

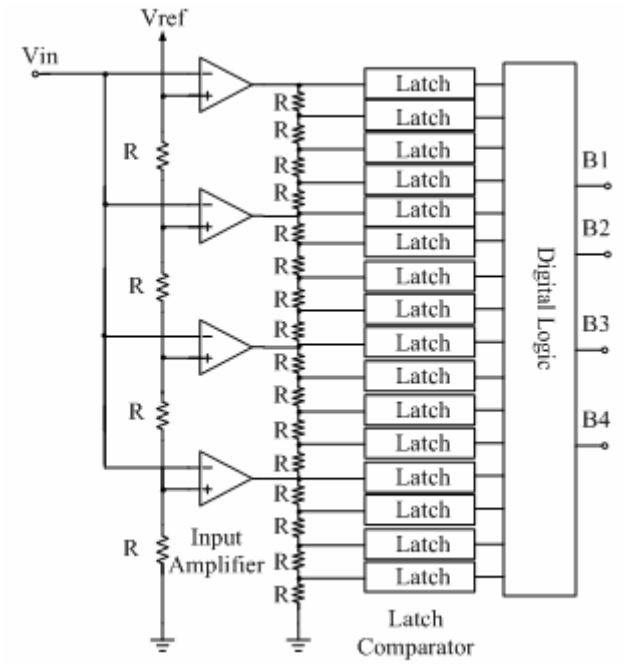


Figure 2.16 Example of a 4-bit interpolating ADC.

The number of input amplifier can be reduced by using the interpolating architecture. However, the number of latch comparators remains at 2^N for an N-bit converter. This large number of the latch comparators can be reduced by using folding architectures.

The folding architecture is similar in operation to a sub-ranging converter in that a group of LSBs are found separately from a group of MSBs. Whereas the sub-ranging converter requires an accurate DAC, a folding converter determines the LSB set more directly through the use of analog preprocessing while the MSB set is determined at the same time. Figure 2.17 shows example of a 4-bit interpolating ADC.

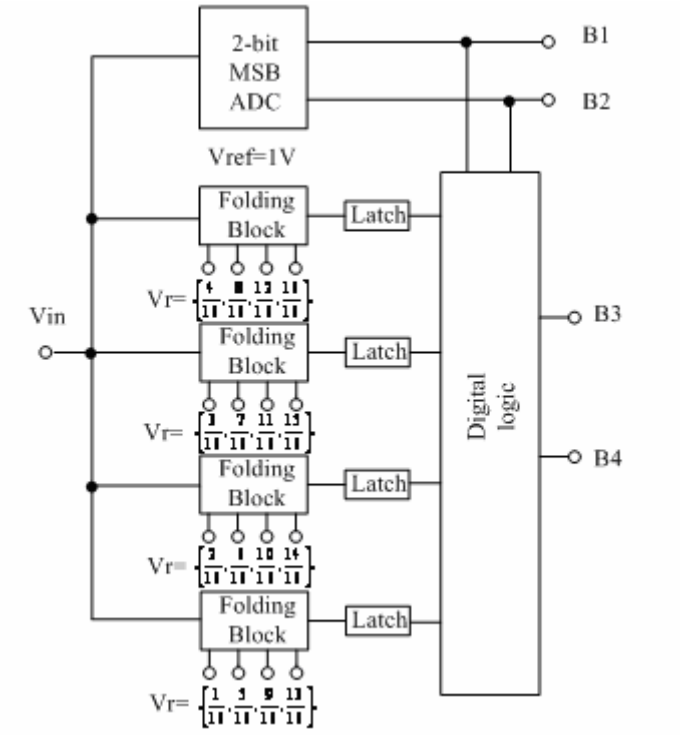


Figure 2.17 Example of a 4-bit folding ADC.

While the folding approach reduces the number of latch comparators, a large input capacitance similar to that for a flash converter is also present with the folding circuit shown. To reduce this large input capacitance, folding converters also make use of an interpolating architecture as shown in figure 2.18 [3].

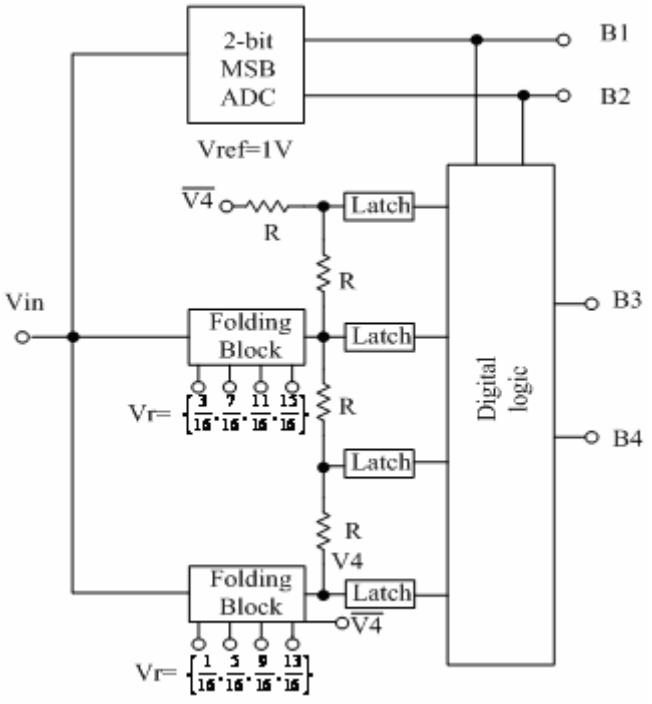


Figure 2.18 Example of a 4-bit folding ADC with an interpolating architecture.

2.3.8 Pipelined ADC

The pipeline ADC is the extension of the two-step structure. The conversion is divided into several stages with each stage generating a certain number of digital bits. The general block diagram is shown in Figure 2.19. There are M stages and the *ith* stage generates Ni digits. If no redundancy is used, the sum of Ni equals to m, the resolution of ADC. All stages operate concurrently. When a stage works on the current sample, the next stage processes the previous one. The nature of concurrence makes the throughput of the converter independent of its resolution, and the same as for a flash ADC. The hardware increases linearly with the increase of resolution, compared to the flash structure. The disadvantage of this structure is the large latency time between valid digital output and the analog input signal. In some applications, such as data recovery in the Local Area Network (LAN) and disk drive read/write channels, the ADC is inside a feedback loop. Excessive latency will make the loop unstable. For most video applications, latency is not an issue [3] [15].

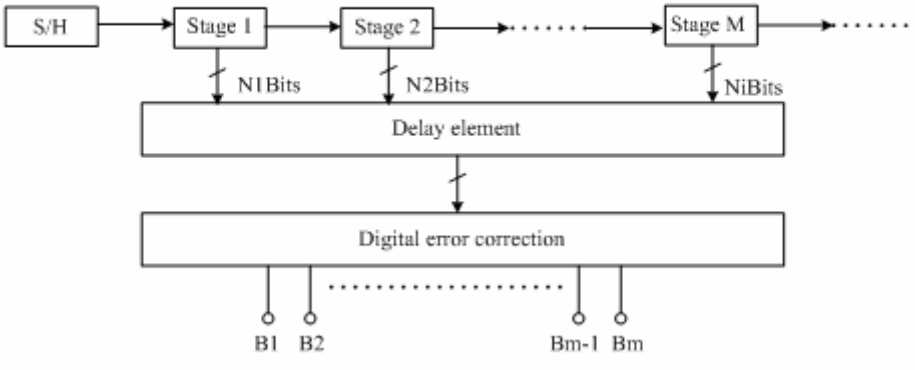


Figure 2.19 Block diagram of an m-bit pipelined ADC

The pipelined ADC has become the most popular ADC architecture for sampling rates from a few megasamples per second (MS/s) up to 100MS/s+, with resolutions from 8 to 16 bits. They offer the resolution and sampling rate to cover a wide range of applications, including CCD imaging, ultrasonic medical imaging, digital receiver, base station, digital video (for example, HDTV), xDSL, cable modem, and fast Ethernet.

2.3.9 Time-interleaved ADC

Very-high-speed ADC conversions can be realized by operating many ADC in parallel. The system architecture for a four-channel ADC is shown in Figure 2.20. Here, ϕ_0 is a clock at four times the rate of ϕ_1 to ϕ_4. Additionally, ϕ_1 to ϕ_4 are delayed with respect to each other by the period of ϕ_0, such that each converter will get successive samples of the input signal, Vin, sampled at the rate of ϕ_0. In this way, the four ADC operate at one-quarter the rate of the input sampling frequency [3].

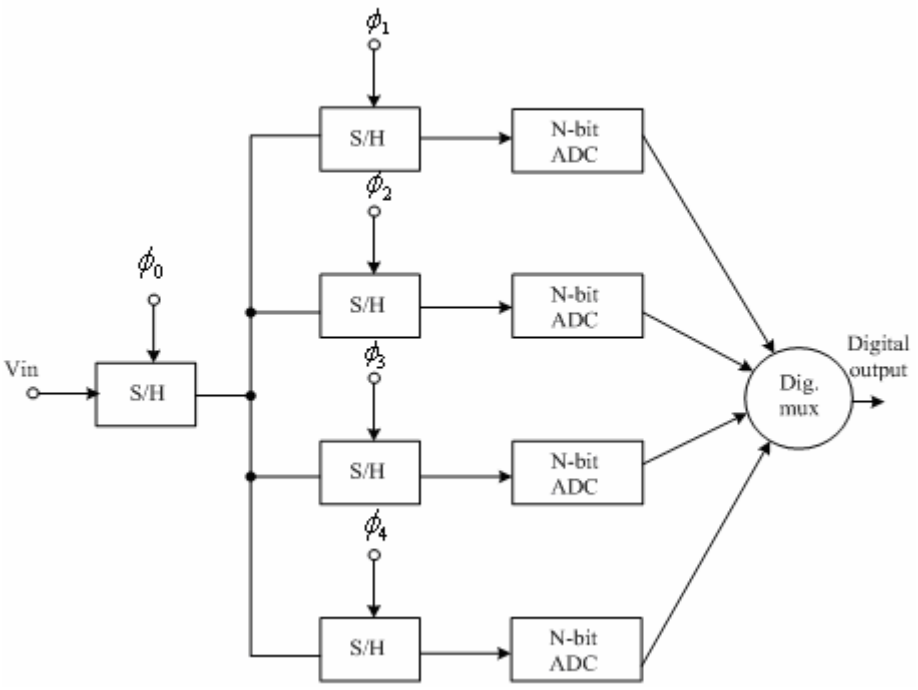


Figure 2.20 A four-channel time-interleaved ADC

2.4 SUMMARY

All advantages and disadvantages of ADC introduced above are summarized in Table 2.3. The target specification of 10-bit 40MSPS ADC is required. The high speed group includes flash, interpolating, folding and pipelined techniques are capable to reach the specification. However, the flash and interpolating architectures cost large percentage of passive components, so we don't adopt them. Therefore, the Folding and pipelined are the most suitable architectures. From the view point of disadvantages, the pipelined architecture has large latency. In many applications, the large latency is not an issue. However, the large capacitance of the folding ADC may increase the loading of the front-end circuit, especially when time interleave technique is adopted. On the other hand, from the view point of advantages, error correction of the pipelined ADC is useful because the process variations may degrade the performance and it can correct the related errors. As discusses above, the pipelined

architecture is adopted.

Table 2.3 The comparisons of ADC architectures [16].

Architectures	Advantages	Disadvantages
SAR	Medium resolution Easy to implement	S/H and DAC required
Integrating	No matching problem High resolution Easy to implement	Very low speed
Flash	Very high speed No latency	High input capacitance Large comparator numbers
Interpolating	Very high speed No latency Less comparators	More resistor required Linear comparator required
Folding	Very high speed No latency Less latches	High input capacitance
Pipelined	Very high speed Error corrections possible Low input capacitance	Large latency
Algorithmic	Error correction possible Low input capacitance Small area and power	Medium speed
Sigma-delta	Very high resolution Process variation insensitive	Low speed
Time-interleaved	Ultra high speed	Large area and power Clock jitter and process variation sensitive

Chapter 3
Architecture of Pipelined Analog-to-Digital Converter

3.1 Overview

In the previous chapter, several high speed architectures are introduced. We adopted pipelined architecture to realize a 10-bit 40MSPS ADC with many considerations. In this chapter, the focus will be the system structure and the operations of the pipelined architecture. The error sources of a switched capacitor (SC) pipeline stage and their effect on the ADC performance are compiled and the design constraints of the pipeline ADC presented

3.2 Basic Pipelined Architecture

The block diagram of the pipelined ADC is introduced in section 2.3.8. The front-end sample-and-hold (S/H) block takes samples of its analog input signal and holds these samples in a memory element. The key feature of this circuit, when used as the front-end of an ADC, is that it relaxes the timing requirements of the latter. This means that the precision and speed of the converter will be limited to a certain degree by the S/H circuit.

The operation of an S/H circuit is divided into two modes, sample and hold. Usually this is done at uniform time intervals, set by a periodic clock that divides circuit operation into two phases. During the sample-mode the output of the circuit can either track the input or reset to some fixed value. In the hold-mode, the output of

the S/H circuit is equal to the input value obtained (sampled) at the end of the sample mode. Figures 3.1 (a) and (b) illustrate example waveforms for an S/H circuit and a T/H (track-and-hold) circuit. Although here a distinction was made between sampling and tracking, the majority of the circuits are referred to as S/H circuits even though they behave as T/H circuits.

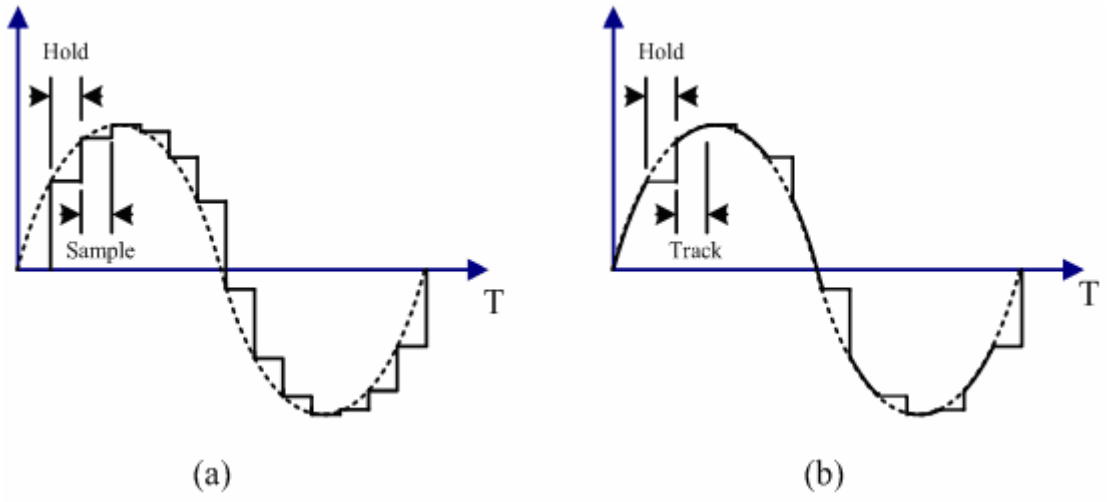


Figure 3.1 (a) S/H circuit and (b) T/H circuit output waveforms.

The most basic form of an S/H circuit combines a switch and a capacitor, as shown in Figure 3.2. The operation of the circuit proceeds as follows. In sampling mode the switch is "on", creating a signal path that allows the capacitor to track the input voltage. When the switch is "off" an open circuit is created that isolates the capacitor from the input, hence changing the circuit from sampling mode into holding mode.

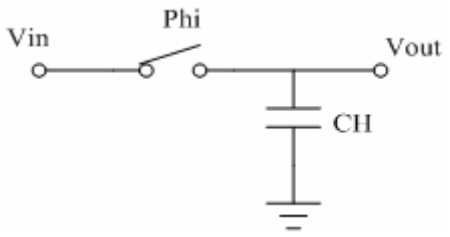


Figure 3.2 Simple sample-and-hold circuit.

Figure 3.3 shows one stage of the pipelined architecture. Each stage comprises a low-resolution sub-analog-to-digital converter (sub-ADC) and an arithmetic unit called the multiplying digital-to-analog converter (MDAC) that performs a sample-and-hold (S/H) operation, coarse D/A conversion, subtraction, and amplification. In operation, each stage performs an A/D conversion of *Bi* effective bits with *r*-bit redundancy, converts the digital output back to analog and subtracts it from the sampled and held analog input. This residue is amplified with a gain of

$$G\,i\;=\;2^{\,Bi+1-r} \tag{3.1}$$

and fed to the next stage. The stages operate concurrently; that is, at any time, the first stage operates on the most recent sample while all other stages operate on residues from previous samples. Serial stages operate in opposite clock phases. The digital outputs of the stages $B1+r....B_k+r_k$ are delayed so that their values correspond to the same input sample.

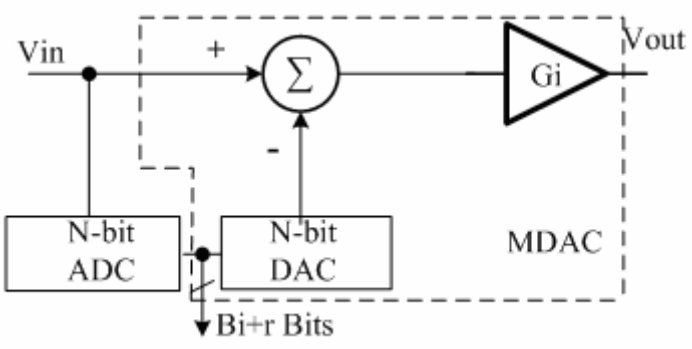


Figure 3.3 Block diagram of one pipeline stage

The analog transfer function of a *Bi*+*r*-bit pipeline stage follows the equation

$$Vout,i = GiVin,i+DiVref \tag{3.2}$$

where *Di* is an integer, the value of which is dependent on the output of the sub-ADC and $Di \in \left[-(2Bi-1),+(2Bi-1)\right]$ with a step of 2 when r = 0 and 1 otherwise. The other terms *Gi* and *Vin*,*i* and the addition in Equation 3.2 are provided by the MDAC [17].

3.2.1 Per-Stage Resolution

The pipelined ADC architecture allows a designer flexibility in the choice of sub-ADC resolution for each stage. As such, the most common implementation of the pipelined ADC is a 1.5 bits-per-stage structure. The reduction in stage resolution allows for very fast conversion times and small power consumptions. This is due to the relaxed requirement of the sub-ADC, and is most effective in designs for low-to-medium resolution.

The most other pipelined ADCs fall into a class of pipelines known as multi-bit pipeline ADCs. These are pipelines with greater than 1.5 bits-per-stage sub-ADC resolution, and are most useful in design situations requiring large overall ADC resolutions. The advantage of a multi-bit pipeline is the large gain at output of the first MDAC – noise power contributions of all following stages are reduced by the squared MDAC gain. High-resolution designs place stringent requirements on the ADC noise and the size and power consumption of the back-end stages can be decreased effectively with the large gain from a multi-bit stage. The aggressive scaling leaves more budgeted power and area available for the critical initial stages of the pipeline.

Therefore, the resolution of 1.5-bits-per-stage is adopted mainly for the following reasons [3] [17] [18] [19]:

1. The bandwidth of the SC circuit stage which limits the overall conversion rate can be maximized.

2. Because the code 11 is never occurred, the number of the required levels in the DAC is reduced by one. It makes sub-DAC faster and less sensitive to capacitor ratio error than conventional counterpart.
3. The design of error correction circuits and control logic is simpler, and the number of comparators in sub-ADC is minimized.
4. The smaller inter-stage gain, which equal to 2, makes faster settling, so the bandwidth can be maximized for high-speed operation.
5. The power consumption can be reduced for high speed operation.

3.2.2 Digital Error Correction

In order to illustrate the algorithm behind digital correction, a 2-bit pipeline stage is presented here as an example. Figure 3.4 shows the ideal transfer function of 2-bit pipeline stage whose block diagram is shown on the left. When the input crosses one of the sub-ADC decision levels, the digital output for the stage is increased by one bit, whereas the stage output decreases by 2 Vref's. With the inter-stage gain of 4, the signal presented to the next stage is the full scale and does not allow any tolerance for errors in sub-ADC and sub-DAC.

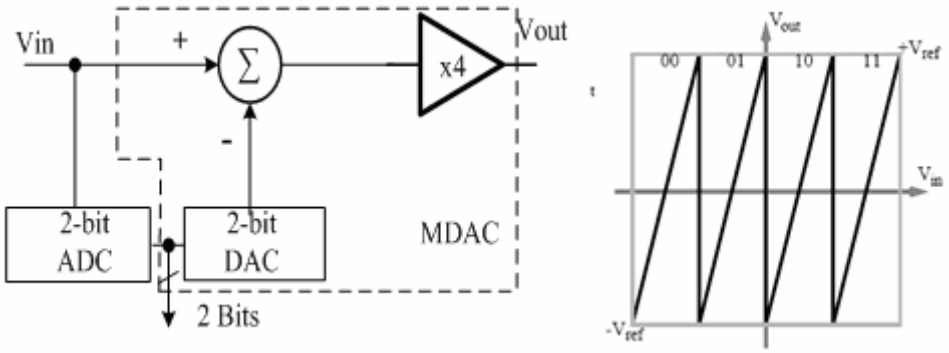


Figure 3.4 Ideal transfer function of a 2-bit pipelined stage.

When an offset occurs in the sub-ADC or sub-DAC, the output of the first stage will exceed the range bounded by $\pm Vref$ as shown in Figure 3.5. This will saturate the second stage and cause missing information. To eliminate this problem, one can increase the range of the second stage sub-ADC or equivalently reduce the inter-stage gain of the first stage to tolerate sub-ADC error.

When the inter-stage gain is reduced to 2, the transfer function becomes Figure 3.6. This allows the sub-ADC error to be as large as $\frac{1}{4}Vref$ and the output is still in the input range of the following stage. However, when a sub-ADC error is present without digital correction, the error will appear in the final digital output. In another words, if digital correction is not used, the first stage sub-ADC must still be as linear as the entire converter. Whereas the later stages, because of inter-stage gain, the requirements can be relaxed. Now, assume the first stage is ideal, with a full scale input to the first stage, the output is only between $-\frac{1}{2}Vref$ and $\frac{1}{2}Vref$, leaving an extra bit on top and bottom of the per-stage resolution. Digital correction simply utilizes the extra bit to correct the overranging section from the previous stage.

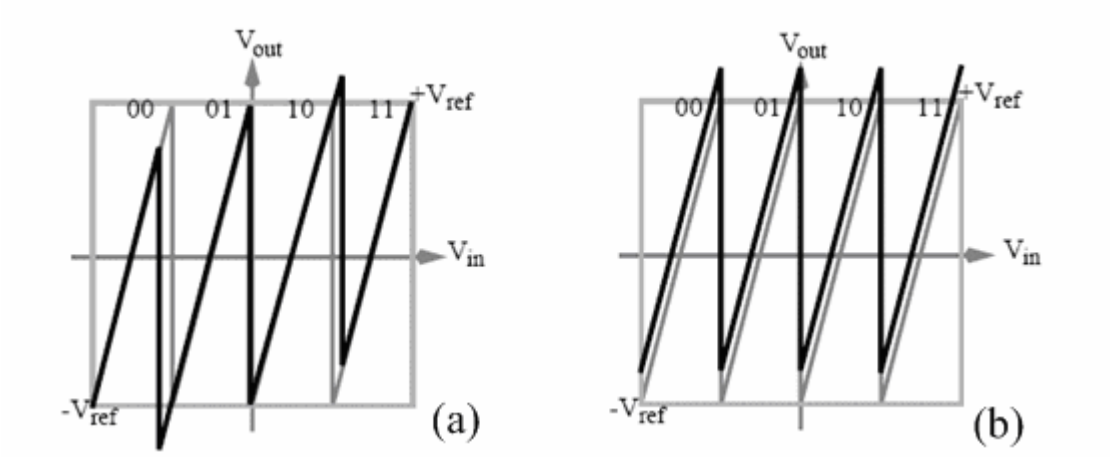


Figure 3.5 Transfer function with sub-ADC error (a) and sub-DAC error (b).

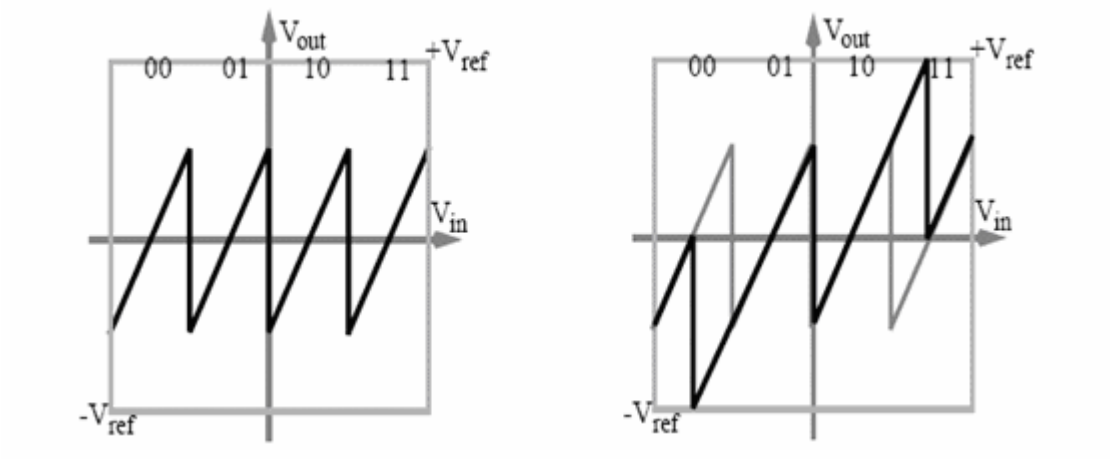


Figure 3.6 Transfer function of inter-stage gain of 2 and sub-ADC error.

For example, when one of the sub-ADC thresholds has an offset, the output of the first stage will exceeds $\frac{1}{2}Vref$. The second stage, sensing the overranging, will increase the output by one LSB. This bit will cause the first stage output to increase by one LSB during the digital correction cycle. In the same way, when the output of the first stage drops below $-\frac{1}{2}Vref$, the second stage will sense the overranging and subtract one LSB during digital correction cycle. With this method, the sub-ADC error, as large as $\frac{1}{4}Vref$, in the stage can be corrected by the following stage with digital correction.

With the above digital correction algorithm, both addition and subtraction need to be present in the digital correction circuit which complicates the code assignment for the pipeline stage. Subtraction can be eliminated by intentionally adding an $-\frac{1}{4}Vref$ offset to the sub-ADC and the output of sub-DAC. A conceptual block diagram and transfer function is shown in Figure 3.7. With this configuration, the sub-ADC error, up to $\frac{1}{4}Vref$, can be tolerated and digital correction circuit is modified to contain adders only.

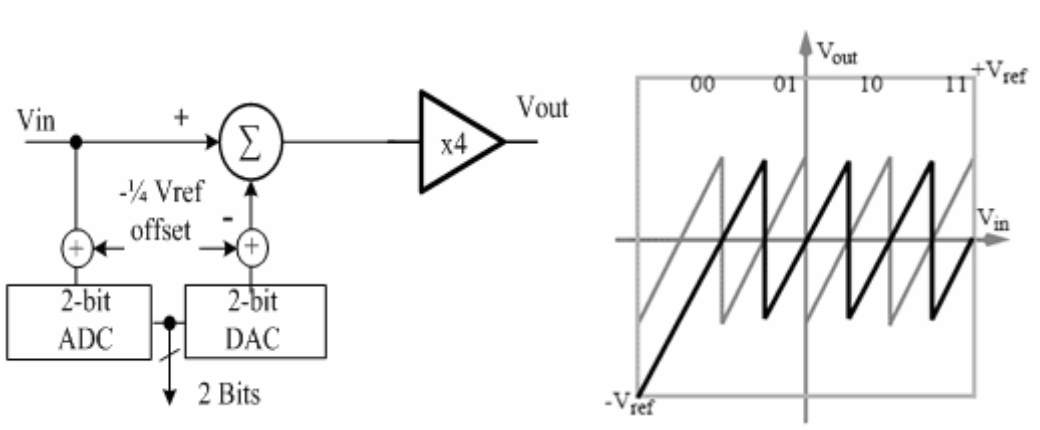


Figure 3.7 Conceptual Block Diagram of Modified Pipeline Stage and Coding.

Since overranging in the transfer function can be detected by the next stage, one can simplify the design even more by eliminating a comparator at $\frac{3}{4}Vref$. The final block diagram and transfer function is shown in Figure 3.8. The comparator thresholds (sub-ADC) are at $-\frac{1}{4}Vref$ and $\frac{1}{4}Vref$; the sub-DAC levels are at $-\frac{1}{2}Vref$, 0 and $\frac{1}{2}Vref$. The codes are shown on top of the transfer function and the overranging part on the transfer function will be digitally corrected by the next stage except the last stage of the pipeline. The 1.5-bit ADC and DAC here represent the effective bits per stage after digital correction [20] [21].

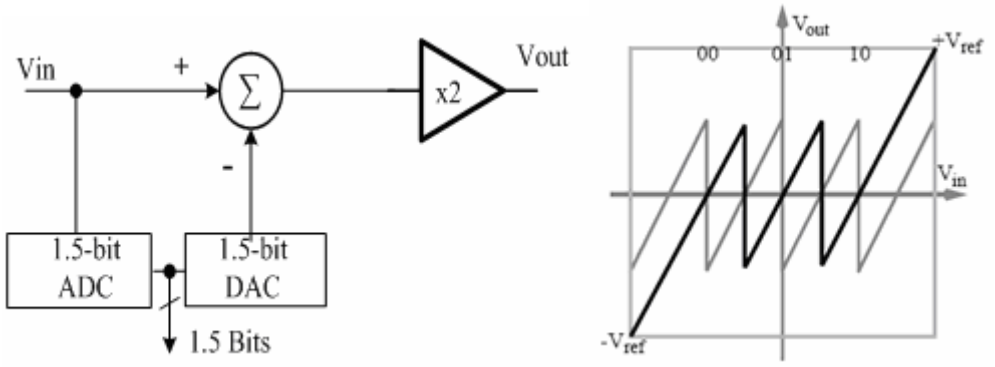


Figure 3.8 Conceptual Block Diagram of Modified Pipeline Stage and Coding.

3.3 ERROR SOURCE OF PIPELINED STAGE

Pipeline Analog-to-Digital data converters have many potential error sources – many of them are the same error sources found in other ADCs. There is, however, a fundamental difference in how the error sources appear in the final converted signal for pipelined ADCs. The segmented nature of the Pipeline ADC is very helpful in addressing power and speed concerns, but complicates understanding and reduction of error propagation from stage to stage. Simple errors in Pipeline ADCs produce non-linearities that are difficult to correct. Much effort has therefore been spent on understanding these errors [3] [17] [22] [23] and finding means of reducing them [24] [25] [26].

3.3.1 Offset Error

Offset errors are simple additive errors that can be modeled as an error constant summed with the signal. Offset error in ADC can be compensated by the digital error correction generally. This is not only for pipelined ADCs but also the other architectures of ADC. Offsets that occurs mid-pipeline can create significant non-linearities; this necessitates special design techniques and careful design to reduce the amount of signal offset present in the pipeline. Common offset sources in pipelined ADCs are charge injection, comparator offsets, operational amplifier offset.

- *Charge Injection*

Charge injection is a general term for when circuit components that add inadvertent charge. The most common source of charge injection in switched-capacitor circuits is “orphaned” charge originating from the inversion layer when a MOSFET switch is turned off. Charge injection offset can be mitigated with careful design. There are also several “tricks” often used to reduce this offset

including early-clocking, dummy switches, and complimentary switches [3].

- *Comparator Offset*

The main error source of the sub-quantization in a pipeline stage is the offset voltage of the comparators. An offset voltage shifts the decision level of the comparator introducing a quantization error to the *Bi*+*r*-bit output the stage. The effect of the threshold level shifting on the transfer function of a 1.5-bit stage is present in Figure 3.9, where the non-zero comparator offset voltage are assumed to be the only non-idealities present.

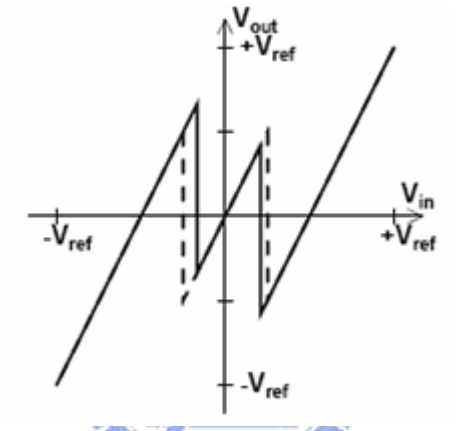


Figure 3.9 Effect of the comparator offset on the transfer function of a 1.5-bit stage.

The comparator offset voltage is originated from several reasons. The main component is inherited from the device mismatch, the combined effect of which can be reduced into the comparator input. Deviation in the reference voltage levels $\triangle Vref$ can be also included in the input referred offset voltage. If no redundancy is exploited, the error in the output voltage of each stage must be less then half of the LSB referred to the resolution of the remaining back-end pipelined ADC. The maximal error allowed in the output of the *mth* stage is given by

$$\Delta V_{out,m} = \frac{1}{2} \cdot \frac{1}{2^{N-\sum_{i=1}^{m-1} B_i}} \cdot V_{FS} \tag{3.3}$$

where $V_{FS} = 2Vref$ is the full scale output voltage. Referred to the stage input, the maximal allowed comparator input referred offset is given by

$$\Delta V_{os,c,m} = \frac{1}{2^{N+B_m-\sum_{i=1}^{m-1} B_i}} \cdot V_{ref} \tag{3.4}$$

When the digital error correction with one-bit redundancy is employed, the comparator offset requirement is described in section 3.2.2, the value of which is much larger than Equation 3.3 and furthermore, independent of the order of the stage.

- *Operational Amplifier Offset*

The operational amplifier offset voltage introduces a constant error of *Vos*, which is directly translated to an equal, constant shift of the output voltage *Vout* as depicted for a negative offset of a 1.5-bit stage in Figure 3.10. The shift can cause the stage output to overflow and saturate the remaining pipeline stages. The effect of this offset voltage can be minimized by using well known circuit techniques like auto-zeroing, i.e. connecting the amplifier in unity gain feedback during the sample phase, or measuring and compensating the offset analogically or digitally.

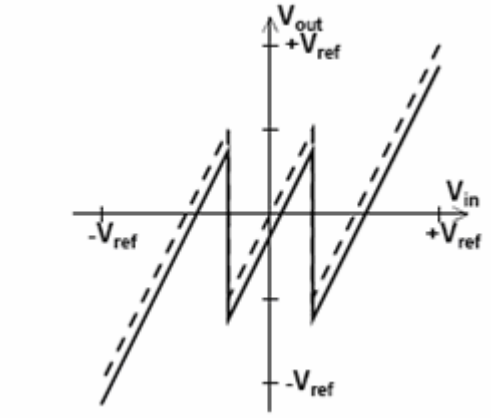


Figure 3.10 Effect of the amplifier offset on the transfer function of a 1.5-bit stage.

3.3.2 Gain Error

Gain error is a multiplicative error that acts on the input signal. It can be modeled as a gain stage where a gain of one is the optimal gain value. Like offset error, gain error on the system level is a fairly simple error to correct. Also, just like offset error within pipelined stages, gain errors can create difficult-to-remove non-linear errors.

The most common gain error sources are finite operational amplifier gain error and feedback capacitor to MDAC capacitor mismatch.

- *Operational Amplifier Gain Error*

The errors result from the finite operational amplifier open loop DC-gain error A_0, which is given in this case by $A_0 = gm \cdot ro$, and from the parasitic input capacitance C_p, which changes the feedback factor. Figure 3.11 shows the structure of the MDAC. For the general unit capacitor MDAC of Figure 3.11, omitting all non-linearities other than the finite open loop DC-gain A_0, it can be written on the charge preservation in the sample and hold mode

$$V_{in}\left(C_f + C_s\right) = V_{out}\left(\left(1+\frac{1}{A_0}\right)\cdot C_f + \frac{C_s}{A_0} + \frac{C_p}{A_0}\right) + V_{ref}\left(m \cdot C_s\right) \tag{3.5}$$

Solving for V_{out} yields

$$V_{out} = \left(\frac{C_f + C_s}{C_f}V_{in} - \frac{m \cdot C_s}{C_f}V_{ref}\right)\cdot\frac{1}{1+\frac{1}{A_0 \cdot f}} \tag{3.6}$$

where the m is a constant multiplier equal to -1, 0 or +1 depending on the output of the sub-ADC, the parameter f is called the feedback factor and is given by

$$f = \frac{C_f}{C_f + C_s + C_p} \tag{3.7}$$

The effect of the amplifier parasitic input capacitance on the feedback factor is also manifested in Equation 3.7. By comparing Equation 3.6 to the ideal transfer function

$$V_{out} = \frac{C_f + C_s}{C_f} V_{in} - \frac{m \cdot C_s}{C_f} V_{ref} \tag{3.8}$$

it can be observed that the error introduced by the amplifier finite open loop DC-gain is given the last term in Equation 3.6, for which, when $\frac{1}{A_0 \cdot f} \ll 1$, the Equation 3.6 is approximately

$$V_{out} = \left(\frac{C_f + C_s}{C_f} V_{in} - \frac{m \cdot C_s}{C_f} V_{ref} \right) \cdot \left(1 - \frac{1}{A_0 \cdot f} \right) \tag{3.9}$$

thus, the amplifier finite DC-gain decrease the gain and steps at the comparator thresholds in the transfer function by an error term ε of

$$\varepsilon = \frac{1}{A_0 \cdot f} \tag{3.10}$$

The effect of the resulting signal-dependent gain error introduced to the transfer function of a 1.5-bit stage is depicted exaggeratedly by the solid line in Figure 3.12.

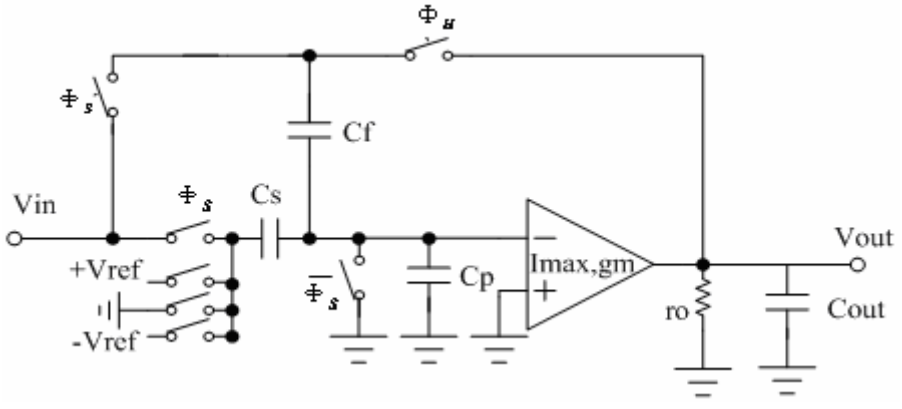


Figure 3.11 The structure of the MDAC

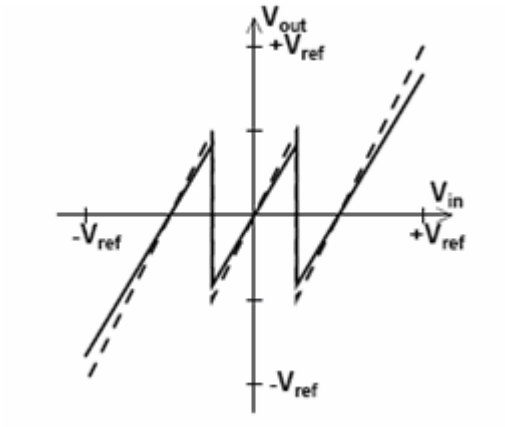


Figure 3.12 Effect of the finite amplifier DC-gain on the transfer function of a 1.5-bit stage.

- *MDAC Capacitor Mismatch*

In switched capacitor MDACs, mismatch of the sampling C_s and feedback C_f capacitors is the major error source. Each of the capacitor can be modeled to consist of an ideal part C_s and C_f plus a mismatch ΔC_s and ΔC_f, respectively, corresponding to the Figure 3.13.

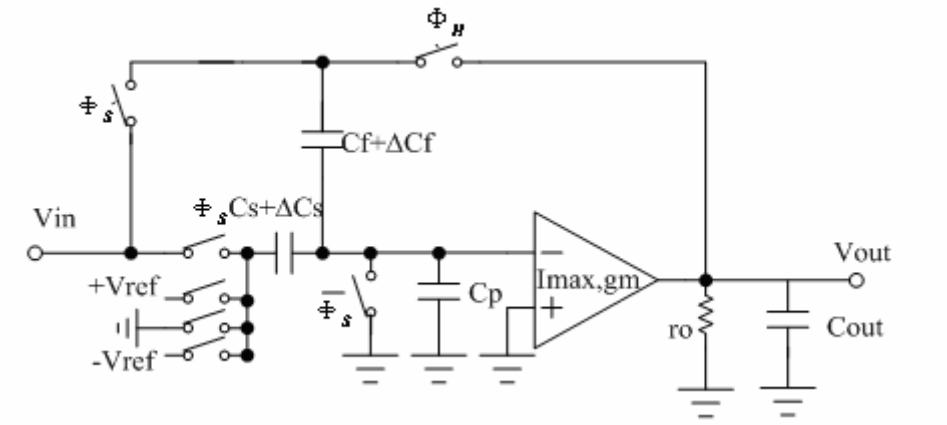


Figure 3.13 The structure of the MDAC with the capacitor mismatch.

Including the capacitor mismatch in the transfer function of a switched capacitor MDAC in Equation 3.8, results in

$$V_{out} = \frac{C_f + \triangle C_f + C_s + \triangle C_s}{C_f + \triangle C_f} V_{in} - \frac{m \cdot (C_s + \triangle C_s)}{C_f + \triangle C_f} V_{ref} \tag{3.11}$$

The multiplier of the input Vin represents a gain error, while the multiplier of the second term introduces an error in the height of the voltage steps at the comparator threshold levels. For the unit capacitor MDAC, by exploiting the property $C_s = C_f = C$, Equation 3.11 can be written as

$$V_{out} = \left(1 + \left(1 + \alpha\right)\right) V_{in} - \left(1 + \alpha\right) V_{ref} \tag{3.12}$$

where for the unit capacitor mismatch α holds

$$1 + \alpha = \frac{C + \triangle C_s}{C + \triangle C_f} = \frac{1 + \frac{\triangle C_s}{C}}{1 + \frac{\triangle C_s}{C}} \tag{3.13}$$

The effect of the capacitor mismatch on the stage transfer function is depicted in Figure 3.14. For a 1.5-bit stage, it is noticed that when Vin = ±Vref, there are no errors result. The gain error and the deviation of the voltage steps at the comparator threshold levels are clearly visible from the figure.

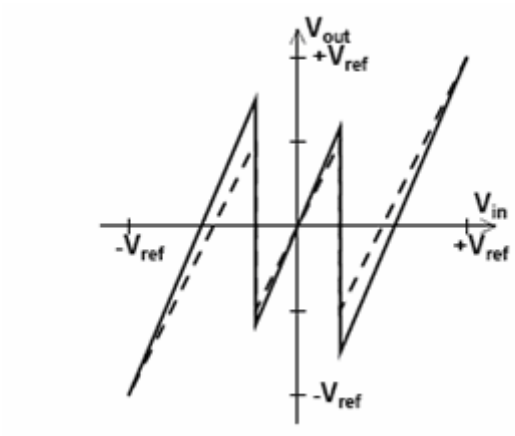


Figure 3.14 Effect of the capacitor mismatch on the transfer function of a 1.5-bit stage.

- *Other Gain Error*

The other gain error source not usually a concern for pipelined ADCs is reference mismatch from stage and stage. Generally the voltage is a very-low impedance signal that is sent to each stage of the pipeline. The reference mismatch is almost negligible.

3.3.3 Slew Rate and Gain Bandwidth Error

A more severe dynamic error in the stage transfer function is caused by the incomplete settling of the operational amplifier output. This error is introduced by the finite slew rate (SR) and gain bandwidth of the operational amplifier. At the beginning of the hold mode, the operational amplifier enters slewing, providing its maximal output current *Imax*, after which it settles exponentially towards the ideal stage output voltage, the settling now being limited by the amplifier transconductance *gm* and the effective load capacitance in this mode $C_{L,H}$. For the slew rate limited part of the settling, it is a good practice to reserve one third of the total settling time of *T*=2, where *T* is the sample clock period, relating to the sample frequency by $f_s = \frac{1}{T}$. The load capacitance, which has to be charged or discharged during the settling, depends on the capacitor charging in the previous sample phase. In the worst case, the total load capacitance during the slewing is $C_{L,total} + C_f$, resulting

$$SR = \frac{I_{\max}}{C_{L,total} + C_f} \tag{3.14}$$

where $C_{L,total} + C_f$ is the total load capacitance including the parasitic capacitance at the amplifier output C_{out}. The stage output voltage is linearly dependent on the slew rate and at the end of this phase given by

$$V_{out}\left(\frac{T}{6}\right)=\frac{SR}{6fs} \tag{3.15}$$

During the exponential settling, the stage output approaches the ideal output $V_{out,ideal}$ according to the equation

$$V_{out}(t)=\left(1-e^{-\omega_{-3dB}t}\right)\cdot V_{out,ideal} \tag{3.16}$$

where the -3dB corner frequency is given by

$$\omega_{-3dB}=\omega_u\cdot f=\frac{gm}{C_{L,H}}\cdot f \tag{3.17}$$

The effective hold mode load capacitance $C_{L,H}$ of the MDAC in Figure 3.11 with a load capacitance C_L is given by

$$C_{L,H}=C_L+C_{out}+\frac{C_f\left(C_s+C_p\right)}{C_f+C_s+C_p} \tag{3.18}$$

From Equation 3.16 – 3.18, the -3dB corner frequency is

$$\omega_{-3dB}=\frac{gm}{\frac{C_{L,total}}{f}+C_s+C_p} \tag{3.19}$$

As the slewing took one third of the settling time, the remaining time for the exponential settling is $t=\frac{T}{3}=\frac{1}{3}fs$. Substituting Equation 3.19 into Equation 3.16 the settling error of the stage output voltage at the end of the hold phase ε_τ can be derived to be

$$\varepsilon_\tau=e^{-\frac{gm}{\frac{C_{L,total}}{f}+C_s+C_p}\cdot\frac{1}{3fs}} \tag{3.20}$$

The settling error ε_τ, being time dependent, creates signal-dependent errors,

which in turn leads to harmonic distortion. Signal-dependent errors are very difficult to cancel or calibrate, which makes the consideration of the amplifier settling behavior very important. The effect of the finite gain bandwidth of the amplifier on the transfer function of a 1.5-bit stage is depicted in Figure 3.15. The error is proportional to the output voltage being larger for stage outputs close to the full scale, which is not the case in the error originated from the amplifier finite gain depicted in Figure 3.12.

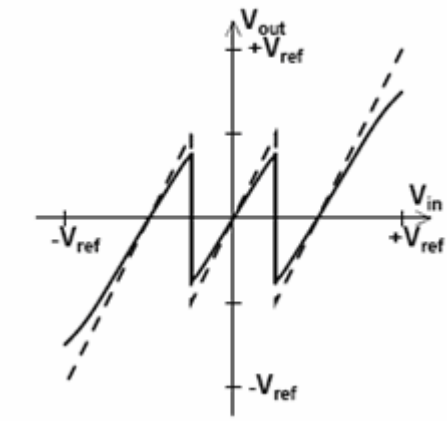


Figure 3.15 Effect of the amplifier gain bandwidth on the transfer function of 1.5-bit stage.

3.3.4 Non-linear Error

Linearity is simply defined as a property of a system whereby the input-to-output characteristic is wholly linear and can be described in the form $y_0 = mx_0 + b$. Earlier discussions in this chapter have discussed how simple error sources such as offset error and gain error can contribute to the system non-linearity. There are also some error sources in Pipeline ADCs that are inherently non-linear. These are operational amplifier output non-linearity, signal-dependant switch resistance, and non-linear capacitance.

- *Operational Amplifier Output Non-linearity*

Operational amplifier non-linearity comes from the open-loop gain dependant on output level. Operational amplifier output stages have a heavily gain dependant output impedance and therefore a signal-dependant open-loop gain. It can be further inferred that the closed-loop characteristics are also affected by this signal-dependence. The most common design approach to this problem is to provide enough open-loop gain over the expected output range to keep the non-linear effects of the signal-dependant gain in the noise of the data converter.

- *Signal-dependant Switch Resistance*

In switched capacitor circuits, almost without exception, MOS switches are used. The non-idealities and error sources attached to them deserve careful consideration when designing SC MDACs. There are two commonly accepted methods for reducing this error. The first is by use of complimentary switches utilizing both NMOS and PMOS devices. The second method for reducing non-linear switch resistance is known as "bootstrapping". This circuit method maintains a constant V_{GS} on the floating sampling switch during the sampling phase and can greatly improve the switch linearity, and it will describe briefly in next chapter.

- *Non-linear Capacitance*

Portions of parasitic capacitance within circuit devices are often non-linear. A common source of this non-linearity is depletion region width dependencies on signal voltage. This is most often present at the P-N junctions located at the source and drain nodes of MOSFET devices but can also exist in some types of capacitor devices.

3.3.5 Thermal Noise

In addition to the deterministic errors limiting the performance of a pipeline ADC, there are random errors originated from noise of the circuit elements and clock

signals. In switched capacitor pipeline ADCs, the dominating thermal noise components are the noise of the operational amplifiers and sampling circuit, latter of which being the dominating source in medium- and low-resolution applications. The noise of the sampling circuit is called kT/C-noise since the thermal noise of the sampling switch is stored to the sampling capacitor resulting in a noise power of

$$e_{kT/C}^2 = \frac{kT}{C_f + C_s} \tag{3.21}$$

where k is the Boltzmann's constant, T absolute temperature, and the total sampling capacitance consists of the feedback capacitor C_f and sampling capacitor C_s.

This holds for, for example, the MDACs of Figure 3.11. Considering the kT/C-noise as the only noise source, the signal-to-noise ratio of one stage for a sinusoidal signal with full-scale amplitude of $V_{FS}/2$ is given by

$$SNR_{kT/C} = \frac{V_{FS}\left(C_f + C_s\right)}{8kT} \tag{3.22}$$

Especially in high-resolution pipeline A/D converters, the total kT/C-noise contribution of all the MDACs of a pipeline ADC determine the minimum size of the capacitors and full-scale voltage which does not degrade the SNR below the quantization noise level..

The noise of the operational amplifiers of the SC MDACs must also be taken into account in the design. The thermal noise of an amplifier is dependent on the circuit topology and can be considered separately superimposed on the kT/C-noise.

3.3.6 Sampling Clock Jitter

The most critical clocking signal in the S/H is the sampling clock, the falling edge of which determines the sampling moment. Random variations of the falling

edge, referred as clock jitter or aperture uncertainty σ_a, are unavoidable. Because of its random nature, the sampling clock jitter does not introduce any fixed pattern tones in the output spectrum but degrades the signal-to-noise ratio.

Figure 3.16 shows the example of the aperture uncertainty error. The effect of the aperture uncertainty comes about because an ADC does not sample the input at precisely equal time-intervals $T_s = \frac{1}{fs}$. The sampling process is random-like and can be characterized by a mean and standard deviation with regard to the location in time of when sampling occurs. The mean is the average position of the sampling instant and the standard deviation is defined as the rms aperture jitter σ_a. The worst-case voltage error due to the aperture jitter corresponds to sampling a sinusoidal waveform with the Nyquist-rate frequency, which is $fs/2$, i.e. a full-scale signal

$$v(t) = \frac{V_{FS}}{2}\sin(2\pi \cdot fs \cdot t) \tag{3.23}$$

The maximum error will occur when attempting to sample the signal $v(t)$ at its zero-crossing, where its derivative gives the maximum slope of the signal

$$\frac{dv(0)}{dt} = \pi \cdot fs \cdot V_{FS} \tag{3.24}$$

The maximum rms voltage error is given by the product of Equation 3.24 and the aperture uncertainty.

$$v_{rms} = \pi \cdot fs \cdot V_{FS} \cdot \sigma_a \tag{3.25}$$

which corresponds to an output noise power of

$$e_{\sigma_a}^2 = \frac{v_{rms}^2}{2} = \frac{\pi^2 \cdot V_{FS}^2 \cdot fs^2 \cdot \sigma_a^2}{2} \tag{3.26}$$

which adds to the quantization noise and degrades the SNR.

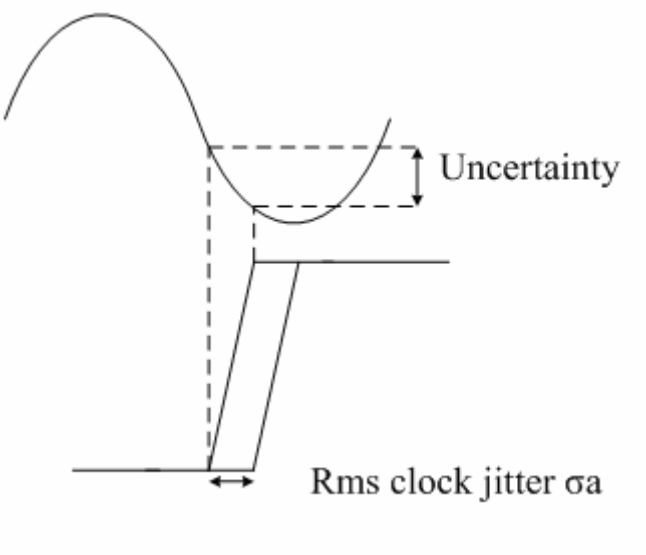


Figure 3.16 Example of the aperture uncertainty error.

In the back-end pipeline stages, which have an almost constant exponentially settling output of the previous stage as their input, the sampling clock jitter is of much less importance than in the first stage. The time varying output of a pipeline stage is given by Equations 3.16-3.19, the derivative of which is given by

$$\frac{d}{dt}V_{out}(t) = -\frac{gm}{\frac{C_{L,total}}{f}+C_s+C_p}\cdot e^{-\frac{gm}{\frac{C_{L,total}}{f}+C_s+C_p}\cdot t}\cdot V_{out,ideal} \tag{3.27}$$

Rms voltage error at the sampling moment of stage *i*, which is at the end of the hold phase of stage *i*-1, i.e. $t=\frac{1}{3fs}$, can be obtained similarly as above to be

$$v_{rms,a} = \frac{d}{dt}V_{out,i-1}\left(\frac{1}{3fs}\right)\cdot\sigma_a \tag{3.28}$$

The corresponding noise power being

$$e_{\sigma_a}^2 = \frac{1}{2}\left(\frac{gm \cdot \sigma_a}{\frac{C_{L,total}}{f} + C_s + C_p}\right)^2 \cdot e^{-\frac{2gm}{\frac{C_{L,total}}{f}+C_s+C_p} \cdot \frac{1}{3fs}} \tag{3.29}$$

The noise contribution of Equation 3.29 is usually much below that of Equation 3.26.

Chapter 4

Circuits Design

4.1 Overview

The Analog-to-Digital converter designed here is a 10-bit 40MS/s pipelined ADC. The entire analog and digital circuits are designed for 3.3V power supply. The full scale input voltage is from -1V to 1V. And all analog circuits are fully differential; include the switches, sample-and-hold, operational amplifier, MDAC, flash type quantizer, and comparators. The digital circuits contain the clock generator, digital error correction. In this chapter, all the circuits will be discussed in detail.

4.2 Input Stage Sample-and-Hold

The conversion process of a pipelined ADC begins at the S/H circuit. Figure 4.1 shows the unity-gain S/H circuit used for this work. The analog signal is applied to the terminals Vin+ and Vin- and the held output is taken at the terminals Vout+ and Vout- . The signal ground COM is the common-mode voltage of the output differential signal. Because the architecture of the operational amplifier is a telescopic amplifier, which has a lower input DC level, the node COMI is for input common-mode voltage. It is different from the output common-mode voltage COM Although the charge stored in the capacitor from different path are not the sane quantity, the input and output voltage signals are not affected apparent.

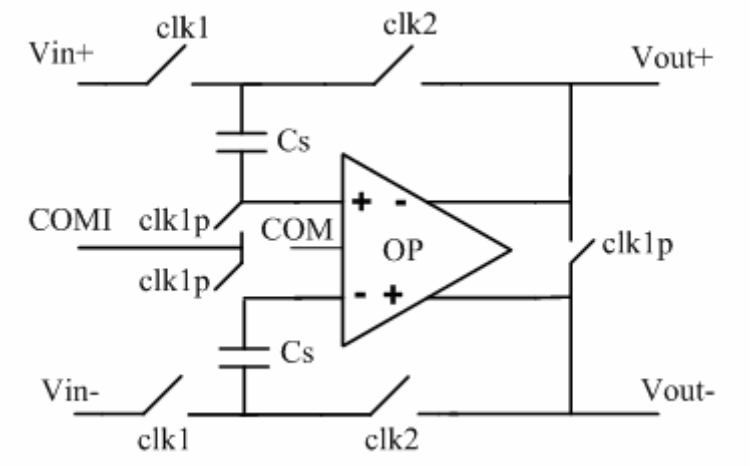


Figure 4.1 The sample-and-hold (S/H) circuit

There are four related clock phase in sample-and-hold as shown in Figure 4.2. The clk1, clk1p are used during the sample phase and clk2 are used during the hold phase. The clk1 and clk2 are non-overlap phases to prevent the charge loss on the path when both the clk1 and clk2 are closed. The clk1p has the same rising edge to the clk1 phase, but earlier falling edge takes the advantage of reducing the charge injection from the sampling switch. There is a switch connects Vout+ and Vout- during the sampling phase, and then the output node of the operational amplifier can keep the voltage at output common-mode and prevent saturation. That reduces the settling time when a non-saturated voltage needs to go back to the target voltage at hold phase [16].

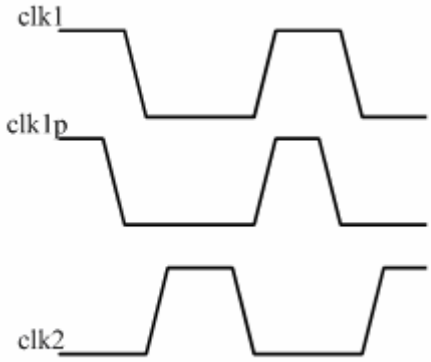


Figure 4.2 Timing diagram of the Sample-and-hold

4.2.1 Capacitors

The size of capacitors played an important role in design of the pipelined ADC. However, because of the architecture of S/H which we adopted, the major problem of capacitor mismatch is removed. The operational amplifier in Figure 4.1, can be simplified as an infinite input impedance and the output has finite gain $gm \cdot ro$. The operational amplifier's input differential pair is usually large sized to reach higher gm. Hence the parasitic capacitance Cp, from the node to ground, is too large to be ignored. A larger sampling capacitor Cs can get small time constant because it is the feedback factor. If the size too small, the clock feed-through and charge-sharing effect will be worse. In this design, the Cs which used for the S/H is 2pF.

4.2.2 Switches

The sample-and-hold circuit which operates in the sample mode is shown in Figure 4.3. The Ron is independent of the input voltage Vin if we choose the bootstrap switches. It enhances the SNR and the linearity of the pipelined ADC. The voltage in the input of the operational amplifier almost does not change when the switches S1 turns on. So using the NMOS transistor only will be suitable [27].

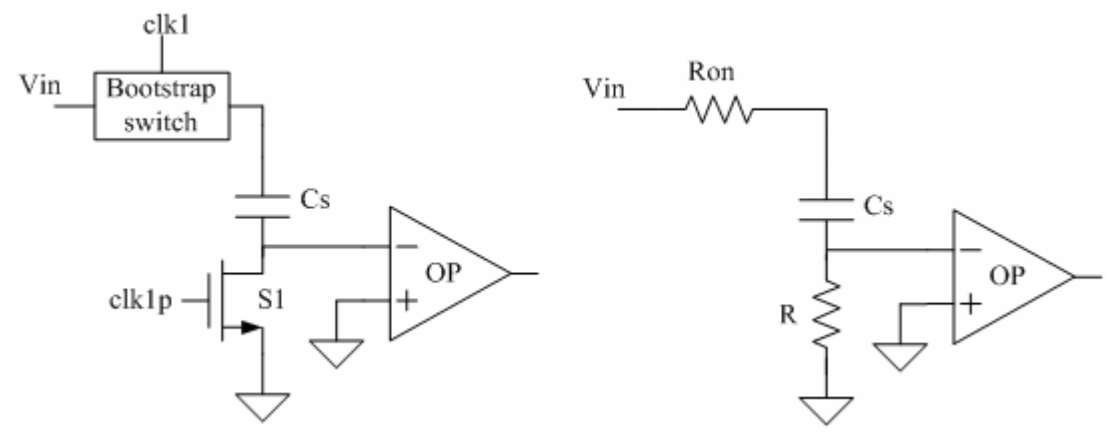


Figure 4.3 Sample-and-hold in sample mode

Figure 4.4 shows the circuit detail of the bootstrap block. It operates on a signal phase clock ϕ that turn the switch M10 on and off. During the off phase ϕ is low, device M6 and M9 discharge the gate of M10 to ground. At the same time, Vdd is applied across capacitor C3 by M3 and M11. This capacitor will act as the battery across the gate and source during the on phase. M7 and M8 isolate the switch from C3 while it is charging. When ϕ goes high, M5 pulls down the gate of M7, allowing charge from the battery capacitor C3 to flow onto the gate G. This turns on both M8 and M10. M8 enables the gate G to track the input voltage S shifted by Vdd. Keeping the gate-source voltage constant regardless of the input signal. For example, if source S is at Vdd, the gate G is 2Vdd, however Vgs=Vdd. Because the body (nwell) of M7 is tied to its source, the latch-up is suppressed.

M1, M2, C1, and C2 from a clock multiplier that enables M3 to unidirectional charge C3 during the offset phase. This entire circuit was carefully designed such that no device experiences a relative terminal voltage greater than Vdd. This circuit is similar to a low distortion sampling switch which provides a constant Vgs across the switching device.

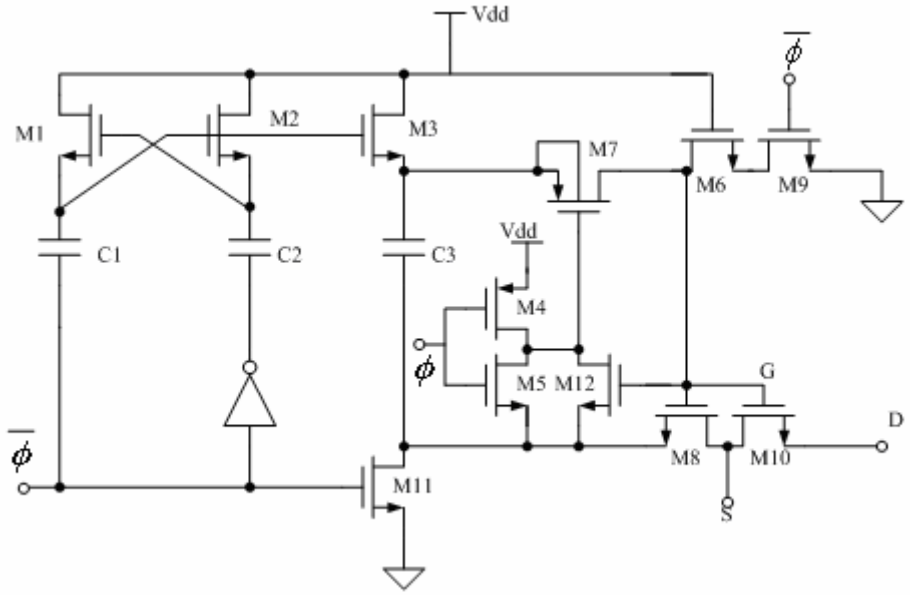


Figure 4.4 Bootstrapped switch circuit

Design guideline: C3 must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitance in the charging path. Otherwise, charge-sharing will significantly reduced the boosted voltage according to the equation as follows:

$$V_g = V_i + \left(\frac{C_3}{C_3 + C_p} \right) V_{dd} \tag{4.1}$$

where C_p is the total parasitic capacitance connected to the top plate of C_3 while it is across the main switching device M10. Figure 4.5 shows the conceptual output waveform of the bootstrap circuit [19].

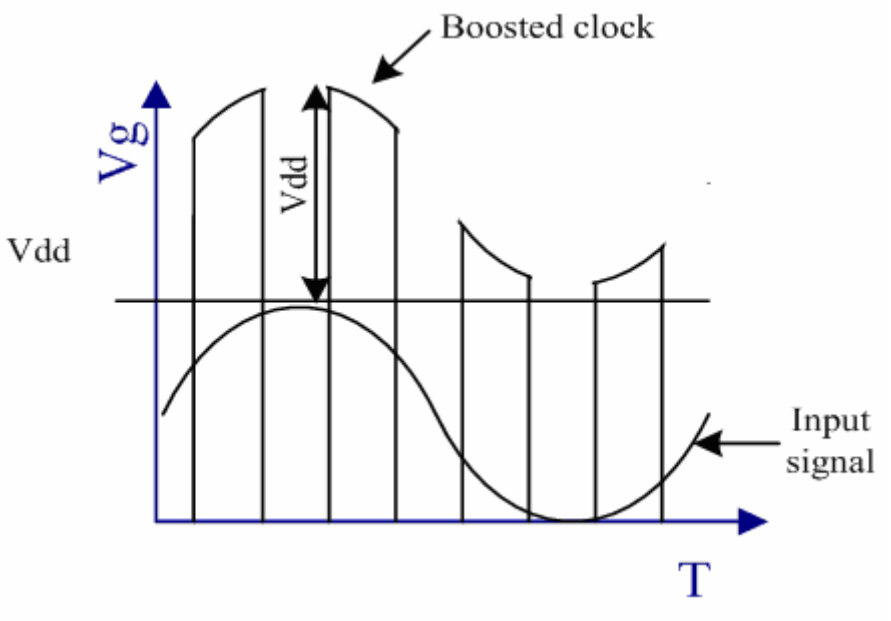


Figure 4.5 Conceptual output waveform of the bootstrap circuit.

4.3 MULTIPLYING DAC

Figure 4.6 shows the differential schematic diagram of the MDAC. The differential held analog input is applied to terminals Vin+ and Vin-, and the held output is taken at terminal Vout+ and Vout-. The MDAC operation and timing are almost the same as S/H. The control switches which are connected with the bottom

plates of Cs+ and Cs-, are used to control the transferred quantity as the function of a subtractor. The control signals a, b and c depending on the state of digital output of the sub-DAC.

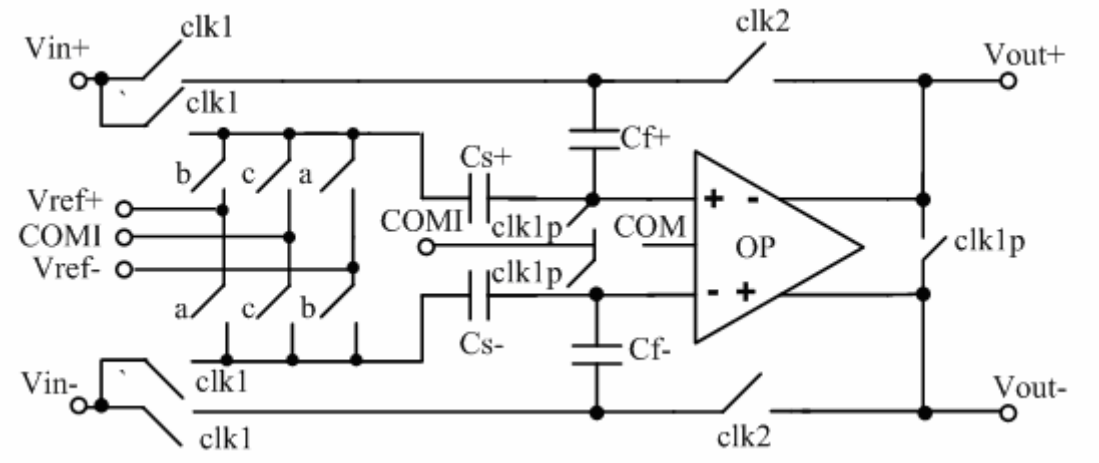


Figure 4.6 Schematic diagram of fully differential MDAC.

4.3.1 Capacitor

Unlike the S/H, the capacitor mismatch of MDAC is very critical. With the discussion in the section 3.3.2 and section 4.2.1, we can determine the minimum capacitors in the design of MDAC. The 1pF capacitor is adopted for this MDAC to meet our specification of 10-bit 40MS/s ADC.

4.3.2 Switches

As the mentioned in the section 4.2.2, the voltage in the input of the operational amplifier in sample phase and the voltage in the bottom plates of Cs+ and Cs- are almost not changed when these switches turns on. So using the NMOS or PMOS transistor only will be suitable.

The other switches are the complementary switches to enhance the linearity of MDAC. Figure 4.7 (a) shows the complementary switch in our design, and Figure 4.7

(b) shows the model of the switch.

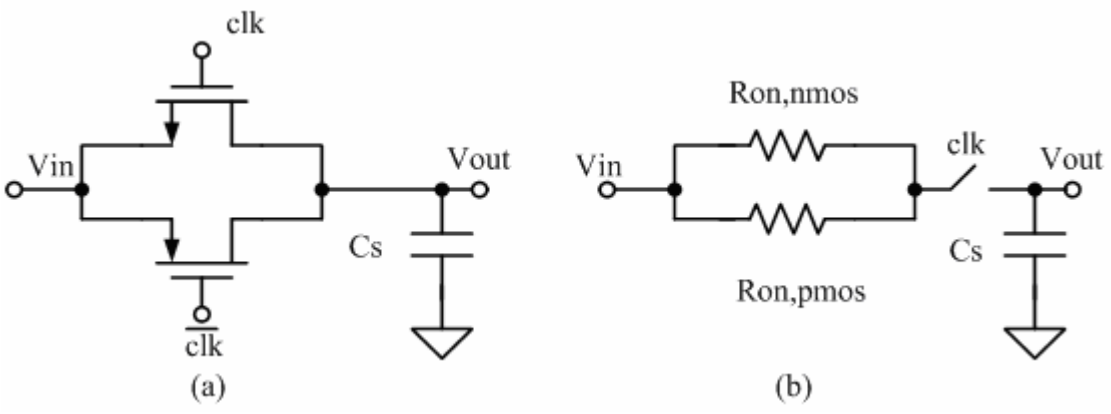


Figure 4.7 (a) The complementary switch, (b) simplify model of switch.

We can observe that the current flowing through the MOS transistors depends on the input voltage level of Vin. In the case of the NMOS, if the turn on voltage of the gate is Vdd and the source-drain voltage is much smaller than $Vdd - V_{th}$, then the transistor must operates in triode region and the flowing current is

$$\begin{aligned} I_{D,NMOS} &= \mu_n C_{ox} \left(\frac{W}{L}\right)_N \left[\left(V_{GS} - V_{THN}\right) \cdot V_{DS} - \frac{V_{DS}^{\,2}}{2} \right] \\ &\cong \mu_n C_{ox} \left(\frac{W}{L}\right)_N \left(V_{DD} - V_{in} - V_{THN}\right) \cdot V_{DS} \end{aligned} \tag{4.2}$$

Then, the turn-on resistance of NMOS is given by

$$R_{on,NMOS} = \frac{V_{DS}}{I_{D,NMOS}} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N \left(V_{DD} - V_{in} - V_{THN}\right)} \tag{4.3}$$

And the PMOS is similar as

$$R_{on,PMOS} = \frac{V_{DS}}{I_{D,PMOS}} = \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_P \left(V_{in} - 0 - \left|V_{THP}\right|\right)} \tag{4.4}$$

Then the total on-resistance is

$$R_{on,total} = R_{on,NMOS} \left\| R_{on,PMOS} \right.$$

$$= \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_N \left(V_{DD} - V_{THN}\right) - \left[\mu_n C_{ox}\left(\frac{W}{L}\right)_N - \mu_p C_{ox}\left(\frac{W}{L}\right)_P\right] \cdot V_{in} - \mu_p C_{ox}\left(\frac{W}{L}\right)_P \left|V_{THP}\right|} \quad (4.5)$$

If $\mu_n C_{ox}\left(\frac{W}{L}\right)_N = \mu_p C_{ox}\left(\frac{W}{L}\right)_P$, the $R_{on,total}$ is independent of the input level. It enhances the SNR and the linearity of the pipelined ADC. Because the mobility $\mu_n \approx 4\mu_p$, the size $\left(\frac{W}{L}\right)_P$ get four times of $\left(\frac{W}{L}\right)_N$ [3] [16]. Figure 4.8 shows the MDAC with all the switches which are adopted.

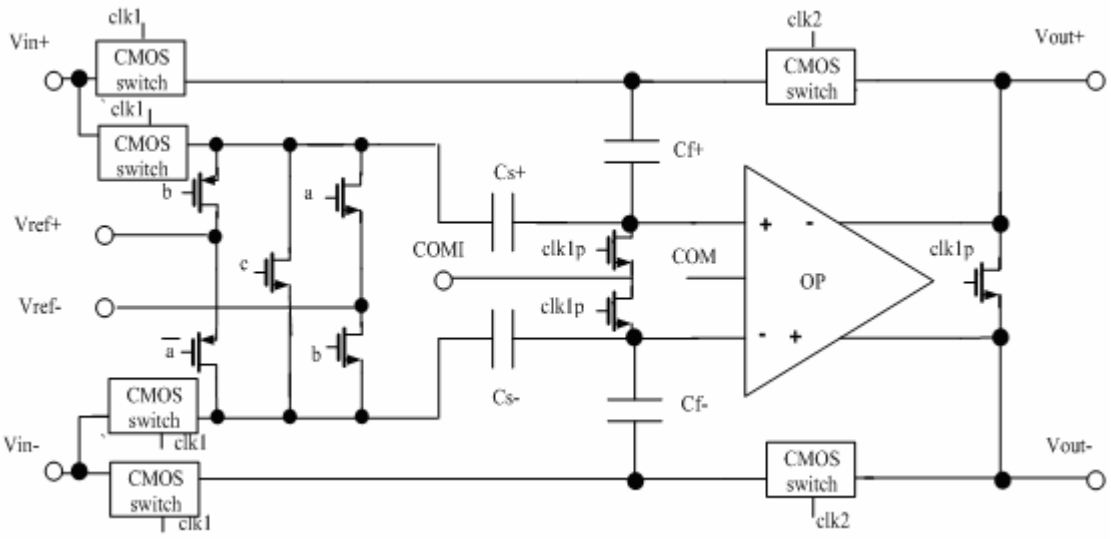


Figure 4.8 A fully differential MDAC with adopted switches

4.4 OPERATIONAL AMPLIFIER

4.4.1 Gain Requirement

The DC open-loop gain of the operational amplifier limits the ADC's resolution. Figure 4.9 shows the operation of the S/H circuit in both sample phase and hold phase. It acts like the MDAC as shown in Figure 4.10 which is discussed in section 3.3.2.

Then we have

$$C_s \cdot V_{in} = C_s (V_{out} - V_-) - C_p \cdot V_- \tag{4.6}$$

Solving for V_{out} yields

$$V_{out} = V_{in} \cdot \left(\frac{1}{1 + \left(\frac{1}{A \cdot f} \right)} \right) \approx V_{in} \cdot \left(1 - \frac{1}{A_0 \cdot f} \right) \tag{4.7}$$

where the feedback factor f is given by

$$f = \frac{C_s}{C_s + C_p} \tag{4.8}$$

The error is approximately $\frac{1}{A_0 \cdot f}$. In design of 10-bit ADC, the Vout of S/H constitutes the input of following 9 stages. The maximum tolerable DNL is 0.5LSB at 10 bit level for the following 9 stages, the $\frac{1}{A_0 \cdot f} \le \frac{1}{2} \cdot \left(\frac{1}{2} \right)^9$. We assumed that the parasitic capacitance $C_p = \frac{1}{5} C_s$, then the required open-loop gain A_0 for S/H stage is 61.79 dB.

The operational amplifier gain requirement for the MDAC is discussed in section 3.3.2. The error is $\frac{1}{A_0 \cdot f}$ too. However, the f in the MDAC is $\frac{C_f}{C_s + C_p + C_f}$, and the Vout constitutes the input of following 8 stages, the $\frac{1}{A_0 \cdot f} \le \frac{1}{2} \cdot \left(\frac{1}{2} \right)^8$. The parasitic capacitance C_p is assumed that $C_s = C_f = 5 \cdot C_p$. Therefore the required open-loop gain for the first stage of MDAC is 61.03 dB

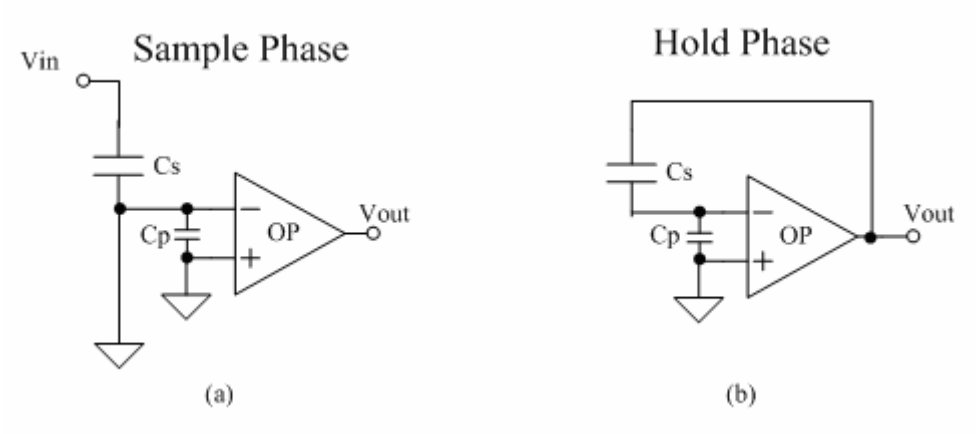


Figure 4.9 Operation of the S/H circuit in (a) sample phase and (b) hold phase.

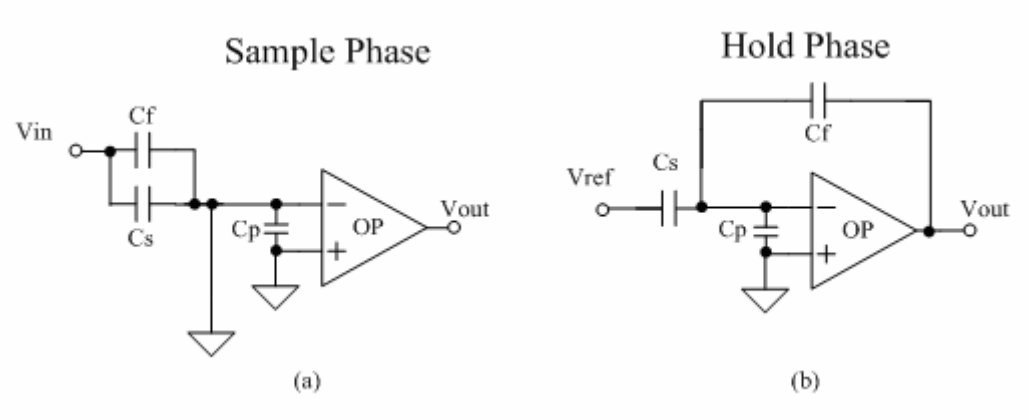


Figure 4.10 Operation of the MDAC circuit in (a) sample phase and (b) hold phase.

4.4.2 Bandwidth Requirement

The successive pipeline stages operate in opposite clock phases, which gives a settling time of a half of the clock cycle (T/2). The settling time is determined first by the slew-rate (SR) and finally by the gain bandwidth (GBW) of the amplifier, as indicated in Figure 4.11.

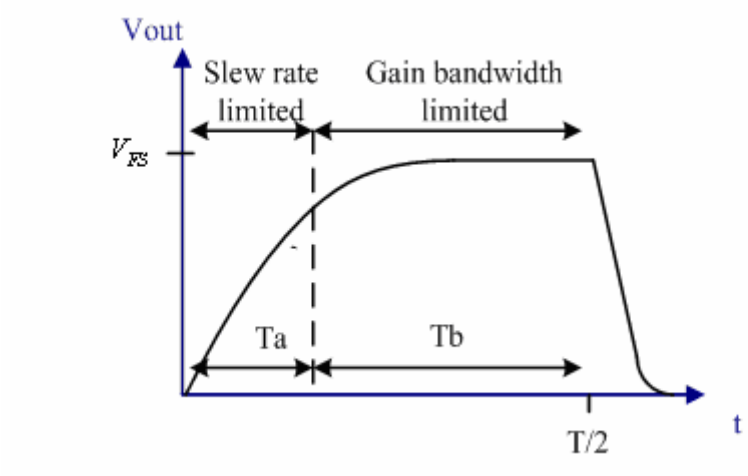


Figure 4.11 Settling of the stage output

The half cycle of the sampling time for 40MHz is 12.5ns. However, the rising time (Tr), falling time (Tf) and non-overlap time must be taken into consideration. And the half cycle (T/2) is approximately 11ns. Briefly we can assume the time ratio of two parts to be about 1:2. That would be 3ns:8ns in our timing arrangement. During the SR limited transient response period, the critical case will be full range swing in 3ns. We can calculate the requirement of SR as

$$SR = \frac{0.5V}{3ns} \approx 167V/us \tag{4.9}$$

The most commonly used operational amplifier can be modeled with a single-pole small-signal model of Figure 4.12.

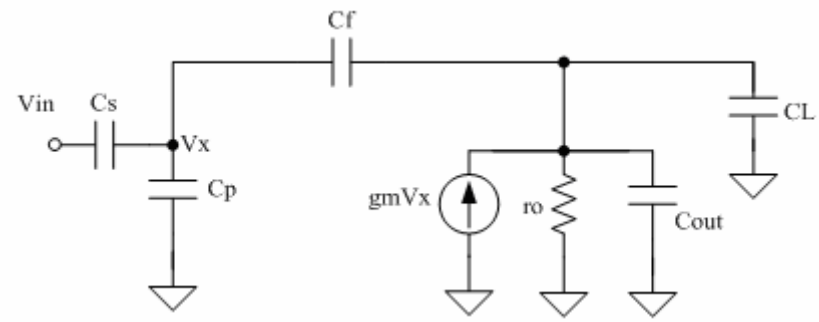


Figure 4.12 Small-signal model of MDAC in the hold phase.

The gain bandwidth frequency of the operational amplifier is related to the transconductance gm by equation

$$gain\ bandwidth = \frac{gm}{2\pi \cdot C_{L,total}} \tag{4.10}$$

where the total load capacitance $C_{L,total} = C_L + C_{out}$ includes the parasitic output capacitance C_{out}. Using the symbol of Figure 4.15, the transfer function is

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{-(C_s + C_p) \cdot C_s}{C_s + C_p} \cdot (gm - C_f \cdot s) \cdot r_o}{r_o \left[C_{L,total} \cdot (C_s + C_p) + C_{L,total} \cdot C_f + (C_s + C_p) \cdot C_f \right] \cdot s + gm \cdot r_o \cdot C_f} \tag{4.11}$$

the corner frequency is given by

$$\omega_{-3dB} = \frac{gm}{\frac{C_{L,total}}{f} + C_s + C_p} \tag{4.12}$$

The error ε_τ caused by the incomplete exponential settling during the time of gain bandwidth limited phase (T_b), is given by

$$\varepsilon_\tau = e^{-\omega_{-3dB} \cdot T_b} = e^{-\frac{g_m}{\frac{C_{L,total}}{f} + C_s + C_p} \cdot T_b} \tag{4.13}$$

In order to fulfill the resolution requirement, the settling error must be less than 0.5LSB, this case reduced to the input of the stage *i*, which results in a condition

$$\varepsilon_\tau < \frac{1}{2^{N_i}} \tag{4.14}$$

where *Ni* is the resolution of the remaining back-end pipeline including the *ith* stage. For S/H the *Ni* is 10, and for the first MDAC stage the *Ni* is 9. By combining Equation 4.13 and Equation 4.14, and solving the amplifier transconductance *gm*

yields

$$g_m > \frac{N_i \cdot \ln 2 \cdot \left(\frac{C_{L,total}}{f} + C_s + C_p \right)}{T_b} \tag{4.15}$$

On the other hand, the transconductance is related to the width *W*, length *L*, and drain current I_D of the transistor by

$$g_m = \sqrt{2\mu \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} \tag{4.16}$$

where μ is the mobility and C_{ox} the gate oxide capacitance. By substituting Equation 4.15 into Equation 4.16, a condition for the minimum drain current of one transistor of the amplifier input differential pair I_D can be derived to be

$$I_D \cdot \frac{W}{L} > \frac{N_i^2 \cdot \ln^2 2 \cdot \left(\frac{C_{L,total}}{f} + C_s + C_p \right)^2}{2\mu \cdot C_{ox} \cdot T_b^2} \tag{4.17}$$

Using Equation 4.10, this can be expressed in terms of the minimal gain bandwidth

$$gain\ bandwidth > \frac{N_i \cdot \ln 2 \cdot \left(\frac{C_{L,total}}{f} + C_s + C_p \right)}{2\pi \cdot T_b \cdot C_{L,total}} \tag{4.18}$$

Table 4.1 shows the gain and bandwidth requirement of operational amplifier in S/H and the first MDAC stage for the design of 10-bit 40MS/s pipelined ADC. It is assumed that $C_{L,total} = 3pF$, $C_s = C_f = 5C_p$ (in S/H, C_s is zero) and $T_b = 8ns$.

Table 4.1 The requirements of operational amplifier in S/H and MDAC

Parameter	S/H	MDAC of the first stage
DC open-loop gain	61.79dB	61.03dB
Unity gain bandwidth	193MHz	359MHz
Slew-rate	167V/us	167V/us

4.4.3 Telescopic Operational Amplifier

The simplest approach for a high-gain operational amplifier is the one-stage telescopic amplifier of Figure 4.13. All transistors in Figure 4.13 are biased in saturation region, PMOS transistors M5, M6, M7, M8 can be considered as current source, NMOS transistors M3, M4 are connected as common-gate form, NMOS transistors M1, M2 are the differential input of the operational amplifier, and M9 is the tail current source. The transistors from Mb1 to Mb16 are the bias circuits of this operational amplifier.

Typically, when using fully-differential operational amplifier in a feedback application, the applied feedback determined the differential signal voltage, but does not affect the common-mode voltages. It is necessary to add additional circuitry to determine the output common-mode voltage and to control it to be equal to some specified voltage. This circuitry, referred to as the common-mode feedback (CMFB) circuitry, is often the most difficult part of the operational amplifier design.

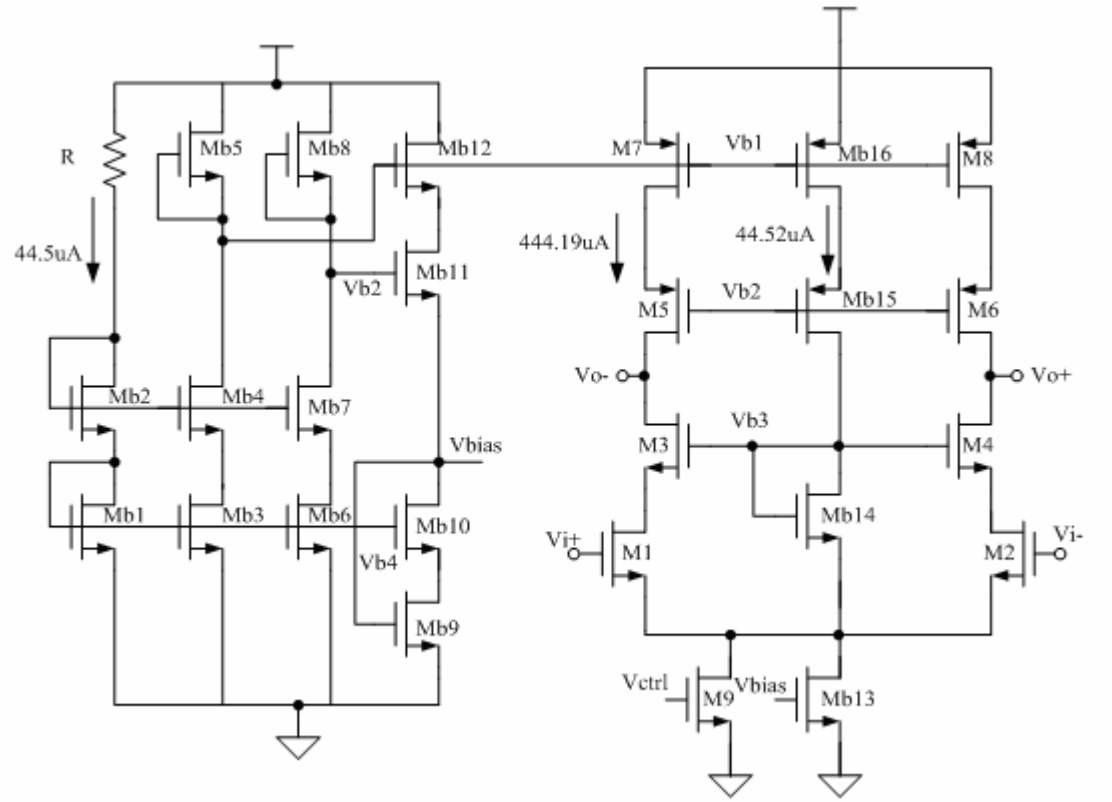


Figure 4.13 Telescopic operational amplifier with bias circuits.

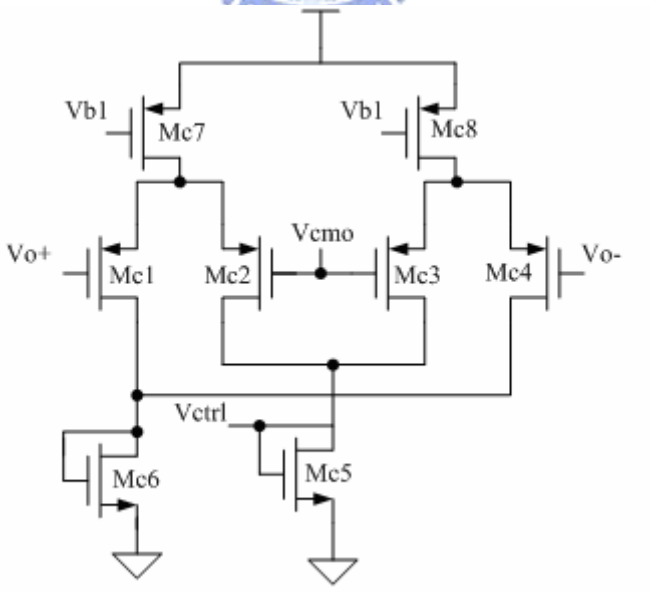


Figure 4.14 Continuous-time CMFB of the telescopic operational amplifier.

Figure 4.14 shows the CMFB in our design. Since the two pairs have the same differential voltages being applied, the current in Mc1 will be equal to the current in Mc3, while the current in Mc2 will be equal to the current in Mc4. As long as the voltage Vo+ is equal to the negative value of Vo-, the current through diode-connected Mc5 will not change even when large differential signal voltages are present. When common-mode voltage of the output is changes (assume a positive common-mode voltage is present), will cause the current in both Mc2 and Mc3 to increase, which causes the current in diode-connected Mc5 to increase, which in turn causes its voltage to increase. This voltage is the bias voltage that sets the current levels in the n-channel current sources at the output of the operational amplifier [3].

The telescopic architecture was chosen rather than folded-cascode architecture, the major reason is the consideration of bandwidth. The biggest disadvantage of this architecture is its low maximum differential output swing. If we want to get higher swing, the DC open-loop gain will be decreased. There are many techniques to solve this problem, and gain-boosting technique is a good choice. However, for fully differential applications, the CMFB are required. Gain-boosting architecture needs one or two additional amplifiers to enhance its gain and output resistance, each of them need CMFB also. If the switch-capacitor CMFB is adopt, the die size will increase and the performance of the circuit will be limited.

Here, we proposed a new technique to enhance the gain of the telescopic architecture as shown in Figure 4.15. The transistors from Mp1 to Mp7 perform the positive feedback operation. In order to guarantee the stability of the operational amplifier, the size of positive feedback circuits is ten times smaller than the original telescopic operational amplifier, and the positive feedback quantity can not be too large.

Although the increase of gm is not obviously, because of the low positive feedback,

the M5, M6, M7, M8 still perform a negative output resistance. Therefore, the gain is enhanced. The operational amplifier we proposed has many advantages. At first, the DC open-loop gain is boosted without using many transistors like gain-booting architecture. Second, the output Vol+ and Vol- are the voltage level shift of Vo+ and Vo- can be used to the CMFB, it will decrease the output capacitance. Finally, the operational amplifier works when the lower Vdd is applied, without sacrificing the output swing and the speed.

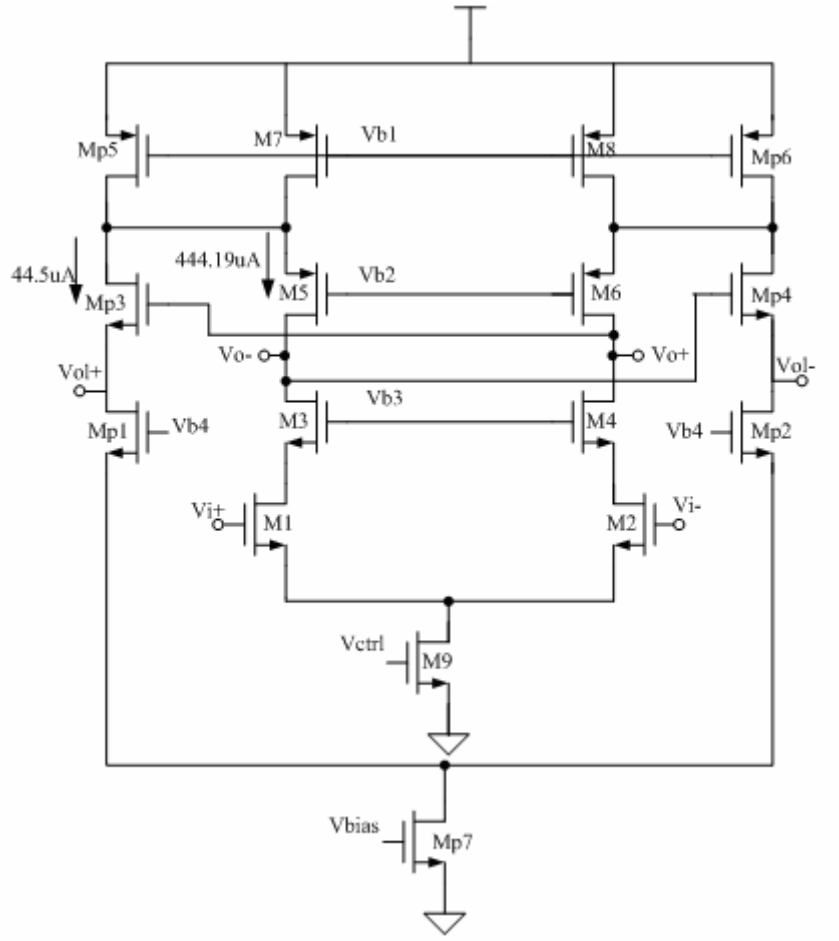


Figure 4.15 Telescopic operational amplifier with the positive feedback circuits.

4.5 COMPARATOR

Figure 4.16 shows the circuit topology of a dynamic latch comparator. A latch with resistive comparing circuits in series with its NMOS is used to give low power during the regeneration mode. However, there is no PMOS precharging circuit and an NMOS pass transistor M12 for output charge sharing is used to equalize the two output voltages to approximately Vdd/2 during the reset mode. This is possible because the latch is totally disconnected from both Vdd and ground by M1, M10 and M11 when clk1p is high and clk1pb is low. Therefore a significant half power reduction, as compared to the precharging approach, is achieved. Note also that at the start of the regeneration mode (comparing mode), the latch is already active since both outputs are at Vdd/2. Hence the comparing speed tends to be fast. However, the comparing speed depends additionally on the different magnitude of the inputs and the amplifying loop gain within the latch. Hence the speed can be increased by enlarging the widths of M2-M5.

The comparator offset comes from the input transistor mismatch, M6-M9 as shown in Equation 4.19,

$$V_{OS} \approx \left|\frac{\triangle\beta_A}{\beta_A}\right|\left(V_{in-} - V_{t,A}\right) + \left|\frac{\triangle\beta_B}{\beta_A}\right|\left(V_{ref-} - V_{t,b}\right) + \left|\triangle V_{t,A}\right| + \frac{\beta_B}{\beta_A}\left|\triangle V_{t,B}\right| \qquad (4.19)$$

where $\triangle\beta$ is the mismatch due to transistor dimensions and $\triangle V_t$ is the mismatch of threshold voltage. In this equation the subscript A, B relate with M6-M7 and M8-M9 pairs respectively. However, the offset error may be increased from Equation 4.19 by unequal loading at its output nodes. Furthermore, the output should not drive a static gate directly since its level during the reset interval is neither high nor low. Thus, an output latch circuit should be used to buffer with the load and convert into static outputs. When clk2 is low and clk2b is high. Ma2, Ma3, Ma6 and Ma7 are off to disable the effect of output of the dynamic comparator. Vout+ and Vout- are

therefore latched at their previous states. When clk2 is low and clk2b is high. Ma2, Ma3, Ma6 and Ma7 are on to enable transferring the comparator outputs to the output latch. The clk2 and clk1p is the same as the timing of S/H and MDAC. The size of M8, M9 is four times smaller than M6, M7, it can reduce a pair of power supply in our design [29].

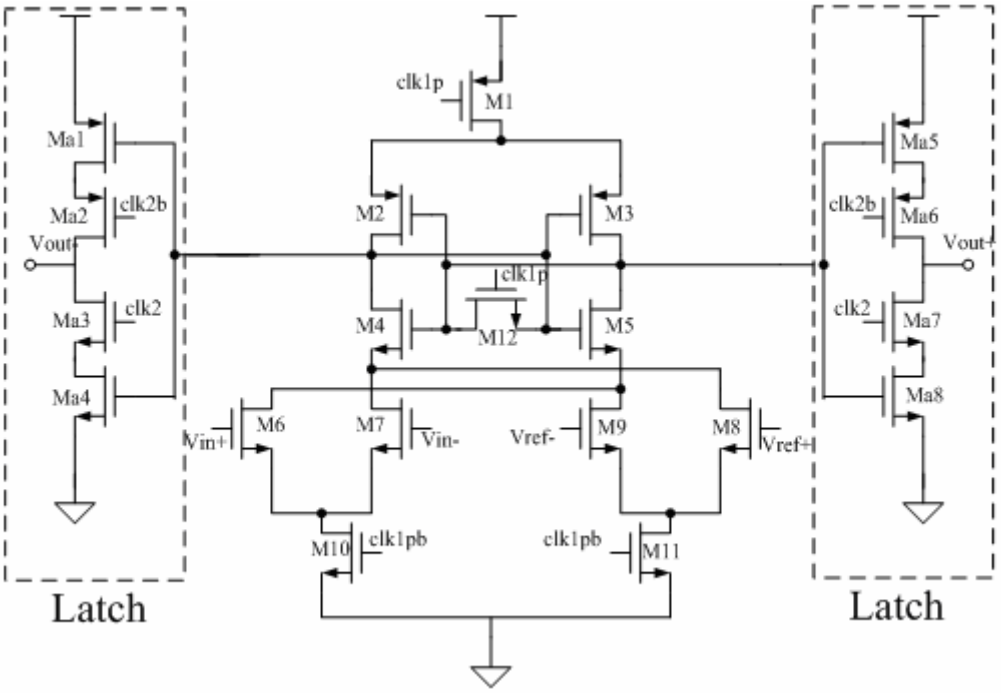


Figure 4.16 A charge sharing latch comparator with latch

4.6 DIGITAL CIRCUITS IN PIPELINED ADC

4.6.1 Clock Generator

Figure 4.17 shows the waveform which the pipelined ADC needs, and Figure 4.18 shows the diagram of the clock generator. Four NMOS are added to bypass the inverter delay chains and lined up the rising edge of the clocks. In practice, the inversion of clock is needed for CMOS switch.

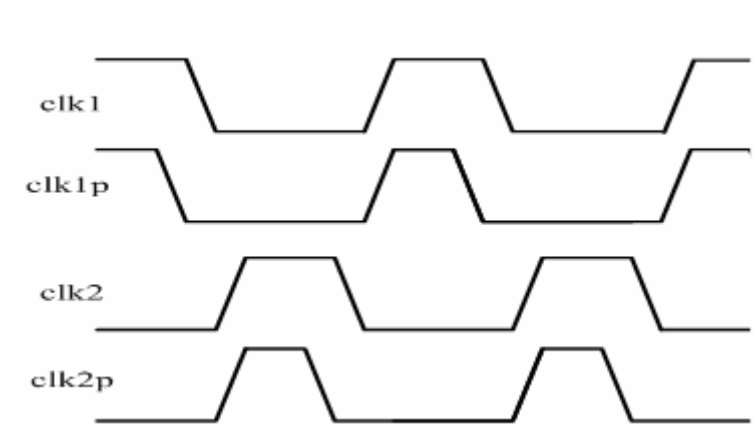


Figure 4.17 The clock waveform for pipelined ADC

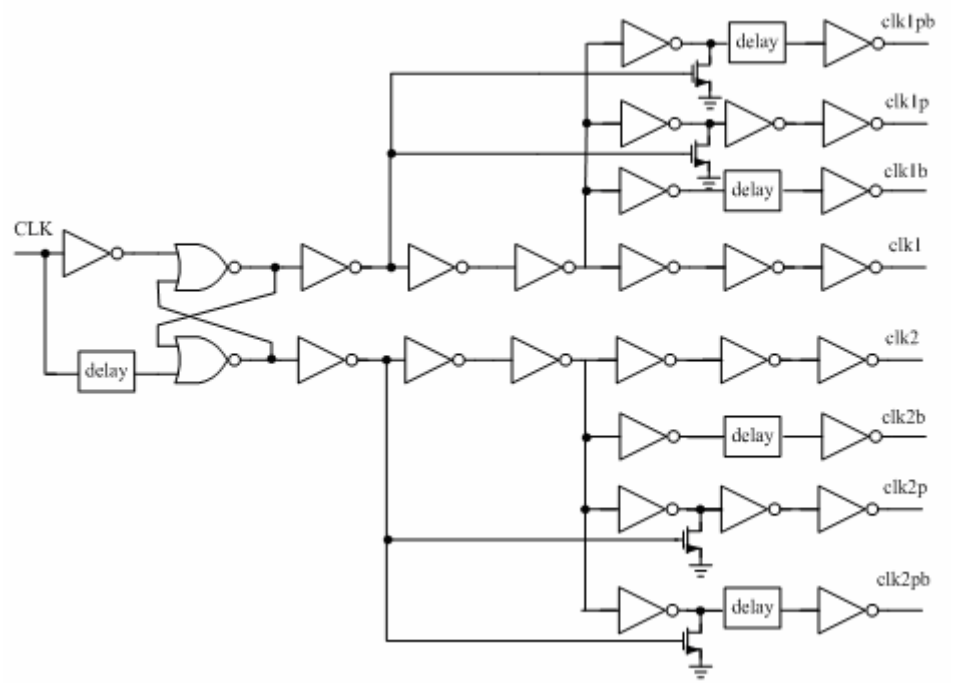


Figure 4.18 Schematic of the non-overlap 2 phase generator.

4.6.2 Control Signals for MDAC

The quantizer in the stages can be seen as the 1.5-bit flash ADC. The 1.5-bit flash ADC consists of two fully-differential comparators and simple logic as shown in Figure 4.19.

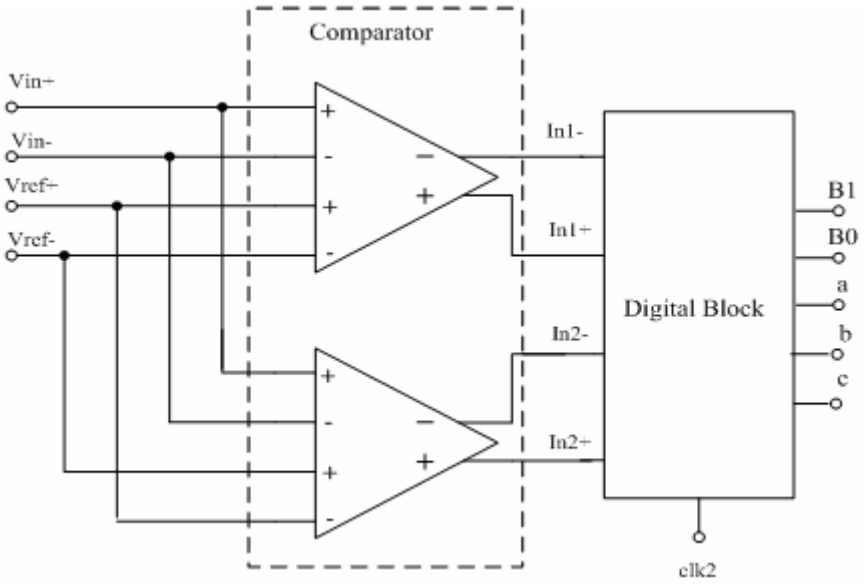


Figure 4.19 The 1.5-bit flash ADC

The differential thermometer code comparators outputs are converted into a single-ended raw ADC binary output code, B0 and B1, and a, b and c are the control signals for the MDAC switches of section 4.3. Figure 4.20 shows the logic detail of the digital block in figure 4.19.

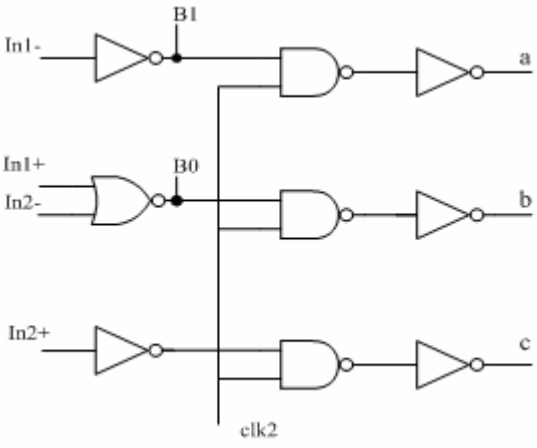


Figure 4.20 Logic detail of the digital block in quantizer.

4.6.3 Digital Error Correction

The detail diagram of the pipelined ADC is shown in Figure 4.21. The shift register array and adder under perform the operations of 1.5-bit digital error correction as shown in Figure 4.22. The registers we used, is **C^{2}MOS** register. It is adopted by the simple structure.

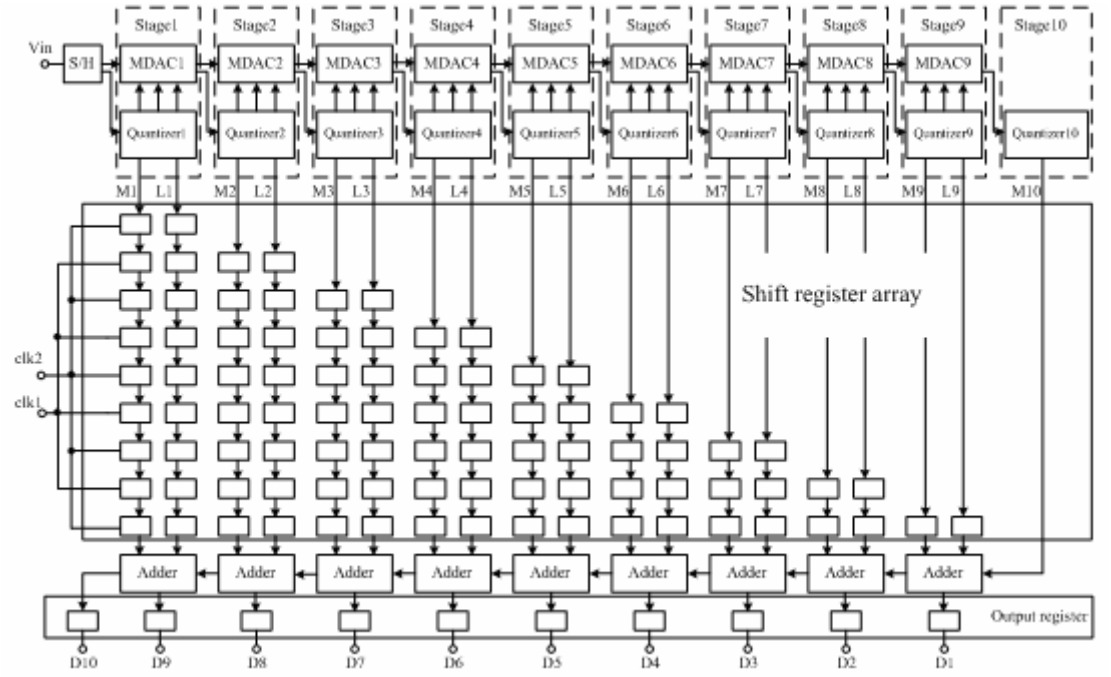


Figure 4.21 The detail diagram of the pipelined stage.

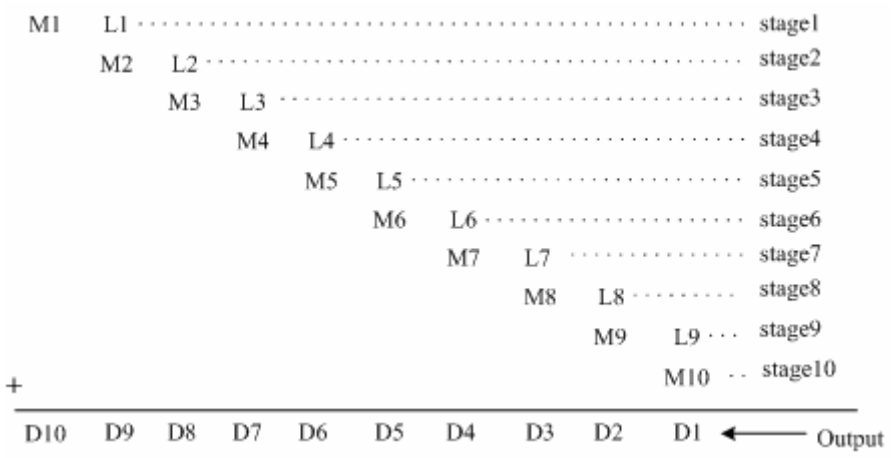


Figure 4.22 The 1.5-bit digital error correction operation.

In Figure 4.21, the adder is not a general full adder. With the operation of the 1.5-bit digital correction, the adder can be simplified as shown in Figure 4.26

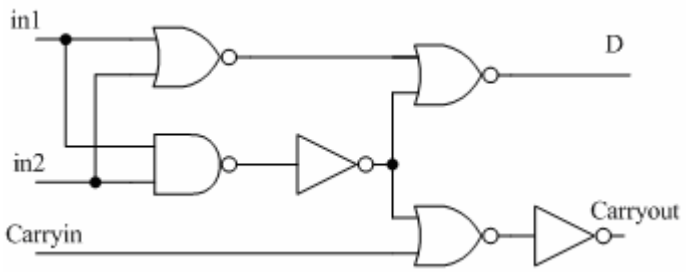


Figure 4.23 A simplified adder in pipelined ADC

4.7 SIMULATION RESULTS

4.7.1 Simulation Results of Bootstrap Switch

Figure 4.24 shows the results of simulation by HSPICE. The input common-mode voltage is at 1.1V, the swing of the signal is ±0.5V. Figure 4.25 shows simulation result of the gate-source voltage of M10 in Figure 4.4. We can obverse that the Vgs of M10 in the sample phase is almost a constant; the Ron of this bootstrap switch is independent with input signal.

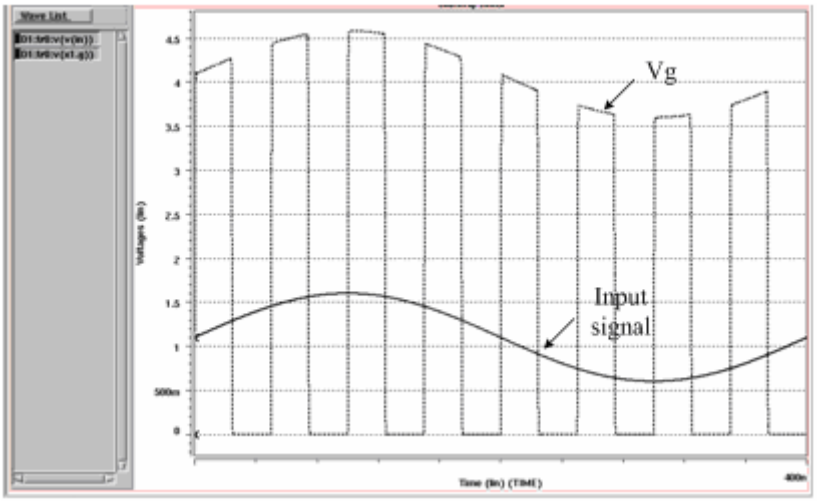


Figure 4.24 Conceptual output waveform of the bootstrap circuit by Hspice.

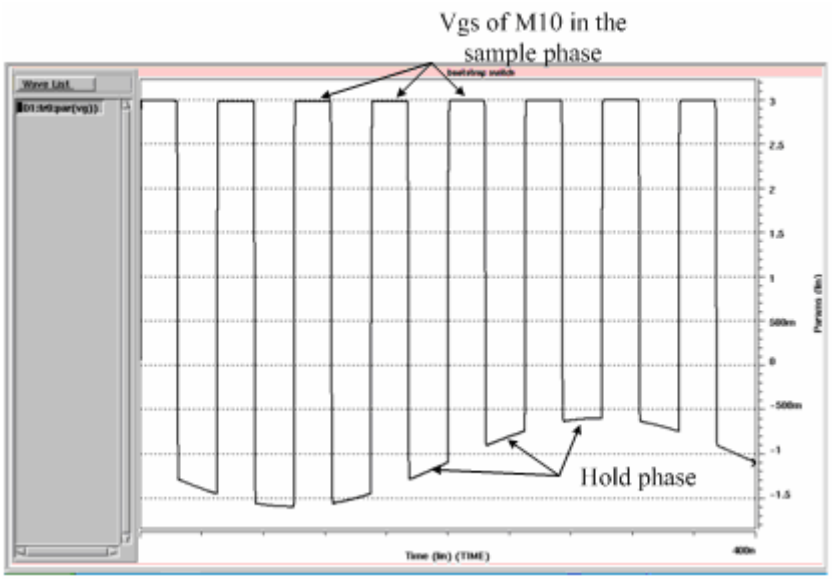


Figure 4.25 Simulation result of the gate-source voltage in the sample phase.

4.7.2 Simulation Results of Operational Amplifier

Figure 4.26 shows the gain of proposed operational amplifier and telescopic operational amplifier. The positive feedback architecture enhances gain by 24dB, and does not affect the unity-gain bandwidth. Figure 4.27 shows the stability when the positive feedback circuits are added.

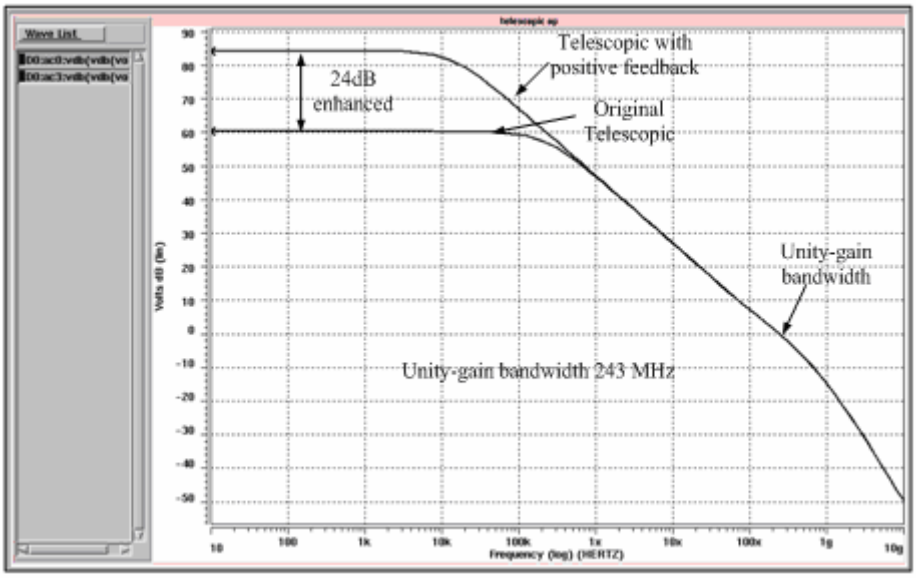


Figure 4.26 The gain comparison of the proposed architecture and original architecture (TT).

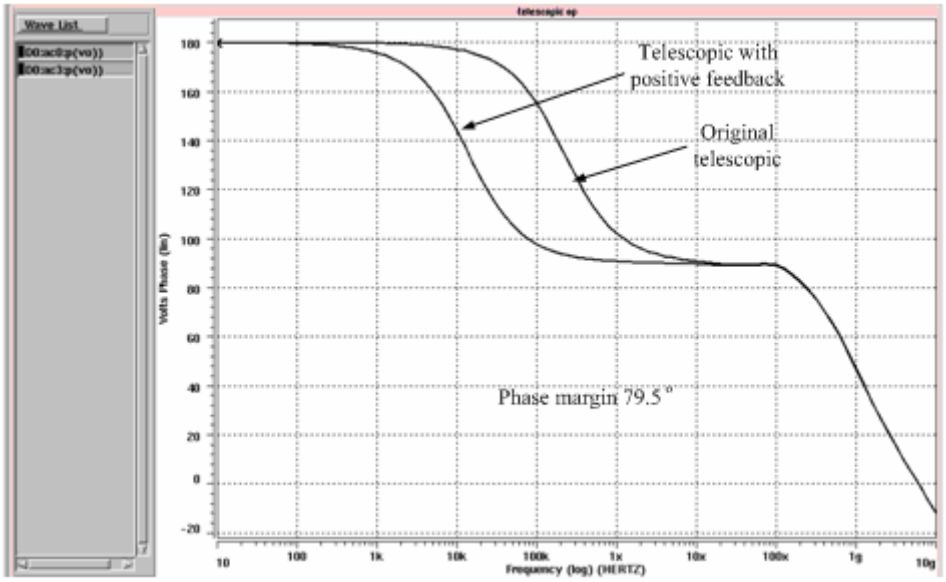


Figure 4.27 The phase margin of the proposed architecture and original architecture (TT).

Figure 4.28 shows the gain of proposed amplifier with different corner, and lists the worst and the best case. From this figure, we can see the gain varies from 77.5dB to 94.4dB.

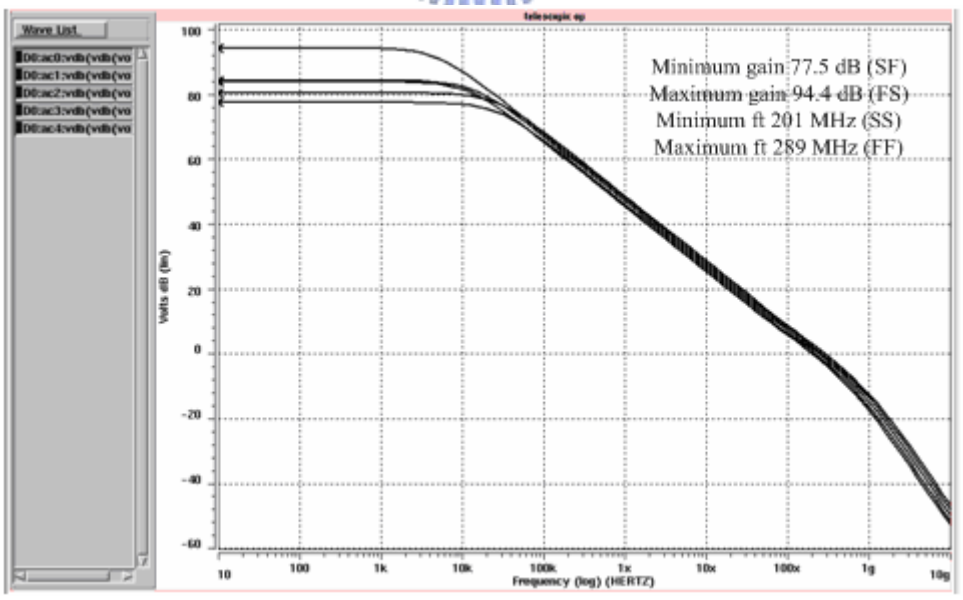


Figure 4.28 The gain of proposed operational amplifier with corner TT, FF, SS, FS and SF.

Figure 4.29 shows the phase margin of the proposed amplifier with different corner. It also shows the stability of the proposed amplifier.

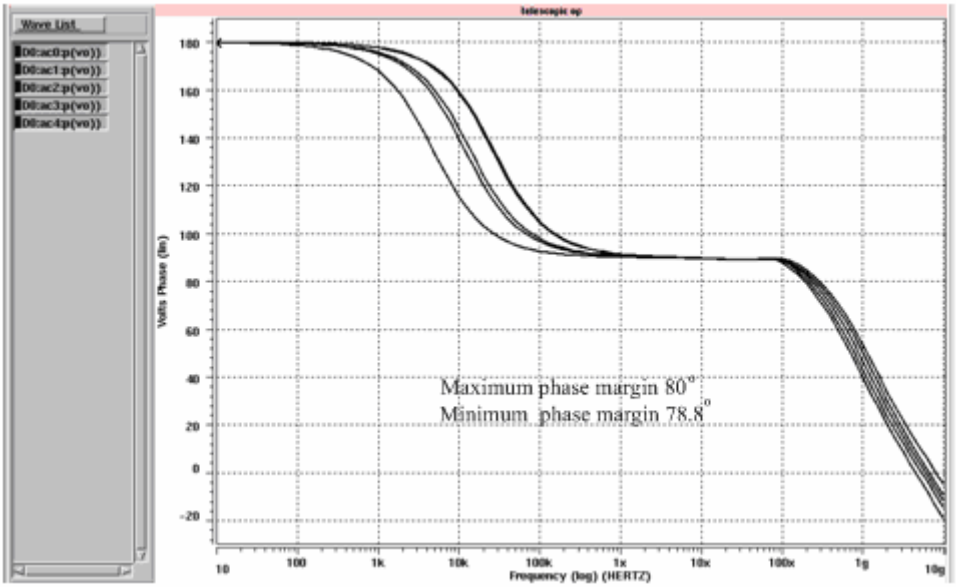


Figure 4.29 The phase of proposed operational amplifier with corner TT, FF, SS, FS,SF.

Table 4.2 summarized the simulation results of the fully differential operational amplifier, can be compared to the minimum requirements of Table 4.1.

Table 4.2 The operational amplifier simulation summary

Use	S/H (loading 3pF, TT 25ºC)	MDAC (loading 3pF, TT 25ºC)
DC gain	84.3dB	84.3dB
Unity gain frequency	241MHz	438MHz
Slew rate	171V/us	335V/us
Output swing	±0.5v	±0.5v
Phase margin	79.5º	67.1º
Input common mode voltage	1.1V	1.1V
Output common voltage	1.9V	1.9V
Power consumption	5.007mW	10.0141mW
Supply voltage	3.3V	3.3V

4.7.3 Simulation Results of S/H

The S/H is the most critical stage in the pipelined stage. We apply the proposed amplifier to the S/H stage, and Figure 4.30 plots the 1024-points FFT plot of the output power spectrum, and the performance is much higher than 10-bit.

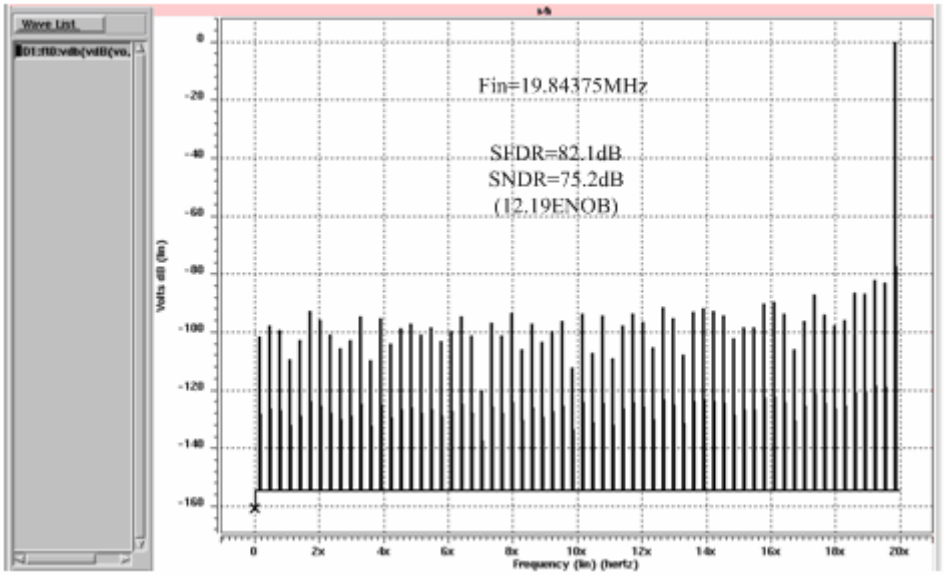


Figure 4.30 FFT analysis of the S/H (TT).

4.7.4 Simulation Results of Quantizer

Figure 4.31 shows the speed of the dynamic comparator, and it also shows the voltage level when the dynamic comparator in the charge sharing phase. Compared to the conventional resistive divider dynamic comparator, it reduces the power consumption. The transient response is shown in Figure 4.32. The comparing threshold voltages are at $\pm\frac{1}{4}Vref$, out+ and out- are the latch outputs of Figure 4.16, and Vin is the differential signal between Vin+ and Vin-.

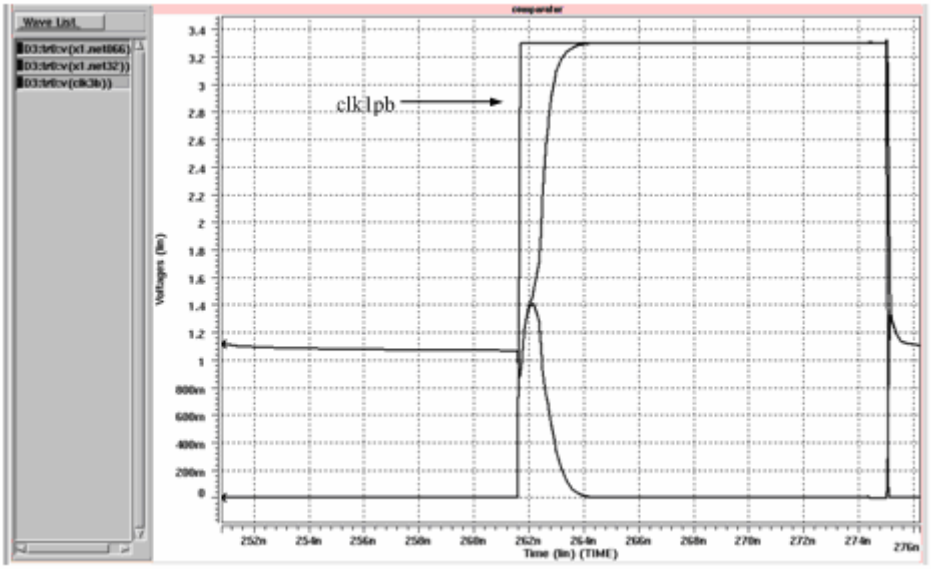


Figure 4.31 The speed of the dynamic comparator.

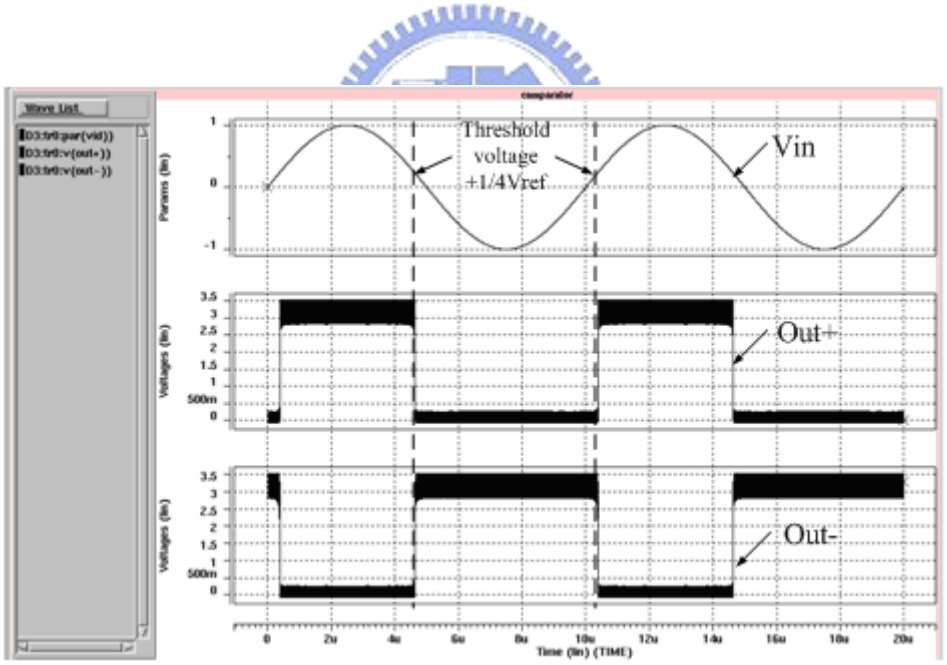


Figure 4.32 Transient response of the dynamic comparator.

The dynamic comparator is used to implement the 1.5-bit flash ADC, and Figure 4.33 shows the simulation of the 1.5-bit flash ADC, and also shows the control signals (a, b, c) which are used in the MDAC.

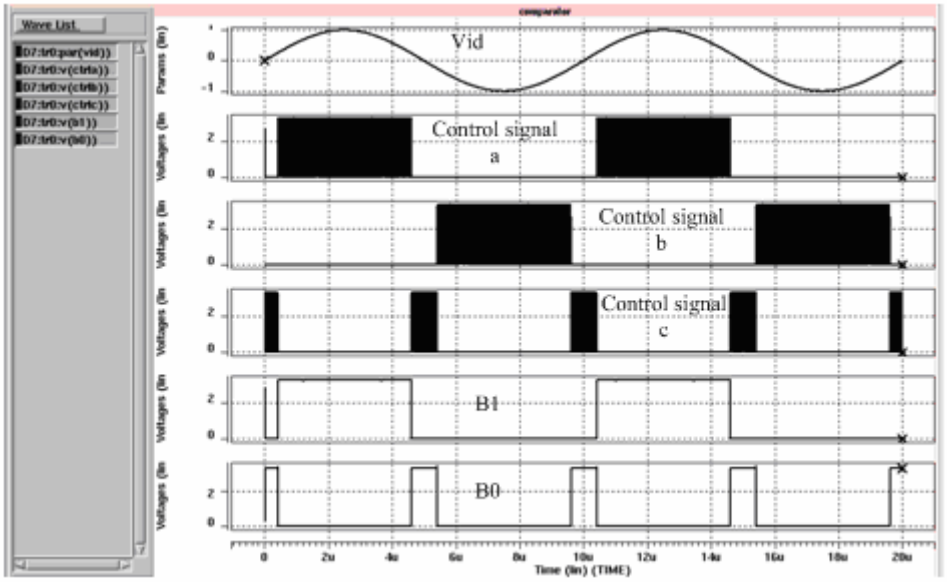


Figure 4.33 Transient response of the quantizer.

4.7.5 Simulation Results of MDAC

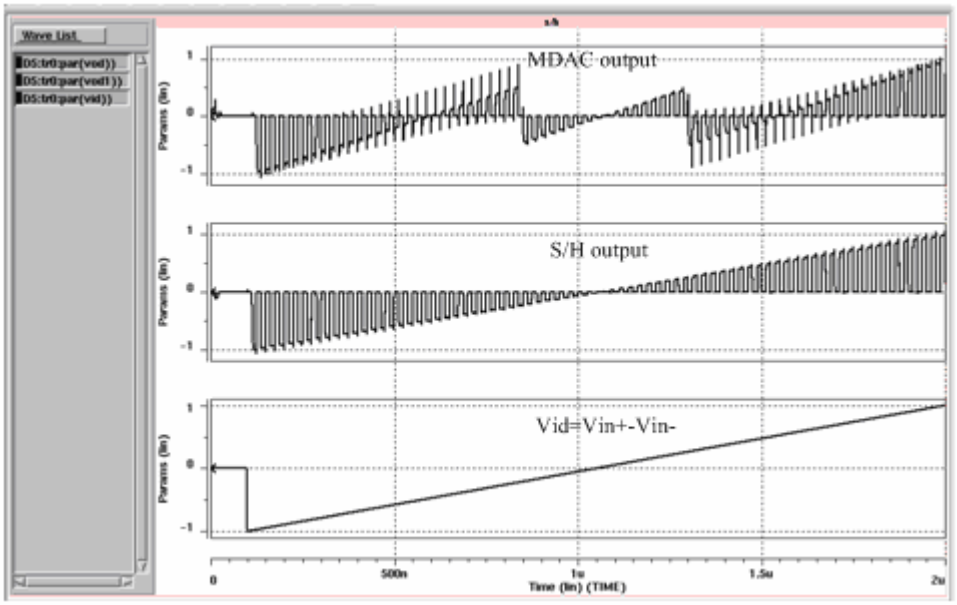


Figure 4.34 Transfer curve of the MDAC.

Figure 4.34 shows the transfer curve of the MDAC, and the voltage threshold is

at $\pm\frac{1}{4}Vref$.

4.7.6 Simulation Results of Clock Generator

The clock generator creates two non-overlap clocks to perform the pipelined architecture. Figure 4.35 shows the two non-overlap clock clk1 and clk2, and clk1p has earlier falling edge of clk1 can reduce some error as described before.

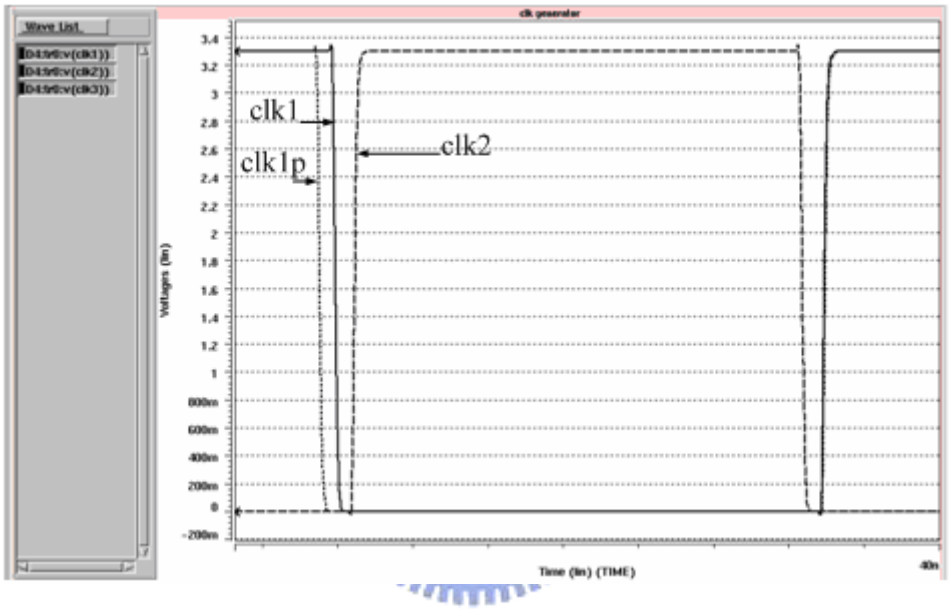


Figure 4.35 Simulation results of the clock generator.

4.7.7 Simulation Results of Whole Chip

Figure 4.36-4.43 show the 1024-point FFT analysis of the pipelined ADC with different frequency of input signal, and the performance is listed on the figure. Figure 4.44 shows the SNDR versus frequency of input signal. Figure 4.45 shows ramp response of the pipelined ADC is used to calculate the DNL and INL. Figure 4.46 and Figure 4.47 show the linearity of the pipelined ADC. In order to minimize the simulation time, each codes of ADC is sampled 3 times to make sure both DNL and INL are under $\frac{1}{2}LSB$.

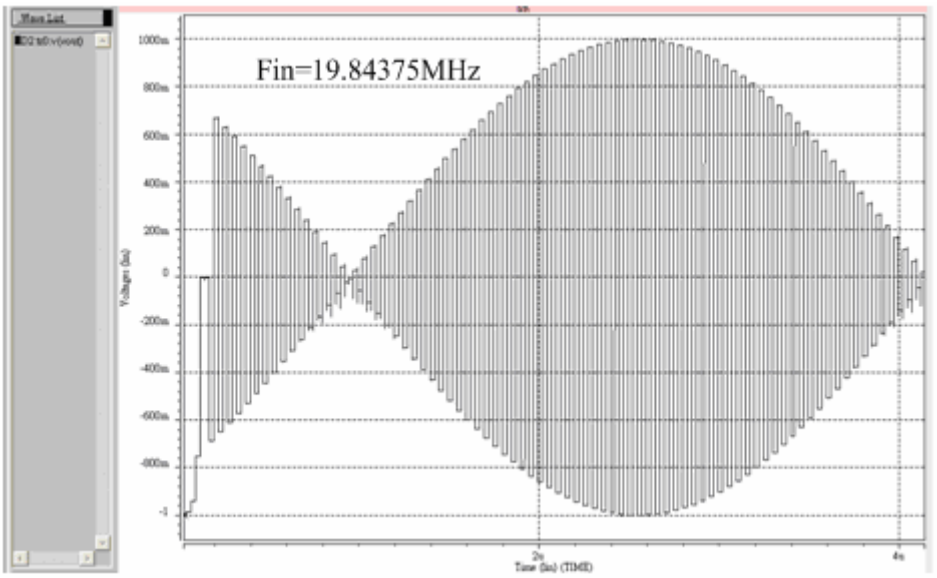


Figure 4.36 The output waveform of the pipelined ADC with an input frequency of 19.84375MHz.

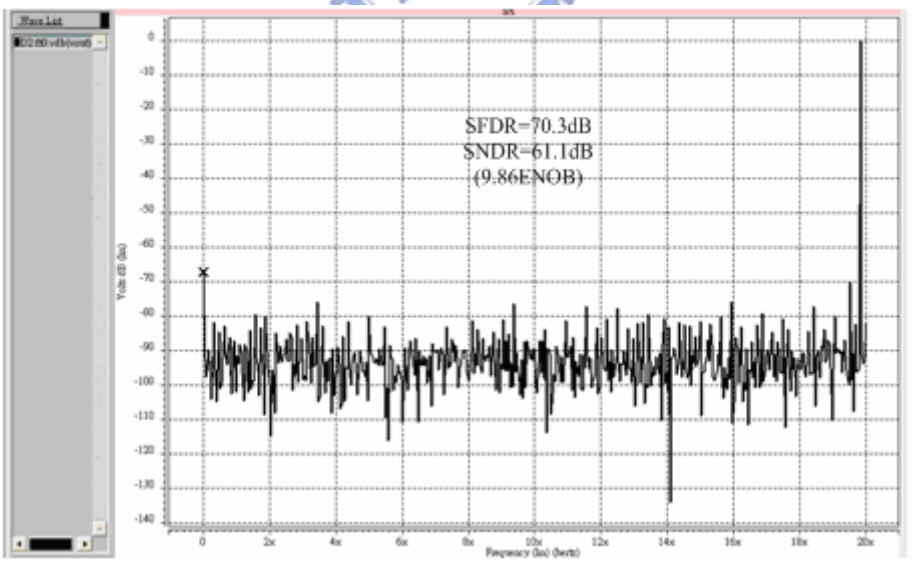


Figure 4.37 The FFT analysis of the pipelined ADC with an input frequency of 19.84375MHz.

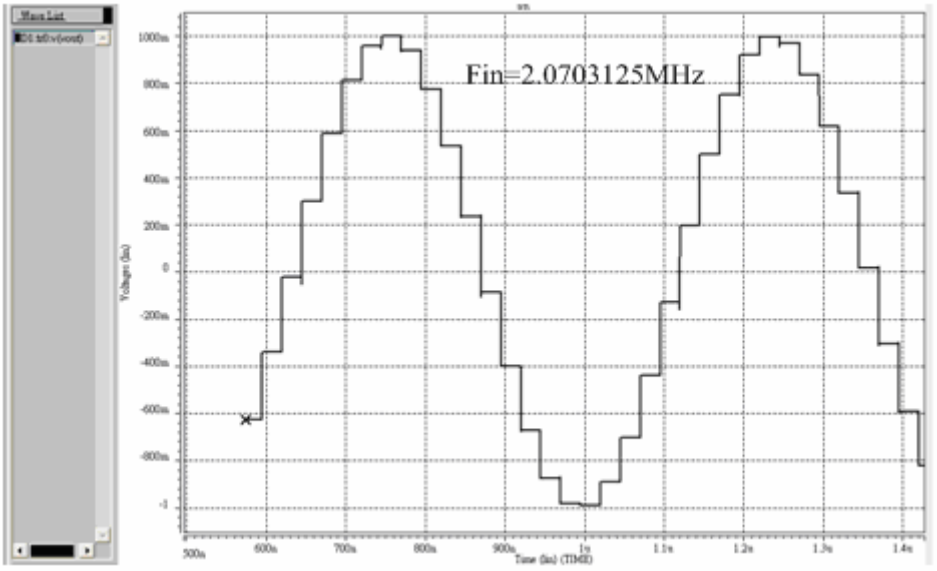


Figure 4.38 The output waveform of the pipelined ADC with an input frequency of 2.0703125MHz.

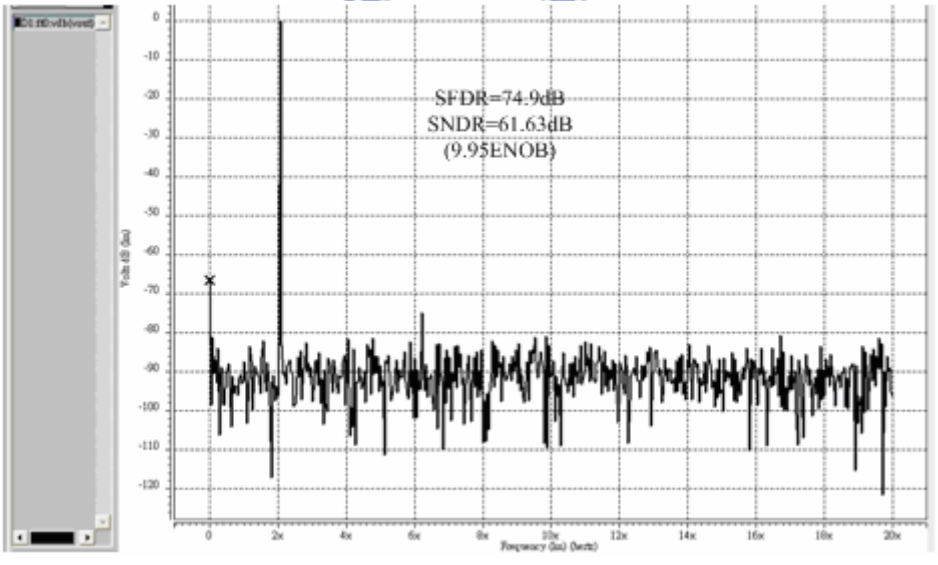


Figure 4.39 The FFT analysis of the pipelined ADC with an input frequency of 2.0703125MHz.

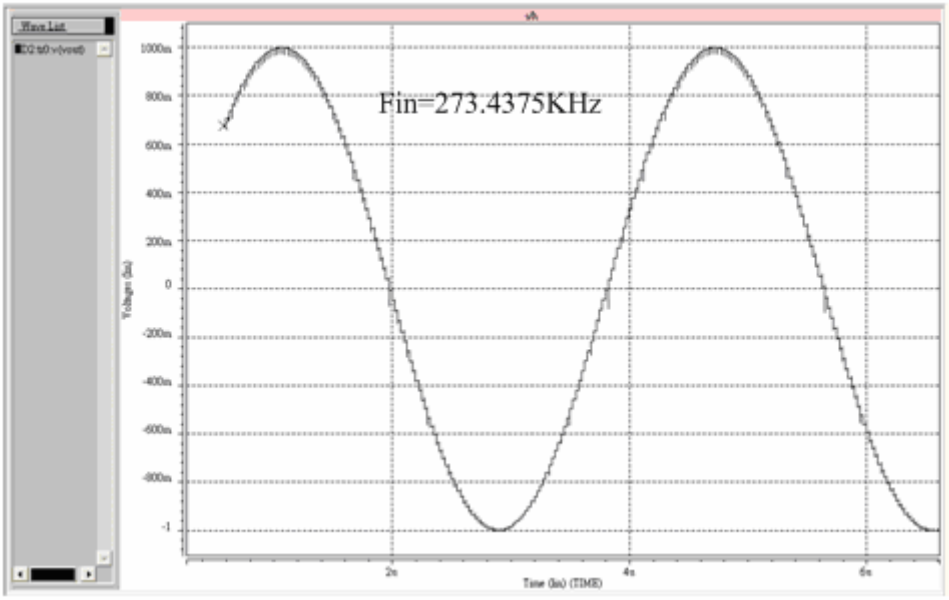


Figure 4.40 The output waveform of the pipelined ADC with an input frequency of 273.4375KHz.

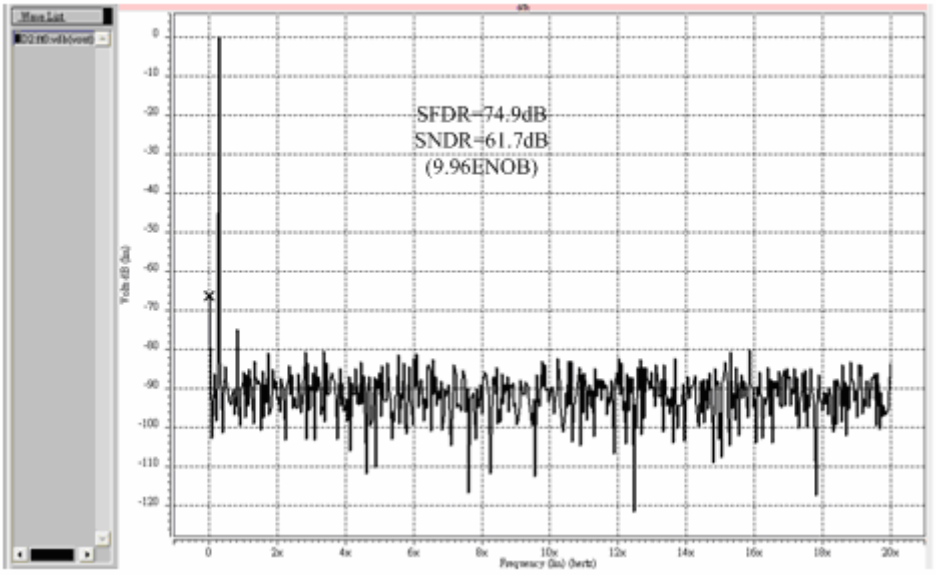


Figure 4.41 The FFT analysis of the pipelined ADC with an input frequency of 273.4375KHz.

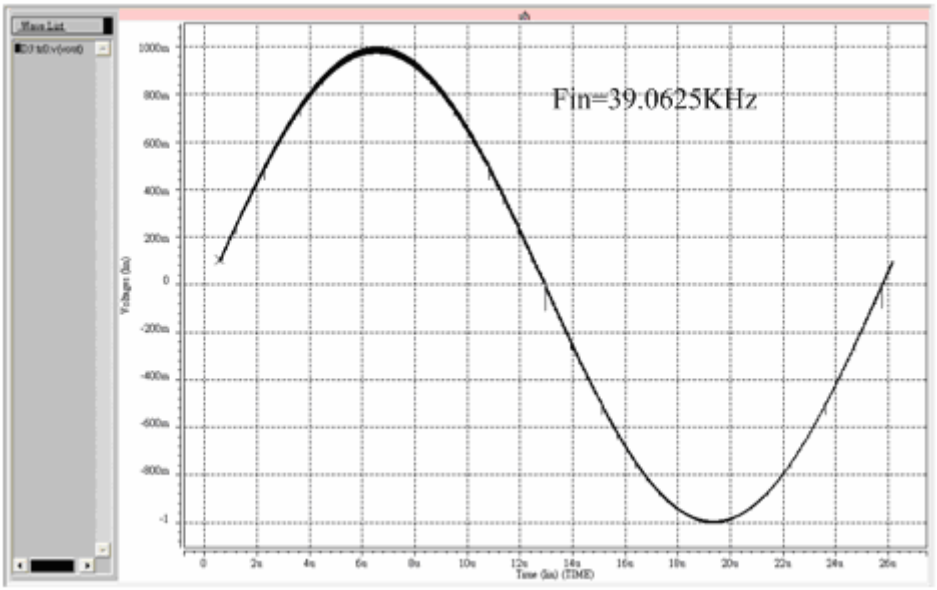


Figure 4.42 The output waveform of the pipelined ADC with an input frequency of 39.0625KHz.

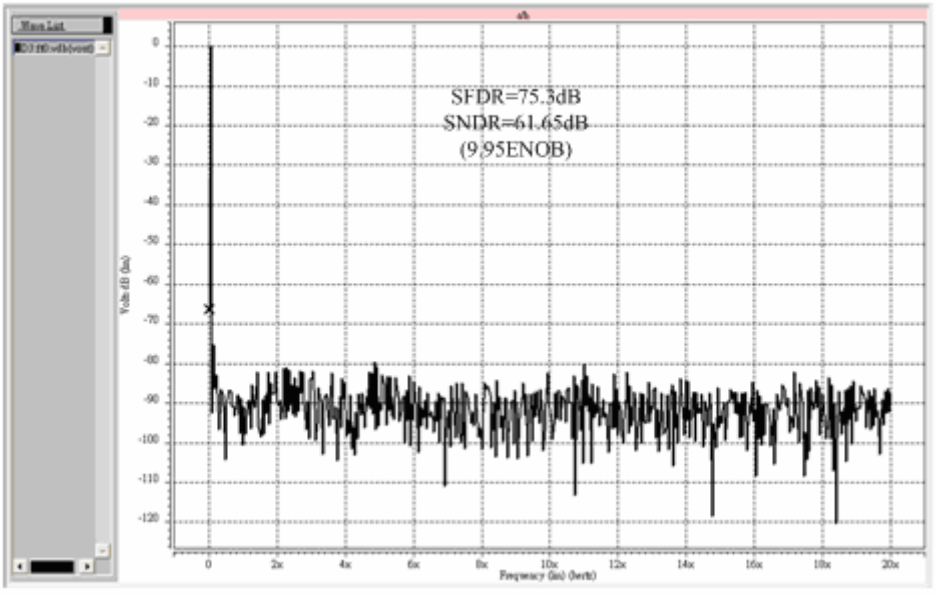


Figure 4.43 The FFT analysis of the pipelined ADC with an input frequency of 39.0625Hz.

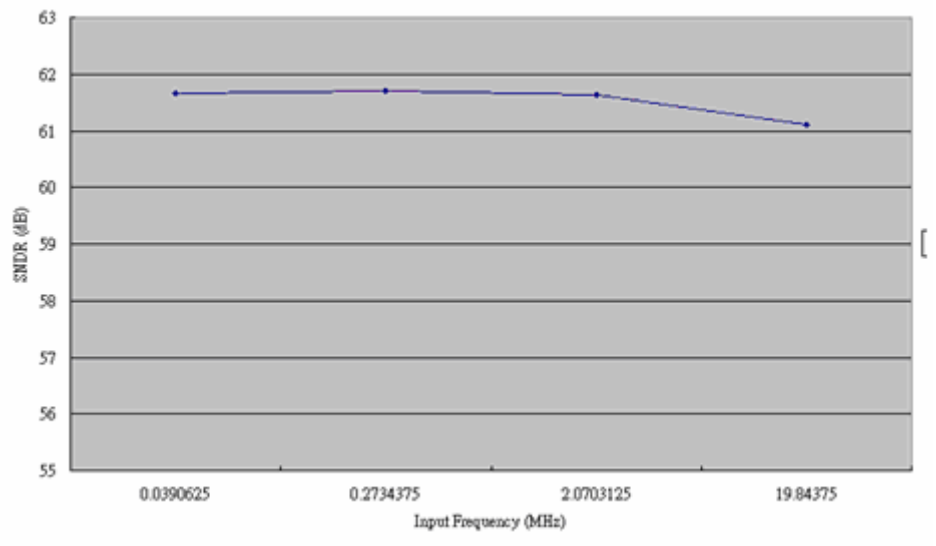


Figure 4.44 SNDR versus Input frequency.

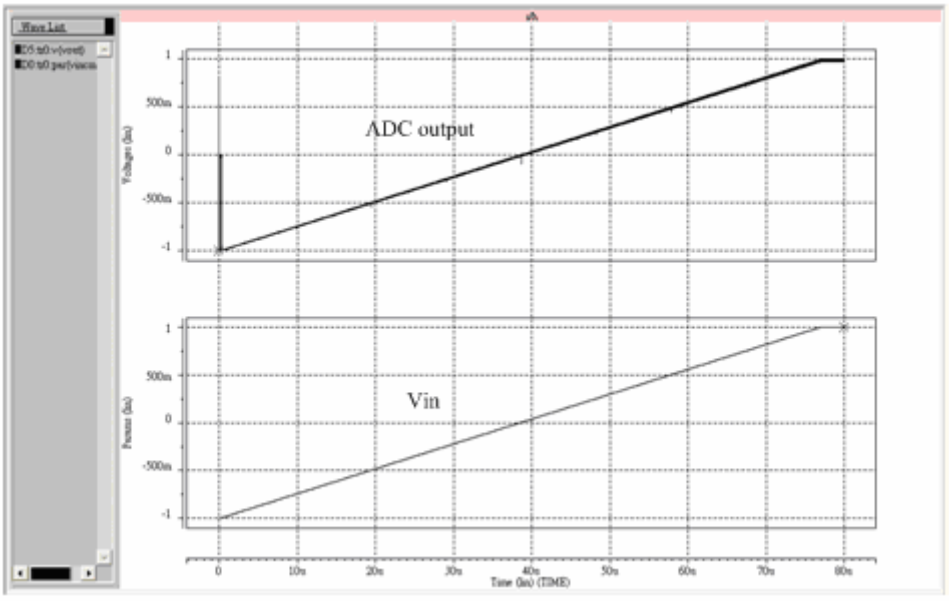


Figure 4.45 Ramp response of the pipelined ADC.

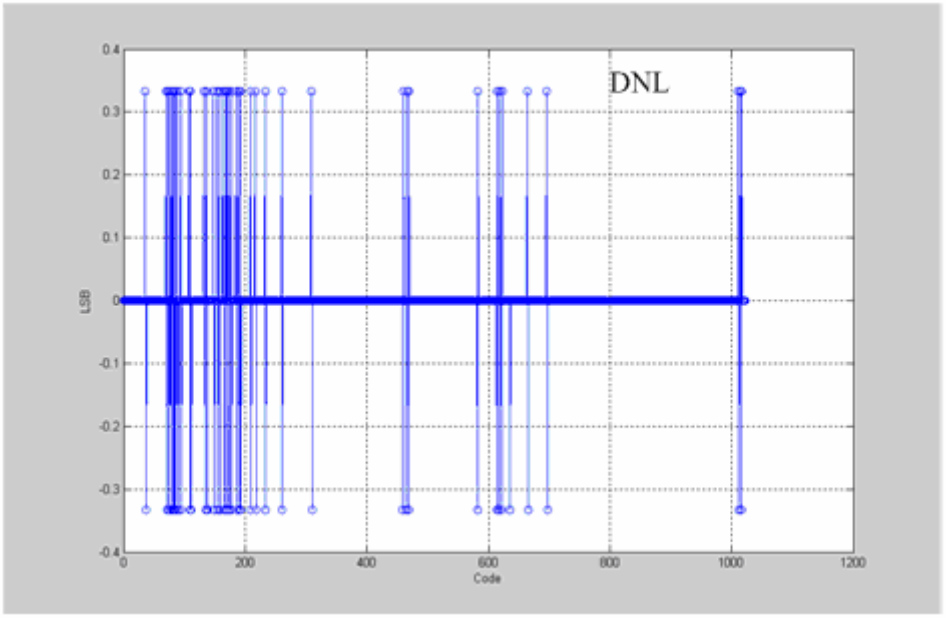


Figure 4.46 DNL of the pipelined ADC.

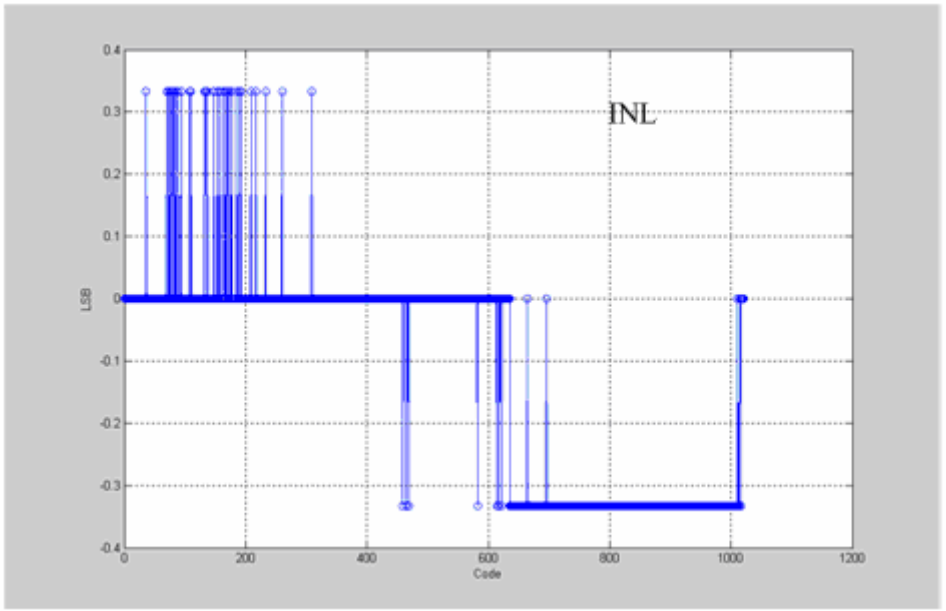


Figure 4.47 INL of the pipelined ADC

Table 4.3 Summary of the pipelined ADC

Parameter	Value
Power supply	3.3V
Architecture	Pipelined ADC
Resolution	10-bit
Operation frequency	40MHz
Input swing (differential)	±1V
SNDR @ Nyquist-rate	61.1dB
Power dissipation	≈100mW
Technology	TSMC 0.35-um 2P4M CMOS process

Chapter 5
Conclusions

5.1 CONCLUSIONS

The operational amplifier is a very important part in the pipelined ADC, and limits the performance of ADC. Under the consideration of accuracy and speed, the new operational amplifier with positive feedback is proposed. With the simulation of the HSPICE, the new amplifier performs high gain and high speed, and is suitable for low power applications. The problems of stability are critical, when designing the positive feedback circuits. In our design, we minimize the positive feedback quantity to make sure the stability. The other parts of the pipelined ADC are carefully designed. It reduces the power, area and reference voltage, and increases the speed and accuracy by using some techniques or idea.

5.2 FUTURE WORK

In this research, there still exist many issues which limit performance of pipelined ADC. First, a better clock arrangement can reduce the area and power. Second, the dynamic comparator should design careful, because it will induce the kick-back noise, although we reduce this affection by arranging clock and changing the output latch of comparator. However, this issue will be more critical in higher speed and resolution applications. Third, we should learn more about the proposed amplifier to achieve higher performance and reduce the non-ideal factor.

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簡歷

姓　　名：黃傑忠

學　　歷：

新竹省立高級中學　　(84年9月~87年6月)

國立中央大學電機工程學系　　(87年9月~91年6月)

國立交通大學電子研究所碩士班　　(92年9月~94年6月)

研究所修習課程：

類比積體電路 I	吳介琮教授
類比積體電路 II	吳重雨教授
數位積體電路	柯明道教授
積體電路設計實驗 I	李鎮宜教授
積體電路設計實驗 II	李鎮宜教授
積體電路之靜電放電防護設計特論	柯明道教授
低功率與高速積體電路設計	周世傑教授
計算機結構	黃俊達教授

永久地址：苗栗縣頭份鎮東庄里六鄰民族路380號

Email： joeey.ee92g@nctu.edu.tw

u3470618@cc.ncu.edu.tw

m9211667@alab.ee.nctu.edu.tw