國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

應用於正交分頻多工為基礎的無線存取系統之低複雜度頻率同步器

A Low Complexity Frequency Synchronizer for OFDM-based Wireless Access Applications

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中華民國九十四年七月

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摘要

在達到高資料傳輸率及低功率消耗的無線基頻設計上，使得能有效的應用在高速及攜帶式的無線通訊產品。而近年來，超寬頻技術被發展成應用在高速資料傳輸上，如無線 USB 2.0 等。

而在解決頻率漂移的頻率同步器上，為了達到高於 500MSamples/s 的處理能力，我們採用了平行化的架構。因此目前頻率同步器的主要挑戰即為在達到高速的情況下，降低其複雜度並且保持系統的效能。本論文的主旨即針對以正交分頻多工為基礎的無線存取系統而設計一個低複雜度之頻率同步器。此設計結合了以資料分割為基礎的相關性演算法，power aware 的概念以及近似特性的補償機制。而設計本身則提供了一個可以減少不必要的運算量同時達到系統可接受的效能損失的方法。甚至，我們可以在環境較好的情況下，利用 power aware 的概念來減少更多的功率消耗。基於資料分割的演算法，我們可以用單一路徑的頻率同步器來達到 528MSamples/s 的處理能力及 480Mb/s 的資料傳輸率。而由模擬結果可得知，在達到 10% PER 的 IEEE 802.11a WLAN 系統下和 8% PER 的 LDPC-COFDM 及 MB-OFDM UWB 的系統下，其效能損失可以限制在 0.6dB SNR 以下。而設計實現後，在達到 528MSamples/s 處理能力下，其功率消耗在 0.18μm 製程中可以減少到原本傳統設計的 69.4%～75.6%。

A Low Complexity Frequency Synchronizer for OFDM-based Wireless Access Applications

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ABSTRACT

The wireless baseband design achieving high data rates and low power dissipation leads the high efficiency of transmission speed and battery life of wireless access applications. Recently the ultra-wideband (UWB) is hotly developed for hundreds Mb/s speed and wireless USB 2.0 applications. In the baseband frequency synchronizer, which solves the carrier frequency offset (CFO), needs to be the parallel architecture to stably achieve > 500MSamples/s throughput rate. Hence the main challenge of the present frequency synchronizer design becomes simultaneously achieving high throughput rate, low hardware complexity, low system packet error rate (PER) demanded by UWB system. In this thesis, a low complexity frequency synchronizer comprises data-partition-based correlation algorithms, power-aware concept and approximate compensation scheme is proposed for OFDM-based wireless access systems. It provides a methodology to reduce redundant computation complexity with an acceptable performance loss; and further, we can reduce more power consumption in the better channel condition by concept of power-aware. Based on data-partition algorithm, a single-path frequency synchronizer with parallel CFO compensators is developed to achieve 528MSamples/s throughput for the 480Mb/s UWB design. Simulation results show the synchronization loss of the proposed design can be limited to 0.6dB SNR for 10% PER of IEEE 802.11a WLAN system and 8% PER of LDPC-COFDM and MB-OFDM UWB systems. The implementation result shows the proposed low-complexity scheme achieving 528MSamples/s throughput rate can reduce 69.4% ~ 75.6% power consumption of a conventional parallel approach in 0.18μm CMOS process.

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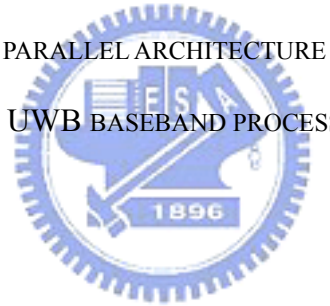

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Chapter 1.
Introduction

In this chapter, the motivation of this research and the concepts of OFDM systems will be introduced. And we also introduce the features of the current approaches. Finally, thesis organization will be listed in the end of this chapter.

1.1 Motivation

OFDM-orthogonal frequency division multiplexing is an up and coming modulation technique for transmitting large amounts of digital data over a radio wave; this concept of using parallel data transmission and frequency division multiplexing was drawn firstly in 1960s [1] -[2]. Due to the high channel efficiency and low multipath distortion that make high data rate possible, OFDM is widely applied in the new generation wireless access systems such as wireless local/personal area network (WLAN/WPAN) [3]-[4] and digital broadcasting systems [5]-[6]. The technique of using orthogonal subcarriers saves the bandwidth, but increases the sensitivity to synchronization errors. Therefore, synchronization is an important issue for OFDM-based systems.

Carrier frequency offset (CFO) is the main data distortion problem in OFDM systems. The reason causing the CFO in wireless communication is the radio frequency (RF) circuit mismatch between the transmitter and the receiver [7]. This effect will destroy the orthogonal property of these subcarriers and the data can't be received perfectly, hence degrade the system performance.

Recently, OFDM-based wireless ultra-wideband (UWB) technology has received attention from both the academia and the industry. It provides high data rates up to 480Mb/s

and low power requirements below 323mW for IEEE 802.15.3a wireless PAN application [8]. In the past ten years, several frequency synchronization schemes were exploited to enhance system performance [10]-[14]. However, the low-power technique was not the main concern or not efficient enough for UWB. In OFDM-base WLAN designs, full FFT symbols are generally used for fine CFO estimation [9]-[11]. The needed memory consumes high power (110mW) even in a power-optimized approach [9]. As system migrates from 20MHz WLAN to 528MHz UWB, it will become more difficult to eliminate the power enlarging with increasing throughput.

The object of this thesis is to design a low power frequency synchronizer, which eliminates the time-domain compound signal distortion caused by CFO. With respect to different requirements of different application systems, the proposed frequency synchronizer consists of decision-mechanism CFO estimation scheme for general OFDM system [3]; and further, a data-partition-based, power-aware CFO estimation scheme and an approximate CFO compensation scheme for high-speed OFDM-based UWB system [4]. It can reduce redundant computation of synchronization algorithm according to performance requirement. In the further, we can reduce more power consumption in the better channel condition by power-aware concept. Simulation results show the power elimination efficiency is 68.5% ~ 71.4% and the paid performance loss can be limited to 0.04 ~ 0.6dB for typical 8% packet-error-rate (PER) for UWB and 10% PER for WLAN. The efficient low power scheme of frequency synchronizer containing performance trade-off and architecture design will be described completely.

1.2 Introduction of OFDM systems

Frequency division multiplexing (FDM) is a technology that transmits multiple signals simultaneously over a single transmission path, such as a cable or wireless system. Each signal travels within its own unique frequency range (carrier), which is modulated by the data

(text, audio, video, etc.). Orthogonal FDM's (OFDM) spread spectrum technique distributes the data over a large number of carriers that are spaced apart at precise frequencies (subcarriers). This spacing provides the "orthogonality" in this technique which prevents the demodulators from seeing frequencies other than their own. The benefits of OFDM are high spectral efficiency, resiliency to RF interference, and lower multi-path distortion. Because of these advantages, OFDM is widely applied in high-speed communication systems. For example : High-speed wire communication systems such as ADSL, VDSL, and XDSL; wireless broadcasting systems such as DAB [5] and DVB [6]；high-speed wireless local area networks (WLAN) such as IEEE 802.11a [3], Hiperlan/2 [15]；OFDM is also the main candidate for the Ultra-Wideband (UWB) systems [4].

The basic idea of OFDM is the parallel-transmitted orthogonal subcarriers. Figure 1.1 shows the subcarriers of an OFDM symbol in the time interval T. The lowest frequency of subcarrier is f_1, which equals the inverse of T. Each subcarrier has exactly an integer number of cycles in the interval T and the difference of cycle numbers between any two adjacent subcarriers is exactly one. This is the property of orthogonal subcarriers.

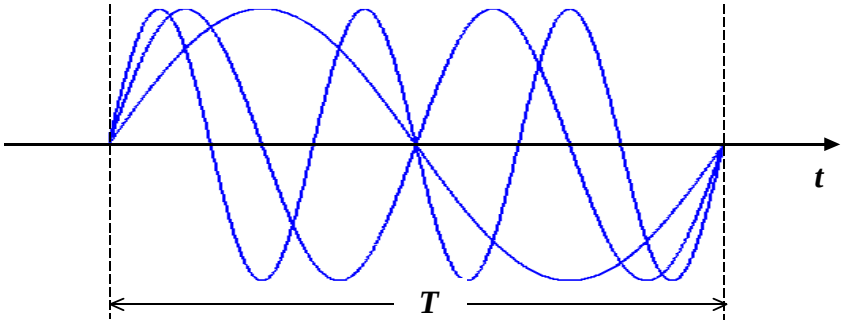


Figure 1.1 Example of three orthogonal subcarriers of an OFDM symbol

In OFDM the subcarrier pulse used for transmission is chosen to be rectangular. This has the advantage that the task of pulse forming and modulation can be performed by a simple Inverse Discrete Fourier Transform (IDFT) seen in Figure 1.2, which can be implemented

very efficiently as a Inverse Fast Fourier Transform (IFFT) [16]. Accordingly in the receiver we only need a FFT to reverse this operation. According to the theorems of the Fourier Transform, the rectangular pulse shape will lead to a $sin(x)/x$ type of spectrum of the subcarriers. In the Figure 1.3(a) and (b), the frequency interval between any two adjacent subcarriers is f_1 and the spectrums of the subcarriers are not separated but overlap. The reason why the information transmitted over the carriers can still be separated is the so called orthogonality relation giving the method its name. By using an IFFT for modulation we implicitly chose the spacing of the subcarriers in such a way that at the frequency where we evaluate the received signal (indicated as arrows) all other signals are zero. In order for this orthogonality to be preserved, the following must be true:

1. The receiver and the transmitter must be perfectly synchronized. This means they both must assume exactly the same modulation frequency.
2. The analog components, part of transmitter and receiver, must be of very high quality.
3. There should be no multipath channel.

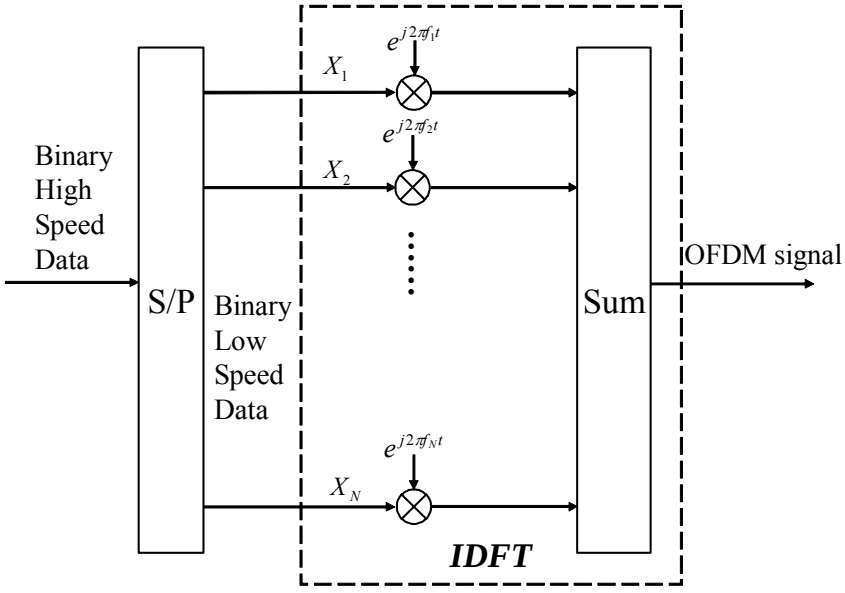


Figure 1.2 OFDM modulator using IDFT

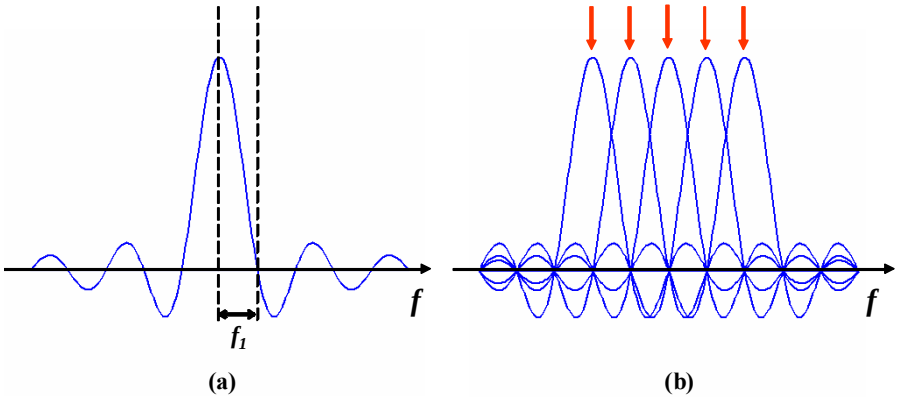


Figure 1.3 Spectrum of (a) a single sub-channel

(b) Orthogonal sub-channels of OFDM systems

In particular the last point is impossible. Fortunately there is an easy solution to deal with multipath delay spread. By dividing the original data stream into several subcarriers, symbol duration extends, which reduces the relative delay spreading. In order to eliminate multipath fading completely, a cyclic prefix (CP) as a guard interval (GI) is introduced after IFFT in OFDM systems. The length of GI is chosen larger than the expected delay spread to avoid ISI. CP is applied to preserve the orthogonality to avoid ICI. The format of OFDM symbol can be shown in Figure 1.4.

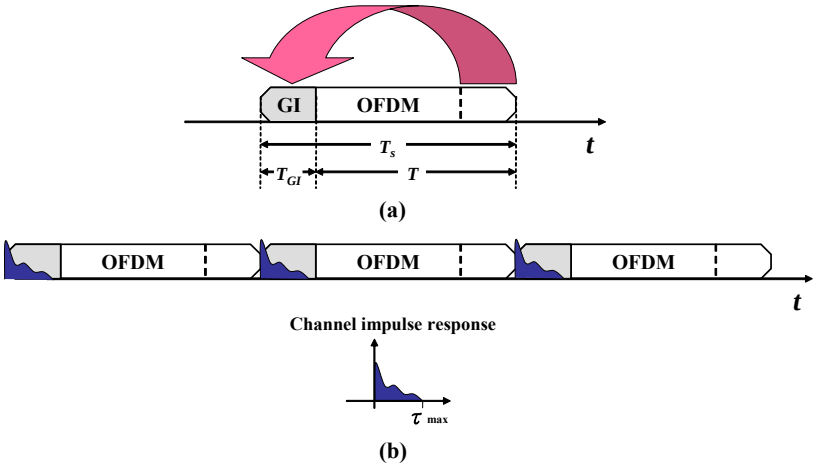


Figure 1.4 (a) a OFDM symbol format

(b) ISI caused by multipath fading channel, $T_{GI} > \tau_{max}$

Forward error correction (FEC) is the other main principle of OFDM system. In OFDM transmission, frequency-selective-fading causes different influence on each subcarrier. That is, some data subcarriers may completely be lost due to deep fading, which dominates the overall system performance. FEC is applied to solve this problem. Errors caused by weak subcarriers can be corrected by the coding information. OFDM systems with FEC scheme are often referred as coded OFDM (COFDM) systems. Figure 1.5 shows the block diagram of a general COFDM system.

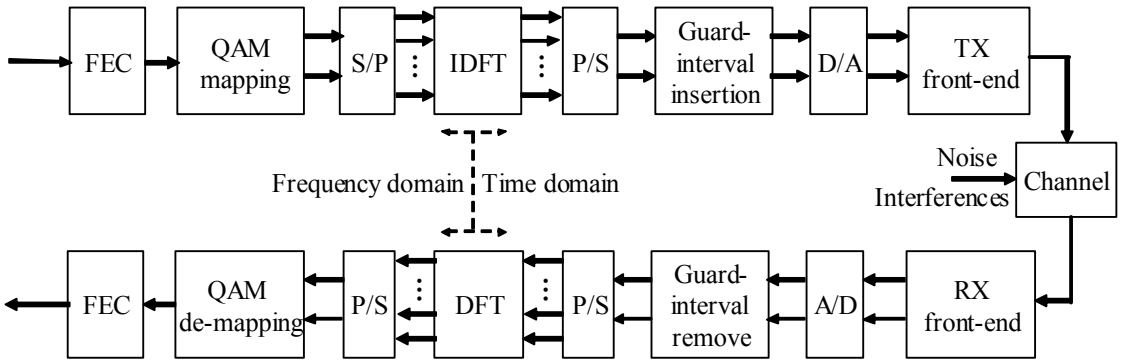


Figure 1.5 Bock diagram of a simple OFDM system

1.3 Organization of This Thesis

This thesis is organized as follows. In Chapter 2, the simulation platform and detail specifications of the IEEE 802.11a WLAN, single-band LDPC-COFDM UWB system [17] and the multi-band OFDM-based Ultra-Wideband [8] system will be introduced. Algorithms of the proposed frequency synchronizer for different requirements will be described in Chapter 3 and Chapter 4 respectively. The simulation result and performance analysis will be discussed in Chapter 5. Chapter 6 will introduce the design methodology, hardware architecture, and the chip summary of the proposed design. Conclusion and future work will be given in Chapter 7.

Chapter 2.
System Platform

In this chapter, we introduce the three system platforms for design analysis and performance simulation. The first one is IEEE 802.11a physical layer (PHY) [3]; the second one is single-band LDPC-COFDM Ultra-Wideband (UWB) system [17]; the other one is IEEE 802.15.3a UWB with multi-band OFDM modulation proposed by Texas Instrument (TI) [4]. The detail block diagram, system specification and preamble format will be described as follows.

2.1 Introduction to IEEE 802.11a System

2.1.1 IEEE 802.11a basic

IEEE 802.11a is an OFDM-based indoor WLAN system. The block diagram of the baseband transceiver can be illustrated in Figure 2.1. The system platform includes a COFDM modem and an indoor radio channel model. The COFDM modem comprises a 64-point DFT-based QAM-OFDM modem and a forward-error correction (FEC) coding. The 64 subcarriers contain 48 data carriers and 4 pilot carriers, the others 16 carriers called as null band are set to zero. The OFDM symbol time T_S is 3.2μs, the bandwidth of the subcarriers is $1/T_S$ = 312.5 KHz and total bandwidth is N/T_S = 20 MHz. The indoor radio channel model comprises a Rayleigh fading channel and AWGN. The supported data rate is from 6Mbits/s to 54 Mbits/s with coding rate equals 1/2, 2/3 and 3/4. The system parameters can be listed in Table 2.1.

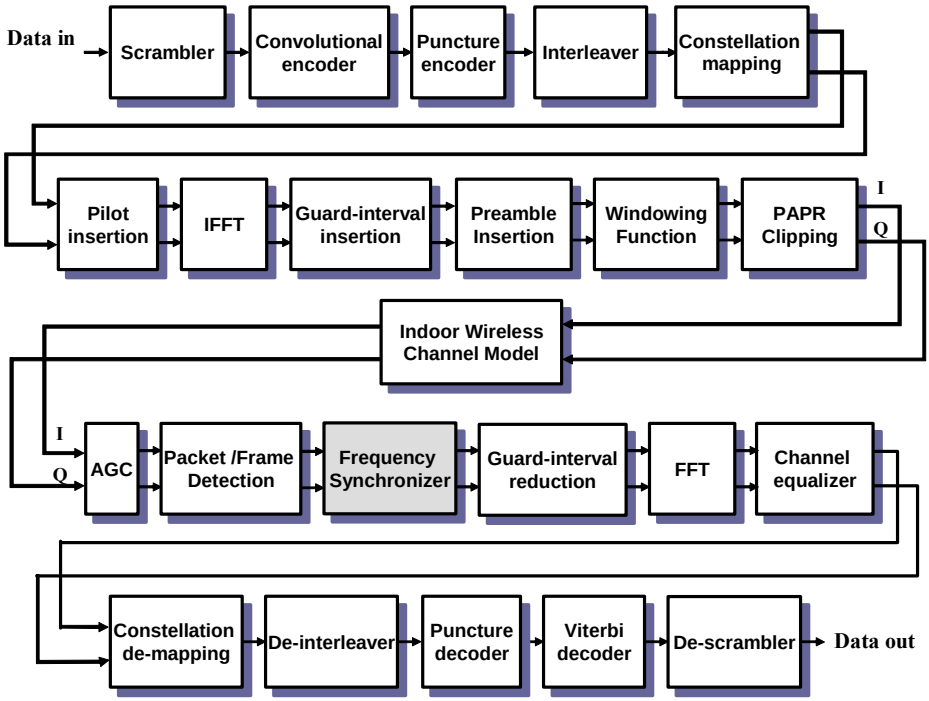


Figure 2.1 System platform of IEEE 802.11a PHY

Table 2.1 System parameters of IEEE 802.11a PHY

Constellation mapping method	BPSK, QPSK, 16QAM, 64QAM
Date rate (Mbits/s)	6, 9, 12, 18, 24, 32, 48, 54
FEC coding rate (R)	1/2, 2/3, 3/4
FFT size (N)	64
Number of used subcarriers (N_{ST})	52
Number of data carriers (N_{SP})	48
Number of pilot carriers (N_{SD})	4
Bandwidth (MHz)	20
Subcarrier bandwidth (KHz)	312.5 (20 MHz/64)
IFFT/FFT period (T_{FFT})	3.2us
GI duration (T_{GI})	0.8us (T_{FFT}/4)
PLCP preamble duration	16us (T_{SHORT} + T_{LONG})

The IEEE 802.11a provides 8 kinds of data rates up to 54 Mb/s by using QAM modulation and convolutional code. The system adopts packet transmission and the PHY protocol data unit (PPDU) frame of IEEE 802.11a shown in Figure 2.2. The PPDU frame format includes the physical layer convergence procedure (PLCP) Preamble, Header and Data fields. The PLCP preamble is a training sequence which is used to perform the synchronization. And the SIGNAL field is always the BPSK modulation and 1/2 coding rate FEC coding. Following the SIGNAL field is the Data field which is used to transmit the general information.

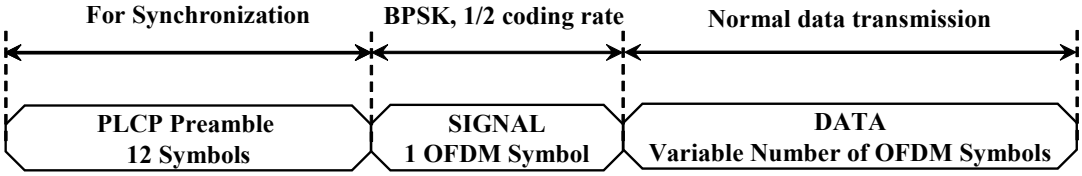
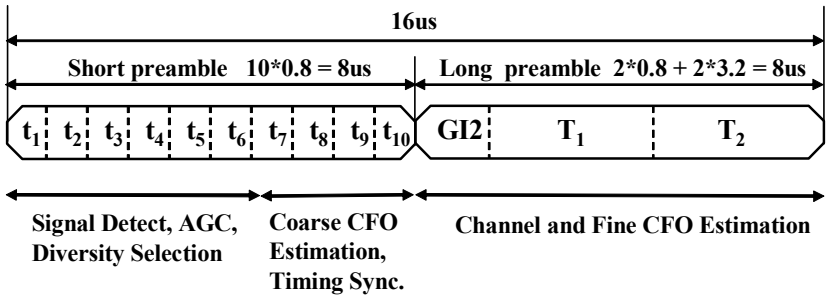


Figure 2.2 PPDU frame format

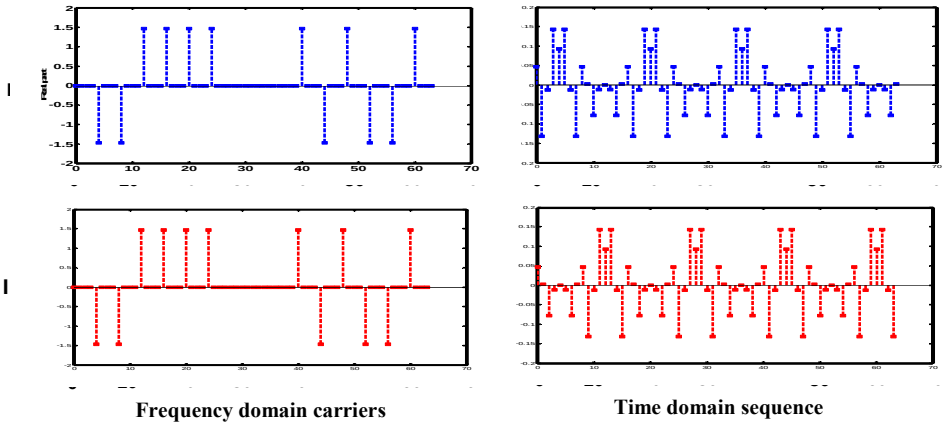
2.1.2 PLCP preamble

Figure 2.3(a) shows the structure of the IEEE 802.11a PLCP preamble. The PLCP preamble is composed of 10 identical short symbols and 2 identical long symbols. The short symbol occupies 0.8 μ sec while the long symbol occupies 3.2 μ sec. The total length of the PLCP preamble is 320 samples, each short training symbol contains 16 samples and each long training symbol contains 64 samples. The short symbols serve to do frame detection, automatic gain control, and coarse timing and frequency offset estimation. The two long symbols can be used to do channel estimation and fine CFO estimation. The generation pattern of the short preamble is shown in the left of Figure 2.3(b). These is only one data every four subcarriers. The data carrier spacing is four times larger than the carrier spacing of normal OFDM symbols. The second partition of the PLCP is the long training sequence. It is generated by the pattern in the left of Figure 2.3(c). The right is the sequence of a long

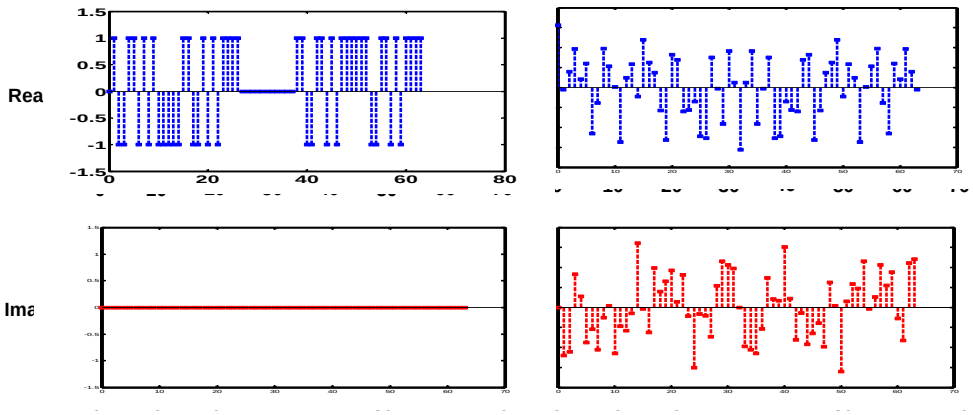
training symbol. The long training sequence contains two repeat OFDM symbols and a guard interval. The GI is two times longer than normal OFDM symbols'.



(a) PLCP preamble format



(b) Short preamble



(c) Long preamble

Figure 2.3 PLCP preamble in IEEE 802.11a

2.1.3 Transmit Center Frequency Tolerance

In the specification of IEEE 802.11a, the transmitter frequency offset is asked to be small than ±20ppm. If the receiver can achieve the same requirement, the relative frequency between the transmitter and the receiver shall be ±40ppm. The working frequency is about 5.3GHz, the frequency tolerance is ±40ppm. The maximum frequency offset is ±212KHz.

2.2 Introduction to Ultra WideBand System

2.2.1 IEEE 802.15.3a UWB basic

OFDM-based wireless ultra-wideband (UWB) technology has received attention from both the academia and the industry. The main reason for the increased attention is the Federal Communications Commission (FCC) allocated 7,500MHz of spectrum (from 3.1GHz to 10.6GHz) for use by UWB devices. It helped to create new standardization, like IEEE 802.15.3a which focuses on developing high-speed wireless communication systems for personal area network. Another reason is because this technology promises to deliver data rates up to 480Mb/s at a distance of 2 meters in realistic multi-path environments.

We have established two kinds of UWB systems in platform; one is single-band LDPC-COFDM UWB system [17] which is used low-density parity check (LDPC) FEC codec, the other one is multi-band OFDM-based UWB system [4] which is used convolutional encoder and Viterbi decoder. The block diagram of the UWB PHY is shown in Figure 2.4 which is similar to the IEEE 802.11a WLAN system. The key differences between these two systems can be listed as follow,

- OFDM symbols are interleaved across both frequency and time. An example of the time-frequency interleaving (TFI) can be shown in Figure 2.5.

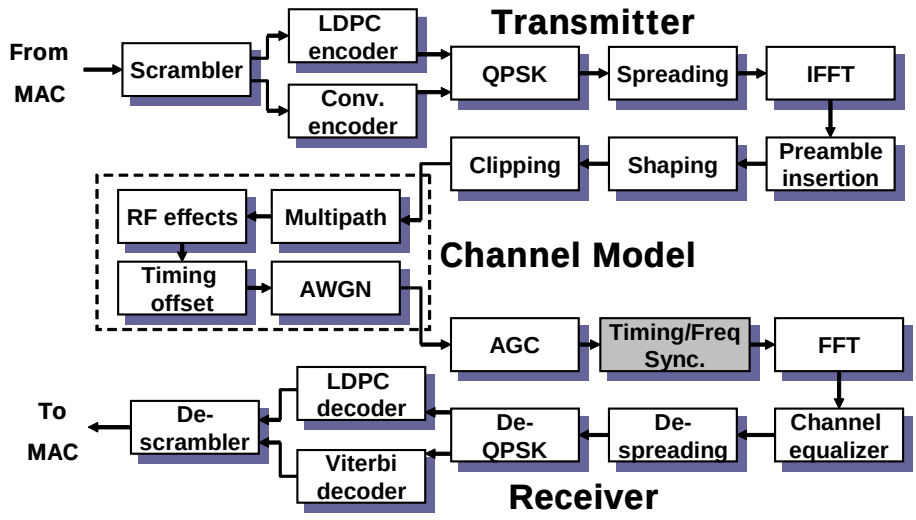


Figure 2.4 System platform of UWB PHY

- The supported data rate is up to 480Mbits/s, which is almost ten times of the data rate in IEEE 802.11a systems. A 128-point FFT is applied and only PSK (BPSK, QPSK) is used in the UWB system.
- The bandwidth is up to 528MHz, which is 26.4 times wider than IEEE 802.11a.

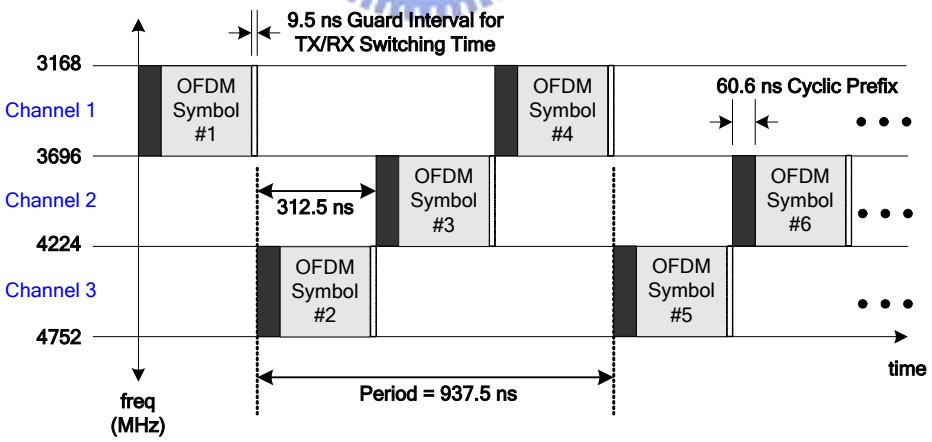


Figure 2.5 TFI example of the UWB PHY [4]

In order to achieve better system performance and higher decoding speed, (600,450) LDPC code is exploited as the kernel of error correcting mechanism in our simulation platform. The parallelism of LDPC decoding makes it easy to decode 480Mb/s data stream or even higher to

multiple Gb/s. Because of fixed 3/4 FEC coding rate with different spreading gain, we have 120Mb/s, 240Mb/s and 480Mb/s three data-rates. The coding performance can be near Shannon limit when using iterative decoding algorithm. We summarize system parameters about UWB platform that we used in Table 2.2.

Table 2.2 System parameters of the LDPC-COFDM UWB PHY

Date rate (Mb/s)	120	240	480
Constellation	QPSK	QPSK	QPSK
FFT size	128	128	128
Coding rate	3/4	3/4	3/4
Spreading gain	4	2	1
Data carrier per OFDM symbol	100	100	100
Baseband bandwidth (MHz)	528	528	528
OFDM symbol duration (ns)	312.5	312.5	312.5

The detail specifications of the multi-band OFDM UWB PHY can be listed in Table 2.3. Because of different FEC coding rate with different spreading gain, we have 8 kinds of data-rates. Figure 2.6 shows the format for the PLCP frame including the PLCP preamble, PLCP header and data-field. The PLCP preamble shall be added prior to the PCLP header to aid receiver algorithms related to synchronization, carrier-offset recovery, and channel estimation. The PLCP header is always sent at an information data rate of 53.3 Mb/s. The remainder of the PLCP frame is sent at the desired information data rate of 53.3, 80, 110, 160, 200, 320, 400 or 480 Mb/s.

Table 2.3 System parameters of the MB-OFDM UWB PHY

Constellation mapping method	BPSK, QPSK
Date rate (Mbits/s)	55, 80, 110, 160, 200, 320, 480
FEC coding rate (R)	1/2, 3/4, 5/8, 11/32
FFT size (N)	128
Bandwidth (MHz)	528
Subcarrier bandwidth (MHz)	4.125 (528 MHz/128)
Data bytes per packet	1024
IFFT/FFT period (T_{FFT})	242.42ns
Cyclic prefix duration (T_{CP})	60.61ns (T_{FFT}/4)
Guard interval duration (T_{GI})	9.47ns
PLCP preamble duration	9.375us (T_{SHORT} + T_{LONG})

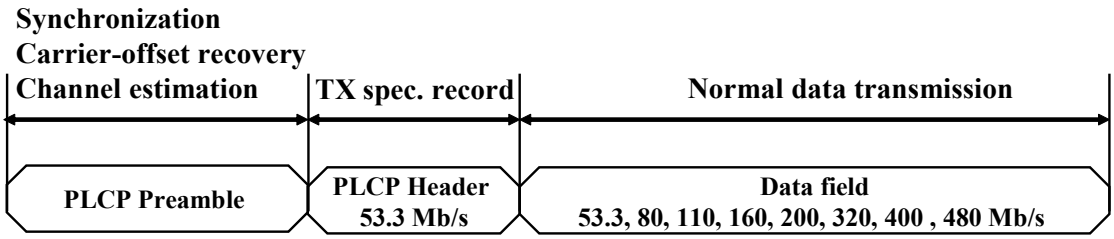


Figure 2.6 PLCP frame format

2.2.2 PLCP preamble

The signal format of the UWB PLCP preamble is shown in Figure 2.7 and it is different from IEEE 802.11a because of the time interleaving. The preamble contains 30 OFDM symbols, 21 are packet synchronization sequence, 3 are frame synchronization sequences and 6 are channel estimation sequences. The packet synchronization portion of the preamble can be used for packet detection and acquisition and coarse carrier frequency estimation. The

frame synchronization portion of the preamble can be used to synchronize the receiver algorithm within the preamble, and it also provides one sequence period per band with an inverted polarity with respect to the packet synchronization portion of the preamble. Finally, the channel estimation portion of the preamble, denoted as $\{CE_0, CE_1, \ldots CE_5\}$, shall be constructed by successively appending 6 periods of an OFDM training sequence.

Each OFDM symbol of the UWB contains 32-point pre-GI, 128-point FFT symbol and 5-point post-GI. In IEEE 802.11a system, GI is the cyclic prefix of each OFDM symbols, which is used for the concern of multipath spreading. In UWB system, cyclic prefix (CP) is for multipath concern and the GI is particularly referred to the time between band switching.

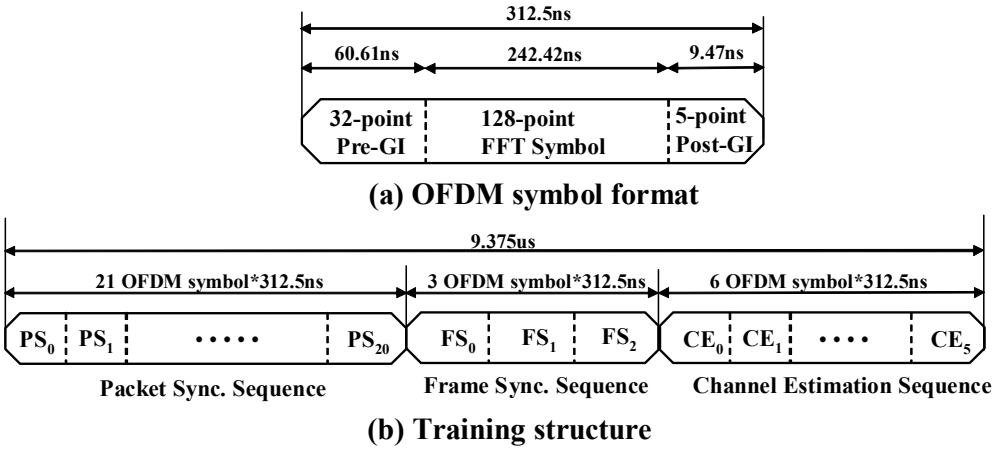


Figure 2.7 UWB PLCP preamble

2.2.3 Transmit Center Frequency Tolerance

The MB-OFDM UWB PHY operates in the 3.1~ 10.6 GHz frequency and the relationship between center frequency and band number are given by the following equation: Band center frequency = 2904 + 528 * n_b, n_b = 1…14 (MHz). This definition provides a unique numbering system for all channels that have a spacing of 528 MHz and lie within the band 3.1~10.6 GHz. Based on this, five band groups are defined, consisting of four groups of three bands each and one group of two bands. Band group 1 is used for Mode 1 devices

(mandatory mode). The remaining band groups are reserved for future use. The frequency of operation form Mode 1 devices is shown in Figure 2.8, and the band allocation is summarized in Table 2.4. In the UWB system, maximum ±20ppm CFO is expected to exist in both transmitter and receiver. So the requested CFO estimation range should be within ±40ppm (TX+RX) of 3.1~10.6 GHz RF frequency. That will be equal ±124KHz~±424KHz.

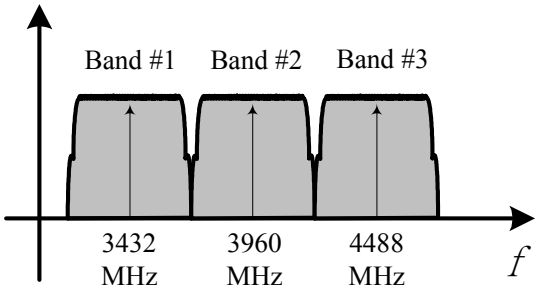


Figure 2.8 Operation frequency for Mode 1 device

Table 2.4 OFDM UWB PHY band allocation

Band Group	BAND_ID	Lower frequency (MHz)	Center frequency (MHz)	Upper frequency (MHz)
1	1	3168	3432	3696
	2	3696	3960	4224
	3	4224	4488	4752
2	4	4752	5016	5280
	5	5280	5544	5808
	6	5808	6072	6336
3	7	6336	6600	6864
	8	6864	7128	7392
	9	7392	7656	7920
4	10	7920	8184	8448
	11	8448	8712	8976
	12	8976	9240	9504
5	13	9504	9768	10032
	14	10032	10296	10560

2.3 The Indoor Wireless Channel Model

In order to simulate the data transmission in the real environment, an indoor wireless channel model is established, which includes a time-variant multipath fading [18]-[19], CFO, SCO, and AWGN. The detailed are introduced individually below

2.3.1 Multipath Fading Channel Model

In wireless communication transmission systems, transmitted signal arrives at receiver through several paths with different time delay and power decay, which is called multipath interference. Figure 2.9 shows the concept of the indoor multipath interference and its channel impulse response and frequency response. The received signal can be modeled as

$$y(t) = x(t) + \sum_{N} \beta_N \cdot x(t - \tau_N) \tag{2-1}$$

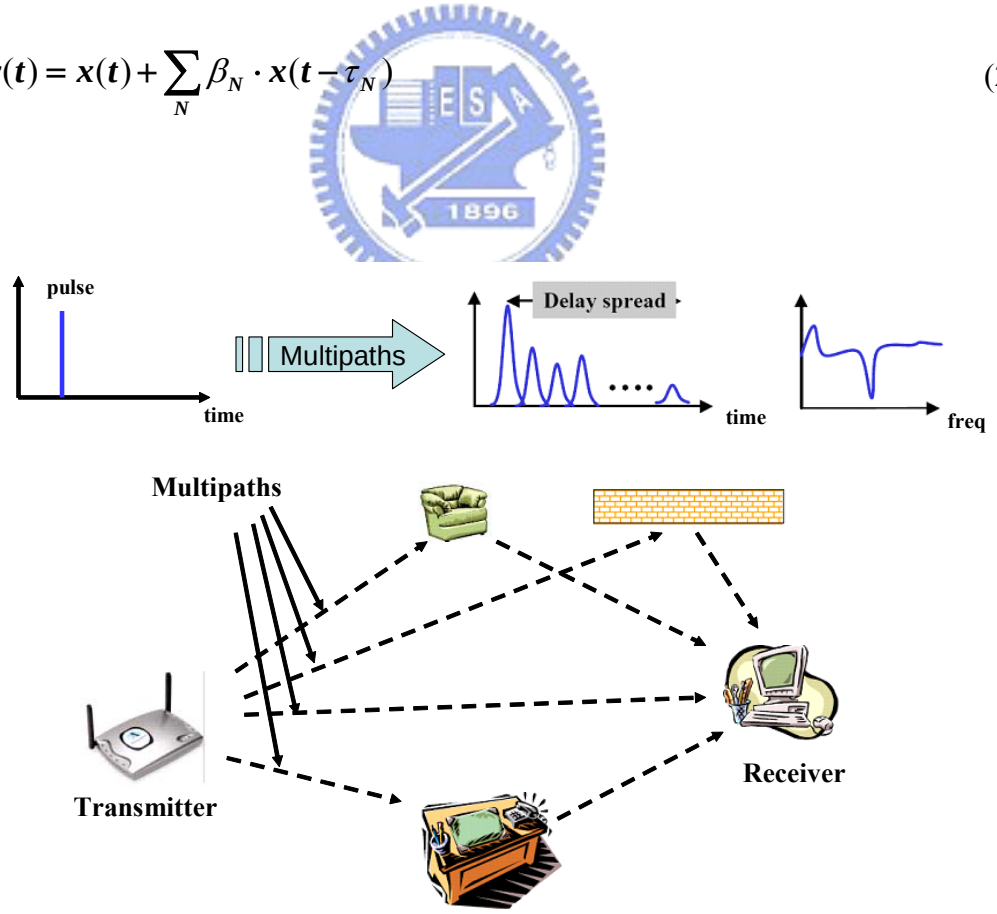


Figure 2.9 Concept of indoor multipath channel

Due to this effect, the Inter-Symbol Interference (ISI) and frequency-selective fading occur when the maximum delay spread is larger than the symbol period or the channel coherent bandwidth is smaller than the data bandwidth. Although the multipath scales tones, it also remains the orthogonal property because of cyclic prefix technique of each OFDM symbol. The applied multipath fading channel is established according to the IEEE specification. It consists of 13 independent taps, which has Rayleigh distributed magnitude, exponentially decayed power and random uniformly distributed phase [18]. Figure 2.10shows the effect of ISI and frequency-selective fading, and the channel impulse response (CIR) and the channel frequency response (CFR) with RMS delay equals 50ns are shown in Figure 2.11.

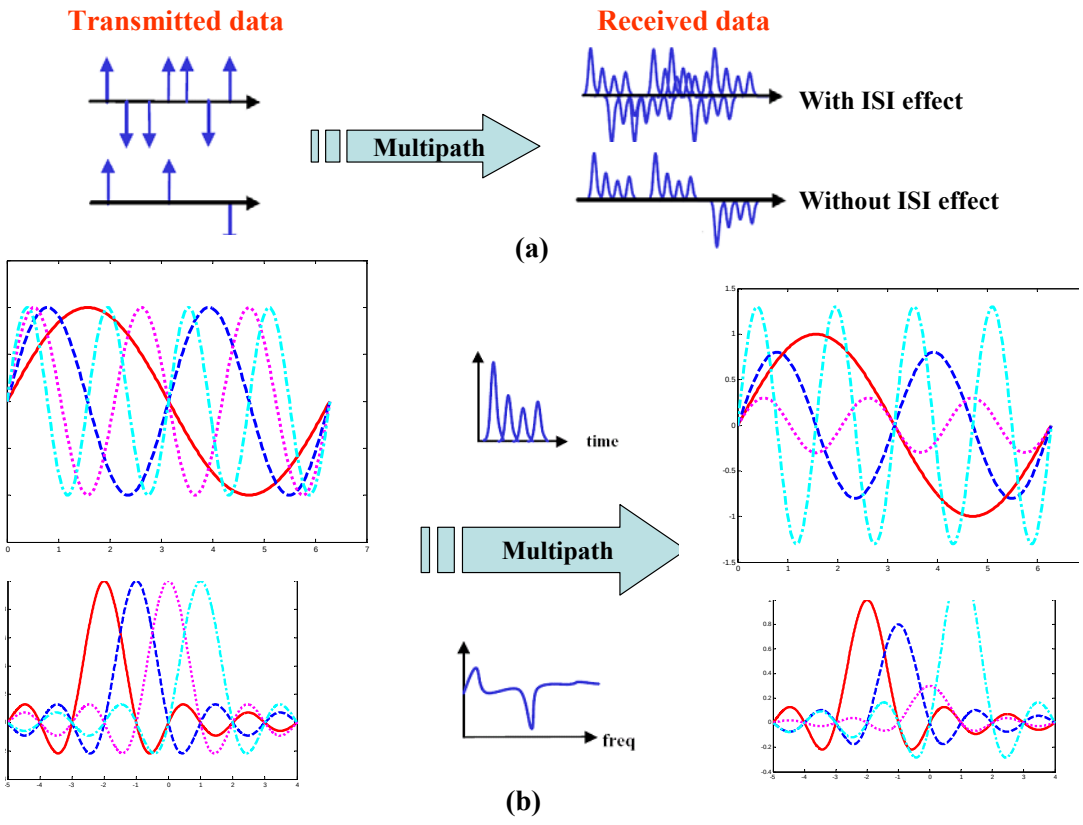


Figure 2.10 (a) ISI effect (b) frequency-selective fading channel

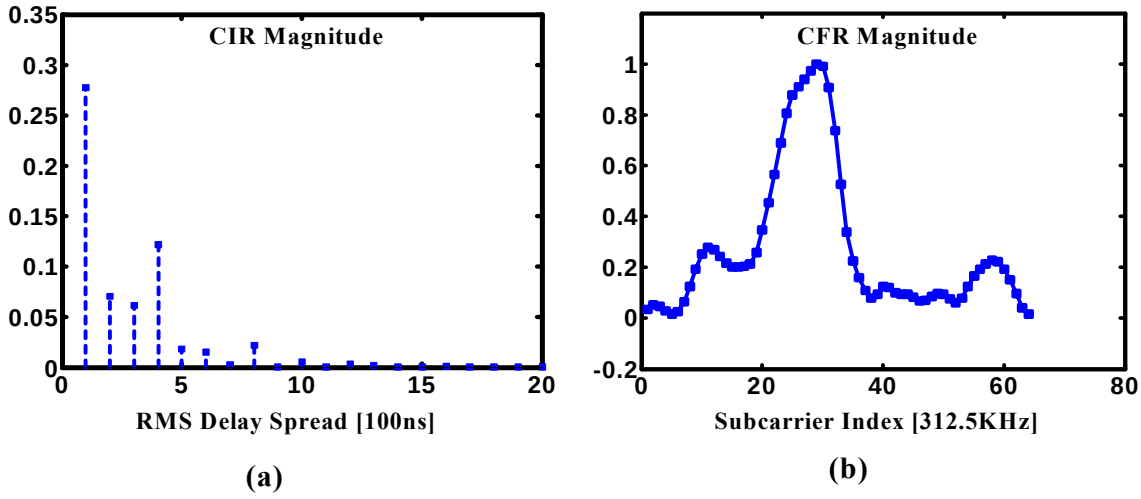


Figure 2.11 (a) CIR (b) CFR example of the multipath fading channel

2.3.2 Carrier Frequency Offset Model

The sensitivity to carrier frequency offset (CFO) is one of the main drawbacks of the OFDM system. One of the reasons causing the CFO in wireless communication is the RF circuit mismatch between the transmitter and the receiver. When the transmitter carriers the data x_t with a frequency f_1 (2.2) and the receiver gets the data with another frequency f_2 (2.3), the received data y_t contains the original data and a sinusoidal signal with a frequency $f_1 - f_2$.

$$T = x_t e^{-j2\pi f_1 t} \tag{2.2}$$

$$y_t = Te^{j2\pi f_2 t} = x_t e^{-j2\pi(f_1 - f_2)t} \tag{2.3}$$

Another reason caused the CFO is the Doppler Effect. From the Doppler equation (2.4), the received signal will not equal to the transmitted one if the relative speed between the transmitter and the receiver is not zero. There will be some frequency offset f_δ existed. Because of the v is the velocity of light, the f_δ is usually negligible as compared with the CFO caused by the circuit mismatch.

$$f' = f_0 \frac{v \pm v_r}{v \pm v_t} \tag{2.4}$$

$$f_\delta = f' - f_0 = f_0 \frac{\pm v_r \ \mu \ v_t}{v \pm v_t} \tag{2.5}$$

No matter the causes of the CFO, the behavior of the CFO in the spectrum domain is shown in the Figure 2.12. The total frequency offset is f_1-f_2+f_δ and it will be expressed as f_Δ in the thesis. Besides, the orthogonal property between each subcarrier is based on the perfect sampling on some specific frequencies in the spectrum domain. When we transmit the data without CFO, the received data will be recovered perfectly because of the influences from others subcarriers' are all zero, which shown in Figure 2.14(a). The equation (2.6) and (2.7) are the N points IDFT and DFT equation. The x_n and X_k in the (2.6) are the data of time domain and frequency domain, respectively.

$$F_N^{-1}\{X_k\} = x_n = \frac{1}{N}\sum_{k=0}^{N-1} X_k e^{2\pi jkn/N}, k = 0,1,2,\ldots N-1 \tag{2.6}$$

$$F_N\{x_n\} = X_k = \sum_{n=0}^{N-1} x_n e^{-2\pi jkn/N}, n = 0,1,2,\ldots N-1 \tag{2.7}$$

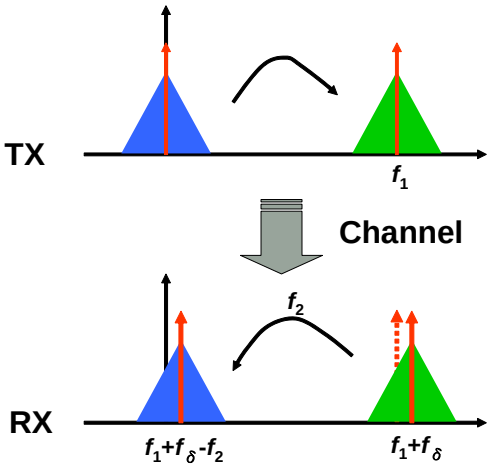


Figure 2.12 The behavior of the CFO in spectrum domain

Applying equation (2.3) to discrete time, if there is no CFO within transmission, the received data y_n is equal to the transmitted data x_n. The received data Y_k in the frequency domain are the same with the transmitted data X_k.

$$
\begin{aligned}
Y_k &= \sum_{n=0}^{N-1} y_n e^{-2\pi jkn/N} = \sum_{n=0}^{N-1} x_n e^{-2\pi jkn/N} \\
&= \sum_{n=0}^{N-1} \left\{ \frac{1}{N} \sum_{k=0}^{N-1} X_k e^{2\pi jkn/N} \right\} e^{-2\pi jkn/N} = X_k
\end{aligned}
\tag{2.8}
$$

However, the data can not be received perfectly in the CFO environment. In the time domain, the received data suffering from CFO is shown as equation (2.9), where T_s is the sampling time and the $1/NT_s$ is the subcarrier bandwidth of an OFDM symbol. We normalize the frequency offset f_Δ to the subcarrier bandwidth and $\in$ is the relative frequency offset.

$$
\begin{aligned}
y_n &= x_n e^{-j2\pi t f_\Delta} = x_n e^{-j2\pi n T_s f_\Delta} \\
&= x_n e^{-j2\pi n (NT_s) f_\Delta / N} = x_n e^{-j2\pi n \in / N}
\end{aligned}
\tag{2.9}
$$

From the publish of Moose [14], the CFO caused linear phase shift in time domain will convert to ICI in the frequency domain after passing the DFT, which shown in Figure 2.13 and Figure 2.14(b) respectively, and the relative equation is shown in (2.10).

$$
\begin{aligned}
Y_k &= \sum_{n=0}^{N-1} y_n e^{-2\pi jkn/N} = \sum_{n=0}^{N-1} y_n e^{-2\pi j(k+\in)n/N} \\
Y_k &= X_k e^{j\pi\in(N-1)/N} \cdot \{[\sin(\pi\in)]/N[\sin(\pi\in)/N]\} \\
&\quad + \sum_{l=0, l\neq k}^{N-1} X_l e^{j\pi\in(N-1)/N} \cdot e^{-j\pi(l-k)/N} \cdot \{[\sin(\pi\in)]/N[\sin\pi(l-k+\in)/N]\}
\end{aligned}
\tag{2.10}
$$

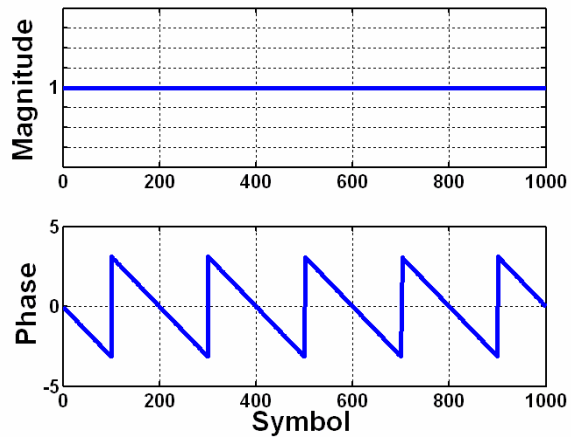


Figure 2.13 Linear phase shift

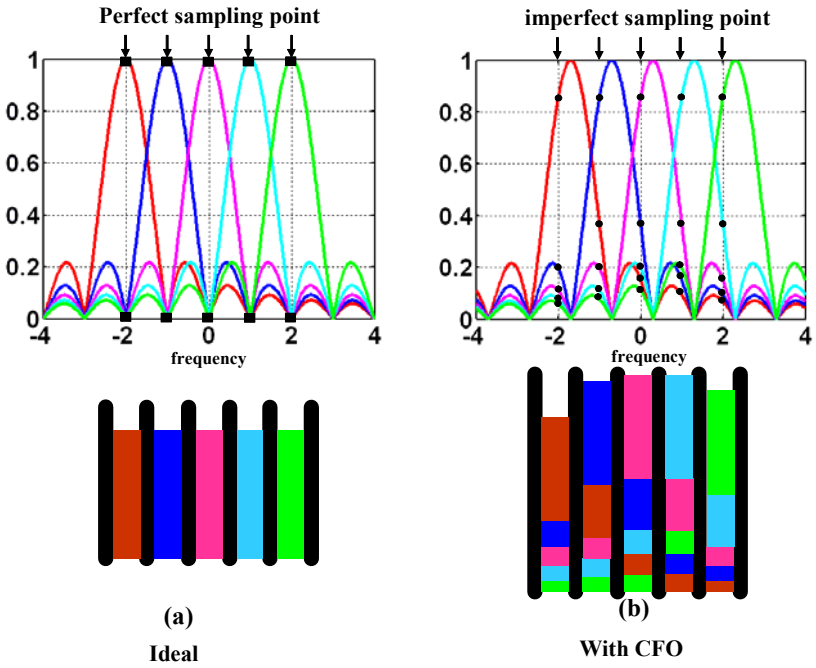


Figure 2.14 The received data (a) without CFO (b) with CFO (ICI)

In order to simulate the real CFO environment, we find a phase noise model such as Figure 2.15. According to this phase noise model, we built it in our platform. Figure 2.16 shows the example of phase noise which normal distributed with 40ppm (400 KHz) mean-CFO. In general, the mean CFO is time-invariant. However, in order to consider about more complete simulation condition, we define the mean CFO could be time-variant. We defined three kinds of CFO environments, the first one is time-invariant (TIV), and the second one is slow-variant (SV) which changed 80ppm within 50ms, and the final one is fast-variant (FV) which changed 80ppm within 5ms. Figure 2.17 shows the three CFO definitions of TIV, SV and FV. These definitions are helpful for explanation of following design.

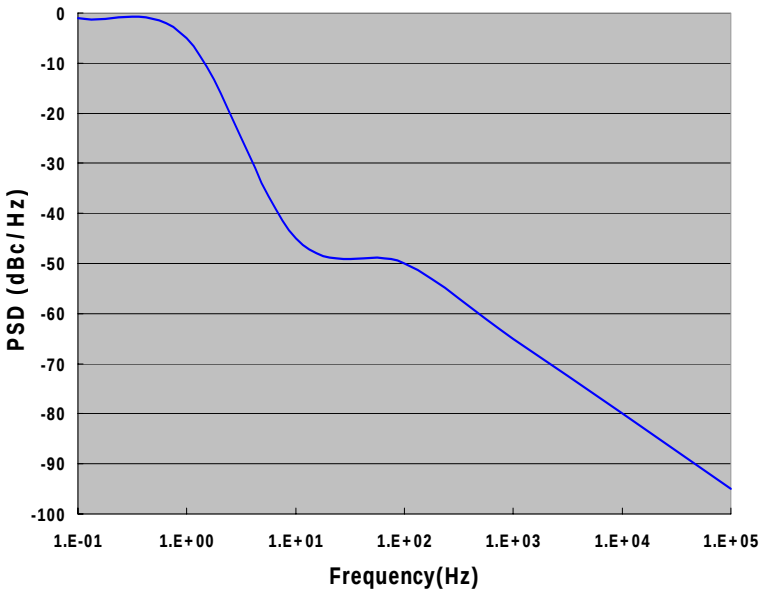


Figure 2.15 Phase noise model

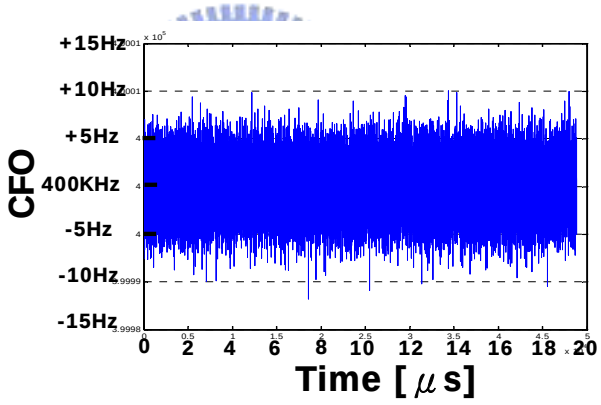


Figure 2.16 Example of phase noise

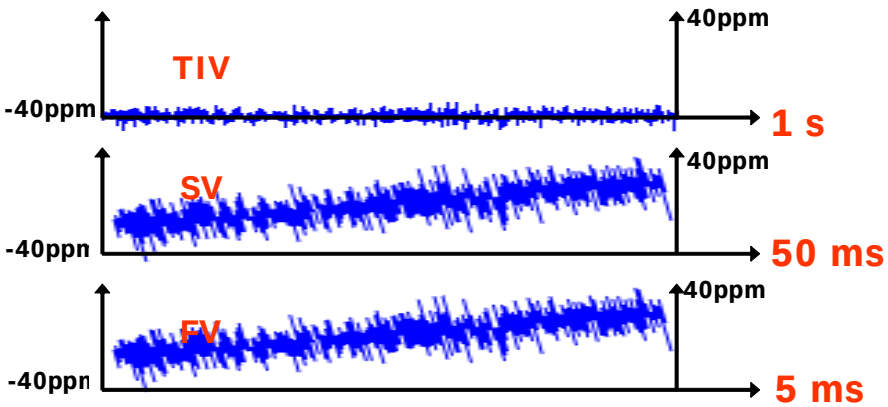


Figure 2.17 Mean CFO definition

2.3.3 Sampling Clock Offset Model

Sampling Clock Offset (SCO) is the sampling clock rate mismatch between the digital to analog converter (DAC) in transmitter and the analog to digital converter (ADC) in receiver. In the platform, the model of clock offset is built using the concept of interpolation. The input digital signals and the shifted *sinc* wave can interpolate the value between two sampling points. The received signal after ADC can be derived as equation (2.11).

$$\begin{aligned} R(nT_s) &= R_{preADC}(nT_s) * \mathrm{sinc}\left(\frac{nT_s - \Delta P_n}{T_s}\right) \\ &= \sum_{k=-l}^{l} R_{preADC}(nT_s - kT_s).\mathrm{sinc}\left(k - \frac{\Delta P_n}{T_s}\right) \end{aligned} \tag{2.11}$$

Where $R(nT_s)$ is output signal of ADC and l is the sampling point index. Because of the SCO, even if the initial sampling point is optimized, the following sampling points will slowly shift with time. This shift in time-domain becomes a phase rotation in frequency-domain. Figure 2.18 shows the time-domain oversampled received data and the frequency-domain linear phase shift caused by SCO.

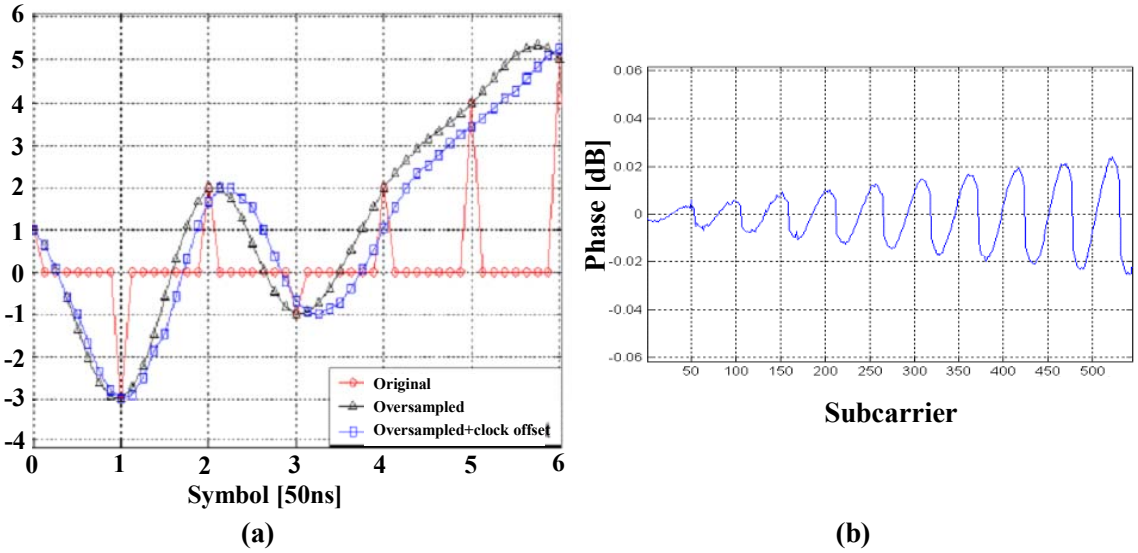


Figure 2.18 (a) the time-domain sampling offset

(b) the frequency-domain linear phase shift

2.3.4 AWGN Model

The AWGN channel model is established by the random generator in Matlab. The output random signal is normally distributed with zero mean and variance equal to 1. The complex AWGN noise can be modeled as

$$\boldsymbol{w(t) = [randn(1, l) + j \cdot randn(1, l)] \cdot \sqrt{\frac{10^{\frac{P_S - SNR}{20}}}{2}}} \tag{2.12}$$

Where P_S is the data signal power, *SNR* is the signal to noise power ratio, and $\boldsymbol{l}$ is the data signal length.

Chapter 3.
A Frequency Synchronizer Design for OFDM WLAN Systems

As for the complement to periodic and non-constant-power preamble in IEEE 802.11a, low-complexity frequency estimators are of interest. Such estimator is relied on the phase information of auto correlations. In this chapter, we chose fewer samples for auto correlation based on the average power of preamble before FFT process. We also derive the performance and show how the correlation samples should be properly chosen with acceptable SNR loss.

3.1 Carrier Frequency Offset Synchronization

For packet-based OFDM wireless systems, the burst synchronization is needed. We generally used data-aided methods which inserted the special synchronization information to estimate the CFO. The data-aided CFO estimation can achieve the system requirement in a very short time period.

3.1.1 The algorithms of CFO estimation and compensation

In the 1994, Paul H. Moose [14] proposed a method to estimate frequency offset from the demodulated data signals in the receiver. This method involves repetition of a data symbol and compares the phases of each of the carriers between the successive symbols. Since the modulation phase values are not changed, the phase shift of each of the carriers between successive repeated symbols is due to the frequency offset.

If an OFDM transmission symbol is repeated, one receives, in the absence of noise, the

received training symbol r_n that interfered by CFO $\in$ is shown in (3.11), and –K…K are subcarriers' indexes.

$$r_n = \frac{1}{N}\sum_{k=-K}^{K} X_k H_k e^{2\pi j(k+\in)n/N}; n = 0,1,...,2N-1 \tag{3.11}$$

The *k*th elements of the N point DFT of the first and second N points of (3.11) are shown in (3.12) and (3.13) respectively.

$$R_{1k} = \sum_{n=0}^{N-1} r_n e^{-2\pi jnk/N}; k = 0,1,2,..., N-1 \tag{3.12}$$

$$R_{2k} = \sum_{n=N}^{2N-1} r_n e^{-2\pi jnk/N} = \sum_{n=0}^{N-1} r_{n+N} e^{-2\pi jnk/N}; k = 0,1,... N-1 \tag{3.13}$$

From (3.11), we know that $r_{n+N} = r_n e^{2\pi j\in}$ and the R_{2k} becomes (3.14)

$$R_{2k} = \sum_{n=0}^{N-1} r_n e^{2\pi j\in} e^{-2\pi jnk/N} = e^{2\pi j\in} \cdot R_{1k} \tag{3.14}$$

Including the AWGN as below,

$$\begin{aligned} Y_{1k} &= R_{1k} + W_{1k} \\ Y_{2k} &= R_{1k} e^{2\pi j\in} + W_{2k}; k = 0,1,..., N-1 \end{aligned} \tag{3.15}$$

Both the ICI and the signal of the first and second observations are altered in exactly the same way, by a phase shift proportional to frequency offset. Therefore, the offset $\in$ will be estimated using observations (3.15) is shown in (3.16).

$$\hat{\in} = (1/2\pi)\tan^{-1}\left\{\left(\sum_{k=-K}^{K} \mathrm{Im}[Y_{2k}Y_{1k}^*]\right)\Big/\left(\sum_{k=-K}^{K} \mathrm{Re}[Y_{2k}Y_{1k}^*]\right)\right\} \tag{3.16}$$

This algorithm, however, can only correctly distinguish the phase rotation in the range [-π, π], the estimation limitation is shown in equation (3.17). In (3.17) and (3.18), the NT_s means the time interval between the two repeat symbols. Minimizing the interval time to the OFDM symbol time can make the maximum CFO estimation range to be half of the subchannel bandwidth. According to the (3.18), the method to get a larger CFO estimation range is to shorten the training symbol time. The idea is also suggested in the [14].

$$|2\pi \in| = |2\pi NT_s f_\Delta| \le \pi \tag{3.17}$$

$$|f_{\Delta}| \leq \frac{1}{2NT_s} \tag{3.18}$$

After finishing the acquisition of CFO, we counteract the frequency offset that we estimated to compensate the following complex data signal as equation (3.19).

$$\hat{r}_k = r_k \cdot \exp(-j2\pi \hat{\in} kT); k = 0,1,2,... \tag{3.19}$$

Where r_k are the received complex signals that influenced by CFO $\in$ and k are the indexes of data signal.

3.1.2 The structure of CFO estimation and compensation

The training symbols are provided for burst synchronization in the packet-based transmission system. As previous discussion in section 3.2.1, the repeated OFDM symbols can be used to perform the CFO synchronization. One reason we using time domain estimation and compensation is that the frame detector can get a less distortion training pattern to judge the frame boundary more accurately. The other one is that the compensated training data can be used to estimate the channel response directly by the channel equalizer after FFT process.

In order to cover a larger CFO estimation range, we need two stages CFO estimation as Figure 3.1 by means of short and long symbols in the preamble. According to the properties of short and long training symbols, coarse CFO estimation gets a rougher estimate under a wider frequency offset range while fine CFO estimation gets narrower but more accurate results. Taking advantages of both estimation results in a more precise estimate for CFO under a wider CFO range. Basing on the IEEE 802.11a specification, the maximum tolerance center frequency offset of the transmitter and the receiver shall be within ±40ppm of 5.3 GHz RF frequency; that is equal to ±212 KHz; and further, due to the 0.8μs short and 3.2μs long training preamble provided for coarse and fine CFO estimation, the enduring estimation range

are about -118ppm ~ 118ppm (-625KHz ~ 625KHz) and -30ppm ~ 30ppm (-156.25KHz ~ 156.25KHz) respectively.

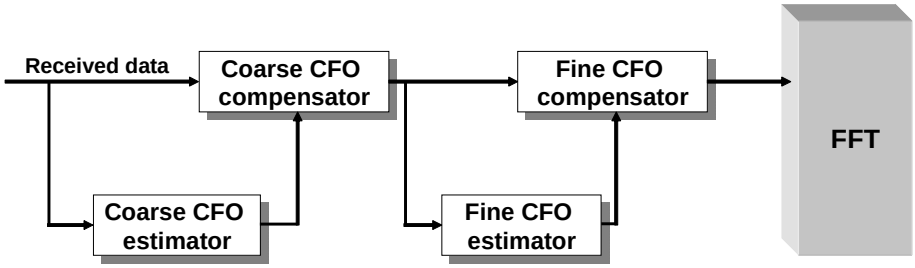


Figure 3.1 The structure of two stages CFO synchronization

In the acquisition scheme, coarse and fine CFO estimations and compensations are performed by using the same algorithms. The coarse CFO estimation is available from equation (3.20).

$$\hat{\epsilon}_{coarse} = \frac{1}{2\pi T_s} \tan^{-1}\left[\frac{\mathrm{Im}\sum_{n=0}^{N_s-1} r_n \cdot r_{n+N_s}^*}{\mathrm{Re}\sum_{n=0}^{N_s-1} r_n \cdot r_{n+N_s}^*}\right] \tag{3.20}$$

Where T_s is short training symbol period; that is 0.8μs; and N_s is the number of samples in a short training symbol. Before fine CFO estimation, the long training symbols shall be compensated with the frequency estimated as equation (3.21).

$$\hat{r}_{k,long} = r_{k,long} \cdot \exp(-j2\pi k\, \hat{\epsilon}_{coarse}\, T); k = 0,1,2,\ldots 127 \tag{3.21}$$

Where k is index of long training symbol, and T is sample period that equal to 1/20MHz. Therefore the fine CFO estimation is represented as equation (3.22).

$$\hat{\epsilon}_{fine} = \frac{1}{2\pi T_l} \tan^{-1}\left[\frac{\mathrm{Im}\sum_{n=0}^{N_L-1} r_n \cdot r_{n+N_L}^*}{\mathrm{Re}\sum_{n=0}^{N_L-1} r_n \cdot r_{n+N_L}^*}\right] \tag{3.22}$$

Where T_l is long training symbol period; that is 3.2μs; and N_L is the number of samples in a long training symbol.

After finishing the acquisition of CFO, both coarse and fine estimation is available. The

following complex data signals including of long symbols, header and payload shall be compensated by estimated coarse and fine CFO as equation (3.23) and r_k is the complex signal beginning from long symbols.

$$\hat{r}_k = r_k \cdot \exp[-j2\pi k(\hat{\epsilon}_{coarse} + \hat{\epsilon}_{fine})T]; k = 0,1,2,... \quad (3.23)$$

3.2 The Proposed CFO Estimation Scheme

In a real system, several synchronization issues must be taken care including frame detection, multipath cancellation and other channel effects. The only purpose that we considered in low-complexity method is trying to reduce the number of correlations as far as we keep the performance of CFO estimation. We analyze the average-power distribution of preamble in IEEE 802.11a, and decided which points of preamble we used for complex multiplier to estimate the CFO.

3.2.1 Property of Preamble

According to the specification of IEEE 802.11a, besides the format of preamble, the signals which carried by the preamble are non-constant power. In other words, the power distribution of each sample in the short and long training symbols is different; it also affects the accuracy of the following frequency synchronization. Therefore, we analyze the power distribution of the time-domain preamble under both AWGN and multipath fading channel as Figure 3.2. Because AGC and packet detection need to take several short training symbols before coarse CFO estimation, we use four short symbols and two long symbols for power analysis. We separate the index of samples of short and long training symbols into two parts; one is even index of samples, the other is odd one; and sum their power respectively. From Figure 3.2(a) and (b), the *z*-axis represents the probability that the odd-index power larger even-index one, and we can obviously see that the results from short and long training

symbols are opposite and they also be influenced graver by multipath effect.

3.2.2 Samples Power Detection

For low complexity method, we can reduce the half samples of short and long training symbols for correlations according to the information of even or odd index from power distribution of samples. In the realistic system, we need the packet detection before the CFO acquisition. Nevertheless, even if we have packet detection, we can not ensure how accurate is; furthermore, because of the multipath effect, the power distribution of samples in the short and long training symbols could be changed probably in the same time. For these reasons, we take one more short-symbol to detect the next coming short symbols which samples have stronger power. Due to one short symbol includes 16 samples, and we sum each sample power of even and odd index respectively. And then we can determine that even or odd index samples have stronger power for coarse CFO estimation. Certainly, the opposite result of the detection can be used for following fine CFO estimation. Therefore, the algorithms of the coarse and fine CFO estimation can be modified as equation (3.24) and (3.25) respectively; and λ is decided by sample power detector. Consider about limited short training symbols and the performance trade off, we used twice correlations that total three short symbols needed. Figure 3.3 shows the synchronization flow with the sample power detection and the interactive between the packet detection and CFO compensation before FFT demodulation.

$$\hat{\epsilon}_{coarse} = \frac{1}{2\pi T_s}\tan^{-1}\left[\frac{\mathrm{Im}\sum_{n=0}^{N_s/2-1} r_{2n+\lambda}\cdot r^{*}_{2n+\lambda+N_s}}{\mathrm{Re}\sum_{n=0}^{N_s/2-1} r_{2n+\lambda}\cdot r^{*}_{2n+\lambda+N_s}}\right];\lambda = 0(even),1(odd) \tag{3.24}$$

$$\hat{\epsilon}_{fine} = \frac{1}{2\pi T_l}\tan^{-1}\left[\frac{\mathrm{Im}\sum_{n=0}^{N_L/2-1} r_{2n+\lambda}\cdot r^{*}_{2n+\lambda+N_L}}{\mathrm{Re}\sum_{n=0}^{N_L/2-1} r_{2n+\lambda}\cdot r^{*}_{2n+\lambda+N_L}}\right];\lambda = 0(even),1(odd) \tag{3.25}$$

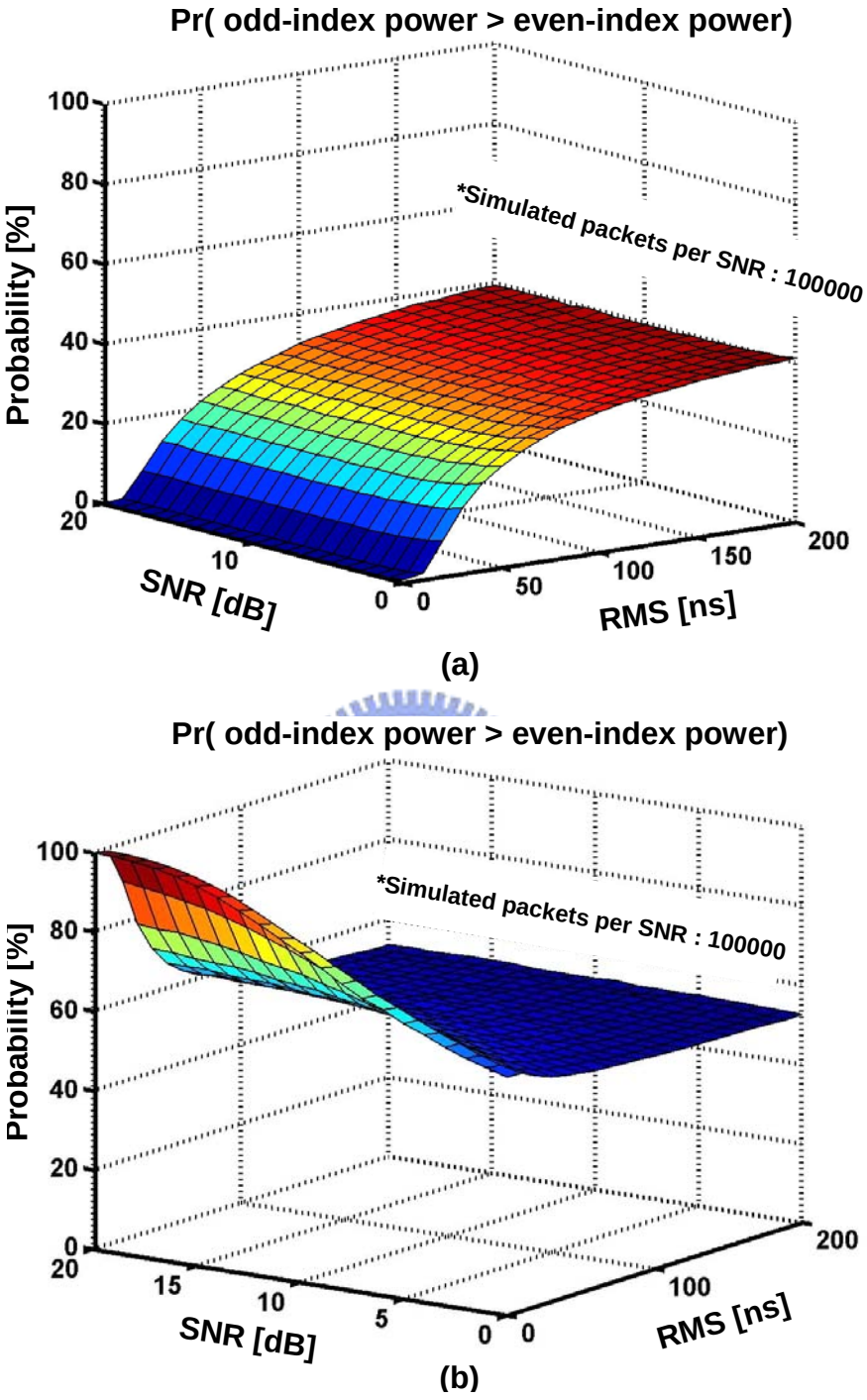


Figure 3.2 Power distribution of (a) Short training symbols

(b) Long training symbols

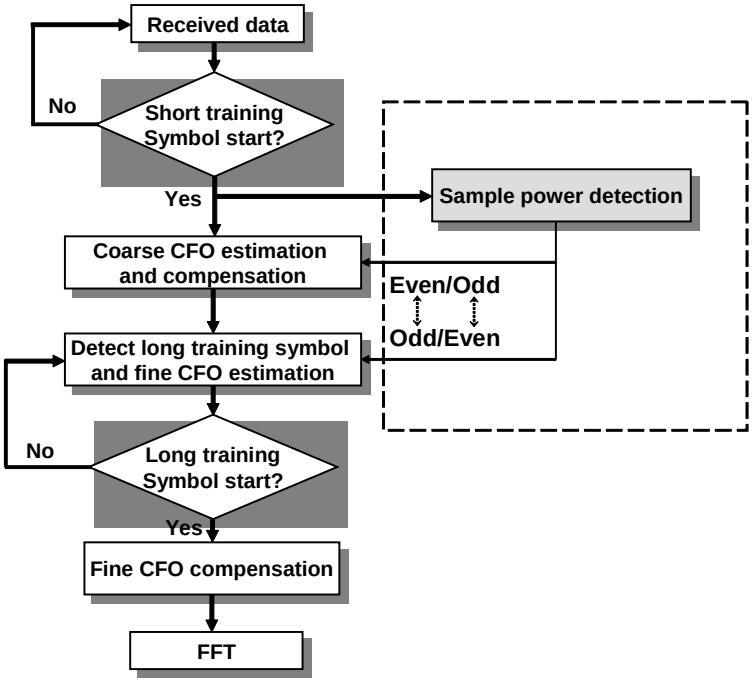


Figure 3.3 The synchronization flowchart with sample power detection

Chapter 4.
A High Speed and Low Complexity Frequency Synchronizer for OFDM-based UWB System

For general OFDM-based wireless access systems, we proposed a frequency synchronizer in chapter 3. Based on this design, the modifications can be made when dealing with different applications with particular requirements and specifications. In this chapter, a high-speed and low complexity frequency synchronizer is proposed for 528MHz OFDM-based UWB system.

4.1 Motivation

To speed up the implementation and power-reduction of 528MHz UWB frequency synchronizer, a novel low-power scheme combining data-partition-based, power-aware CFO estimation and approximate phasor compensation is proposed. It can reduce redundant computation of synchronization algorithm according to performance requirement. Following the algorithm improvement, the needed memory and clock speed of frequency synchronizer can be both decreased. In the further, we can reduce more power consumption in the better channel condition by power-aware concept. Simulation results show the power elimination efficiency is 69.4 ~ 75.6% and the paid performance loss can be limited to 0.04 ~ 0.6dB for typical 8% packet-error-rate (PER) for UWB.

4.2 Effect of Carrier Frequency Offset

In UWB system, maximum ±20ppm CFO is expected to exist in both transmitter and

receiver. So the required CFO estimation range must be ±40ppm (TX+RX) in frequency synchronizer. Besides, in order to enhance system performance, an accurate CFO estimation is generally requested in frequency synchronizer. However as system migrates from WLAN to UWB, the performance degradation caused by CFO becomes different. According to [14], the average power of frequency-domain signal without inter-carrier interference (ICI) can be derived as equation (4.1).

$$E\left[\left|Y_K\right|^2\right] = \left|X\right|^2\left|H\right|^2\left\{[\sin \pi \in]/[N \sin(\pi \in / N)]\right\}^2 \quad (4.1)$$

Where Y_K is the received signal, $|X|^2$ is the average transmitted signal power, $|H|^2$ is the average channel response power, $\in$ is the relative CFO of the channel (the ratio of actual CFO to the subcarrier spacing), and N is the point number of the DFT used for OFDM. In the (4.1), it can be found that the signal power is degraded by relative CFO $\in$. The CFO also causes ICI which is added to the received signal. According to [14], the average power of ICI can be derived as equation (4.2).

$$E\left[\left|I_K\right|^2\right] = \left|X\right|^2\left|H\right|^2\left\{\sin \pi \in\right\}^2 \sum_{\substack{p=-K-k \\ p\neq 0}}^{K-k} 1/\left\{N \sin[\pi(p+\in)/N]\right\}^2 \quad (4.2)$$

Where I_K is the ICI of the OFDM system, which using 2K+1 subcarriers. From (4.1) and (4.2), the signal-to-ICI ratio (SIR) of UWB and WLAN system can be calculated and then drawn in Figure 4.1. Since the specifications containing subcarrier spacing, RF frequency, and subcarrier number of UWB and WLAN system are different, the SIR of UWB is ~18dB higher than that of WLAN. The main cause is that the subcarrier spacing of UWB (4.125MHz) is 13.2 times wider than that of WLAN (312.5 KHz). Therefore the relative CFO $\in$ of UWB becomes lower. The lower relative CFO leads to less performance degradation.

To understand the required CFO-estimation accuracy from a system-level view, we simulated baseband PER with different CFO-estimation error. The simulated SNR loss for 8% PER caused by CFO-estimation error is shown in Figure 4.2.From Figure 4.2, it is found the

tolerant CFO-estimation error of UWB can be higher than of WLAN in the same SNR-loss constraint. For example, in 1dB SNR-loss constraint, the estimation error of UWB can be tolerated to 5ppm, but the estimation error of WLAN must be lower than 0.4ppm. Based on the performance comparison, the required accuracy and design complexity of CFO estimation in UWB can be less than that in WLAN. And a low-power scheme with algorithm reduction can be exploited in frequency synchronizer.

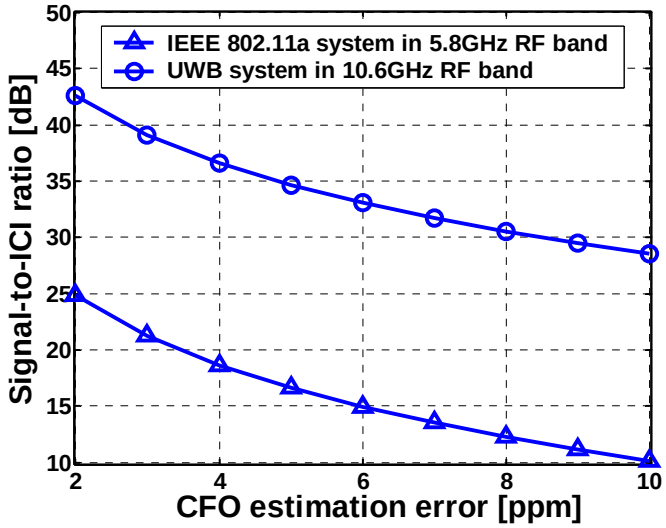
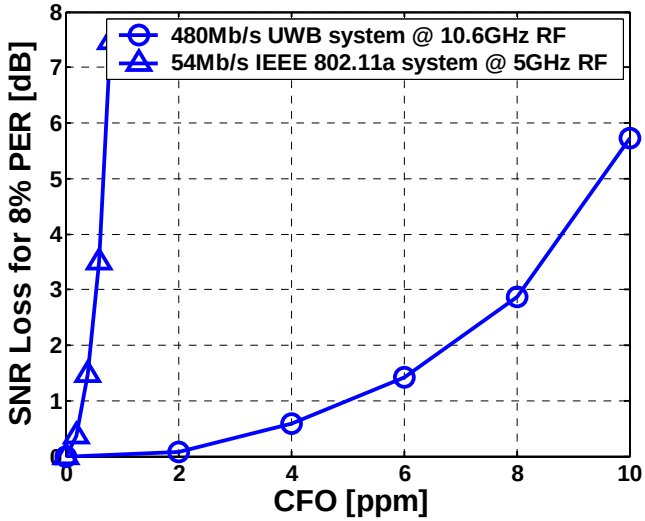


Figure 4.1 Signal-to-ICI ratio under CFO effect



∗Simulated packets per SNR: 1500, Data bytes per packet: 1024

Figure 4.2 SNR loss caused by CFO estimation error

4.3 The Proposed CFO Estimation and Compensation Scheme

The Figure 4.3 shows the block diagram of the proposed frequency synchronizer. In the beginning, the received preamble is sent to CFO estimator. Then the estimated result is sent to CFO compensator. And the late preamble and data signal are compensated and sent out. The compensated output signal can be used for timing synchronization and data demodulation. Besides, the proposed design is developed based on a data partition scheme in CFO estimator and an approximate phasor compensation scheme in CFO compensator to reduce design complexity. The proposed low-complexity algorithms will be described below.

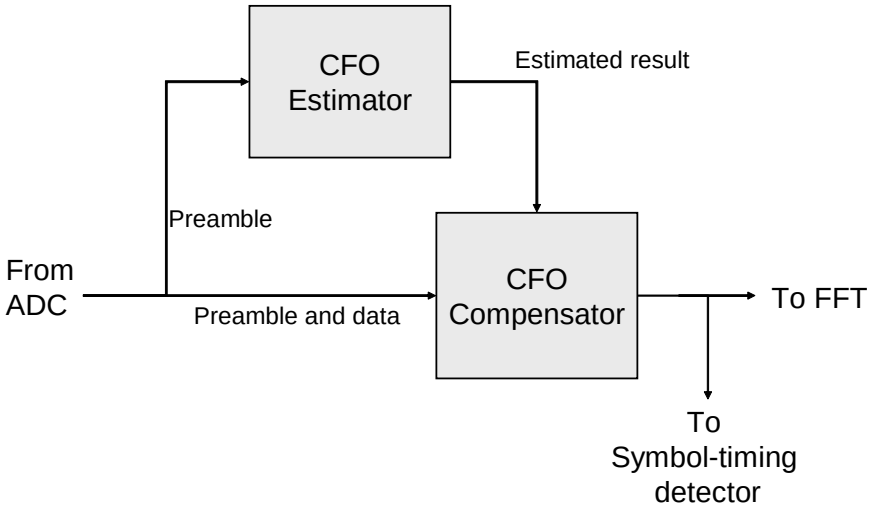


Figure 4.3 Block diagram of frequency synchronizer

4.3.1 Data-partition-based CFO Estimation

The conventional CFO estimator algorithm which uses full repeated symbols for auto-correlation is derived as equation (4.3).

$$\hat{\epsilon} = \frac{1}{2\pi NT} \tan^{-1}\left\{ \frac{\mathrm{Im}\sum_{n=0}^{N-1} r_n \cdot r_{n+N}^*}{\mathrm{Re}\sum_{n=0}^{N-1} r_n \cdot r_{n+N}^*} \right\} \quad (4.3)$$

Where $\hat{\epsilon}$ is the estimated CFO, r_n is the n-th received sample, and N is the total sample amount of one symbol. So $r_0 \sim r_{N-1}$ are the samples of one symbol duration. In UWB system, N is equal to 165 for repeated OFDM symbols [8]. And in CFO estimator, the first symbol with N samples needs to be stored in memory or delay-line [9]. To reduce the required memory access, a low-power algorithm based on data partition is proposed. It can be derived as equation (4.4).

$$\hat{\epsilon} = \frac{1}{6\pi NT} \left\{ \frac{\mathrm{Im}\sum_{n=0}^{\lfloor N/\lambda \rfloor - 1} r_{\lambda n} \cdot r_{\lambda n+3N}^*}{\mathrm{Re}\sum_{n=0}^{\lfloor N/\lambda \rfloor - 1} r_{\lambda n} \cdot r_{\lambda n+3N}^*} \right\} \quad (4.4)$$

Where the used samples of the first repetitive symbol duration are r_0, r_λ, $r_{2\lambda}$, $r_{3\lambda}$, …, and $r_{(\lfloor N/\lambda \rfloor - 1)\times\lambda}$,which are just $\lfloor N/\lambda \rfloor$ samples. In the proposed CFO estimation algorithm, the used sample amount is reduced from N to $\lfloor N/\lambda \rfloor$, which shown in Figure 4.4. Therefore, the design complexity of auto-correlation containing the memory size to store the used samples and the multiplication of used samples can be efficiently reduced.

Besides, the different correlation distance will affect the estimation accuracy and range. The signal power of image part will be increased because of long correlation distance, and then the estimation accuracy will be improved. However, the long correlation distance also decreased the estimation range. For the estimation accuracy and range trade off, the correlation distance is limited to $3NT$, that equal to 0.9375μs. So the estimation range can achieve ±0.5/0.9375μs = ±533KHz [14], that is ±50.3ppm of the highest RF frequency (10.6GHz) of UWB system. Thus the proposed algorithm can meet the requested ±40ppm CFO estimation range. Coincident, the $3NT$ correlation distance also can be applied in the

multi-band UWB system [4], for example, used time-frequency code 1 for band group 1, where the first OFDM symbol is transmitted on sub-band 1, the second OFDM symbol is transmitted on sub-band 2, the third OFDM symbol is transmitted on sub-band 3, the fourth OFDM symbol is transmitted on sub-band 1, and so on. This concept of the correlation distance also shown in Figure 4.4(b).

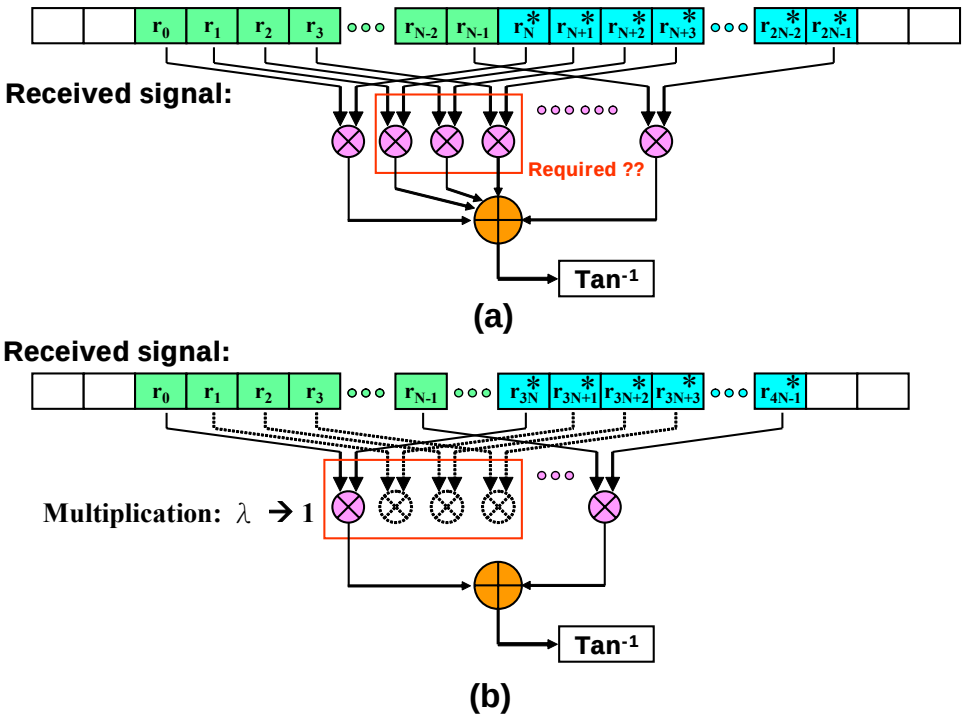


Figure 4.4 (a) The conventional CFO estimation

(b) The proposed data-partition-based CFO estimation

In order to reduce complexity and keep performance simultaneously, we have to find a good λ value. As Figure 4.5 shown, if high λ value is chosen, the complexity will be lower, but the CFO estimation error will be increased. In the section 4.3.3, we will choose a good λ value according to the performance loss.

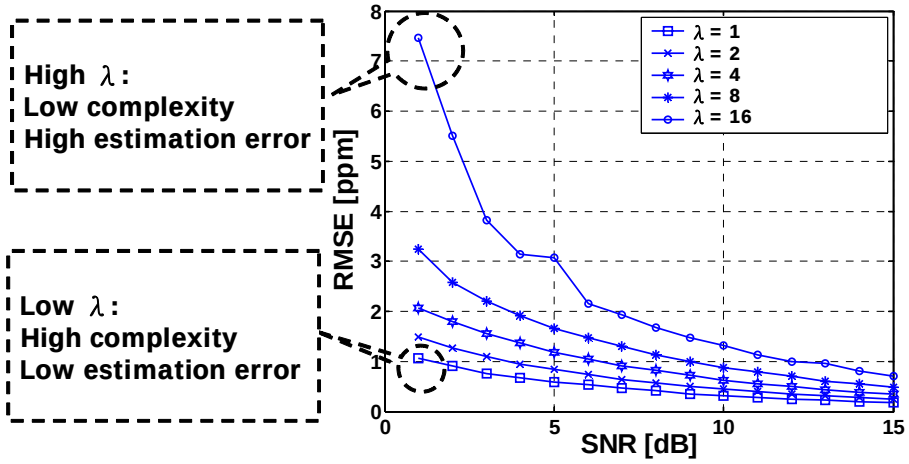


Figure 4.5 CFO estimation error with different complexity

4.3.2 Approximate phasor Compensation

In compensation part, the ideal method is to directly compensate the received signal with the phasor. It can be derived as equation (4.5).

$$\hat{r}_k = r_k \cdot \exp(-j2\pi \hat{\epsilon} kT) \tag{4.5}$$

Where r_k is the k-th received sample, $\hat{\epsilon}$ is the estimated CFO, T is the sample period, $\exp(-j2\pi \hat{\epsilon} kT)$ is the compensating value, and $\hat{r}_k$ is the compensated sample. In UWB system, the sample period (T=1/bandwidth=1/528MHz) is shorter than 1.9ns. So the compensating phasors for neighboring samples are approximate to each other. Hence the proposed approximate compensation scheme is derived as equation (4.6).

$$\hat{r}_k = r_k \cdot \exp(-j2\pi \hat{\epsilon} \left\lfloor \frac{k}{\lambda} \right\rfloor \lambda T) \tag{4.6}$$

Where $\exp(-j2\pi \hat{\epsilon} \lfloor k/\lambda \rfloor \lambda T)$ is the compensating phasor, and it remains the same for λ samples. For example, the phasors for $r_0 \sim r_{\lambda-1}$ are the same and equal to exp(j0) = 1 since $\lfloor k/\lambda \rfloor$ with k = 0 ~ λ-1 are all equal to 0; and the Figure 4.6 shows this example of the proposed algorithm where λ = 4. So each phasor can be used to compensate λ samples. And the phasor computations of (4.6) can be reduced to ~ 1/λ of that of (4.5). Figure 4.7 shows the examples which are the real parts of compensating phasor of (4.5) and (4.6) with λ = 4 and

$\hat{\epsilon}$= 424 KHz (40pm of 10.6GHz). And the x-axis is the receiving time (kT). As shown in Figure 4.7, the difference between the real parts of compensating phasor can be less than 2%. The difference is small so the approximate phasor compensation can be used to reduce the phasor computations.

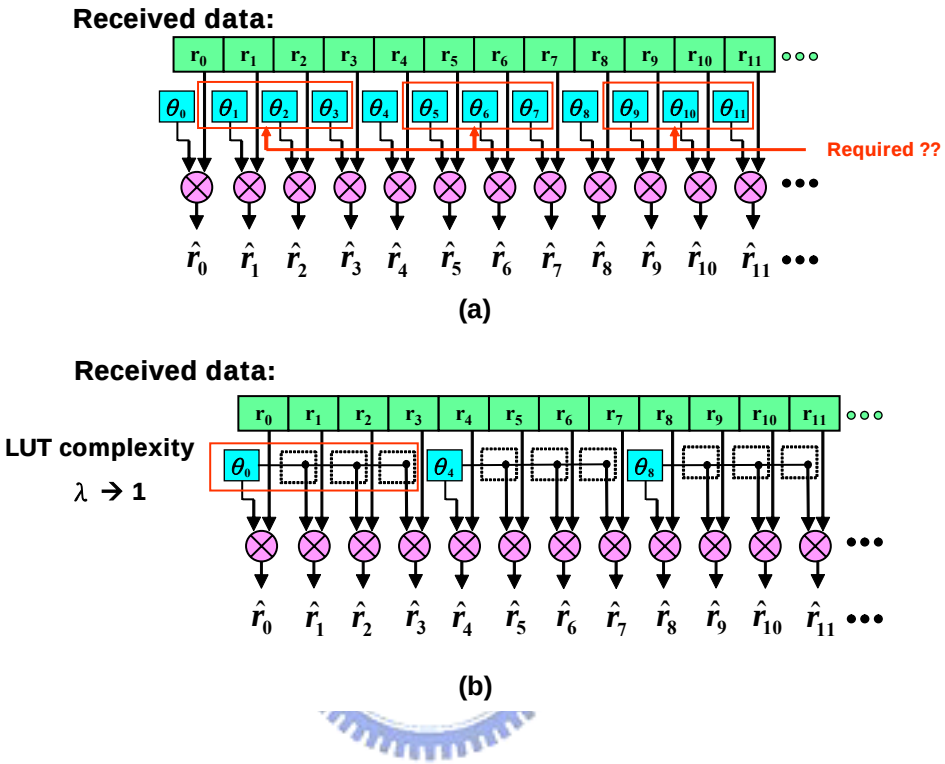


Figure 4.6 CFO compensation scheme (a) Conventional approach (b) Proposed approach

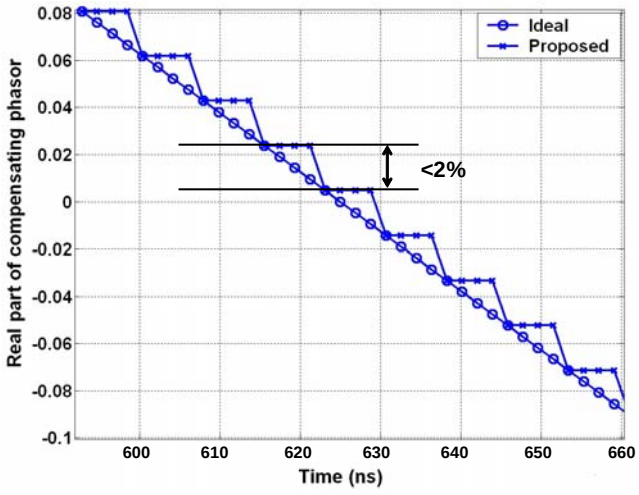


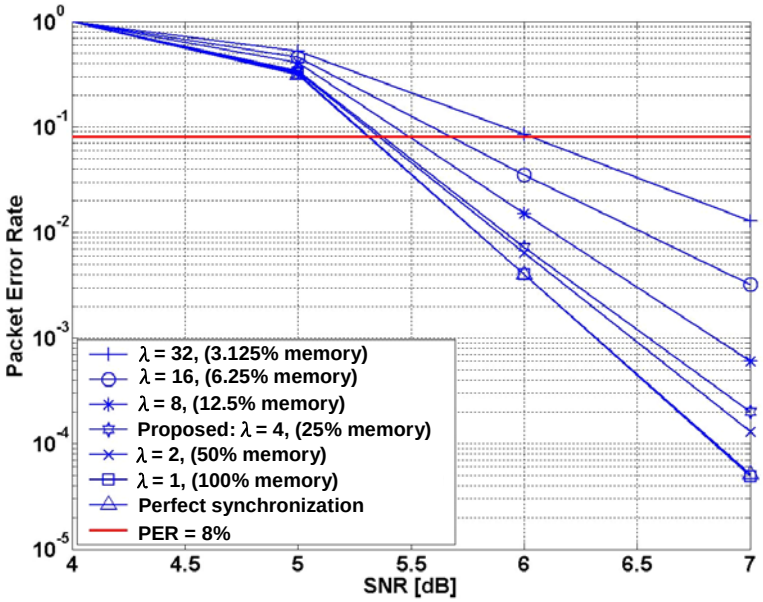
Figure 4.7 Real parts of compensating phasor

4.3.3 Reduced parameter search

In order to find a good λ for data-partition CFO estimation and approximate CFO compensation scheme, we simulated the PER curves with different design complexity.

- **PER Analysis with Different Design Complexity**

  Figure 4.8 shows the PER curves with different λ values which control required memory size and design complexity. The required SNR of different design complexity and its SNR loss are listed in Table 4.1. The SNR loss of the proposed design (λ=4) compared with perfect synchronization (CFO-estimation error = 0.0ppm) is only 0.07dB for 8% PER. PER of the proposed design is close to the design with λ = 2. That means the design complexity can be reduced from 50% to 25% with very little SNR loss. As λ is increased from 4 to 8, only 25%-12.5% = 12.5% design complexity are reduced further. But the SNR loss will be increased to 0.21dB equal to three times of the proposed design. Hence the design with λ = 4 is proposed to achieve low design complexity with an acceptable performance loss.



∗Data rate: 240Mb/s, Simulated packets per SNR: 1500,
Data bytes per packet: 1024, Channel CFO: 40ppm

Figure 4.8 PER with different design complexity

Table 4.1 The required SNR for 8% PER of the different design complexity

Design Parameter (λ)	Design SNR (dB)	SNR Loss compared with perfect synchronization (dB)
1	5.31	0
2	5.34	0.03
4	**5.38**	**0.07**
8	5.52	0.21
16	5.67	0.36
32	6.02	0.71

4.3.4 Power Aware CFO estimation

After introduction of the approximate CFO compensation, we focus on data-partition CFO estimation again. We'll try to reduce more complexity of data-partition estimation by power-aware concept. In the previous design, we used higher accuracy estimation which means higher complexity to estimate the CFO at every packet; we define it as fine estimation. However, in the better CFO environment, we can reduce the turn on probability of fine estimation at every packet. First, we used a lower accuracy estimation which means lower complexity to estimate the CFO at every packet; we define it as coarse estimation. The coarse estimation is used to decide whether the fine estimation turn on or not according to CFO environment. So we will not use any estimated result from coarse estimation. If coarse-estimation detect the worst CFO environment (fast variation), then fine-estimation will turn on; otherwise, we will use the previous result of fine estimation. For this reason, the complexity will be reduced greatly in the better CFO environment. Figure 4.9 shows the concept of power aware.

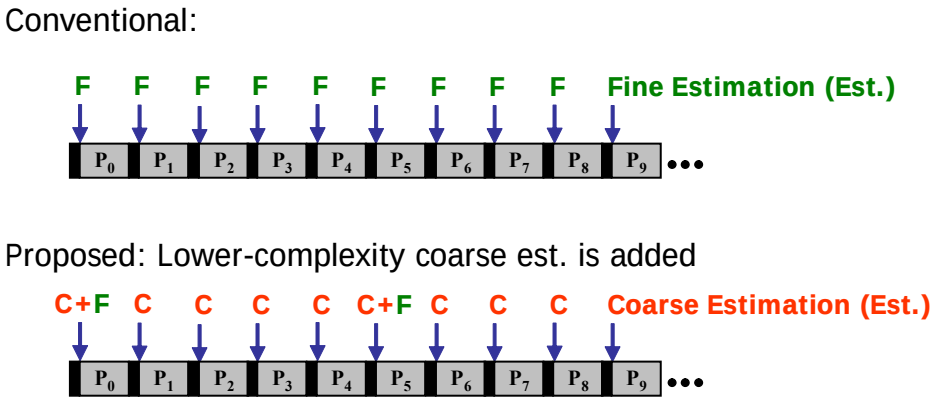


Figure 4.9 Power aware concept

In the further, we have to decide when the fine estimation turns on. We have a decision methodology as Figure 4.10. First, we will choose a threshold. If the difference of estimated results between coarse estimation and previous fine estimation is greater than threshold, then the fine estimation will be turned on. Therefore, the current estimated result is from new fine estimation. Otherwise, the fine estimation is turned off; the current estimated result is from previous fine estimation. We can notice that the turn on time of coarse and fine estimation is not overlap, and then the hardware can be shared. Besides, if the threshold is larger, the turn on probability of fine estimation is lower. Of course, the estimation complexity can be reduced.

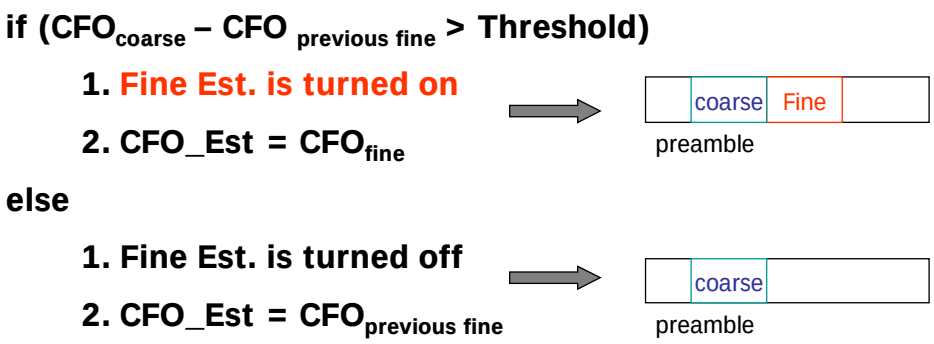


Figure 4.10 Decision methodology of fine estimation turn on

Figure 4.11 shows an example which used coarse estimation (λ =1/64 complexity) and fine estimation (λ =1/4 complexity). These three z-axes represent fine estimation turn on rate, CFO estimation error (RMSE) and estimation complexity respectively. X-axis and y-axis represent SNR and threshold respectively. From these figures, when the threshold is increased, the turn on probability of fine estimation will be decreased. Because of the lower turn on probability of fine estimation, the CFO estimation error will be increased, but the complexity can be reduced. Therefore, the estimation error and complexity are trade-off. For this reason, a good threshold for balance among performance, complexity and CFO environment is important. We will show the performance loss for different threshold and CFO environment in the next section.

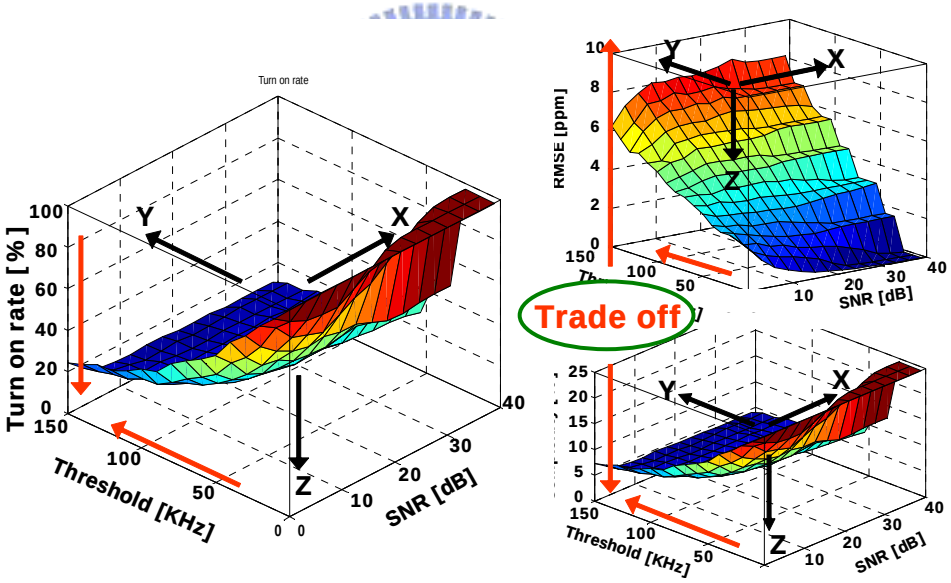


Figure 4.11 Relation among fine estimation turn on rate, estimation error and complexity

4.3.4 Threshold search

The decision of threshold is related to system performance and CFO environment. In the FV environment, in order to keep the performance, the turn on probability of the fine

estimation should be higher. That means the threshold should be decreased. In the SV environment, the threshold can be increased that makes the higher turn on probability of the fine estimation and lower complexity. We simulated the PER with different threshold in two CFO environments, one is SV which is shown in Figure 4.12, the other is FV which is shown in Figure 4.13. According to Table 4.2, the SNR loss of the threshold equal to 10ppm compared with the perfect synchronization is 0.6dB for 8% PER. However, when threshold is extended from 10ppm to 12ppm, the SNR loss is larger than 1dB. That means the threshold = 10ppm is chosen to achieve low design complexity with an acceptable performance loss in the SV environment.

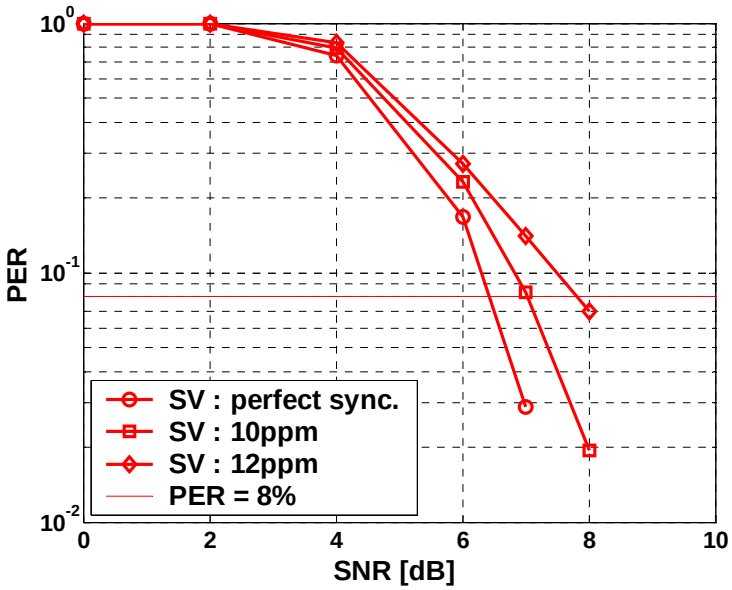


Figure 4.12 Threshold search in 110Mb/s SV environment

Table 4.2 Performance of different threshold in SV environment

Threshold	SNR for 8% PER (dB)	SNR loss (dB)
Perfect synchronization	6.4	0
10ppm	7.0	0.6
12ppm	7.8	1.4

From Table 4.3, the SNR loss of the threshold equal to 2ppm compared with the perfect synchronization is 0.1dB for 8% PER. However, when threshold is extended from 2ppm to 4ppm, the SNR loss is equal to 1dB. That means in the FV environment, the threshold = 2ppm is chosen to achieve acceptable performance loss. However, because of the lower threshold, the complexity of the CFO estimation in the FV environment could not be reduced as more as in the SV environment. Therefore, the concept of the power-aware is truly used in proposed design.

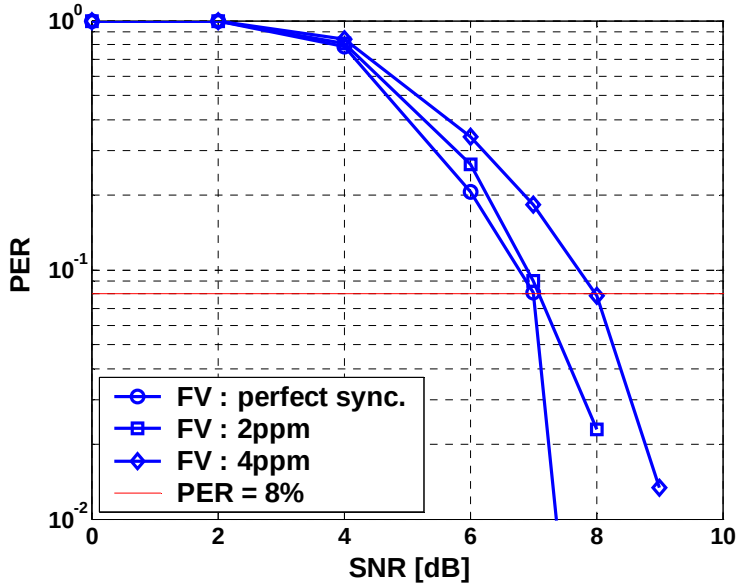


Figure 4.13 Threshold search in 110Mb/s FV environment

Table 4.3 Performance of different threshold in FV environment

Threshold	SNR for 8% PER (dB)	SNR loss (dB)
Perfect synchronization	7.0	0
2ppm	7.1	0.1
4ppm	8.0	1.0

Chapter 5.
Simulation Results and Performance Analysis

In order to verify the proposed design, the complete system platforms of the IEEE 802.11a and UWB proposal are established on Matlab. These platforms have been introduced in chapter2. The performance of the proposed design will be simulated and compared with the conventional approaches in the following analysis.

5.1 Performance Analysis of the Proposed Frequency Synchronizer for OFDM WLAN Systems

The proposed frequency synchronizer for OFDM-based wireless systems is simulated in the system platform compliant to the IEEE 802.11a PHY. The PER analysis will focus on the 10% PER, which is the requirement in IEEE 802.11a standard

5.1.1 CFO Estimation Accuracy Analysis

- **RMSE Analysis**

To analyze the CFO estimation accuracy of the proposed frequency synchronizer, the Root-Mean-Square-Error (RMSE) between the estimated CFO and the real CFO is measured, which has shown in Figure 5.1. Because AGC and packet detection need to take several short training symbols before frequency synchronization, we use three short symbols for coarse CFO estimation and one short symbol for sample-power detection. In the beginning, we simulated 4 cases for known sample-power-distribution without multipath effect; of course,

we don't need sample power detection. These 4 curves show me that even-samples in short symbol and odd-samples in long symbol (the square-mark curve) have more accuracy than opposite results (the triangle-up-mark curve) in SNR less than 5dB compared with 100% memory rate (the circle-mark curve). However, because of the multipath effect, the known sample power distribution will be interfered and estimation accuracy also decreased as the diamond-mark curve. In order to overcome this problem, the sample-power-detection could be applied to improve the estimation accuracy as the proposed curve. The reason that the accuracy of the proposed curve can't close to the square-mark curve is only one short symbol for power detection, the correct decision probability could not achieve 100%.

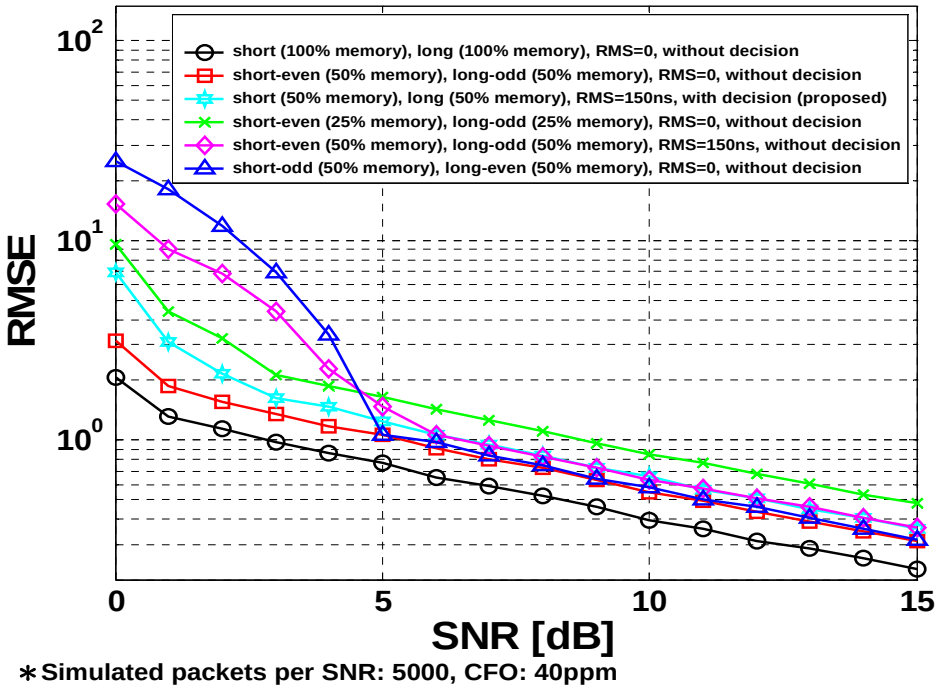


Figure 5.1 RMSE analysis of the proposed design

- **PER Analysis**

For performance analysis of the propose design, PER is simulated with the typical indoor wireless channel model that contains 50ns multipath RMS delay spread, 40ppm CFO and 40ppm SCO. The PER curves of 6Mb/s and 54Mb/s with perfect synchronization (CFO-estimation error = 0.0ppm), 100% memory approach and proposed design can be

shown in Figure 5.2. From Figure 5.2, the SNR loss of the proposed design (50% memory) compared with the 100% memory approach in the 6Mb/s and 54Mb/s are only 0.1dB and 0.13dB respectively for 10% PER. However, the memory size and computational complexity can be reduced from 100% to 50% with very low SNR loss.

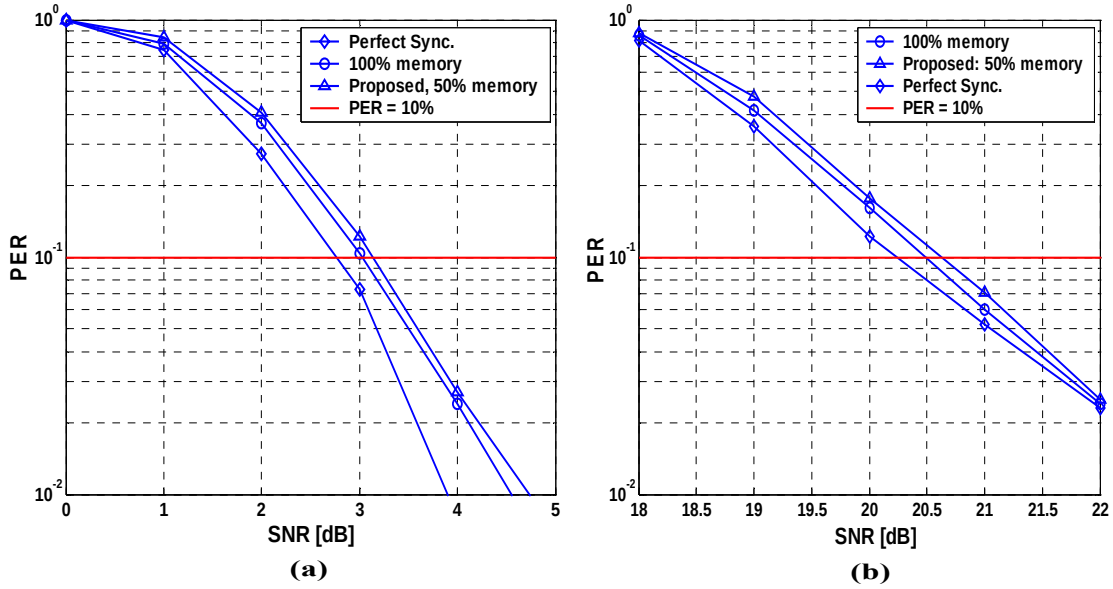


Figure 5.2 PER of the proposed design in (a) 6Mb/s (b) 54Mb/s data rates

5.1.2 System Performance

The PER curves of the OFDM-based WLAN system with 6Mb/s ~ 54Mb/s data rates are shown in Figure 5.3 and the design SNR for 10% PER are listed in Table 5.1. Compared with the perfect synchronization, the SNR loss of the proposed design is 0.15 ~ 0.38dB for 10% PER. Figure 5.4 shows the root-mean-square-error (RMSE) of the proposed CFO estimation. Within ±100ppm estimation range, the estimation RMSE can be ≤ 1ppm when SNR is ≥ 5dB. The simulation result shows the proposed design can achieve low SNR-loss and meet the estimation range requirement for OFDM WLAN system.

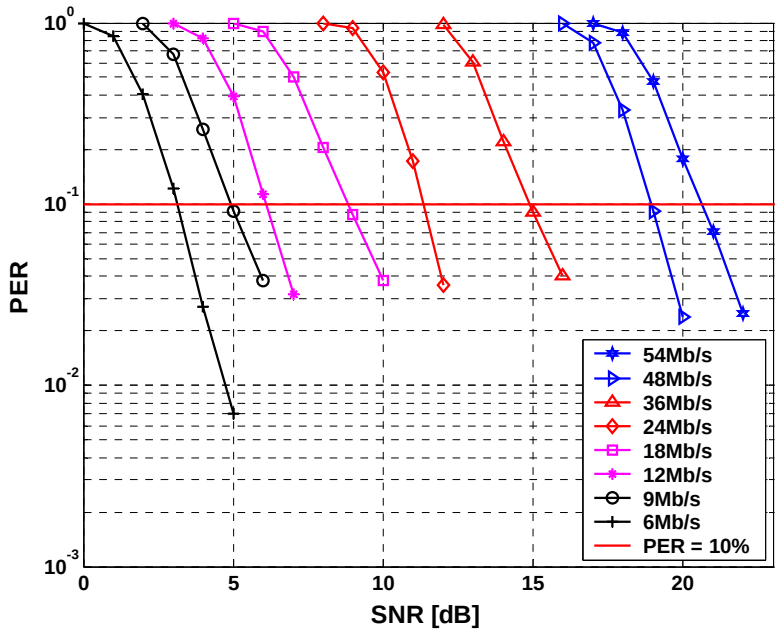


Figure 5.3 System PER performance

Table 5.1 Required SNR for 10% PER

Data Rate (Mbits/s)	Proposed design (dB)	Perfect Sync. (dB)	SNR Loss (dB)	IEEE 802.11a Requirement
6	3.13	2.76	0.37	9.7
9	4.92	4.7	0.22	10.7
12	6.10	5.88	0.22	12.7
18	8.85	8.48	0.37	14.7
24	11.35	11.10	0.25	17.7
36	14.88	14.73	0.15	21.7
48	18.94	18.62	0.32	25.7
54	20.62	20.24	0.38	26.7

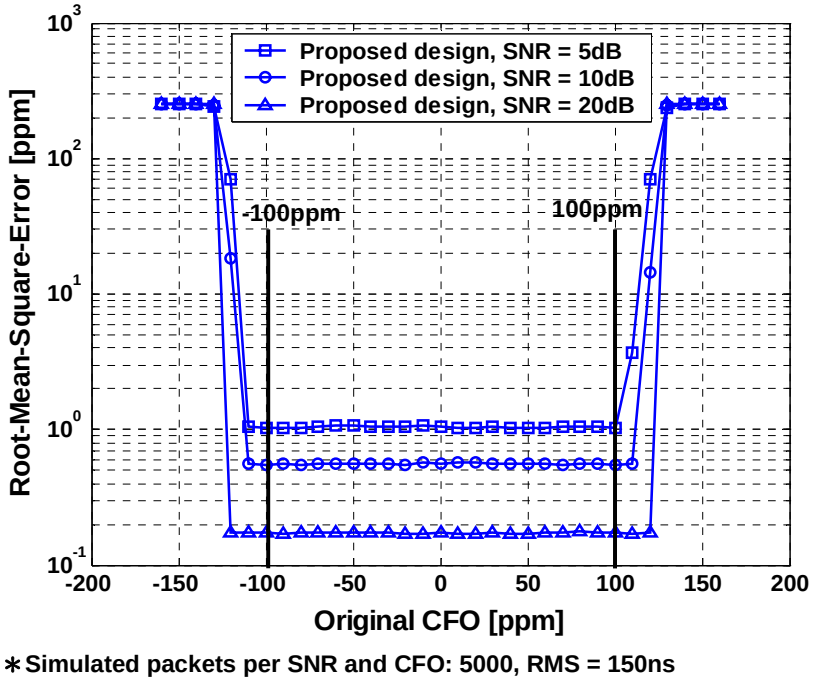


Figure 5.4 The CFO estimation performance in different CFO environment

5.2 Performance Analysis of the Proposed Frequency Synchronizer for UWB Systems

In this section, the simulated system PER with proposed (λ =4) data-partition-based, power-aware CFO estimation and approximate CFO compensation is analyzed in LDPC-COFDM and MB-OFDM UWB systems. Further, the simulated complexity and power reduction are also shown.

5.2.1 LDPC-COFDM UWB System Performance

PER curves of the LDPC-COFDM UWB system with 120Mb/s ~ 480Mb/s data rates are shown in Figure 5.5. Compared with the perfect synchronization, the SNR loss of the proposed design is 0.04 ~0.07dB for 8% PER. Figure 5.6 shows the root-mean-square-error (RMSE) of the proposed CFO estimation. With the estimation range of ±45ppm of 10.6GHz frequency, the estimation RMSE can be ≤ 1.3ppm when SNR is ≥ 3dB. The simulation results

show that the proposed design which has only 25% design complexity can achieve low SNR-loss and meet the estimation range requirement. The computational complexity of the proposed design is listed in Table 5.3. In Table 5.3, N is the sample amount of each repetitive symbol, and m is the auto-correlation times. Compared with the conventional design with λ = 1, the proposed design can save ~ 75% memory capacity and computational requirements.

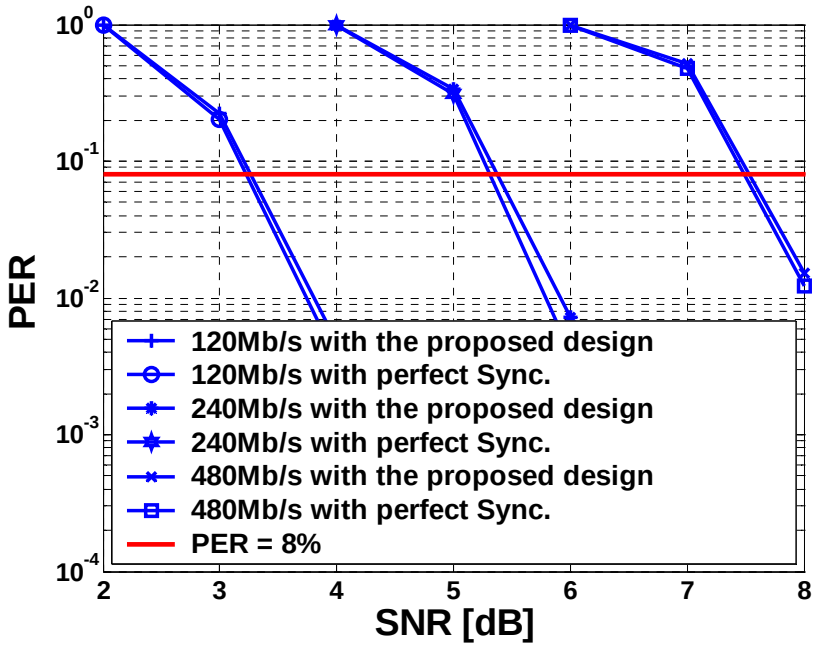


Figure 5.5 LDPC-COFDM UWB system PER

Table 5.2 Required SNR for 8% PER

Data Rate (Mb/s)	Perfect Sync. SNR (dB)	Proposed Design (dB)	System Required (dB)	SNR loss (dB)
120	3.22	3.27	7.6	0.05
240	5.31	5.38	16.0	0.07
480	7.49	7.53	21.1	0.04

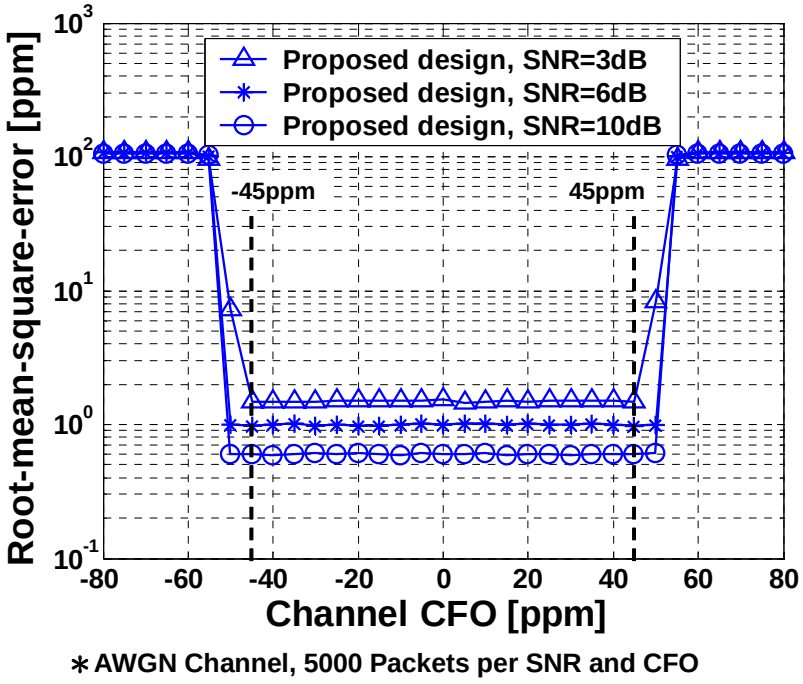


Figure 5.6 The CFO estimation performance in different CFO environment

Table 5.3 Design complexity

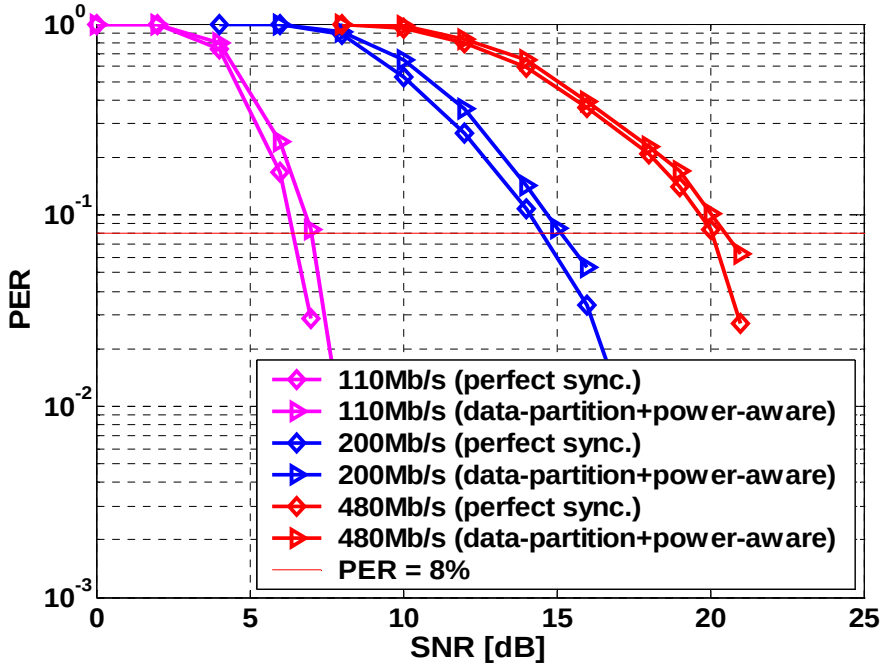
	Design with λ = 1	The proposed design
Memory size of CFO estimation	N	$\lfloor N/4 \rfloor$
Multiplications of CFO estimation	$N \times m$	$\lfloor N/4 \rfloor \times m$
Average phasor computations for each received sample	**1**	**1/4**

5.2.2 MB-OFDM UWB system performance

In this section, the simulated PER with data-partition-based, power-aware CFO estimation and approximate CFO compensation scheme is analyzed in MB-OFDM UWB system. In order to prove the power aware CFO estimation is still work, the CFO environment is slow-variant (SV) with phase noise which is mentioned in section 2.3.5. The threshold in SV environment is 10ppm (100 KHz) which is mentioned in section 4.3.5.

- **System Performance**

PER curves of the MB-OFDM UWB system with 110Mb/s ~ 480Mb/s data rates are shown in Figure 5.7. Compared with the perfect synchronization, the SNR loss of the proposed design is 0.5 ~0.6dB for 8% PER in worst CM channel of 110Mb/s, 200Mb/s and 480Mb/s, which shown in Table 5.4. The design SNR for 8% PER are 7dB, 15.1dB and 20.5dB and tally with the system required 7.1dB, 15.2dB and 21.1dB.



Simulation condition: CM channel, SV CFO, 40ppm SCO

Figure 5.7 MB-OFDM UWB system PER

Table 5.4 Required SNR for 8% PER

Data Rate (Mb/s)	CM channel	Perfect Sync. SNR (dB)	Proposed Design (dB)	System Required (dB)	SNR loss (dB)
110	CM4	6.4	7.0	7.1	0.6
200	CM4	14.5	15.1	15.2	0.6
480	CM2	20.0	20.5	21.1	0.5

- **PER vs. distance**

Figure 5.8 shows the PER performance for as a function of distance and information data rate in worst CM channel environment with SV-CFO condition. From Table 5.5, the distances of proposed design are 10.2 meter, 4.1 meter and 2.2 meter for 8% PER in worst CM channel of 110Mb/s, 200Mb/s and 480Mb/s. The design distances for 8% PER are still tally with the system required 10 meter, 4 meter and 2 meter.

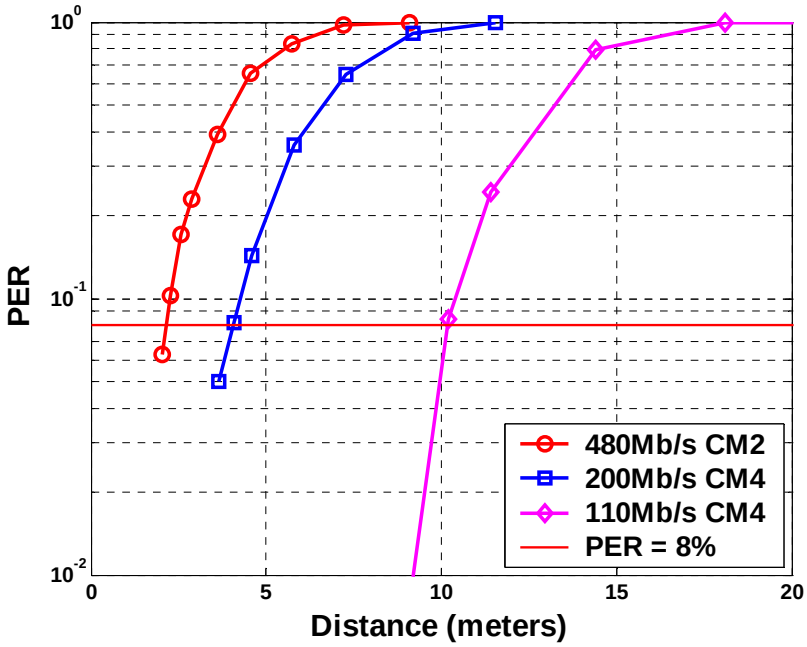


Figure 5.8 PER vs. distance

Table 5.5 Required distance for 8% PER

Data rates (Mb/s)	CM channel	Required (meter)	Proposed (meter)
110	CM4	10	10.2
200	CM4	4	4.1
480	CM2	2	2.2

5.2.3 Complexity and power reduction summary

Figure 5.9 shows the complexity reduction of CFO estimation and power reduction of proposed frequency synchronizer respectively. The complexity of proposed data-partition can be reduced to 25% of conventional estimation approach. If we combine the method of power-aware, the complexity can be reduced more 15% in low SNR, and 23% in high SNR. Besides, the power of proposed data-partition can be reduced to 40% of conventional frequency synchronizer. If we combine the method of power-aware, the power can be reduce more 10.3% in low SNR, and 16.5% in high SNR.

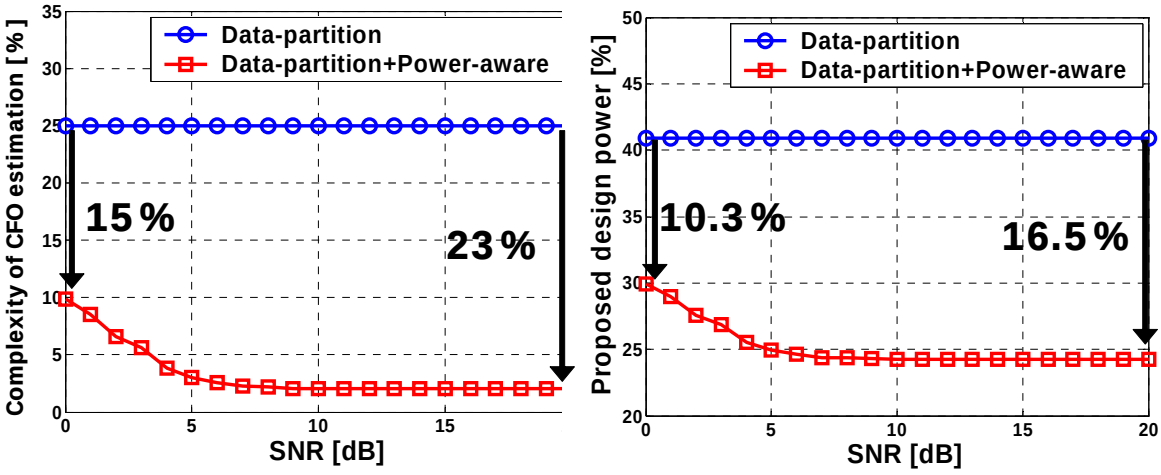


Figure 5.9 Complexity and power reduction

Chapter 6.
Hardware Implementation

In this chapter, we will introduce the platform based design flow. The architecture of the proposed design, hardware synthesis information and chip summary will be shown in the following sections.

6.1 Design Methodology

The trend of IC technology is towards to System-on-Chip (SoC). System-level simulation becomes very important in today's design flow. Our design methodology from system simulation to hardware implementation can be shown in Figure 6.1.

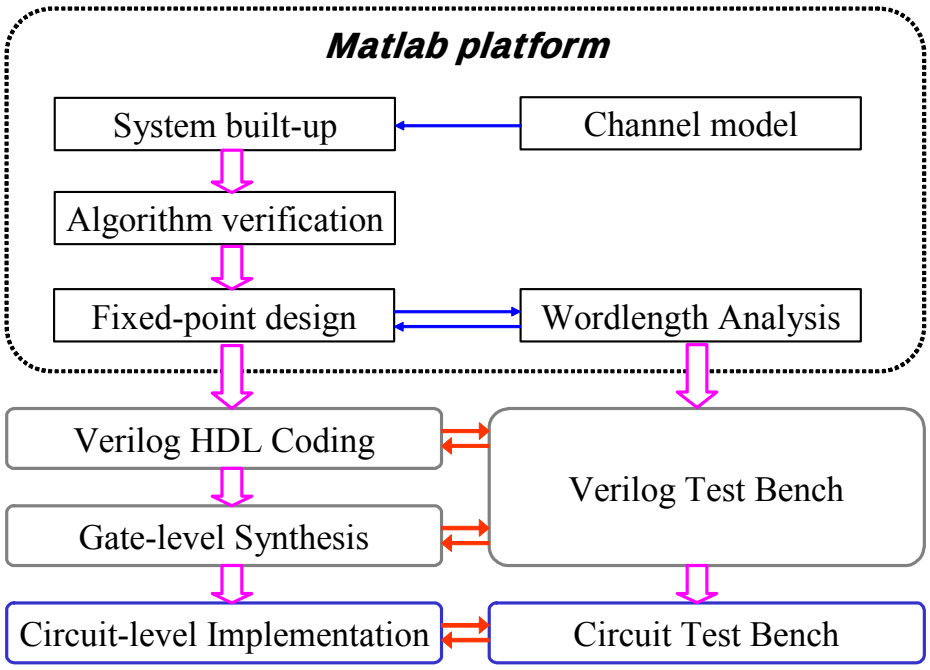


Figure 6.1 Platform-based design methodology

First, the system platform with channel modals should be established according to the system specification, which ensures the design in the practical condition. Algorithm and architecture developments of each function block should be verified in the system platform to ensure the whole system performance. Fixed-point simulation is applied before hardware implementation to make a trade-off between system performance and hardware cost. An example of the word-length distribution analysis can be shown in Figure 6.1.2. Based on the signal distribution analysis and the PER simulation, a reasonable word-length of each signal can be decided. In hardware implementation, the HDL modules are verified with the test benches dumped from the equivalent Matlab blocks to ensure the correctness.

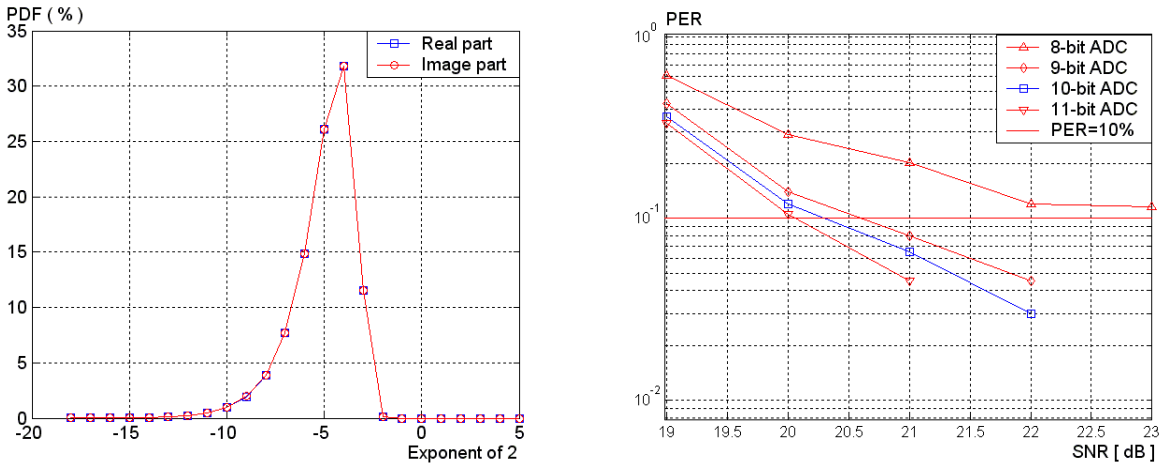


Figure 6.2 (a) Signal distribution analysis

(b) PER analysis of different word-length

6.2 The High-Speed and Low-Complexity Frequency Synchronizer for UWB Systems

6.2.1 Architecture of the Proposed Frequency Synchronizer

The architecture of the proposed frequency synchronizer is shown in Figure 6.3. It's developed based on the proposed algorithms with λ = 4. Since the needed computation rate of equation (4.4) and (4.6) can be reduced to 1/λ of equation (4.3) and (4.5) respectively, the proposed design can work on 528MHz/4 = 132MHz low clock frequency. Before CFO estimator, data-partition controller selects one input sample from four data paths in each clock cycle. To avoid burst noise or serious interference causing CFO estimation failure, twice CFO estimation is applied. And a memory is used to store $2\times\lfloor N/\lambda \rfloor$ = 82 samples. Then CFO is estimated after arc-tangent circuit. Since calculation rate of compensating phasor is reduced by equation (4.6), the proposed CFO compensator can work with single phase accumulator (ACC) and single phase-to-I/Q lookup table (LUT) at 132MHz clock frequency. The needed parallel part is only the complex multipliers to compensate the received FFT symbols of preamble and data signal. Based on data partition and approximate phasor compensation scheme, the proposed design can achieve 528MS/s throughput through a single architecture with parallel multipliers at 132MHz clock frequency.

The detail architecture of the proposed CFO estimator is shown in Figure 6.4. According to this figure, we can see that, the register-files are used instead of the memory because only 82 samples that are 656 bits (4-bits x 82-samples x 2-I/Q) needed to be stored. If we used memory to store the samples, compare with the register files, the required area and power consumption will be enlarged. Besides, consider about dynamic power consumption issue, we denied the shift registers to store the samples, even if its area is smaller than register-files.

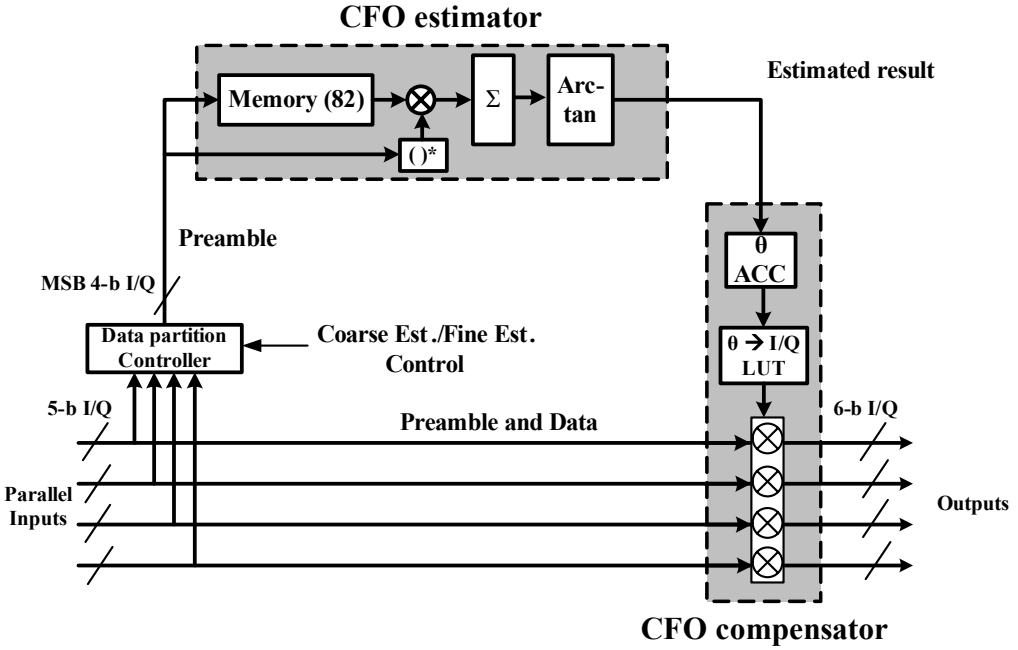


Figure 6.3 Architecture of proposed frequency synchronizer

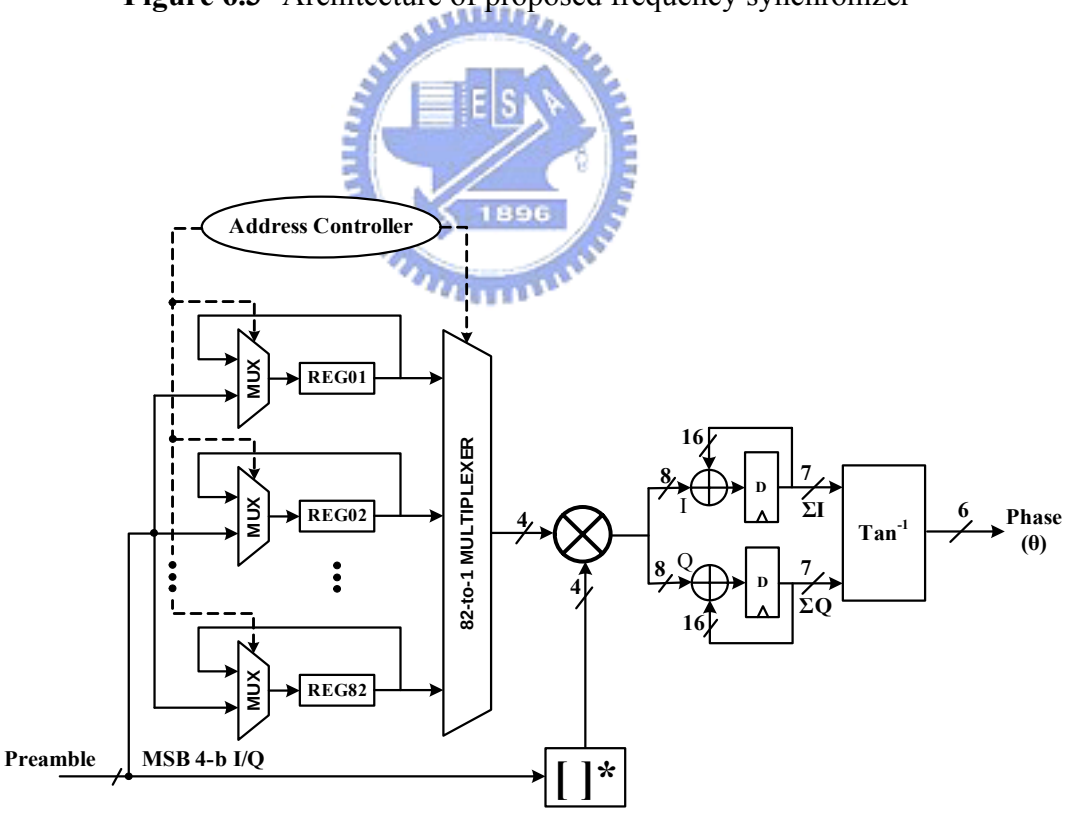


Figure 6.4 Detail architecture of proposed CFO estimator

The detail architecture of the proposed CFO compensator is shown in Figure 6.5(a) and its mapping diagram of sine and cosine is shown in Figure 6.5(b). The sine and cosine generator is designed using lookup table. Both the two function have the same property. The value in the first quadrant can be mapped onto other quadrants by simple sign transformation. Another property is that the values of sine or cosine can be transformed to each other. Generally, we can only build the first quadrant table of sine function and get the cosine values using the mapping function. In the system, however, the sine and cosine generator is used to generate complex values. The relative values have to be accessed at the same time for an angle. If the table only contains the sine values, there must be two accesses for a complex value. In our design, we build a table which contains the sine and cosine values, and we can produce a complex value using an access. The input range of the table is half of the previous. If the input angle is larger than the 45^0, exchange the output values of sine and cosine. Besides, the complexity of lookup table can be reduced because of the approximate CFO compensation scheme.

A conventional approach based on equation (4.3) and (4.5) is shown in Figure 6.6. It uses parallel-4 architecture to achieve 528MS/s throughput in 132MHz clock frequency. Compared with the parallel approach, the proposed design can reduce 75% memory size and complex multiplications. Implementation result will show the proposed design can efficiently reduce hardware cost and power consumption.

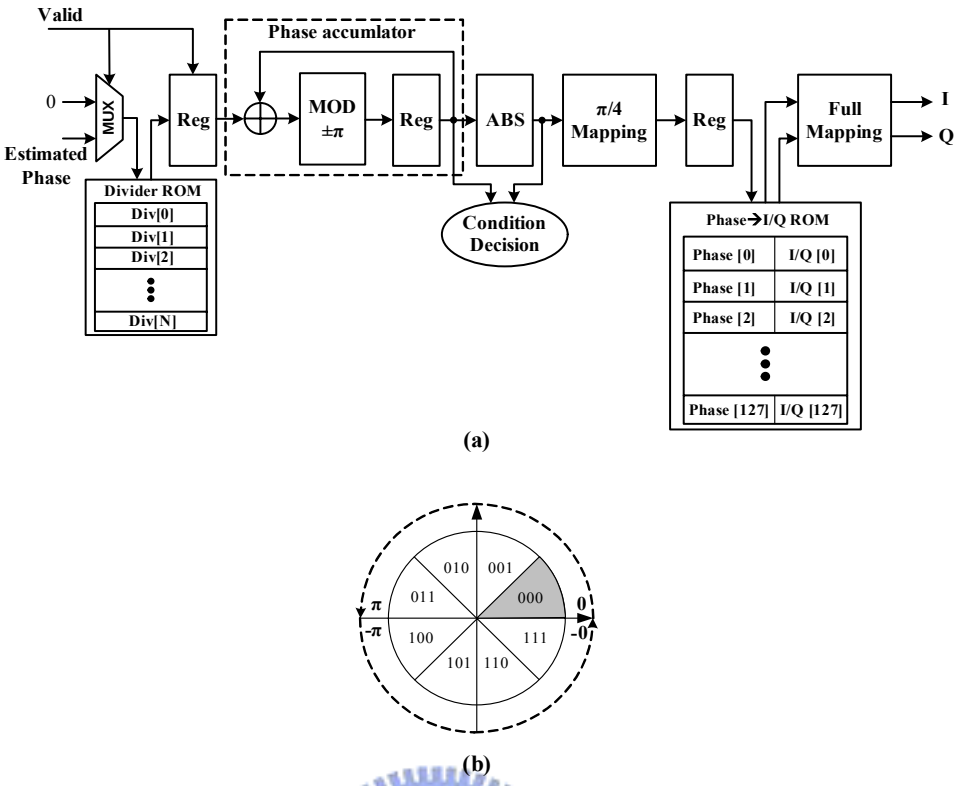


Figure 6.5 (a) detail architecture of proposed CFO compensator

(b) Mapping diagram of sine and cosine

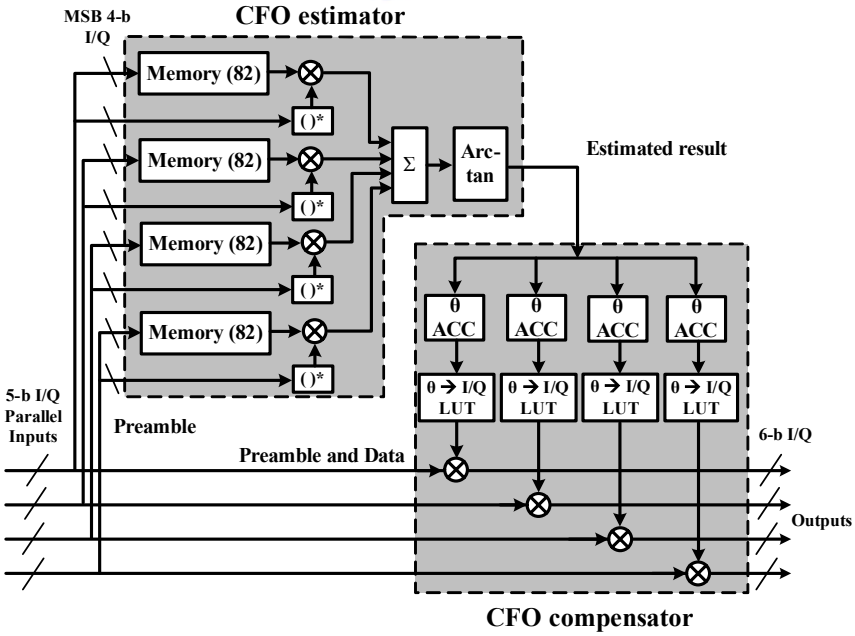


Figure 6.6 Conventional parallel architecture

6.2.2 Hardware Synthesis

The equivalent gate-count of the proposed design and the power consumption measured by post-layout simulation are listed in Table 6.1 and Table 6.2 respectively. Compared with the conventional parallel approach as shown in Figure 6.6, the proposed design combining with the data-partition-based, power-aware CFO estimation and approximate CFO compensation scheme can reduce 59% gate count and 69.4 ~ 75.6% power consumption.

Table 6.1 Equivalent gate-count of UWB frequency synchronizer

Gate-count	CFO estimator	CFO compensator	Total
Conventional parallel design	41K	20K	61K
Proposed design	11K	14K	25K
Reduction Percentage	49.2%	9.8%	59%

Table 6.2 Power of UWB frequency synchronizer (528MS/s)

Power (mW)	CFO estimator	CFO compensator	Total
Conventional parallel design	41.3	16.2	57.5
Proposed design	0.9 ~ 4.2	13.1	23.5
Reduction Percentage	64 ~ 70.2% (data-partition +power-aware)	5.4%	69.4 ~ 75.6%

6.3 UWB Baseband Processor

Figure 6.7 shows the micro-photo of the LDPC-COFDM UWB baseband processor integrating the proposed design in standard 0.18μm CMOS process. Its features also listed in

Table 6.3. Measured result shows 21.4mW power is consumed by the proposed 528MS/s frequency synchronizer.

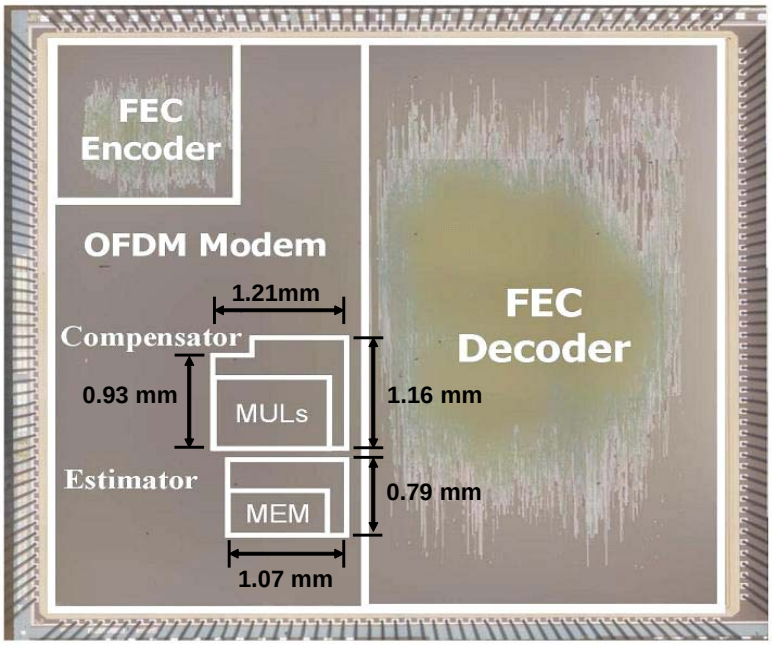


Figure 6.7 LDPC-COFDM UWB baseband processor

Table 6.3 LDPC-COFDM UWB PHY baseband feature

Technology	0.18μm CMOS 1P6M
Package	208 CQFP
Die area	42.25 mm^2 (6.5 mm x 6.5 mm)
Max. Working Frequency	264 MHz
Core Power at 480Mb/s (TX/RX)	523 mW/575 mW
Supply Voltage	1.8V Core, 3.3V I/O
Design Area	2.17 mm^2 (5.1%)
Design Power	21.4 mW (3.7%) @480Mb/s RX

Chapter 7.
Conclusion and Future Work

After design description, performance analysis and hardware comparison, a novel frequency synchronizer is proposed here to achieve high throughput, low power, and satisfy performance for OFDM-based WLAN and UWB system. Combining data-partition-based, power-aware CFO estimation and approximate CFO compensation scheme, our proposal can reduce 69.4% ~ 75.6% power consumption with achievable 0.04 ~ 0.6dB SNR loss for 10% PER of IEEE 802.11a WLAN system and 8% PER of LDPC-COFDM and MB-OFDM UWB systems; and further, the CFO-estimation range of ±100ppm in WLAN and of ±45ppm in UWB also can achieve the system requirement. The proposed design can achieve 528MSamples/s high throughput in both standard 0.13μm and 0.18μm CMOS processes.

For simulation of the power-aware CFO estimation, we established pseudo time-variant mean-CFO with phase noise model includes TIV (time-invariant), SV (slow-variant) and FV (fast-variant). However, the practical CFO model is also needed. In the future, we will survey more practical model to verify the design even if our pseudo model has considered about the worst CFO condition. Therefore, we are supposed to have more power reduction in general simulation case which mean-CFO is time-invariant.

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