國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

低功率預先比對之內容可定址記憶體電路和轉換後備緩衝器之設計

Low Power Pre-comparison Content Addressable Memory and Translation Lookaside Buffer Design

研 究 生：張維耿

指導教授：黃 威 教授

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研 究 生：張維耿　　Student：Wei-Keng Chang

指導教授：黃　威 教授　　Advisor：Prof. Wei Hwang

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摘　　要

使用預先比對電路和結合電源閘及雙電壓技巧用於內容可定址記憶體和轉換後備緩衝器實現在本篇論文中。預先比對電路允許一些已儲存的資料和一些欲比對的資料預先做比較的動作。透過這種機制來減少比對線電路的放電次數。應用此技巧於一個 32 行 x 32 位元的內容可定址記憶體，並利用 TSMC 0.13um CMOS 技術來加以實現。根據模擬結果，使用預先比對電路之內容可定址記憶體可以減少 22.8% 的動態功率之消耗，在使用 4 位元的預先比對電路情形之下。

電源閘及雙電壓技巧被用於預先比對電路之內容可定址記憶體和轉換後備緩衝器。一個 32 行 x 32 位元之內容可定址記憶體和 36 行 x 32 位元之靜態隨機儲取記憶體被結合成一個轉換後備緩衝器。利用 TSMC 100nm CMOS 技術來加以模擬。根據模擬結果，使用預先比對電路之內容可定址記憶體可以減少 31.1% 的漏電功率之消耗，而轉換後備緩衝器則可以省下 33.4%之漏電功率。

Low Power Pre-comparison CAM and TLB Design

Student：Wei-Keng Chang　　Advisor：Prof. Wei Hwang

Department of Electronics Engineering & Institute of Electronics
National Chiao-Tung University

ABSTRACT

Using pre-comparison circuit and combining power gating as well as dual vdd for Content-Addressable Memory (CAM) and Translation Lookaside Buffer (TLB) is presented in this thesis. The pre-comparison circuit allows some storing data and searching data for pre-comparison in advance. Through this mechanism, reduce the times of match line discharging. Applying the techniques to 32 words x 32 bits CAM is implemented in TSMC 0.13um CMOS technology. According to simulation results, the pre-comparison CAM achieves 22.8% dynamic power reduction for four pre-comparison bits.

The techniques of power gating and dual vdd are applied to pre-comparison CAM and TLB to reduce leakage power. A 32 words x 32 bits pre-comparison CAM and 32 words x 36 bits SRAM are combined for TLB. A TSMC 100nm CMOS technology is used to simulation here. According to simulation results, the pre-comparison CAM can save 31.1% leakage power and TLB can save 33.4% leakage power with those techniques.

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Table of Contents

List of Tables

List of Figures