振盪環測試應用於非同步序向電路

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摘　要

在此篇論文中，我們利用振盪環測試的原理來偵測序向電路上之定值障礙。而所謂的振盪環是指藉由奇數個反相邏輯閘所建構而成的封閉路徑。當給予適當之圖樣至電路的輸入端，振盪環將會振盪。而藉由輸入序列來尋找有效之狀態，我們使用狀態轉換表來建構振盪環及產生圖樣。再藉由觀察漢明距離為 1 之狀態組合，我們就可以產生狀態圖樣。而爲了證明這個方法，我們在幾個基準的大電路作了實驗。同樣地，我們已經發展了一套狀態設定程序來指定非同步電路中的狀態值，使得電路能更加可測試。

OR-Test for Asynchronous Sequential Circuits

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Abstract

In this thesis, we use the oscillation ring test methodology to test stuck-at faults for sequential circuits. Oscillation rings are the closed loops which are formed with odd inversion logic gates. Oscillation rings will oscillate when appropriate patterns are applied to inputs of the circuit. We use the state transition table to form oscillation rings and generate patterns by searching valid states through traversing input sequences. By observing state sets with hamming distance of 1, we generate state patterns. Experiment has been done on several large benchmark circuits to show this methodology. Also, we have developed a state assignment procedure to assign state for an asynchronous circuit to make the circuit more oscillation testable.