

Contents

Chinese abstract.....	I
English abstract.....	II
Contents.....	III
List of Figures.....	V
List of Tables.....	VII
Chapter 1 Introduction.....	1
1.1 Introduction.....	1
1.2 Characteristic of Tested Asynchronous Circuits.....	1
1.3 Outline of The Thesis.....	2
Chapter 2 Application of OR-Test Methodology to the Asynchronous Circuit.....	4
2.1 OR-Test Methodology.....	4
2.2 Basic Architecture of OR-Test.....	4
2.3 Fault Detection.....	5
2.4 Formation of Oscillation Rings.....	8
2.4.1 Relation of State Sets for Oscillation Rings.....	8
2.4.2 True Table of State Variable and Function Table of Feedback Cell.....	11
2.5 State Pattern.....	12
2.5.1 Type 1: Bypass State.....	12
2.5.2 Type 2: INV State.....	12
2.5.3 Type 3: Hold State.....	13

2.5.4 Type 4: Fail State.....	14
2.6 Condition of State Patterns.....	15
Chapter 3 Procedure to Generate OR-Test Test Patterns.....	17
3.1 Flow of OR-Test by State Transition Table.....	17
3.2 Algorithm of Input Sequence Finding.....	18
3.3 Algorithm of State Pattern.....	20
3.4 Fault Simulation.....	22
Chapter 4 Experimental Results on Benchmark Circuits.....	24
Chapter 5 State Assignment to Improve OR-Testability for Asynchronous Circuits.....	26
5.1 Assignment Flow.....	26
5.2 Example and Result Analysis.....	27
Chapter 6 Conclusion.....	32
Reference.....	33
Vita.....	35



List of Figures

Figure 2.1 Simple illustration of OR-Test.....	4
Figure 2.2 (a) Sketch map of asynchronous circuits.....	5
Figure 2.2 (b) Architecture of feedback cells.....	5
Figure 2.2 (c) Operation of control signals.....	5
Figure 2.3 A Fault-free circuit of Case A.....	6
Figure 2.4 A Faulty circuit of Case A.....	6
Figure 2.5 A Fault-free circuit of Case B.....	7
Figure 2.6 A Faulty circuit of Case B.....	7
Figure 2.7 (a) Oscillation relation of state set [a, b].....	9
Figure 2.7 (b) Circuit diagram of state set [a, b].....	9
Figure 2.8 (a) Oscillation relation of state set [a, d]	10
Figure 2.8 (b) Circuit diagram of state set [a, d]	10
Figure 2.9 (a) Operation set {L, L}.....	12
Figure 2.9 (b) Operation set {H, H}.....	12
Figure 2.10 Example of operation set {L, L}.....	12
Figure 2.11 (a) Operation set {L, H}.....	13
Figure 2.11 (b) Operation set {H, L}.....	13
Figure 2.12 Example of operation set {L, H}.....	13
Figure 2.13 (a) Operation set {L, R}.....	14
Figure 2.13 (b) Operation set {H, F}.....	14
Figure 2.14 Example of operation set {L, R}.....	14
Figure 2.15 (a) Operation set {L, F}.....	14
Figure 2.15 (b) Operation set {H, R}.....	14
Figure 2.16 Example of operation set {L, F}.....	15

Figure 2.17 (a) Condition I of state patterns.....15

Figure 2.17 (b) Condition II of state patterns.....15

Figure 2.18 (a) $W \uparrow$ in Condition II.....16

Figure 2.18 (b) $W \uparrow$ in Condition I.....16

Figure 3.1 Flow chart of OR-Test by state transition table.....17

Figure 3.2 Illustration of finding input sequence.....19

Figure 3.3 Binary search of Table 3.1.....20

Figure 3.4 Flow chart of finding state patterns.....21

Figure 3.5 Simple flow chart of fault simulation.....22



List of Tables

Table 2.1 A State transition table.....	8
Table 2.2 (a) True table of state variable.....	11
Table 2.2 (b) Function table of feedback cell.....	11
Table 3.1 Example of state transition table.....	19
Table 3.2 State transition table in certain input.....	21
Table 4.1 Experimental results applying the OR Test methodology to benchmark circuits.....	25
Table 5.1(a) Original flow table of an asynchronous circuit.....	28
Table 5.1(b) Original state transition table of an asynchronous circuit.....	28
Table 5.2 State sets of oscillation rings of Table 5.1.....	28
Table 5.3 State transition table after executing Step 2.....	29
Table 5.4 State transition table after executing Step 3.....	29
Table 5.5 State transition table after executing Step 5.....	30
Table 5.6 Final state transition table.....	30
Table 5.7 Simulation result of two state transition tables.....	31