Modeling Harmonic Distortions Caused by Nonlinear Op-Amp DC Gain for Switched-Capacitor Sigma–Delta Modulators

Fu-Chuang Chen and Chih-Lung Hsieh

***Abstract*—Op-amps are crucial components in sigma–delta modulators (SDMs). As device dimensions and supply voltages continue to scale down, it is increasingly critical to determine a suitable op-amp dc gain. If the dc gain is set too high, then the op-amp consumes too much power; if the dc gain is too small, then nonlinear distortion becomes serious. However, there exists no efficient approach for selecting dc gains. In this brief, we propose to use a nonlinear function to model nonlinear op-amp dc gain curves. Then, this nonlinear function is employed to derive an SDM nonlinear distortion model as a function of SDM system parameters. The obtained SDM nonlinear distortion model can subsequently be used to compute the minimum required op-amp dc gain such that nonlinear distortions are kept under a tolerable value. The nonlinear dc gain curve model and the SDM nonlinear distortion model proposed in this brief are verified by behavior simulations and transistor-level simulations.**

***Index Terms*—Nonlinear distortion, op-amp dc gain, sigma–delta modulator (SDM).**

I. Introduction

SIGMA–DELTA modulators (SDMs) based on switched-capacitor circuits have been suitable for high-resolution applications. Recently, low-power designs have become a very important trend for SDM applications. Since op-amps consume most power in SDM, it is crucial to determine a suitable op-amp dc gain. If the dc gain is set too high, then the op-amp can consume too much power; if dc gain is too small, then nonlinear distortion can become serious. However, there exists no efficient and systematic approach for selecting dc gains.

Currently, there are two major approaches for selecting op-amp dc gains. The first approach is *ad hoc* based [1]–[3], which usually suggests setting the dc gain at a sufficiently large value, e.g., 70 dB, so that nonlinear distortion can be small enough. This can be too conservative, since the dc gain can actually be smaller for certain applications. The other approach for selecting the op-amp dc gain requires intensive simulations and subsequent computations [4]–[6]. In this approach, time-consuming SPICE simulation is first used to identify the nonlinear dc gain curve of a specific op-amp design, and then the magnitude of distortion is computed from the nonlinear curve identified. If the computed distortion is too large or too conservative (too small), then the op-amp design has to be modified so that the dc gain can be adjusted. Then, one needs to carry out the aforementioned simulation and computation again. This iterative process would continue until a suitable dc gain is determined. Therefore, the existing approaches are either not accurate enough or not time efficient.

In this brief, we propose an accurate and efficient approach for selecting the op-amp dc gain. An essential first step in our method is the creation of a general model for nonlinear op-amp dc gain curves. The importance of this nonlinear dc gain model is that it eliminates the need for time-consuming SPICE simulations described above. Then, the nonlinear dc gain curve model can be employed to analytically derive the nonlinear distortion, which appears at the SDM output. Since the nonlinear distortion model is expressed in terms of dc gain and other SDM parameters, it can be used to accurately compute the minimum required op-amp dc gain such that the nonlinear distortion is kept under a tolerable value. The nonlinear dc gain curve model and the nonlinear distortion model are verified by transistor-level simulations. Their application to SDMs is verified by behavior simulations.

II. Op-Amp Nonlinear DC Gain Curves

A. DC Gain Distortion Can Be Severe

A second-order SDM with $OSR = 20$, $V_{\mathrm{OS}} = 0.6$, a 3-bit quantizer, a 1-V sinusoidal input signal, and a relatively small dc gain $A_O = 50$ dB will see a severe dc gain distortion at about -61 dB, which easily dominates other noises and distortions, e.g., quantization noise (-81 dB) and digital to analog converter distortion (-76 dB, without dynamic element matching), and results in a poor signal to noise plus distortion ratio at 60 dB.

B. Modeling Nonlinear DC Gain Curves

It is well known that the output resistance of op-amp output-stage transistors is dependent on the output voltage V_O. This dependency results in nonlinear op-amp dc gain when V_O changes, as shown in Fig. 1. A typical nonlinear dc gain curve can be approximated by the polynomial

$$A_V(V_o) = A_0\left(1 + q_2 V_o^2 + q_4 V_o^4\right) \tag{1}$$

where $A_V(V_o)$ is the nonlinear dc gain of the op-amp, and A_O is the maximum dc gain when V_O is in the neighborhood of 0 V.

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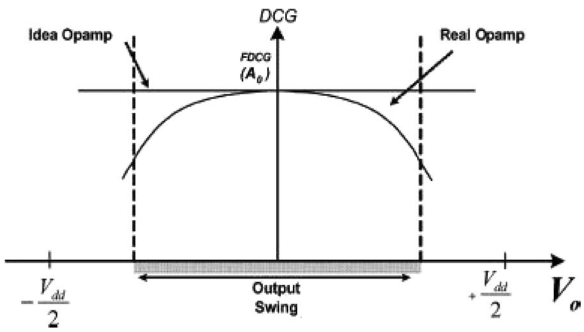


Fig. 1. DC-gain curve versus output voltage with the rail-to-rail voltage of VDD.

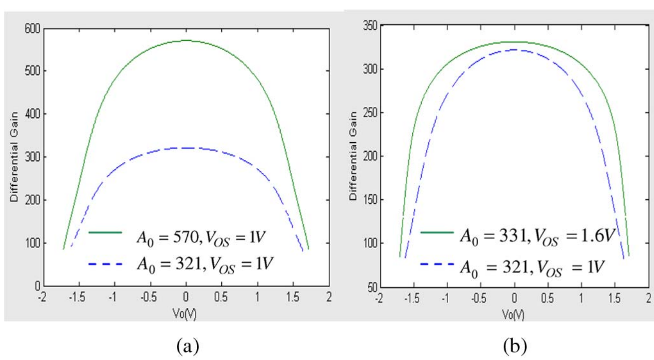


Fig. 2. (a) Two nonlinear dc gain curves with identical V_{OS} but different A_O. (b) Two nonlinear dc gain curves with similar A_O but different V_{OS}.

It is well known that the $|V_{\mathrm{GSQ}}|$ of the output-stage transistors and the maximum dc gain A_O are the only two parameters that can affect the shape of the nonlinear curves $A_V(V_0)$. It is also well known that maximum output swing V_{OS} and $|V_{\mathrm{GSQ}}|$ have a germane relation with each other. Since V_{OS} makes much more sense for practical designers, we replace $|V_{\mathrm{GSQ}}|$ by V_{OS}, and in the rest of this brief, V_{OS} and A_O are the only two parameters that affect $A_V(V_o)$. To demonstrate the effects of V_{OS} and A_O on $A_V(V_o)$, SPICE op-amp simulations in Fig. 2(a) and (b) respectively show the effects that A_O and V_{OS} can have on the shape of the dc gain curves.

To model the nonlinear gain $A_V(V_0)$, we tried various combinations of A_O and V_{OS} to create a set of representative curves for the family of nonlinear dc gain curves. Then, we endeavored to find out suitable q_2 and q_4 such that (1) can reasonably fit all of these curves. After intensive trials and errors, we come up with q_2 and q_4 in (1) to be

$$q_2 \equiv -9 \cdot \left(\frac{A_O^{0.01}}{(1+V_{\mathrm{OS}})^{2.6}}\right)^2 \tag{2}$$

$$q_4 \equiv -6 \cdot \left(\frac{A_O^{0.0001}}{(1+V_{\mathrm{OS}})^{0.83}}\right)^4. \tag{3}$$

Although q_2 and q_4 are obtained from trials and errors, the searching and testing time for them is more than one year. We are confident that the model in (1)–(3) is sufficiently general and accurate, as is verified in the next section.

C. Verifying Nonlinear DC Gain Curve Model

Comparisons of dc gain curves from real op-amps and from our model (1)–(3) are shown in Fig. 3. The comparisons are deliberately planed to cover various op-amp structures and representative points in op-amp parameter space. The subfigures in Fig. 3 are cross related as follows.

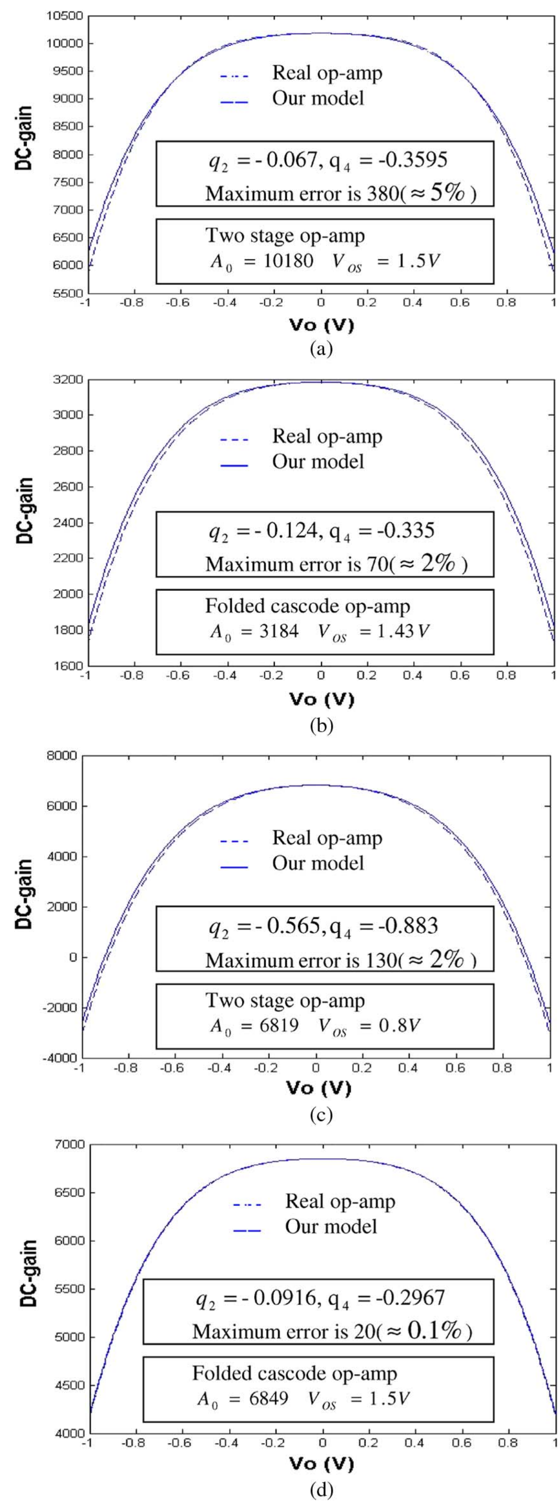


Fig. 3. Comparisons between op-amp nonlinear dc gain curves (solid line) from real op-amp and (dashed line) from our model.

1) Parts (a) and (c) show two-stage op-amps, and parts (b) and (d) show folded cascode op-amps.
2) Parts (a) and (b) show a large difference in the values of A_O.
3) Parts (c) and (d) mainly differ in V_{OS}.

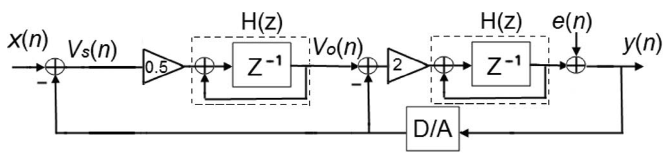
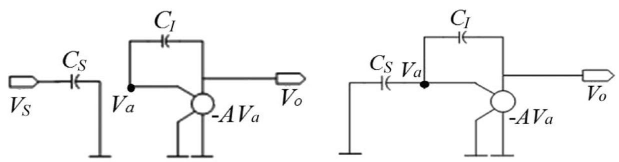


Fig. 4. Single-loop second-order ΣΔ modulator.



(a) (b)

Fig. 5. Switch-capacitor integrator with nonlinear dc gain op-amp. (a) Sampling phase. (b) Integration phase.

For the four cases presented in Fig. 3, the errors between op-amp nonlinear dc gain curves from real op-amps and from our model range from 0.1% to 5%. This demonstrates that our model [see (1)–(3)] is sufficiently general and accurate.

III. SDM Distortion Due to the Nonlinear DC Gain of the Operational Amplifier

In Section II, we analyzed the op-amp nonlinear dc gain phenomenon and obtained a nonlinear dc gain model (1)–(3). In this section, based on the model in (1)–(3), we want to derive a nonlinear distortion model for single-loop second-order SDM output distortions caused by nonlinear dc gain in op-amps. Fig. 4 shows the block diagram of an ideal SDM. We will first discuss the property of V_S, which is the input to the first integrator. Then, the transfer characteristics of the integrator are analyzed, based on which the SDM nonlinear dc gain distortion model is derived. Distortion models for other SDM structures can be obtained following the approach in this section.

A. Properties of V_S

In Fig. 4, the switched-capacitor integrator input V_S can be expressed as

$$V_S(z) = (1 - z^{-2})X(z) - (1 - z^{-1})^2 E(z) \tag{4}$$

which includes the signal and noise parts. The noise part can be ignored here. To analyze the signal part, with $x(n) = A_{\text{in}} \sin(wnT)$, we perform inverse z-transform in (4) and obtain

$$\begin{aligned} V_S(nT) &= A_{\text{in}} \sin(wnT) \\ &\quad - A_{\text{in}} \sin\left(w(n-2)T\right) \cdot u\left(w(n-2)T\right) \\ &\approx A_{\text{in}} \cdot \sin\left(\frac{2\pi}{OSR}\right) \cdot \cos(wnT). \end{aligned} \tag{5}$$

Then, the amplitude of V_S can be approximated as

$$|A_{VS}| = |V_S(2nT)| = |A_{\text{in}} \sin(2wnT)| \cong 2A_{\text{in}} \cdot w \cdot T. \tag{6}$$

B. Transfer Characteristics of the First Integrator

The sampling and integration phases of a switch capacitor integrator are shown in Fig. 5. In the following discussion, signals $V_O((n+1/2)T)$, $V_O((n-1/2)T)$, and $V_S(nT)$ will respectively be denoted by V_O^+, V_O^-, and V_S. Suppose the settling problem is ignored, which requires separate treatment. Then, the sampling phase is ideal, and the input/output characteristics of the integration phase can completely be described by the following three equations:

$$A_V(V_O) = A_O\left(1 + q_2 V_O^2 + q_4 V_O^4\right) \tag{7}$$

$$V_O^{\pm} = -A_V\left(V_O^{\pm}\right) \cdot V_a^{\pm} \tag{8}$$

$$C_I \cdot \left(V_o^+ - V_a^+\right) - C_S \cdot V_a^+ = C_I \cdot \left(V_o^- - V_a^-\right) + C_S \cdot V_S. \tag{9}$$

Substituting (7) and (8) into (9), we obtain the following expression:

$$\begin{aligned} &V_O^+ - V_O^- \\ &= K_S \cdot \Bigg\{ 1 + \frac{1}{A_O} \\ &\quad \cdot \Big[q_2 \cdot \left(\left(V_O^+\right)^2 + \left(V_O^+\right)\left(V_O^-\right) + \left(V_O^-\right)^2 \right) + \left(q_4 - q_2^2\right) \\ &\quad \cdot \left(\left(V_O^+\right)^4 + \left(V_O^+\right)^3 \left(V_O^-\right)^1 + \left(V_O^+\right)^2 \left(V_O^-\right)^2 \right. \\ &\quad \left. + \left(V_O^+\right)^1 \left(V_O^-\right)^3 + \left(V_O^-\right)^4 \right) \Big] + \cdots \frac{1}{A_O^{\infty}} \Bigg\} \cdot V_S \end{aligned} \tag{10}$$

where K_S is C_S/C_I. The problem with (10) is that the integrator output $V_O^{\pm}$ also appears on the right-hand side of (10). However, since $V_O^{\pm}$ can be shown to relate to V_S in (5) as

$$\begin{aligned} V_O^{\pm} \approx &-\frac{K_S}{1 + \frac{1+K_S}{A_O}} \cdot \frac{1}{\sqrt{4 - \frac{4 \cdot K_S}{A_O} \cdot \sin\frac{wT}{2}}} \\ &\cdot \left\{ A_{VS} \cdot \sin\left(w \left(n \pm \frac{1}{2} \right) T \right) \right\} \end{aligned} \tag{11}$$

$V_O^{\pm}$ and V_S at the right-hand side of (10) can be substituted by (11) and (5), which results in

$$\begin{aligned} &V_O^+ - V_O^- \\ &= K_S \cdot \frac{1}{A_O} \Bigg\{ \frac{3}{4 - \frac{4K_s}{A_O}} \cdot \left(\frac{K_S}{1 + \frac{1+K_S}{A_O}} \right)^2 \cdot A_{VS}^2 \cdot q_2 \\ &\quad \cdot \cot^2\left(\frac{1.5708}{OSR}\right) \cdot \sin^2(wnT) \\ &\quad + \frac{5}{\left(4 - \frac{4K_S}{A_O}\right)^2} \cdot \left(\frac{K_S}{1 + \frac{1+K_S}{A_O}} \right)^4 \cdot A_{VS}^4 \\ &\quad \cdot \left(q_4 - q_2^2\right) \cdot \cot^4\left(\frac{1.5708}{OSR}\right) \cdot \sin^4(wnT) \\ &\quad + \frac{10}{\left(4 - \frac{4K_S}{A_O}\right)^2} \cdot \left(\frac{K_S}{1 + \frac{1}{A_O}} \right)^4 \cdot A_{VS}^4 \\ &\quad \cdot \left(q_4 - q_2^2\right) \cdot \cot^2\left(\frac{1.5708}{OSR}\right) \cdot \cos^2(wnT) \\ &\quad \cdot \sin^2(wnT) + \frac{1}{\left(4 - \frac{4K_S}{A_O}\right)^2} \cdot \left(\frac{K_S}{1 + \frac{1}{A_O}} \right)^4 \\ &\quad \cdot A_{VS}^4 \cdot \left(q_4 - q_2^2\right) \cdot \cos^4(wnT) \Bigg\} \\ &\cdot \left\{ A_{\text{in}} \sin(wnT) - A_{\text{in}} \sin\left(w(n-2)T\right) \cdot u\left((n-2)T\right) \right\}. \end{aligned} \tag{12}$$

Equation (12) can be used to compute the nonlinear dc gain distortions appearing at first integrator output.

C. Nonlinear DC Gain Distortions at SDM Output

It is known that if the gain of the second integrator is equal to 1, i.e., $C_{S2}/C_{I2} = 1$, then the same distortions appearing at the first integrator output would appear at the SDM output. Otherwise, some modification is needed on the distortions at the SDM output. Suppose the second integrator gain is equal to 1. Then, the third harmonic magnitude in dc gain distortions can be computed from (12) as

$$\begin{aligned} \mathrm{A}_{\sin\_3} &= K_S \cdot \frac{1}{A_O} \cdot \frac{1}{16} \\ &\cdot \left\{ \left[\frac{-12}{4-\frac{4K_S}{A_O}} \cdot \cot^2\left(\frac{1.5708}{OSR}\right) + \frac{4}{4-\frac{4K_S}{A_O}} \right] \right. \\ &\cdot \left[\frac{K_S}{1+\frac{1+K_S}{A_0}} \right]^2 \cdot A_{VS}^2 \cdot A_{\text{in}} \cdot q_2 \\ &+ \left[\frac{-25}{\left(4-\frac{4K_S}{A_O}\right)^2} \cdot \cot^4\left(\frac{1.5708}{OSR}\right) + \frac{10}{\left(4-\frac{4K_S}{A_O}\right)^2} \right. \\ &\left. \cdot \cot^2\left(\frac{1.5708}{OSR}\right) + \frac{3}{\left(4-\frac{4K_S}{A_O}\right)^2} \right] \\ &\left. \cdot \left[\frac{K_S}{1+\frac{1+K_S}{A_0}} \right]^4 \cdot A_{VS}^4 \cdot A_{\text{in}} \cdot \left(q_4 - q_2^2\right) \right\} \\ &\cdot \left[1 - \cos\left(\frac{2\pi}{OSR}\right) \right] \end{aligned} \tag{13}$$

$$\begin{aligned} \mathrm{A}_{\cos\_3} &= K_S \cdot \frac{1}{A_O} \cdot \frac{1}{16} \\ &\cdot \left\{ \left[\frac{-12}{\left(4-\frac{4K_S}{A_O}\right)^2} \cdot \cot^2\left(\frac{1.5708}{OSR}\right) - \frac{4}{\left(4-\frac{4K_S}{A_O}\right)^2} \right] \right. \\ &\cdot \left[\frac{K_S}{1+\frac{1+K_S}{A_0}} \right]^2 \cdot A_{VS}^2 \cdot A_{\text{in}} \cdot q_2 \\ &+ \left[\frac{-15}{\left(4-\frac{4K_S}{A_O}\right)^2} \cdot \cot^4\left(\frac{1.5708}{OSR}\right) - \frac{10}{\left(4-\frac{4K_S}{A_O}\right)^2} \right. \\ &\left. \cdot \cot^2\left(\frac{1.5708}{OSR}\right) + \frac{5}{\left(4-\frac{4K_S}{A_O}\right)^2} \right] \\ &\left. \cdot \left[\frac{K_S}{1+\frac{1+K_S}{A_0}} \right]^4 \cdot A_{VS}^4 \cdot A_{\text{in}} \cdot \left(q_4 - q_2^2\right) \right\} \\ &\cdot \left[\sin\left(\frac{2\pi}{OSR}\right) \right]. \end{aligned} \tag{14}$$

TABLE I
RELATIONSHIP BETWEEN EACH PARAMETER AND THE HARMONIC DISTORTIONS

	$C_I\uparrow$	$C_S\uparrow$	$A_{in}\uparrow$	$A_0\uparrow$	$V_{os}\uparrow$	$OSR\uparrow$
Distortion magnitude	↓	↑	↑	↓	↓	↓

TABLE II
MINIMUM REQUIRED A_O AND OSR

HD3 distortion power(dB)	HD5 distortion power(dB)	A_0	***OSR***
-70	-80	≧1000	≧16
-90	-100	≧3000	≧64
-110	-120	≧6400	≧256

The forms for magnitudes of fifth harmonics $A_{\sin\_5}$ and $A_{\cos\_5}$ can also be computed from (12), but are omitted here. Then, the powers of the third and fifth harmonic distortions are

$$HD3_{\text{NFDCG}}\ (\text{in decibels}) = 10\log\frac{\left(A_{\sin\_3}^2 + A_{\cos\_3}^2\right)}{2} \tag{15}$$

$$HD5_{\text{NFDCG}}\ (\text{in decibels}) = 10\log\frac{\left(A_{\sin\_5}^2 + A_{\cos\_5}^2\right)}{2}. \tag{16}$$

The model in (13)–(16) indicates that the dc gain distortions at SDM output are related to C_I, C_S, A_{in}, A_O, V_{OS}, and OSR. Some qualitative properties about how each parameter can affect the distortion magnitude are obtained from (13)–(16) and listed in Table I.

Some quantitative investigation based on (13)–(16) shows that A_O and OSR are the most influential parameters on SDM dc gain distortions. Therefore, an interesting example about how (13)–(16) can be utilized is that if the four parameters are fixed at $A_{\text{in}} = 1$ v, $V_{\text{OS}} = 0.8$, $C_S = 1$ pF, and $C_I = 2$ pF, then (13)–(16) can be employed to determine the minimum A_O and OSR required so that the dc gain distortion can be kept under a certain value. The results are tabulated in Table II.

Due to loop shaping, the dc gain nonlinearity in the second integrator degrades the performance to a much lesser extent, allowing a more relaxed design [7]. Therefore, only the dc gain distortion caused by first integrator is considered in this brief.

IV. TRANSISTOR-LEVEL SIMULATION RESULT

The proposed model serves as a powerful tool for analyzing the nonlinear dc gain distortion for SDMs. To verify the accuracy of our model at transistor level, the circuit of a general integrator has been realized using classical two-stage architecture in SPICE.

The specifications of the op-amp are $A_O = 80$ dB, $V_{\text{OS}} = \pm 1.5$ V, $K_S = 1$, and the sinusoidal input frequency is 10 k. The integrator output fast Fourier transform (FFT) is shown in Fig. 6. The total harmonic distortion is mainly determined by the third harmonic distortion (HD3) and the fifth harmonic distortion (HD5). It is indicated in Fig. 6 that HD3 and HD5 are −56.9 and −67.3 dB, respectively, and the HD3 and HD5 generated from our model are −63.9 and −73.5978 dB, respectively. The theoretical and simulation results are close and listed in Table III.

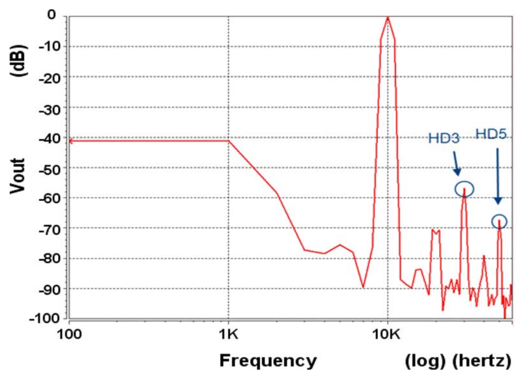


Fig. 6. SPICE simulation FFT results with $K_S = 1$, $A_O = 80$ dB, $V_{\mathrm{OS}} = 1.5$ V, and $F_{\mathrm{in}} = 10$ k.

TABLE III
COMPARISON OF THEORETIC RESULT AND SPICE SIMULATION

	Theoretic (dB)	Spice simulation (dB)
HD3	-63.9	-56.9
HD5	-73.5978	-67.3

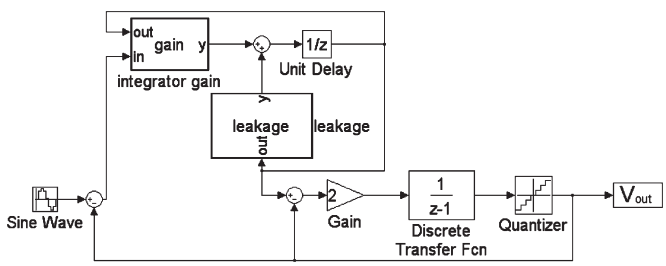


Fig. 7. Second-order SDM behavior model with nonlinear dc gain.

V. Behavior Model Simulation Results

A. Behavior Model of Nonlinear DC Gain

We use a calculable behavior model to verify our SDM nonlinear dc gain distortion model. The z-domain transfer function of a delayed integrator of SDM is

$$H(z) = g \cdot \frac{z^{-1}}{1 - \alpha \cdot z^{-1}} \tag{17}$$

where g and α are the integrator gain and the leakage, respectively [8].

B. Behavior Model of SDM With Nonlinear DC Gain

Then, one can place the nonlinear dc gain behavior model in (17) into the complete SDM behavior simulation scheme. The diagram is shown in Fig. 7.

The behavior simulations are conducted for two different cases. The SDM output FFTs are shown in Fig. 8. The comparisons between simulation results and theoretical results are shown in Table IV. The results from both simulation cases are very close to those obtained from our dc gain distortion model.

VI. Conclusion

In this brief, we have first derived the model for op-amp nonlinear dc gain curves and then the model for dc gain distortion at SDM output. The nonlinear dc gain curve model has never been seen in the literature before. It can be useful and important for

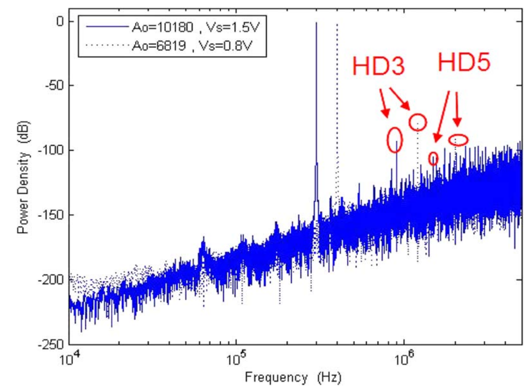


Fig. 8. Modulator's output power spectral density.

TABLE IV
COMPARISON OF THEORETIC RESULT AND SIMULINK SIMULATION

	Theoretic (dB)	Simulink(dB)
$A_o = 10180$, $V_{os} = 1.5$	HD3 = -93.72 HD5 = -105.42	HD3 = -92.55 HD5 = -104.2
$A_o = 6819$, $V_{os} = 0.8$	HD3 = -81.44 HD5 = -94.23	HD3 = -80.19 HD5 = -93.43

both industrial and academia applications. The completeness and precision of our dc gain distortion model are also new and important contributions. Both models are intensively verified by transistor-level and/or behavior simulations.

There are many different ways to apply the two models proposed in this brief, some of which have been suggested in Section III. In particular, our models will be very useful in model-based $\Sigma\Delta$ modulator design optimization. Behavior-simulation-based $\Sigma\Delta$ modulator design optimization has been reported in [9]. In comparison, model-based optimization can be much faster and provide more insights about the system under design.

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