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## OPTIMIZATION AND MODELING FOR MOS VARACTORS IN 65 nm LOW-POWER MIXED-SIGNAL/RADIO-FREQUENCY TECHNOLOGY

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**ABSTRACT:** CMOS technology scaling opens up the possibility of designing variable capacitors based on a metal oxide semiconductor (MOS) structure with improved tuning range and quality factor. In this work, the high  $Q$ -factor 24 and 21, wide tuning ratio 45% and 36% can be achieved by 65 nm low power technology  $n^+/n$ -well and  $p^+/p$ -well MOS varactor up to 10 GHz, respectively. Meanwhile, the equivalent circuit model, to model intrinsic and extrinsic parameters of MOS varactor, also have demonstrated that parasitic resistance is a main issue to dominate  $Q$ -factors, and the measured flicker noise result of MOS varactor is directly dependant on gate leakage current. © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 2119–2121, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24567

**Key words:** CMOS; MOS varactor; LC\_tank;  $Q$ -factor; flicker noise

### 1. INTRODUCTION

The growth of modern wireless communication system calls for lower cost and more integrated wireless transceivers [1]. The voltage-controlled oscillator (VCO) is one of the key elements of

modern wireless transceivers. A high-efficiency VCO with low-phase noise requires a high-quality LC tank, in which both the inductor and varactor need to have high  $Q$ -factor [2]. The metal oxide semiconductor (MOS) varactor, completed with other capacitors, has some advantages such as a smaller size, a higher tuning ratio, and a larger unit capacitance than the  $p$ - $n$  junction varactor [3]. Currently, some modified methods of micromachined [4], gated varactor [5], SOI varactor [6] come close to the high performance of high tuning ratio and high  $Q$ -factors. However, with an increasing oscillator frequency, it is very difficult to obtain both optimized high  $Q$ -factors and high tuning-ratio range MOS varactor without a post-process variation. For this reason, it is necessary to study the geometrical relationship between MOS varactor with high  $Q$ -factors and tuning ratio urgently as well as its scalable equivalent circuit models. The simulated result agreed with the measured result, which predicted that parasitic parameters could be truly reflected on its electrical behavior.

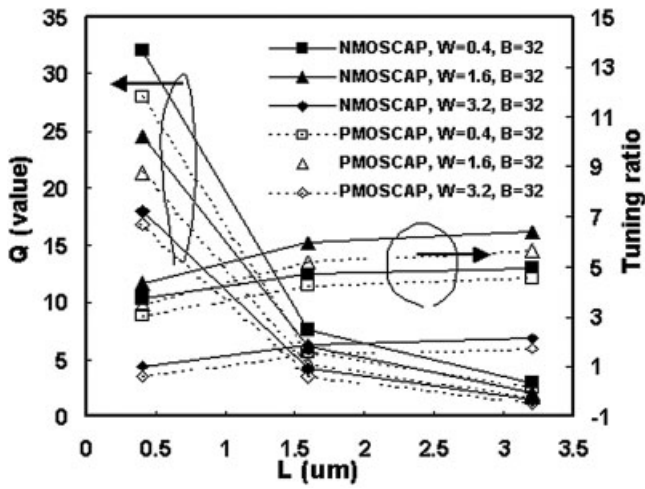
Besides, the phase noise of VCO usually comes from MOSFET and the circuit design and few papers studies have shown that the MOS varactor has a relationship with noise characteristics [7]. However, the  $1/f$  noise at low frequencies can be converted to a higher frequency, contributing to a  $1/f^3$  sideband around the carrier frequency, which impacts on the phase noise in these nonlinear circuits [8]. To explore current leakage affecting flicker noise, the measured flicker noise on MOS varactor also is explained in this article.

### 2. EXPERIMENTAL SETUP DESCRIPTION

MOS varactors are manufactured in 65 nm low-power (LP) CMOS process and characterized on the CASCADE probe station for full wafer measurement. The  $S$ -parameters measurements were carried out up to 30 GHz by using the CASCADE on-wafer probes, an Agilent 8510C network analyzer, and the dummy devices for the open and short calibration to eliminate the parasitic effects of probe pads from the Si substrates. Agilent 3561A dynamic signal analyzer is used to measure the low-frequency noise, in the frequency range from 10 to 100 kHz, with an external low-noise amplifier.

### 3. DEVICE CHARACTERISTICS AND MODELS

To optimize both  $Q$ -factors and tuning range of MOS varactor, the channel length ( $L$ ), the channel width ( $W$ ), and  $p$ -well and  $n$ -well could be viewed as flexible parameters to approach the high  $Q$ -factors and tuning range, respectively. Moreover, the fixed oxidation definition (GROUP) and finger number (BRANCH) can support the  $C$  to minimize parasitic well resistance and maximize the quality factor. In Figure 1,  $Q$  factors are unchanged from the length of 3.2  $\mu\text{m}$  to 1.6  $\mu\text{m}$ , but increase dramatically when shrinking down from 1.6  $\mu\text{m}$  to 0.4  $\mu\text{m}$ . The dimension of device with  $W \times L \times G \times B = 1.6 \times 0.4 \times 1 \times 32$  has been chosen to be the best candidate for its tuning ratio greater than three and  $Q$  greater than 10 which meets the requirements of a LC tank of 10 GHz. The simulated and measured  $C_F$  model results of  $n^+/n$ -well and  $p^+/p$ -well varactors have been presented in Figure 2(a). Higher than 45% tuning ratio due to scaling channel length to reduce  $C_{\text{dep}}$  and enhance unit capacitance on 65LP NMOS varactor. Thirty-five percent tuning ratio on 65LP PMOS varactor also offer designers to choose different kind of LC\_tank structure [9] to meet VCO with high-quality performance. The capacitance has not shown a large vibration with increasing frequency, so that parasitic inductance is not so sensitive as to affect the capacitance on smaller dimension. The  $C_{\text{min}}$  difference between  $n$ -type and  $p$ -type MOS varactor is due to the difference of substrate doping and



**Figure 1** The simulated Q-factors and tuning ratio for 65LP NMOS and PMOS varactors with different channel lengths and widths for group = 1 and finger number = 32

contact resistance similar with the simulated results. To see the Q-factor, it can be first characterized by the following Eq. (1):

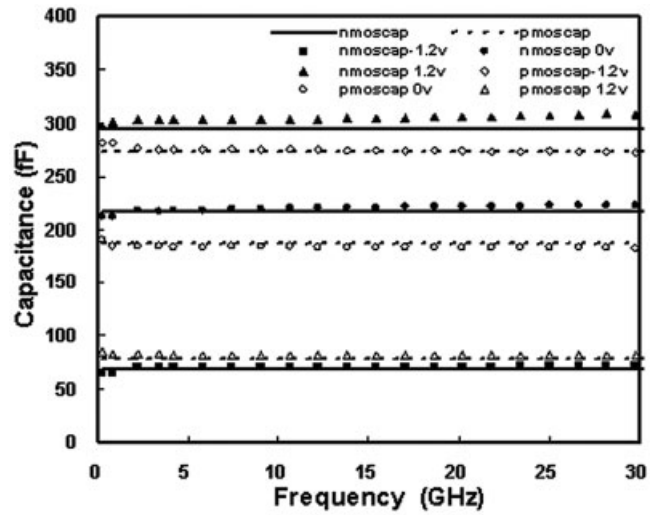
$$Q = \frac{1}{2\pi f R_s C} = \frac{\text{Im}\left(\frac{1}{Y_{11}}\right)}{\text{Re}\left(\frac{1}{Y_{11}}\right)}, \quad (1)$$

where real and image  $Y_{11}$  are caused by the parasitic resistance components and intrinsic capacitance, respectively. In Figure 2(b), the measured data have a good agreement with simulated results so that it is available to compare overall parameters of tuning ratio, Q-factors,  $R_g + R_{ds}$ , and  $R_{sub}$ . The measured Q-factors completely agree with simulated results by extracting the reliable ( $R_g + R_{ds}$ ) resistance 3.27 ohmic/square on NMOS varactor with 4.5 ohmic/square on PMOS varactor and  $R_{sub}$  from 39.8 to 54.8, respectively. It can be explained that different Q-factors between NMOS and PMOS varactor is mainly attributed as dominated parasitic resistance included such  $R_g$ ,  $R_{sd}$ , and  $R_{sub}$  rather than the intrinsic capacitance.

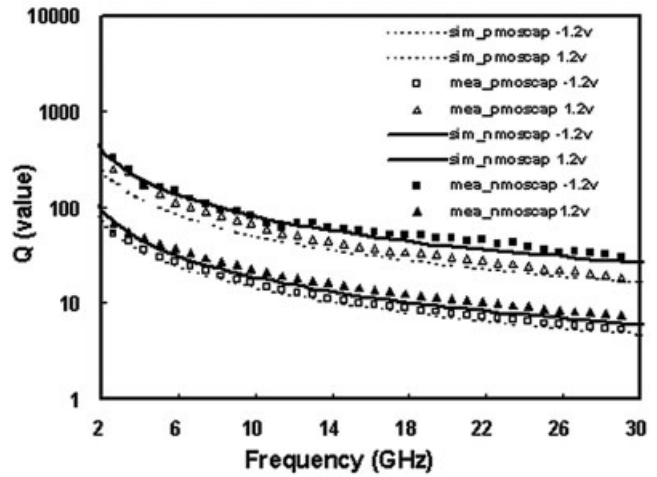
The equivalent circuit of n+/n-well and p+/p-well MOS varactor shown in Figure 3, where the scalable geometrical model can be replaced by intrinsic oxidation capacitance ( $C_{gate}$ ), parasitic resistance, and inductance ( $R_g$ ,  $L_{gate}$ ,  $R_{ds}$ , and  $L_{ds}$ ), n-well and p-well diode, and substrate network ( $R_{sub}$  and  $C_{sub}$ ). To model RF characteristics of MOS varactor, with NMOS and PMOS varactors on 65 technologies is due to n+/n-well in well depletion is significantly larger than that of p+/p-well mainly attributed to higher electron minority carrier mobility in n-well.  $L_{gate}$  and  $L_{sd}$  on this dimension will contribute a minor factor to affect capacitance variation when  $C_{max}$  has the value less than 0.3 pF and demonstrated on asymmetrical C-V model between NMOS and PMOS varactor.

#### 4. FLICKER NOISE ON VARACTOR ELEMENT

Noise characterization also plays an important role since MOS varactors can contribute a little noise that many disturb the operation of circuit. With the constant scaling of channel length and oxide thickness, noise generated by not only active devices but also passive devices increases the phase noise for a VCO. In our equivalent circuit, leakage current is also modeled as the path

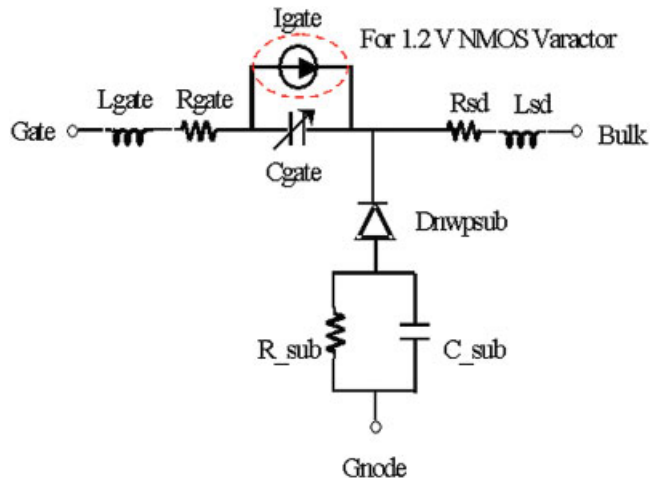


(a)

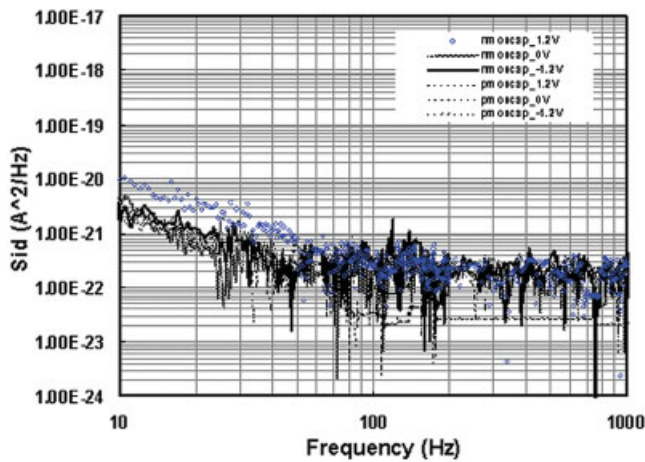


(b)

**Figure 2** (a) The capacitance versus frequency model and (b) Q-factors have a relationship with frequency, of the measured and simulated results for 65 nm NMOS and PMOS varactors, respectively



**Figure 3** Equivalent circuit model for n+/n-well and p+/p-well MOS varactors. [Color figure can be viewed in the online issue, which is available at [www.interscience.wiley.com](http://www.interscience.wiley.com)]



**Figure 4** The measured flicker noise has a relationship with the frequency for 65 nm NMOS and PMOS varactors. [Color figure can be viewed in the online issue, which is available at [www.interscience.wiley.com](http://www.interscience.wiley.com)]

passed from the  $C_{gate}$  to the bulk ground. In Figure 4, the measured MOS varactor flicker noise, where the dimensions of  $W \times L \times G \times B = 1.6 \times 0.4 \times 8 \times 64$ , has presented a different flicker noise level at 1.2 V as a result of the leakage current being one order of magnitude higher compared with other DC bias conditions. This can be explained by the fact that an increased modeling parameter for  $I_{gate}$  results in an increased leakage current of NMOS varactor at 1.2 V. It was noticed that there was an increase in noise when the current was higher than  $10^{-4}$  mA. This phenomenon did not occur when the leakage current is  $10^{-5}$  and  $10^{-6}$  mA at  $-1.2$  and  $0$  V, respectively. Also,  $I_{gate}$  changes the flicker noise level, as  $I_{gate}$  rises above than  $10^{-4}$  mA. Moreover, it was found that measured results for PMOS varactor are always lower than  $10^{-5}$  mA between the  $-1.2$  and  $1.2$  V, so would have no impact on the noise level variation. Although the measured noise of MOS varactor has a lower level than the one created by MOSFET, adding the fitting parameters to the simulator is an unavoidable trend as noise level rapidly increases with increased leakage current.

## 5. CONCLUSIONS

In this study, we investigated the optimum 65 nm LP MOS varactors geometrical relation in terms of microwave characteristics and low frequency noise performances. The equivalent circuit model also achieves precisely extracting parasitic parameters and agrees with measured results. The  $I_{gate}$  parameter of the MOS varactor model also can be validated as a relationship with flicker noise on MOS varactor.

## ACKNOWLEDGMENTS

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## DESIGN OF A STOPBAND-IMPROVED UWB FILTER USING A PAIR OF SHUNT AND EMBEDDED OPEN STUBS

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**ABSTRACT:** In this letter, an ultrawideband (UWB) bandpass filter (BPF) with an improved stopband has been proposed. The proposed UWB BPF, having a lower passband of 3.5–5.2 GHz and a higher passband of 6.5–9.7 GHz, mainly comprises the parallel-coupled lines and slot-line resonator. A wide stopband of the proposed BPF from 10 to 20 GHz can be achieved by using a pair of shunt and embedded open stubs. The proposed UWB BPF is designed, fabricated, and measured. Good agreement with the electro-magnetic simulation and measurement is demonstrated. © 2009 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 51: 2121–2124, 2009; Published online in Wiley InterScience ([www.interscience.wiley.com](http://www.interscience.wiley.com)). DOI 10.1002/mop.24556

**Key words:** ultrawideband (UWB); bandpass filter (BPF); parallel-coupled lines; slot-line resonator (SLR); bandstop filter (BSF)

## 1. INTRODUCTION

Since the U.S. Federal Communications Commission proposed the unlicensed use of ultrawideband (UWB) (range of 3.1–10.6 GHz) for commercial purposes in early 2002 [1], the UWB bandpass filter (BPF) has been investigated extensively. Recently, several methods for designing UWB BPFs have been proposed, such as multiple-mode resonator [2], stepped-impedance resonator (SIR) [3], parallel coupled line [4], or slot-line structure [5–8]. For example, a UWB BPF is proposed by using two microstrip open-circuited stubs coupled to a single CPW resonator on the other side of a commercial substrate [5]. Additionally, a notch band is needed