Electrostatic Discharge Robustness of Si Nanowire Field-Effect Transistors

Wen Liu, Juin J. Liou, Andy Chung, Yoon-Ha Jeong, Wei-Chen Chen, and Horng-Chih Lin

***Abstract*—Electrostatic discharge (ESD) performance of N-type double-gated Si nanowire (NW) thin-film transistors is investigated, for the first time, using the transmission line pulsing technique. The ESD robustness of these devices depends on the NW dimension, number of channels, plasma treatment, and layout topology. The failure currents, leakage currents, and ON-state resistances are characterized, and possible ESD protection applications of these devices for future NW field-effect-transistor-based integrated circuits are also discussed.**

***Index Terms*—Electrostatic discharge (ESD), failure current I_{t2}, nanowire (NW) field-effect transistor, ON-state resistance.**

I. Introduction

As THE scaling of silicon devices continues, nanowire (NW) structures have received increasing attention [1], [2]. The availability of electrostatic discharge (ESD) protection solutions is known to be a serious problem for integrated circuits (ICs) fabricated using advanced deep-submicrometer technologies [3], and this is particularly true for future NW-based ICs. As such, evaluating and understanding the ESD robustness of NW devices are urgently needed in preparation for the next-generation electronics for commercial applications.

A promising NW device being proposed is the poly-Si NW thin-film transistor (NWTFT) [4], and the schematic of an NWTFT with two square-shaped NWs (i.e., two channels) is shown in the inset of Fig. 1(a). The NWTFT possesses several advantages, including simple fabrication flow, reliable drain/source contact, low cost, and precise alignment of the NWs [5]. In this letter, the suitability of such devices for ESD protection applications will be characterized based on the transmission line pulsing (TLP) technique. To the best of our knowledge, this is the first time that TLP results are presented and analyzed for the NW field-effect transistor.

II. Measurement Results and Discussions

N-channel NWTFTs (N-NWTFTs) having different channel numbers (NW numbers), different channel lengths, an NW width of 43 nm, and an NW spacing of 500 nm were fabricated at the National Chiao-Tung University, Taiwan [4]. Only the bipolar mode (gate grounded) was fully characterized, as it is a configuration commonly employed in ESD protection applications. The Barth 4002 TLP tester was used, which generates pulses equivalent to those associated with the human body model. The experimental TLP results shown in Fig. 1(a) and (b) can be summarized as follows: 1) N-NWTFTs turn on in the voltage range of 10–15 V without the snapback due to the fact that the base terminal of the parasitic bipolar transistor imbedded in the N-NWTFT is floating; 2) a shorter channel length results in a higher failure current I_{t2} (i.e., the currents where the I–V curves end) and smaller on-resistance $R_{\rm on}$ (i.e., the slopes of the I–V curves after the devices are turned on); and 3) while I_{t2} and $R_{\rm on}$ increase and decrease with increasing channel number, they do not scale linearly with the number of channels.

It is worth mentioning that when the gate is connected to the drain (diode mode), the NWTFT triggers at around 0.7 V and exhibits a linear I–V behavior after it is triggered. In addition, its failure current is about four times higher than that of the bipolar mode NWTFT due to the smaller trigger voltage.

To further investigate the ESD robustness, N-NWTFTs having wide and narrow NWs ($W = 43$ and 18 nm) and with and without the plasma treatment were measured and compared in terms of I_{t2}, failure current density J_{t2} ($J_{t2} = I_{t2}/(nanowire\ width \times\ number\ of\ nanowires)$), and leakage current (measured at 1 V) as functions of the channel number and length, as shown in Fig. 2(a)–(f). Plasma treatment is typically used to passivate the inherent intergrain and intragrain boundary defects located in the poly-Si to achieve better electrical characteristics [6]. However, the results in Fig. 2 suggest that the ESD robustness of the N-NWTFT does not benefit from having the plasma treatment, except for the reduced leakage current for large channel number devices. This may result from the possibility that the NWs become more fragile after the treatment. Clearly, the narrower the NW, the higher is the J_{t2}. In addition, increasing the channel number increases the overall I_{t2} but, to a lesser extent, decreases J_{t2}, a trend confirming that I_{t2} does not scale linearly with the

Manuscript received May 17, 2009. First published July 21, 2009; current version published August 27, 2009. This work was supported in part by a research grant provided by the National Center for Nanomaterials Technology, Pohang University of Science and Technology, Korea, and in part by the Chunhui Scholar Program, Ministry of Education, China. The review of this letter was arranged by Editor C. Bulucea.

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Digital Object Identifier 10.1109/LED.2009.2025610

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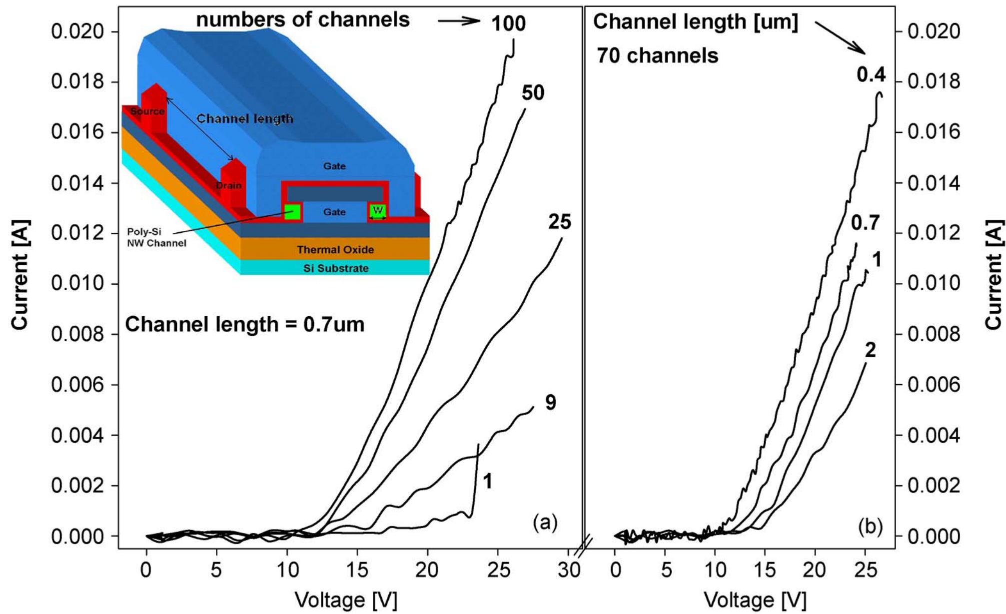

Fig. 1. TLP I–V curves of bipolar mode N-NWTFTs with (a) 0.7-μm channel length and different numbers of channels, and (b) 70 channels and various channel lengths. The inset in (a) shows the structure of a two-NW N-NWTFT.

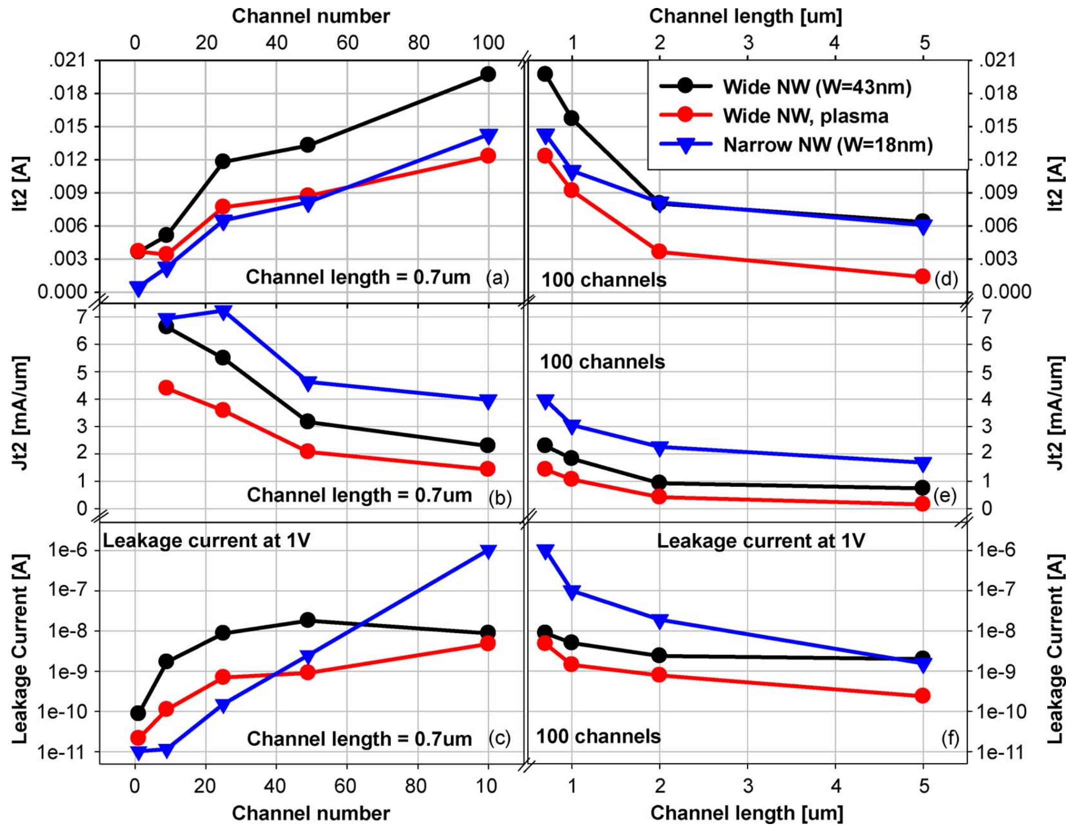

Fig. 2. Comparisons of (a) failure current I_{t2}, (b) failure current density J_{t2}, (c) leakage current versus channel number, (d) I_{t2}, (e) J_{t2}, and (f) leakage current versus channel length for the gate-grounded N-NWTFTs having wide and narrow NWs (width $W = 43$ and 18 nm) and (red lines) with and (black and blue lines) without the plasma treatment.

channel number. When the channel length is increased, both the narrow and wide N-NWTFTs become less robust, but their leakage currents decreased.

The preceding analysis has indicated that the gate-grounded N-NWTFTs with a relatively short channel length and large channel number can be triggered at a moderate voltage and possess an acceptable I_{t2}. This can be attributed to the fact that fewer grains existed in the shorter NWs. Fewer grains lead to a larger voltage drop in each depletion region and, consequently, a higher electric field under the same drain voltage, which allows for the impact ionization to be activated at a smaller voltage (i.e., smaller trigger voltage). Fewer grains can also lower

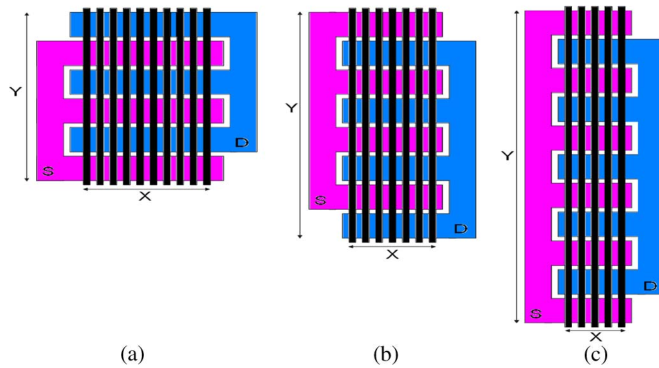

Fig. 3. N-NWTFTs having the same total channel number of 50 but with (a) three drain/source fingers, (b) four drain/source fingers, and (c) five drain and six source fingers. Black lines denote the NW channels.

TABLE I
SUMMARY OF TLP RESULTS OF MULTIPLE-CHANNEL N-NWTFTS HAVING THE THREE DIFFERENT LAYOUTS SHOWN IN FIG. 3(a)–(c)

Layout topology	Channel number	It2 (mA)	Area under nanowires (area of XY) (μm^2)	Leakage current (measured at 1 V) (nA)
Fig. 3(a)	50	12.5	653	3.84
Fig. 3(b)	50	13.3	606	1.81
Fig. 3(c)	50	16.9	589	0.71

the source barrier potential and cause the current conduction to take place deeper in the junction [7], thus giving rise to a higher I_{t2}. The higher I_{t2} is also due, in part, to the smaller trigger voltage when the channel length is reduced [see Fig. 1(b)].

The narrower NW device exhibits a higher J_{t2} due to the presence of the relatively high resistivity in these narrow channels, a mechanism similar to that of MOS device imbedded with a ballast resistor [8], in which the increased voltage drop across the spreading resistance minimizes the likelihood of filamentation. Note that, for the same channel number, using wider NWs gives rise to a larger device size and, hence, a larger I_{t2} even though J_{t2} is smaller.

The decreasing J_{t2} versus channel number characteristics [Fig. 2(b)] are resulted from the nonuniform turn-on among the multiple channels of N-NWTFTs. This undesirable effect can be minimized by choosing a proper drain/source layout topology. Fig. 3(a)–(c) shows devices having three different drain/source layouts but the same total channel number of 50, and their TLP measurement results are compared in Table I. In the direction shown in Fig. 3(a)–(c), while the drain and source finger number is increased (from three to five), the channel number for each drain/source pair is decreased (from ten to five). It is evident that the layout in Fig. 3(c) yields the highest I_{t2}, lowest leakage current, and smallest area under the NWs, followed by the layout in Fig. 3(b), and the layout in Fig. 3(a) renders the worst performance. Therefore, in addition to increasing the total channel number, decreasing the channel length, and decreasing the NW width, increasing the drain and source finger number would be an excellent approach for enhancing the ESD robustness of multiple-channel N-NWTFTs. Nonetheless, the relatively high trigger voltage and low robustness of the grounded-gate NWTFT can impose a great difficulty in implementing ESD protection for future low-power NWTFT-based ICs operating at relatively low operating voltages (i.e., around or below 1 V). More research work is definitely needed to address these issues, and the diode-mode NWTFT having a trigger voltage of about 0.7 V appears to be more attractive for such applications.

III. CONLUSION

This letter presented, for the first time, valuable and interesting data pertinent to the ESD robustness of a promising NW device called the poly-Si NWTFT. The TLP measurement results revealed that these devices are, in general, suitable for serving as ESD protection elements. The study further suggested that a higher ESD robustness can be obtained by decreasing the channel length and increasing the number of channels. For NWTFTs having a fixed number of channels, improved ESD robustness and smaller area consumption can be achieved using a multiple drain/source layout. Plasma treatment commonly used to enhance the electrical performance of poly-Si-based devices did not seem to improve the NWTFT's ESD current handling capability. The finding should provide useful insight into the design of ESD protection solutions for the next-generation NW-based ICs.

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