國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

低電壓能帶隙參考電壓產生器之設計

Research and Design of Low Voltage High PSRR Bandgap Circuit

研 究 生　：王冀康　　Chi-Kang Wang

指導教授　：郭治群博士　　Dr. Jyh-Chyurn Guo

中華民國九十五年八月

低電壓能帶隙參考電壓產生器之設計

Research and Design of Low Voltage High PSRR Bandgap Circuit

研究生：王冀康　　Student : Chi-Kang Wang

指導教授：郭治群 博士　　Advisor : Dr. Jyh-Chyurn Guo

國 立 交 通 大 學

電子工程學系　電子研究所

碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of Master

In

Electronics Engineering

August 2006

Hsinchu, Taiwan, Republic of China

中華民國九十五年八月

低電壓能帶隙參考電壓產生器之設計

研究生：王冀康　　指導教授：郭治群

國立交通大學

電子工程學系　電子研究所　碩士班

中文摘要

從理論分析，bandgap 電路內的 OPA，其 performance 對 bandgap 電路的整體效能有決定性的影響。再者，以 nMOS 作為輸入差動對的 OPA，其 Voltage Gain 會比以 pMOS 作為輸入差動對的 OPA 要好。此外，bandgap 電路內的 OPA，若以 pMOS 作為輸入差動對，則其輸入端的 voltage offset 會被放大 $\frac{R_3}{R_1}(1+\frac{R_{A2}}{R_{A1}})$ 倍。反之，以 nMOS 作為 OPA 輸入差動對的 bandgap 電路，其輸入端的 voltage offset 則只會被放大 $\frac{R_3}{R_1}$ 倍。

然而，由於 bandgap core circuit 的電路架構限制，過去的 bandgap 電路，在使用 CMOS 製程的基礎下，均使用 pMOS 作為其 OPA 的輸入差動對。

因此本篇論文的研究方向，是藉由修改 bandgap core circuit 的架構，突破以往限制，設計出新式的 bandgap 電路，而其 OPA 是以 nMOS 作為輸入差動對。

最後，以 nMOS 作為輸入差動對的 bandgap 電路，與以 pMOS 作為輸入差動對的 bandgap 電路比較後發現：其 layout 所需面積較小，performance 也較好。

本論文總共提出四種不同的電路架構。

Type A與Type B的設計、模擬是使用TSMC 0.18μm CMOS technology。其中Type A電路是使用pMOS作為運算放大器的輸入差動對; 而Type B電路則是使用nMOS作為其運算放大器的輸入差動對。實驗顯示，Type A與Type B 的輸出參考電壓可以達到 772mV與 737mV，相對應的最低工作電壓則為 1.1V。PSRR

(power supply rejection ratio) 部份，Type A / B： -56 / -51 dB, -29 / -33 dB and -15.2 / -26 dB分別對應於 1K, 10K, 100KHz。至於溫度補償方面，$TC_{F(eff)}$ = 140 ppm/℃，from – 40℃ to 140℃。$TC_{F(eff)}$表現較差的原因是diffusion電阻與poly電阻在面對製程變化，其電阻值改變時，diffusion電阻值的改變率與poly電阻值的改變率並不相等，與電路架構無關，這部份在第三章有詳細討論。

Type C與Type D則是將上述二個電路重新設計改良，使其能符合TT, SS, SF, FS, FF等 5 個 process corner condition。電路的設計、模擬是使用TSMC 0.35μm CMOS technology。其中Type C電路是使用pMOS作為運算放大器的輸入差動對; 而Type D電路則是使用nMOS作為其運算放大器的輸入差動對。實驗顯示，Type C與Type D的輸出參考電壓分別可以達到 766mV與 829mV，相對應的最低工作電壓則分別為 1.3V與 1.1V。PSRR部份，Type C / D： -18 / -25 dB, -2.7 / -10 dB and -0.1 / -0.42 dB分別對應於 1K, 10K, 100KHz。PSRR的表現不如預期，推測是因為受到寄生電阻與寄生電容的影響。至於溫度補償方面，Type C / D: 90.2 / 34.1 ppm /℃ at Vdd = 1.3V. 由此實驗結果顯示：$TC_{F(eff)}$ 表現回復正常，因為Type C / D bandgap core circuit內部，均使用相同的電阻材質(即擴散層片電阻)。

Research and Design of Low Voltage High PSRR Bandgap Circuit

Student: Chi-Kang Wang Advisor: Jyh-Chyurn Guo

Department of Electronics Engineering and

Institute of Electronics

National Chiao Tung University

Abstract

OP-Amplifier plays an important role in the bandgap circuits. According to the theory, the OPA which use nMOS as the input stage will get a better voltage gain than that using pMOS as the input stage. Besides, for OPA using pMOS as the input stage, the voltage offset on the input port will be multiplied by $\frac{R_3}{R_1}(1+\frac{R_{A2}}{R_{A1}})$. By contrast, for bandgap circuits that use nMOS as the OPA's input stage, the voltage offset on the OPA's input port will only be multiplied by ($\frac{R_3}{R_1}$).

However, because of the limitation of conventional bandgap circuit for providing the OPA's input common mode voltage, most bandgap circuit was designed by using pMOS as the input stage in the past.

So we modify the conventional bandgap core circuit topology to create new type of bandgap circuit topologies. The new types of topologies can drive OPA that use nMOS as the input stage.

In this thesis, four kinds of low voltage-operated bandgap reference (BGR)

circuits in CMOS technology, with high PSRR (power supply rejection ratio) are presented. Two of those proposed circuits use the OP-Amplifier in which the input stages are composed of pMOS. The others use nMOS as the input stage of the OP-Amplifier.

In this study, TSMC 0.18μm and 0.35μm CMOS process were adopted for circuit fabrication and verification. Type A and B were implemented by using 0.18μm process in which pMOS differential pair were adopted for type A while nMOS differential pair were employed for type B. Regarding type C and D which were fabricated by 0.35μm process, type C adopted pMOS differential pair while type D employed nMOS differential pair.

The experimental results show that it is possible to achieve 700mV reference voltage with low power supply voltage at 1.1V and a well-controlled temperature compensation performance.

For types A and B implemented by 0.18μm technology, the output reference voltages were achieved at 772mV and 737mV corresponding to the minimum supply voltage at 1.10V. PSRR under varying frequencies were achieved at -56 / -51 dB, -29 / -33 dB and -15.2 / -26 dB corresponding to 1K, 10K, and 100KHz for type A / B respectively. The effective temperature coefficient ($TC_{F(eff)}$) was as high as 140 ppm/℃ due to deviation of resistance ratio caused by the asymmetric process variation between diffusion resistors and poly-Si resistors.

As for type C and D fabricated by 0.35μm technology, the output reference voltages were achieved at 766mV and 829mV corresponding to the minimum supply voltage at 1.3 / 1.1V. PSRR under varying frequencies were achieved at -18 / -25 dB, -2.7 / -10 dB and -0.1 / -0.42 dB corresponding to 1K, 10K, and 100KHz for type C / D respectively. The PSRR is not as good as that predicted by simulation due to suspected parasitic resistance and capacitance effects. $TC_{F(eff)}$ were achieved as 90.2 / 34.1 ppm/℃ for type C / D at Vdd = 1.3V, which shows significant improvement as compared with type A / B to adoption of diffusion resistors over the whole circuit chip.

Based on the simulation and measurement results, we make the conclusion that BGR circuits which use nMOS as the OP-Amplifier's differential pair provide better performance and enable lower cost due to reduced chip area.

誌 謝

首先，由衷的感謝指導老師郭治群教授的指導，以及茂達電子謎志吉處長與陳志源學長的協助，帶我進入類比電路這個領域，使我學到不少寶貴的類比電路知識與研究方法。

接下來要感謝國家晶片系統設計中心彭罡(立宁)講師，在“Full Custom IC Design Kit”這門課，教學認真，傳授很多關於晶片實作的寶貴知識、經驗與技術。

此外，還要感謝我想科技陳有棟經理及王智揚副理的指導與協助，從他們身上，我學得了許多關於電路設計的專業知識及為人處世的方法，使我獲益良多。

最後，感謝家人的支持，及實驗室學長、學弟的鼓勵。謝謝所有幫助過我、關心過我的人。

王冀康

九十五年八月

Abstract(Chinese)

Abstract(English)

Acknowledgement

Contents

TABLE CAPTIONS

FIGURE CAPTIONS

符 號 說 明

BGR ：bandgap reference circuit

n-Vref ：output reference voltage of bandgap circuits which use nMOS as the OPA's input differential pair

m ：the ratio of BJT's emitter area of Q_1 and Q_2

OPA ：operational amplifier

PSRR ：power supply rejection ratio

PTAT ：proportional to the absolute temperature

p-Vref ：output reference voltage of bandgap circuits which use pMOS as the OPA's input differential pair

$TC_{F(eff)}$ ：effective temperature coefficient

TC ：temperature compensation

V_{BG} ：temperature compensation voltage

V_{BE} ：base-to-emitter junction voltage of BJT

Vdd ：power supply voltage

Vg ：the gate voltage of pMOS or nMOS

Vgs ：gate-source voltage of pMOS or nMOS

Vthn ：threshold voltage of nMOS

Vthp ：threshold voltage of pMOS

V_{REF} ：output reference voltage of conventional bandgap circuits

Vref ：output reference voltage of bandgap circuits proposed in this thesis

Φ_T ：thermal voltage

ξ ：the slope of the "OPA's input common-mode voltage vs. Temperature" curve

Chapter 1 INTRODUCTION

1.1 Background

Bandgap voltage reference (BGR) circuit have been widely used in analog mixed-mode circuits such as ADC，portable equipments and battery-powered devices. In order to increase battery efficiency and extend battery life time, low voltage BGR circuit is the trend in the near future.

Besides, PSRR is another important issue in BGR design , especially for power management system. Because the power supply noise have a serious impact on BGR circuits performance.

For low voltage requirement, many solutions have been proposed, for example, using Bi-CMOS process [1], biasing the MOSFET in the sub- threshold region [2], or forward biasing the source-bulk junctions of the MOSFET [3], etc. Some of the solutions can be implemented by using the CMOS process, but some others cannot.

As for the high PSRR issue, some useful solutions have been proposed. For example, we can increase the impedance to power supply noise by using cascoded-MOS pair circuits [4]. However it is hard to satisfy the low voltage requirement by using the cascoded-MOS pair circuit topology.

In this thesis, we try to reach the high PSRR requirement based on the low voltage circuit topology implemented by standard CMOS process.

1.2 Review on CMOS Bandgap Reference Circuits (I)

1.2.1 What is The "Bandgap"

The bandgap circuits operates based on the principle of compensating the negative temperature coefficient of V_{BE} (Base-to-Emitter junction voltage) with the positive temperature coefficient of Φ_T (thermal voltage), where Φ_T = kT/q is proportional to the absolute temperature and is often referred it by using the acronym PTAT.

We can create a full temperature compensation voltage at room temperature by combining the terms of positive temperature coefficient with another negative temperature coefficient by the formula given described below：

$$V_{BG} = V_{BE} + M\Phi_T = V_{BE} + M\,(kT / q)$$

Since the temperature coefficient of V_{BE}, at room temperature, is around -2.2 mV/°C；while the positive coefficient of the thermal voltage, Φ_T, is 0.086 mV/°C. The constant coefficient M must be around to 25.6 (=2.2/0.086) in order to make the temperature coefficient of V_{BG} equal to zero at room temperature.

As we know that the value of V_{BE} at low currents is close to 0.60V, and Φ_T at room temperature is 25.8 mV, the voltage of V_{BG} achieved by a bandgap circuit is typically equal to 1.26 V.

$$V_{BG} = V_{BE} + M\Phi_T = 0.60V + 25.6 \times 25.8\ mV = 1.26\ V$$

Such a value is just slightly more than the silicon energy gap (expressed in volts is 1.21 V). Therefore, we normally call this voltage as bandgap reference voltage.

1.2.2 Conceptual Implementation

1.2.2.1 Conventional Bandgap Circuit

Fig.1-1 shows a conventional bandgap circuit. Two components build up the bandgap reference voltage, V_{REF}. One is the voltage across a directly BJT-connected diode (V_{BE}), and the other is Φ_T, a term proportional to the absolute temperature (PTAT).

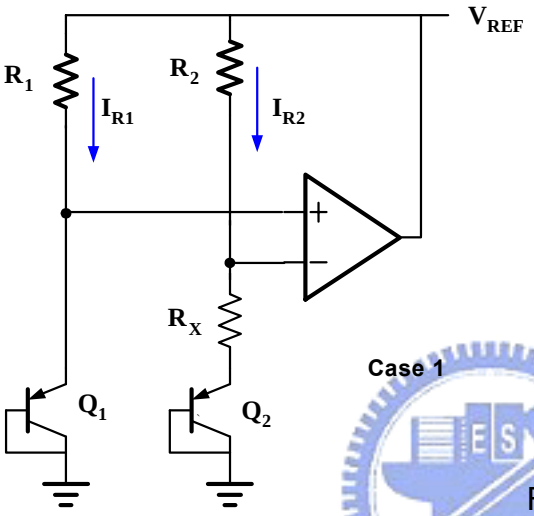


Fig. 1-1 Conventional bandgap circuit

$V_{REF} = V_{R2} + V_{RX} + V_{BE2}$

$\because \quad V_{R2} / V_{RX} = R_2 / R_X$

$V_{R2} = (R_2 / R_X) \times V_{RX}$

$$\therefore V_{REF} = V_{RX}\left(\frac{R_2}{R_X} + 1\right) + V_{BE2} \qquad (1.1)$$

Besides, $V_{RX} = V_{BE1} - V_{BE2} = \Phi_T \ln \frac{I_{R1}}{I_{R2}}$

$$\therefore V_{REF} = M\Phi_T + V_{BE2} \qquad (1.2)$$

where, $M = \ln \frac{R2}{R1} \times \left(\frac{R_2}{R_X} + 1\right)$ is a temperature-independent constant $^{NOTE\_1}$

Secondly, Known : $V_{REF} = M\Phi_T + V_{BE2}$

We hope the temperature coefficient of $V_{REF} = 0$

$$\left(\text{i.e. } \frac{\partial}{\partial T} V_{REF} = M \frac{\partial}{\partial T} \Phi_T \Big|_{T_0} + \frac{\partial}{\partial T} V_{BE2} \Big|_{T_0} = 0 \right)$$

So, we should adjust M, such that

$$M \frac{\partial}{\partial T} \Phi_T \Big|_{T_0} + \frac{\partial}{\partial T} V_{BE2} \Big|_{T_0} = 0 \quad (1.3)$$

Step 1 $\because \Phi_T = \frac{KT}{q}$

$$\therefore \frac{\partial}{\partial T} \Phi_T = \frac{K}{q} = \frac{KT}{q} \times \frac{1}{T} = \frac{1}{T} \Phi_T \quad (1.4)$$

Step 2 $\frac{\partial}{\partial T} V_{BE2} = \frac{\partial}{\partial T} [\Phi_T \times \ln(I_{R2} / I_S)]$

$$= (\frac{\partial}{\partial T} \Phi_T) \ln(I_{R2} / I_S) + \Phi_T \frac{\partial}{\partial T} (\ln I_{R2} - \ln I_S)$$

$$= \frac{1}{T} \Phi_T \ln(I_{R2} / I_S) - \Phi_T \frac{\partial}{\partial T} (\ln I_S) \quad (1.5)$$

Where $I_S = BA_E T^3 \exp(-\frac{V_{G0}}{\phi_T})$ NOTE_2 (1.6)

$V_{GO} = \frac{E_{g(Si)}}{q}$ (1.7)

B is a temperature-independent constant

A_E is the base-emitter junction area

$E_{g(Si)}$ is the band gap energy of Silicon

So, $\frac{\partial}{\partial T} V_{BE2} = \frac{1}{T} \Phi_T \ln(I_{R2} / I_S) - \Phi_T \frac{\partial}{\partial T} (\ln(BA_E) + 3 \ln T - \frac{V_{G0}}{\phi_T})$

$$= \frac{1}{T} V_{BE2} - \Phi_T \times 3 \frac{1}{T} - \frac{V_{G0}}{T} \quad (1.8)$$

Step 3 Substituting (1.4) and (1.8) into (1.3) gives

$$\frac{\partial}{\partial T} V_{REF} = M \frac{\partial}{\partial T} \Phi_T \Big|_{T_0} + \frac{\partial}{\partial T} V_{BE2} \Big|_{T_0}$$

$$= M \frac{1}{T_0} \Phi_{T_0} + \frac{1}{T_0} V_{BE2} - \Phi_T \times \frac{3}{T_0} - \frac{V_{G0}}{T_0} = 0 \qquad (1.9)$$

We derive $M\Phi_{T_0} = 3\Phi_{T_0} + V_{G0} - V_{BE2}$ (1.10)

So, $M = 3 + (V_{G0} - V_{BE2} \Big|_{T_0}) / \Phi_{T_0}$ (1.11)

Step 4 Substituting M into (1.2) gives

$$V_{REF} = M\Phi_{T_0} + V_{BE2}$$

$$= (3\Phi_{T_0} + V_{G0} - V_{BE2}) + V_{BE2}$$

$$= 3\Phi_{T_0} + V_{G0} \qquad (1.12)$$

Finally, The bandgap voltage of silicon $V_{GO} = \frac{E_{g(Si)}}{q} = 1.205$ V

So that, $V_{REF} = 3 \times (25.6\text{ mV}) + 1.205\text{ V} = 1.282\text{V}$ (1.13)

Note_1:

We set $M = \ln \frac{R_2}{R_1} \times (\frac{R_2}{R_X} + 1)$ which is temperature – independent.

In fact, the individual resistances (R_1, R_2, R_X) will vary its value with temperature. But the ratio can keep nearly constant, that is,

$\frac{R2 + \Delta R2}{R1 + \Delta R1} \fallingdotseq \frac{R2}{R1}$ independent of temperature

Proof：

$$\Delta R2 = \frac{\partial R2}{\partial T}\Delta T \quad \text{and} \quad \Delta R1 = \frac{\partial R1}{\partial T}\Delta T \tag{1.14}$$

$$\frac{R2 + \Delta R2}{R1 + \Delta R1} = \frac{R2 + \frac{\partial R2}{\partial T}\Delta T}{R1 + \frac{\partial R1}{\partial T}\Delta T} = \frac{R2(1 + \frac{1}{R2} \times \frac{\partial R2}{\partial T}\Delta T)}{R1(1 + \frac{1}{R1} \times \frac{\partial R1}{\partial T}\Delta T)} \tag{1.15}$$

$$\because \quad \frac{1}{R2} \times \frac{\partial R2}{\partial T}\Delta T \cong \frac{1}{R1} \times \frac{\partial R1}{\partial T}\Delta T$$

$$\therefore \quad \frac{R2 + \Delta R2}{R1 + \Delta R1} \fallingdotseq \frac{R2}{R1} \tag{1.16}$$

Similarly, $\frac{R2 + \Delta R2}{R_X + \Delta R_X} \fallingdotseq \frac{R_2}{R_X}$ when temperature change (1.17)

Note_2:

$$I_S = \frac{q \times A_E \times n_i^2 \times \overline{D_n}}{Q_B} = B' \times n_i^2 \times \overline{D_n} \quad (1.18)$$

Where n_i : intrinsic minority – carrier concentration

Q_B : the total base doping density per unit area

A_E : emitter – base junction area

B' : temperature – independent constant

By Einstein equation : $\mu_n = \frac{q}{KT} \times \overline{D_n}$, $\overline{D_n} = \Phi_T \times \mu_n$ (1.19)

$$\therefore I_S = B' \times n_i^2 \times (\mu_n \phi_T) = B' \times \frac{K}{q} \times n_i^2 \times T \times \mu_n \quad (1.20)$$

Set $I_S = B'' \times n_i^2 \times T \times \mu_n$

Known $\mu_n = CT^{-n}$, C is a temperature – independent constant

$n_i^2 = DT^3 \exp(-\frac{V_{G0}}{\phi_T})$, D is a temp. – independent constant

Finally, we assume n = 1 and get

$$I_S = B'' \times DT^3 \exp(-\frac{V_{G0}}{\phi_T}) \times T \times CT^{-1}$$

$$= B \times A_E \times T^3 \times \exp(-\frac{V_{G0}}{\phi_T}) \quad (1.21)$$

1.2.2.2 Recently Proposed Bandgap Circuit

According to the previous analysis, If the power supply voltage is lower than 1.28V, the conventional bandgap reference circuit cannot be used.

In order to meet the demand that power supply voltage is lower than 1.3V, one solution was proposed by using current-mode structures and low operating voltage of OP-Amplifiers to achieve the low voltage (V_{DD} ≤ 1.0V) bandgap reference circuit as shown in Fig. 1-2 and described below [8].

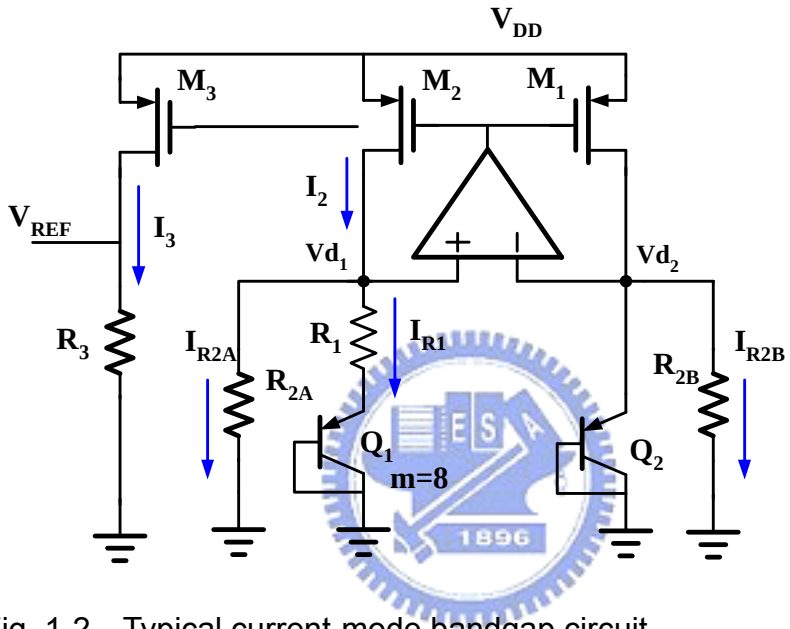


Fig. 1-2 Typical current-mode bandgap circuit

$$\because I_3 = I_2 = I_{R2A} + I_{R1} \text{ and } R_{2A} = R_{2B}$$
$$\text{then, we can derive } I_{R2A} = I_{R2B}$$

$$\begin{aligned}
\therefore V_{REF} &= I_3 R_3 \\
&= (I_{R2A} + I_{R1}) R_3 \\
&= (I_{R2B} + I_{R1}) R_3 \\
&= \left(\frac{V_{EB2}}{R_{2B}} + \frac{V_{EB2} - V_{EB1}}{R_1}\right) R_3 \\
&= V_{EB2} \frac{R_3}{R_{2B}} + \frac{R_3}{R_1} (\ln 8) \phi_T
\end{aligned}$$

Fig. 1-2 shows a typical current-mode BGR circuit topology. First, we set Vd1=Vd2 by utilizing the OPA negative feedback characteristic. Second, according to the BJT device physics, the circuit will create two currents, which are I_{R1} and I_{R2A}. The current I_{R1} will increase as the temperature increase, which is called the positive temperature coefficient. And the current I_{R2A} will decrease as the temperature increase, which is called the negative temperature coefficient. Theoretically, these two currents (I_{R1} and I_{R2A}) will compensate to each other. So we can get a new stable current which is independent of temperature by adding these two currents (I_{R1} and I_{R2A}). Finally, making the new stable current (I_3) pass through a resistor can produce the so-called reference voltage.

According to the theory, it is possible to achieve 0.7V reference with 1.0V power supply voltage and a well-controlled temperature behavior.

However, the OP-Amplifier is the most critical block. The supply voltage used must ensure correct operation of the operational amplifier and, indeed, it is the true limit of the circuit.

So, how to design a good OP-Amplifier is an important issue and the detail will be presented in chapter 2 and chapter 4.

1.3 Review on CMOS Bandgap Reference Circuits (II)

There are several kinds of bandgap reference circuits. In this section, we will introduce and discuss the most representative circuits from the conventional one to the recently proposed ones. We can roughly classify the BGR circuits into two categories, the sum of voltage (Class-A) ; the sum of currents (Class-B).

1.3.1 The Class-A of Bandgap Circuit (The Sum of Voltage)

Case1: [5]

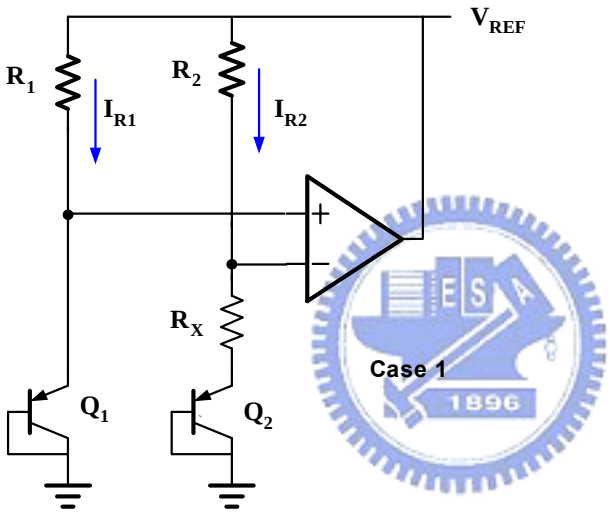
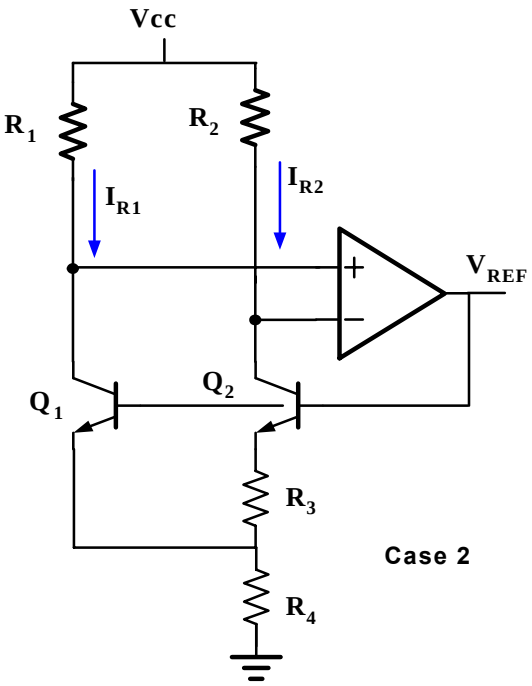


Fig. 1-3 The case1 bandgap circuit with V_{DD} > 1.0V and V_{REF} > 1.0V

$$
\begin{aligned}
V_{REF} &= I_{R1}R_1 + V_{EB1} \\
&= I_{R2}R_2 + V_{EB1} \\
&= \frac{V_{EB1} - V_{EB2}}{R_X} R_2 + V_{EB1} \\
&= \frac{R_2}{R_X} \ln\left(\frac{R_2}{R_1}\right)\phi_T + V_{EB1}
\end{aligned}
$$

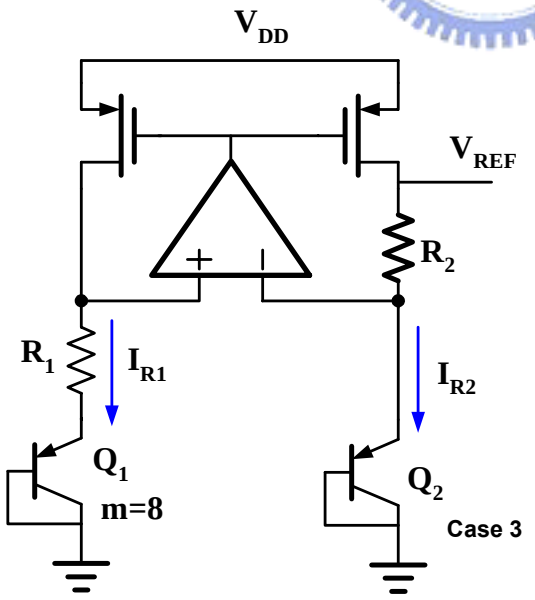
Case2 : [6]



$$V_{REF} = (I_{R1} + I_{R2})R_4 + V_{BE1}$$
$$= I_{R2}(\frac{I_{R1}}{I_{R2}} + 1)R_4 + V_{BE1}$$
$$= (\frac{V_{BE1} - V_{BE2}}{R_3})(\frac{R_2}{R_1} + 1)R_4 + V_{BE1}$$
$$= (\frac{R_2}{R_1} + 1)\frac{R_4}{R_3}\ln(\frac{R_2}{R_1})\phi_T + V_{BE1}$$

Fig. 1-4 The case2 band-gap circuit with V_{DD} > 1.0V and V_{REF} > 1.0V

Case3 : [7]



$$V_{REF} = I_{R2}R_2 + V_{EB2}$$
$$= \frac{V_{BE2} - V_{BE1}}{R_1}R_2 + V_{EB2}$$
$$= \frac{R_2}{R_1}(\ln\frac{I_{R2}}{I_{R2}/8})\phi_T + V_{EB2}$$
$$= \frac{R_2}{R_1}(\ln 8)\phi_T + V_{EB2}$$

Fig. 1-5 The case3 Band-gap circuit with V_{DD} > 1.0V and V_{REF} > 1.0V

1.3.2 The Class-B of Bandgap Circuit (The Sum of Current)

Case4 : [8]

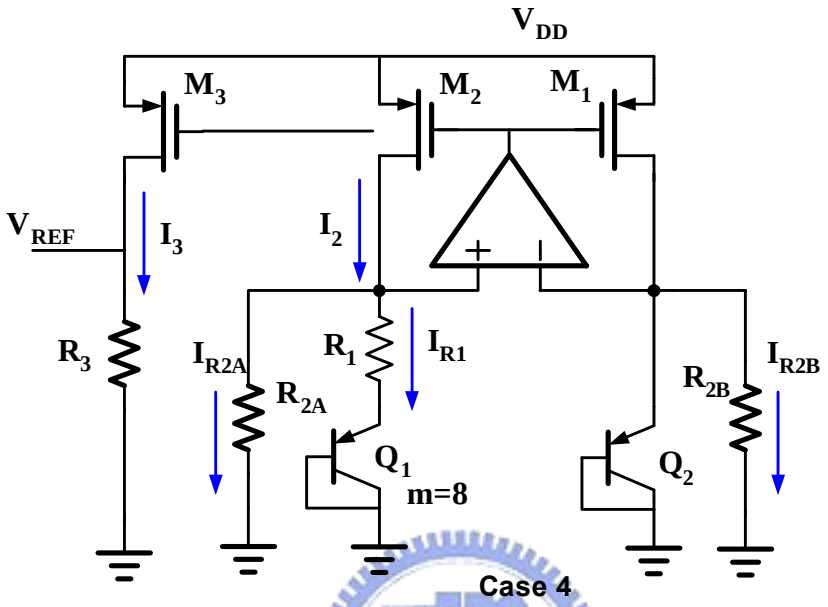


Fig. 1-6 The case4 bandgap circuit with V_{DD} ≤ 1.0V and V_{REF} < 1.0V

$$\because I_3 = I_2 = I_{R2A} + I_{R1} \quad and \quad R_{2A} = R_{2B}$$

$$\text{We derive} \quad I_{R2A} = I_{R2B}$$

$$\therefore V_{REF} = I_3 R_3$$

$$= (I_{R2A} + I_{R1}) R_3$$

$$= (I_{R2B} + I_{R1}) R_3$$

$$= \left(\frac{V_{EB2}}{R_{2B}} + \frac{V_{EB2} - V_{EB1}}{R_1}\right) R_3$$

$$= V_{EB2} \frac{R_3}{R_{2B}} + \frac{R_3}{R_1} (\ln 8) \phi_T$$

Case5 : [3]

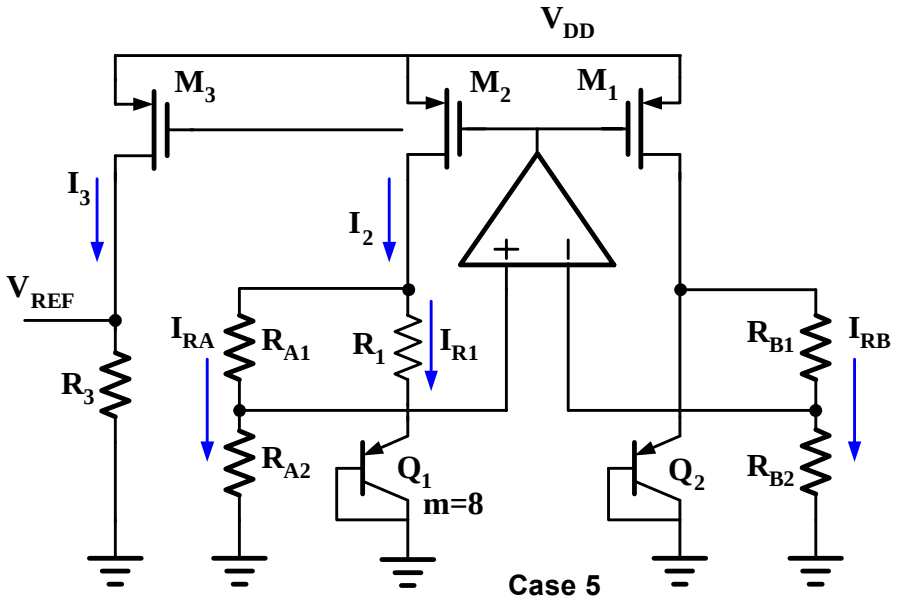


Fig. 1-7 The case5 bandgap circuit with $V_{DD} \leq 1.0V$ and $V_{REF} < 1.0V$

$$\because I_3 = I_2 = I_{RA} + I_{R1} \text{ and } R_{A1} = R_{B1},\ R_{A2} = R_{B2}$$

We derive $I_{RA} = I_{RB}$

$$\therefore V_{REF} = I_3 R_3$$

$$= (I_{RA} + I_{R1}) R_3$$

$$= (I_{RB} + I_{R1}) R_3$$

$$= \left(\frac{V_{EB2}}{R_{B1} + R_{B2}} + \frac{V_{EB2} - V_{EB1}}{R_1}\right) R_3$$

$$= V_{EB2} \frac{R_3}{R_{B1} + R_{B2}} + \frac{R_3}{R_1} (\ln 8)\phi_T$$

Table-1 Classification of bandgap reference circuits

	Class A (the sum of voltages)	Class B (the sum of currents)
$V_{DD} > 1.0V$	case-1, case-2, case-3	Type C and Type D of this thesis (by TSMC 0.35μm)
$V_{DD} \leq 1.0V$		case4, case5, and Type A & Type B of this thesis (by TSMC 0.18μm)

1.4 Organization of This Thesis

This thesis is divided into six chapters. In Chapter 1, the background and motivation are presented and the representative bandgap circuits are classified and introduced. Furthermore, we construct a complete classification as shown in Table-1.

In Chapter 2, Type A and Type B bandgap circuits based on the class B topology implemented by TSMC 0.18μm CMOS process was proposed. The design consideration is discussed in section 2.1. Then the design concepts including V_{REF} and PSRR are presented in sections 2.2 and 2.3. The circuit realization is described in section 2.4.

In chapter 3, the circuits layout based on TSMC 0.18μm CMOS process is presented. The chip testing result and comparison with simulation are shown in the following subsections.

In Chapter 4, we improve the circuits topology proposed on chapter 2, to create two new types of bandgap circuits, which are named as Type C and Type D. The new topology ensures that the circuits can meet all process corners. The organization of chapter 4 is the same as chapter 2. The design consideration is discussed in section 4.1. Then the design concept is presented in section 4.2. The circuit realization is detailed in section 4.3.

In chapter 5, the circuits' layout based on TSMC 0.35μm CMOS process is presented. The chip testing result and comparison with simulation are shown in the following subsections.

In chap 6, conclusion and future work are given.

Chapter 2 DESIGN OF LOW VOLTAGE HIGH PSRR BANDGAP REFERENCE CIRCUIT WITH TSMC 0.18μm CMOS PROCESS

2.1 Design Motivation

Until now, most OPAs in the bandgap circuits use pMOS as the differential pair because the conventional bandgap circuit topology limit the common mode voltage of OPA. For example, if we use nMOS as the OPA's input stage then the input common-mode voltage of the OP-Amplifier must meet the following condition, as shown in Fig. 2-1 [3] :

$V_{COMM} = Vthn + 2V_{DS(sat)} < V_{EB(ON)} \fallingdotseq 650mV$

The above condition implies that Vthn < 550mV is required (assuming $V_{DS(sat)}$ = 50mV). This requirement can be satisfied in many technologies, but it is only for TT (Typical – Typical) process. However, considering the other process corner (e.g. SS and SF), the above requirement cannot be easily satisfied. Take TSMC 0.18μm 1P6M CMOS technology as an example:
Vthn = 440mV at Typical case, but Vthn = 540mV at slow corner (S).

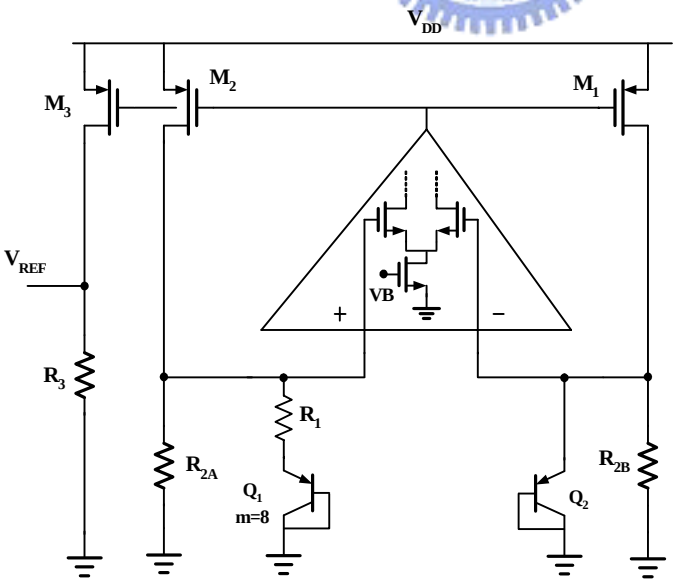


Fig. 2-1 Bandgap circuit that uses nMOS as input stage

Because of the circuit structure limitation as mentioned above, most bandgap circuits were implemented by using pMOS as the OPA's differential pair. But there are two disadvantages when using pMOS as the differential pair. One is the smaller voltage gain due to the smaller g_m for pMOS.

The other disadvantage is that the OPA's offset voltage will be multiplied by $\frac{R_3}{R_1}(1+\frac{R_{A2}}{R_{A1}})$ when using pMOS as the differential pair. By contrast, the OPA's offset voltage will only be multiplied by ($\frac{R_3}{R_1}$) if we use nMOS as the differential pairs [NOTE_3].

NOTE_3

Discuss the impact of the OPA's offset voltage on different bandgap circuit topology where Fig. 2-2 shows the pMOS as the OPA's input differential pair while Fig. 2-3 shows the nMOS as the OPA's input differential pair.

(A) Bandgap circuit that use pMOS as differential pair

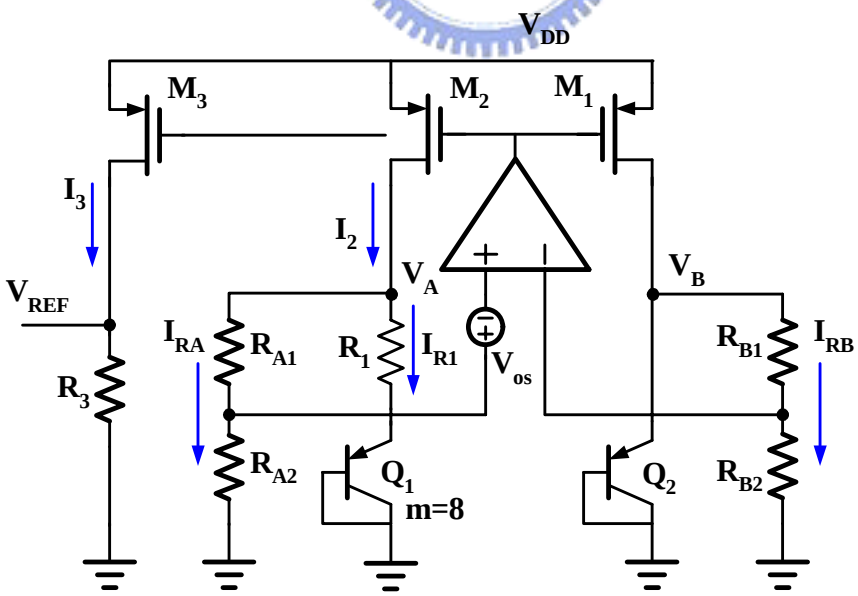


Fig. 2-2 Bandgap circuit that uses pMOS as differential pair

(1) $V_A(\frac{R_{A2}}{R_{A1}+R_{A2}}) - V_{os} = V_B(\frac{R_{B2}}{R_{B1}+R_{B2}})$

$\because V_A = I_{R1}R_1 + V_{EB1}$, $V_B = V_{EB2}$, $(\frac{R_{A2}}{R_{A1}+R_{A2}}) = (\frac{R_{B2}}{R_{B1}+R_{B2}})$

$\therefore (I_{R1}R_1 + V_{EB1})(\frac{R_{A2}}{R_{A1}+R_{A2}}) - V_{os} = V_{EB2}(\frac{R_{B2}}{R_{B1}+R_{B2}})$

We derive $(I_{R1}R_1 + V_{EB1}) - (\frac{R_{A1}+R_{A2}}{R_{A2}})V_{os} = V_{EB2}$

So $I_{R1}R_1 = V_{EB2} - V_{EB1} + (\frac{R_{A1}+R_{A2}}{R_{A2}})V_{os}$

Finally $I_{R1} = \frac{1}{R_1}(\phi_T \ln m) + \frac{1}{R_1}(\frac{R_{A1}+R_{A2}}{R_{A2}})V_{os}$ (2.1)

(2) $I_2 = I_{R1} + I_{RA}$ and $I_{RA} = I_{RB}$

$= I_{R1} + V_{EB2}(\frac{1}{R_{B1}+R_{B2}}) = I_{R3}$ (2.2)

(3) $V_{REF} = I_3R_3 = I_2R_3$

$= I_{R1}R_3 + V_{EB2}(\frac{R_3}{R_{B1}+R_{B2}})$

$= \frac{R_3}{R_1}(\phi_T \ln m) + \frac{R_3}{R_1}(1+\frac{R_{A2}}{R_{A1}})V_{os} + V_{EB2}(\frac{R_3}{R_{B1}+R_{B2}})$ (2.3)

(4) Substituting m = 8

$V_{REF} = \frac{R_3}{R_1}(\phi_T \ln 8) + \frac{R_3}{R_1}(1+\frac{R_{A2}}{R_{A1}})V_{os} + V_{EB2}(\frac{R_3}{R_{B1}+R_{B2}})$ (2.4)

(5) Unfortunately, V_{os} is not independent of temperature. Even worse, it will be multiplied by $\frac{R_3}{R_1}(1+\frac{R_{A2}}{R_{A1}})$, when using pMOS as differential pair.

(B) Bandgap circuit that use nMOS as differential pair

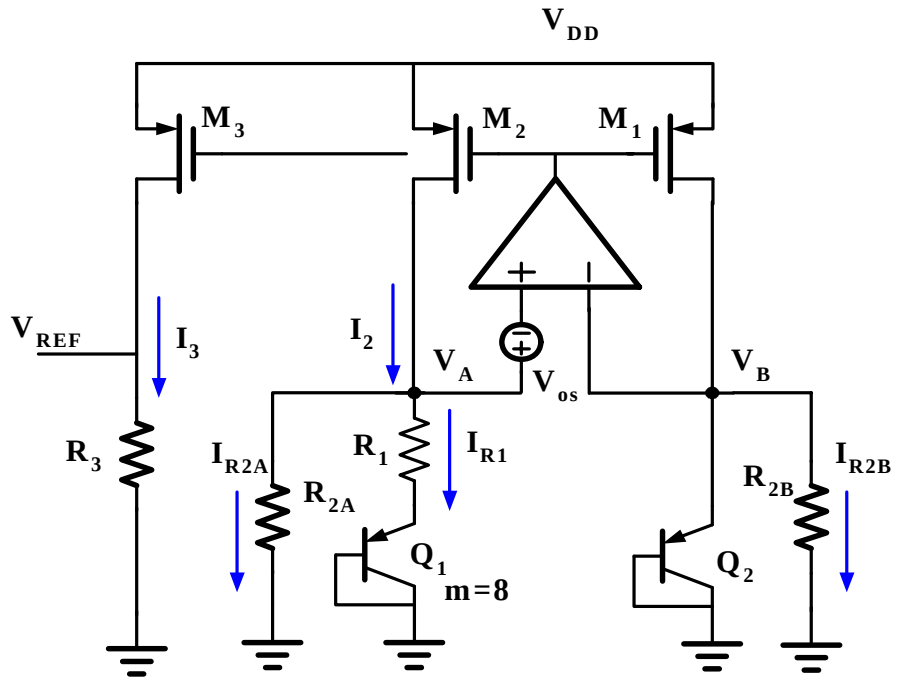


Fig. 2-3 Bandgap circuit that uses nMOS as differential pair

(1) $V_A - V_{os} = V_B$

$\because V_A = I_{R1}R_1 + V_{EB1}$, $V_B = V_{EB2}$

$\therefore (I_{R1}R_1 + V_{EB1}) - V_{os} = V_{EB2}$

We derive $I_{R1}R_1 = V_{EB2} - V_{EB1} + V_{os}$

So $I_{R1} = \frac{1}{R_1}(\phi_T \ln m) + \frac{1}{R_1}V_{os}$ (2.5)

(2) $I_2 = I_{R1} + I_{R2B}$ ($I_2 = I_{R1} + I_{R2A}$ and $I_{R2A} = I_{R2B}$)

$= I_{R1} + V_{EB2}(\frac{1}{R_{2B}})$ (2.6)

(3) $V_{REF} = I_3 R_3$

$= I_{R1}R_3 + V_{EB2}(\frac{R_3}{R_{2B}})$

$= \frac{R_3}{R_1}(\phi_T \ln m) + \frac{R_3}{R_1}V_{os} + V_{EB2}(\frac{R_3}{R_{2B}})$ (2.7)

(4) Substituting m = 8

$$V_{REF} = \frac{R_3}{R_1}(\phi_T \ln 8) + \frac{R_3}{R_1}V_{os} + V_{EB2}(\frac{R_3}{R_{2B}}) \qquad (2.8)$$

(5) Unfortunately, V_{os} is not independent of temperature. But, it will only be amplified by ($\frac{R_3}{R_1}$), when using nMOS as differential pair.

So, in this chapter, we modify the bandgap core circuit to break through the limitation on OPA when using nMOS as the differential pair. Hope to create a new kind of bandgap circuit in which the OPA's differential pair is composed of nMOS. In this way, the new topology of bandgap circuit will occupy less layout area but provide better performance than the existing topology using pMOS as the OPA's differential pair.

2.2 Bandgap Reference Circuit Design Concepts (I)

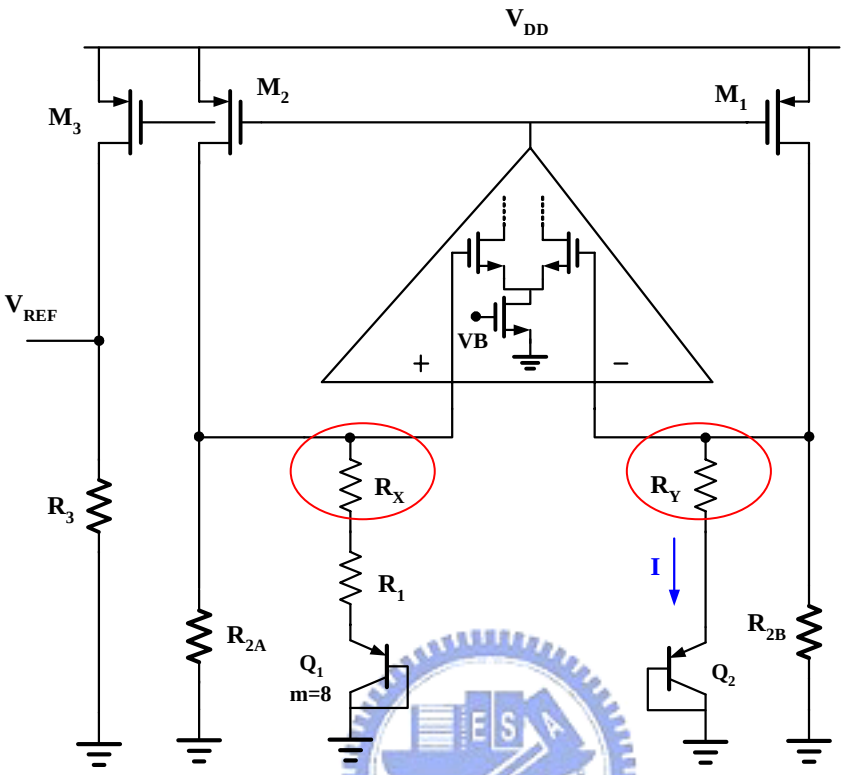


Fig. 2-4 Bandgap circuit inserting R_X, R_Y to upgrade common-mode voltage

As shown in Fig. 2-4, after inserting another resistor pair, R_X and R_Y, (as marked by red circle), the "the input common-mode voltage of the OP-Amplifier" is no longer restricted to the $V_{EB(ON)}$, That is

$$Vthn + 2V_{DS} < V_{EB(ON)} + I \times R_Y \fallingdotseq 750\ mV$$

So the bandgap core circuit will provide a common-mod voltage that is large enough to drive OPA's nMOS differential pair and keep it working in the saturation region. Finally the OPA will provide large voltage gain to drive the bandgap core circuit,

It is another feature in this thesis that the output reference voltage can reach 760 ~ 800 mV, which is higher than the others proposed by existing papers, as shown in Table-2.

Table-2 Comparison of low-voltage bandgap reference test chip

	This work Type A	This work Type B	This work Type C	This work Type D
Technology	0.18-μm CMOS	0.18-μm CMOS	0.35-μm CMOS	0.35-μm CMOS
Threshold Voltage	Vthp = -0.44V Vthn = +0.44V	Vthp = -0.44V Vthn =+0.44V	Vthp = -0.74V Vthn =+0.54V	Vthp = -0.74V Vthn = +0.54V
Min Vdd	1.10V	1.10V	1.30V	1.10V
Power Supply Range (工作電壓)	1.1 ~ 3.0V	1.1 ~ 3.0V	1.3 ~ 4.5V	1.1 ~ 4.5V
Max. Supply currets	38.1μA	34.4μA	54μA	41μA
Vref (參考電壓)	772mV	737mV	766mV	829mV
$TC_{F(eff)}$	140 ppm /℃ (-40 ~ 140℃)	149 ppm /℃ (-40 ~ 140℃)	90.2 ppm /℃ (-20 ~ 100℃)	34.1 ppm /℃ (-40~120℃)
PSRR for 1KHz	- 56dB	- 51dB	-18dB	-25dB
PSRR for 10KHz	- 29dB	- 33dB	-2.7dB	-10dB
PSRR for 100KHz	-15.2dB	-26dB	-0.1dB	-0.42dB
Size	0.192 mm^2	0.145 mm^2	0.294 mm^2	0.238 mm^2

	Ka Nang Leung [3]	J. Doyle et al. [2]	Neuteboom et.al [19]	Malcovati et al. [1]
Technology	AMS 0.6-μm CMOS	0.5-μm CMOS	0.8-μm CMOS	0.8-μm BiCMOS
Threshold Voltage	Vthp = -0.9V Vthn = +0.9V	N / A	Vthp = -0.7V Vthn = +0.5V	Vthp = -0.7V Vthn = +0.7V
Min Vdd	0.98V	0.95V	0.90V	0.95V
Power Supply Range (工作電壓)	0.98 ~ 1.5V	0.95 ~ 6.0V	N / A	0.95 ~ 2.0V
Max. Supply currets	18uA	10.0uA	N / A	< 92.0uA
Vref (參考電壓)	603mV	626mV	670mV	536mV
$TC_{F(eff)}$	15 ppm /℃ (0~100℃)	17 ppm /℃ (-40 ~ 125℃)	N / A	19 ppm /℃ (0~100℃)
PSRR for 1KHz	N / A	N / A	N / A	N / A
PSRR for 10KHz	- 44dB	N / A	N / A	N / A
PSRR for 10MHz	- 17dB	N / A	N / A	N / A
Size	0.24 mm^2	1.09 mm^2	N / A	N / A

From Table-2, the output reference voltage proposed in this thesis is 760 ~ 800mV, while the others is about 600 ~ 670mV. The reason is that HSPICE simulation suggests the best PSRR corresponding to Vref = Vd1 = Vd2 as shown in Fig. 2-5. Taking Fig. 2-5 with TSMC 0.18μm CMOS process as an example, the best PSRR performance occur at Vref = 675mV, marked by the red circle in the Table-3.

Table-3 Simulation result of PSRR at Vd1 = Vd2 = 670mV based on TSMC 0.18μm CMOS process

R3	70k	80k	90k	100k	110k	120k	130k
Vref	473mV	540mV	607mV	675mV	742mV	808mV	874mV
PSRR(DC)	-60dB	-61dB	-64dB	-84dB	-56dB	-45.8dB	-36.2dB
PSRR(10kHz)	-60dB	-61dB	-64dB	-84dB	-56dB	-45.8dB	-36.2dB

Note：PSRR = 20 log ($\frac{\Delta Vref}{\Delta Vdd}$)

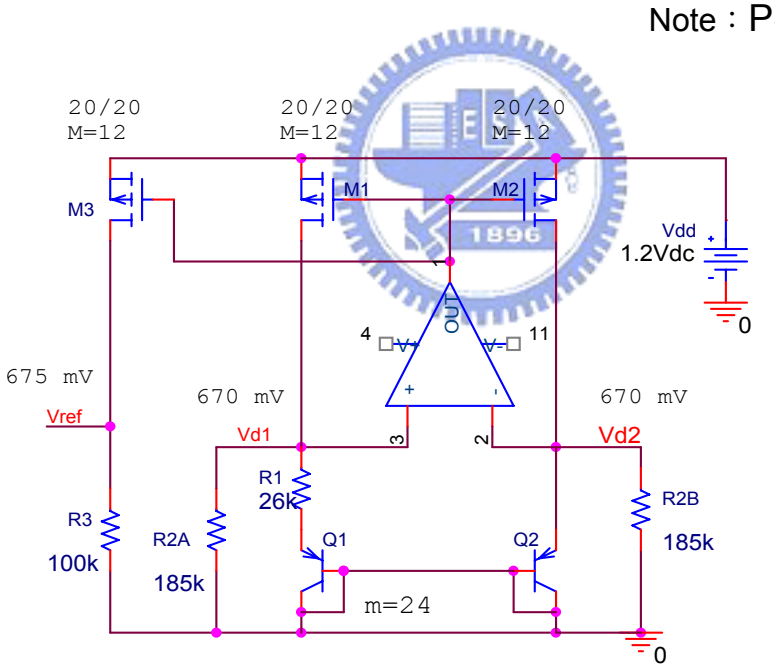


Fig. 2-5 Conventional BGR circuit topology

However, Vref = 675mV cannot meet the industrial requirement. For IC design industry, the Vref should be 750mV ~ 800mV. But, if we increase the reference voltage to 750mV by only adjusting the resistor R3 value, the PSRR performance will degrade rapidly, as shown in Table-3.

Now, by inserting resistor pairs, R_X and R_Y, we get another advantage : increase Vd1 and Vd2 voltage to 760mV. In this manner, the PSRR is optimal corresponding to Vref = Vd1 = Vd2 = 760mV, as shown in Fig. 2-6 and Table-4.

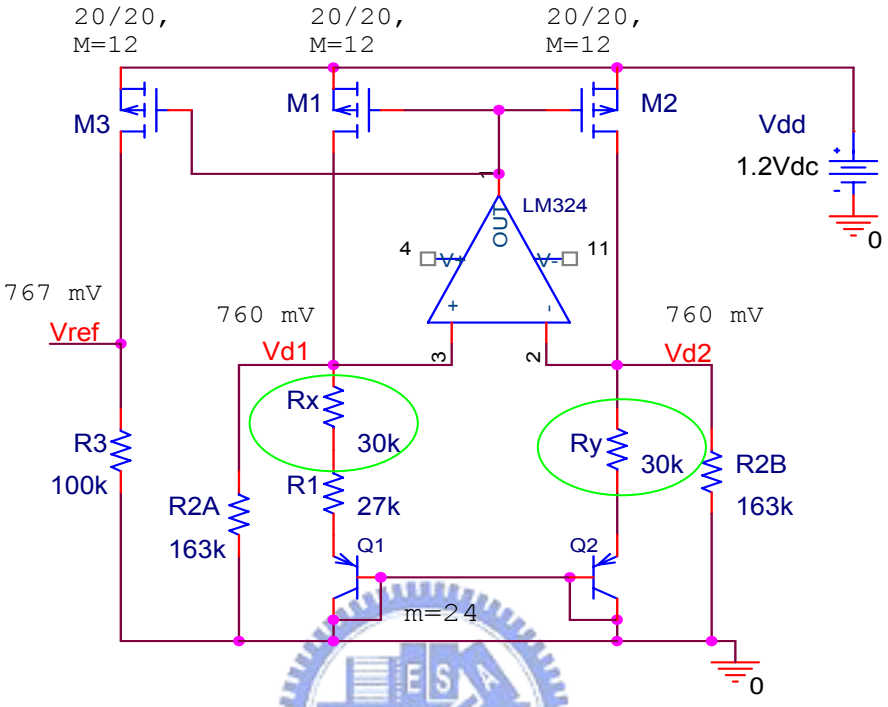


Fig. 2-6 Modified BGR circuit topology proposed in this thesis

Table-4 Simulation result of PSRR at Vd1 = Vd2 = 760mV based on TSMC 0.18μm CMOS process, known Vd1 = Vd2 = 760mV

R3	80k	90k	100k	110k	120k	130k
Vref	540mV	607mV	767mV	742mV	808mV	874mV
PSRR(DC)	-61dB	-64dB	-69dB	-56dB	-45.8dB	-36.2dB
PSRR(10kHz)	-61dB	-64dB	-69dB	-56dB	-45.8dB	-36.2dB

In this thesis，we provide Vref ≒ 735 ~ 800 mV, which is higher than the output reference voltages provided by other papers, i.e. around 600mV, and much more meet the industrial requirement. Besides, we can keep the PSRR at the optimal state and maintain a well-controlled temperature compensation performance as shown in the Table-2.

2.3 Bandgap Reference Circuit Design Concepts (II)

The preceding description is based on the simulation result. In order to get more conviction, we try to formulate the simulation result by using MOS small signal model and equivalent circuit to analyze.

(1) For simplification, we only analyze the mechanism of the PSRR of M3, as marked by the circle shown in the Fig. 2-6.

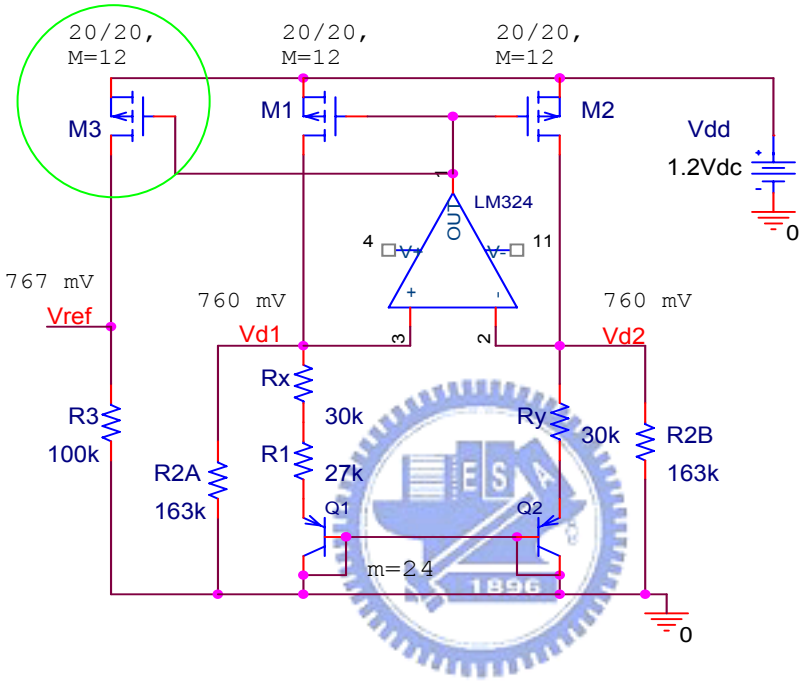


Fig. 2-6 Modified BGR circuit topology proposed in this thesis

(2) Set up the equivalent circuit of pMOS M3 for analyzing the mechanism of the PSRR as shown in Fig. 2-7.

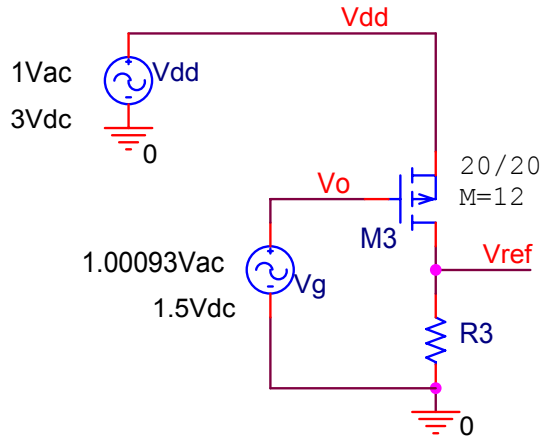


Fig. 2-7 Analysis of the single pMOS device (M3) for PSRR study

The small signal model as shown in Fig. 2-8：

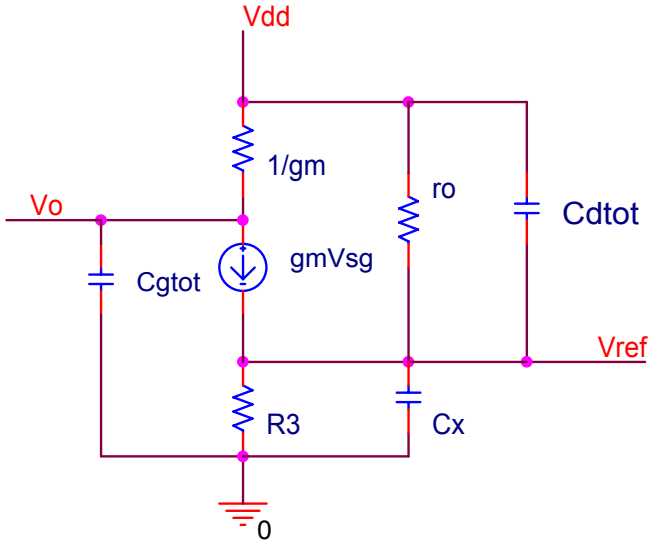


Fig. 2-8　Small signal model analysis of pMOS device (M3) for PSRR study

The PSRR formula can be derived as follow：

$$\frac{Vref}{Vdd} = g_m R_3 \left(1 - \frac{Vo}{Vdd}\right)\left(\frac{1}{1 + sR_3C_{dtot}}\right) + K\left(\frac{s + W_Z}{s + W_P}\right)$$

$$= g_m R_3 \left(1 - \frac{Vo}{Vdd}\right)\left(\frac{1}{1 + sR_3C_{dtot}}\right) + \frac{C_{dtot}}{C_{dtot} + C_X}\left(\frac{s + W_Z}{s + W_P}\right)$$

Where　$W_z = (1 / r_o C_{dtot})$，　$W_p = [\, 1 / (r_o \| R_3)\,(C_{dtot} + C_X)\,]$，　$C_{dtot} >> C_X$

And　　C_X is negligible

From Table-4, we know that PSRR will be at the optimal state when Vd1 = Vd2 = 760mV.

We now analyze the device parameter based on different bandgap reference voltage (Vref) as shown in Table-5.

Table-5 Simulation result of the different bandgap reference voltage based on TSMC 0.18μm CMOS process

R3	70k	80k	100k	110k	130k
Vref	538mV	540mV	767mV	742mV	874mV
I_d	7.68uA	6.75uA	7.67uA	6.74uA	6.72uA
g_m	92.9u	85.6u	92.7u	85.5u	85.2u
V_{ds}	661mV	659mV	432m	458mV	325mV
g_{ds}	61.6n	55.48n	103n	81.0n	187n
r_o	16.2M	18.02M	9.70M	12.3M	5.34M
ΔVref / ΔVdd	-2.69m	-873.5u	334u	1.60m	15.4m
Vo / Vdd	1.0010799	1.0007751	1.0010799	1.0007751	1.0007751
PSRR (DC)	-51.3dB	-61dB	-69.5dB	-55.9dB	-36.2dB
C_{dtot}	295f	295.8f	309f	308f	317f
C_{gtot}	27.3p	26.9p	27.3p	26.9p	26.9p
C_{stot}	31.8p	31.08p	31.8p	31.08p	31.08p
C_{btot}	11.1p	11.12p	11.1p	11.12p	11.12p
C_{gs}	23.5p	22.95p	23.5p	22.95p	22.95p
C_{gd}	78.6f	78.60f	78.6f	78.60f	78.60f
Wp(rad/sec)	-48.5M	-42.44M	-32.6M	-29.7M	-24.7M
Wz(rad/sec)	-2.69M	-1.37M	-6.35M	-3.00M	-7.88M

For hand calculation：

R3 = 70k

$$\frac{Vref}{Vdd} = g_m R_3 (1 - \frac{Vo}{Vdd}) + (\frac{R_3}{r_o + R_3}) = 92.9u * 70k(1-1.0010799) + \frac{70k}{16.2M + 70K}$$

= - 0.0070225 + 0.0043023

= - 0.00272 = - 2.72m

$$\text{PSRR for DC} = \left|\frac{Vref}{Vdd}\right|_{dB} = 20 \log (2.72m) = -51.3dB \text{ (S：- 51.4dB)}$$

And the frequency of dominant pole

$Wp = [\ 1 / (r_o || R_d)(\ C_{dtot} + C_X)\ ] = 1 / (\ 70k \times 295f\ ) = -48.42$ M rad /sec

Good match with the simulation, Wp = - 48.5M rad/ sec

(1) R3 = 100k

$$\frac{Vref}{Vdd} = g_m R_3 \left(1-\frac{Vo}{Vdd}\right)+\left(\frac{R_3}{r_o+R_3}\right)$$

$$= 92.7u * 100k(1-1.0010799) + \frac{100k}{9.7M+100K}$$

$$= - 0.0100106 + 0.010204$$

$$= 0.0001934$$

$$= 193.4u$$

PSRR for DC = $\left|\frac{Vref}{Vdd}\right|_{dB}$ = 20 log (193.4u) = - 74.26dB (S：- 69.5dB)

Good match with the simulation , PSRR = - 69.5 dB

(3) R3 = 130k

$$\frac{Vref}{Vdd} = 85.2u \times 130k\,(1-1.0007751) + \frac{130k}{5.34M+130K}$$

$$= - 0.008585 + 0.0237659$$

$$= 0.0151809$$

$$= 15.18m$$

PSRR for DC = $\left|\frac{Vref}{Vdd}\right|_{dB}$ = 20 log (15.18m) = - 36.37dB (S：- 36.2dB)

Good match with the simulation , PSRR = - 36.2 dB

Conclusion：

From the derived formulas, we see that PSRR is composed of two terms. The first term is always a negative value, while the second term is always a positive value. When Vd1 = Vd2, the first term and the second term cancel each other. That behavior makes the PSRR approach to minimum value, that is, best performance. So, the theoretical analysis of MOS small signal equivalent circuit can prove the simulation result.

2.4 Circuit Implementation

In chapter two, there are two types of BGR circuits. The bandgap core circuits are the same, as shown previously, but the OP-Amplifiers are different. The first circuit (a conventional one) named as Type A uses pMOS as the input stage, as shown in Fig. 2-9, while the second circuit celled as Type B uses nMOS as the input stage, as shown in Fig. 2-10.

Here, one important thing we want to mention is that in conventional BGR circuits, the emitter area ratio of BJT Q1 and Q2 is usually 8：1. So, the $\triangle V_{BE}$ is about 50mV in the conventional BGR circuits.

Note：$\triangle V_{BE} = \Phi_T * \ln(m) = 26mV * \ln(8) = 54.06mV$

But, According to reference paper [2]：

“ A large$\triangle V_{BE}$ can reduces the effect of amplifier input offset ”。

And this conclusion can be verified by the formulas (2.3) or (2.7).

So, in this thesis, we put the emitter area ratio of BJT Q1 and Q2 to 24：1. In this way, the $\triangle V_{BE}$ is increased to around 80mV。

Finally, the simulated features of the two types of OP-Amplifier are summarized in Table-6.

Table-6 Operational Amplifier features of Type A and Type B

	Type A pMOS as the input stage	Type B nMOS as the input stage
DC Loop gain	65 dB	70 dB
Gain-Bandwidth product	6.5 MHz	10.5 MHz
Phase Margin	51.8°	80.1°
Supply Voltage	1.10 V	1.10 V

Here below is the complete circuit topology of Type A and Type B

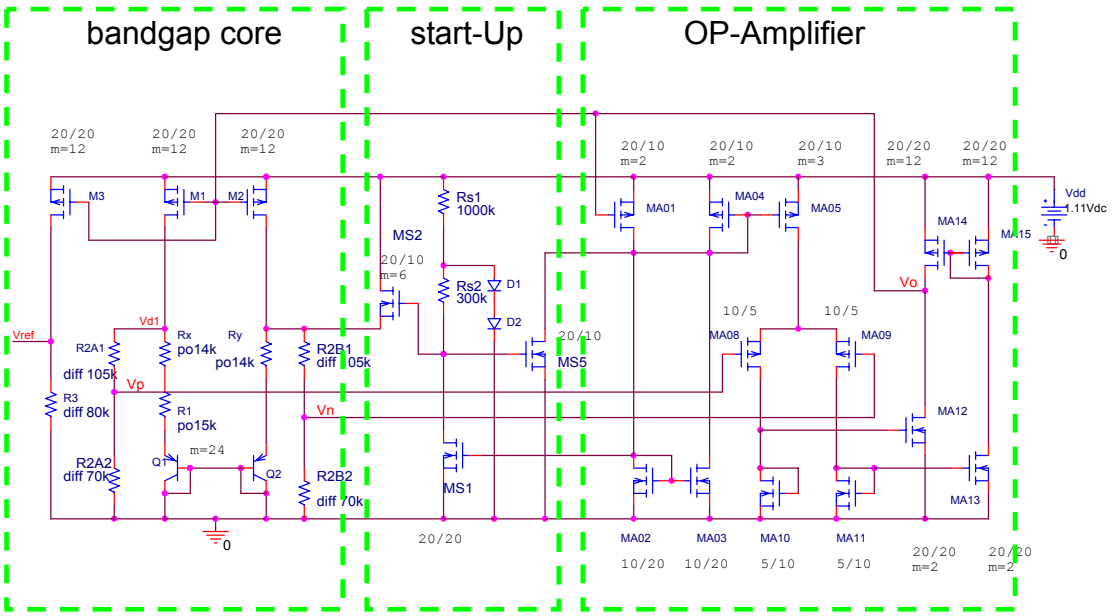


Fig. 2-9 The complete bandgap circuit topology of Type A (bandgap core + start-Up + OP-Amplifier with pMOS input stage)

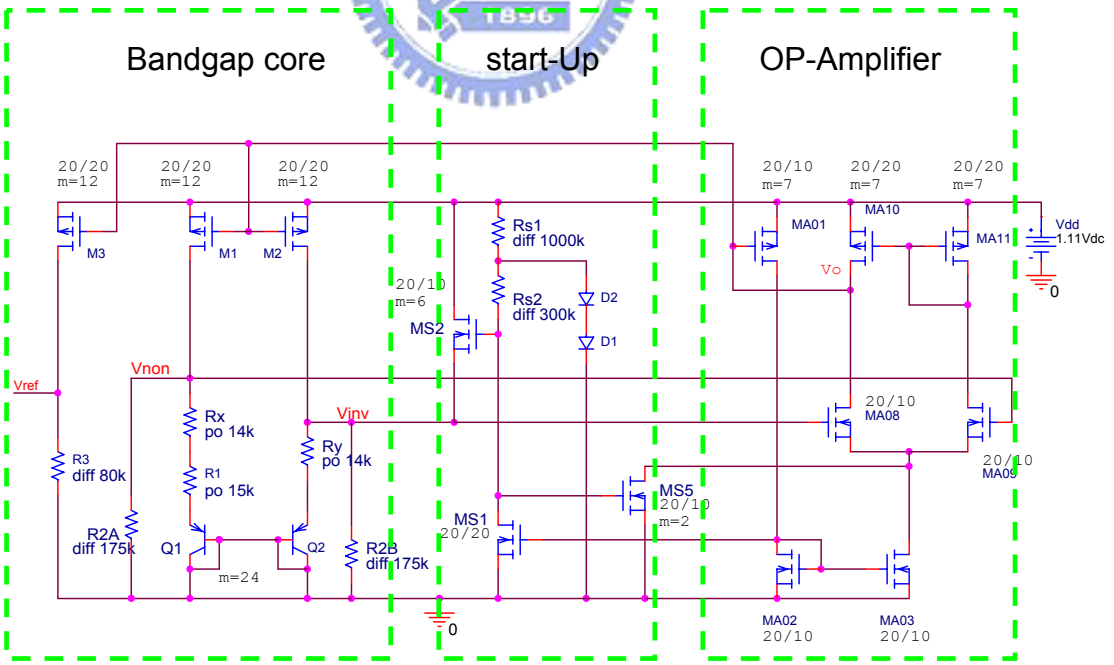


Fig. 2-10 The complete bandgap circuit topology of Type B (bandgap core + start-Up + OP-Amplifier with nMOS input stage)

Chapter 3 CHIP LAYOUT DESCRIPTION AND EXPERIMENTAL RESULTS WITH TSMC 0.18μm CMOS PROCESS

3.1 Chip Layout Descriptions

The test chip is designed and fabricated by TSMC 0.18μm single-poly-six-metal (1P6M) CMOS technology. Fig. 3-1 shows the overall die photo of the Type A and Type B, which include the bandgap core circuit and OP-Amplifier. The chip area is 0.192 mm^2 for Type A and 0.145 mm^2 for Type B. The transistors used are totally 21 for Type A, 15 for Type B.

The bandgap core circuit in Fig. 3-1 consists of the startup circuits, bipolar transistors, bias resistors, and the MOS transistors that provide the current through the bias resistors and the BJT group (Q_1 & Q_2), respectively. Since the mismatching of the MOS transistors in the differential pair will make the current different, the same size MOS transistors are placed as close as possible to minimize this kind of mismatching.

The most important devices in the bandgap circuit are the bipolar transistors with large thermal coefficient. The parasitic vertical PNP BJTs are used in this test chip. The layout should be arranged carefully to ensure matching and accurate ratio of these BJTs. Thus, we choose the ratio of the emitter area of Q_1 and that of Q_2 to be 24, and arrange the 24 Q_1s to circulate the single Q_2. The reason why we choose the ratio to be 24 has been explained in the section 2.4. The total emitter area of Q_1 is 2400um^2 and that of Q_2 is 100 um^2 in this layout. This arrangement not only reduces the mismatching of these bipolar transistors, but also makes the temperature coefficient of these bipolar transistors as close as possible

.

The accuracy of the resistance value on the chip is the most difficult job to realize in the process. Hence, the output reference voltage is designed to be dependent on the ratio instead of absolute value. Besides, a unit dimension of the resistors is defined, and all the resistors are series-connected by the unit resistors in order to reduce the mismatching of the resistors arising process non-uniformity.

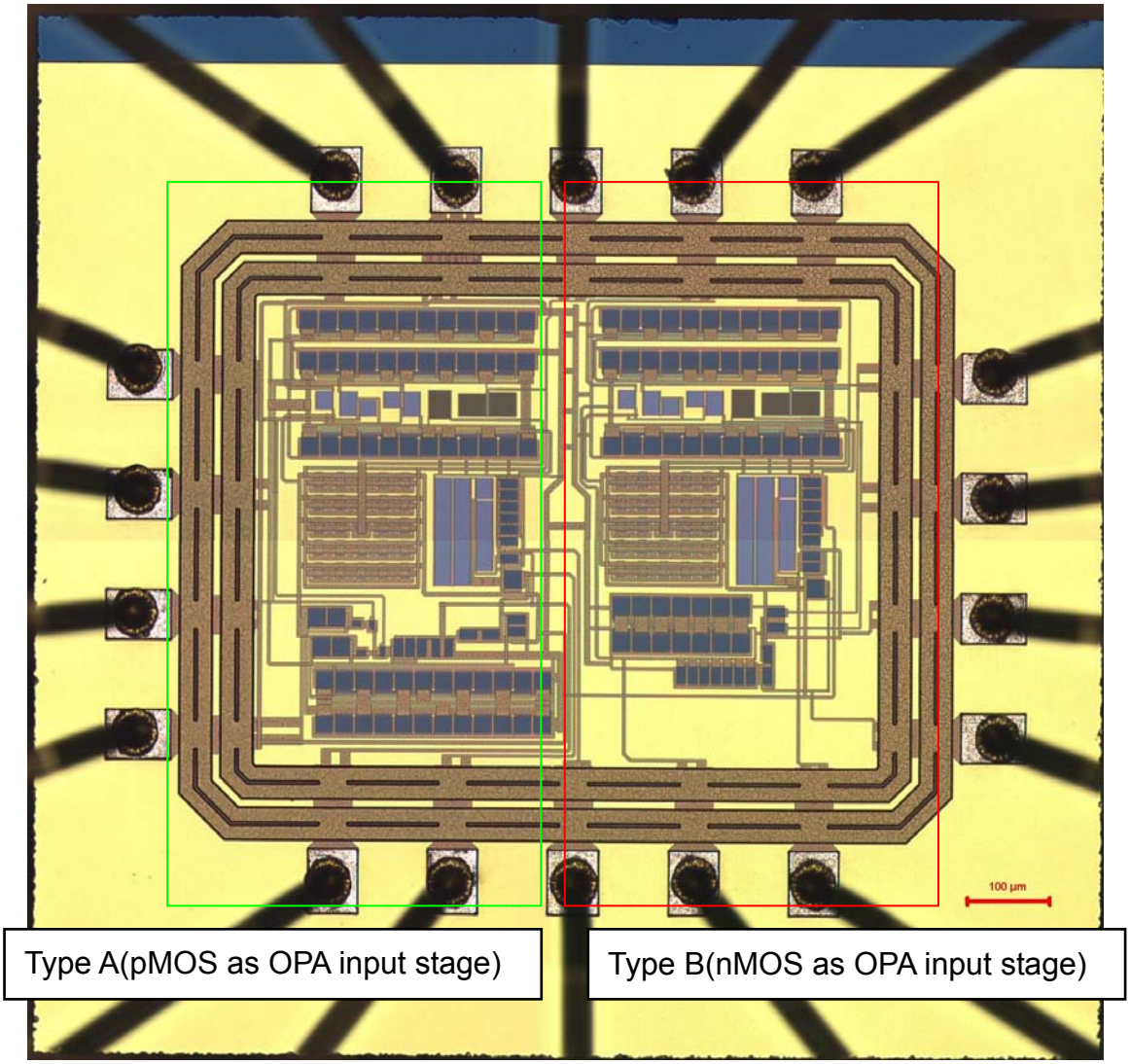


Fig. 3-1 The overall die photo of the Type A and Type B

Note：In this test chip, a set of I/O PAD library developed by ITRI (Industrial Technology Research Institute) was chosen to use. The detailed library name is “STC Pure 1.8V Linear I/O Library in 0.18µm CMOS process, version 1.0”

3.2 Measurement Setup

(1) The set up required to measure “Vref (Reference Voltage) vs. Vdd ” are power supply and voltage meter.

(2) The set up required to measure “Transient Response curve” are power supply, function generator, and Oscilloscope。Fig. 3-2 shows an example of measured transient response for Type B (nMOS as OPA’s input stage) where the output voltage of the function generator is set up from 1.3V to 2.3V。

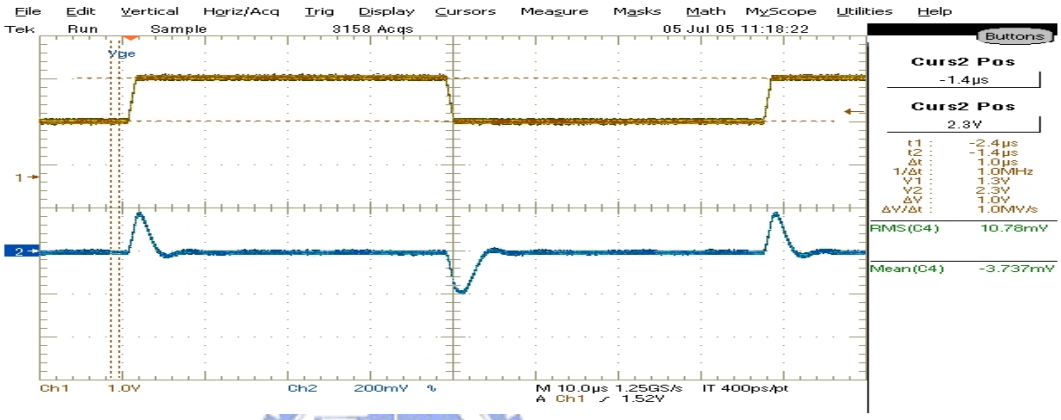


Fig. 3-2 Typical transient response curve

(3) The PSRR for high freq. (from 50KHz to 10MHz) can be calculated by the output waveform as shown in Fig. 3-3, which was produced by using the power supply、Function generator and Oscilloscope.

Fig. 3-3 shows the PSRR of Vref at freq. = 50KHz, where the input supply voltage is a Sin Wave (amplitude = 131mV). And the output reference voltage is also a Sin Wave (amplitude= 121mV).

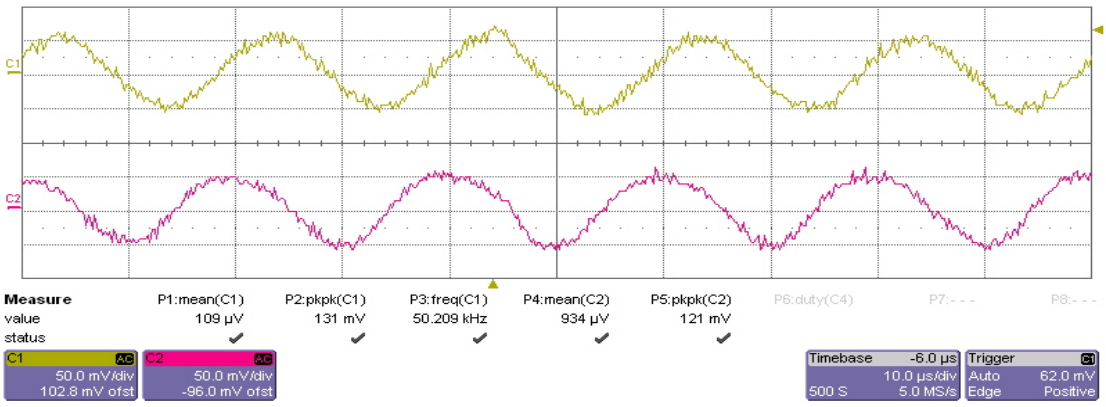


Fig. 3-3 PSRR of n-Vref at freq. = 50KHz at AC mode

Calculation：

Take Fig. 3-3 as an example, in which frequency = 50KHz；

The variation of input power supply voltage is 131mV and the resulted variation of output reference voltage is 121mV.

Based on the definition of PSRR we can get

$$\text{PSRR} = 20\log\left(\frac{\Delta Vref}{\Delta Vdd}\right) = 20\log\left(\frac{121mV}{131mV}\right) = -0.68 \text{ dB at freq.} = 50\text{KHz}$$

(4) As for the measurement set up for PSRR at low frequency (from 100Hz to 50kHz), a network analyzer, power supply and a high gain OP-Amplifier are used. The measurement setup is shown in Fig. 3-4.

where PSRR = S_{21} = $\frac{V_{port\_B}}{V_{port\_R}}$

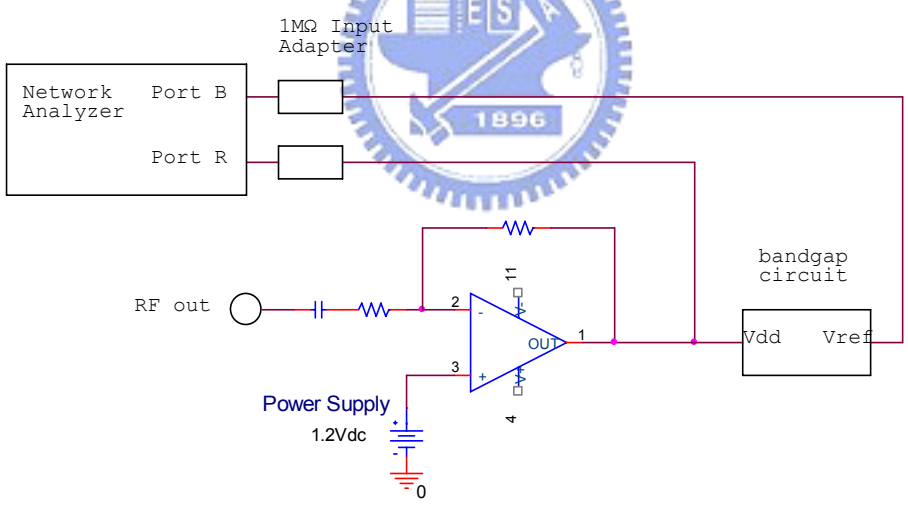


Fig. 3-4 The measurement setup for low frequency PSRR test

(5) The measurement of “Temperature Compensation Curve ” is done by the Precision Temperature Forcing System (T-2800). The test chip was put into the chamber, and the temperature was set from -40℃ to 150℃, to measure the output Reference. The temperature was increased by each step of 5℃, to collect the temperature compensation curve and calculate the corresponding temperature coefficient, $TC_{F(eff)}$.

3.3 Experimental Results

3.3.1 Experimental Results of Type A (pMOS as OPA input stage)

PART (I) Vref (Reference Voltage) vs. Vdd

(1) Measured Result of Type A

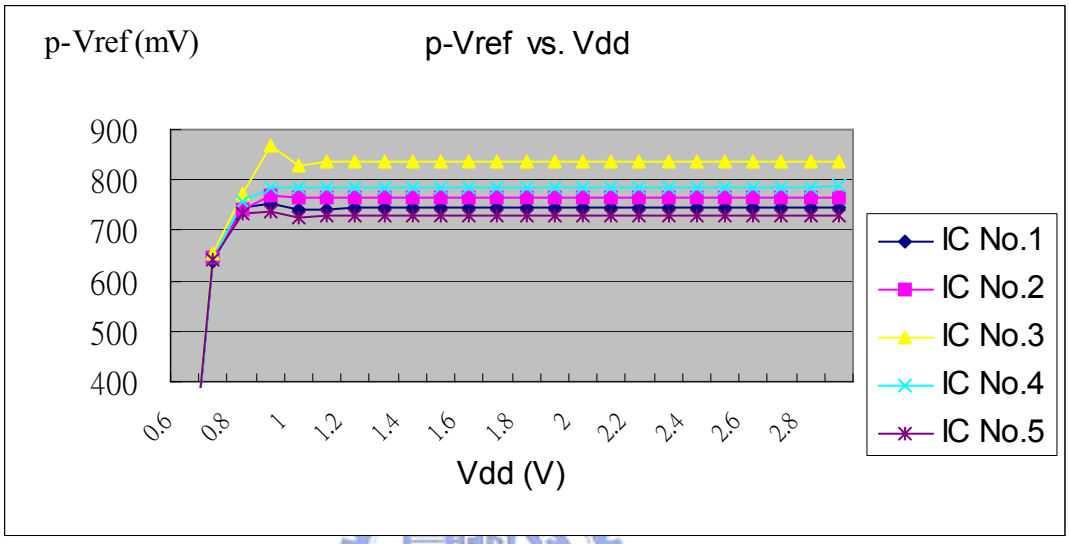


Fig. 3-5 Measured p-Vref vs. Vdd of Type A

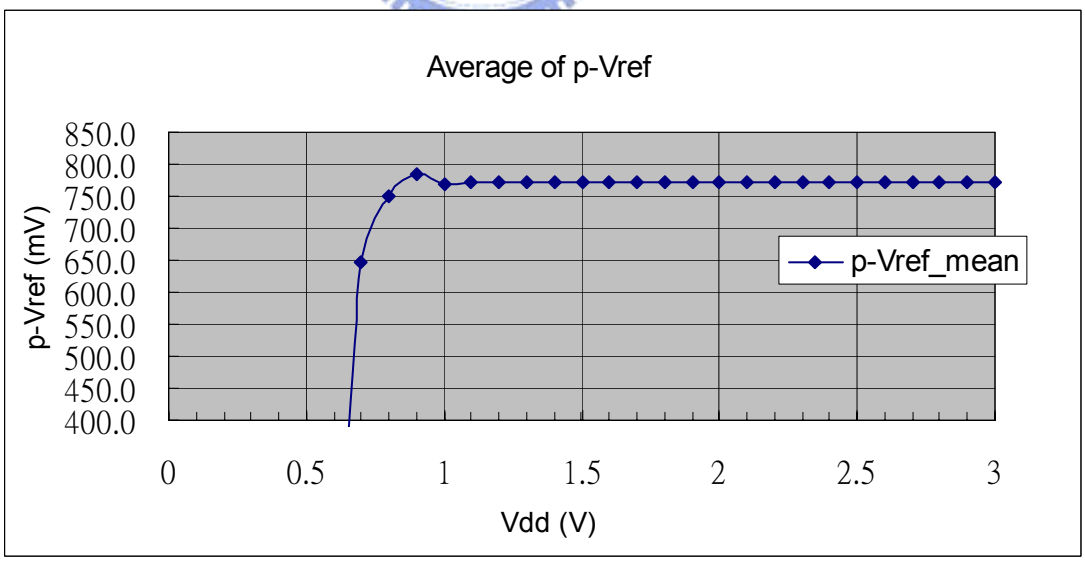


Fig. 3-6 Average of measured p-Vref vs. Vdd of Type A

Note : mean value = 772.1 mV ； STD value = 42.6 mV

PART (II) Temperature Compensation Curve

(1) Simulation Result of Type A at TT

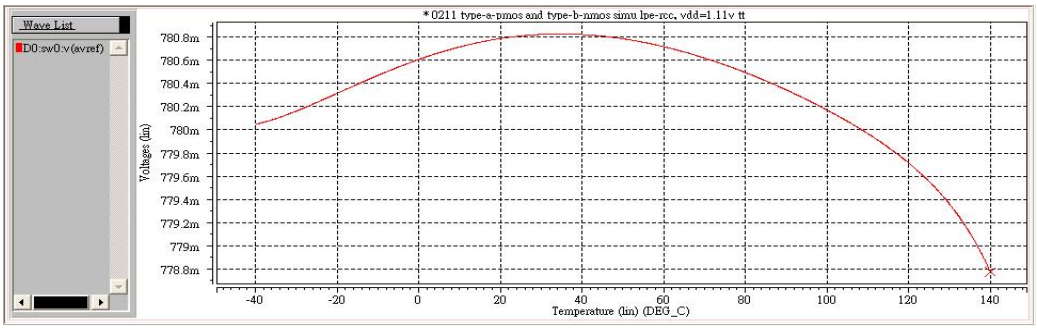


Fig. 3-7 Simulated TC curve of Type A under typical condition
axis X : temperature (℃) ; axis Y : p-Vref (mV)

(2) Measured Result of Type A

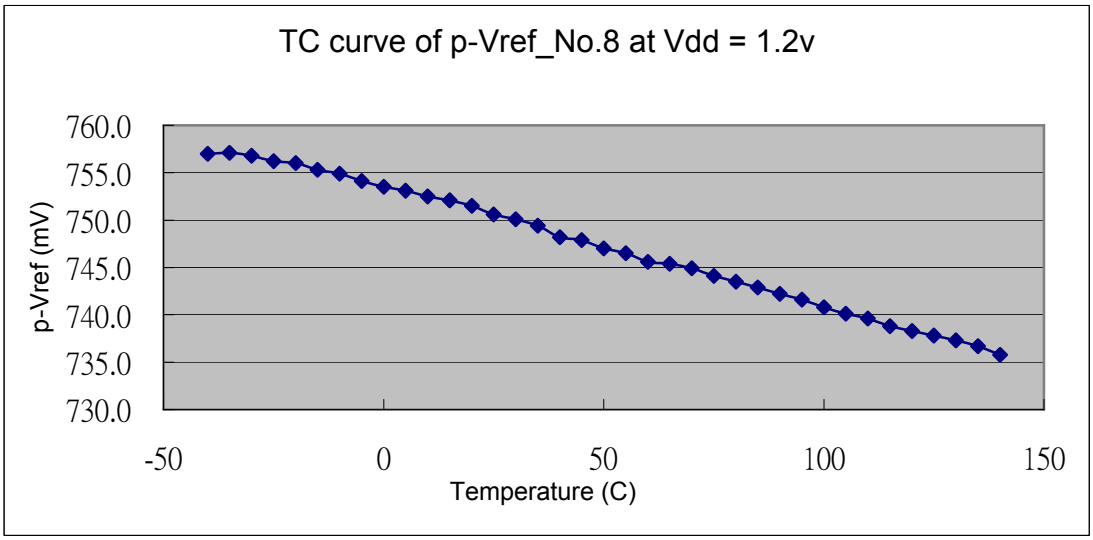


Fig. 3-8 Measured TC curve of Type A

$$TC_{F(eff)} = \frac{1}{745\ mv}\left(\frac{756-737mV}{140-(-40)}\right) = 141\ ppm/℃$$

Fig. 3-8 shows that a dramatic deviation of measured result from the simulation. Why does this IC chip fail to show the correct function of temperature compensation? The process variation associated with diffusion resistor and poly resistor is the root cause. We will have a detailed explanation in section 3.3.2 PART (II).

PART (III) Transient Response:

(1) Simulation Result of Type A at TT

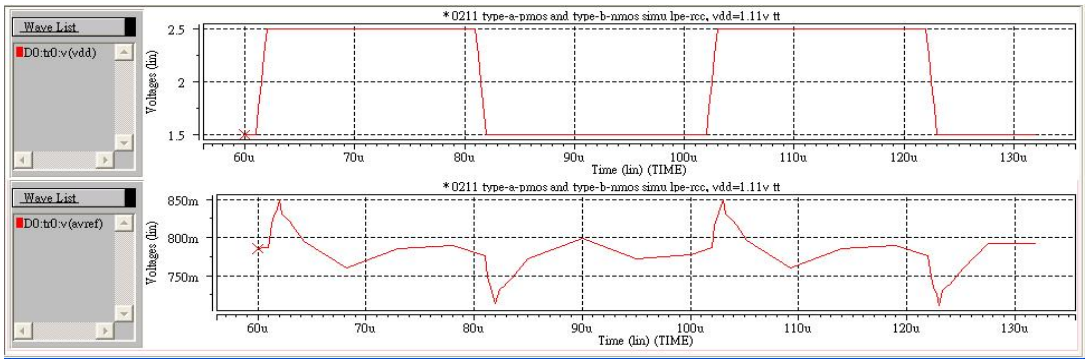


Fig. 3-9 Simulated transient response of Type A under typical condition
upper axis X : time (sec) ; axis Y : Vdd (V)
lower axis X : time (sec) ; axis Y : p-Vref (mV)

(2) Measured Result of Type A

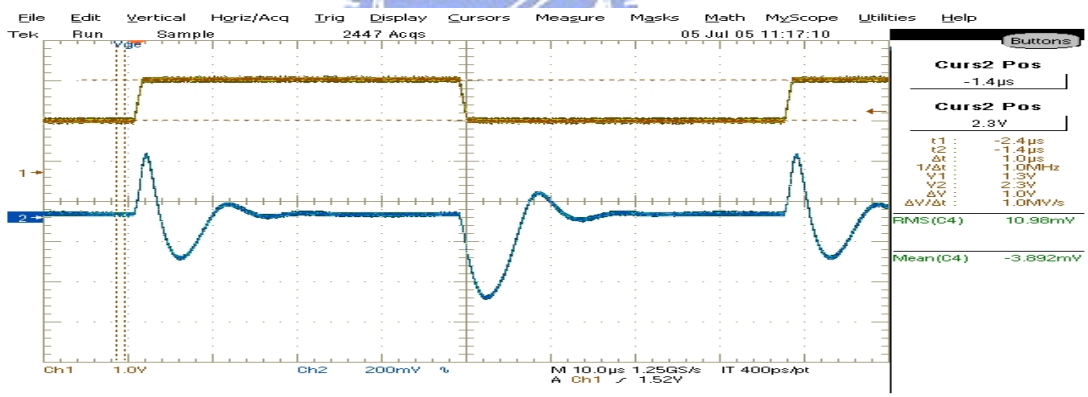


Fig. 3-10 Measured transient response of Type A at AC mode
upper axis X : time (sec) ; axis Y : Vdd (V)
lower axis X : time (sec) ; axis Y : p-Vref (mV)

PART (IV)　PSRR (Power Supply Rejection Ratio)

(1) Simulation Result of Type A under typical condition and Vdd =1.15V

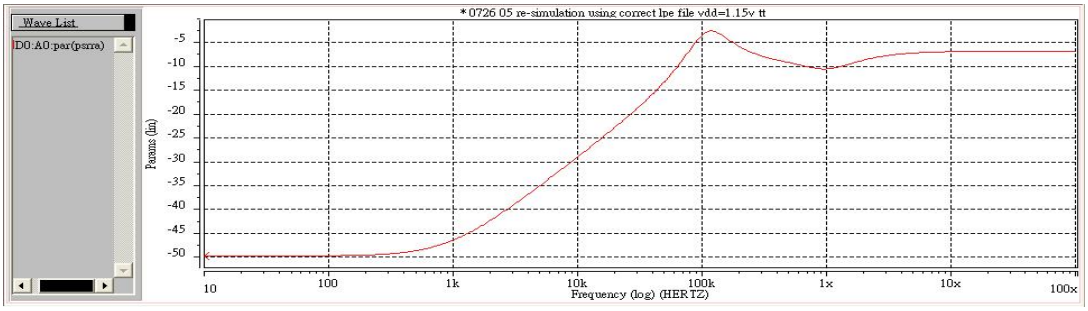


Fig. 3-11　Simulated PSRR of Type A under typical condition
axis X : frequency (Hz) ; axis Y : PSRR of p-Vref (dB)

(2) Measured Result of Type A by using network analyzer and oscilloscope

Because of the wide rage of frequencies, we use different measurement set up to collect the PSRR data.

1. For low frequency (from 100 to 100kHz)：using network analyzer to collect the data.

2. For high frequency (from100kHz to 5MHz)：using oscillator-scope to collect the data.

Next, put the measurement and simulation together for comparison, as shown in Fig. 3-12.

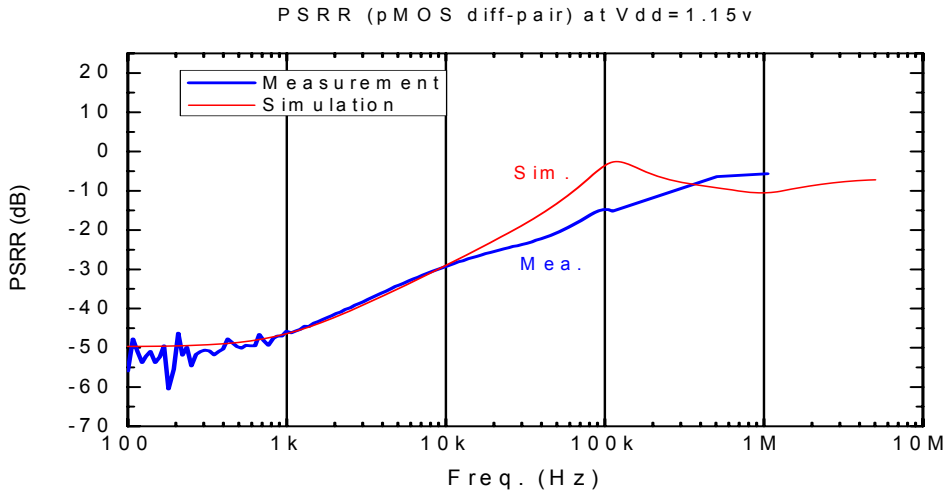


Fig. 3-12　Comparison of the measurement and simulation of PSRR of Type A under Vdd = 1.15V

Table-7 Summary table of PSRR for Type A at Vdd = 1.15V

PSRR at 1.15V	DC dB	10K dB	50K dB	114K dB	500K dB	1M dB
simulation	-49.6	-29	-13.2	-2.7	-9.2	-10.5
measurement	-55.9	-28.9	-20.6	-15.2	-6.4	-5.67
Spec.	<-60	<-30	N/A	N/A	N/A	N/A

And Fig. 3-13 shows the PSRR performance of Type A under various Vdd, 1.0V, 1.1V, 1.2V, 2.5V

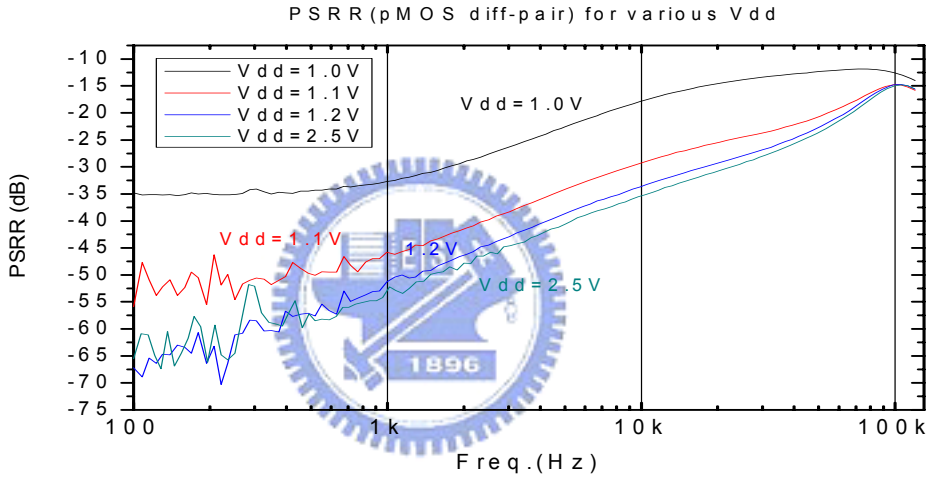


Fig. 3-13 Measured PSRR vs. frequency of Type A under various Vdd = 1.0V, 1.1V, 1.2V, 2.5V

3.3.2 Experimental Results of Type B (nMOS as OPA input stage)

PART (I) Vref (Reference Voltage) vs. Vdd

(1) Measured Result of Type B

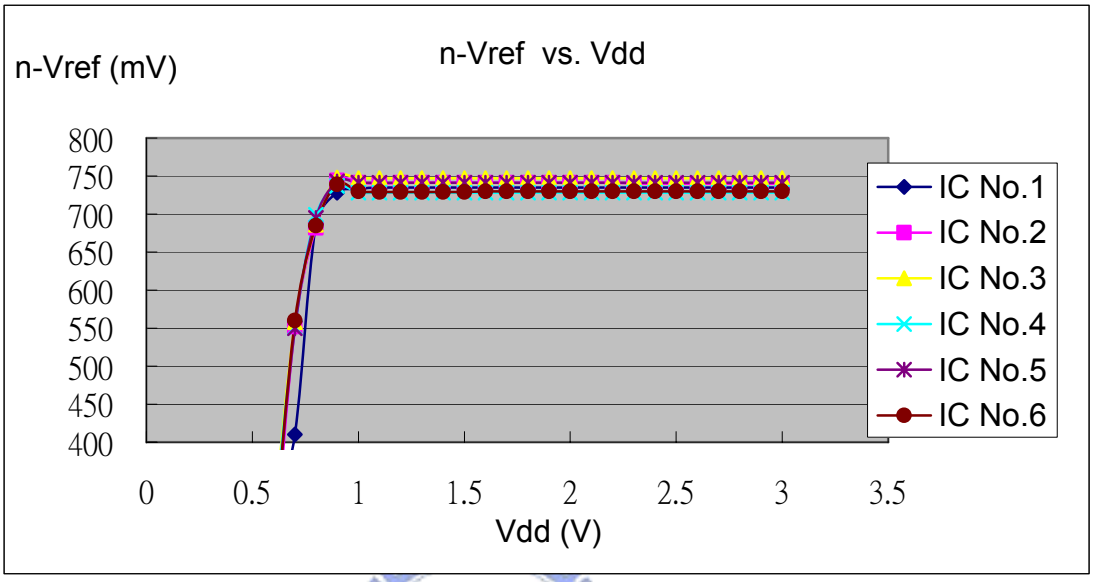


Fig. 3-14 Measured n-Vref vs. Vdd of Type B

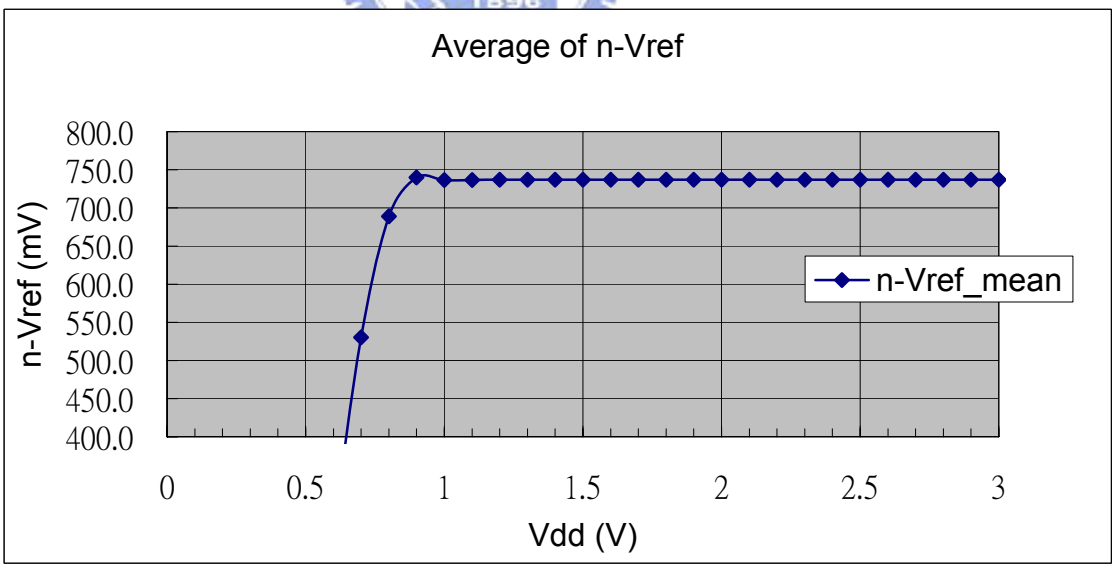


Fig. 3-15 Average of measured n-Vref vs. Vdd of Type B

Note : mean value = 737.0 mV STD value = 7.3mV

PART (II) Temperature Compensation Curve

(1) Simulation Result of Type B at TT

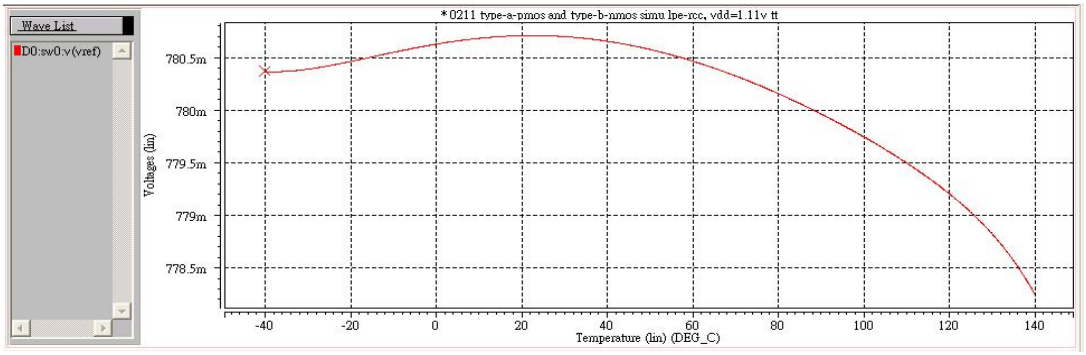


Fig. 3-16 Simulated TC curve of Type B under typical condition
axis X : temperature (℃) ; axis Y : n-Vref (mV)

(2) Measured Result of Type B

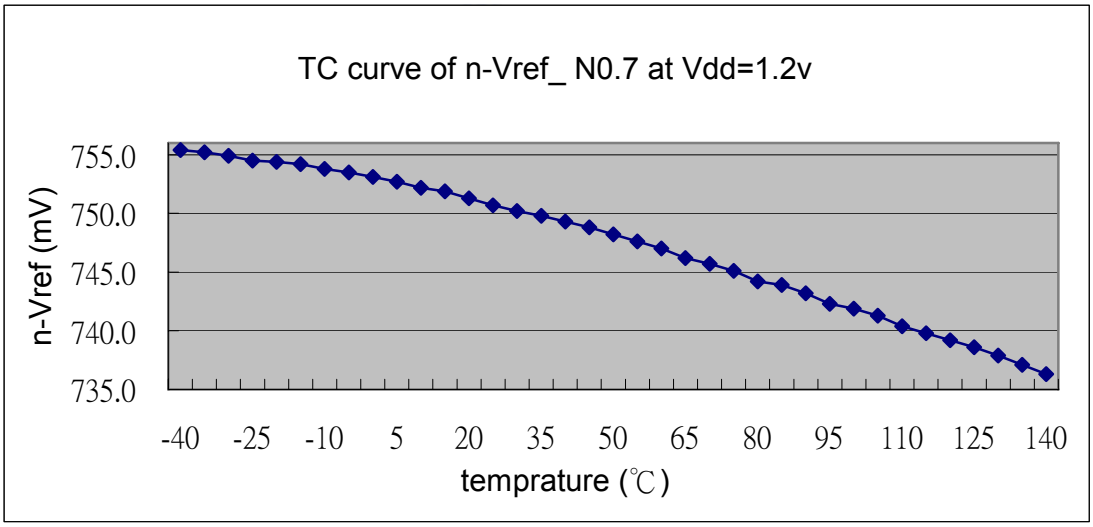


Fig. 3-17 Measured temperature compensation curve of Type B

$$TC_{F(eff)} = \frac{1}{745\ mv}\left(\frac{755-735mV}{140-(-40)}\right) = \text{ 149 ppm/℃}$$

Why does this IC chip fail to show the correct function of the temperature compensation? The process variation suffered by diffusion resistor and poly resistor is the root cause. We will have a detailed explanation on next paragraph.

(3) Experimental Result Discussion

Take Type B (nMOS as OPA's input stage) circuit as an example：

At first, we make sure the OPA can work normally, that is, the inverter port and non-inverter port keep at the virtual short condition, as shown in Table-8.

Table-8 Measured input port and output port voltage of OPA of Type B circuit at different power supply voltage

OPA Port	Vnon (mV)	Vinv (mV)	Vref (mV)	Vo (OPA)	Vdd - Vo
Vdd =3.0	764	767	754	2.44V	0.560V
Vdd =1.5	762	761	740	0.941V	0.559V
Vdd =1.2	761.1	761	738.4	0.640V	0.560V
Vdd =1.0	751.5	751.1	748.5	0.360V	0.640V

Next, we use voltage meter to measure each resistor value of the bandgap circuit in the IC chip, as shown in Table-9.

Table-9 Comparison of the design target and measured data of resistors of Type B circuit

Element name	design target	measured data	Difference
$R_X + R_1$	P^+ Poly w/i silicide 29k	29.1k	+ 0.3 %
R_{2A}	P^+ Diff w/o silicide 175k	153.9k	- 12.0 %
R_{2B}	P^+ Diff w/o silicide 175k	154.1k	- 11.9 %
R_3	P^+ Diff w/o silicide 80k	70.5k	- 11.8 %
$R_{S1} + R_{S2}$	P^+ Diff w/o silicide 1300k	1147k	- 11.7 %

Note：We use voltage meter via I/O pad of the IC chip to measure the OPA port voltage and calculate the actual resistor values.

From Table-9, we see that during the manufacture the poly resistance deviation due to process variation keep below 0.3%; however, the diffusion resistance reveals the deviation as high as 12% due to process variation. That is the reason why the circuits failed to meet TC (temperature compensation) target.

For getting more persuasive data, we put the measured resistor values into HSPICE to get the updated simulation result of Vref vs. Vdd.

After putting the updated simulation result and the measurement data together for comparison, we can see that two curves match to each other shown in Fig. 3-18.

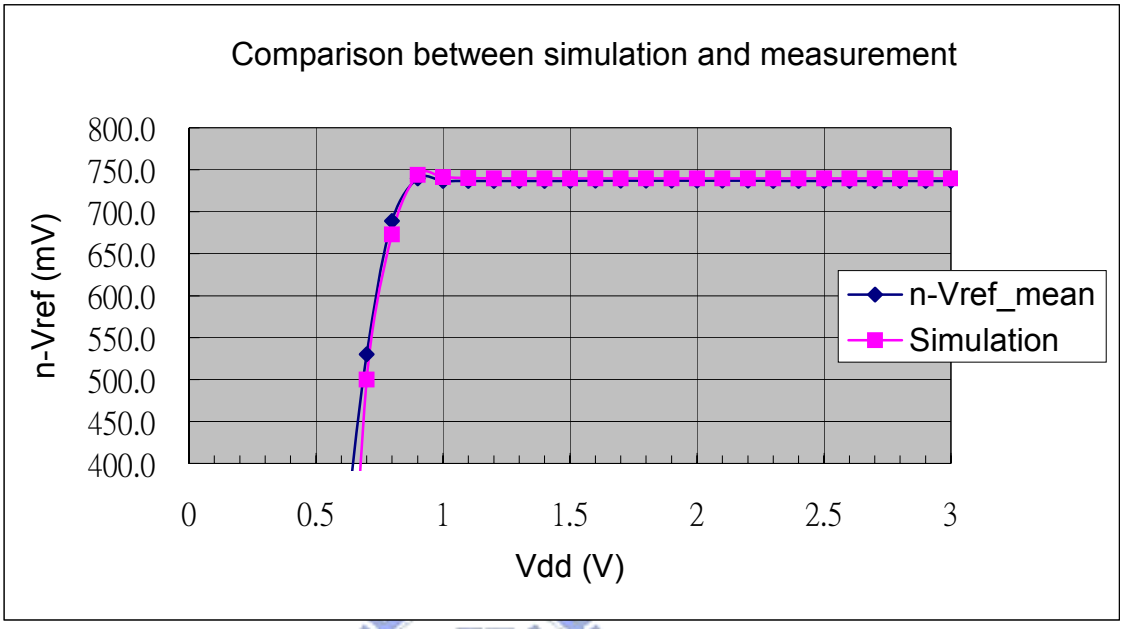


Fig. 3-18 Comparison of n-Vref vs. Vdd of new Type B-1 between simulation and measurement

This experiment gives us strong evidence to believe that the measured resistor values of the IC chip via the I/O pad are reasonable.

Using the same way, we can get the updated simulation result of temperature compensation curve.

After that, we put the updated simulation result and the measurement data together for comparison. We can see that two curves better match to each other as shown in Fig. 3-19.

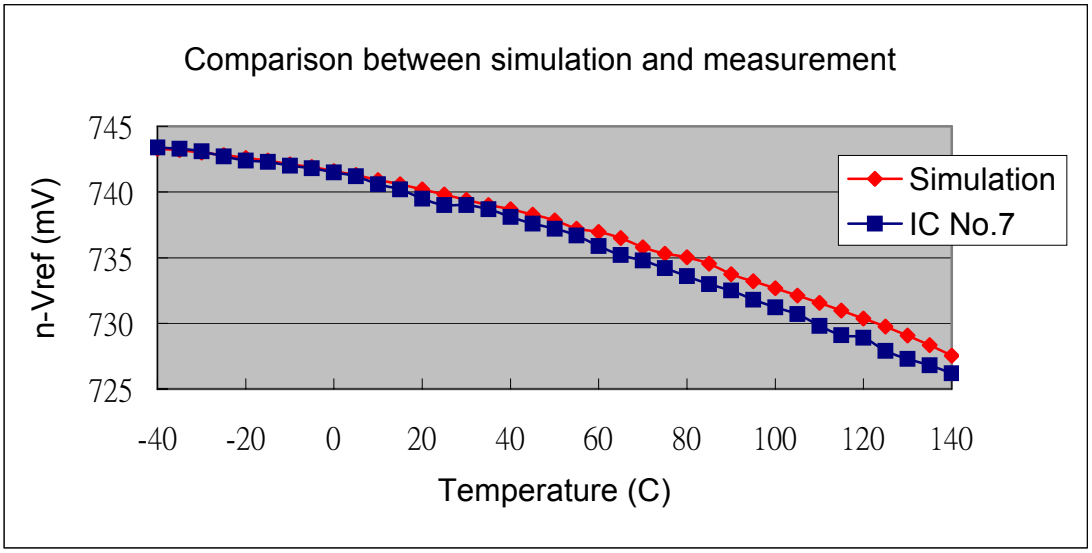


Fig. 3-19 Comparison of TC curve of new Type B-1 for simulation and measurement

Currently, we can confirm the reason responsible for the failure of the circuit in TC target. The reason comes from the different process variation between the diffusion resistor and poly resistor. If all the resistors in circuit adopted the same material, either diffusion or poly, during the layout drawing, then we can get a reasonably good measured TC curve for the bandgap circuit.

PART (III)　Transient Response：

(1) Simulation Result of Type B at TT

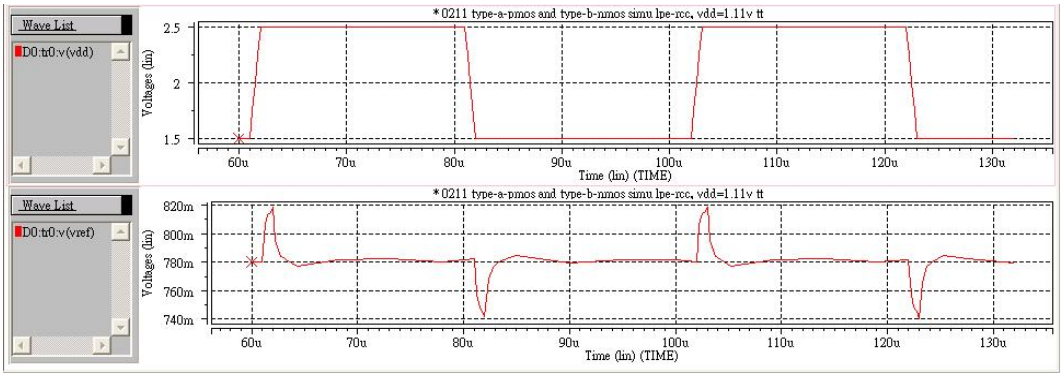


Fig. 3-20　Simulated transient response of Type B under typical condition
upper axis X : time (sec) ; axis Y : Vdd (V)
lower axis X : time (sec) ; axis Y : n-Vref (mV)

(2) Measured Result of Type B

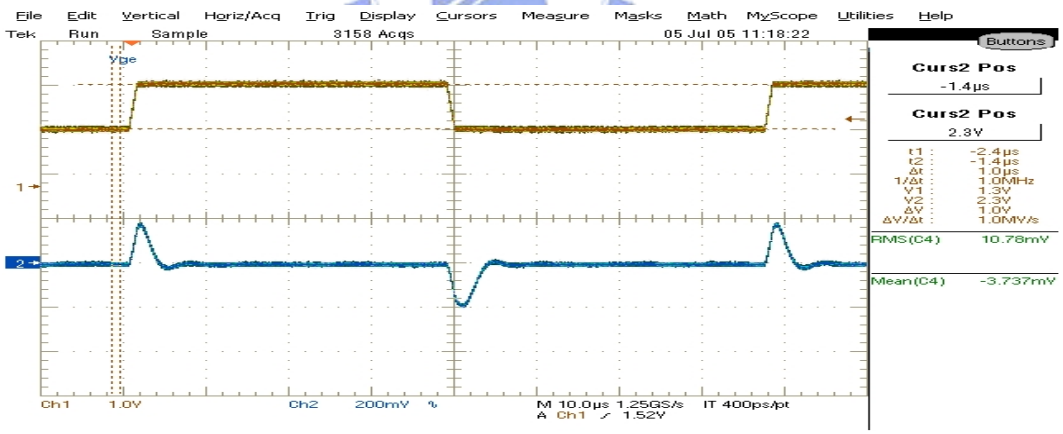


Fig. 3-21　Measured transient response of Type B at AC mode
upper axis X : time (sec) ; axis Y : Vdd (V)
lower axis X : time (sec) ; axis Y : n-Vref (mV)

PART (IV)　PSRR (Power Supply Rejection Ratio)

(1) Simulation Result of Type B under typical condition and Vdd = 1,15V

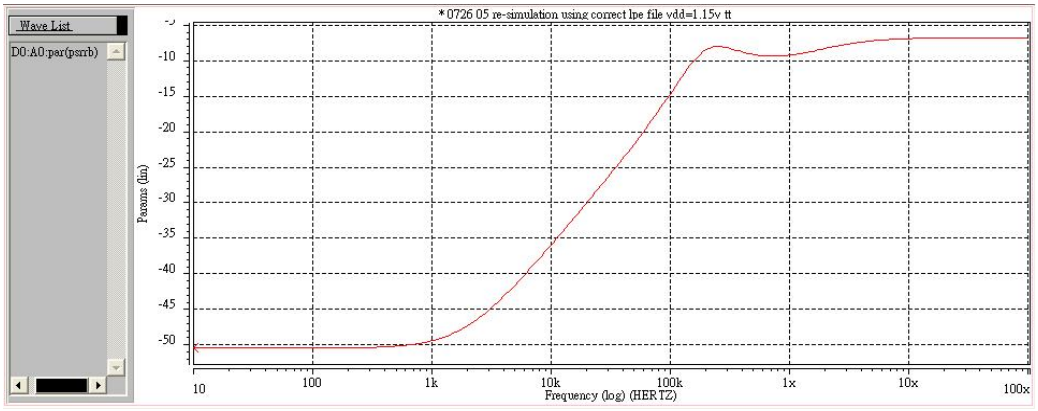


Fig. 3-22　Simulated PSRR of Type B under typical condition
axis X : frequency (Hz) ; axis Y : PSRR of n-Vref (dB)

(2) Measured Result of Type B by using network analyzer and oscilloscope

Following the same way, we put the measured data and the simulated data together for comparison, as shown in Fig. 3-23.

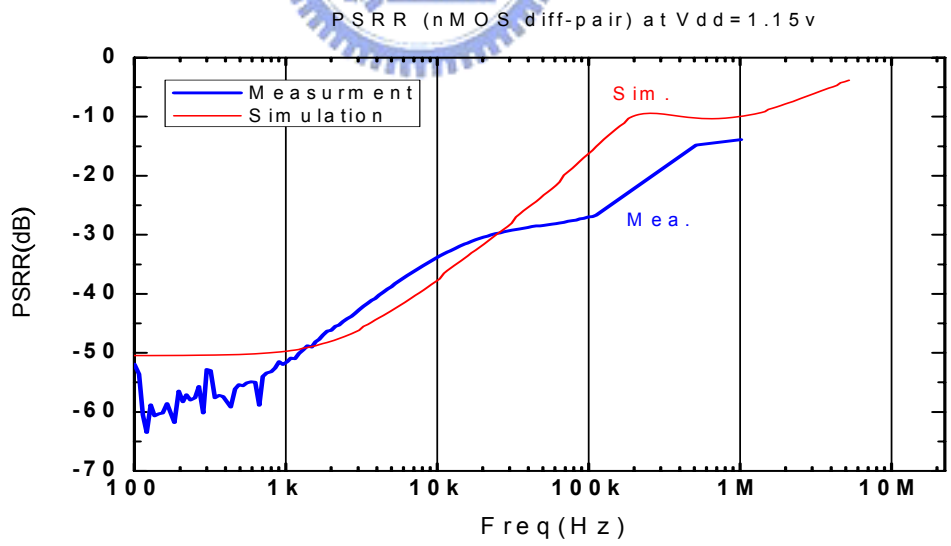


Fig. 3-23　Comparison of the measured and simulated PSRR for Type B under Vdd = 1.15V

Table-10 Summary table of PSRR for Type B at Vdd = 1.15V

PSRR at 1.15V	DC dB	10K dB	50K dB	114K dB	500K dB	1M dB
simulation	-50.4	-37.4	-23.2	-15.0	-10.2	-9.9
measurement	-51.5	-33.8	-28.4	-26.7	-14.8	-13.9
Spec.	<-60	<-30	N/A	N/A	N/A	N/A

And Fig. 3-24 shows the PSRR performance of Type B under various Vdd, 1.0V, 1.1V, 1.2V, 2.5V

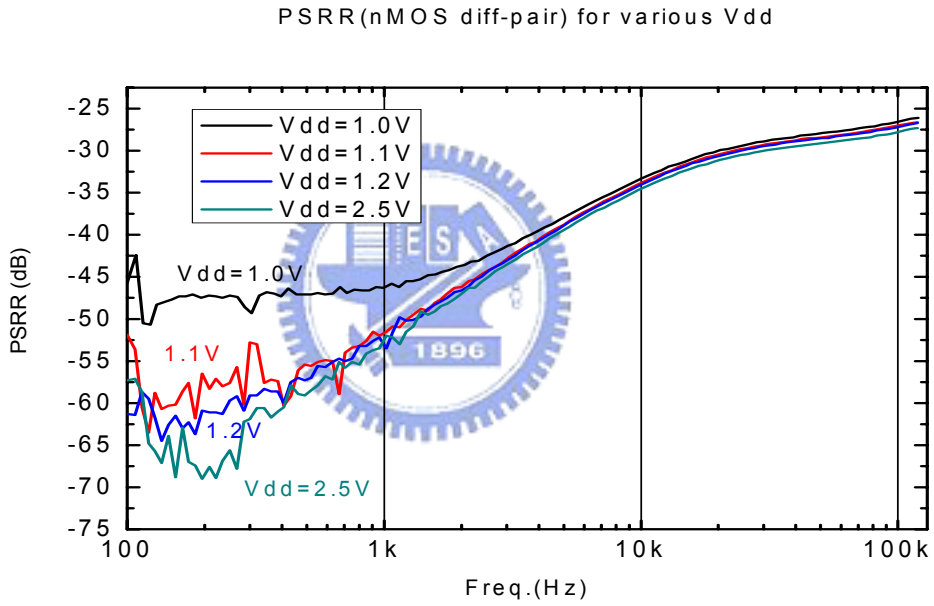


Fig. 3-24 Measured PSRR vs. frequency of Type B under various Vdd, 1.0V, 1.1V, 1.2V, 2.5V

(3)Experimental Result Discussion

1. Both simulated and measured results suggest that the higher power supply voltage, the better PSRR.

2. Fig. 3-25 shows the comparison of the pre-layout simulation and the post-layout simulation.

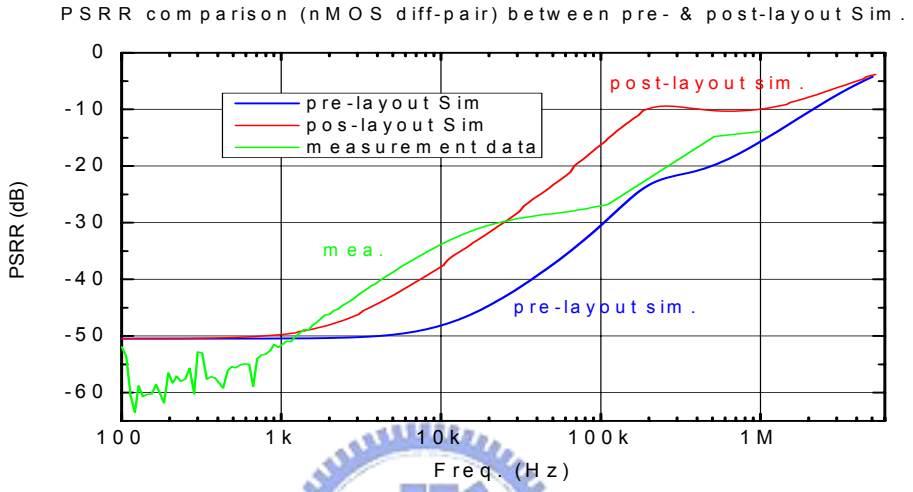


Fig. 3-25 Comparison of the pre-layout simulation and the post-layout simulation

3. From Fig. 3-25, we see that the post-layout simulation deviated from the pre-layout simulation since frequency above 1KHz. What factor causes the PSRR to become worse with increasing frequency above 1KHz ? The root cause maybe come from layout symmetry of pMOS M1, M2, M3 as shown in Fig. 3-26.

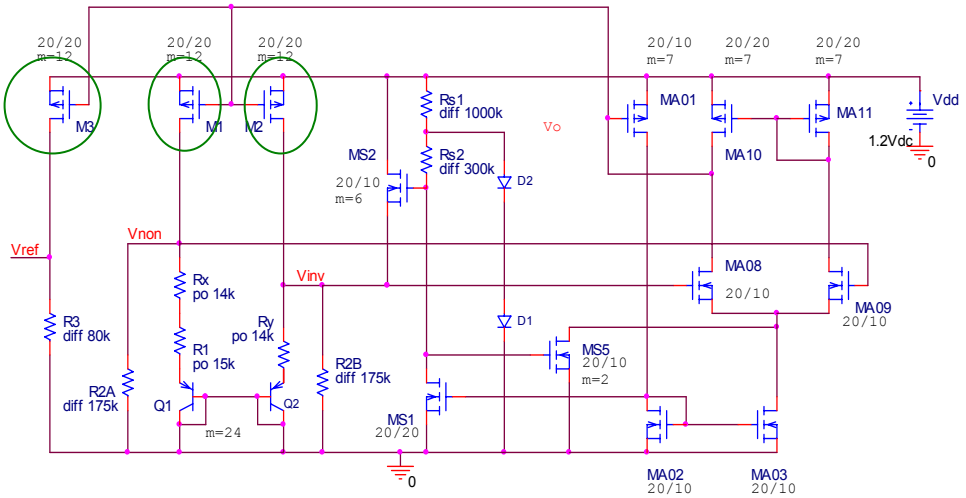


Fig. 3-26 pMOS M1, M2, M3 in the bandgap type B circuit

The verification was done by skipping the layout drawing of the pMOS M1, M2, M3 and supporting them as ideal devices .The results shown in Fig. 3-27 indicates better match between pre-layout and post layout simulation.

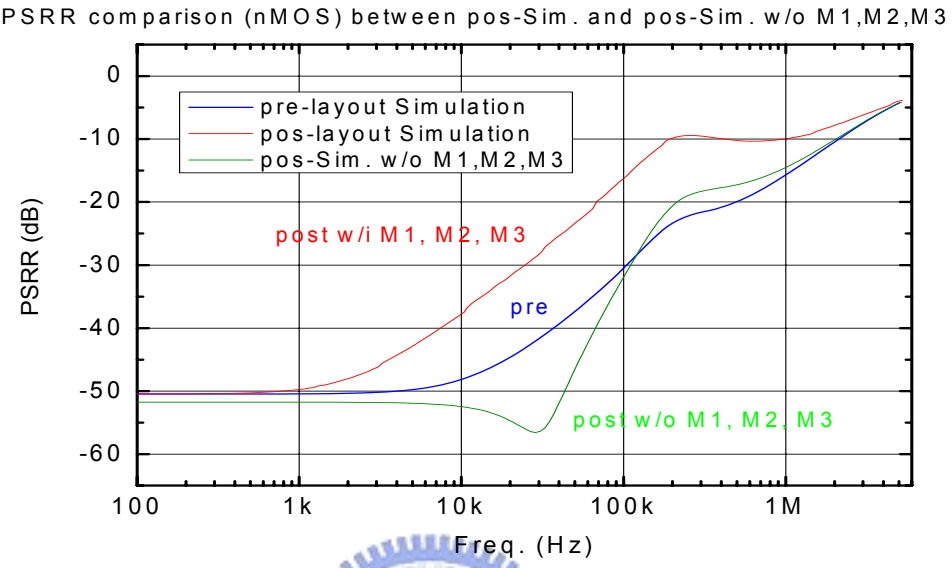


Fig. 3-27 The post-layout simulation of the PSRR of the experiment

Chapter 4 DESIGN OF LOW VOLTAGE HIGH PSRR BANDGAP REFERENCE CIRCUIT WITH TSMC 0.35μm CMOS PROCESS

4.1 Design Motivation

In chapter 2, we demonstrated two kinds of bandgap reference voltage circuits by using TSMC 0.18μm CMOS process as shown in Fig. 2-9.

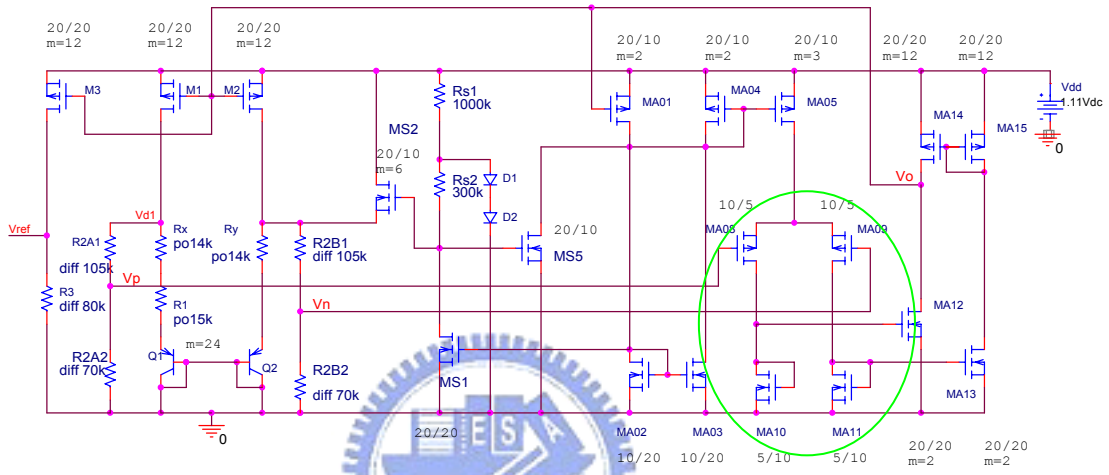


Fig. 2-9 The bandgap circuit topology for Type A

However, using this circuit topology, the differential pair MOSFET in OPA cannot work in saturation region for all process corners if we use low-end and low cost process, e.g. TSMC 0.35μm CMOS process.

For example：The pMOS differential pair, MA08 & MA09, will be forced into triode region at the process corner SF and 125℃. The cause comes from the MOS-connected diode as shown in Table-11 and circuit schematic in Fig. 4-1.

Table-11 Threshold voltage of nMOS & pMOS at different corners

125℃	Vthn (mV)	Vth,p (mV)
corner S	545	-669
corner T	445	-569
corner F	345	-469

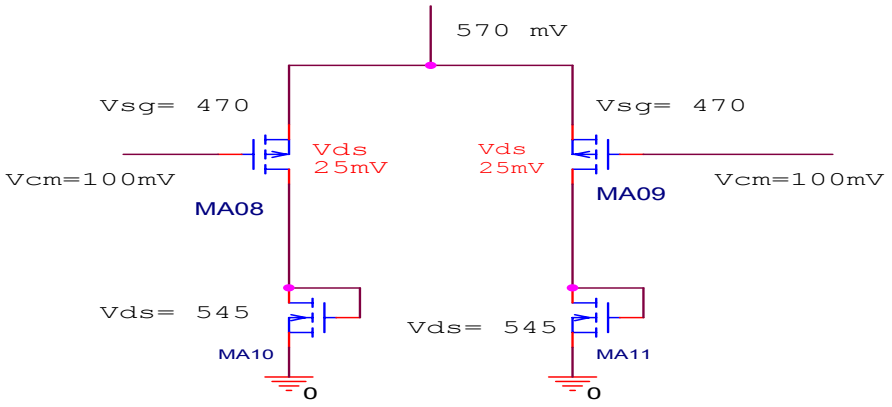


Fig. 4-1 Detailed analysis of the OPA's differential pair

For T=125℃, the nMOS threshold voltage, Vthn, at slow corner (S), is 545mV, and the pMOS threshold voltage, Vthp, at fast corner (F), is about -470mV. This implies that the pMOS differential pairs (MA08, MA09) will be forced into triode region if we assume the common mode voltage is 100mV.

So, in chapter 4 we evaluate other kinds of OPA architectures, aiming to find others of OPA architectures that can work at low voltage and all process corners if a low-end and low cost process is used, e.g. TSMC 0.35μm CMOS process.

The same as chapter 2, there are two kinds of bandgap circuits in this chapter. The purpose is to verify technology-scaling effect on BGR circuit performance.

The first circuit (Type D) use nMOS as its OPA's differential pairs. The main difference (compared with the previous circuit – Type B in chapter 2) is that we use current source instead of current mirror.

Besides, the temperature effect on the base-emitter voltage and threshold voltage should be considered. So we modify the bandgap core circuits by inserting resistors. The reason is that we want to change the slope of OPA's common mode voltage vs. temperature. To speak clearly, the OPA's common mode voltage provided by the bandgap core circuit will degrade as the ambient temperature is rising.

For example, the temperature coefficient of the base-emitter voltage is approximately -1.85mV/K while that of the threshold voltage of the nMOS transistor is around -1.0mV/K in TSMC 0.35μm CMOS technology. That is, at high temperatures, $V_{EB(on)}$ may be less than Vthn + $2V_{DS(sat)}$, and the bandgap reference circuit will not function properly.

But after modifying the bandgap core circuit, the OPA's differential pair can work in the saturation region even at the worst case (e.g. corner SS, SF, and T = 125℃).

The second circuit (Type C) use pMOS as its OPA's differential pair. The main difference (compared with the corresponding circuit – Type A in chapter 2) is that we use current sources instead of the MOS-connected diodes. Besides, we put two CG (common gate) nMOS as the current followers at the output stage in order to get a stable biased voltage and biased current. This kind of topology is different from that of Type A (pMOS as OPA's differential pair). The reasons will be presented in the following sections.

4.2 Design Concepts and Circuit Implementation

4.2.1 Design Concepts and Circuit Implementation of Type D

Fig. 4-2 shows a complete circuit topology of Type D in which bandgap core, start up, and OP-Amplifier circuits are incorporated.

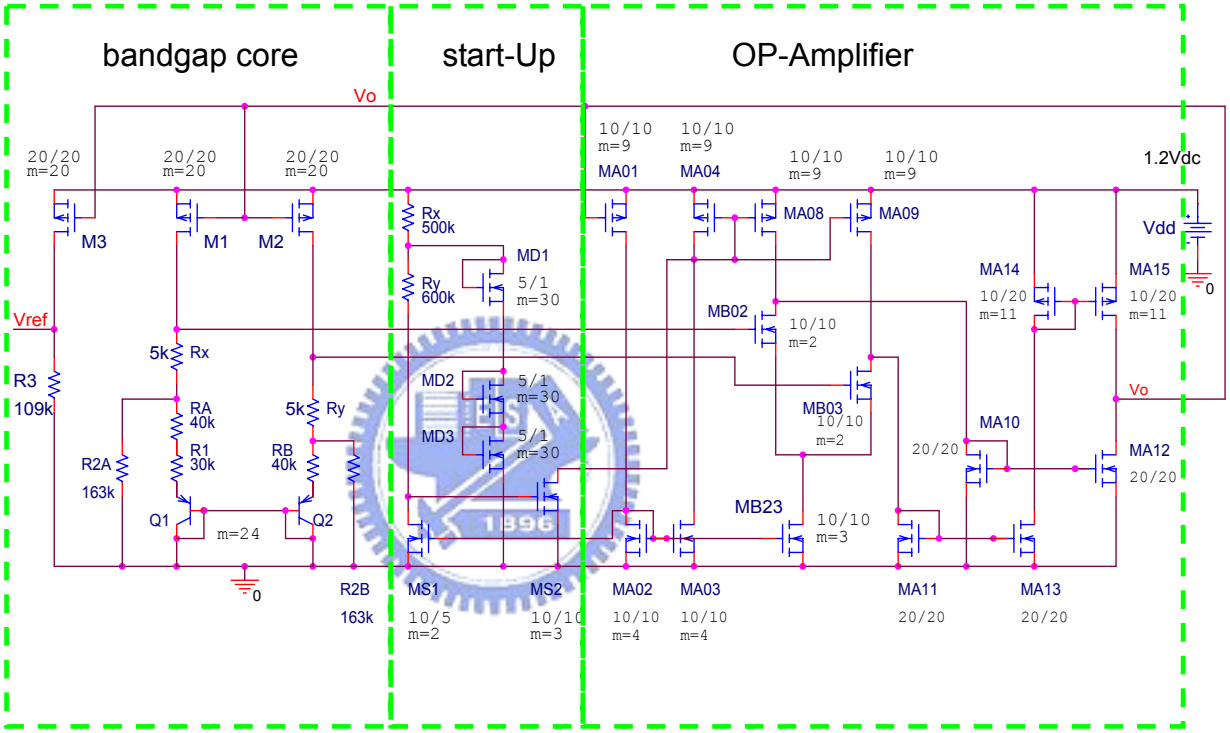


Fig. 4-2 The complete bandgap circuit topology of Type D (bandgap core + start-up + OP-Amplifier with nMOS input stage)

The idea of Type D circuit comes from the previous work done by P. Malcovati et al. [1] as shown in Fig. 4-3 and Fig. 4-4. We modify the circuit presented in the referred work to create the Type D circuit.

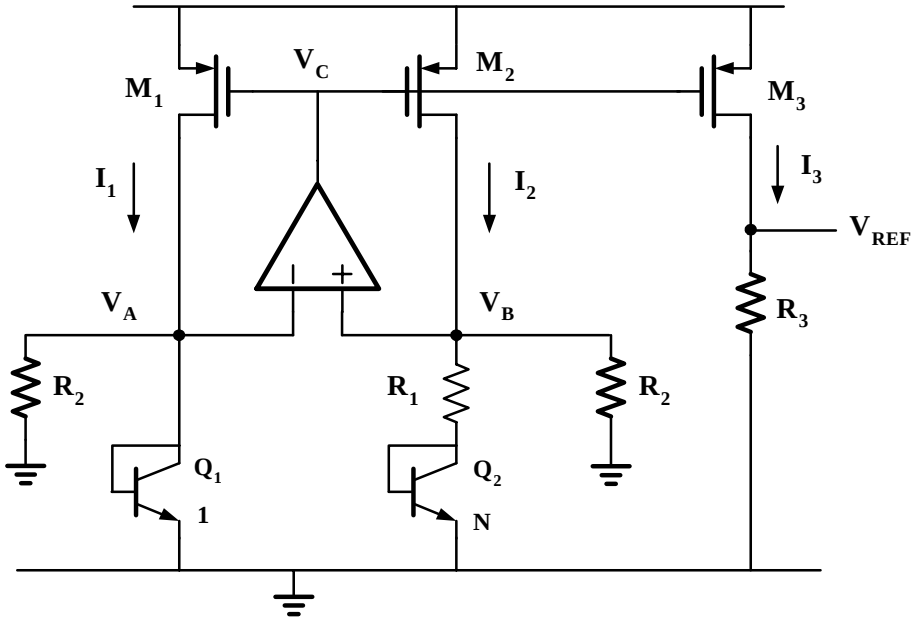


Fig. 4-3 Schematic of bandgap circuit proposed by the previous work done by P. Malcovati et al. [1]

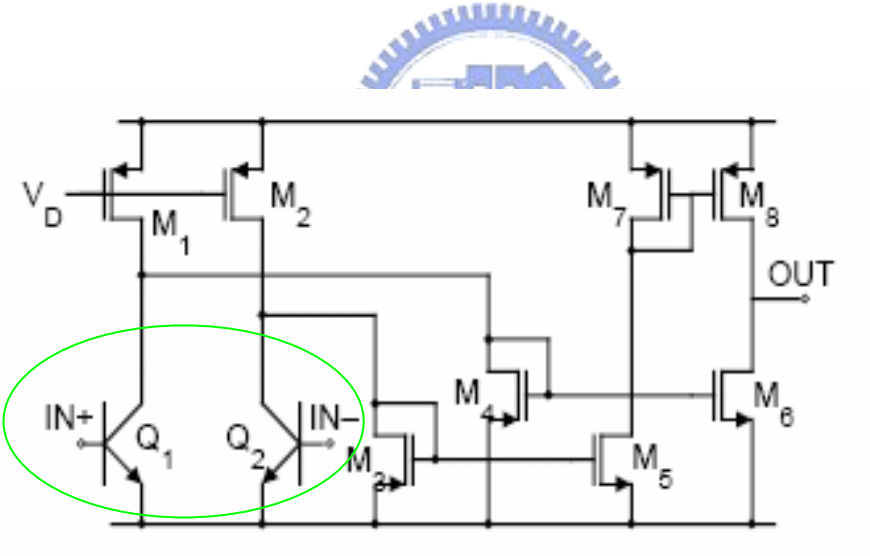


Fig. 4-4 Schematic of the two-stage operational amplifier

In Fig. 4-4, M_1 and M_2 are current sources; Q_1 and Q_2 are differential amplifiers.

We created a similar topology as shown in Fig. 4-5. The difference is that we use nMOS (MB02, MB03) as the differential pair to replace the BJT Q_1, Q_2

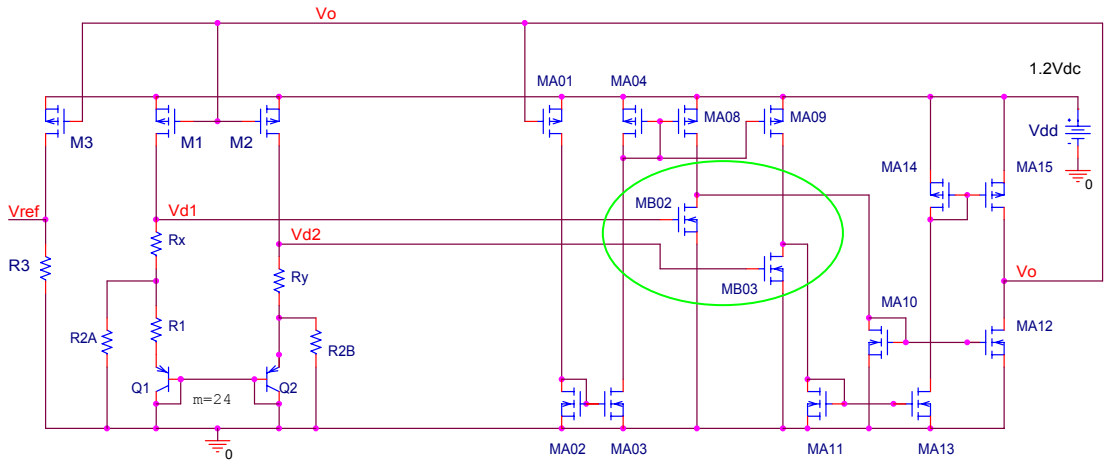


Fig. 4-5 Prototype-1 circuit topology of Type D

But this kind of circuit reveals a serious disadvantage in that it can only pass TT, but fails at all other corners FF, SS, FS, SF.

We analyze the cause of failure and find that at the different process corners, the gate voltages of the OPA's differential pair, which is provided by the bandgap core circuit, keep the same, but the Vthn of the nMOS of the differential pair are different. This physical phenomenon will make the biased current change at the different process corners.

To speak clearly, we want to keep the bias point the same at the different process corners, but in fact the bias point will shift at various process corners. This is why this kind of OPA can only work at TT, but fails at the other corners.

Taking TSMC 0.35μm CMOS process and model as an example, we can see the relationship between Vthn and temperature at various corners as shown in Fig. 4-6.

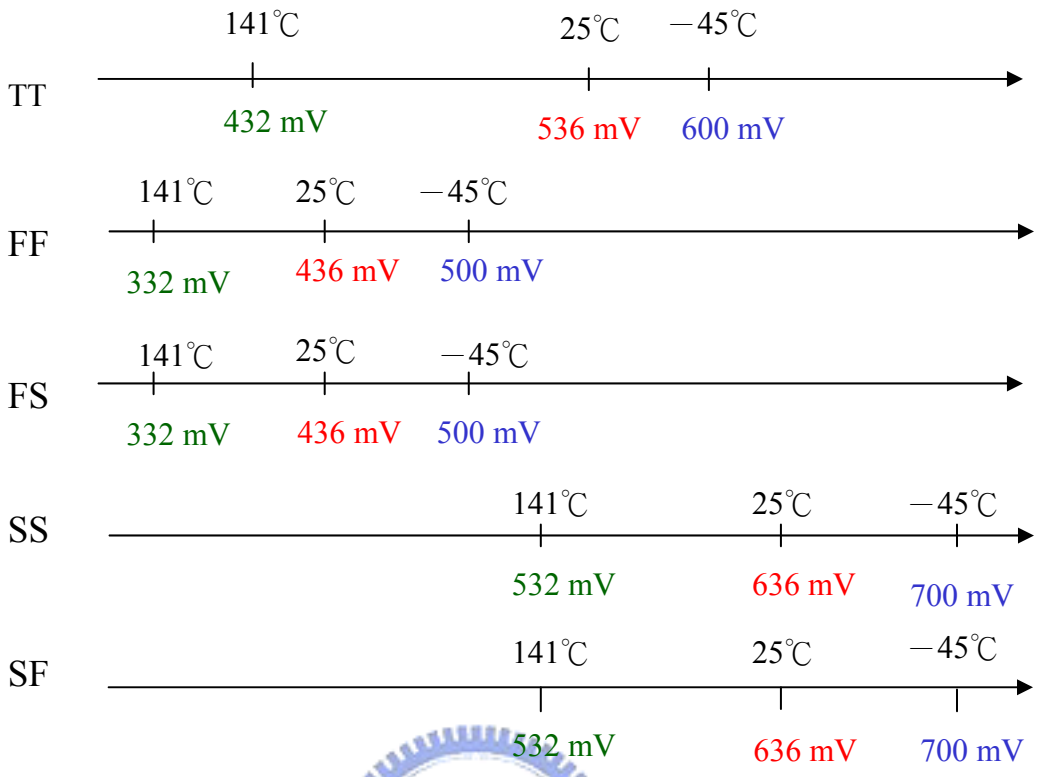


Fig. 4-6 Vthn vs. temperature at various corners

In order to solve the corner failure issue mentioned for prototype-1 circuit of Type D in Fig.4-5, we add a current source below the differential pair. That result in the prototype-2 circuit of Type D as shown in Fig. 4-7.

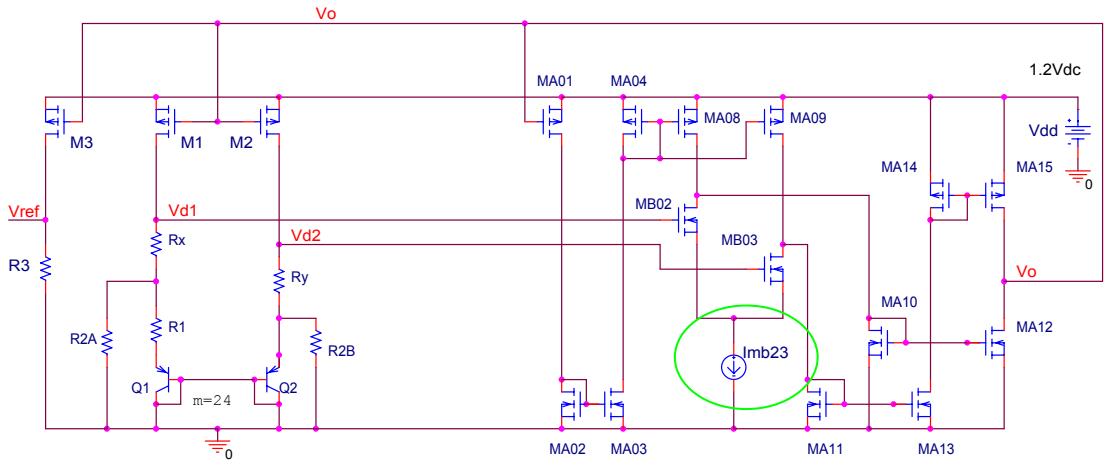


Fig. 4 -7 Prototype-2 circuit topology of Type D

However, the temperature effect on the V_{BE} and Vthn should be considered.

We find that the node voltage Vd1 & Vd2 can not drive the OPA at high temperature even though the nMOS threshold voltage (Vthn) degrade as the ambient temperature rise. In other words, the down slope of the node voltage Vd1 & Vd2 vs. temperature curve is falling sharply than the slope of the nMOS threshold voltage (Vthn) vs. temperature as shown in Fig. 4-8, Table-12 and Table-13.

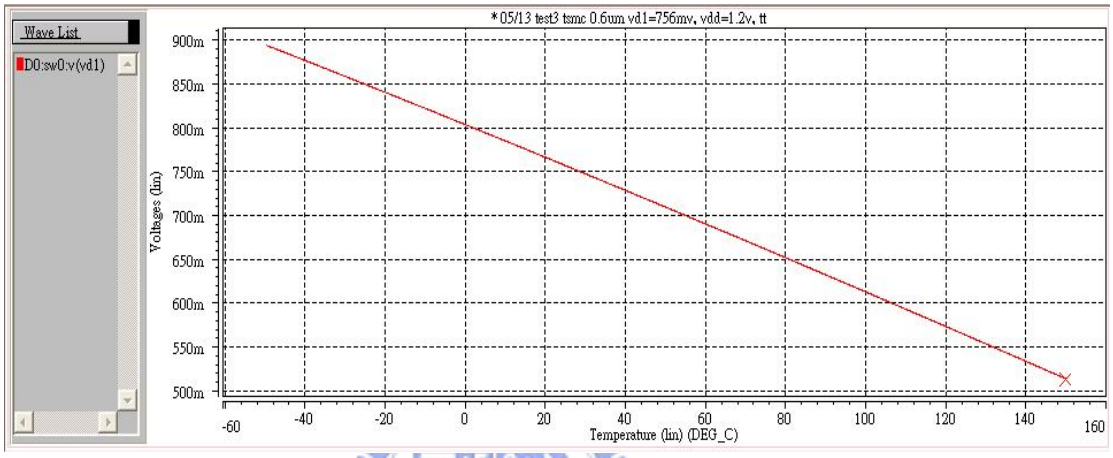


Fig. 4-8 Node voltage Vd1 vs. temp. of the prototype-2 circuit of Type D

Table-12 Node voltage Vd1 vs. temp. of the prototype-2 circuit of Type D

	-45℃	-20℃	25℃	125℃	140℃
Vd1(mV)	885	840	756	563	533

Table-13 The Vthn of TSMC 0.35μm CMOS process

	-45℃	-20℃	25℃	125℃	140℃
Vthn (mV) at S	**700**	**676**	**636**	**545**	**532**
Vthn (mV) at Typical	600	577	536	445	432

Comparing node voltage Vd1 in the Table-12 with the Vthn at slow corner (S) in Table-13, we find that:

1. The worst case does not occur at the low temperature but at the high temperature. From Table-12 and 13, we see that the Vd1 is almost equal to Vthn at corner S and T = 140℃. So this circuit topology is still not useful for all process corners.

2. The temperature coefficient of the base-emitter voltage is approximately -1.85mV/K while that of the threshold voltage of the nMOS transistor is around -1.0mV/K in TSMC 0.35μm CMOS technology. That is, at high temperatures, $V_{EB(on)}$ may be less than Vthn + $2V_{DS(sat)}$, and the bandgap reference circuit will not function properly.

To fix this problem, we insert another resistor pairs, R_A & R_B, as shown in Fig.4-9. The purpose is to change the down slope of "Vd1 vs. temperature" curve as shown in Fig.4-10.

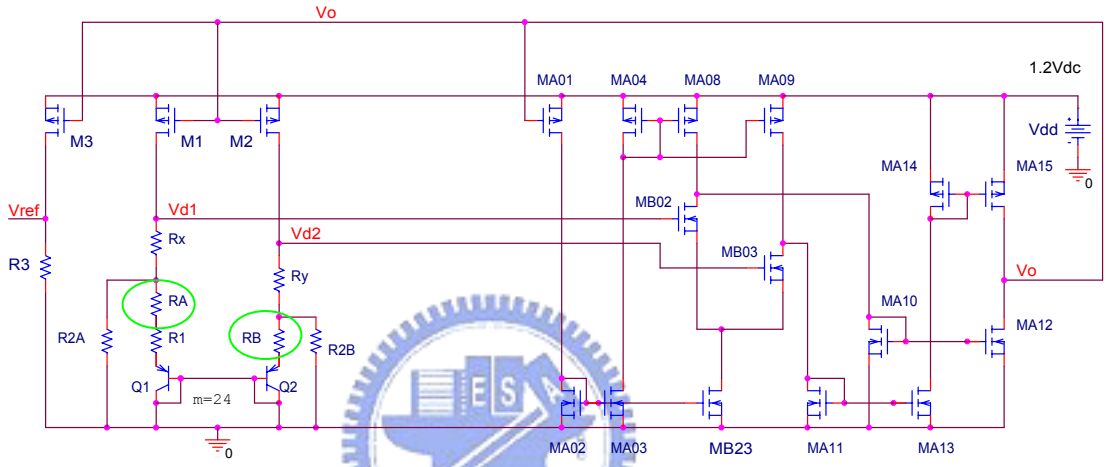


Fig. 4-9 The final circuit topology of Type D

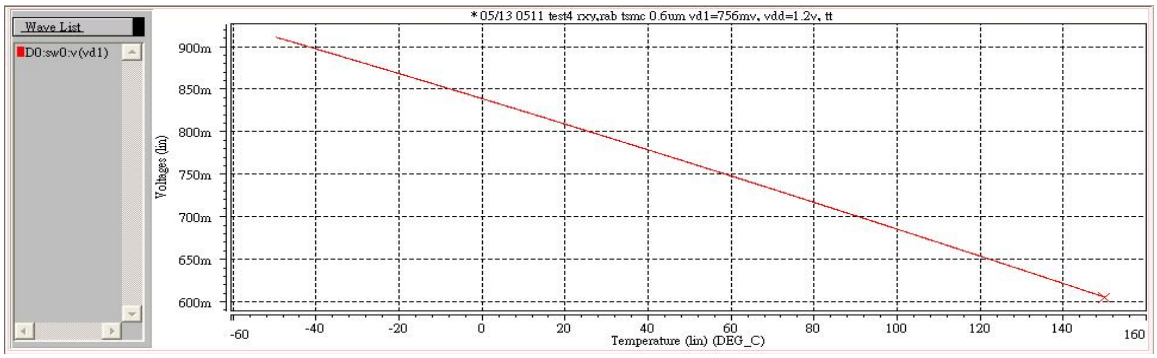


Fig. 4-10 Node voltage Vd1 vs. temperature curve of the Type D

Fig. 4-10 and Table-14 show the relationship of node voltage Vd1 and temperature for the Type D final circuit.

Table-14 Node voltage Vd1 vs. temperature curve of the Type D

	-45℃	-20℃	25℃	125℃	140℃
Vd1(mV)	904	868	801	645	621

After comparing Table-13 and 14, we can make a conclusion：after inserting resistors R_A & R_B, the down slope of the “Vd1 vs. Temperature“ curve has changed. That will make the node voltage, Vd1, large enough to drive the nMOS (of the OPA’s differential pair) at all process corners with temperature range from - 40℃ to 140℃

What reason makes the slope of “Vd1 vs. Temperature” curve change after inserting R_A & R_B? The answer can be found by the node voltage analysis as shown in Fig. 4-11:

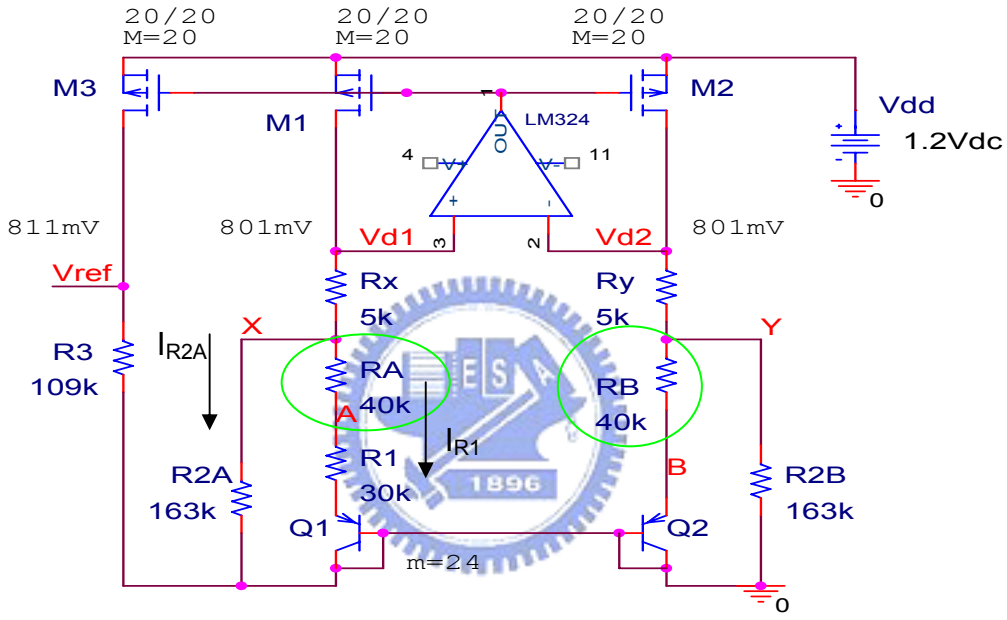


Fig. 4-11 The simplified bandgap circuit topology of Type D

1. We want to change the slope, ξ, of the curve of the “Vd1 vs. Temperature”, which can be expressed as $Vd2 = \xi \times T + K$
2. $Vd2 = V_Y + (I_{R1} + I_{R2A}) Ry = V_Y + K$
3. $V_Y = I_{R1} R_B + V_{EB2} = \Phi_T \ln 24 (R_B / R1) + V_{EB2}$
4. We can get that $Vd2 = \Phi_T \ln 24 (R_B / R1) + V_{EB2} + (I_{R1} + I_{R2A})Ry$

$= \xi \times T + K$

4.2.2 Design Concepts and Circuit Implementation of Type C

An interesting question follows the design of the Type D circuit：is there any possible to implement the “OP-Amplifier with pMOS input stage” based on the same idea? The answer is “Yes”, with Type C circuit as shown in Fig. 4-12. However the circuit’s architecture becomes more complicated. Besides, this circuit occupies more layout area but provide worse performance compared with the Type D (OP-Amplifier with nMOS as the input stage).

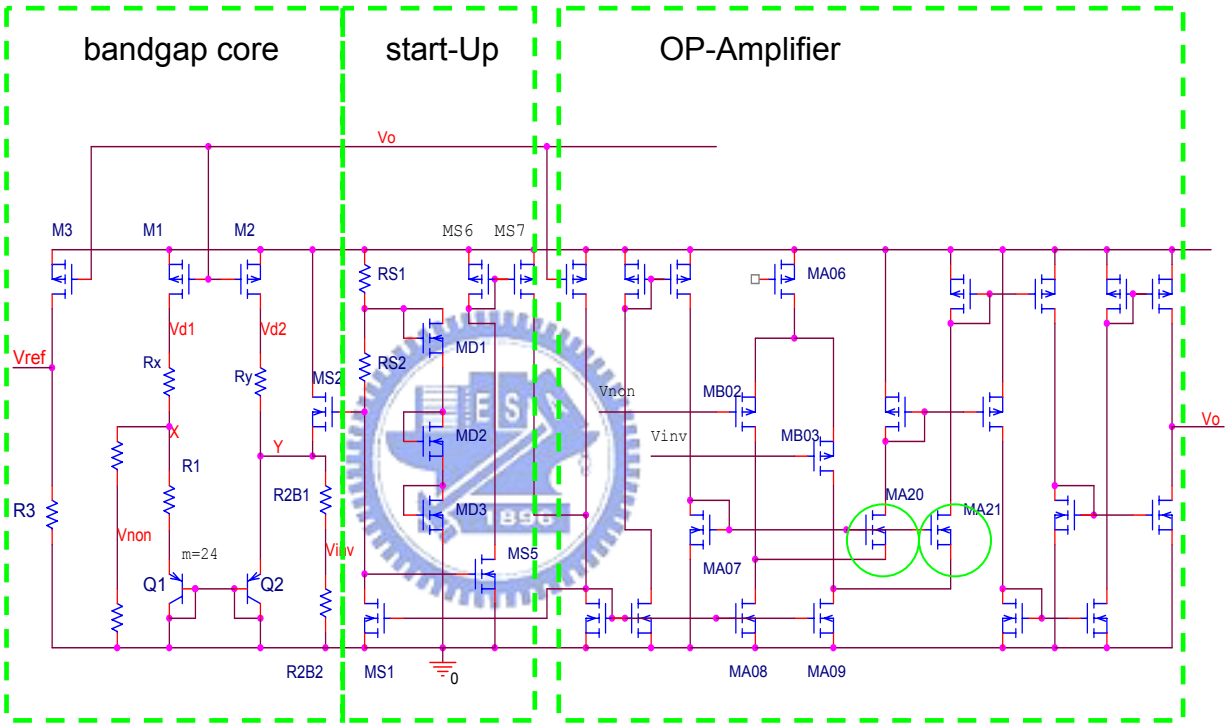


Fig. 4 –12 The complete bandgap circuit topology of Type C adopting pMOS as input differential pair

In Type C, we put two CG (common gate) nMOS - MA20, MA21 - as the current followers at the output stage in order to get a stable biased voltage and biased current. It is an important point in the Type C circuit.

Without these two CG nMOS – MA20 & MA21, as shown in Fig. 4-13, this kind of circuit cannot work. The reason can be explained through node voltage analysis as follows：

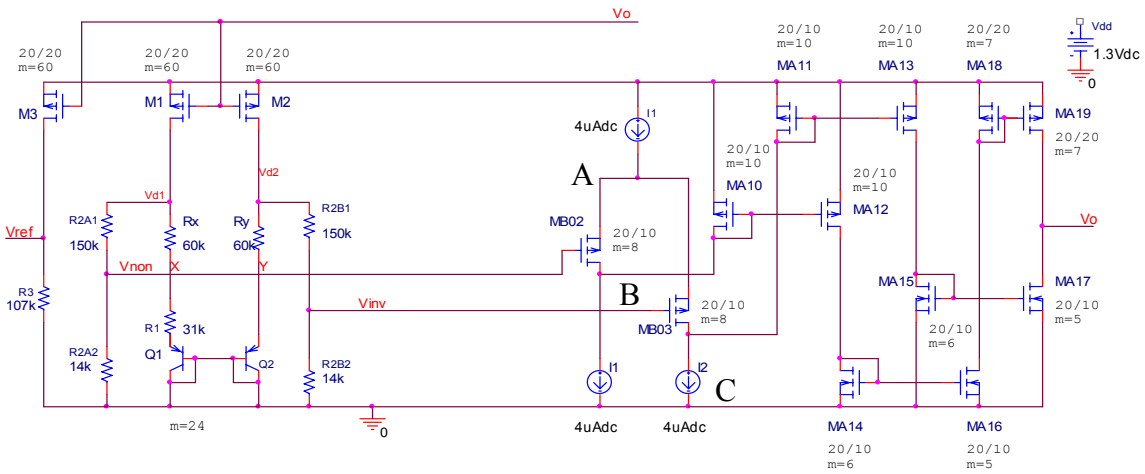


Fig. 4-13 Simplified prototype-1 circuit topology of Type C

Assumption:

(1) Vdd = 4V

(2) The Vgs of pMOS MA11, MA13 is 0.8V.

(3) The common mode voltage V_{CM}=0.1V

Follow this assumption , the node C voltage = 4 - 0.8 = 3.2 V

the node B voltage = 4 - 0.8 = 3.2 V

the node A voltage = 3.3 V

and the Vgs of differential pairs MB02, MB03 = 3.3 - 0.1V = 3.2 V

So, the biased voltage of the pMOS differential pairs, Vgs, will drift when the power supply Vdd change, as shown in Fig. 4-14. This kind of circuit topology can not work.

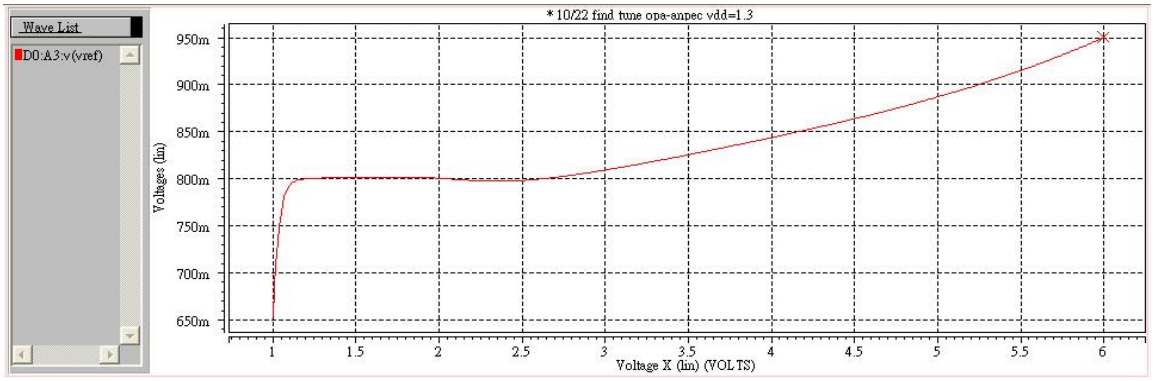


Fig. 4-14 Simulated Vref vs. Vdd of the prototype-1 circuit of Type C

If we put two current followers (common gate nMOS) MA05, MA06 at the bottom of the MA10 , MA11 respectively, as shown in Fig. 4-15, we will get the correct simulation result, as shown in Fig. 4-16.

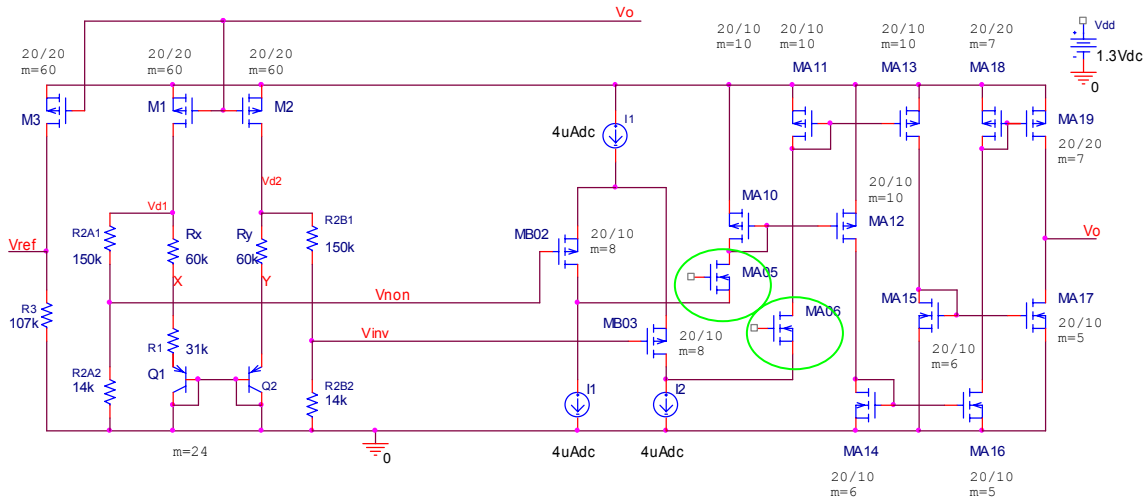


Fig. 4-15 Simplified bandgap circuit topology of Type C

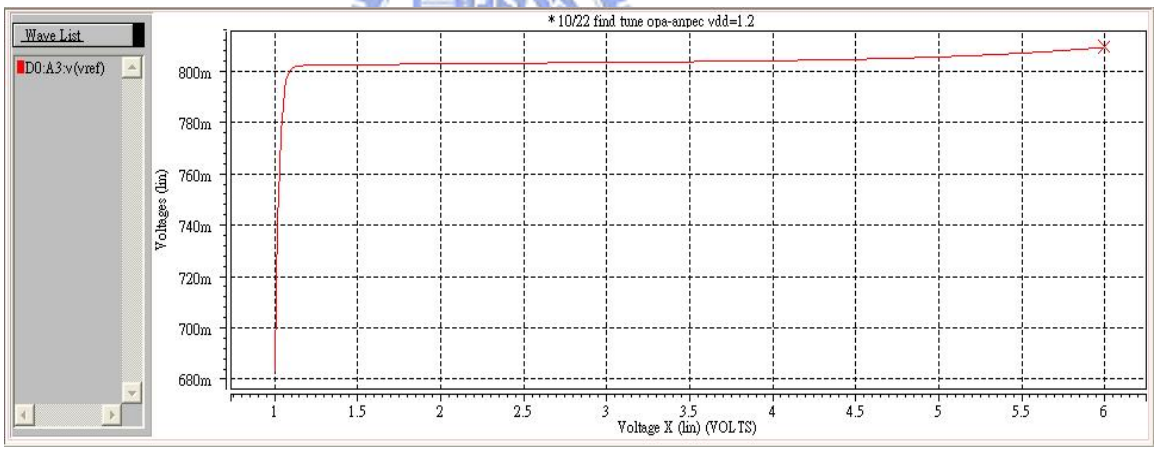


Fig. 4-16 Simulated Vref vs. Vdd of the simplified circuit of Type C

In fact, the bandgap circuit shown in the Fig. 4-15 can be simplified to the circuit with a folded-cascode OP-Amplifier as shown in Fig. 4-17. But we finally decided to choose the more complicated circuit (as shown in Fig. 4-15) because the simulation result show that the PSRR of the simplified circuit (as shown in Fig. 4-17) is not as good as the complicated one.

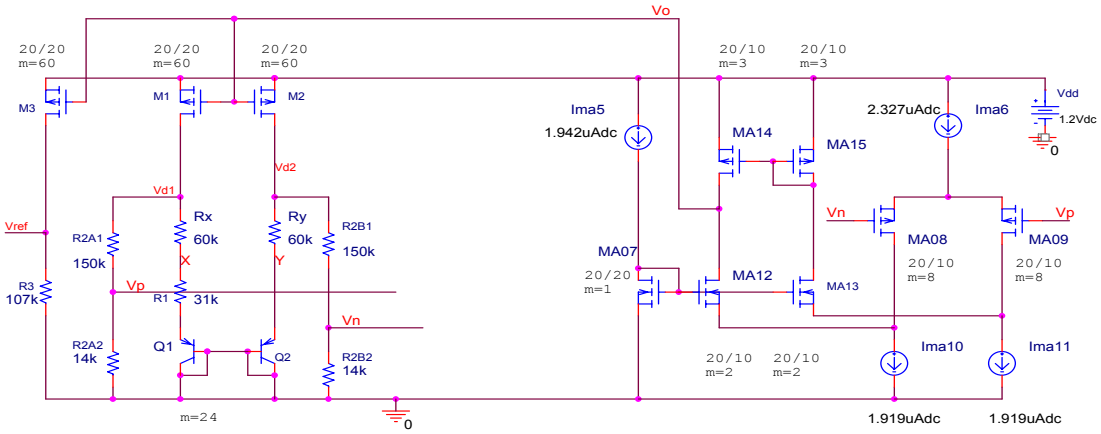


Fig. 4-17 Another bandgap circuit topology of Type C with a folded-cascode OP-Amplifier

4.2.3 Operational Amplifier Features of Type C and Type D

The simulated features of the two types of OP-Amplifier are summarized in Table-15.

Table-15 Operational Amplifier features of Type C and Type D

	Type C pMOS as the input stage	Type D nMOS as the input stage
DC Loop gain	60 dB	65 dB
Gain-Bandwidth product	9.0 MHz	7.8 MHz
Phase Margin	71.6°	63.6°
Supply Voltage	1.20 V	1.20 V

Chapter 5 CHIP LAYOUT DESCRIPTION AND EXPERIMENTAL RESULTS WITH TSMC 0.35μm CMOS PROCESS

5.1 Chip Layout Descriptions

Similarly, Fig. 5-1 show layout view of the Type D and Type C with TSMC 0.35μm Mixed-Mode double-poly-four-metal (2P4M) 3.3 / 5VCMOS technology. The bandgap reference circuits in Fig. 5-1 include the bandgap core circuit and OP-Amplifier. The chip area is 0.294 mm^2 for Type C and 0.238 mm^2 for Type D. The total transistor used on Type C is 33, and that of Type D is 23.

Again, both of the emitter areas of Q_1 are 24 times of the Q_2's. Since the mismatching of the same size MOS pairs makes the currents different, the same size MOS transistors are placed together to reduce these mismatching impact.

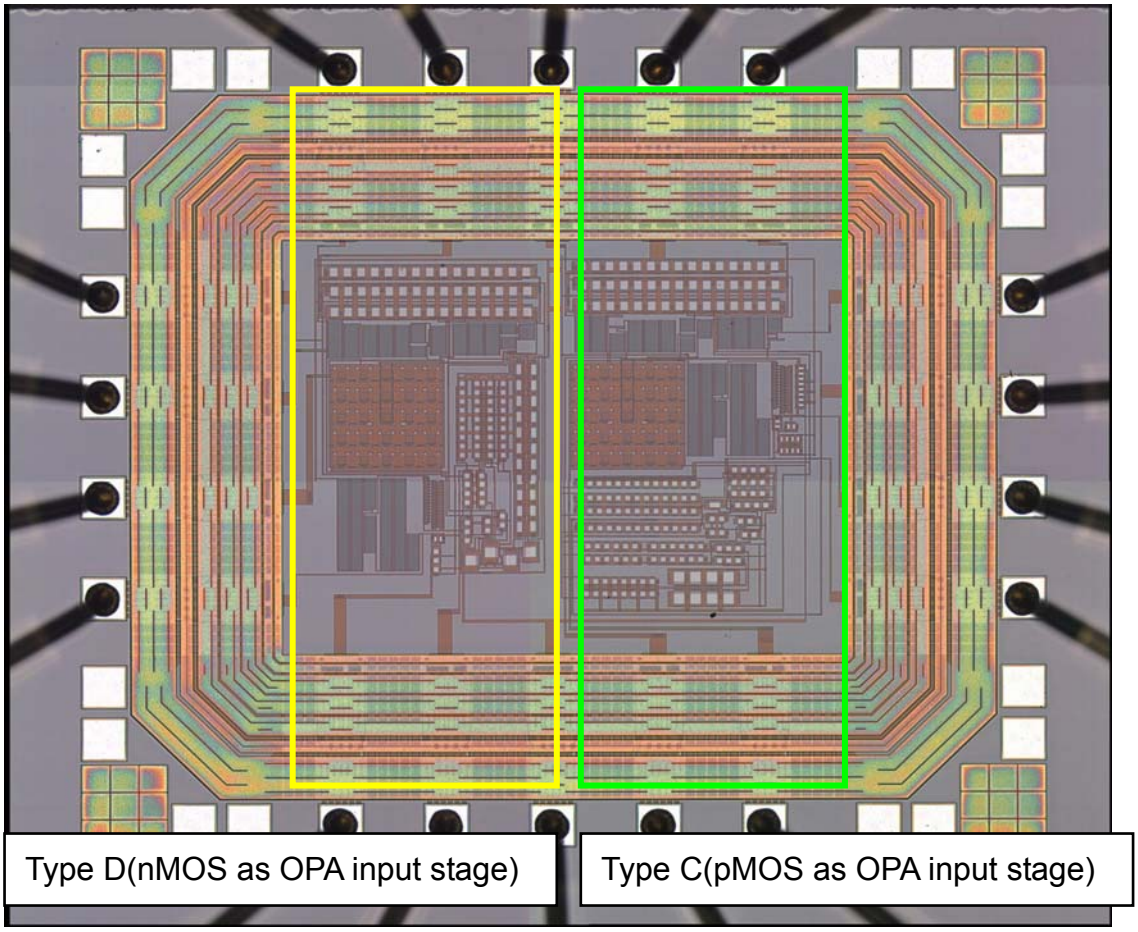


Fig. 5-1 The overall die photo of the Type D and Type C

Note：A standard I/O PAD developed by TSMC was chosen to use.

5.2 Measurement Setup

The measurement setup is the same with section 3.2.

5.3 Experimental Results

5.3.1 Experimental Results of Type D (nMOS as OPA input stage)

At first, we use voltage meter to measure the actual resistor values after fabrication, and the measurement result is shown in Table-16.

Table-16 Comparison of the design target and measured data of resistors of Type D circuit

Type D (n-diff. pair)			
Element name	Design target	Measured data	Tolerance
$R_{XN} + R_{AN} + R_{1N}$	N^+ diff 76.0k	71.6 k	- 5.8 %
$R_{XN} + R_{2AN}$	N^+ diff 174.0k	163.3k	- 6.1 %
$R_{YN} + R_{2BN}$	N^+ diff 174.0k	163.2k	- 6.2 %
R_{3N}	N^+ diff 111.0k	104.5k	- 5.9 %
$R_{S1N} + R_{S2N}$	P^+ diff 1100k	1082k	- 1.6 %

Substitute the measured resistor value into the bandgap circuit as shown in Fig. 5-2 and re-simulate the circuit again. Next compare the simulated result with the measured data.

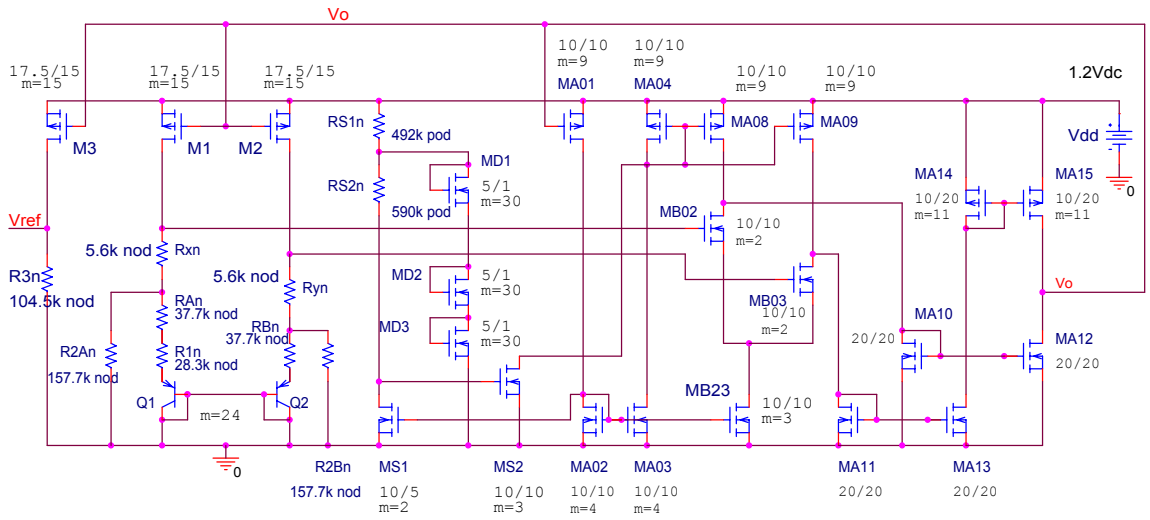


Fig. 5-2 Bandgap circuit of Type D with measured resistor values

PART (I) Vref (Reference Voltage) vs. Vdd

Measured Result of Type D

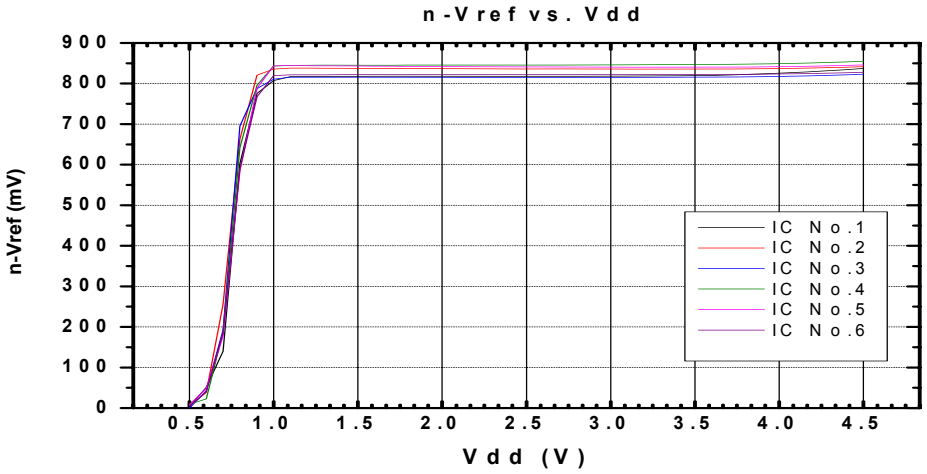


Fig. 5-3 Measured n-Vref vs. Vdd of Type D

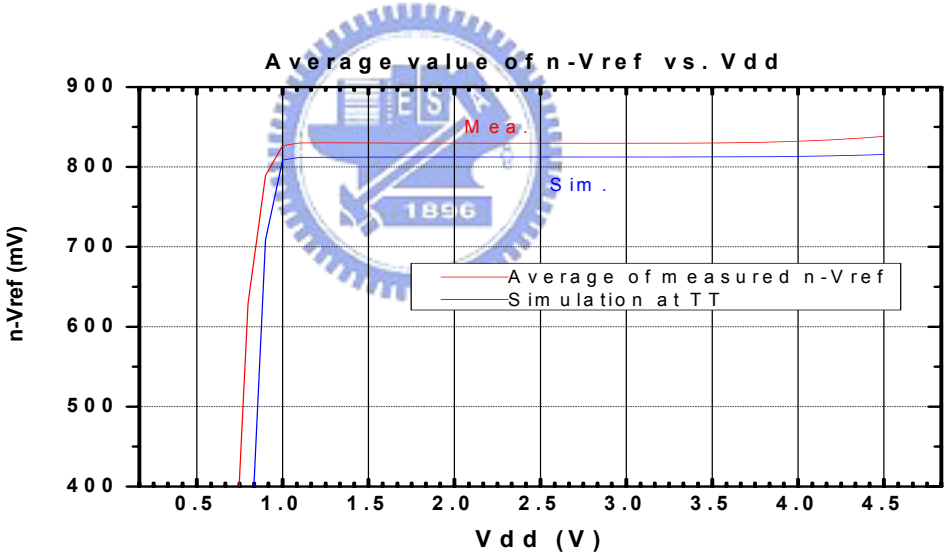


Fig. 5-4 Comparison of n-Vref vs. Vdd of Type D between simulation and measurement

Note : mean value = 829.5 mV

STD value = 12.8mV

PART (II) Temperature Compensation Curve

(1) Simulation Result of Type D at TT

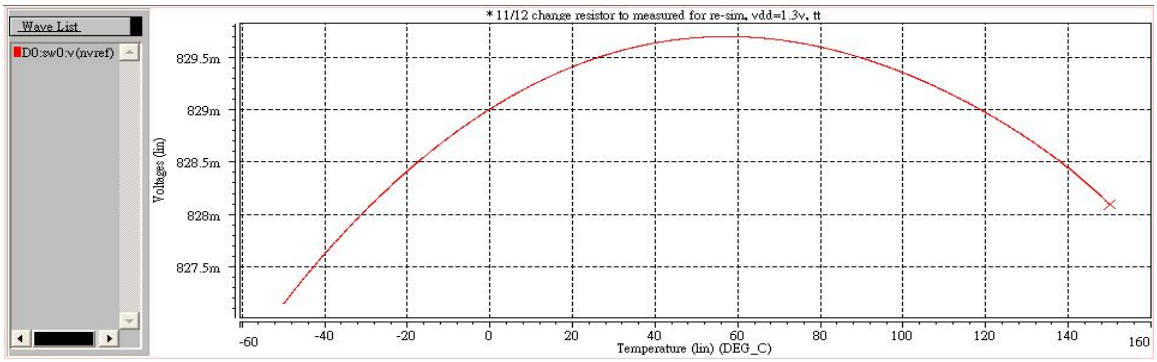


Fig. 5-5 Simulated TC curve of Type D under typical condition
axis X : temperature (℃) ; axis Y : n-Vref (mV)

At Vdd =1.3V from – 40 to 120℃

$$TC_{F(eff)} = \frac{1}{828mV}\left(\frac{829.7-827.7mV}{120-(-40)}\right) = 14.9ppm/℃$$

(2) Measured Result of Type D at Vdd = 3.0V, 2.0V, 1.3V

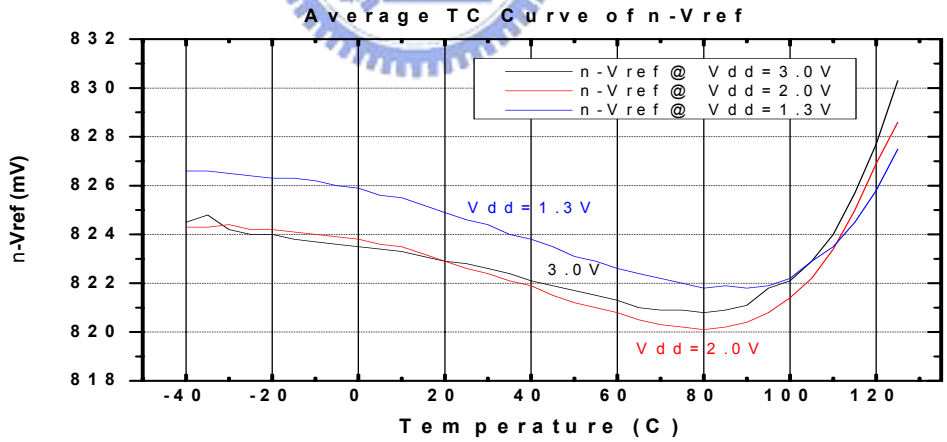


Fig. 5-6 Measured TC curve of Type D

At Vdd =1.3V，from – 40 to 120℃

$$TC_{F(eff)} = \frac{1}{824mV}\left(\frac{826.5-822mV}{120-(-40)}\right) = 34.1ppm/℃$$

(3) Experimental Results discussion

1. The $TC_{F(eff)}$ by Simulation is 15.0ppm/℃. The measured data of $TC_{F(eff)}$ is 34.1ppm/℃. It is acceptable.

2. It is at the General Case that we get $TC_{F(eff)}$ =34.1ppm/℃. Right now, we want to observe the extreme case, Vdd = 1.1V.

   At Vdd = 1.1V, we get the $TC_{F(eff)}$ =73.6 ppm/℃, as shown Fig. 5-7.

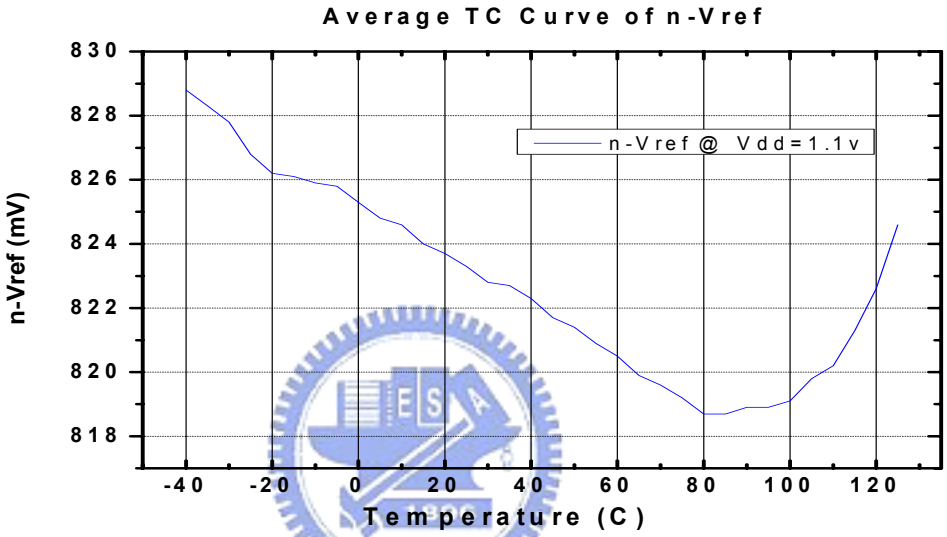
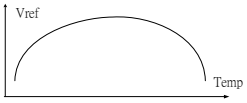


Fig. 5-7 Measured TC curve of Type D at the worst case

3. Next, we want to discuss an interesting phenomenon：

   Why do the measurement data of TC curve look like 

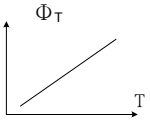
,

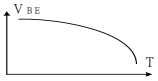
   rather than 

, which is presented by the simulation.

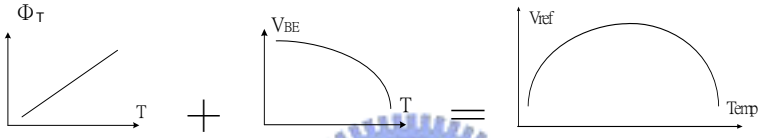
   We think this phenomenon is related with the TSMC 0.35μm device characteristic.

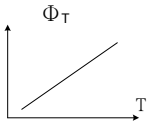
According to theory, two temperature-compensated currents create bandgap output reference voltage. One is the PTAT current (coming from the thermal voltage Φ_T)；the other is negative temperature coefficient current (coming from the V_{BE} voltage).

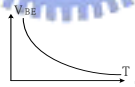
In general, the Φ_T vs. temperature curve is like 

；and the V_{BE} vs. temperature curve is like 

When Φ_T combine with the V_{BE}, the whole TC curve was dominated by Φ_T at low temperature and by V_{BE} at high temperature. So, we can get the curve as shown below.

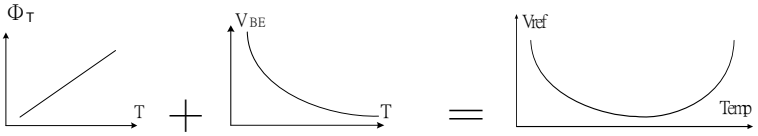


Right now, by the measurement result, we make an assumption that：for TSMC 0.35μm device, the Φ_T vs. temp. curve is still like 

, but the V_{BE} vs. temp. curve is like 

.

Based on this kind of assumption, when Φ_T combine with the V_{BE}, the whole TC curve was dominated by V_{BE} at low temperature and by Φ_T at high temperature. So, we can get the curve as shown below.



Next we want to verify the assumption by measure the temperature coefficient of V_{BE} and Φ_T respectively.

(i) Verify the assumption for the temperature coefficient of Φ_T

We verify the temperature coefficient of Φ_T by measuring the ΔV_{BE} .

Note : $\Delta V_{BE} = V_{BE1} - V_{BE2} = \Phi_T \ln(m)$

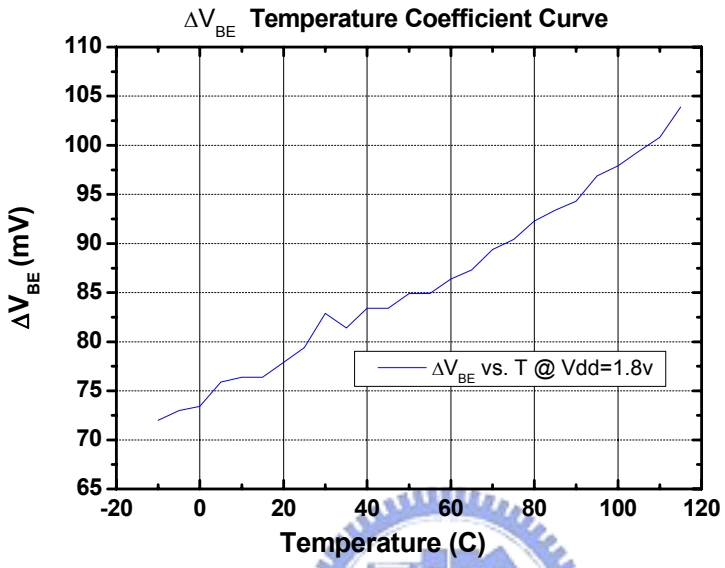
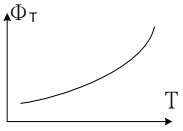


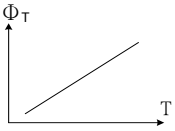
Fig. 5-8 ΔV_{BE} Temperature Coefficient Curve

For -10 ~ 80 ℃ : TC = $(\frac{92.3-72mV}{80-(-10)})$ = 0.225 Volt /℃

For 100 ~ 115 ℃ : TC = $(\frac{103.9-97.9mV}{115-(100)})$ = 0.4 Volt /℃

The temp coefficient of low temp ＜ The temp coefficient of high temp

So, the Φ_T vs. temp. curve is like 

, not as expect 

(ii) Verify the assumption by measuring the temperature coefficient of V_{BE}.

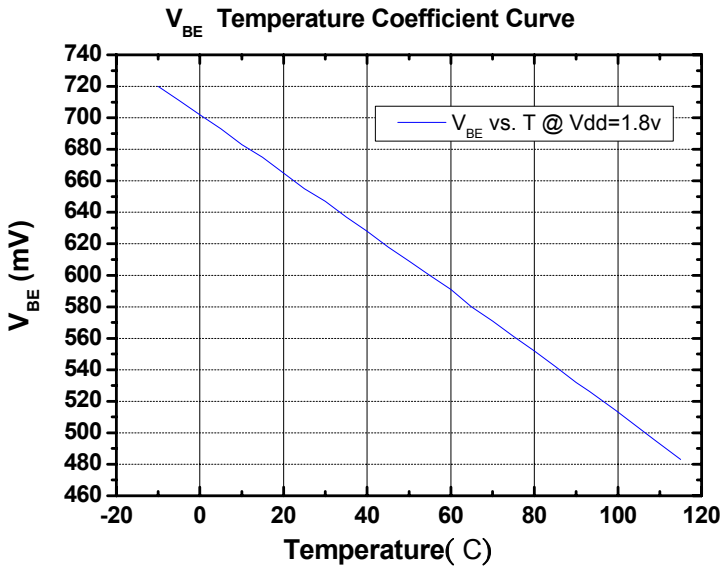
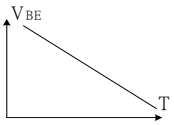


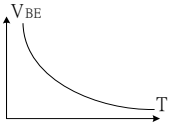
Fig. 5-9 V_{BE} Temperature Coefficient Curve

For –10 ~ 80 ℃ : TC = $(\frac{552-720mV}{80-(-10)})$ = - 1.866 Volt /℃

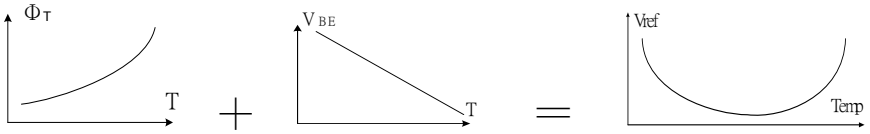
For 100 ~ 115 ℃ : TC = $(\frac{483-513mV}{115-(100)})$ = - 2 Volt /℃

The temperature coefficient for low temp. and high temp. are almost the same.

So, the V_{BE} vs. temp. curve is like 

, not as expect 

Although the temperature coefficients of Φ_T and V_{BE} do not meet our expectation, however, it can prove that the whole TC curve is affected by the temperature coefficient of thermal voltage (Φ_T) and result in the case that the curve face upward.



Put the measured data from Fig. 5-8 and Fig. 5-9 into (5.1), we can get the similar measured TC curve as shown in Fig. 5-10

$$V_{REF} = \frac{R_3}{R_1}(\Delta V_{BE}) + \frac{R_3}{R_1}(1 + \frac{R_{A2}}{R_{A1}})V_{os} + V_{EB2}(\frac{R_3}{R_{B1} + R_{B2}}) \quad (5.1)$$

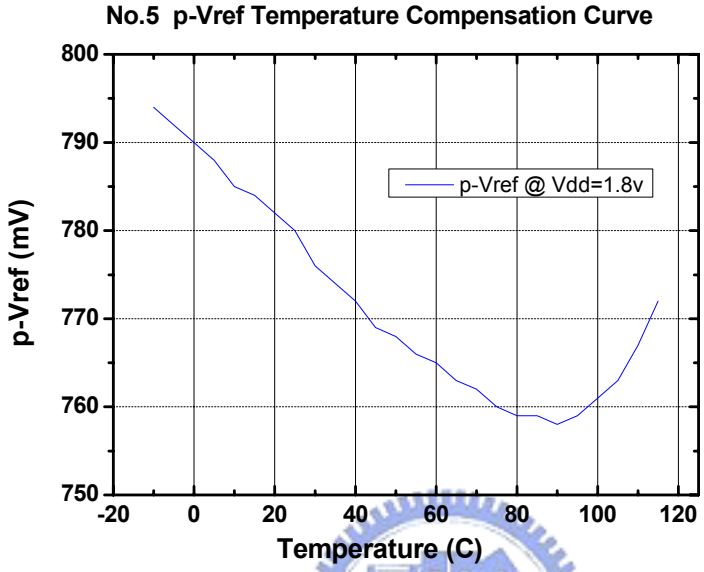


Fig. 5-10 Measured TC curve of Type C - No.5 p-Vref

PART (III)　Transient Response

(1) Simulation Result of Type D at TT

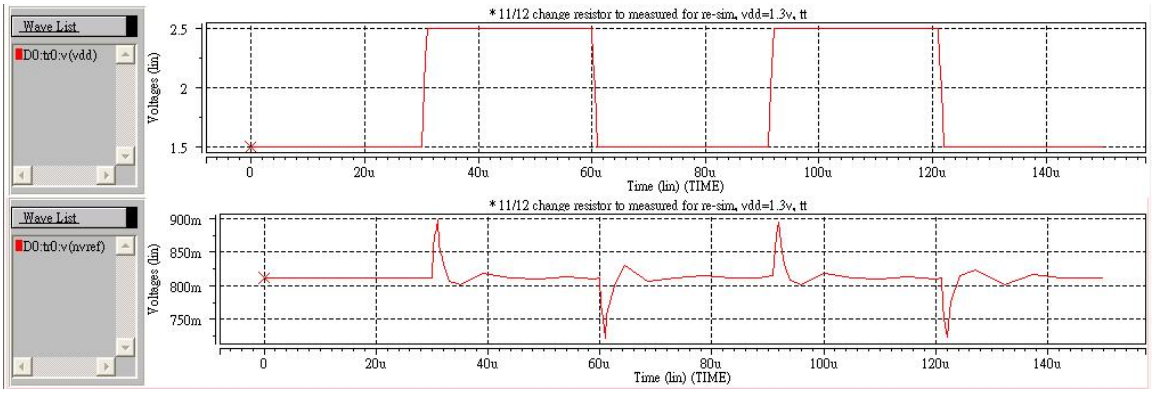


Fig. 5-11　Simulated transient response of Type D under typical condition
upper axis X : time (sec) ; axis Y : Vdd (V)
lower axis X : time (sec) ; axis Y : n-Vref (mV)

(2) Measured Result of Type D at AC mode

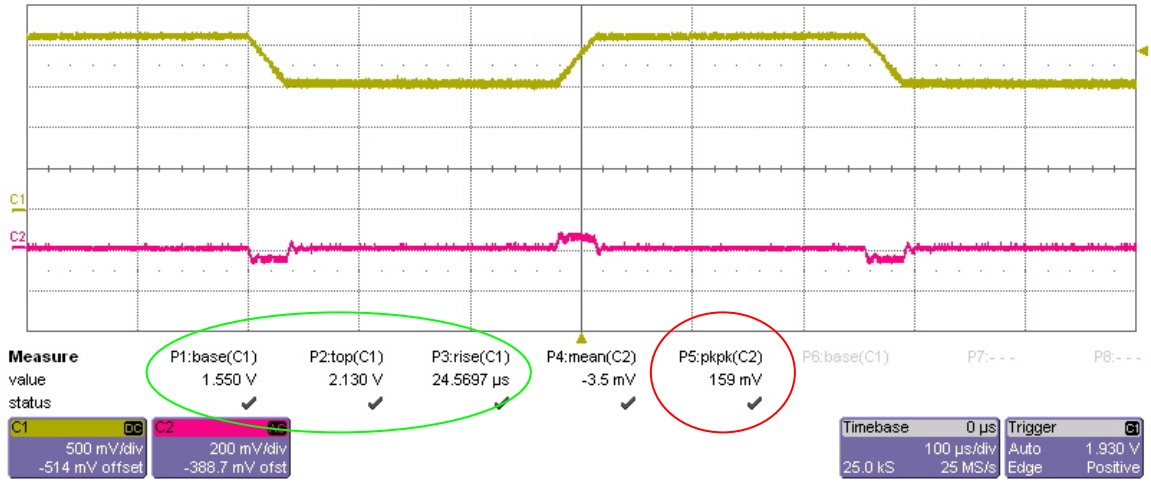


Fig. 5-12　Measured transient response of Type D at AC mode
upper axis X : time (sec) ; axis Y : Vdd (V)
lower axis X : time (sec) ; axis Y : n-Vref (mV)

Description：

1. The input signal (marked by the yellow curve) is shown on the DC mode but the output reference voltage (marked by the red curve) is shown on the AC mode.
2. The input voltage varies between 1.550V and 2.130V. The rise time ≒ 24.5us (as shown on the green circle), and the peak to peak voltage of the output reference voltage ≒ 159mV (as shown on the red circle).

PART (IV)　PSRR (Power Supply Rejection Ratio)

(1) Simulation Result of Type D under typical condition and Vdd =1.3V

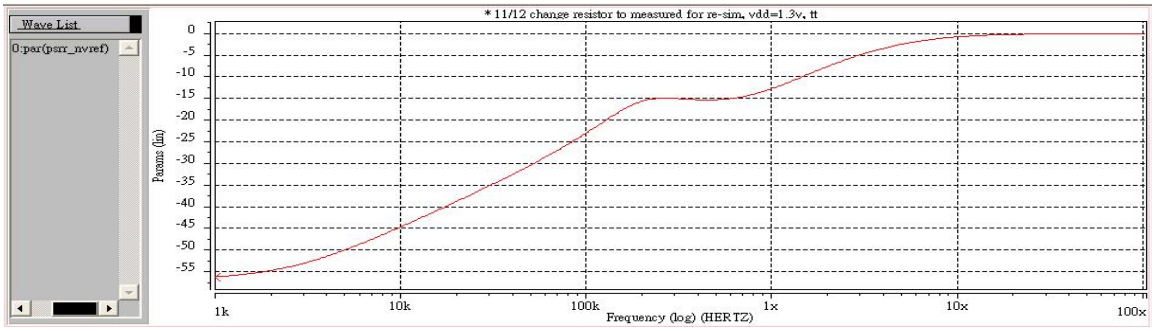


Fig. 5-13　Simulated PSRR of Type D under typical condition
axis X : frequency (Hz) ; axis Y : PSRR of n-Vref (dB)

(1) Measured Result of Type D by using Oscilloscope at Vdd = 1.5V, 2.0V

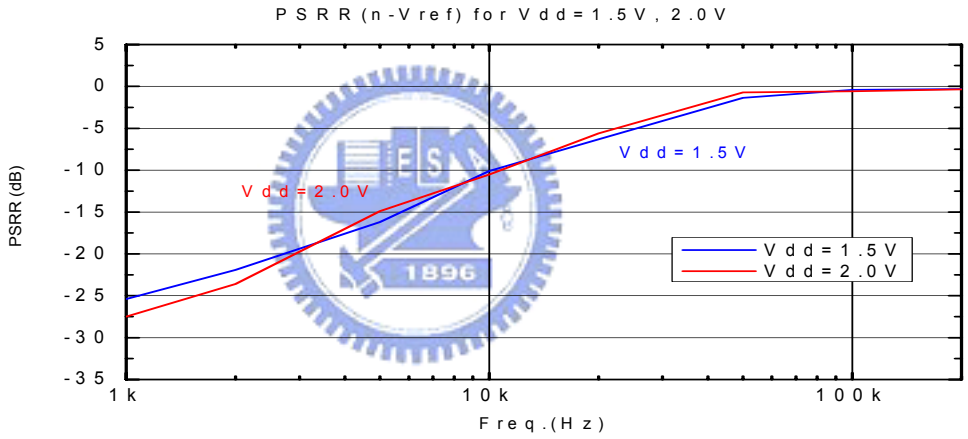


Fig. 5-14　Measured PSRR of Type D

(2) Comparison：Simulation versus Measurement as shown in Table-17.

Table-17　Summary table of PSRR of Type D at Vdd = 1.5V

PSRR	1KHz	5KHz	10KHz	50KHz	100KHz
Simulation	-52dB	-50dB	-45dB	-30dB	-23dB
Measurement	-25dB	-16dB	-10dB	-0.68dB	-0.42dB

(4)　Experimental Results discussion

The PSRR performance is not as good as we expect. We guess the reason of the poor PSRR performance may be related with the parasitic resistor and parasitic capacitance.

5.3.2 Experimental Results of Type C (pMOS as OPA input stage)

We use voltage meter to measure the actual resistor values after fabrication, and the measurement result is shown in Table-18.

Table-18 Comparison of the design target and measured data of resistors of Type C circuit

Type C (p-diff. pair)			
Element name	Design target	Measured data	誤差
$R_{2A1P} + R_{1P}$	N^+ diff 182.0k	171.4k	- 5.8 %
R_{2A2P}	N^+ diff 30.0k	28.4k	- 5.3 %
R_{2B2P}	N^+ diff 30.0k	28.4k	- 5.3 %
R_{2B1P}	N^+ diff 155.0k	146.1k	- 5.7 %
R_{3P}	N^+ diff 120.0k	113.1k	- 5.8 %
$R_{S1P} + R_{S2P}$	P^+ diff 1100k	1087k	- 1.2 %

Substitute the measured resistor value into the bandgap circuit as shown in Fig. 5-15 and re-simulate the circuit again. Next compare the simulated result with the measured data.

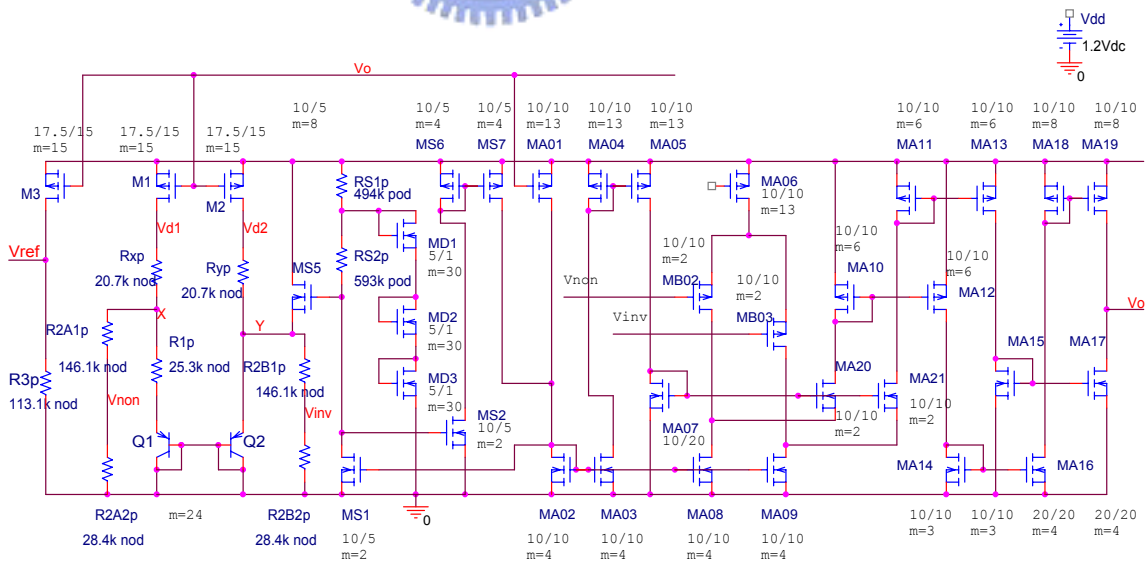


Fig. 5-15 Bandgap circuit of Type C with the measured resistor values

PART (I) Reference Voltage (Vref) vs. Vdd

(1) Measured Result of Type C

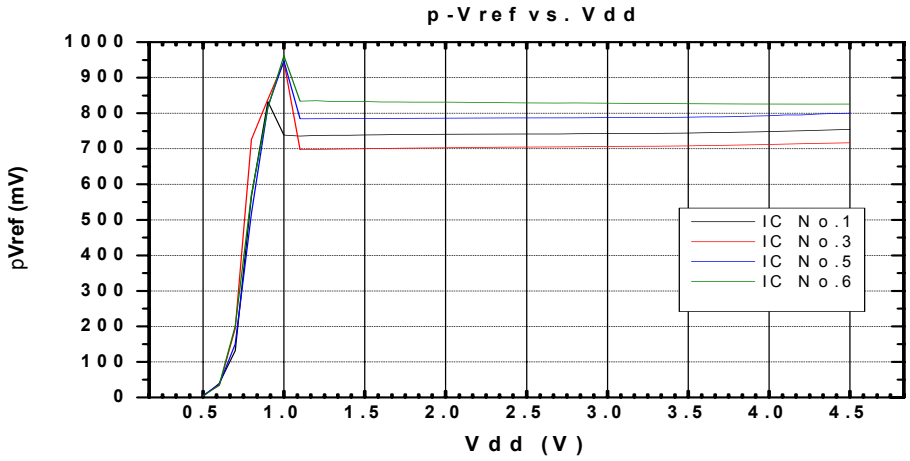


Fig. 5-16 Measured p-Vref vs. Vdd of Type C

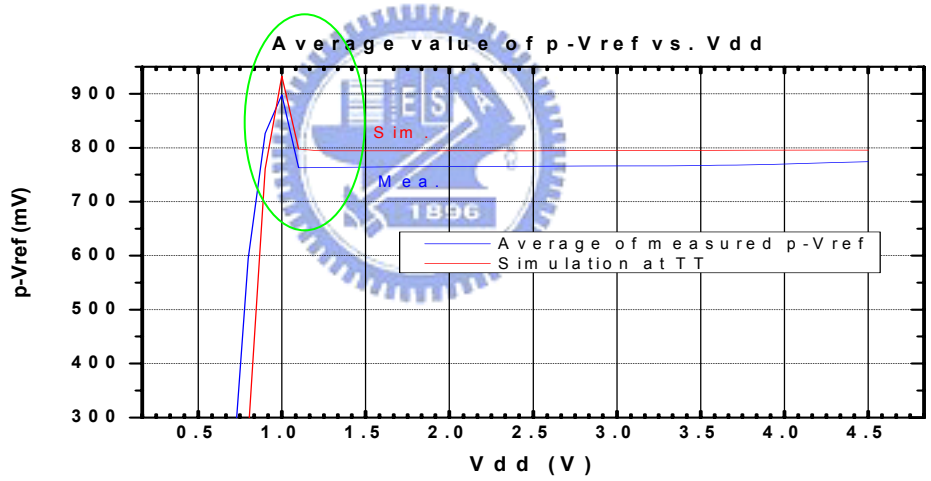


Fig. 5-17 Comparison of p-Vref vs. Vdd of Type C between simulation and measurement

Note ：mean value = 766.1 mV; STD value = 53.6 mV

(3) Experimental Results discussion

1. From Fig. 5-17, we see that, no matter simulation or measurement, p-Vref $\fallingdotseq$ 900mV when Vdd = 1.0V (as shown on the green circle). This phenomenon will not present on the n-Vref circuit. The reason is that when Vdd $<$ 1.0V, the OPA of the p-Vref bandgap circuit can not work at normal condition. A current sources (MA06, as shown in Fig. 5-15), which is responsible to provide the pMOS differential pairs a stable biased current, will go into the triode region. That will induce an abnormal output reference current, resulting in a peak value shown on the output reference voltage waveform.

The correspondent OPA of the n-Vref circuit will not have this kind of phenomenon. Even though Vdd = 1.0V, its current source (MB23, as shown in Fig. 5-2), which is responsible to provide the nMOS differential pairs a stable biased current, is still working on the saturation region. This is another advantage of the n-Vref bandgap circuit.

PART (II) Temperature Compensation Curve

(1) Simulation Result of Type C at TT

Fig. 5-18 Simulated TC curve of Type C under typical condition
axis X : temperature (℃) ; axis Y : p-Vref (mV)

At Vdd =1.3V from – 40 to 120℃, $TC_{F(eff)}$ ＝15.8ppm/℃

(2) Measured Result of Type C

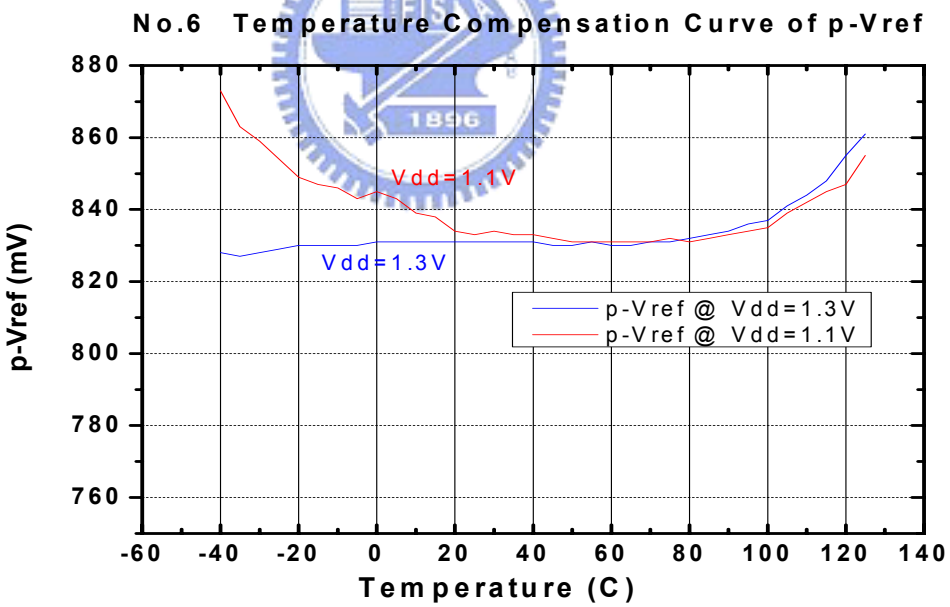


Fig. 5-19 Measured TC curve of Type C

At Vdd =1.3V, $TC_{F(eff)} = \frac{1}{831mV}\left(\frac{837-828mV}{100-(-20)}\right)$=90.2ppm/℃, from – 20 to 100℃

At Vdd =1.1V, $TC_{F(eff)} = \frac{1}{834mV}\left(\frac{847-831mV}{120-(-20)}\right)$=137 ppm/℃, from – 20 to 120℃

PART (III) Transient Response

(1) Simulation Result of Type C at TT

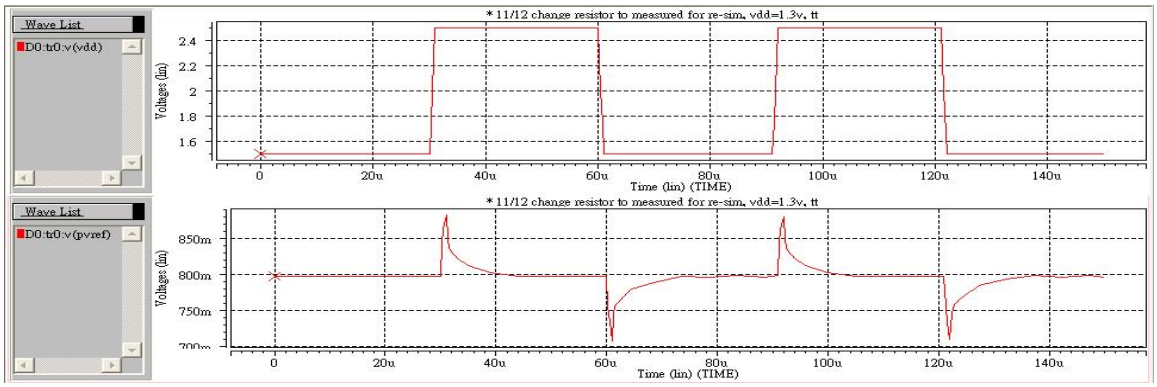


Fig. 5-20 Simulated transient response of Type C under typical condition
upper axis X : time (sec) ; axis Y : Vdd (V)
lower axis X : time (sec) ; axis Y : p-Vref (mV)

(2) Measured Result of Type C at AC mode

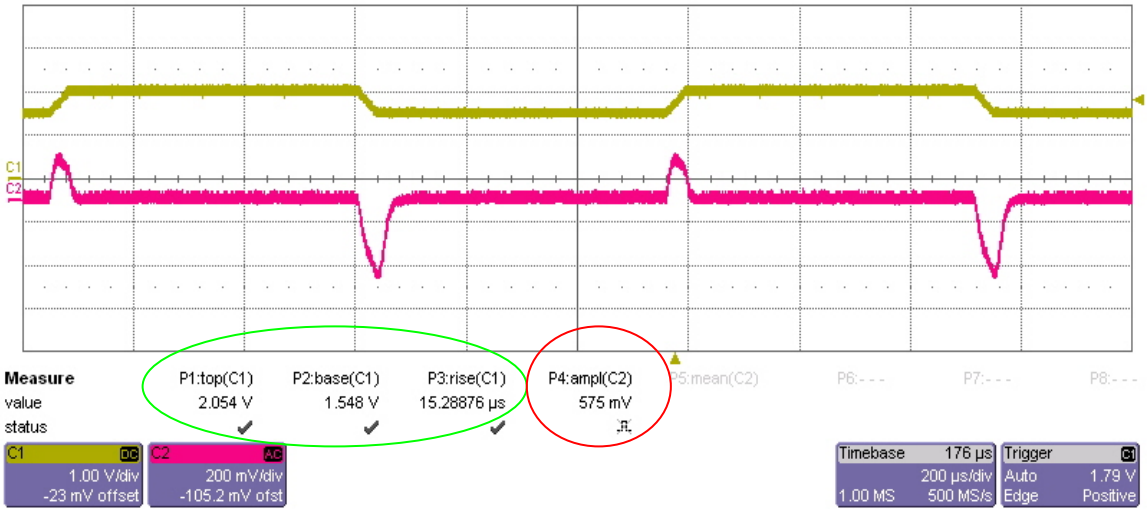


Fig. 5-21 Measured transient response of Type C at AC mode
upper axis X : time (sec) ; axis Y : Vdd (V)
lower axis X : time (sec) ; axis Y : p-Vref (mV)

Description:

1. The input signal (marked by the yellow curve) is shown on the DC mode but the output reference voltage (marked by the red curve) is shown on the AC mode
2. The input voltage varies between 1.548V and 2.054V. The rise time ≒ 15.3us (as shown on the green circle). The peak to peak voltage of the output reference voltage ≒ 575mV (as shown on the red circle).

PART (IV)　PSRR (Power Supply Rejection Ratio)

(1) Simulation Result of Type C under typical condition and Vdd = 1.3V

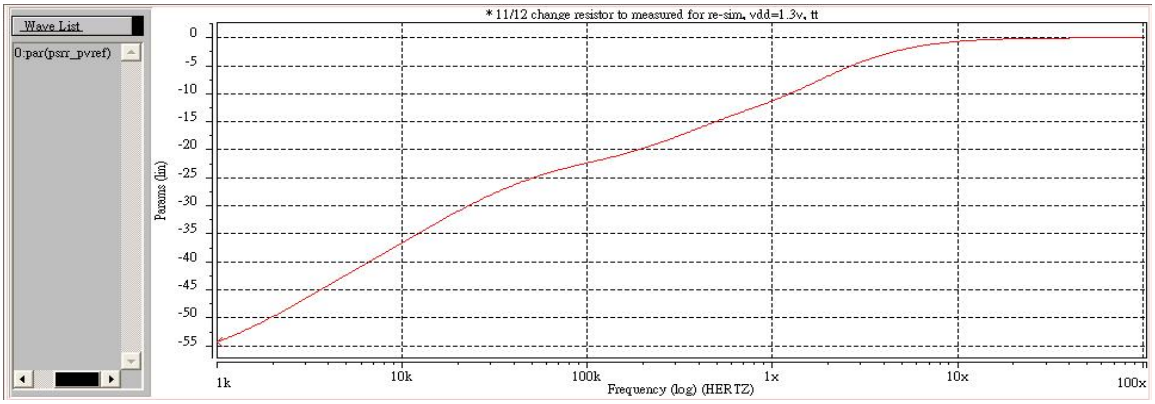


Fig. 5-22　Simulated PSRR of Type C under typical condition
axis X : frequency (Hz) ; axis Y : PSRR of p-Vref (dB)

(2) Measured Result of Type C by using Oscilloscope at Vdd = 1.5V, 2.0V

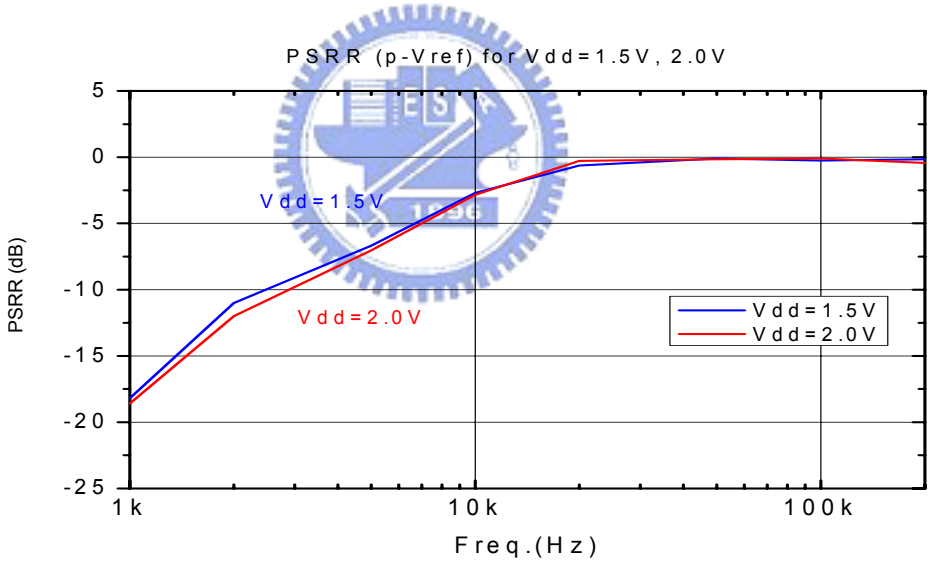


Fig. 5-23　Measured PSRR of Type C

(3) Comparison　：Simulation versus Measurement as shown in Table-19.

Table-19　Summary table of PSRR of Type C at Vdd = 1.5V

PSRR	1KHz	5KHz	10KHz	50KHz	100KHz
Simulation	-55dB	-42dB	-36dB	-25dB	-22dB
Measurement	-18dB	-6.7dB	-2.7dB	-0.26 dB	-0.1 dB

Chapter 6 CONCLUSIONS AND FUTURE WORKS

6.1 Conclusions

According to the theory and simulated data, we think if the OP-Amplifier's input stage can be implemented by using nMOS, the bandgap circuit performance will be better. Now this assumption has been verified by the measurement result. It is clear that bandgap circuit with nMOS differential pairs will have better performance and enable lower cost due to reduced chip area no matter TSMC 0.18μm process or TSMC 0.35μm process.

(1) Output Reference Voltage vs. Vdd:

For TSMC 0.18μm, the STD value of Type A (pMOS as OPA input stage) is 42.6 mV as shown in Fig. 3-6；however, The STD value of Type B (nMOS as OPA input stage) is only 7.3mV as shown in Fig. 3-15. So, Type B circuit is superior to the Type A.

For TSMC 0.35μm, the STD value of Type C (pMOS as OPA input stage) is 53.6 mV as shown in Fig. 5-17 ; however, The STD value of Type D (nMOS as OPA input stage) is only 12.8mV as shown in Fig. 5-4. So, Type D circuit is superior to the Type C.

(2) Temperature Compensation Curve:

For TSMC 0.35μm, the $TC_{F(eff)}$ of Type D is only 34.1 ppm/℃ as shown in Fig. 5-6；however, That of Type C is 90.2 ppm/℃ as shown in Fig. 5-19. So, Type D circuit is superior to the Type C.

(3) Transient Response:

For TSMC 0.18μm, after comparing Fig. 3-10 and 3-21, we can see that Type B is obviously superior to the Type A.

For TSMC 0.35μm, after comparing the measured waveform of Type D as shown in Fig. 5-12 with the correspondent waveform of Type C as shown in Fig. 5-21, we see that at the same test environment the peak to peak voltage of Type D is equal to 159mV ; the peak to peak voltage of Type C is equal to 575mV. So, the transient response of Type D is superior to the transient response of Type C.

(4) PSRR (Power Supply Rejection Ratio):

For TSMC 0.18μm, by comparing Fig. 3-13 and 3-24, we can see that Type B circuit is superior to the Type A.

For TSMC 0.35μm, by comparing Fig. 5-14 and 5-23, we can see that Type D circuit is superior to the Type C.

6.2 Future Works

Nowadays, the bandgap reference circuits have been widely used in battery-operated portable application. As the coming of deep-submicron technology and the low supply voltage, the demand for the low voltage and low power of bandgap reference circuits have been on the increase.

The minimum supply voltage of the conventional BGR circuits is constrained by two factors. One is the output reference voltage that is around 1.25V, equal to the silicon energy gap measured in electron volts. The other is the low operating voltage of operational amplifier. The first constrain have been solved by the resistive subdivision methods. As for the second constrain, we use low threshold voltage devices to lower the OPA's operating voltage. But, the input common-mode voltage of the OP-Amplifier is still an issue when we try to design the low-voltage bandgap core circuit. In other words, the input common-mode voltage of the amplifier limits the low-voltage design of the bandgap core circuits. In the future, the proposed circuits can be modified and improved in these directions.

Besides, the PSRR (Power Supply Rejection Ratio) is another important factor to evaluate the performance of the bandgap reference circuit. In this paper, the effort that we put to study the impact of device parameters on the performance of PSRR is not enough. In the future, this can be another study topic.

Finally, the chip size is another concern in IC design industry. In this thesis, the layout area of the all the proposed circuits is a little bigger than expected, although not bigger than those proposed by the other papers. In the future, the proposed circuits can be improved in these directions.

REFERENCES

[1] P. Malcovati, F. Maloberti, M. Pruzzi and C. Fiocchi, “Curvature Compensated BiCMOS Bandgap with 1 V Supply Voltage,” in Proc. ESSCIRC’ 2000, pp. 52-55.

[2] J. Doyle, Y. J. Lee, Y. B. Kim, H. Wilsch, and F. Lombardi, “A CMOS Subbandgap Reference Circuit with 1-V Power Supply Voltage,” IEEE Journal of Solid-State Circuits, vol. 39, No. 1, January 2004.

[3] K. N. Leung, and P. K. T. Mok, “A Sub-1-V 15-ppm/℃ CMOS Bandgap Voltage Reference Without Requiring Low Threshold Voltage Device,” IEEE Journal of Solid-State Circuits, vol. 37, No. 4, April 2002.

[4] P. R. Gray, et al., Analysis and Design of Analog Integrated Circuits, 4th ed. pp. 326, New York : Wiley, 2001.

[5] B. Razavi, Design of Analog CMOS Integrated Circuits, pp. 386, Boston, MA : McGraw-Hill, 2001.

[6] D. A. Johns and K. Martin, Analog integrated circuit design, pp. 358, MA : John Wiley & Sons, 1996.

[7] Y. Jiang and E. K. F. Lee, “Design of low-voltage bandgap reference using transimpedance amplifier,” IEEE Trans. Circuits Syst. II, vol. 47, pp. 552-555, June 2000.

[8] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, “A CMOS bandgap reference circuit with sub-1-V operation,” IEEE Journal of Solid-State Circuits, vol. 34, No. 5, pp. 670-674, May 1999.

[9] M. Ferro et al., “A floating CMOS bandgap voltage reference for differential application,” IEEE Journal of Solid-State Circuits, vol. 24, No. 3, pp. 690-697, June 1989.

[10] A. Boni, “Op-Amps and Startup Circuits for CMOS Bandgap References With Near 1-V Supply,” IEEE J. Solid-State Circuits, vol. 37, No. 10, October 2002.

[11] K. E. Kuijk, “A precision reference voltage source,” IEEE Journal of Solid-State Circuits, vol. SC-8, pp. 222-226, June 1973.

[12] B. S. Song and P. R. Gray, “A precision curvature-compensated CMOS bandgap reference,” IEEE Journal of Solid-State Circuits, vol. SC-18, No. 6, pp. 634-643, December. 1983.

[13] S. L. Lin and C. A. T. Salama, “A Vbe(T) model with application to bandgap reference design,” IEEE Journal of Solid-State Circuits, vol. SC-20, pp. 1283-1285, December 1985.

[14] G. Giustolisi, “A Low-Voltage Low-Power Voltage Reference Based on Subthreshold MOSFETs,” IEEE Journal of Solid-State Circuits, vol.38, No. 1, January 2003.

[15] S. M. Sze, Semiconductor Devices Physics and Technology, pp. 12-13, Wiley, 1985.

[16] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. pp. 28-29, Wiley, 1985.

[17] H. Neuteboom, B. M. J. Kup, and M. Janssens, “A DSP-based hearing instrument IC,” IEEE Journal of Solid-State Circuits, vol. 32, pp. 1790-1806, November 1997.

簡　歷

姓 名：　王冀康

學 歷：

國立新竹高級中學　　（73年9月~76年6月）

國立交通大學機械工程學系　　（76年9月~80年6月）

國立交通大學電子工程研究所碩士班　（92年9月~95年6月）