Chapter 1
Introduction

1.1 General Background and Motivation

Low temperature polycrystalline silicon (LTPS) thin film transistors (TFT's) have received much attention in recent years because of their increasing use in pixel transistors and integrated river circuitry on large area flat panel displays (FPD), such as active-matrix liquid crystal displays (AMLCD)[1.1]-[1.3] and active-matrix organic light emitting diodes(AMOLCD)[1.4]-[1.6], and solar cells. The ability of fabricating high-performance LTPS TFT enables their use in a wide range of new applications. Therefore, there is great interest in improving the performance of LTPS TFT's.

The study of polycrystalline silicon (poly-Si) thin film transistors (TFT's) fabricated using a maximum temperature below 600℃ commenced in 1980s. The original motivation of this concept was to replace quartz with low-cost glass for active matrix display application. This would make large-area high-definition active matrix displays more practical and less expensive. But .the present first generation of AMLCD relies predominately upon a-Si:H TFT for the pixel switching devices. The a-Si :H film exhibits high OFF-state impedance which can reduce the leakage current of TFT's. Unfortunately, the extremely low field-effect mobility(typically below 1cm^2/V*sec) in a-Si:H TFTs limits the technology from being developed to form integrated drive on the active matrix plate. On the country, the electron mobility of low-temperature poly-Si thin-film-transistors (TFTs) is about 100 times larger than that of the conventional amorphous silicon TFTs. So the low-temperature processed polycrystalline-silicon (poly-Si) has been widely investigated as a material for mobile

applications such as digital cameras [1.7] and notebook computers. High field-effect mobility implies higher drive current. The high drive current allows smaller TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance.[1.8]

Because low-temperature technology is required on inexpensive glass substrates, since the maximum process temperature is limited to less than 600 C. A variety of technology have been investigated for the poly-Si, including solid phase crystallization(SPC) [1.9],eximer laser crystallization(ELC) [1.10],rapid thermal annealing(RTA)[1.11] and metal-induced crystallization(MIC) [1.12]. SPC is the mostly common method to form poly-silicon active layer. SPC have inexpensive batch process, but it processing temperature of around 600℃ still exceeds the upper temperature limit of glass substrates and cause high thermal budget. RTA is a high temperature process(>600℃) and the films contain high densities of defects. ELC have low temperature process and low defect densities within grains. However, it takes high cost, high process complexity; a narrow process windows, and high surface roughness. MIC is superior because, unlike LC, it is a low-cost batch process and unliked SPC, better quality poly-Si thin films can be obtained. Moreover, it’s also simple to control grain orientation using silicide as a seeding agent to crystallize amorphous silicon films. Utilizing this method, we get the device performance that will be discussed later.

The poly-Si TFTs require not only high on-state current but also low leakage current and long-term reliability. So several degradation mechanisms have been proposed [1.13]-[1.15]:(1) hot-carrier degradation;(2) trapping of carriers by gate bias;(3) creation of defects either by hot carrier or by gate bias. Hot-carrier degradation in poly-Si TFT is similar to that in a single-crystal Si MOSFET, where a combination of interface state creation and carrier trapping in the oxide give the

degradation in the performance. Such effects are only seen at high drain bias, where the carrier can attain sufficient energy from the field to be injected into the gate oxide and/or defect creation at the interface[1.16], [1.17].To suppress the leakage current resulting from the high electric field of drain junction, an offset-gate structure and lightly doped drain (LDD) TFTs have been widely used[1.18][1.19].This is because the anomalous current leakage current is resulted in the high electric field near the drain junction. So the reduction of electric field near the drain junction by using LDD can also enhance the hot carrier endurance of poly-Si TFTs[1.20]. Although using the LDD structure can effectively suppress leakage current and enhance device reliability, however, this LDD structures suffer from high parasitic S/D resistance which leads to a severe on-current reduction [1.21].

Another kind of LDD structure, which is called gate-overlapping LDD, was proposed[1.21]-[1.24].Instead the LDDs are outside the gate edges, the GOLDD structure puts the LDDs under the gate edges. The GOLDD TFT device exhibits much lower leakage current, higher on/off current ratio and better hot carrier stress endurance than conventioal TFTs due to the lower electric field generated by graded LDD dopant profile. The stability of device characteristics after a long-term operation is indispensable for circuit applications. These reliability issues arise from either weak Si-Si/Si-H bonds in the channel region or the hot carriers induced by the intense drain electric field. We demonstrated an elevated channel with gate-overlapped LDD structure to address the reliability problems while gain some other benefits including high mobility, suppressed kink phenomenon, low leakage current and reduced contact resistances through the proposed architecture.

The enhancement of crystallization of the a-Si films and thus lowering of the crystallization temperature, called “metal induced crystallization (MIC)”, have been reported to be induced by two kinds of metal-induced process. One involves a metal

forming a eutectic with Si and the other involves silicide-forming metals. For the former case, metal atoms dissolved in a-Si films may weaken Si bonds and enhance nucleation of crystalline Si.[1.25] For the latter case, the origin of the enhancement has not been clearly revealed but a thin epitaxial silicide phase is thought to act as a nucleus for Si crystallization.[1.26].However, in spite of low crystallization temperature, metal contamination is a serious problem in metal induced crystallized poly-Si. In order to reduced the metal contamination, some people have fabricated poly-Si using the metal solution or by deposition ultra-thin discrete metal layer on a-Si[1.27][1.28]. Recently, metal-induced lateral crystallization (MILC) was proposed, which successfully eliminate Ni-incorporation in grown poly-Si films [1.29]. This resulted in a successful fabrication of high-performance TFT0. However, growth velocity of MILC is so slow that long annealing time of 20 h is necessary to obtain large grains (approx. 10 um) at 500 C[1.12] . We confer that the electrical characteristic of the MILC poly-Si TFT's are used a SiN_x nanocap layer between a-Si and Ni layer. This method may have merit such as nondirect contact of metal to a-Si and the reduction of metal impurities in poly-Si[1.30][1.31]. The paper[1.32] are proposed that the Ge doped in a-Si can enhance the velocity. So we also confer that the electrical characteristic of the MILC poly-Si TFT's with Ge layer.

1.2 Thesis Organization

In this thesis, we made efforts on GOLDD with elevated channel and metal induced lateral crystallization (MILC) with SiN_x layer or Ge layer. Chapter 1 describes the background and motivation.

In chapter 2, a elevated-channel TFT structure as described was fabricated and the recrystallization method was MILC. Here, we changed the thickness of active area ranging from 15 nm to 100 nm, and also varied the impurity concentration of the

lightly-doped regions. Detailed electrical characteristics were examined to figure out the effects of active layer thickness and LDD dosages.

In chapter 3, Si_3N_4 nanocap layer as filter and Ge layer is applied to fabricate MILC poly-Si TFT's. And the device performance of different annealing temperature are discussed.

As last, in chapter 4, a conclusion is given for this thesis, and some future works extended form our investigation are proposed.