Chapter 2

Poly-Si TFTs with Elevated Channel and Gate Overlapped Structure by Metal-Induced Lateral Crystallization

2.1 Introduction

Poly-Si TFT's are required for active matrix liquid crystal displays with integrated peripheral circuits and pixel transistors [2.1].However, conventional TFTs have several undesired effects, including large OFF-state leakage current, anomalous drain current increase at high source-drain voltages, the so-called kink effect, and electrical instabilities after long term operation [2.2].A common method to reduce the anomalous leakage current of poly–Si TFT's is to reduce the electric field near the drain junction. So, an offset or lightly doped drain (LDD) structure has been used to reduce the leakage current and enhance device reliability by suppressing the electric field near the drain junction [2.3][2.4].However, these structure might degrade the device driving capability due to the large series resistance existing in the LDD regions [2.5].In order to avoid the disadvantage of increasing series resistance occurring in LDD TFT's, gate-overlapped LDD structure[2.6][2.7] has been adopted. The GOLDD poly-Si TFT exhibited lower leakage current and suppressed kink effect while a high on-state current remains.

In this chapter, we will discuss a novel thin-film transistor structure with thin channel region. Poly-Si TFT with thin channel layers are known to have some effects like MOSFET's with thin channel layers.[2.8][2.9].These advantages include high mobility, kink elimination, saturation current enhancement, and steeper subthreshold

slope. The recrystallization method of a-Si was metal-induced lateral crystallization instead of solid-phase crystallization (SPC).Because by using SPC, the grain size decrease dramatically as the film thickness of poly-Si film decreasing[2.9]. Comparing to SPC, the MILC method provides a flat poly-Si surface even with very thin film and a very large grain size. So it is potential for fabricating high performance TFTs with MILC[2.10], [2.11].

So in this chapter, we'll combining the gate overlapped light-doped drain and elevated channel structures[2.18][2.19], called elevated-channel thin-film transistor (ECTFT) structure. And this ECTFT structure with different active layer thickness are made an experiment. Furthermore, we examined the electrical properties and reliability characteristics of TFTs and found both device performance and kink phenomenon can be effectively improved.

2.2 Experiment Details

2.2.1 Elevated Channel TFTs with Different Thickness of Active Layer

Detail processes for fabricating ECTFT sample with GOLDD structure are shown in Fig. 2-1. At first, a 50-nm amorphous silicon layer was deposited on an oxidized silicon substrate by LPCVD at 550^{o}C. Then the thin channel (trench) region was patterned by photo lithography and Si etchant composed of HNO_3, NH_4F and H_2O. Next, without removing photoresist, the samples were soaked into super saturated H_2SiF_6 solution at 23^{o}C; the SLPD-oxide would deposit at the sidewall and the bottom of the trench except the surface of photoresist. For ECTFT structure, the selective liquid-phase deposition (S-LPD) technique will become a key process to planarize the trench area at room temperature without utilizing CMP or additional

photo-masks, thus fully compatible for LTPS process on glass substrate. Because the wet chemical etching and the deposition of LPD oxide are both isotropic, a planar surface can be established precisely and was checked by surface profiler. After photoresist removal, a phosphorous implantation with a dosage of 1×10^{13} cm^{-2} at 30 keV was performed to generate lightly doped region(LDD).

Next, an amorphous-Si layer with different thickness including 15 nm, 30 nm, 50 nm and 100 nm was deposited by LPCVD at 550°C as the active layer. The samples with various thickness of active layer were abbreviated to **ECT15, ECT30, ECT50, and ECT100**, respectively. For comparison, control samples with the active layer thickness from 15 nm to 100 nm were also prepared, and were abbreviated to **AA15, AA30, AA50, and AA100**, respectively. After the active area was patterned, a 125-nm gate oxide layer by PECVD and 300-nm poly-Si gate electrodes by LPCVD at 620°C were formed. For n-channel transistors, a self-aligned phosphorous implantation with a dosage of 5×10^{15} cm^{-2} at 60 keV was carried out to generate S/D regions, as shown in Fig. 2-1(i). Here, the gate-overlapped length **d** as indicated in the figure ranges from 0 to 3 μm.

After depositing TEOS oxide by PECVD as a passivation layer, the contact holes were etched by buffered oxide etcher (BOE). Without removing photoresists about contact holes, a 5 nm Ni was deposited subsequently by Dual E-Gun evaporation system and the photoresists were then lift-off by ACE. Using contact hole pattern can like a offset MILC poly TFT, because the distance from the edge of Ni seeding window to the edge of gate electrode is 15 μm. This structure can made the MIC/MILC junction not at the drain junction to exclusion the Ni silicide phase in depleted junction regions.[2.12].Next, the samples underwent a furnace annealing at 550°C in N_2 atmosphere for 48 hr, which not only activated the doped area but also accomplished the Ni-MILC in the channel region, as shown in Fig. 2-1(k). Thereafter,

the remaining Ni was removed by hot H_2SO_4 and H_2O_2 mixtures. Then, the samples were dipped in the diluted HF solution to remove the native oxide formed in the previous step. Finally, contact holes formation and metallization were carried out to complete the process, as shown in Fig. 2-1(l), while the conventional TFT structure was shown in Fig. 2-2. Moreover, a part of TFTs samples were subjected to plasma passivation.

The detailed process flow was listed below:

1. Initial RCA cleaning
2. 500 nm SiO_2: thermal wet oxidation at 1050^oC
3. 50 nm a-Si: LPCVD, SiH_4 source at 40 sccm, 550^oC
4. Mask #1: define the a-Si trench for the thin channel region
5. Wet chemical etching of the a-Si trench: poly etchant (NH_4F, HNO_3 and H_2O mixture) at room temperature
6. 50 nm SiO_2 by S-LPD method: (without removing photoresist) in super-saturated H_2SiF_6, at 23^oC for about 2.5 hr
7. P.R. removal
8. Ion implantation for LDD region: P^{31}, 30 keV, 1×10^{13} cm^{-2}
9. RCA cleaning
10. a-Si thin film deposition: LPCVD, SiH_4 source at 40 sccm, 550^oC, 100 mtorr
    a. ECTFT: ECT15, ECT30, ECT50, ECT100 (thickness in nm)
    b. conventional TFTs: AA15, AA30, AA50, AA100
11. Mask #2: define the active area
12. Dry etching of the active area: SAMCO® RIE-200L system with SF_6 at 20 Pa
13. RCA cleaning
14. 125 nm gate oxide: PECVD, TEOS and O_2 source, 350^oC, 250 W

15. 300 nm poly-Si gate: LPCVD, SiH_4 source at 40 sccm, 620^{o}C, 120 mtorr
16. Mask #3: define gate electrode
17. Dry etching of gate electrode: RIE-200L system with SF_6 at 20 Pa to etch poly, then BOE to etch gate oxide.
18. RCA cleaning
19. Ion implantation: P^{31}, 60 keV, 5×10^{15} cm^{-2} for ECTFT series; for AA15, AA30 and AA100 samples, the implantation energy is reduced to 30 – 50 keV
20. RCA cleaning
21. 500 nm passivation layer: PECVD TEOS SiO_2
22. Mask #4: Contact hole definition
23. Wet chemical etching for contact hole formation: buffered oxide etcher (NH_4F : HF = 6 : 1)
24. 5 nm Ni: Duel E-Gun evaporation system, 0.5 Å/sec at room temperature, base pressure below 2×10^{-6} torr
25. P.R. lift-off: ACE with ultra-sonic vibrations
26. Metal-induced lateral crystallization and dopants activation: furnace annealing, 48 hr, 550^{o}C in N_2 atmosphere
27. Residual Ni removal: hot SPM solution at 150^{o}C for 20 min
28. Native oxide removal: diluted HF, 20 sec
29. 500 nm Al: thermal coater, base pressure below 4×10^{-6} torr
30. Mask #5: Al patterned
31. Wet chemical etching for Al etching: H_3PO_4, HNO_3, CH_3COOH, H_2O mixture
32. Al sintering at 400^{o}C, 30 min in N_2 atmosphere
33. Hydrogenated for 1hr in an RF NH_3 plasma at 350 ^{o}C.

2.2.2 Elevated Channel TFTs with Different Doping Concentration of LDD

The impurity concentration of lightly doped drain region would undoubtedly affect the distribution of the electric field near the drain side. In section 2.2.1, the LDD concentration was fixed at 1×10^{13} cm^{-2}. Here, four different implantation conditions were applied to the LDD region; they were non-LDD doping, and LDD dosage among 1×10^{13} cm^{-2}, 5×10^{13} cm^{-2} and 1×10^{14} cm^{-2}, but the implantation energy was still kept in 30 keV. Except the LDD concentrations, all of the other process steps were identical with those described in Section 2.2.1.

2.3 Results and Discussion

2.3.1 Electrical Characteristics of ECTFT without GOLDD Structure and without NH3 Passivation

The transfer curves of conventional TFTs with different thickness of active layer are illustrated figure 2-3 . It is shown that the samples of AA100 exhibit the highest ON current and the smallest threshold voltage. The I_{ON} of TFTs depend on the trap-state density in the active layer, so this figure is indicated good crystallinity achieved. The ON current of those TFTs with thinner active layer is notably suppressed, and we believed that the large source/drain series resistance would be the primary reason. And thinning the active area of TFTs would also cause many other side effects such as poor drain/source contact, and low drain breakdown. And for sample AA100, it also find a increasing OFF-state leakage current, generally regarded as gate-induced drain leakage (GIDL) current, at V_G=-20V and V_D = 5 V is as large as sample AA15. This anomalous leakage current may attribute to the process of MILC.

When decreasing thickness from 100 to 30 nm, the MILC length rate will decrease gradually with thickness. Below 30 nm, a more drastic reduction is observed (figure.2-4[2.13]), with essentially no observable MILC for the 10 nm thick films significant.[2.13]. Form figure.2-5[2.13], we can see that the size of the NiSi2 nodules trapped at or near the MILC interface increases with decreasing film thickness. This $NiSi_2$ nodules could be caused by increased confinement of Ni diffusion by the top and bottom surfaces of the a-Si film. Then we are known that the MILC rate increases with decreasing $NiSi_2$ thickness[2.14].And the defective silicide layer will result in a large leakage current at AA15. Because the leakage current depends on the trap states density of the active layer and the lateral electric field near the drain side. Then AA30 and AA50 have low leakage current than AA100, because AA30 and AA50 MILC poly-Si active layer have better crystalline uniformity compared to the AA100.[2.15]

The I_D-V_{GS} curves of TFTs with elevated channel structure and different channel thickness are illustrated Fig. 2-6, while the gate overlapped length is zero (d = 0).Compare to the case of conventional TFTs, the ECTFT exhibit satisfactory ON current, OFF current, and ON/OFF current ratio exceeding 10^6. The Off-state leakage current of sample ECT30 even excesses 10^{-10} A at V_D = 5 V and V_{GS} = 0 V. And the GIDL current of ECT100 (1.5×10^{-9}A) is low than AA100(6.22×10^{-8}A).The reason are that the amount of the trap states in the active layer is decreased with increasing the Drain/Source thickness and the lateral electric field at the drain is reduced by adding an LDD region [2.16]Nevertheless, the sample ECT15 without gate overlapping LDD(GOLDD) structure (i.e. S/D = 65 nm, channel thickness = 15 nm and d = 0 μm) was failed in this experiment. From figure 2-7(a), a possible reason arose from the misalignment between the top-gate edge and the bottom trench region, and over etching the thin channel region by RIE maybe damaged during the definition of gate electrodes. Another possible failure mechanism was the planarization result by S-LPD.

As illustrated in Fig. 2-7(b), the planar surface filled by the S-LPD oxide would be slightly etched for approximately 20 ~ 40 Å during the following RCA cleaning process. The trench corner would cause problems such as step coverage or result in larger electric field during the operation of TFTs, and a thin active layer was more susceptible to the surface morphology in the trench corner. We cannot conclude which failure mechanism is correct at this stage, maybe both of them, so more investigations such as TEM analysis are required.

Fig. 2-8 show the field-effect mobility versus gate length for TFTs with different channel thickness. The μ_{FE} of sample ECT100 is 30 cm^2/Vs and gradually decreases when increasing the gate length or reducing the channel thickness. The former phenomenon can be explained by the number of grain boundaries in the channel region and. by the channel thickness. We are known that shrinking the thickness of channel layer can enlarge the parasitic source/drain resistance, leading to a degraded driving ability[2.17]. Therefore, one kind of TFT structure (ECT structure) with thin channel and thick source/drain region is developed to overcome these side effects while maintaining the benefits of thinning the active area [2.18], [2.19]. So we can see that the the mobility of ECT structure are obvious large than conventional structure by the Fig 2-8. It can be found that the mobility of sample AA100 becomes larger than that of ECT100. The excess trap states introduced between two deposition steps of a-Si (i.e. first for depositing S/D pads and second for forming the active area) were believed to cause the degradation of μ_{FE}. Due to the MILC process depends on a tiny nodule of $NiSi_2$ exists between a crystallized silicon(c-Si) region and an a-Si region. The c-Si grows mainly along the Si {111} direction via the epitaxial incorporation of Si generated from the decomposition of $NiSi_2$ near the c-Si/$NiSi_2$ interface[2.14].Form this process, it had been reported that the efficiency of MILC decreases with

increasing the length between the Ni seeding window and the device area. Therefore, as the crystallization front far from the seeding window of Ni, the crystallinity is poorer due to the rate of MILC becomes slower. So TFTs with long gate length could occupy more defective grain boundaries in the channel region; these grain boundaries establish potential barriers which impede the transportation of free carriers, contributing to the degradation of the mobility.

In this work, the carrier mobility decreased with reducing the channel thickness for both conventional and ECTFT structures. This phenomenon is associated with the thickness of channel. When the thickness of a-Si film decreases, the migration of $NiSi_2$ precipitates is restricted by the top and bottom surface of the a-Si thin film and thus the recrystallization rate drops significantly for lack of the $NiSi_2$ supply. In addition, the size of $NiSi_2$ precipitate is generally about several tens of nanometers and forms slowly in a thin a-Si film [2.15].And in this experiment, the distance from the edge of Ni seeding window to the edge of gate electrode is 15 μm, so the channel region should have recrystallized by spontaneous crystallization of a-Si (i.e. SPC) before the growth front of MILC reaches. This deduction was supported by the fact that the mobility of TFTs recrystallized by conventional SPC is not improved with decreasing the channel thickness [2.9], [2.11].

Figure 2-9 illustrates the off-state leakage current of TFT's at V_{GS} = -20 V. The sample AA100 exhibits the $I_{D,\,GIDL}$ an order of magnitude larger than ECT100 does. And the leakage current of AA50 at V_{GS} = -20 V also larger than that of ECT50.This is because the electric field dominates the leakage mechanism at Vg=-20.That condition implying that the channel electric field has been redistributed and relieved effectively by increasing the junction depth in the S/D region. Nevertheless, if we further reduce the channel thickness as in the case of ECT30 and AA30, the ECTFT structure seems not to alleviate the electric field. A 2-D simulation for the distribution

of the channel electric field in ECTFT configuration is required to confirm this hypothesis.

2.3.2 Electrical Characteristics of ECTFT with GOLDD Structure and without NH3 Passivation

Now we're going to discuss about the ECTFT with different doping concentration of LDD and gate-overlapped length. Figure 2-10 compares the transfer curves of ECTFT with various doping concentration of LDD region where the gate overlapped length d = 0 μm. The table 2.1 are shown that comparisons of device characteristics between conventional MILC TFT's and ECTFT with W/L=20μm/8μm at d=0. In general d equals zero, but the misalignment between the top gate and the bottom trench region still contributed to a small gate overlapped region about 0.5-μm long, as show in Figure.2-11. Moreover, for GOLDD samples, the S/D regions suffered two doping steps from LDD and self-aligned source/drain ion implantation, respectively, so that the S/D resistance became even lower. In contrast, there were no dopants in the misaligned region below the gate electrode for non-LDD device, resulting in slightly lower ON current. Figure 2-12 compares the mobility versus gate length with different LDD doping concentration; we found no differences among these samples. In general, the GIDL current increase significantly with increasing LDD doping concentration, this is because the location of peak electric field tend to shift to gate edge with increasing LDD doping level[2.20].But from Figure. 2-13 we don't see this condition, it may be concentration of LDD region non-uniform. Because the control of doping concentration is rather difficult because the doping efficiency in the poly-Si is closely related to the grain size and defect at the grain boundary and with in the grain[2.21].

Figure 2-14 are shown the I_D - V_G curves of ECTFT with various doping concentration of LDD region at d = 2 μm. In this case the overlapped length is large enough to compensate the error resulted from the misalignment. Since the gate electrode would induce excess carriers in both the thin channel and the thick overlapped region at ON state of TFTs, we did not observe obvious reduction of I_{ON} for the sample without LDD doping. Contrarily, for non-LDD and low LDD dosage (1×10^{13} cm^{-2}) conditions, the overlapped region forms an additional low conductance area and contributes to low leakage current at the OFF state of TFTs. Besides, the threshold voltage decreases with increasing the doping concentration in the overlapped region, which is quite straightforward.

Figure 2-15 shows the transfer curves of ECTFT with different gate overlapped length *d*. We can find that the electrical characteristics of ECTFT are insensible to the overlapped length, such as mobility, threshold voltage and ON/OFF ratio, etc. This condition may be that the ECTFT devices were recrystallized by MILC (or partial SPC, especially for the active layer far from the Ni seeding window), and the grain size was uniformly distributed in either the thin channel or the thickened S/D region, so that the I-V characteristics of samples with various length *d* were nearly identical. Increasing the gate overlapped length could decrease the OFF current (at Vg=0V) of TFTs. This is because the electron density in the overlapped region will be increased due to the enhanced vertical electric field. This results in an inversion layer induced underneath the overlapped region , thereby passivating the traps of the region.

In Figure 2-16, we made a forward-reverse measurement to the ECTFT devices. The transfer curves of TFTs were measured first as *forward* I-V characteristics and then the source/drain electrodes were interchanged while *reverse* I-V characteristics were obtained. Where the solid lines represent a forward measurement and the dash

lines represent a reverse measurement. There's small difference in the value of carrier mobility, but the other electrical properties are nearly identical. Although there's small asymmetry of the ECTFT structure owing to the misalignment between the top gate electrode and the thin-channel region, the transfer curves of ECTFT are still independent of the gate overlapped length.

One of the main advantages of the proposed ECTFT devices is that the thickened source/drain region can effectively reduce the series resistance when the channel region becomes thinner. Then Fig 2-17 shows the value of R_{SD} with respect to different TFT structures, active layer thickness and dopant concentration of LDD.When the channel thickness reduces to 30 nm, the S/D series resistance of conventional TFT is 933 kΩ. And this large parasitic resistance effects could degrade the performance of TFTs. Contrarily, the thickened source/drain regions of sample ECT30 exhibits a much lowered R_{SD} of 430 kΩ; the sample ECT50 also shows R_{SD} of around 200 kΩ. as compared to the sample AA50 with R_{SD} of 250 kΩ. Besides, the LDD doping concentration has no impression upon the S/D series resistance, and when the channel thickness increases to 100 nm, the R_{SD} cannot be further reduced by ECTFT structure.

The floating body effect, also called "kink" effect, because of the impact ionization occurring in the high electric field region at the drain end of the channel. The GOLDD poly-Si TFT exhibited suppressed kink effect compared to the conventional poly-Si TFT due to the reduction of drain field, so that the large lateral electric field can be redistributed and relieved.[2.22]. The ECTFT architecture would increase the junction depth of the drain side, so the kink effect can be greatly improved by the elevated channel with gate overlapped structure. Fig 2-18 is shown the I_D - V_D curves of TFTs extracted at V_G = 25 V, where the gate-overlapped length *d* is 0 μm in Fig. 2-18(a) and *d* is 2 μm in Fig. 2-18(b).The ECT samples with d = 0

exhibit no obviously improvement to the kink suppression compared to the sample AA50. But the kink phenomenon can be effectively eliminated by increasing the gate overlapped length d to 2 μm. Figure 2-19 are shown that the averaged kink point from at least three samples for ECTFT. The kink starting point can be found by the derivative of drain current, that is, the corresponding drain voltage V_D at which the output conductance dI_{DS}/dV_{DS} curve starts to bend.

2.3.3 Electrical Characteristics of ECTFT with NH3 Plasma Passivation

In this subsection, we will talk about the electrical characteristics of ECTFT with NH_3 passivation. Due to poly-Si thin films consist of differently oriented grains and grain boundaries that contain many lattice defects in these irregular regions. These lattice defects act as trap centers and degrade the performance of poly-Si TFTs [2.22]. The characteristics of poly-Si TFTs depend strongly on defects in poly-Si active thin film and at the interface of poly-Si thin film and gate dielectric [2.23]. Traditionally, to passivate the grain boundary defects and silicon dangling bonds, hydrogen or NH_3 plasma treatment has proved to be very effective for promoting the performance of LTPS TFTs. [2.24].

Fig.2-20 show the transfer characteristics for ECT TFT's before and after 1hr NH_3 plasma passivation after annealing at 350 ^oC . It is clean that the NH_3 plasma treated sampled exhibit the better electrical characteristics in OFF states. This is due to the nature of deposition of gate oxide, there are more dangling bonds and weak Si–O and Si–Si bonds in oxide and at interface between gate oxide and poly-Si channel layer in poly-Si TFT. The trap states would become generation-recombination centers, contributing to a large leakage current at OFF state. The NH_3 plasma treatment can

improve the quality of oxide and interface between poly-Si thin film and oxide by passivating the dangling bonds, and hence improve the characteristics of poly-Si TFTs[2.25].

Fig.2-21 show the transfer characteristics of ECT structure with different thickness of the active layer after passivation. It appeals that ECT50 TFT has higher ON current than ECT30 and lower OFF current than ECT100.The first condition is because ECT50 have better grain structure[2.15]; the latter is due to the source/drain thickness of ECT50 is 100 nm, so it can have less MIC/MILC junction depth area which have high density of grain boundary trap states. Since leakage current at high Drain voltage is dominated by trap-assisted field-emission current, the combination of high electric field in the junction and high trap density in the MIC/MILC junction will result significantly higher leakage current[2.26]. Figure. 2-22 show the output characteristic for 1 hr NH_3 plasma treatment at V_G = 25 V for channel width 50nm samples. The identical improvements are shown for three structure samples. It appeal that NH_3 is effective in reducing the interface trap density. And can be noted from Fig 2-23, the anomalous current increase, occurring above pinch-off and related to impact ionization, is sensibly reduced in the ECT with gate overlapping structure. It is believe that the moderate kink effect in gate overlapping LDD region is mainly due to a relative low field near the drain junction.

2.3.4 Reliability of ECTFT with NH3 Plasma Passivation

For poly-Si TFT under hot carrier stress, it is known that the degradation mechanism is the channel states near the drain junction accompanying with hot carrier injecting into the gate oxide and creating new interface and/or bulk traps, which is caused by high electric field near the drain junction [2.27] So hot carrier stress was

used to test the long-term reliability of ECT TFTs in this work. The DC stress condition was V_{DS} = 25V and V_{GS} =7.5V or 12V for 5000 seconds. Figure 2-24 show variation of threshold voltage at V_{DS}=5V under hot carrier stress. The dominant degradation in conventional hydrogenated poly-Si TFTs without a sidewall spacer and a lightly doped drain structure (AA50,ECT50 with D=0) is caused by drain avalanche hot carriers (DAHCs). [2.28][2.29.][2.30].When a positive gate voltage is applied, the electric field will cause electrons injected from channel into gate oxide [2.31]. These injected electrons might be trapped into the disorder region of gate oxide, and consequently inducing positive shift of threshold voltage. However, due to the drain field relief in the gate overlapping LDD region, those in ECT TFTs structure degraded more slow, which result from fewer trap creations during the stress.

Figure 2-25 show variation of mobility at V_{DS}=0.1V under hot carrier stress. For conventional TFT (ECT50), mobility decreases monotonically, due to the tail states generation at the gate oxide/channel interface[2.32][2.33].But for other conditions, the mobility initially increases then saturates and finally starts to decrease. Mobility rising is because that holes injected into the gate oxide region near drain attribute to channel shortening effect. When the injected holes reach saturation at the turnaround point, then tail states generation in the grain boundaries and gate oxide/channel interface start to dominate mobility degradation [2.32]. Compared to Fig. 2-26, the ECT TFTs with gate overlapping do not severe variation of the mobility. This is due to reduction of drain field, so the avalanche carrier generation rate in TFTs is reducted.

Figure 2-27 show that variation of ON current at V_{DS}=5V under hot carrier stress**.** The on current will be degradation, this is due to the hot carrier induced degradation increases the density of the band tail traps in a region 200 nm from the drain and the series resistance on the drain side[2.34] increase of the hot carrier induced tail state density[2.35]. The ample ECT50 without LDD does not show good hot carrier

reliability, implying that just increasing the drain junction depth can not to reduce the drain electric field.. The ECT50 sample without LDD dopants compared to the sample AA50 exhibit no notable improvement to the kink suppression. Compared to Figure 2-28, the ECTFT with gate overlapping LDD exhibited much better hot carrier stress endurance[2.36], due to reduction of drain field in ECT structure.

2.4 Summary

The ON current decreased with reducing the channel thickness for both conventional. One of the main advantages of the proposed ECTFT devices is that the thickened source/drain region can effectively reduce the series resistance when the channel region becomes thinner. The lateral electric field at the drain for ECTFT is reduced by adding an LDD region. And the kink phenomenon can be effectively eliminated by increasing the gate overlapped length d to 2 μm. The ECTFT with gate overlapping LDD exhibited much better hot carrier stress endurance, due to reduction of drain field in ECT structure.