Chapter 3

Effects of Ge Layer and Si_3N_4 NanoCap Layer On Metal-Induced Laterally Crystallized Polycrystalline Silicon TFTs

3.1 Introduction

We known that the three major methods to recrystallize amorphous silicon are: Rapid Thermal Annealing(RTA), Excimer Laser Crystallization (ELC) and Solid Phase Crystallization(SPC)[3.1][3.2].Solid phase crystallization and RTA has several advantages over laser crystallization which include smoother surfaces, better uniformity, and batch process in furnace annealing. But in order to achieve the requirements imposed by the integrated fabrication on glass substrate, the polysilicon TFT's performance must be optimized and fabricated at a suited temperature (<600℃).So SPC and RTA, their processing temperature of around 600 still exceeds the upper temperature limit of glass substrates, are not suited to use.

Nevertheless, it has been reported earlier that amorphous silicon (a-Si) thin films can be crystallized at temperatures as low as 450℃ by metal-induced crystallization (MIC) method[3.3][3.4][3.5].But the annealing temperature (>=500℃) is still too high for poly-Si TFT device to fabricated on conventional glass substrate , and the long annealing time of MILC, also increase the thermal budget in the poly-Si TFT fabrication process. However in current years, the papers are proposed that using a Ge layer can enhance MILC growth velocity three times compared with that in the a-Si single layers[3.6] and decrease nucleation temperature significantly with increasing Ge fraction[3.7].But they are still never to test the electrical characteristic.

Thin film transistors (TFTs) fabricated by this MIC process still have other drawback : significant incorporation of Ni in MIC poly-Si[3.8].So we can use the SiNx[3.9] or SiO_2[3.10] layer be a filter against too metal contamination for metal induced crystallization. General, in solid-phase crystallization, to get a large grain must decrease the nucleation rate and increase the grain growth rate.[3.11]The same ,for MILC, the crystallization proceeds from the NiSi2 precipitates(the seed or nucleation site), the long-range metal-induced grain growth is possible only in the radial direction, since growth in any other directions is quickly arrested by collision [3.12] among the grains. For this reason , if the metal contamination is decrease, the number of NiSi2 seeds will be decrease. Then we will have the long grain size.

Here, we will show electrical characteristics of the MILC TFTs with Ge Layer and Si_3N_4 NanoCap Layer. And we know that the post-MILC high temperature treatment led to further improvement in MILC poly-Si material and device characteristics [3.13]. Therefore we also will compare the annealing temperature effect of MILC TFTs with Si_3N_4 NanoCap Layer.

3.2 Experiment Details

Detail processes for fabricating MILC poly-Si TFT sample with Ge Layer and Si_3N_4 NanoCap Layer are shown in Figure 3-1.Conventional co-planar N-channel MILC poly-Si TFT's are fabricated on 4-inch-diamater wafers. A 500 nm thermal oxide was deposition on bare-wafer as a buffer layer. Then a 100 nm thick amorphous a-Si was deposition by LPCVD system using pure silane gas at 550 ℃. A control sample was using SPC at 600 ℃ for 24 hours in furnace. After the active layer was patterned, all samples were cleaned by RCA process. Then a 125-nm gate oxide layer by PECVD and 300-nm poly-Si gate electrodes by LPCVD at 620^{o}C were formed.

After defining the gate geometry, some samples was deposition 5 or 20 nm thickness Si_3N_4 as filter layer by the PECVD system. Using contact hole mask to pattern metal layer, then samples were formed a metal layer by Dual E-gun system : Ni 5nm/a-Si , Ni 5nm/SiN 5nm/a-Si, Ni 5nm/SiN 20nm/a-Si, Ni 5nm/Ge 5nm/a-Si, Ge 5nm/Ni 5nm/a-Si. Metal was patterned only existing in source and drain surface by lifting off photo-resistor in ACE solution. Then the samples underwent a furnace annealing at 550℃ in N_2 atmosphere for 24 hr. Thereafter, the remaining metal was removed by hot H_2SO_4 and H_2O_2 mixtures. And the remaining Si_3N_4 was removed by hot H_3PO_4. For n-channel transistors, a self-aligned phosphorous implantation with a dosage of 5×10^{15} cm^{-2} at 60 keV was carried out to generate S/D regions. After depositing a 500nm thick tetraethylorthosilicate(TEOS) oxide by PECVD as a passivation layer. The samples underwent a furnace annealing activated the doped area : 600℃-48 hr and 900℃-30 min. Then the contact holes were etched by buffered oxide etcher (BOE). A 500 nm thick aluminum layer was evaporated and patterned. Aluminum sintering was performed at 400℃ for 30 minutes. Post passivation was treated by Hydrogen(H_2) plasma in PECVD system for l hr. The detailed fabrication process flow is listed as follows.

1. Initial RCA cleaning
2. 500 nm–thick SiO_2: thermal wet oxidation at 1050^oC
3. 100 nm-thick a-Si: LPCVD, SiH_4 source at 40 sccm, 550^oC
4. A control sample: SPC, 72 hr, 600 ^oC
5. Mask #1: Define the active area
6. Dry etching of the active area: SAMCO® RIE-200L system with SF_6 at 20 Pa
7. RCA cleaning
8. 125 nm gate oxide: PECVD, TEOS and O_2 source, 350^oC, 250 W

9. 300 nm poly-Si gate: LPCVD, SiH_4 source at 40 sccm, 620^oC, 120 mtorr
10. Mask #2: define gate electrode
11. Dry etching of gate electrode: SAMCO® RIE-200L system with SF_6 at 20 Pa
12. RCA cleaning
13. 5nm and 20nm Si_3N_4: PECVD, SiH_4 and N_20 mixture.
14. Mask #3: define metal pad.
15. Ni,Ge: Duel E-Gun evaporation system, 0.5 Å/sec at room temperature, base pressure below 2×10^{-6} torr
16. P.R. lift-off: ACE with ultra-sonic vibrations
17. Metal-induced lateral crystallization: furnace annealing, 24 hr, 550^oC in N_2 atmosphere.
18. Residual Ni removal: hot SPM solution at 150^oC for 20 min.
19. Residual Si_3N_4 removal: hot H_3PO_4 solution.
20. Ion implantation: P^{31}, 60 keV, 5×10^{15} cm^{-2}
21. RCA cleaning
22. 500 nm passivation layer: PECVD TEOS SiO_2
23. Dopants activation: Some sample furnace annealing, 48 hr, 600^oC in N_2 atmosphere,other 30 min, 900^oC
24. Mask #4: Contact hole definition
25. Wet chemical etching for contact hole formation: buffered oxide etcher (NH_4F : HF = 6 : 1)
26. Native oxide removal: diluted HF, 20 sec
27. 500 nm Al: thermal coater, base pressure below 4×10^{-6} torr
28. Mask #5: Al patterned
29. Wet chemical etching for Al etching: H_3PO_4, HNO_3, CH_3COOH, H_2O mixture

30. Al sintering at 400^{o}C, 30 min in N_2 atmosphere

31. Hydrogenated for 1hr in an RF NH_3 plasma at 350 ^{o}C.

3.3 Results and Discussion

3.3.1 Electrical characteristics on Si_3N_4 NanoCap layer

In the subsection, we will in detail investigate the comparison of electrical characteristics of MILC TFT with or without Si_3N_4 cap layer. Fig 3-2 and 3-3 show the comparison of transfer characteristics for comparison of MILC TFT's with and without Si_3N_4 filter layer. It is clean that the MILC TFT's samples exhibit the better electrical characteristics than the SPC sample. From Fig.3-4 show that field-effect mobility of MILC TFT's with Si_3N_4 filter layer only close to 30 cm^2/(V*Sec). This because that the grains of MILC do not fill channel up.

We must first realize that the MILC process is mediated by the migration of the NiSi2 precipitates. A NiSi2 precipitates can act as nucleation sites and participate in the lateral crystallization process. So adding a cap layer on the a-Si can reduce the number of nuclei with reducing metal contamination and have a uniform grain size with a clean and smooth surface[3.14].And the fully crystallized poly-Si with a capping layer could form hexagonal shaped or disk-shaped grains. Note that the disklike grains can be grown without a cap layer when the Ni density is low. The hexagonal shaped or disk-shaped grains is due to lateral grain growth from NiSi2 precipitates. But it is known that conventional crystallization without cap layer is mediated by the migration of the NiSi2 precipitates throughout the a-Si, leaving behind a trail of needlelike Si crystallite. On the other word, the MILC length with cap layer, from MIC/MILC junction is shorter than that of conventional MILC without cap layer, which is due to the shortage of nickel source for lateral growth.

And if the channel length is too long, the appearance of the solid phase characterization of a-Si will be increase with MILC time. Once the SPC start, the lateral crystallization is clogged by the crystalline region in the film resulting from SPC process[3.15][3.16]. So the middle of channel will have more grains due to SPC. This also increase the trap states in the channel. And we know that the mobility of LTPS-TFT is dominated by the trap states in the poly-Si grain, grain boundary or poly-Si channel/gate-oxide interface. These trap states would create a potential barrier that impedes the movement of free carriers during ON state of TFTs or become generation-recombination centers, contributing to a large leakage current at OFF state. The extraction of the effective trap-state density(Nt) for MILC TFT's and SPC TFT's are shown in Fig. 3-5 by modified Levinson theorem. We found that Nt of MILC with cap layer are nearly the same with MILC without cap layer. This result is in agreement with previous analysis.

The SPC poly-Si has intra-grain defects and high temperature process can reduce them [3.17]. So the anneal resulted in significant improvement in the material quality. Consequently, the electrical properties of the high temperature annealed MILC poly-Si resistors were greatly enhanced, showing conduction behavior approaching that of single-crystal Si[3.19]. Fig. 3.6~Fig 3.8 show the transfer characteristics of MILC TFT's after 900 ^{o}C annealing. We can see that the ON current and mobility increase, the subthreshold swing and threshold voltage decrease. Table 3-1 and 3-2 list the device parameters for MILC TFT's and SPC after annealing 600 ^{o}C and 900 ^{o}C in N_2 gas. We found that 900 ^{o}C annealing treatment effect are better than 600 ^{o}C annealing treatment. This is because that the low-angle GBs could be drastic change in the microstructure of MILC poly-Si [3.18]and improvement in the crystal quality by eliminating the small amorphous fraction [3.21] during the high-temperature anneal. The rearrangement of the atoms along low-angle GBs by annealing , at the

same time, recrystallization of the elongated grains takes place in MILC poly-Si. The paper[3.20] is proposed that when merging misorientated grains, the GBs can be removed and the lattice stress relaxed by the formation of line defects. And it is well know that SPC poly-Si has poly-Si has a columnar grain structure with grain boundaries randomly oriented with respect to the direction of Id[3.20]. These grain boundaries trap charge carriers and build up potential barrier to the flow of carriers. So 900 ^{o}C annealing treatment can decrease the numbers of grain boundaries and improve the grain quality in the channel of MILC TFT's and SPC TFT's. And after 900 ^{o}C treatment, the mobility effect of conventional TFT is greater than MILC TFT's with cap layer. This can again confirm that NiSi2 precipitates lack enough Nickel source to form longitudinal grain and the middle of channel have poly-Si of SPC.

3.3.2 Effect on adding Ge layer

Fig. 3-9 and Fig.3-10 show the transfer curves at V_d=0.1V and 5V with Ge layer. And figure 3-11 are shown that comparison of mobility for MILC TFT's deposited Ge layer at V_{DS}=0.1V. The results of device parameters analyzed by HP4145C are summarized in Table 3-3. As compared in conventional MILC TFT's, Ge performs better in high mobility, but bed in threshold voltage and trap-state density(Nt). We know that the deep-state creation of grain boundary is accompanied with threshold voltage, so TFT gives rise to parallel shift of transfer curve. And midgap state creation don't change significant change in the field-effect mobility[3.22]. The mobility is more sensitive to the population of tail states and intra-grain defect[3.23] [3.24]. So this result of electrical characteristic is that adding Ge to MILC TFT's can have good grain quality but bed grain boundaries.

Now the recrystallization rate for three types of metal films(Ge 5nm/Ni 5nm/a-Si , Ni 5nm/Ge 5nm/a-Si, Ni 5nm/Ge 20nm/a-Si) were investigated with various

temperature (500 ^{o}C, 550 ^{o}C,600. ^{o}C). From Fig 3.12-3.14, recrystallization rate for different conditions were extracted from plots of lateral crystallization length versus crystallization time. Here we can find out Ge 5nm/Ni 5nm/a-Si samples show the fastest recrystallization rate and others samples show lower at 550 ^{o}C and 600 ^{o}C.

An Arrhenius plot of grown rate versus reciprocal temperature is shown in Fig 3.15. The growth rate can be described by an Arrhenius-type equation of the form:

$r = r_0 \exp\left(\frac{-E_a}{k_B T_s}\right)$, where r_o is the maximal growth rate (ie. the asymptotic limites as $T_s \to \infty$), E_a the apparent activation energy for the process, k_a the Boltzmann constant, and T_s the absolute substrate temperature. If the rate-limiting step process is a temperature dependent surface reaction, the natural log of the growth rate data will show a linear dependence on the reciprocal of the substrate temperature. The slope of the linear least square fit to the data gives the apparent activation energy E_a while the intercept gives the asymptotic growth rate r_o. In table 3-4 , all the extracted data for recrystallization rate. Between these parameters, Ge 5nm/Ni 5nm/a-Si samples show the highest activation energy(1.903 eV). Since the activation energy could be considered as the barrier for nucleation, it needs more energy to form nuclei for its higher E_a Value. On the other word, it's more difficult for to start nucleation at lower temperature. In Fig3.15, we can indicate that the higher r_o value reflects the higher increasing tendency in crystallization rate as annealing temperature. But with the increasing temperature, the rate for Ni/Ge/a-Si samples are small than Ge/Ni/a-Si. This condition may be that Ge was not introduced into Si layers during annealing, but Crystal nucleation is initiated in the a-Ge layers during MILC[3.25]. So this phenomenon are interfered Ni diffused into Si. Furthermore, increasing the annealing temperature at 600 ^{o}C reduces the growth rate for Ni/Ge/a-Si samples at 550 ^{o}C, this is due to the random nucleation and spontaneous crystallization(SPC) of a-Si first are

occurred before Ni contacts Si film at high temperatures.[3.26]

From Figure 3-16, we can see that the Ge/Ni/a-Si. sample have faster recrystallization rate than the Ni/a-Si sample. This phenomenon is attributed to the change of the bonding energies in the a-Si layers. The influences of Ge doping in a-Si is bond rearrangement in the a-Si layers, resulting in the increases of MILC velocity[3.7][3.27]. And figure 3-17 show that the SEM graph of Secco-etched Ni MILC poly–Si for difference structure (including $Si_{0.85}Ge_{0.15}$ film) after 6 hr at 550 ^{o}C. From the graph, we can obviously discriminate needlelike poly-Si and a-Si for Ge/Ni/a-Si sample and small number of poly-Si grains for Ni/Ge/a-Si sample. This phenomenon can confirm the previous reason of why the lower growth rate of grain for Ni/Ge/a-Si samples. And the graph of $Si_{0.85}Ge_{0.15}$ film is still a-Si layer and very small poly-Si grains, so it will have high resistance value. And it can confirm from the figure 3-18, the a-SiGe film have very large sheet resistance compared with a-Si films.

3.4 Summary

The MILC with Si3N4 nanocap layer can decrease density of states and have good grain quality. This is because that using the SiNx layer as a filter can decrease the number of NiSi2 and to have the long grain size. And the MILC length with cap layer, from MIC/MILC junction is shorter than that of conventional MILC without cap layer, which is due to the shortage of nickel source for lateral growth. So the grains of MILC do not fill channel up.

The influences of Ge in a-Si is bond rearrangement in the a-Si layers. So the Ge in a-Si can enhance the crystallization velocity and decrease nucleation temperature. If Ge layers during MILC wiil crystallize nucleation,. this phenomenon can interfere Ni diffused into Si.