Chapter 4

Conclusions

4.1 Conclusions

In this thesis, we utilized combining the gate overlapped light-doped drain and elevated channel structures, called elevated-channel thin-film transistor (ECTFT) structure, to improve the performance of device. Furthermore, we also investigated the effect of MILC with Si_3N_4 and Ge .

For the ECTFT technology, we can obtain satisfactory ON current, OFF current, and ON/OFF current ratio exceeding 10^6 at channel thickness 50nm . This is because we thick source/drain region to overcome high parasitic source/drain resistance while maintaining the benefits of thinning the active area. And the leakage current can suppress at Vg=-20V, Vd=10V by adding an LDD region to reduce the lateral electric field at the drain. In general, the GIDL current increase significantly with increasing LDD doping concentration, but we don't see this condition, it may be concentration of LDD region non-uniform. There's small asymmetry of the ECTFT structure owing to the misalignment between the top gate electrode and the thin-channel region, but from the forward-reverse measurement , it is done not influence the electrical properties of ECTFT. The ECTFT exhibited suppressed kink effect, the kink phenomenon can be effectively eliminated by increasing the gate overlapped length, this is because the channel electric field at drain junction has been redistributed and relieved effectively. Furthermore, after passivation treatment, the NH_3 plasma treated effective to reduce the interface trap density and dangling bond, it exhibit the better electrical characteristics. From stress treatment, the ECT TFTs structure are degraded more slow, due to the drain field relief in the gate overlapping LDD region, so which can result

from fewer trap creations. The avalanche carrier generation rate in ECTFT with gate overlapping can reduce, so it can not severe variation of the mobility and ON current. So the ECTFT with gate overlapping LDD exhibited much better hot carrier stress endurance.

For MILC with Si_3N_4, it was found that using nanocap layer can have reduced density of states, so it can have better performance parameters. And after 900 ℃ treatment, we are known the channel with nanocap layer is not fill channel up, due to shortage of enough $NiSi_2$ and SPC occurred in the channel. And the Ge in a-Si can enhance the crystallization velocity and decrease nucleation temperature. But Ge also will interfere Ni diffused into Si, if Ge layers first crystallize nucleation.

4.2 Future Works

There are still some problems should be solved. We introduction these issues :

(1)The ECTFT with LDD can decrease the lateral electric field at drain junction. with different LDD doping concentration. But the GIDL current don't increase significantly with increasing LDD doping concentration. So we wiil use a 2-D simulation to that the distribution of the channel electric field in ECTFT configuration.

(2)The MIC/MILC junction area will increase with the source/drain thickness and influence the device performance. So in the future, we will make ECTFT with the same source/drain thickness and different channel thickness to eliminate the infulence.

(3)From the crystallization process of MIC and MILC, we can know that MIC with Si_3N_4 can have better performance than MILC. So, we will make MIC with Si_3N_4 and gate oxide by using SLPD.

Appendix

A.1 Determination of Effective Trap State Density (N_t)

The trap-state density, which can be determined be the theory established by Levinson et al.[A.1],is based on Seto's theory[A.2].

For a thin-film transistor, the source-drain current I_{DS} can be given as following[A.1],

$$I_{DS} = (\frac{W}{L})C_{OX}V_{DS}u_{FE}V_{GS}\exp(\frac{-q^3N_t^2L_C}{8\varepsilon_{Si}kTC_{OX}V_{GS}}) \quad \text{.....(Eq. 1)}$$

Here,

u_{FE} is the field-effect mobility of the carriers.

Q is the electron charge.

k is Boltzmann's constant.

ε_{Si} is the silicon dielectric constant.

T is the temperature.

N_t is the trap-state density per unit area.

L_C is the channel thickness.

This expression, first developed by Levinson et al. [A.1], is a standard MOSFET's equation with an activated mobility, which depends on the grain-boundary barrier height as introduced by Seto[A.2].Levinson et al. assumed that the channel thickness was constant and equal to the thickness of polysilicon film (t). This simplifying assumption is permissible only for very thin film (t < 100Å). The trap-states density can be obtained by extracting a straight line on the plot of $\ln(I_{DS}/I_{GS})$ versus $1/V_{GS}$ at low source-drain voltage and high gate voltages.

Proano et al. [A.3] thought that a better approximation is to calculate the gate induced carrier channel thickness by solving Poisson's equation for an undoped

material and to define the channel thickness as a thickness which 80 percent of the total charge induced by the gate. Doing so, one obtains

$$L_C = \left(\frac{8kTt_{OX}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}}}{q(V_{GS}-V_{fb})}\right) \quad \text{.....(Eq. 2)}$$

, which varies inversely with (V_{GS}-Vfb). This predicts, by substituting Eq.2 into Eq. 1,that In[I_{DS}/(V_{GS}-V_{fb})] varies linearly with 1/(V_{GS}-V_{fb})^2 . We used the gate voltage at which minimum leakage current occurs as the V_{fb}. And the slope is get from the graphic of In[I_{DS}/(V_{GS}-V_{fb})] varies linearly with 1/(V_{GS}-V_{fb})^2 .Effective trap-state density Nt can be determined from the square root of the slope.

$$N_t = \frac{C_{OX}}{q}\sqrt{|Slope|} \quad \text{.....(Eq. 3)}$$

A.2 Determination of the S/D series resistance R_{SD}

For small drain bias V_D at a high gate drive, it is assumed that the ON resistance R_{ON} of TFTs consists of the channel resistance R_{ch} and the S/D series resistance R_{SD} [A.4], [A.5], that is,

$$I_{DS} = \frac{W}{L}\mu C_i(V_G - V_{th} - \frac{V_D}{2})V_D \qquad \text{as } V_D << V_G - V_{th} \text{ .....(Eq. 4)}$$

$$R_{ON} = \frac{\partial V_D}{\partial I_{DS}}\Big|_{\substack{V_G \\ V_D \to 0}} = R_{ch} + R_{SD} \quad \text{.....(Eq. 5)}$$

and the channel resistance in the linear region is approximately given by

$$R_{ch} = \frac{L}{W\mu C_i(V_G - V_T)} \quad \text{.....(Eq. 6)}$$

where L is the channel length, W is the channel width, C_i is the capacitance per unit area of the insulating layer, V_{th} is the threshold voltage, and μ is the field effect mobility. Then the R_{SD} can be extracted by measuring R_{ON} of output characteristics of TFTs in the linear region and by plotting $R_{ON}W$ as a function of L. Hence, the R_{SD} is a set of these straight lines intersecting at a small triangle area.