

# References

## Chapter 1

- [1.1]Yasuhsia Oana," Current and future technology of low-temperature poly-Si TFT-LCDs," Journal of the SID, vol. 9, pp. 169-172, 2001.
- [1.2] Kiyoshi Yoneda,Hidenori Ogata, Shinji Yuda, Kohji Suzuki, Toshifumi Yamaji, Shiro Nakanishi, Tsutomu Yamada, and Yoshihiro Mirimoto, " Optimization of low-temperature poly-Si TFT-LCDs and a large-scale production line for large glass substrate," Journal of the SID, vol 9,pp. 173-179,2001.
- [1.3] J.G. Blake, J.D. III Stevens, and R. Young," Impact of low temperature polysilicon on the AMLCD maket," Solod State Tech, vol. 41, pp. 56-62, 1998.
- [1.4] M. Kimura, I. Yudasaka, S. Kanbe, H. Kobayashi, H. Kiguchi, S. Seki, S. Miyashita, T. Shimoda, T. Ozawa, K. Kitawada, T. Nakazawa, W. Miyazawa, and H. Ohshima, "Low-temperature polysilicon thin-film transistor driving with integrated driver for high-resolution light emitting polymer display," IEEE Trans. Electron Devices, vol. 46, pp.2282-2288, Dec. 1999.
- [1.5]Mark Stewart, Robert S.Howell,Leo Pries, and Mitiadis K, Hatalis," Polysilicon TFT technology for active matrix OLED displays," IEEE Trans. Electron Devices,vol. 48,pp. 845-851, 2001.
- [1.6]Zhiguo Meng and Man Wong," active-matrix organic light-emitting diode displays realized using metal-induced unilaterally crystallized polycrystalline silicon thin-film transistors," IEEE Trans.Electron Devices, vol. 49, pp. 991-996,2002.
- [1.7]M. Furuta, S. Maegawa, H. Sano, T. Yoshioka, Y. Uraoka, H. Tsutsu,I. Kobayashi, T. Kawamura, and Y. Miyata, "A 2.8-in. diagonal lowtemperature-purcessed poly-Si TFT with a new LDD structure," in Proc.Euro Display, 1996, pp. 547–550.
- [1.8] I.-W.Wu, "Cell design considerations for high-aperture-ratio direct-view and projection polysilicon TFT-LCD's," in Dig. Tech. Papers, SID'1995,pp. 19–22.
- [1.9]M. K. Hatalis and D. W. Greve, "Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited amorphous silicon films," J. Appl. Phys., vol. 63, p. 2260, 1988.
- [1.10]H. J. Kim and J. S. Im, "New excimer-laser-crystallization method for producing large-grained and grain boundary-location-controlled Si films or thin film transistors," Appl. Phys. Lett., vol. 68, p. 1513, 1996

- [1.11] Bonnel, M; Duhamel, N.; Haji,L.; loisel,B.”; Stoemenos,J.,’Polycrystalline silicon thin-film transistors with two-step annealing process,” IEEE Electron Device Letters, Vol. 14, no. 12, pp. 551-553, Dec.1993.
- [1.12] S. W. Lee and S. K. Joo, “Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization,” IEEE Electron Device Lett., vol. 17, pp. 160–162, Apr. 1996.
- [1.13] D. J. Dimaria and J. W. Stasiak, “Trap creation in silicon dioxide produced by hot electrons,” J. Appl. Phys., vol. 65, pp. 2342–2356, 1989.
- [1.14] M. Hack, A. G. Lewis, and I. W. Wu, “Physical models for degradation effects in polysilicon thin-film transistors,” IEEE Trans. Electron Devices, vol. 40, pp. 890–897, May 1993.
- [1.15] N. D. Young, “The formation and annealing of hot-carrier-induced degradation in poly-Si TFTs MOSFETs, and SOI devices, and similarities to state-creation in a-Si:H,” IEEE Trans. Electron Devices, vol. 43, pp. 450–456, Feb. 1996.
- [1.16] C. Y. Chang, H. Y. Lin, T. F. Lei, J. Y. Cheng, L. P. Chen, and B. T. Dai, “Fabrication of thin film transistors by chemical mechanical polished polycrystalline silicon films,” IEEE Electron Device Lett., vol. 17, pp. 100–102, Feb. 1996.
- [1.17] F. V. Farmakis, J. Brini, G. Kamarinos, and C. A. Dimitriadis, “Anomalous turn-on voltage degradation during hot carrier stress in polycrystalline silicon thin-film transistors,” IEEE Electron Device Lett., vol. 22, pp. 74–76, Jan. 2001.
- [1.18] S. Seki, O. Kogure, and B. Tsujiyama, “Leakage current characteristics of offset-gate-structure polycrystalline-silicon MOSFET’s,” IEEE Electron Device Lett., vol. 8, pp. 434-436, 1987.
- [1.19] K. Tanaka, H. Arai, and S. Kohda,“Characteristics of offset-structure polycrystalline-silicon thin-film transistors,” IEEE Electron Device Lett., vol. 9, pp. 23–25, Jan. 1988.
- [1.20] Yukiharu Uraoka, Tomoaki Hatayama, Takashi Fuyuki, Tetsuya Kawamura, and Yuji Tsuchihashi, “Reliability of Low Temperature Poly-Silicon TFTs Under Inverter Operation,” IEEE Trans. Electron Devices, VOL. 48, NO. 10, OCTOBER 2001.
- [1.21] K. Y. Choi, J. W. Lee, and M. K. Han, “Gate-overlapped lightly doped drain poly-Si thin-film transistors for large area-AMLCD,” IEEE Trans.Electron Devices, vol. 45, pp. 1272–1279, June 1998.
- [1.22] M. Hatano, H. Akimoto, and T. Sakai, “A novel self-aligned gate-overlapped LDD poly-Si TFT with high reliability and performance,” in IEDM Tech. Dig., 1997, pp. 523–526.
- [1.23] K. Ohgata, Y. Mishima, and N. Sasaki, “A new dopant activation technique for

- poly-Si TFTs with a self-aligned gate-overlapped LDD structure," in IEDM Tech. Dig., 2000, pp. 205–208.
- [1.24]A. Valletta, L. Mariucci, G. Fortunato, S. D. Brotherton, and J. R. Ayres, "Hot carrier-induced degradation of gate overlapped lightly doped drain (GOLDD) polysilicon TFTs," IEEE Trans. Electron Devices, vol. 49, pp. 636–642, Apr. 2002.
- [1.25]G. Radnoci, A. Robertsson, H. T. G. Hentzell, S. F. Gong, and M.-A. Hasan, "Al induced crystallization of a-Si," J. Appl. Phys., vol. 69, no.9, pp. 6394-6399, 1991
- [1.26] Y. Kawazu, H. Kudo, S. Onari, and T. Arai, "Low-temperature crystallization of hydrogenated amorphous silicon induced by nickel silicide formation," Jpn. J. Appl. Phys., vol. 29, pp. 2698–2704, 1990.
- [1.27]S. Y. Yoon, K. H. Kim, C. O. Kim, J. Y. Oh, and J. Jang, "Low temperature metal induced crystallization of amorphous silicon using a Ni solution," J. Appl. Phys., vol. 82, no. 11, pp. 5865–5867, 1997.
- [1.28]S. Y. Yoon, S. K. Kim, J. Y. Oh, Y. J. Choi, W. S. Shon, C. O. Kim, and J. Jang, "A high performance polycrystalline silicon thin film transistor using metal induced crystallization with a Ni solution," Jpn. J. Appl. Phys., vol. 37, pp. 7193–7197, 1998.
- [1.29]S. Yamaguchi, S. K. Park, and N. Sugii, Mater. Res. Soc. Symp. Proc.638, F14.12 (2001).
- [1.30]Y. J. Chang,<sup>b</sup> K. H. Kim,<sup>a</sup> J. H. Oh,<sup>a</sup> and Jin Janga,"Ni-Mediated Crystallization of Amorphous Silicon with a SiO<sub>2</sub> Nanocap,"Electrochemical and Solid-State Letters,vol 7,pp G207-G209,2004
- [1.31]W. S. Shon, J. H. Choi, J. H. Oh, S. S. Kim, and J. Jang, "Crystalline orientation of polycrystalline silicon with disklike grains produced by silicide-mediate crystallization of the amorphous phase," J. Appl. Phys., vol. 94, pp. 4326–4331, October 2003.
- [1.32]Hiroshi KANNO, Isao TSUNODA, Atsushi KENJO, Taizoh SADOH, Shinya YAMAGUCHI<sup>1</sup> and Masanobu MIYAO,"Metal-Induced Solid-Phase Crystallization of Amorphous SiGe Films on Insulator,"Jpn. J. Appl. Phys, Vol.42,pp. 1933-1936,2003

## Chapter 2

- [2.1] T. Serikawa, S. Shirai, A. Okamoto, and S. Suyama, “Low-temperature fabrication of high-mobility poly-Si TFTs for large-area LCDs,” IEEE Trans. Electron Devices, vol. 36, pp. 1929–1933, Sept. 1989.
- [2.2] A. Bonfiglietti, M. Cuscuna, A. Valletta, L. Mariucci, A. Pecora, G. Fortunato, S. D. Brotherton, and J. R. Ayres, “Analysis of Electrical Characteristics of Gate Overlapped Lightly Doped Drain (GOLDD) Polysilicon Thin-Film Transistors With Different LDD Doping Concentration,” IEEE Trans. Electron Devices, vol. 50, No. 12, pp. 2425-2433, 2003.
- [2.3] K. Tanaka, H. Arai, and S. Kohda, “Characteristics of offset-structure polycrystalline-silicon thin-film transistors,” IEEE Electron Device Lett., vol. 9, pp. 23–25, Jan. 1988
- [2.4] C. A. Dimitriadiis and M. Miyasaka, “Performance enhancement of offset gated polysilicon thin-film transistors,” IEEE Electron Device Lett., vol. 21, pp. 584–586, Apr. 2000
- [2.5] K.-Y. Choi, J.-W. Lee, and M.-K. Han, “Gate-overlapped lightly doped drain poly-Si thin-film transistors for large area-AMLCD,” IEEE Trans. Electron Devices, vol. 45, pp. 1272–1279, June 1998.
- [2.6] M. Hatano, H. Akimoto, and T. Sakai, “A novel self-aligned gate-overlapped LDD poly-Si TFT with high reliability and performance,” in IEDM Tech. Dig., 1997, pp. 523–526.
- [2.7] K. Ohgata, Y. Mishima, and N. Sasaki, “A new dopant activation technique for poly-Si TFTs with a self-aligned gate-overlapped LDD structure,” in IEDM Tech. Dig., 2000, pp. 205–208
- [2.8] M. Miyasaka, T. Komatsu, W. Itoh, A. Yamaguchi, and H. Ohshima, “Effects of semiconductor thickness on poly-crystalline silicon thin filmtransistors,” Jpn. J. Appl. Phys., vol. 35, p. 923, 1996.
- [2.9] T. W. Little, K. I. Takahara, H. Koike, T. Nakazawa, I. Yudasaka, and H. Ohshima, “Low temperature poly-Si TFT’s using solid phase crystallization of very thin films and an electron cyclotron resonance chemical vapor deposition gate insulator,” Jpn. J. Appl. Phys., vol. 30,no. 12B, p. 3724, 1991.
- [2.10] J. H. Jin, G. A. Gururaj, M. Yeung, H. S. Kwok, and M. Wong, “Nickel induced crystallization of amorphous silicon thin films,” J. Appl. Phys.,vol. 84, no. 1, pp. 194–200, July 1998.
- [2.11] Zhonghe JIN,. “Comparison Study of Metal Induced Lateral Crystallized and Solid-Phase Crystallized Polycrystalline Silicon Thin Film Transistors with Different Channel Thickness,”Jpn. J. Appl. Phys., vol. 40,no. 11, p. 6325-6326, 2001.

- [2.12] T.-H. Ihn, T.-K. Kim, B.-I. Lee, and S. K. Joo, “A study on the leakage current of poly-Si TFTs fabricated by metal induced lateral crystallization,” *Microelectron. Reliability*, vol. 39, pp. 53–58, 1998.
- [2.13] T. Ma and M. Wong, “Dopant and thickness dependence of metal-induced lateral crystallization of amorphous silicon films,” *J. Appl. Phys.*, vol. 91, pp. 1236–1241, 2002
- [2.14] C. Hayzelden and J. L. Batstone, “Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films,” *J. Appl. Phys.*, vol. 73, pp. 8279–8289, June 1993.
- [2.15] Ting-Kuo Chang, Ching-Wei Lin, Yuan-Hsun Chang, Chang-Ho Tseng, Fang-Tsun Chu, Huang-Chung Cheng, and Li-Jen Choub, “Thickness Dependence of Microstructure of Laterally Crystallized Poly-Si Thin Films and Electrical Characteristics of Low-Temperature Poly-Si TFTs,” *Journal of The Electrochemical Society*, vol 150, PP 494-497, 2003.
- [2.16] K.-Y. Choi, J.-W. Lee, and M.-K. Han, “Gate-overlapped lightly doped drain poly-Si thin-film transistors for large area-AMLCD,” *IEEE Trans. Electron Devices*, vol. 45, pp. 1272–1279, June 1998.
- [2.17] M. Miyasaka, T. Komatsu, W. Itoh, A. Yamaguchi, and H. Ohshima, “Effects of semiconductor thickness on poly-crystalline silicon thin film transistors,” *Jpn. J. Appl. Phys.*, vol. 35, p. 923, 1996.
- [2.18] Du-Zen Peng, Po-Sheng Shih, Hsiao-Wen Zan, Chun-Yen Chan, Ting-Chang Chang, Chiung-Wei Lin, “A novel self-aligned SiGe elevated S/D polycrystalline-silicon thin-film transistor,” *SID Digest*, pp 204-207, 2002.
- [2.19] Shengdong Zhang, Chunxiang Zhu, Johnny K. O. Sin, and Pilip K. T. Mok, “A novel ultrathin evelated channel low-temperature poly-Si TFT,” *IEEE Electron Device Lett.*, vol 20, No.11, pp. 569-571, Nov. 1999.
- [2.20] K. Marayam, J. C. Lee, and C. Hu, “A model for the electric field in light-doped drain structures,” *IEEE Trans. Electron Devices*, vol. ED-34, No. 7, pp. 1509, 1987.
- [2.21] T.Y. Huang, I.-W., A. G. Lewis, A. Chiang, and R. H. Bruce, “A simpler 100-V polysilicon TFT with improved turn-on characteristics,” *IEEE Electron Device Lett.*, vol 11, No. 6, pp. 244-246, Nov. 1990.
- [2.22] Matsumura M, Oh CH,. “Advanced excimer-laser annealing process for quasi single-crystal silicon thin-film devices. ,” *Thin Solid Films*, vol 337, pp 123–128, 1999.
- [2.23] Miyasaka M., “Excimer laser annealing of amorphous and solid-phase-crystallized silicon films.”. *J Appl Phys* ,vol 86,pp 5556–5565, 1999.

- [2.24] Farmakis FV, Tsamados D, Brini MJ, Kamarinos G,Dimitriadis CA, Miyasaka M,“ Hydrogenation in laser annealed polysilicon thin film transistors (TFTs) .”. Thin Solid Films;vol 383,pp 151–153,2001.
- [2.25] Tsai MJ, Wang FS, Cheng KL, Wang SY, Feng MS,Cheng HC. “ Characterization of H<sub>2</sub>/N<sub>2</sub> plasma passivation process for poly-Si thin-film transistors (TFTs).,” Solid-State Electron;vol 38,pp:1233–1238.,1995
- [2.26] Man Wong, Zhonghe Jin, Gururaj A. Bhat, , Philip C. Wong, and Hoi Sing Kwok. “ Characterization of the MIC/MILC Interface and Its Effects on the Performance of MILC Thin-Film Transistors.,” IEEE Trans. Electron Devices, vol.47, No. 5, pp. 1061-1067 , MAY 2000.
- [2.27] G.Fortunato,A Pecora, G. Tallarida, L. Mariucci, C.Reita , and P. Migliorato,” Hot carrier effects in n-channel polycrystalline silicon thin-film transistors a correlation between off current and transconductance variations,” IEEE Trans. Electron Devices, vol.41, No. 3, pp. 340-346 , 1994
- [2.28]N. D. Young, “The formation and annealing of hot-carrier-induced degradation in poly-Si TFTs MOSFETs, and SOI devices, and similarities to state-creation in a-Si:H,” IEEE Trans. Electron Devices, vol. 43,pp. 450–456, Feb. 1996.
- [2.29]L. Mariucci, G. Fortunato, R. Carluccio, A. Pecora, S. Giovannini, F. Massussi, L. Colalongo, and M. Valdinoci, “Determination of hot-carrier induced interface state density in polycrystalline silicon thin-film transistors,” J. Appl. Phys., vol. 84, pp. 2341–2348, 1998.
- [2.30]F. V. Farmakis et al., “Hot-carrier phenomena in high temperature processed undoped-hydrogenated n-channel polysilicon thin film transistors (TFT’s),” Solid-State Electron., vol. 43, p. 1259, 1999.
- [2.31]. J. Levinson, F. R. Shepherd, P. Scanlon, W. D. Westwood, G. Este, and M. Rider, “Conductivity behavior in polycrystalline semiconductor thin film transistors,” J. Appl. Phys., vol. 53, no. 2, p. 1193, Feb. 1982.
- [2.32]. .V. Farmakis, J. Brini, G. Kamarinos, and C. A. Dimitriadis, “Anomalous turn-on voltage degradation during hot-carrier stress in polycrystallinesilicon thin-film transistors,” IEEE Electron Device Lett., vol. 22,pp. 74–76, Feb. 2001.
- [2.33]G. A. Armstrong, S. Uppal, S. D. Brotherton, and J. R. Ayres, “Differentiation of effects due to grain boundary traps in laser annealed poly-Si thin film transistors,” Jpn. J. Appl. Phys., vol. 37, pp. 1271–1276, 1998.
- [2.34]A. Hatzopoulos, N. Archontas, N. A. Hastas, C. A. Dimitriadis, Member, IEEE, G. Kamarinos, N. Georgoulas, and A. Thanailakis, “Change in Transfer and Low-Frequency Noise Characteristics of n-Channel Polysilicon TFTs Due to Hot-Carrier Degradation,” IEEE Electron Device Lett., vol. 25, pp.390–392,

JUNE. 2004.

- [2.35]B. Doyle, M. Bourcerie, J.-C. Marchetaux, and A. Boudou, “Interface state creation and charge trapping in the medium-to-high voltage range ( $V > V > V = 2$ ) during hot-carrier stressing of n-MOS transistors,” IEEE Trans. Electron Devices, vol. 37, no. 4, pp. 744–754, Apr. 1990
- [2.36]J. R. Ayres, S. D. Brotherton, D. J. McCulloch, and M. J. Trainor, “Analysis of drain field and hot carrier stability of poly-Si thin film transistors,” Jpn. J. Appl. Phys., vol. 37, pp. 1801–1808, 1998.



## Chapter 3

- [3.1] PR. B. Iverson and R. Reif, "Recrystallization of amorphized polycrystalline silicon films on SiO<sub>2</sub> : Temperature dependence of the crystallization parameters," *J. Appl. Phys.*, vol. 62, no. 5, pp. 1675–1680, Sept.
- [3.2] J. S. Im and R. S. Sposili, "Crystalline Si films for integrated activematrix liquid crystal displays," *MRS Bull.*, vol. 21, no. 3, pp. 39–48, 1996
- [3.3] G. Radnoci et al., "Al induced crystallization of a-Si," *J. Appl. Phys.*, vol. 69, pp. 6394–6399, May 1991.
- [3.4] S. Y. Yoon, K. H. Kim, C. O. Kim, J. Y. Oh, and J. Jang, "Low temperature metal induced crystallization of amorphous silicon using a Ni solution," *J. Appl. Phys.*, vol. 82, no. 11, pp. 5865–5867, 1997.
- [3.5] S. Y. Yoon, S. K. Kim, J. Y. Oh, Y. J. Choi, W. S. Shon, C. O. Kim, and J. Jang, "A high performance polycrystalline silicon thin film transistor using metal induced crystallization with a Ni solution," *Jpn. J. Appl. Phys.*, vol. 37, pp. 7193–7197, 1998.
- [3.6] Hiroshi Kanno, Atsushi Kenjo, Taizoh Sadoh, and Masanobu Miyao, "Modified metal-induced lateral crystallization using amorphous Ge/Si layered structure," *Appl. Phys. Lett.*, Vol 85, pp 899-901, AUGUST 2004.
- [3.7] Hiroshi Kanno, Atsushi Kenjo, Taizoh Sadoh, Masanobu Miyao, "Enhancement of metal-induced crystallization in Ge/Si/Ni/SiO<sub>2</sub> layered structure," *Thin Solid Films*, pp 324–327, 2004.
- [3.8] C. Hayzelden and J. L. Batstone, "Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films," *J. Appl. Phys.*, vol. 73, pp. 8279–8289, 1993.
- [3.9] W. S. Shon, J. H. Choi, J. H. Oh, S. S. Kim, and J. Jang, "Crystalline orientation of polycrystalline silicon with disklike grains produced by silicide-mediated crystallization of the amorphous phase," *J. Appl. Phys.*, vol. 94, pp. 4326–4331, October 2003.
- [3.10] Y. J. Chang,<sup>b</sup> K. H. Kim,<sup>a</sup> J. H. Oh,<sup>a</sup> and Jin Janga, "Ni-Mediated Crystallization of Amorphous Silicon with a SiO<sub>2</sub> Nanocap," *Electrochemical and Solid-State Letters*, vol 7, pp G207-G209, 2004.
- [3.11] M. Moniwa, K. Kusukawa, M. Ohkura, and E. Takeda, "Controlling the Solid-Phase Nucleation of Amorphous Si by Means of a Substrate Step Structure and Local Phosphorus Doping", *Jpn. J. Appl. Phys.*, vol 32, pp 312-317 ,1993.
- [3.12] Z. Jin, K. Moulding, H. S. Kwok, and M. Wong, "The effects of extended heat treatment on Ni induced lateral crystallization of amorphous silicon thin films,"

- IEEE Trans. Electron Devices, vol. 46, pp. 78–82, Jan. 1999.
- [3.13]T.-H. Ihn, B.-I. Lee, S.-K. Joo, and Y.-C. Jeon, “Electrical stress effect on poly-Si thin film transistors fabricated by metal induced lateral crystallization,”Jpn. J. Appl. Phys., vol. 36, p. 5029, 1997.
- [3.14]J. H. Choi, D. Y. Kim, B. K. Choo, W. S. Shon, and J. Jang, “Metal induced lateral crystallization amorphous silicon through a silicon nitride cap layer,” Electrochem. Solid-State Lett., pp. G16–G18, 2003
- [3.15]PR. B. Iverson and R. Reif, “Recrystallization of amorphized polycrystalline silicon films on SiO : Temperature dependence of the crystallization parameters,” J. Appl. Phys., vol. 62, no. 5, pp. 1675–1680, Sept 1987.
- [3.16]I.-W. Wu, A. Chiang, M. Fuse, L. Öveçoglu, and T. Y. Huang, “Retardation of nucleation rate for grain size enhancement by deep silicon ion implantation of low-pressure chemical vapor deposited amorphous silicon films,” J. Appl. Phys., vol. 65, no. 10, pp. 4036–4039, May 1989.
- [3.17]S. Girginoudi, D. Girginoudi, A. Thanailakis, N. Georgoulas, J. Appl. Phys, Vol 84 ,pp 1968,1998.
- [3.18]M. Wang, Z. Meng, and M. Wong, “The effects of high temperature annealing on metal-induced laterally crystallized polycrystalline silicon,”IEEE Trans. Electron Devices, vol. 47, pp. 2061–2067, Nov. 2000.
- [3.19]A. Mimura, N. Konishi, K. Ono, J.-I. Ohwada, Y. Hosokawa, Y. A.Ono, T. Suzuki, K. Miyata, and H. Kawakami, “High-performance low temperature poly-Si n-channel TFT’s for LCD,” IEEE Trans. Electron Devices, vol. 36, pp. 351–358, Feb. 1989.
- [3.20]J. H. Kim, J. Y. Lee, and K. S. Nam, “High-resolution transmission electron microscopy study of solid phase crystallized silicon thin film on SiO : Crystal growth and defects formation,” J. Appl. Phys., vol. 77, p.95, 1995.
- [3.21]S. Y. Yoon, J. Y. Oh, C. O. Kim, and J. Jang, “Low temperature solidphase crystallization of amorphous silicon at 380 C,” J. Appl. Phys.,vol. 84, p. 6463, 1998.
- [3.22]D. J. Dimaria and J. W. Stasiak, “Trap creation in silicon dioxide produced by hot electrons,” J. Appl. Phys., vol. 65, pp. 2342–2356, 1989.
- [3.23]I. W. Wu et al., “Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation,” IEEE Electron Device Lett., vol. 12, Apr. 1991.
- [3.24] K. Y. Choi, J. S. Yoo, M. K. Han, and Y. S. Kim, “Hydrogen passivation on the grain boundary and intragranular defects in various polysilicon thin film transistors,” Jpn. J. Appl. Phys., pt. I, vol. 35, pp. 915–918, Feb. 1996.
- [3.25]Hiroshi Kanno, Atsushi Kenjo, Taizoh Sadoh, and Masanobu Miyaoa, "Modified metal-induced lateral crystallization using amorphous Ge/Si layered structure,"

Appl. Phys. Lett ,Vol 85,pp 899-901, AUGUST 2004

- [3.26]Qin, Ming; Poon, M.C.; Fan, L.J.; Chan, M.; Yuen, C.Y.; Chan, W.Y, "Study of grain growth of polysilicon formed by nickel-induced-lateral-crystallization of amorphous silicon and subsequent high temperature annealing,"Thin Solid Films,vol 406,pp 17-22, March, 2002
- [3.27]Hiroshi KANNO, Isao TSUNODA, Atsushi KENJO, Taizoh SADOH, Shinya YAMAGUCHI1 and Masanobu MIYAO,"Metal-Induced Solid-Phase Crystallization of Amorphous SiGe Films on Insulator,"Jpn. J. Appl. Phys, Vol.42,pp. 1933-1936,2003.



## **Appendix**

- [A.1] J. Levinson, G. Este, M. Rider, P. J. Scanlon, F. R. Shepherd, and W. D. Westwood, "Conductivity behavior in polycrystalline semiconductor thin film transistor," *J. Appl. Phys.*, Vol.53, no.2 ,p. 1193,1982.
- [A.2] J. Y. W. Seto," The electrical properties of polycrystalline silicon films," *J. Appl. Phys.* vol. 46,no. 12, p.5247, 1975.
- [A.3] R. E. Proano et al., "Development and electrical properties of undoped polycrystalline silicon thin film transistors," *IEEE Trans. Electron Devices*, vol. 36, no.9, p. 1915, 1989.
- [A.4] P. V. Necliudov, M. S. Shur, D.J. Gundlach, T. N. Jackson, "modeling of organic thin film transistors of different designs," *J. Appl. Phys*, vol.88, No. 11,Dec. 2000.
- [A.5] Shengwen Luan and Gerold W. Neudeck, " An experimental study of source/drain parasitic resistance effects in amorphous silicon thin film transistors," *J. Appl. Phys.*, vol. 72(2),No. 15 ,Jul. 1992.

