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論文題目：1.8 伏金氧半低雜訊放大器應用於超寬頻 3.1-10.6GH_Z 無線接收端

A 1.8 -V CMOS LNA applied for Ultra-Wideband 3.1 to 10.6GH_Z Wireless Receivers

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摘要

本論文研製一個應用於超寬頻 3.1-10.6 GHz 的低雜訊放大器是採用電感-電容階梯式做輸入匹配，而在輸出端是用 L-section 做匹配。本研究是以 0.18 微米互補式金氧半製程實現。此低雜訊放大器是以兩級放大為主架構，第一級為 CS-CG 堆疊結構，是為了改善逆向隔離 S_{12} 及頻率響應，第二級為 Darlington pair 結構，可以增加單位增益頻寬 f_T。為了能在所應用的頻段內達到相對的平坦增益，利用 shunt peaking 的方法去實現。供應電壓 V_{DD} 為 1.8 伏特時，整個電路功率消耗約為 22mW，及包含 pad 的情況下整個電路大小約為 1 mm^2。本研究的低雜訊放大器所量測的規格，平均順向增益(S_{21})約為 7dB，逆向隔離(S_{12})約為-35dB，S11 約為-7dB，S22 約為-8dB。而平均雜訊指數約為 8dB。

A 1.8 -V CMOS LNA applied for Ultra-Wideband 3.1 to 10.6GH$_Z$ Wireless Receivers

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Abstract

A 3.1-10.6 GH$_Z$ low noise amplifier is applied for ultra-wideband, it introduces LC ladder for input matching. And L section is used for output matching. This research is fabricated in 0.18- μm CMOS process. Two amplified stages are formed for main topology in low noise amplifier. The first stage introduces CS-CG cascode configuration, it can improve the reverse isolation and frequency response. The second stage introduce Darlington pair configuration, it can boost the unity gain bandwidth. Relatively flat gain is essential over the entire desired band. The low noise amplifier introduces the shunt peaking to achieve the above purpose. The total power dissipation of the chip is about 22 mW at power supply 1.8 volt. The chip size included pad is 1 mm^2. The measurement result of this study expect that the average forward S_{21} is 7 dB, the reverse isolation S_{12} is -35 dB, the magnitude of S_{11} is -7 dB, the magnitude of S_{22} is -8 dB, and the noise figure is 8 dB.

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Chapter 1

Introduction

1.1 Motivation

Ultra-wideband (UWB) system is a new wireless technology capable of transmitting data over a wide spectrum frequency bands with very low power and high date rates. It communicates with short pulses on the order of nanoseconds, thus spreading the energy of the radio signal over a very wide bandwidth. Compared to traditional narrow band communication systems, UWB technology has the promising ability to provide high data rate at low cost with relatively low power consumption. The FCC has allocated 7.5 GH_Z of spectrum for unlicensed use of UWB devices in the 3.1 to 10.6 GH_Z frequency band. The low noise amplifier needs to amplify the received UWB signal with sufficient gain and as little as possible. From Shannon's equation $C = B\log(1+\frac{BS_0}{BN_0})$ for the channel capacity, we know that a UWB wireless network, the bandwidth will likely be much higher than the data rate, so that the system can operate at very low signal to noise ratio [1].

For the overwhelming majority DSP chips, most designer introduces the CMOS process to achieve system on chip (SOC). But for analog and radio frequency chips, due to the electricity, noise and other parameters have strict demands. In order to achieve the specification of the products, different communication systems have different demands in process. In the past, due to G_aA_s process has excellent high frequency parameters, so most designer introduces the G_aA_s process to design theirs products. But the deep sub-micro CMOS process has acceptable high frequency parameters. Recently there are designers introduce 0.25 micrometer, 0.18 micrometer or 0.13 micrometer CMOS process to design radio frequency transceivers. Because CMOS process's cost is less

expensive than other process's. And that radio frequency transceiver introduces CMOS process is facile integration with base-band circuit. Achieving perfection of the SOC is feasible in future.

Chapter 2

Basic Concept in RF Design

2.1 Nonlinear Effect in RF Circuits

While many RF circuits can be approximated with a linear model to obtain their response to small signals, nonlinearities often lead to interesting and important phenomena. For simplicity, we assume that

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{1}$$

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency.

If $x(t) = A\cos\omega t$, then

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 A^3 \cos^3 \omega t \tag{2}$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \tag{3}$$

In Eq. (3), then term with the input frequency is called the "fundamental" and the higher-order terms the "harmonics." The amplitude of the *n*th harmonic consists of a term proportional to A^n.

In (3) this occurs if $\alpha_3 < 0$. Written as $\alpha_1 + \frac{3\alpha_3 A^2}{4}$, the gain is therefore a decreasing function of A. In most circuits, the output is a "compressive" or "saturating" function of the input; that is, the gain approached zero for sufficiently high input levels. This effect is quantified by the "1-dB compression point," defined as the input signal level that causes the small-signal gain to drop by 1 dB. If plotted on a log-log scale as a function of the input level, the output level falls below its ideal value by 1 dB at the 1-dB compression point.

When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are not harmonics of the input frequencies. Called intermodulation (IM), this phenomenon arises from multiplication of the two signals when their sum is raised to a power greater than unity. We assume that

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \tag{4}$$

Thus,

$$y(t) = \alpha_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 + \alpha 3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \tag{5}$$

Expanding the left side and discarding DC terms and harmonics, we obtain the intermodulation products:

$$\omega \to 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1{}^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1{}^2 A_2}{4} \cos(2\omega_1 - \omega_2)t \tag{6}$$

$$\omega \to 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2{}^2 A_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_2{}^2 A_1}{4} \cos(2\omega_2 - \omega_1)t \tag{7}$$

Because the difference between ω_1 and ω_2 is small, the components at $2\omega_1$-ω_2 and $2\omega_2$-ω_1 appear in the vicinity of ω_1 and ω_2. In a typical two-tone test, A_1=A_2=A, and the ratio of the amplitude of the output third-order products to α_1A defines the IM distortion. If a weak signal accompanied by two strong interferers experiences third-order nonlinearity, then one of the IM products falls in the band of interest, corrupting the desired component.

Use IP_3 to characterize this behavior. Called the “third intercept point” (IP_3), this parameter is measured by a two-tone test in which A is chosen to be sufficiently small so that higher-order nonlinear terms are negligible and the gain is relatively constant

and equal to α_1. The third-order intercept point is defined to be at the intersection of the two lines [2].

2.2 Noise

Noise is usually generated by the random motions of charges or charge carriers in devices and materials. Because the noise process is random, one cannot identify a specific value of voltage at a particular time, and the only recourse is to characterize the noise with statistical measures, such as the mean-square or root-mean-square values. Because of having various noise sources in the circuit, we need to simplify calculation of the total noise at the output [3]. Obviously, the output-referred noise does not allow a fair comparison of the performance of different circuits because it depends on the gain. According the circuit theory, we can use the input-referred noise of circuits to represent the noise of behavior in the circuits. To overcome the above confusion, we specify the "input-referred noise" of circuits. Illustrate conceptually in Fig. 2-2. To represent the effect of all noise sources in the circuit by a single noise source. The input-referred noise and the input signal are both multiplied by the gain as they are processed by the circuit. Thus, the input-referred noise indicates how much the input signal is corrupted by the circuit's noise. The input-referred noise is a spurious quantity in that in cannot be measured at the input of the circuit. The two circuits of Figs. 2-2(a) and (b) are equivalent in mathematics but the real physical circuit is still that in Fig. 2-2(b). The noise of a two-port network can be modeled by two input noise sources: a series voltage source and a parallel current source. Generally, the correlation between the two sources must be taken into account. The situation is shown in Fig. 2-3, where a two-port network containing noise sources is represented by the same network with internal noise sources removed and with a noise voltage and current source connected at the input. It can be shown that this representation is valid for any source impedance, provided that

correlation between the two noise sources is considered [4].

The signal-to-noise ratio (SNR), defined as the ratio of the signal power to the total noise power, is an important parameter. In RF circuit, most of the front-end receiver blocks are characterized in terms of their "noise figure" rather than the input-referred noise. Noise figure has many different definitions. The most commonly accepted definition is

$$\text{noise figure} = \frac{SNR_{in}}{SNR_{out}}, \tag{8}$$

Noise figure is a measure of how much the SNR degrades as the signal passes through a circuit. If a circuit has no noise source, the SNR_{out}=SNR_{in}, regardless of the gain.

The noise figure of a two-port amplifier is given by

$$F = F_{\min} + \frac{r_n}{g_s}\left|y_s - y_{opt}\right| \tag{9}$$

where r_n is the equivalent normalized noise resistance of the two-port, y_s=g_s+jb_s represents the normalized source admittance, and y_{opt}=g_{opt}+jb_{opt} represents the normalized source admittance which results in the minimum noise figure, called F_{min}. If we express y_s and y_{opt} in terms of the reflection coefficients Γ_s and Γ_{opt}.

$$y_s = \frac{1-\Gamma_s}{1+\Gamma_s} \tag{10}$$

$$y_{opt} = \frac{1-\Gamma_{opt}}{1+\Gamma_{opt}} \tag{11}$$

Substitute (10) and (11) into (9) results in the relation

$$F = F_{\min} + \frac{4r_n\left|\Gamma_s - \Gamma_{opt}\right|^2}{(1-\left|\Gamma_s\right|^2)\left|1+\Gamma_{opt}\right|^2} \tag{12}$$

When Γ_s=Γ_{opt} occurs, the value of F is equal to F_{min}. F_{min} is a function of the device bias current and operating frequency [5].

For a cascade of stages, the overall noise figure can be obtained in terms of the NF and gain of each stage. For m-stages, the NF_{tot} is equal to

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \cdots A_{p(m-1)}} \tag{13}$$

where A_{pm} is the available power gain of the m-th stage. This is called the Friis equation. The Friis equation indicates that the noise contributed by each stage decreases as the gain preceding the stage increases, implying that the first few stages in a cascade are the most critical [2].

2.3 Cascaded Nonlinear Stages

Since in RF systems, signals are processed by cascaded stages, it is important to know how the nonlinearity of each stage is referred to the input of the cascade. Consider two nonlinear stages in cascade. As shown in Fig.2-4. Assuming that the input-output relationship is

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{14}$$

$$y_2(t) = \beta_1 y_1(t) + \beta_2 y_1^{\,2}(t) + \beta_3 y_1^{\,3}(t)\,. \tag{15}$$

Substitute (14) into (15) results in the relation

$$y_2(t) = \alpha_1\beta_1 x(t) + (\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^{\,3}\beta_3)x^3(t) \tag{16}$$

. If we consider only the first- and third-order terms, then

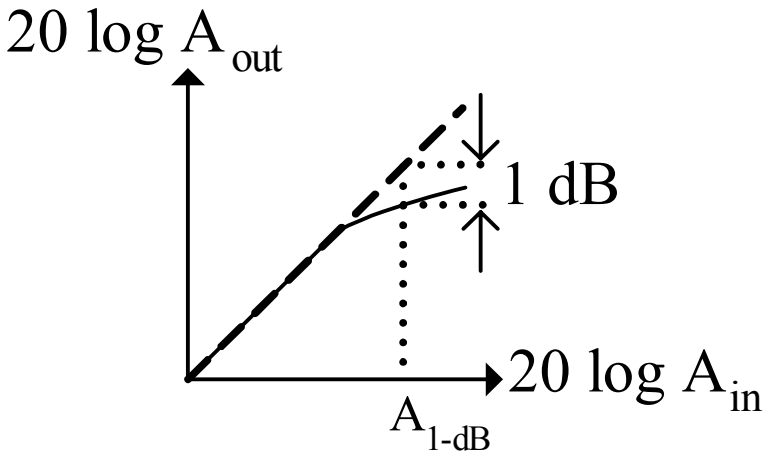
$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1\beta_1}{\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^{\,3}\beta_3}\right|}\,. \tag{17}$$

From equation (17) can be simplified if the two sides are inverted and squared:

$$\frac{1}{A^2_{IP3}} = \frac{1}{A^2_{IP3,1}} + \frac{3\alpha_2\beta_2}{2\beta_1} + \frac{\alpha_1^{\,2}}{A^2_{IP3,2}}\,, \tag{18}$$

where $A_{IP3,1}$ and $A_{IP3,2}$ represent the input IP_3 points of the first and second stages, respectively. From the above result, we note that as α_1 increases, the overall IP_3 decreases. This is because with higher gain in the first stage, the second stage senses larger input levels, thereby producing much greater

IM_3 products [2].



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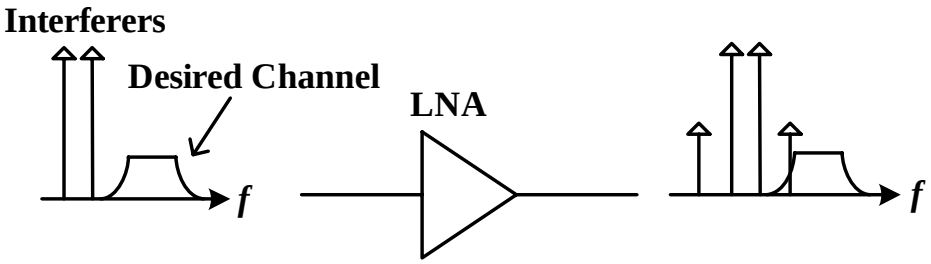

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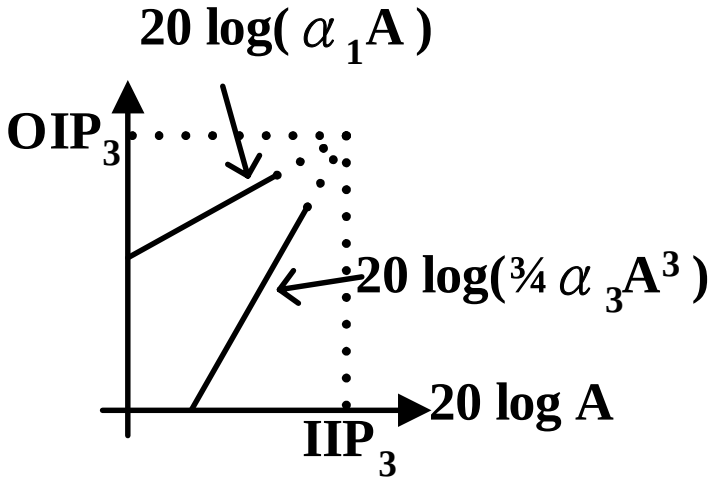
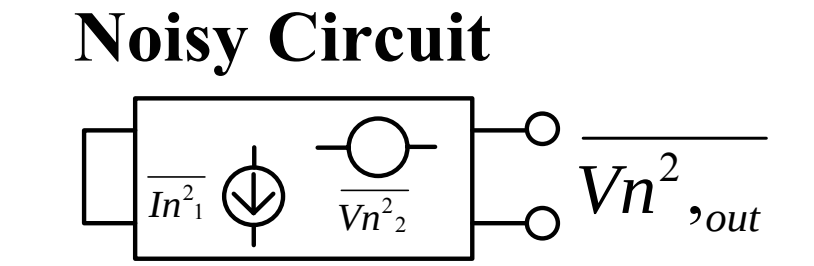
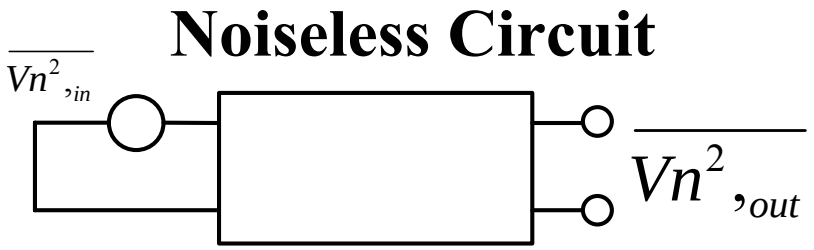


(c)

Fig. 2-1 (a) Definition of the 1-dB compression point, (b) Corruption of a signal due to intermodulation, (c) The third-order intercept point

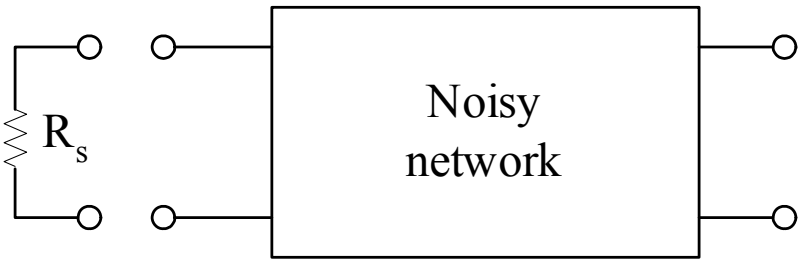


(a)

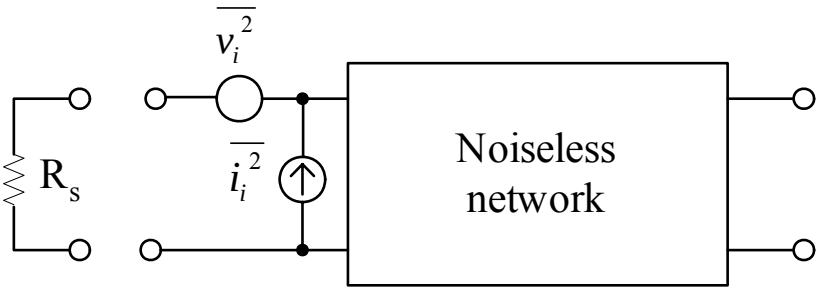


(b)

Fig. 2-2 Determination of input-referred noise voltage.



(a)



(b)

Fig. 2-3 Representation of noise in a two-port network by equivalent input voltage and current sources.

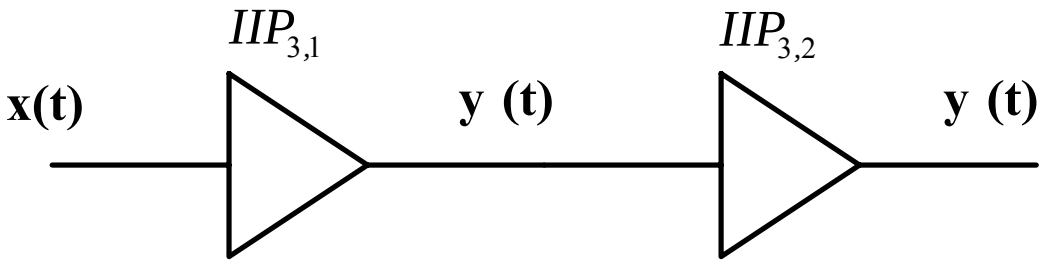


Fig. 2-4 Cascaded nonlinear stages.

Chapter 3

Basic Low-Noise Amplifiers Design

3.1 General consideration in Low-Noise Amplifiers

The stability of an amplifier is a very important consideration in a design and can be determined from the S parameters, the matching networks, and the terminations. A two-port network to be unconditionally stable can be derived from (19) to (22).

$$|\Gamma_s| < 1 \tag{19}$$

$$|\Gamma_L| < 1 \tag{20}$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{21}$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_S} \right| < 1 \tag{22}$$

The two-port network is shown in Fig. 3-1. For unconditional stability any passive load or source in the network must produce a stable condition. The solution of (19) to (22) gives the required conditions for the two-port network to be unconditionally stable [].

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{23}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{24}$$

A convenient way of expressing the necessary and sufficient conditions for unconditional stability is

$$k > 1 \tag{25}$$

$$|\Delta| < 1. \tag{26}$$

The need for matching networks arises because amplifiers, in order to deliver maximum power to a load or to perform in a certain desired way, must be properly terminated at both the input and the output ports. Figure 3.2 illustrates a typical situation in which a transistor, in order to deliver maximum power to the 50-ohm load, must have the terminations Z_S and Z_L. The input matching network is designed to transform the generator impedance to the source impedance Z_S, and the output matching network transforms the 50-ohm termination to the load impedance Z_L. In a resonant circuit, the ratio of its resonant frequency f_o to its bandwidth is known as the loaded Q of circuit. That is,

$$Q_L = \frac{\omega_o}{BW} \tag{27}$$

The matching networks in Fig. 3-3 are used to provide a match at a certain frequency. The frequency response of a matching network can be classified as either a two-pole low-pass filter or a high-pass filter. At each node of the matching networks, there is an equivalent series input impedance, denoted by R_S+jX_S. Hence, a circuit node Q, denoted by Q_n, can be defined at each node as

$$Q_n = \frac{|X_S|}{R_S} \tag{28}$$

If the equivalent parallel input admittance at the node is G_P+jB_P, the circuit node Q can be expressed in the form

$$Q_n = \frac{|B_P|}{G_P} \tag{29}$$

In order to obtain a high value of Q_L, the circuit node Q must be high. Higher values of Q_L than those obtained with the matching networks in Fig 3-3 can be obtained using matching circuits with three elements. The addition of a third element to a matching networks in Fig 3-3 results in either the lossless Tee network or the lossless Pi network. The addition of a third element introduces flexibility in the selection of the loaded Q, since the equivalent series impedance at the nodes in the circuit will determine various

values of Q_n. Obviously, a high value of Q_n in the circuit will result in a high value of Q_L. However, it is not simple to exactly relate Q_n to Q_L in these circuits. The Q of a Tee or Pi network is normally taken as the highest value of Q_n in the circuit. The upper and lower parts of the constant-Q contours can be shown to satisfy a circle equation as follows. Since

$$z = r + jx = \frac{1+\Gamma}{1-\Gamma} = \frac{1-U^2-V^2}{(1-U)^2+V^2} + j\frac{2U}{(1-U)^2+V^2} \tag{30}$$

then

$$Q_n = \frac{|x|}{r} = \frac{2U}{1-U^2-V^2} \tag{31}$$

which can be written as

$$U^2 + \left(V \pm \frac{1}{Q_n}\right)^2 = 1 + \frac{1}{Q^2{}_n} \tag{32}$$

The plus sign applies when x is positive, and the minus sign when x is negative. Equation (32) is recognized as the equation of a circle. For $x>0$, the center in the Γ plane is at $(0, -1/Q_n)$, and for $x<0$ at $(0, 1/Q_n)$; the radius of the circle is

$$\sqrt{1 + \frac{1}{Q^2{}_n}} \tag{33}$$

In a RF amplifier, the input and output matching networks provide the appropriate ac impedances to the transistor. The transistor must also be biased at an appropriate quiescent point. A complete RF amplifier contains both dc bias components and the ac matching network. RFC_S, bypass capacitors, and coupling capacitors need to be introduced so the dc bias components do not affect the ac performance of the amplifier. Illustrate conceptually in Fig. 3-4. [5]

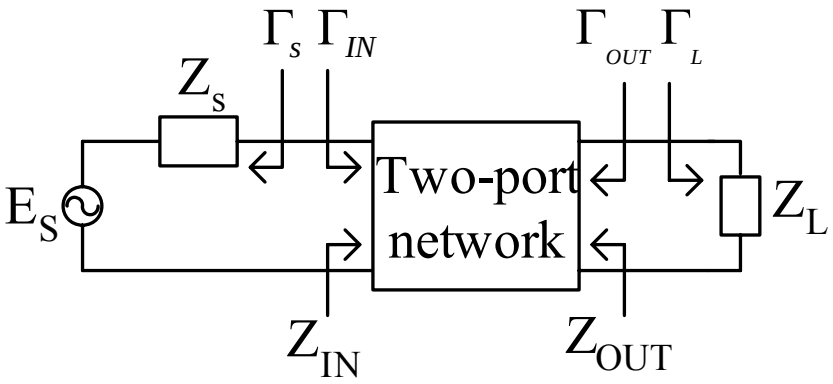


Fig. 3-1 Stability of two-port networks.

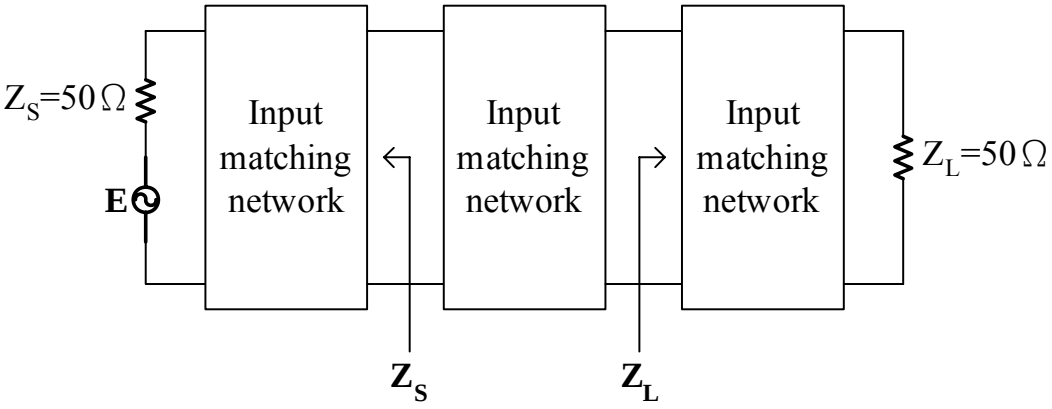


Fig. 3-2 Block diagram of an amplifier.

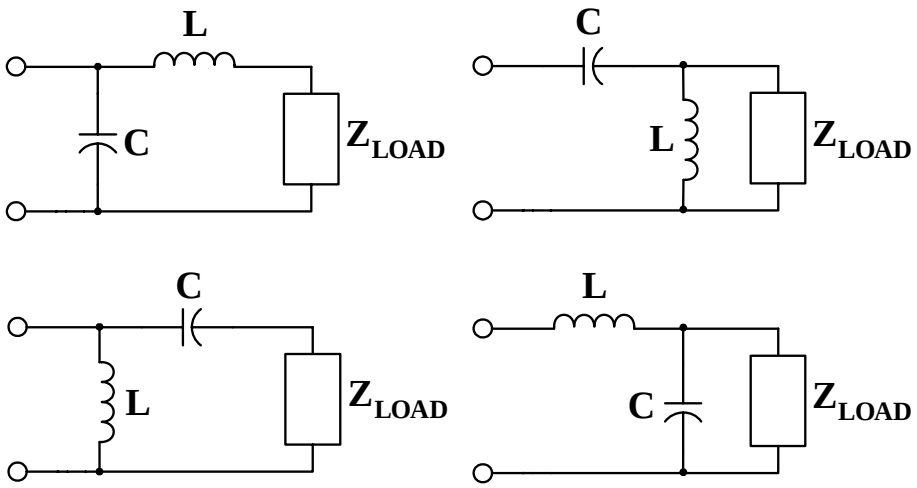
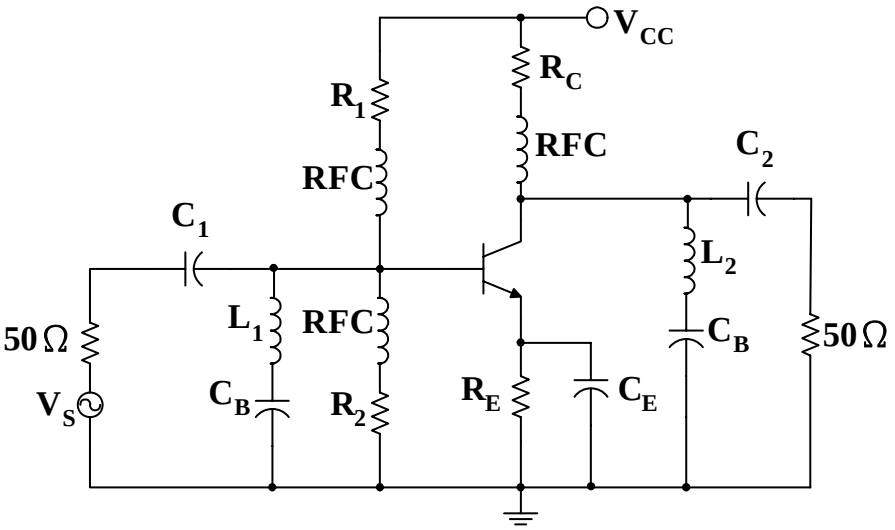
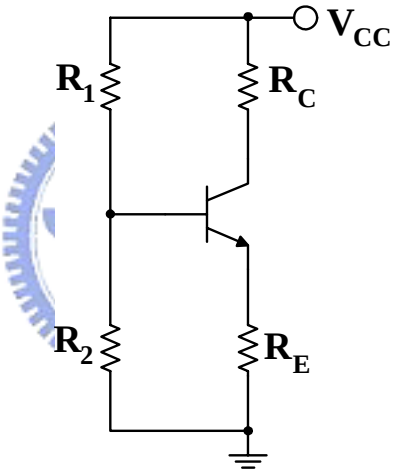


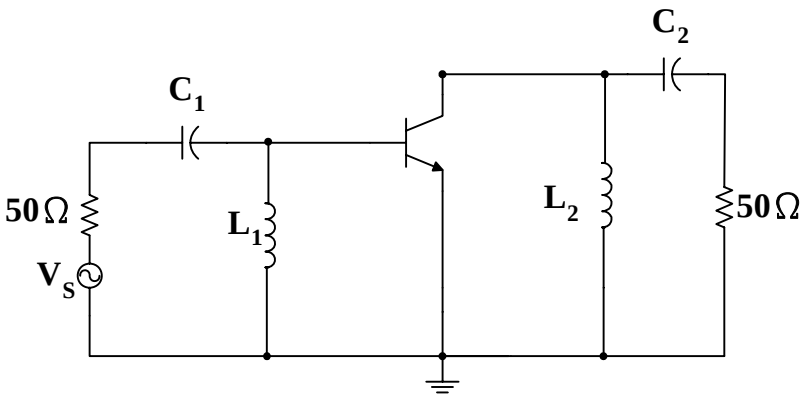
Fig. 3-3 Matching networks.



(a)



(b)



(c)

Fig. 3-4 (a) A discrete RF amplifier; (b) the dc model; (c) the ac model.

3.2 Conventional LNA design

3.2.1 Narrow band LNA design

In the design of low noise amplifier, there are many important goals. These include noise figure minimization, providing sufficient gain with good linearity, and the reasonable power consumption. Fig 3-5 illustrates the input stage of the low noise amplifier with source degeneration. A simple calculation is

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs2}} + \left(\frac{g_{m2}}{C_{gs_2}}\right)L_s \qquad (34)$$

If choose appropriate value of inductance and capacitance, then L_g+L_s and C_{gs} will resonate at certain frequency. By choosing L_s appropriately, the real term can be made equal to 50Ω. The gate inductance L_g is used to set the resonance frequency once Ls is chosen to satisfy the criterion of a 50Ω input impedance. The matching method in noise performance is better than using resistance termination of the input end.

The reverse isolation of low noise amplifier determines the amount of LO signal that leaks from the mixer to the antenna. The leakage arises from capacitive paths, substrate coupling, and bond wire coupling. In heterodyne receivers with a high first IF, the image-reject filter and the front-end duplexer significantly suppress the leakage because the LO frequency falls in their stop-band. In homodyne topology, the leakage is attenuated primarily by the LNA reverse characteristics. Equation (23) suggests that stability improves as S_{12} decrease, i.e., as the reverse isolation of the circuit increases. The feedback can be suppressed through the use of a cascade configuration, but at the cost of a somewhat higher noise figure. The common-gate transistor in the Fig 3-5, M_1, plays two important roles by increasing the reverse isolation of the LNA: (1) it lowers the LO leakage produced by the following mixer, and (2) it improves the stability of the circuit by minimizing the feedback from the output to the input [6].

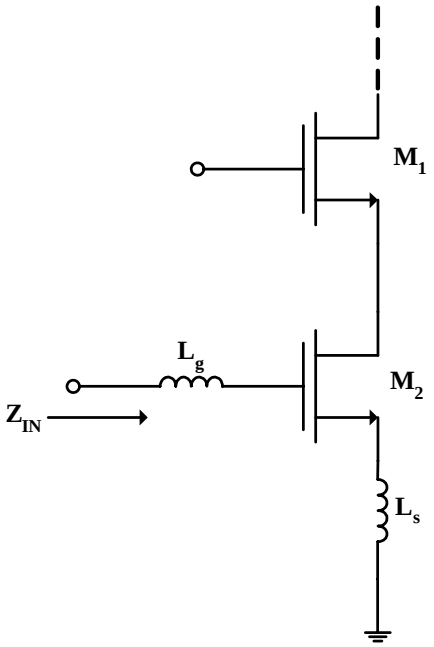


Fig. 3-5 Common source stage use inductance degeneration.

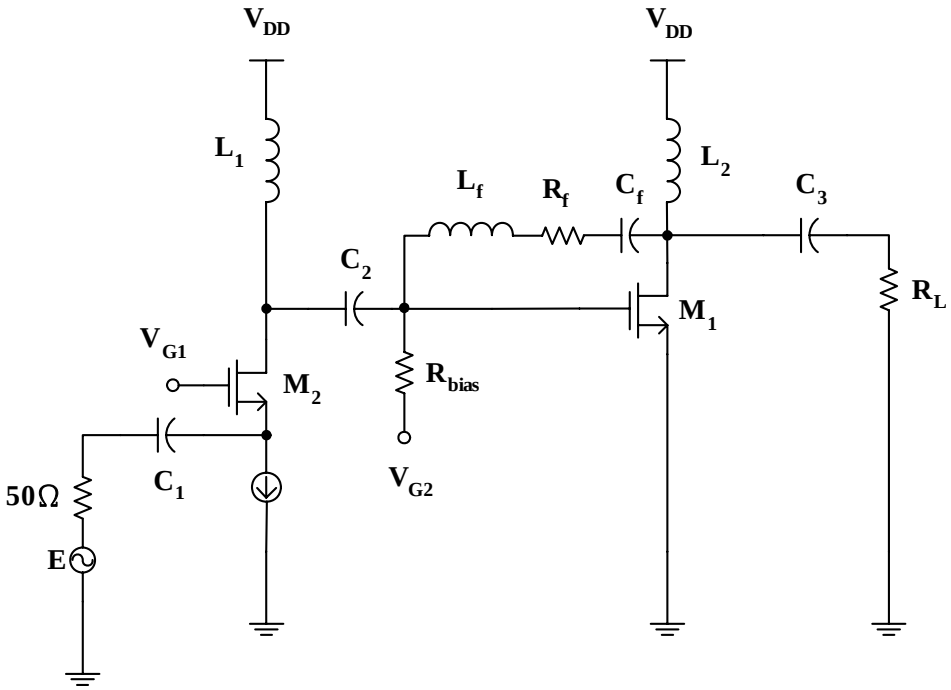


Fig. 3-6 Wide-band LNA circuit schematic.

3.2.2 wide-band LNA design

Figure 3-6 is the LNA circuit schematic. We discuss this circuit step by step from the first stage. First, to make $1/g_m = 50\Omega$, the g_m value of common gate amplifier is going to be fixed at certain trans-conductance. An additional stage is required to provide sufficient gain over the desired band. A shunt feedback common source amplifier is used in the second stage for this purpose. The first step is the selection of transistor size and bias condition of the M1 to yield $\mathrm{Re}|Z_{11}| = 1/g_m = 50\Omega$. This ensures input matching condition for wide-band of frequency. But this condition is violated with optimum noise condition. There is a trade-off between noise and impedance matching in the LNA circuit. One of the major problems in the wide bandwidth amplifier design is the limitation imposed by the gain-bandwidth product of the active device. We know that any active device has a gain roll off at high frequency because of the gate-drain and gate-source capacitance in the transistor. This effect degrades the forward gain as the frequency increases and eventually the transistor stops functioning as an amplifier at the high frequency. Therefore the second design step is the selection of optimal bias point of second stage of LNA so that it operates at its maximum f_T. In addition to this $|S_{21}|$ degradation with frequency other complications that arises in wide-bandwidth amplifier design includes, increase in reverse gain $|S_{12}|$ and noise figure at high frequency. Negative feedback configuration is used to reduce these effects and increase the bandwidth. An inductor L is connected in series with R_f such that after certain frequency the negative feedback decreases in proportion to the S_{21} roll-off. This technique improves gain flatness at high frequency. The load inductance of L_1 and L_2 replace the resistor load which is used conventionally. The magnitude of the inductor's impedance increases as frequency increases. This increase inductor impedance compensates the active device gain degradation that occurs at high frequency [7].

Another wide-band LNA design schematic is shown in Fig. 3-7. In figure 3-7, the R_f is added as a shunt feedback element to the conventional cascade narrow band LNA and L_{load} is used as shunt peaking inductor at the output. The capacitor C_f is used for the ac coupling purpose. The source follower, composed of M_3 and M_4, is added for measurement proposes only, and provides wideband output matching. C_1 and C_2 are ac coupling capacitor. The small-signal equivalent circuit at he input of the LNA is shown in Fig. 3-8. The resistor $R_{fM} = R_f /(1 - A_v)$ represents the Miller equivalent input resistance of R_f, where A_v is the open-loop voltage gain of the LNA. From equivalent circuit, the value of R_f can be much larger than that of the conventional resistance shunt-feedback. In the conventional resistance shunt-feedback, the size of R_f is limited as R_{fM} determines the input impedance. One of the key roles of the feedback resistor R_f is to reduce the Q-factor of the resonating narrowband LNA input circuit. The Q-factor of the circuit shown in Fig. 3-8 can be approximately given by

$$Q_{WB} \approx \frac{1}{\left[R_S + \omega_T L_S + \frac{(\omega_0 L_g)^2}{R_{fM}}\right] \bullet \omega_0 \bullet C_{gs}}. \tag{35}$$

From equation (35), and considering the inversely linear relation between the -3dB bandwidth and the Q-factor, the narrowband LNA in Fig. 3-7 can be converted into a wideband amplifier by the proper selection of R_f. To design a wideband amplifier that covers a certain frequency band, the narrowband amplifier will be optimized at the center frequency. The feedback resistor R_f also provides its conventional roles of flattening the gain over a wider bandwidth of frequency with much smaller noise figure degradation [8].

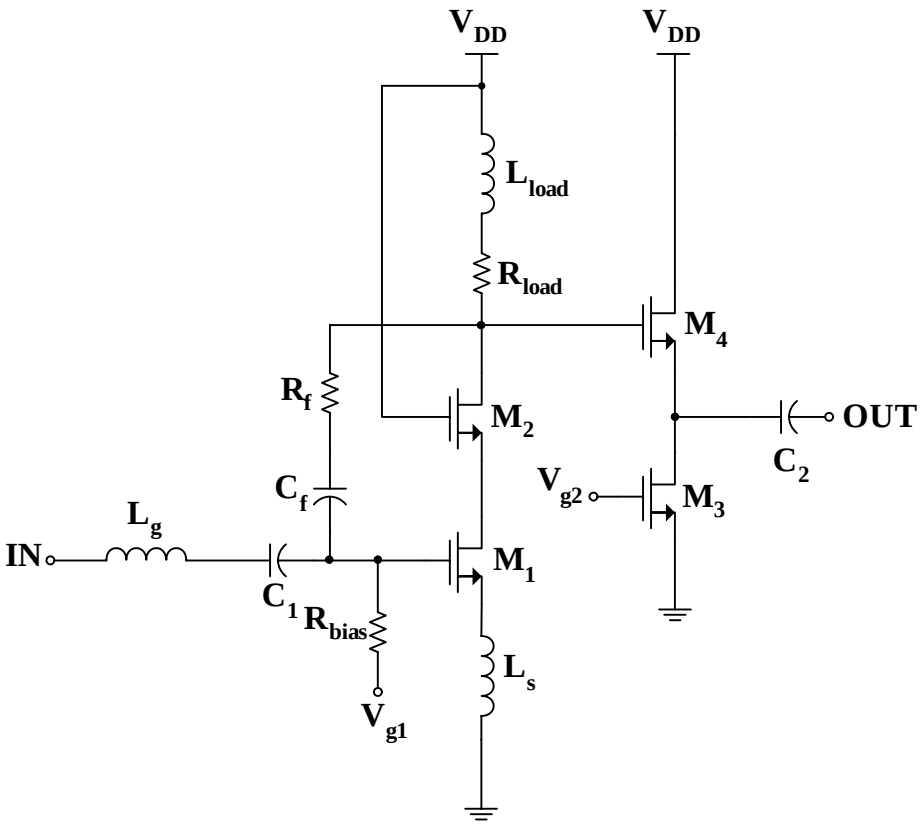


Fig. 3-7. Another wide-band LNA schematic.

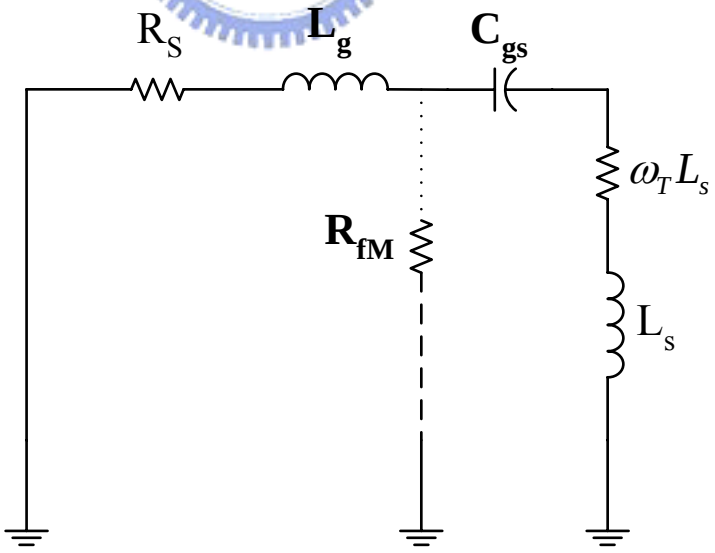


Fig. 3-8. Small-signal equivalent circuit at the input.

Another circuit topology for wide-band application is distributed amplifier (DA). Distributed amplifier was first introduced by [9]. MMIC DA was mainly implemented using G_aA_s-based or S_iG_e devices. The distributed amplifier schematic is shown in Fig. 3-9. From the Fig. 3-9, we can observe that the power gain of a cascade pair is considerably higher than that of a common-source single transistor. The input signal propagates down the gate line, with each FET tapping off some of the input power. The amplified output signals from the FETs form a traveling wave on the drain line. The propagation constants and lengths of the gate and drain lines are chosen for constructive phasing of the output signals, and the termination impedanc3es on the lines serve to absorb waves traveling in the reverse directions. According to equivalent circuit of a single unit cell of the gate line and drain line, we can get optimal number of section [10].

$$N_{opt} = \frac{\ln(\alpha_g l_g / \alpha_d l_d)}{\alpha_g l_g - \alpha_d l_d} \tag{36}$$

A small resistor R_{gx} is added in the gate of common-gate transistor to improve the entire circuit stability. The input and output impedances of the cascade device are needed. In the DA design, the input and output of the cascade FETs used in the distributed amplifier were terminated by the gate line characteristic impedance Z_{og} and drain line characteristic impedance Z_{od}, respectively. Higher gain can be obtained by choosing higher characteristic impedance of gate (Z_{og}) and drain lines (Z_{od}) but the cutoff frequency will be lower, which will limit the bandwidth. The m-derived matching section is used in our design to overcome the well-known non-constant image impedance from the constant-k sections. A de-embedded m-derived π equivalent circuit is shown in Fig. 3-10. Distributed amplifiers are not capable of very high gains or very low noise figure, however, and generally are larger in size than an amplifier having comparable gain over a narrower bandwidth.

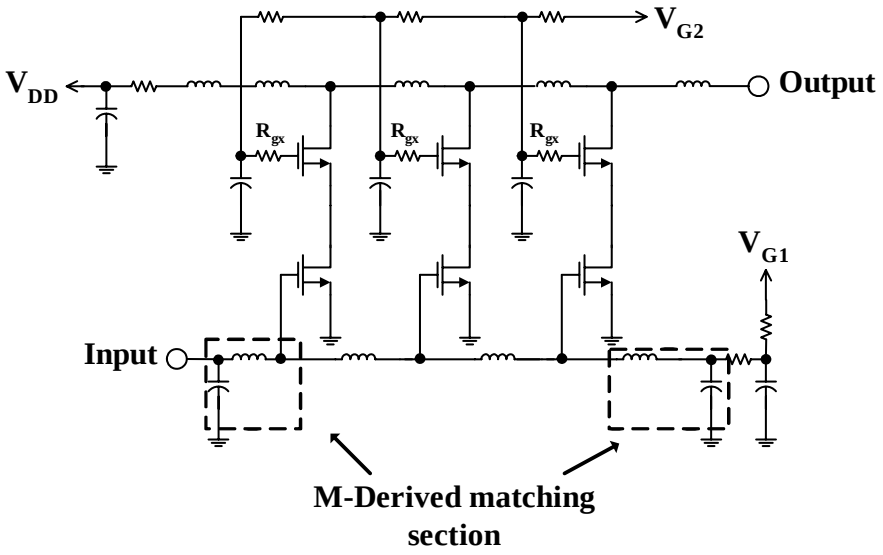


Fig. 3-9. Schematic circuit diagram of the cascade distributed amplifier.

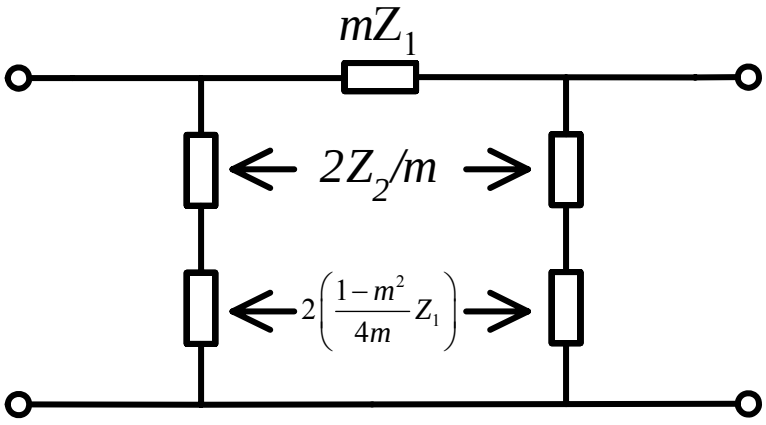


Fig. 3-10. A de-embedded m-derived π -equivalent.

Chapter 4

Ultra-Wideband CMOS LNA Design

4.1 Circuit topology and Design flow

4.1.1 Overall circuit introduction

Figure 4-1 shows the proposed ultra-wideband CMOS low noise amplifier topology. From Fig. 4-1, we can observe that it is a two stage low noise amplifier. Where, the output stage is formed by Darlington pair. Because any MOSFET has a property of gain decreases as frequency increases. The parameter ω_T represents the gain-bandwidth frequency. It is the frequency where the short circuit gain approximates unity. So, it is expected that the parameter ω_T can decide high frequency performance. Device f_T is bounded within any given technology, so it would seem that once biasing conditions that maximize f_T have been established. Equation (37) represents the f_T.

$$2\pi f_T = \frac{g_m}{C_{gs} + C_{gd}} \tag{37}$$

Briefly speaking, f_T is the ratio of trans-conductance to input capacitance. If a way could be found to, say, decreasing trans-conductance, f_T would increase. The ordinary differential pair may be considered an f_T doubler by this definition, for the device capacitances are in series as far as a differential input is concerned. Hence, the differential input capacitance is one half that of each transistor. The differential trans-conductance, on the other hand, is unchanged because, although the input voltage divides equally between the two transistors, the differential output current is twice the current in each device. Hence, the overall stage trans-conductance is equal to that of each transistor, and a doubling of f_T results [3].

The ultra-wideband is for 3.1 to 10.6 GH_Z application. The flat forward gain over the whole bandwidth is essential. A technique that satisfied this requirement of large

bandwidth at low cost is known as shunt peaking. The resistance R_d improves the gain at lower frequency. At high frequency, the L_d can improve the gain.

L-section matching network is used for measurement purposes to drive an external 50Ω load. And C_{in} and C_{out} is AC coupling capacitor. Between the first and second stage is $C_{inter\text{-}stage}$ that block the DC bias point and provide an AC path from the first stage to next stage.

The cascode topology improves the reverse isolation (S_{12}) and the frequency response of the amplifier. Because the M_2 of the cascode topology has the small input impedance, it can yield the small Miller capacitor. The cascode component is chosen as small as possible to reduce the parasitic capacitors.

4.1.2 Noise analysis

The noise contribution of the input network is due to the finite quality factor Q of the integrated inductors. The MOSFET transistor noise sources are shown in figure 4-2. In reference [11], the noise generator $\overline{i^2_d}$ is

$$\overline{i^2_d} = 4kT\left(\frac{2}{3}g_m\right)\Delta f + k\frac{I^a{}_D}{f}\Delta f \ , \tag{38}$$

where $4kT\left(\frac{2}{3}g_m\right)\Delta f$ is thermal noise component, and $k\frac{I^a{}_D}{f}\Delta f$ is flicker noise component. And noise generator $\overline{i^2_g}$ is

$$\overline{i^2_g} = 2qI_G\Delta f \ . \tag{39}$$

As shown in figure 4-2 (b), because the current gain of the source degeneration is $\beta(j\omega) = \frac{\omega_T}{j\omega}$, and the cut frequency is $\omega_T \approx \frac{g_m}{C_{gs}}$, so the $\overline{i^2_n}$ is

$$\overline{i^2_n} = \overline{i^2_g} + \frac{j\omega C_{gs}}{g_m}\overline{i^2_d} \ , \tag{40}$$

and $\overline{v^2_n}$ is

$$\overline{v^2_n} = Z\overline{i^2_g} + (1-\omega^2 C_{gs}Z)\frac{\overline{i^2_d}}{g_m}, \tag{41}$$

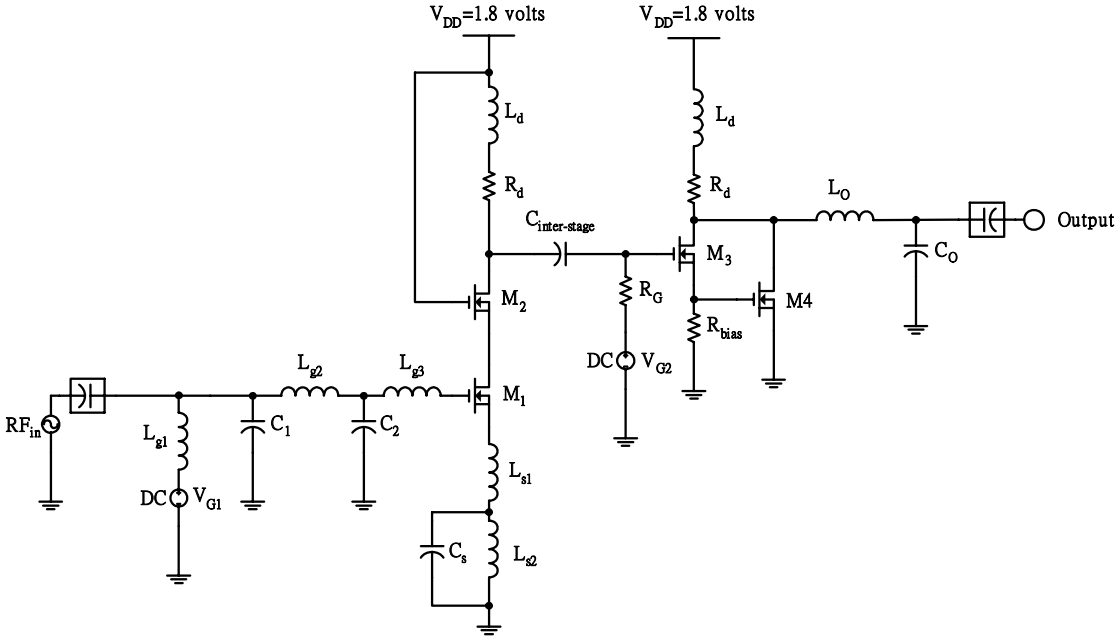
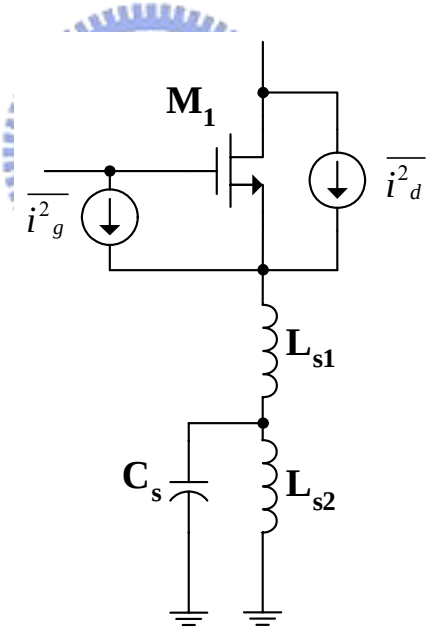
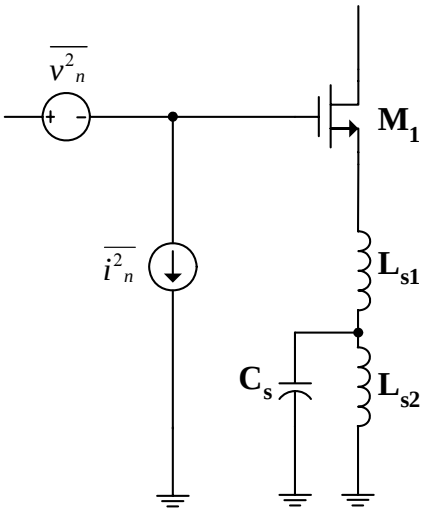


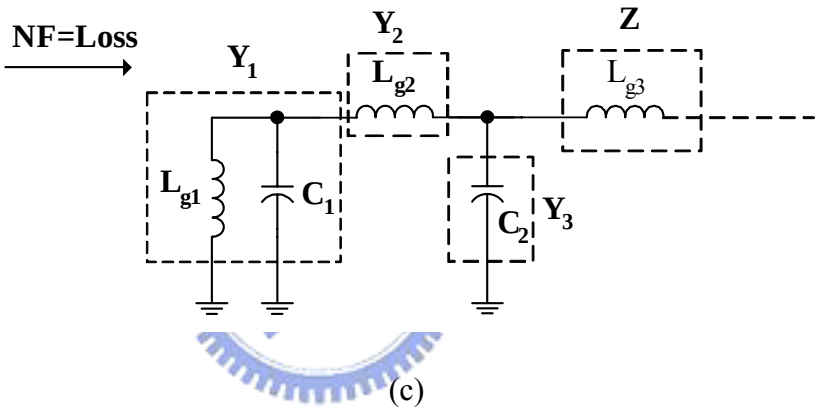
Fig.4-1. Proposed Low noise amplifier schematic.



(a)



(b)



(c)

Fig. 4-2. (a) M_1 noise sources. (b) Input-referred equivalent noise sources. (c) The part of the passive matching network.

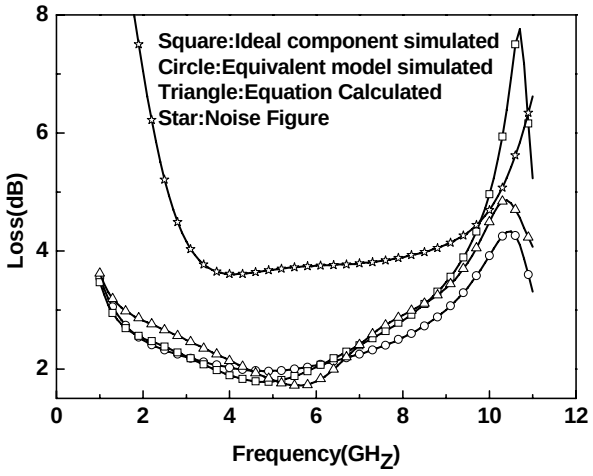


Fig.4-3. The power loss of passive network.

where Z is

$$Z = j\omega L_{s1} + \frac{j\omega L_{s2}}{1-\omega^2 C_s L_{s2}}. \tag{42}$$

For a lossy passive reciprocal network the noise figure is equal to the loss [10]. The noise contribution of the passive network in the figure 4-2 (c) is

$$10\log\left(1 - {S_{11}}^2 - {S_{21}}^2\right) \tag{43}$$

where S_{11} is equal to

$$\frac{A + B/50 - 50C - D}{A + B/50 + 50C + D}, \tag{44}$$

and S_{21} is equal to

$$\frac{2}{A + B/50 + 50C + D}. \tag{45}$$

The transmission matrix parameters [10] A is equal to

$$1 - \omega^2 C_2 L_{g2}, \tag{46}$$

and B is equal to

$$j\omega L_{g3}\left(1 - \omega_2 C_2 L_{g2}\right) + j\omega L_{g2}, \tag{47}$$

and C is equal to

$$j\omega C_2 + \frac{1-\omega^2 C_1 L_{g1}}{j\omega L_{g1}}\left(1 - \omega^2 C_2 L_{g2}\right), \tag{48}$$

and D is equal to

$$j\omega L_{g3}\left[j\omega C_2 + \frac{1-\omega^2 C_1 L_{g1}}{j\omega L_{g1}}\left(1 - \omega^2 C_2 L_{g2}\right)\right] + 1 + \frac{L_{g2}}{L_{g1}}\left(1 - \omega^2 C_1 L_{g1}\right). \tag{49}$$

The loss of the passive network is shown in figure 4-3.

4.1.3 Input matching and output matching

The input impedance of the MOS transistor with the inductive source degeneration is a series RLC circuit. The input impedance Z_2 is

$$Z_2 = s\left(L_{g3} + L_{s1}\right) + \frac{1}{sC_{gs1}} + \frac{sL_{s2}}{1+s^2C_sL_{s2}} + \frac{g_{m1}}{C_{gs1}}\left(L_{s1} + \frac{L_{s2}}{1+s^2C_sL_{s2}}\right). \quad (50)$$

And the parallel impedance Z_1 is

$$Z_1 = \frac{sL_{g1}}{1+s^2C_1L_{g1}}. \quad (51)$$

Figure 4-4 shows the two port network for calculating input impedance.

$$Y_1 = \frac{1}{Z_1}, Y_2 = \frac{1+sC_2Z_2}{Z_2}, Y_3 = \frac{1}{sL_{g2}} \quad (52)$$

$$A = 1 + \frac{Y_2}{Y_3}, B = \frac{1}{Y_3}, C = Y_1 + Y_2 + \frac{Y_1Y_2}{Y_3}, D = 1 + \frac{Y_1}{Y_3} \quad (53)$$

According to transmission matrix theory, we can find the input impedance from ABCD parameters.

$$Z_{in} = \sqrt{\frac{AB}{CD}} = \sqrt{\frac{sL_{g2} \times \left(1 + \frac{(1+sC_2Z_2)sL_{g2}}{Z_2}\right)}{\left(1 + \frac{sL_{g2}}{Z_1}\right) \times \left(\frac{1}{Z_1} + \frac{Z_2}{1+sC_2Z_2} + \frac{sL_{g2}(1+sC_2Z_2)}{Z_1Z_2}\right)}} \quad (54)$$

The Z_2 involves the real part and imaginary part. The real part of the Z2 is dependant of the operation frequency. Because in reference[6], the real part of the input impedance is $\frac{g_m}{C_{gs}}L_s$. Assume that the inductance of the L_s has fifteen percent error due to the process variation. The real part of the input impedance would have fifteen percent error. But in equation (50), the real part of the Z_2 would have only six percent error. It proves that the LC parallel network in series at the source would reduce the real part of the input impedance error.

The output impedance R_{out} of the Darlington pair is

$$R_{out} = \left[R_{bias} + (1 + g_{m3}R_{bias})r_{o3}\right] // r_{o4} \approx r_{o4}. \quad (55)$$

Because the real part of the impedance is r_{o2} parallel R_d, but the value of r_{o2} is larger than R_d. So the real part of the output impedance is about R_d. Choosing proper the value

of the Rd, can reach purpose of the output matching. The imaginary part of the output impedance is

$$\frac{sL_d}{1+s^2C_{ds4}L_d} // \left[sC_{ds3} // \left(sC_{gs4} + sC_{gd4}\left(1+g_{m4}\frac{R_d}{2}\right)\right)\right] = \frac{sL_d}{1+s^2C_TL_d}. \quad (56)$$

And the L-section method is used for cancel the imaginary part of the output impedance over the entire operation band.

4.1.4 Darlington pair

The schematic is shown in Fig. 4-9. By proper choosing size of the transistor, the overall trans-conductance is

$$G_m = \frac{g_{m4}}{\left(1+\frac{1}{g_{m3}R_{bias}}\right)} \approx 0.9g_{m4}, \quad (57)$$

and the overall parasitic capacitance is

$$\frac{C_{gs3}\bullet C_{gs4}}{C_{gs3}+C_{gs4}} + C_{gd3} + C_{gd4} \approx 0.5\left(C_{gs4}+C_{gd4}\right), \quad (58)$$

so the f_{TD} would

$$f_{TD} = \frac{G_m}{2\pi\left(\frac{C_{gs3}\bullet C_{gs4}}{C_{gs_3}+C_{gs4}} + C_{gd3} + C_{gd4}\right)} \approx \frac{0.9g_{m4}}{0.5\left(C_{gs4}+C_{gd4}\right)} \approx 1.8\, f_{TS}. \quad (59)$$

Then, the overall cut-frequency would approximately twice with single transistor at same power consumption level. With f_T doubling circuits it is often possible to obtain 80% increase in bandwidth, although the exact improvement depends on numerous and variable factors. The simulation result is shown in figure 4-10. From simulation result we can observe that the f_T is similar, but the gain of the Darlington pair in the desired frequency band is higher than single transistor's gain.

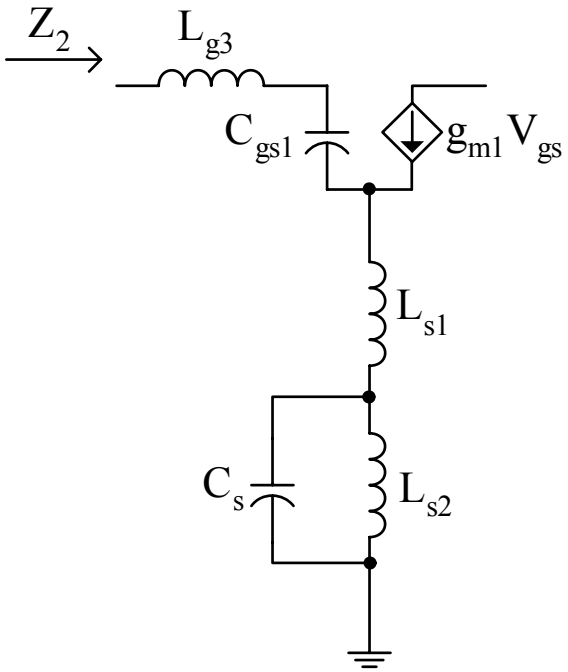


Fig. 4-4. The equivalent circuit of the Z_2 input impedance.

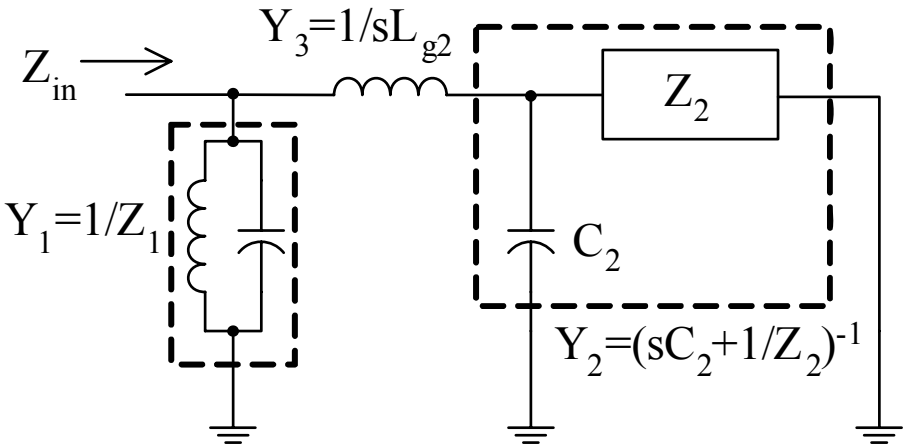


Fig. 4-5. The equivalent circuit of the Z_{in} input impedance.

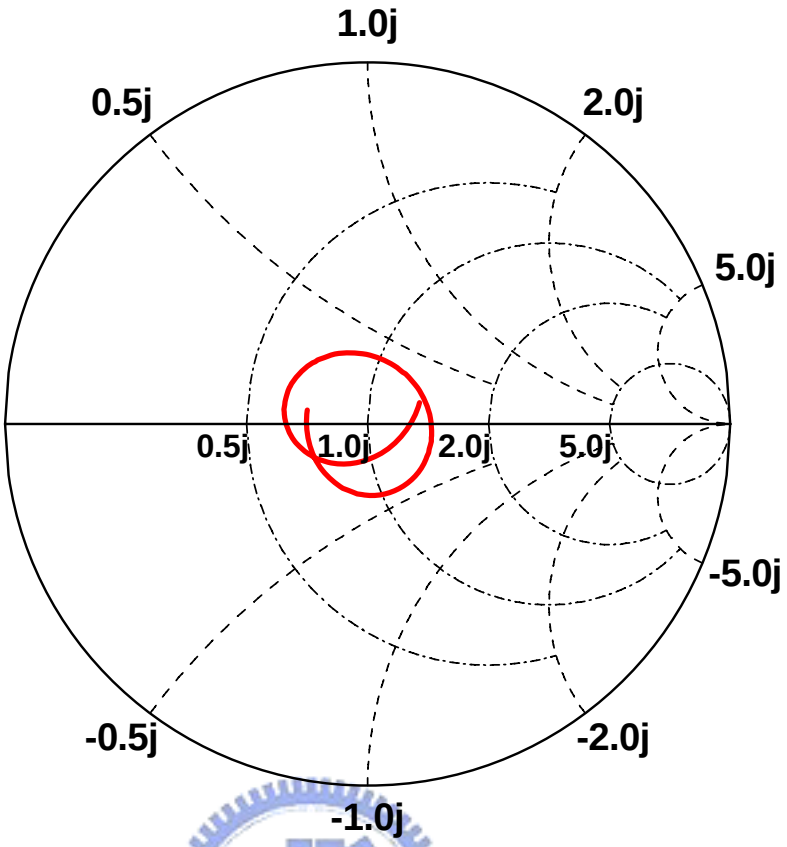


Fig. 4-6. The simulated S_{11} of the proposed LNA.

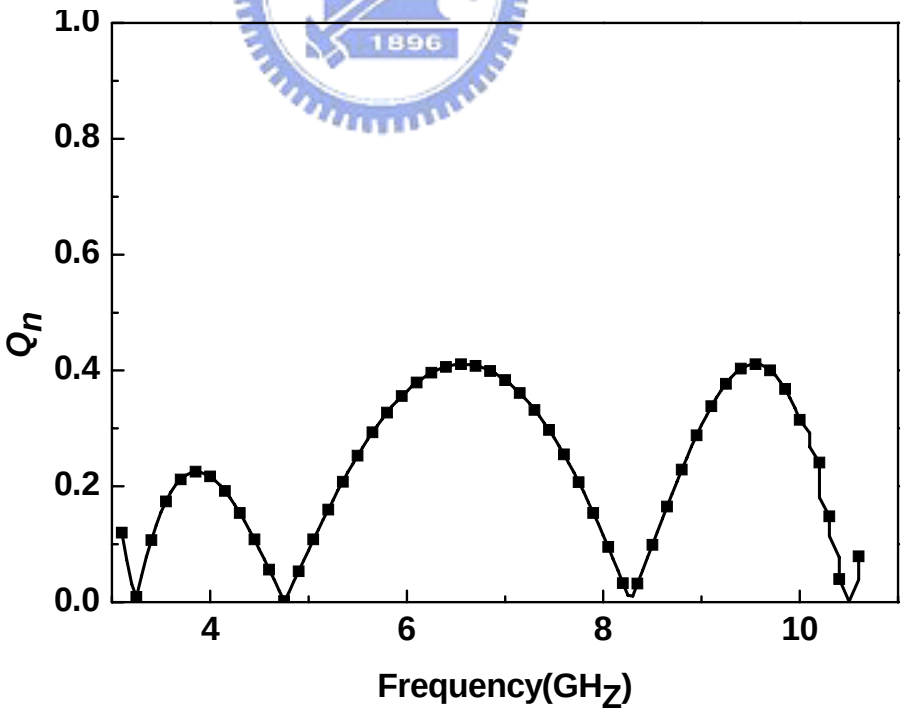


Fig. 4-7. The Q_n of the proposed LNA.

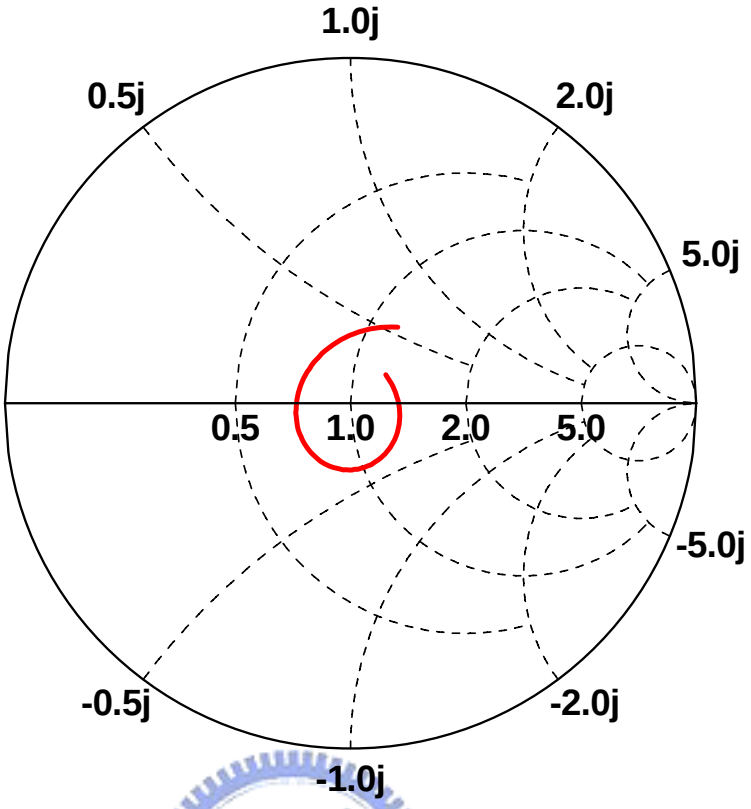


Fig. 4-8. The simulated S_{22} of the proposed LNA.

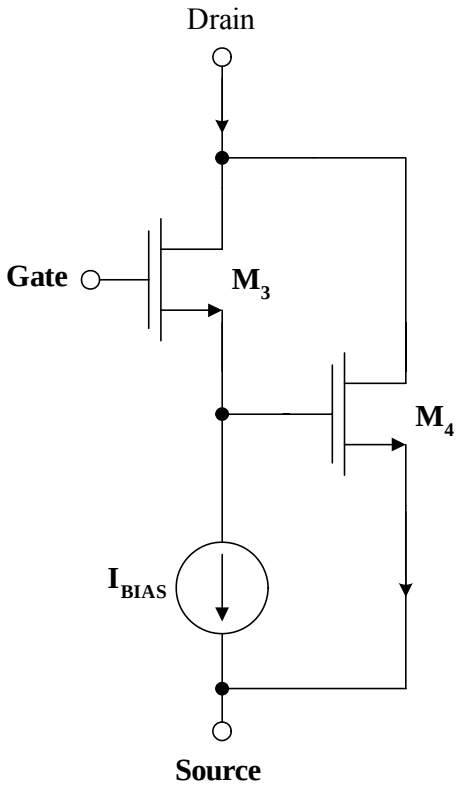


Fig. 4-9. The Darlington pair schematic.

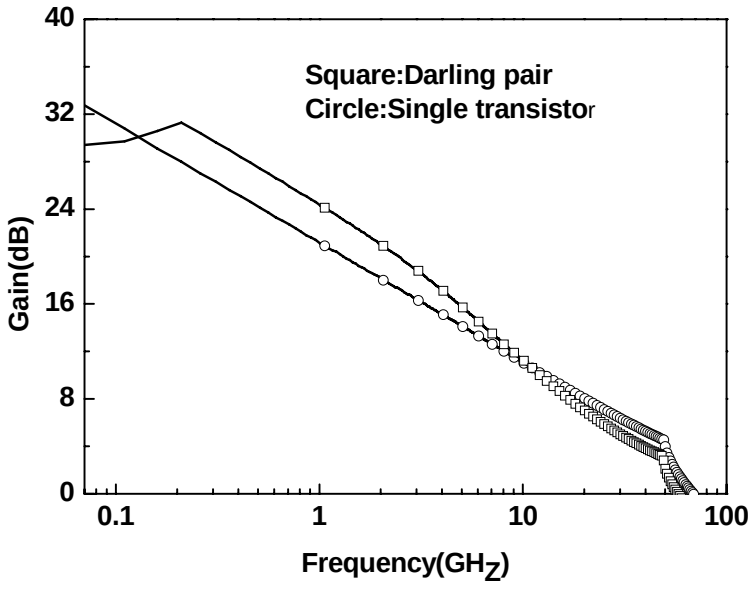


Fig.4-10. The simulation result of the Darlington pair compared with single transistor.

4.1.5 Shunt peaking

A model of shunt peaking amplifier is shown in Fig. 4-11. The capacitance *C* may be taken to represent all the loading on the output node, including that of a subsequent stage. The resistance *R* is the effective load resistance at that node and the inductor provides the bandwidth enhancement. It's clear from the model that the transfer function v_{out}/i_{in} is just the impedance of the *RLC* network, so it should be straightforward to analyze. The addition of an inductance in series with the load resistor provides an impedance component that increases with frequency, which helps offset the decreasing impedance of the capacitance, leaving net impedance that remains roughly constant over a broader frequency range than that of the original *RC* network. The impedance of the *RLC* network may be written as

$$Z(s) = (sL + R) // \frac{1}{sC}. \tag{60}$$

In addition to a zero, there are two poles. We introduce a factor *m*, defined as the ratio of the *RC* and *L/R* time constant:

$$m = \frac{RC}{L/R} \tag{61}$$

Then, the transfer function becomes

$$Z(s) = \frac{R[s(L/R)]+1}{s^2LC + sRC + 1} = \frac{R(\tau s + 1)}{s^2\tau^2 m + s\tau m + 1}, \tag{62}$$

where $\tau = L/R$.

The magnitude of the impedance, normalized to the DC value as a function of frequency, is then

$$\frac{|Z(j\omega)|}{R} = \sqrt{\frac{(\omega\tau)^2 + 1}{(1-\omega^2\tau^2 m)^2 + (\omega\tau m)^2}}, \tag{63}$$

so that

$$\frac{\omega}{\omega_1} = \sqrt{\sqrt{(-\frac{m^2}{2}+m+1)^2+m^2}+(-\frac{m^2}{2}+m+1)}\,, \tag{64}$$

where ω_1 is the uncompensated -3dB frequency. If chose $m=\sqrt{2}\approx 1.414$, then can extend the bandwidth to a value about 1.85 times as large as the uncompensated bandwidth. However, this choice of m leads to nearly a 20% peak in the frequency response, a value often considered undesirably high. If chose $m=1+\sqrt{2}\approx 2.414$, then can lead to a bandwidth that is about 1.72 times as large as the un-peaked case. Hence, at least for the shunt-peaked amplifier, both a maximally flat response and a substantial bandwidth extension can be obtained simultaneously. In my design, the m is about 2.31, then $\omega \approx 1.743\omega_1$.

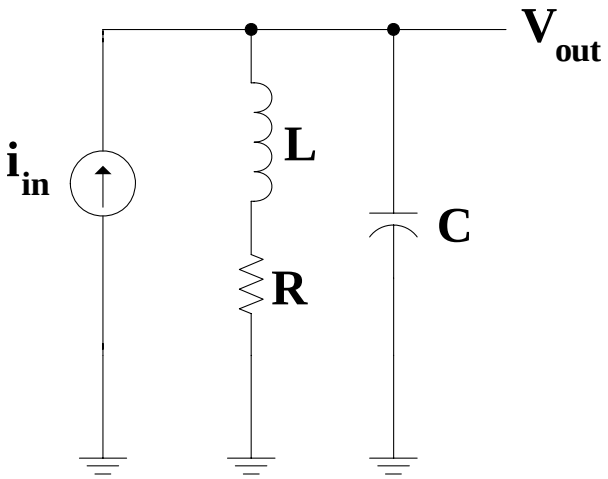


Fig. 4-11. The model of shunt peaking amplifier.

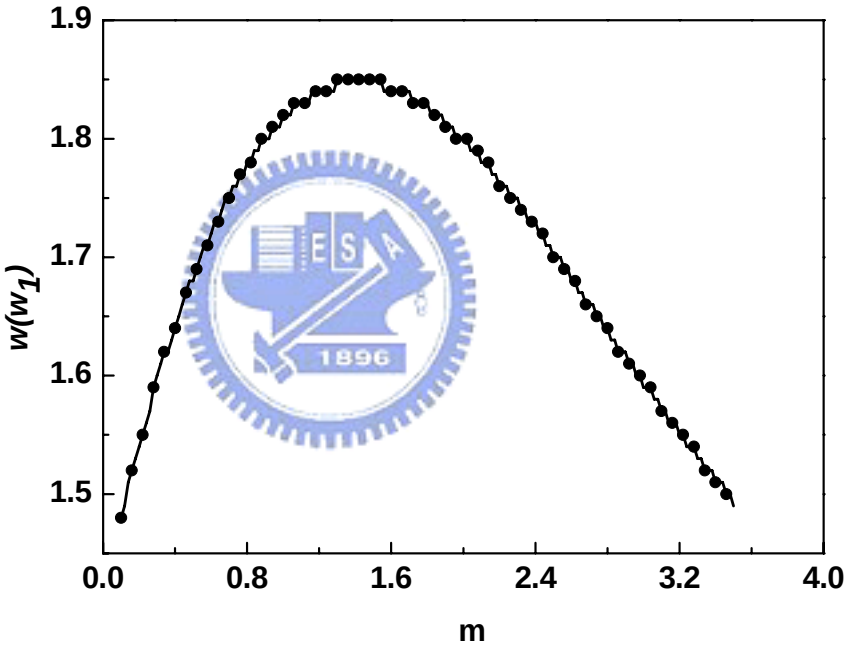


Fig. 4-12. The relationship of the value of m and ω_1.

4.2 Layout and Other Consideration

4.2.1 Layout consideration

Figure 4-13 is the layout diagram. The measurement instruments have the parasitic loading effect. To avoid the effect we must parallel the bypass capacitor with the bias pad to ground. The parallel bypass capacitor can provide a short path to ground at high frequency. The parallel bypass capacitor requires essential capacitance so that make a result of ground at high frequency.

The discontinuities introduce parasitic capacitance or inductance that can lead to phase and amplitude errors, input and output mismatch, and possibly spurious coupling. One approach for eliminating such effects is to construct an equivalent circuit for the discontinuity, including it in the design of the circuit, and compensating for its effect by adjusting other circuit parameters. Another approach is to minimize the effect of a discontinuity by compensating the discontinuity directly, often by chamfering of mitering the conductor. The right-angle bend can e compensated by mitering the cornet, which has the effect of reducing the excess capacitance at the bend. The technique of mitering can also be used to compensate step and T-junction discontinuities.

4.2.2 Inductors implementation

This design is fabricated by TSMC CMOS 0.18 μ m process. Because that this process there is not providing inductor model beyond 6 GH_Z. In this design, inductors are essential components. Then, I use EM simulator to generate inductor model and size parameters. But CMOS process is silicon based substrate, the coupling effect is critical. And the EM simulator is not accurate enough for estimating coupling loss effect. In reference [12], it provides more accurate equation to estimate inductance and quality factor by physical size. So we can use equation and EM simulator to design inductors simultaneously. The size parameters of the inductor has four parameters, i.e. turns of

number, space between two metal lines, width of the metal line and inner radius. When we get the inductors' S-parameters, then use equivalent circuit model to obtain the components parameters. Use the obtained components parameters to place into the low noise amplifier circuit. Therefore we can get the result of post-simulation with inductors. Considering the cross coupling effect between two inductors and other components, must place inductor a distance from other components. The inductor equivalent circuit model is shown in figure 4-14.

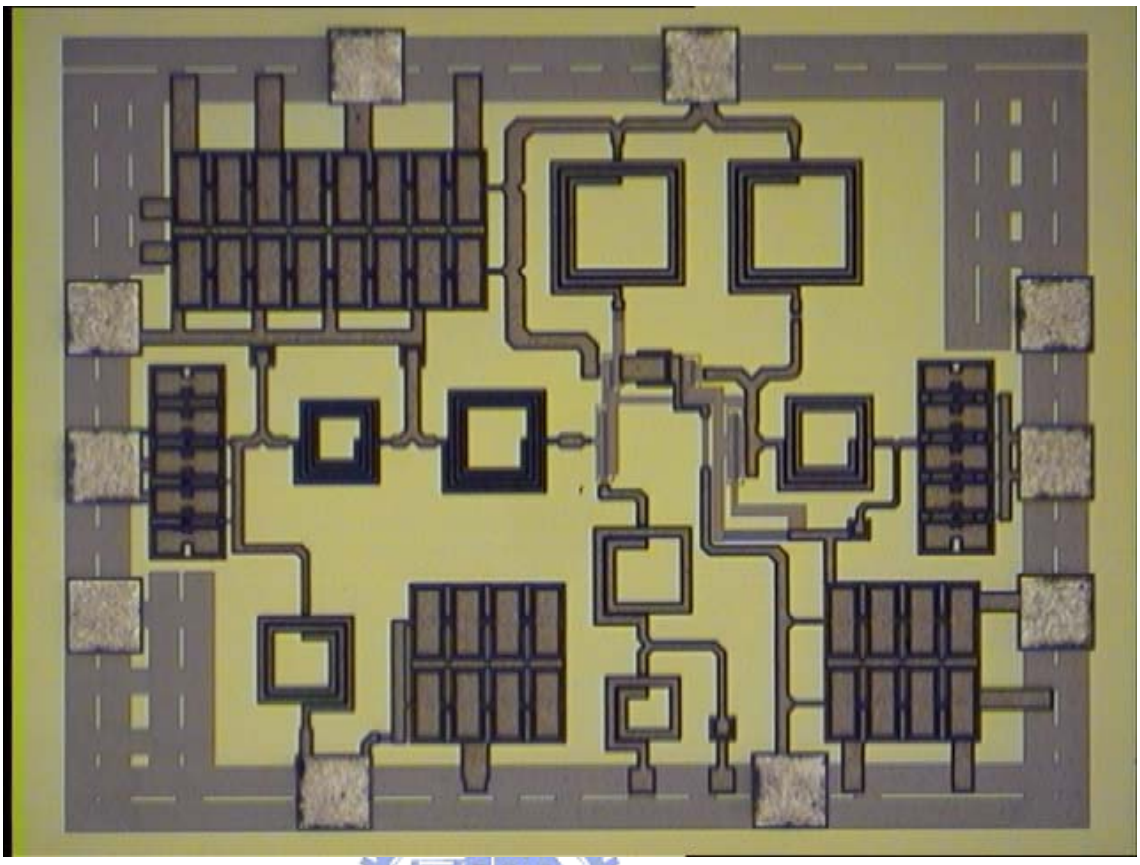


Fig. 4-13. The die diagram of the proposed low noise amplifier.

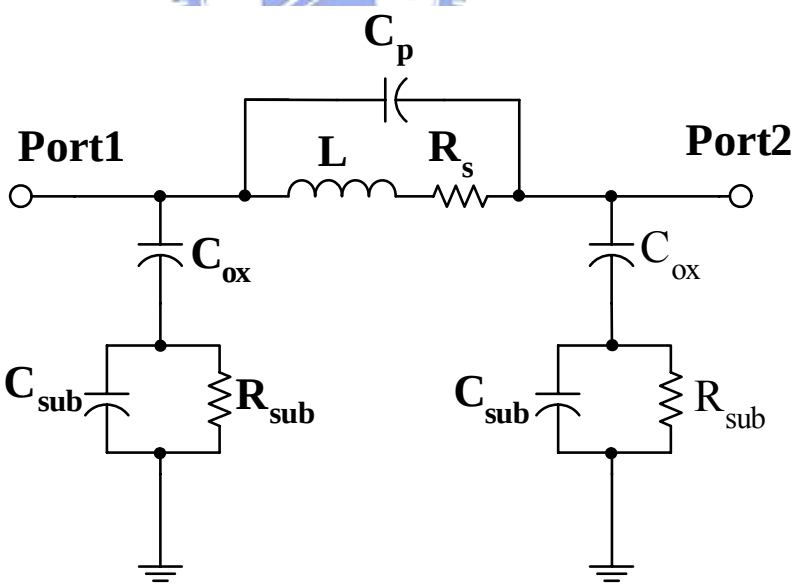
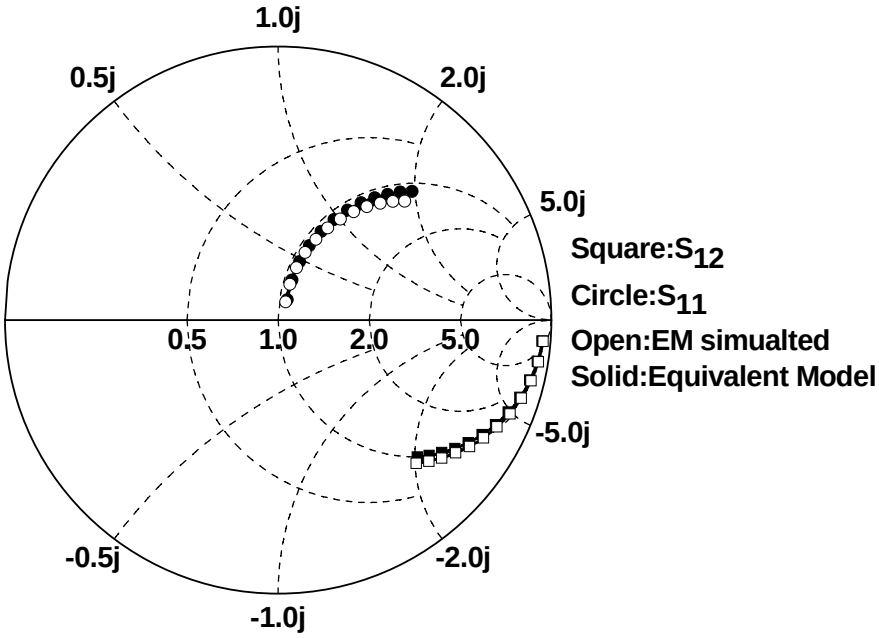
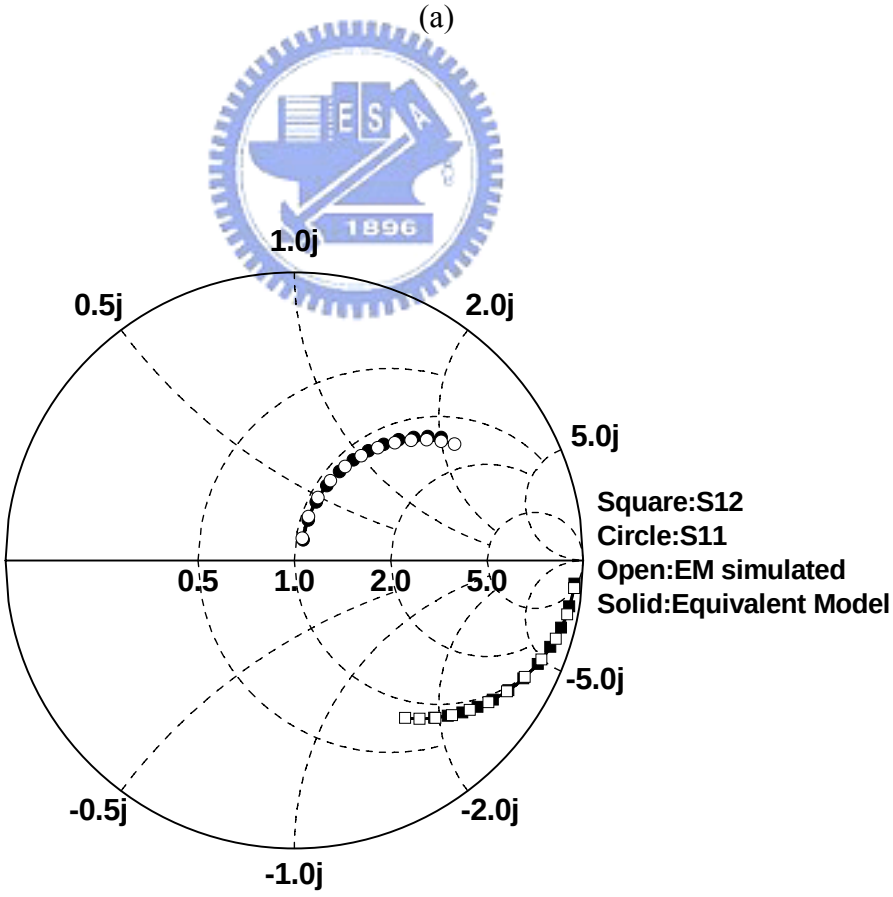


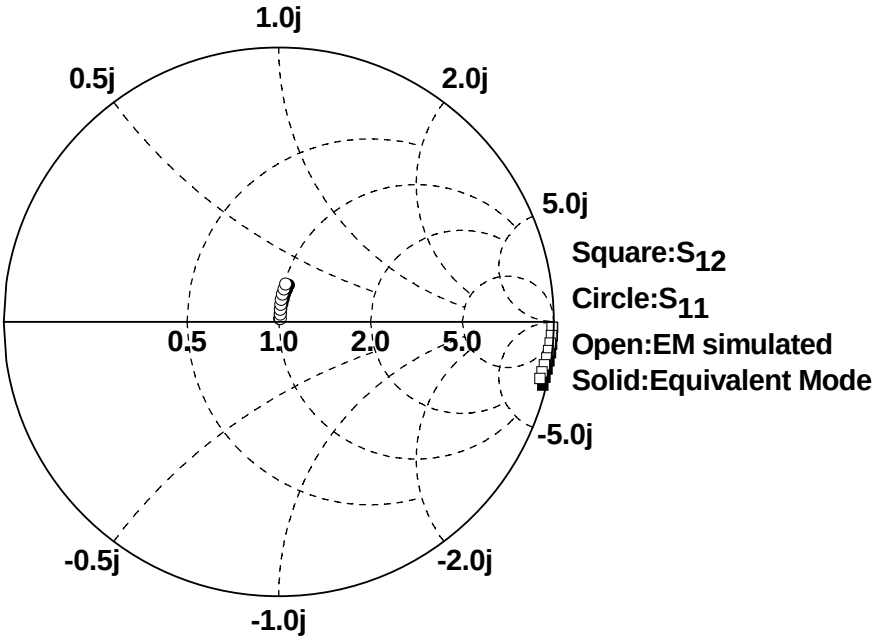
Fig. 4-14. The equivalent circuit model of the inductor.


1.0j
0.5j
2.0j
5.0j
Square:S12
Circle:S11
0.5
1.0
2.0
5.0
Open:EM simualted
Solid:Equivalent Model
-5.0j
-0.5j
-2.0j
-1.0j

(a)


1.0j
0.5j
2.0j
5.0j
Square:S12
Circle:S11
0.5
1.0
2.0
5.0
Open:EM simulated
Solid:Equivalent Model
-5.0j
-0.5j
-2.0j
-1.0j

(b)



(c)

Fig. 4-15. (a) L_{g3} EM simulation v.s. Equivalent model. (b) L_d EM simulation v.s. Equivalent model. (c) L_{s1} EM simulation v.s. Equivalent model.

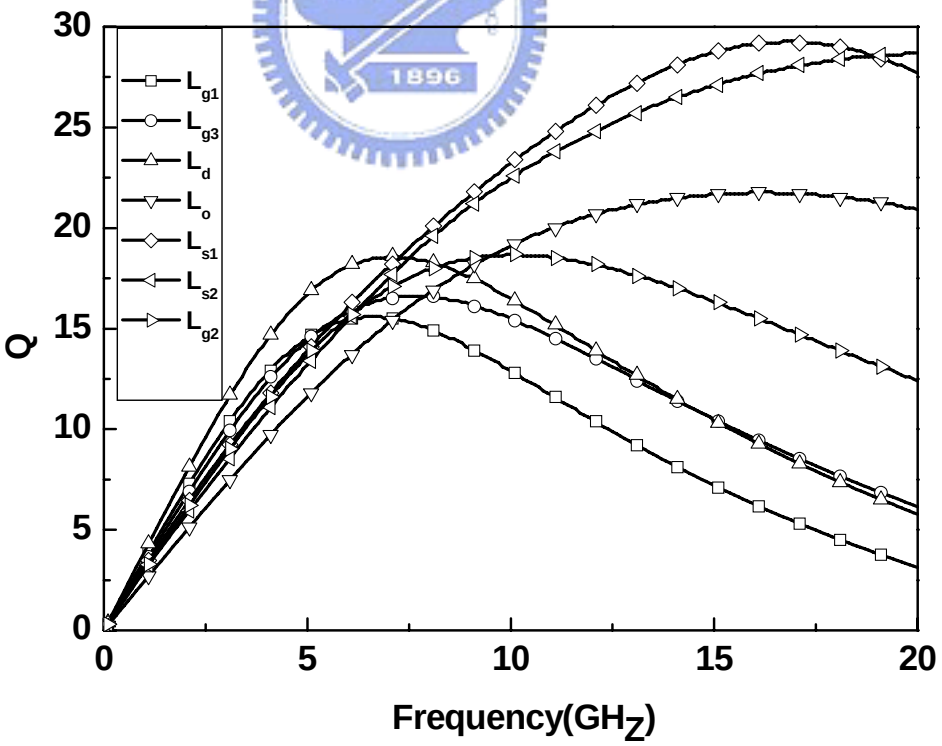


Fig. 4-16. The quality factor of the inductors in the low noise amplifier.

Chapter 5

Experimental Result and Discussion

5.1 Experimental Result

Figure 5-1 is simulated forward gain and reverse isolation respectively. The average forward gain is about 7dB and the reverse isolation is below -35dB at high frequency band. And the forward gain is flat in entire operation frequency band.

Figure 5-2 is simulated S_{11} and S_{22} of the low noise amplifier. The average magnitude of the S_{11} is about -12dB and S_{22} is about -7dB in entire operation frequency band, respectively.

Figure 5-3 is simulated noise figure of the low noise amplifier. The average noise figure is about 8dB in entire operation frequency band.

The total power consumption is about 22mW with a power supply of 1.8 volts. And the die area including the pads is 1 mm^2.

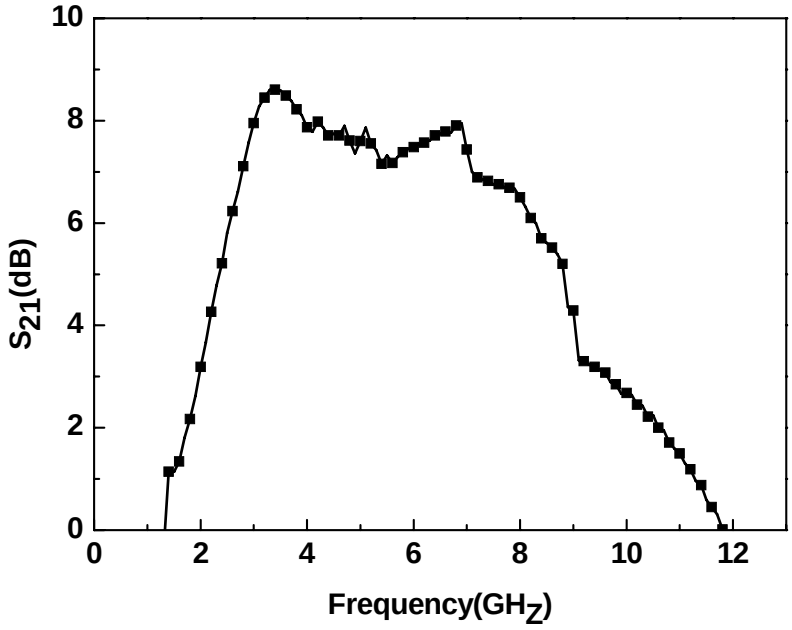
5.2 Discussion and Conclusion

From result of the figure 5-1 (b), we can observe that when the operation frequency is increasing, the magnitude of the S_{12} is increasing. Because the gate-drain capacitors (C_{gd}) provide a feedback path from drain end of MOSFET to gate end of MOSFET at high frequency. And since the silicon substrate coupling effect, the conductive silicon substrate provides a conductive path. The result of flat gain is caused by shunt peaking. The bandwidth is very extensive due to using Darlington pair as output stage.

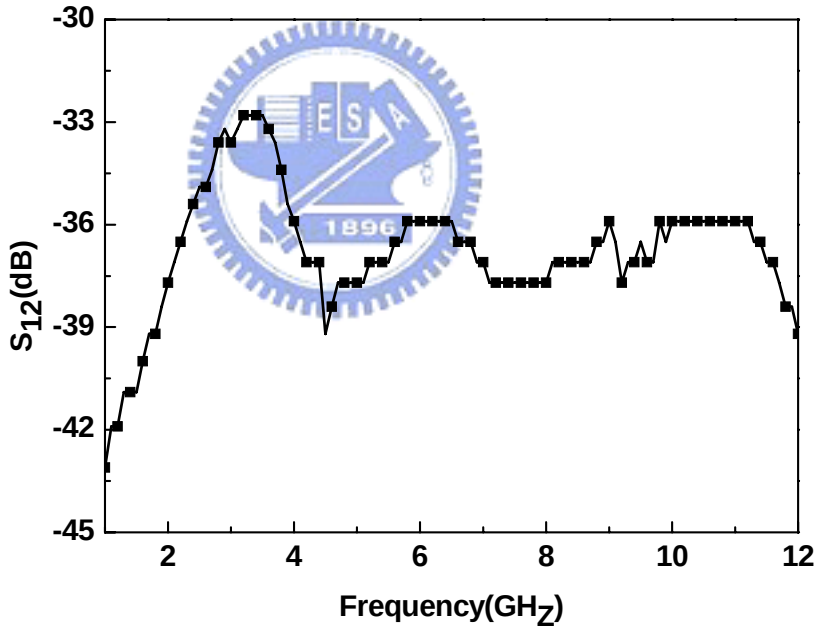
The magnitude of input reflection coefficient S_{11} is below -7dB. There are two resonance points at 3.5 GH_Z, and 8.5 GH_Z, respectively. The magnitude of output reflection coefficient S_{22} is below -7dB. Because the reactance of the output stage is smaller than input stage, the output stage can introduce little components to reach matching. At low frequency, the reactance isn't effective, and the resistance is

dominant.

The noise figure of the low noise amplifier is about 8dB. Because that input matching network introduce much passive components to reach matching. The passive component between input source and MOSFET gate end can cause noise degrade. The figure 4-3 shows the situation. But for the purpose of input matching, we need considerable passive components to form matching network. And the inductor is introduced greatly in my design. Because of the silicon substrate loss may cause noise coupling through large size inductors.

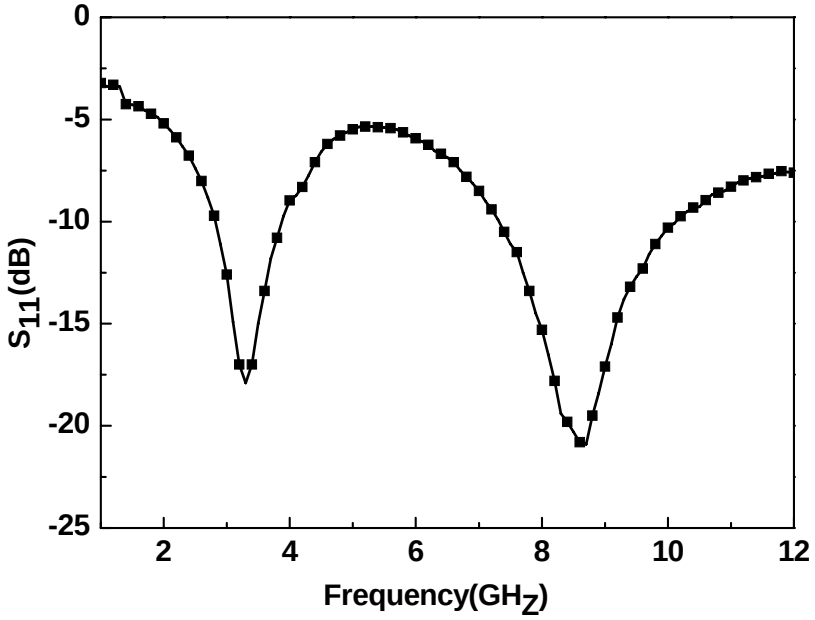


(a)

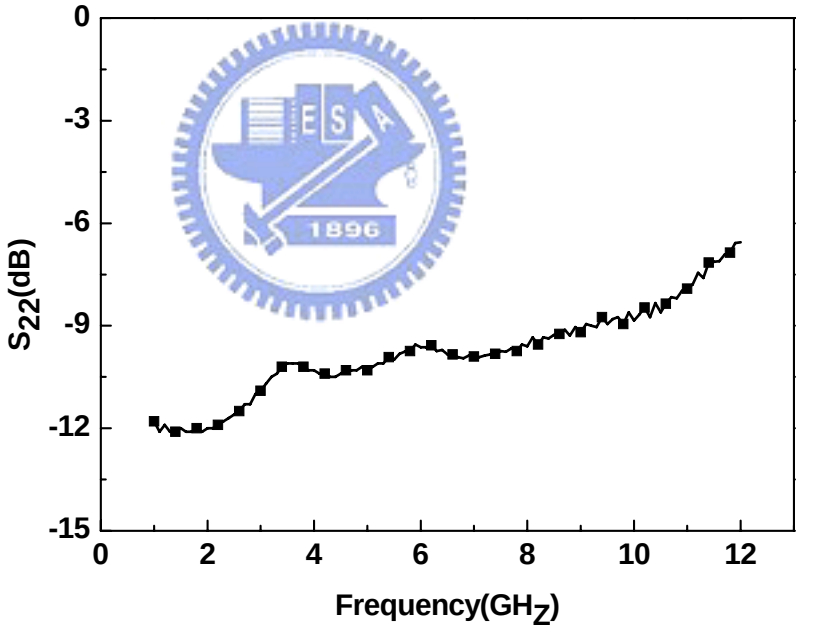


(b)

Fig. 5-1. (a) The measured forward gain of the low noise amplifier. (b) The measured reverse isolation of the low noise amplifier.



(a)



(b)

Fig. 5-2. (a) The measured magnitude of S_{11} of the low noise amplifier. (b) The measured magnitude of S_{22} of the low noise amplifier.

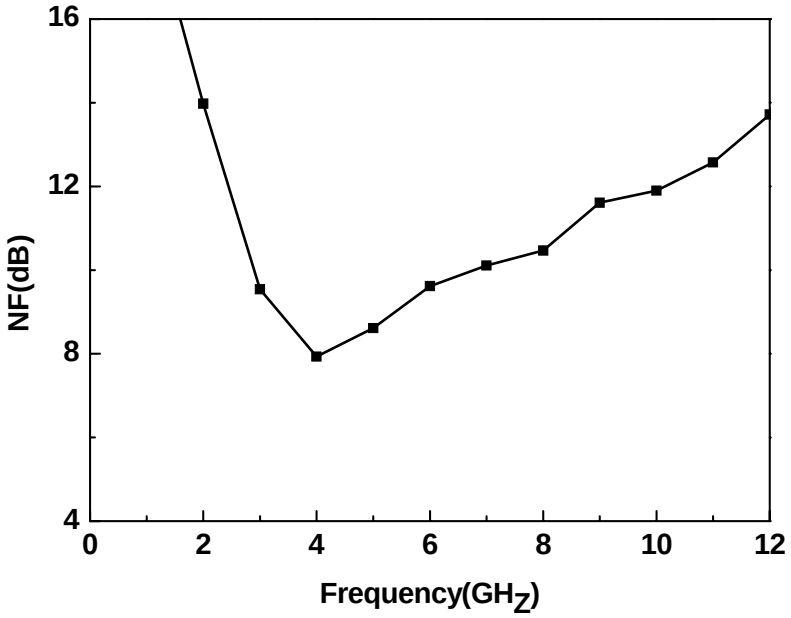


Fig. 5-3. The measured noise figure.

References

[1] P. Heydari, "Design Considerations for Low-Power Ultra Wideband Receivers," *IEEE* Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on 21-23 March 2005 Page(s):668 - 673

[2] B. Razavi, *RF Microelectronics*, 1st ed. NJ, USA: Prentice-Hall PTR, 1998.

[3] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 1st ed. New York: Cambridge Univ. Press, 1998.

[4] B. Razavi, *Design of Analog CMOS Integrated Circuits*, International ed. NY: McGraw Hill Co. 2001.

[5] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*, 2nd ed. NJ: Prentice-Hall, Inc. 1997.

[6] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp; 745-759, May, 1997.

[7] S. Vishwakarma, S. Jung and Y. Joo, "Ultra Wideband CMOS Low Noise Amplifier with Active Input Matching," *IEEE Ultra Wideband Systems*, 2004. Joint with Conference on Ultrawideband Systems and Technologies. Joint UWBST & IWUWBS. 2004 International Workshop on 18-21 May 2004, pp. 415-419.

[8] C-W. Kim, M-S. Kang, P. T. Anh, H-T. Kim and S-G. Lee, "An Ultra-Wideband CMOS Low Noise Amplifier for 3-5-GHz UWB System," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, February, 2005.

[9] R-C. Liu, K-L. Deng, and H. Wang, "A 0.6-22-GHZ broadband CMOS distributed amplifier," in *IEEE Radio Frequency Integrated Circuits Symp. Dig. Papaers*, 2003, pp. 103-106

[10] D. M. Pozar, *Microwave Engineering*, 2nd ed. Crawfordsville: John Wiley & Sons, Inc. 1998.

[11] P. R. Gary, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of*

Analog Integrated Circuits, 4th ed. Crawfordsville: John Wiley & Sons, Inc. 2001.

[12] C. P. Yue, C. Ryu, J. Lau, T. H. Lee, and S. S. Wong, "A physical model for planar spiral inductors on silicon," *IEEE, Electron Devices Meeting,* 1996. International 8-11 Dec. 1996 pp. 155-158.

[13] A. Bevilacqua, and A. M. Niknejad, "An Ultrawideband CMOS Low-Noise Amplifier for 3.1-10.6-GH_Z Wireless Receivers," *IEEE J. Solid-State Circuits*, vol.39, no. 12. December 2004.

[14] J. N. Burghartz, D. C. Edelstein, H. A. Ainspan, and K. A. Jenkins, "RF Circuit Design Aspects of Spiral Inductors on Silicon," *IEEE J. Solid-State Circuits*, vol.33, no. 12. December 1998.

[15] H. Dedieu, C. Dehollain, J. Neirynck, and G. Rhodes, "A New Method for Solving Broadband Matching Problems," *IEEE Tran. Circuits and Systems*, vol. 41, no. 9. September 1994.

[16] H. J. Carlin, and P. Amstutz, "On Optimum Broad-Band Matching," *IEEE Tran. Circuits and Systems*, vol. 28, no. 8. May 1981.

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(92 年 9 月入學)

論文題目：

1.8 伏金氧半低雜訊放大器應用於超寬頻 3.1-10.6GHz 無線接收端

(A 1.8 -V CMOS LNA applied for Ultra-Wideband 3.1 to 10.6GHz Wireless Receivers)