應用於 CMOS 電路測試之內建熱加速自我測試電路

研究生:劉 坪　　　　　　指導教授:李崇仁　博士

國立交通大學

電子工程學系　電子研究所碩士班

摘　要

本論文提出及研究一個內建熱加速自我測試電路的方法，目的在於當 SOC 測試時找出早期錯誤率。因此，在晶片內自動產生一組輸入樣式可以使功率消耗最大用以測試待測電路，而不需經由傳統的高溫爐測試。本論文首先研究組合電路的測試產生方法並應用此結果於序向電路。

此外，我們推導出用於 PLA 電路的輸入樣式用以產生最大的切換個數，換言之，產生最大的功率消耗。再則，提出一個 DRAM 及 SRAM 的改良設計方法使它們可以輕易的被用於內建熱加速自我測試的方法。此方法用於一些 ISCAS 標準電路產生的實驗結果顯示，經由方法產生的輸入樣式可以有效的增加代測電路的功率消耗。此外，提出一個用於 SOC 的內建自我測試電路的架構。

BIST Burn-in Methodology for the CMOS Circuit

Student:Ping Liu Adviser:Prof. Chung Len Lee

Department of Electronics Engineering

& Institute of Electronics

National Chiao Tung University

Abstract

This thesis proposes and studies a BIST burn-in methodology which is aimed to finding early failure in CMOS SOC testing. It is to, on-chip, apply a set of patterns which maximizes the power dissipation to burn-in test the CUT without resorting to the conventional burn-in furnace testing. The thesis first studies the test generation for the combinational circuit and then apply the result to the sequential circuit. Also, we derive the patterns for the PLA type of circuits to achieve the maximal switching, i.e., the maximal power consumption. Moreover, we propose a modified design for

DRAM and SRAM to let them easily be easily applied BIST burn-in testing methodology. Experimental results of applying this approach to some ISCAS benchmark circuits have shown that the patterns generated by this method significantly increase the power dissipation for the circuit to be tested. Furthermore, an architecture for applying the BIST scheme to the SOC is also proposed.