Contents

Chinese ab	ostrac	2t	Ι
English ab	strac	t	Π
Acknowled	gmer	nts	IV
Contents	•••••		v
List of Figu	ıre		VII
List of Tab	les		IX
Chapter 1	Int	roduction	1
	1.1	Reliability and Rurn-in Testing	1
	1.2	Power Consumption of CMOS Circuits	4
		1.2.1 Dynamic capacitive switching power	5
		1.2.2 Short circuit power	6
		1.2.3 Leakage power	7
	1.3	Proposed BIST Burn-in Test Methodology	8
	1.4	Review of Related Research	9
	1.5	Outline of Dissertation	10
Chapter 2	Test	t Generation for Combinational Circuit	11
	2.1	General Description of the Test Generation for Combinational	
		Circuit	11
	2.2	The method of Expansion Rely on Event-driven	13
		2.2.1 Event-driven Simulation	13
		2.2.2 The Method of Expansion for Modified Modified	
		Circuit	14

2.3	The Principle and Flow	v of ATPG	23
-----	------------------------	-----------	----

2.3.1 The Principle of ATPG for Maximum Transitions23				
2.3.2 ATPG for Maximum Cyclic Average Transitions24				
Chapter 3 Test Generation for Sequential, PLA and Memory Cicuirt26				
3.1 Test Generation for Sequential Circuit				
3.2 Test Generation for PLA type of circuit				
3.3 Test Generation for Memory type of circuit				
Chapter 4 Simulation Result				
4.1 Maximum Transitions32				
4.2 Maximum Cyclic Average Transitions				
4.3 Simulation on Power Consumption under Applied Cyclic Patterns				
4.4 Power Consumption versus Frequency of Applied Pattern35				
Chapter 5 Built-in Self Test Circuit in CMOS Circuit				
Chapter 6 Conclusion				
References				

List of Figures

Figure 1.1	Dynamic transition current
Figure 1.2	Short circuit current7
Figure 1.3	Leakage current7
Figure 1.4	The proposed BIST bun-in test methodology8
Figure 2.1	The flowchart of the test generation12
Figure 2.2	Example to illustrate the method of expansion14
Figure 2.3	The signal passes on the path and what new value is generated14
Figure 2.4	The waveform of each gate16
Figure 2.5	The whole possibility that what time will each gate produce a
	transition
Figure 2.6	The whole XOR gates will be used in this circuit
Figure 2.7	The list of every gate that will probably generate new value
Figure 2.8	The semi-finished circuit19
Figure 2.9	The complete circuit under variable delay20
Figure 2.10	The list of every gate that will probably generate new value under zero
	delay model21
Figure 2.11	The complete circuit under zero delay21
Figure 2.12	The list of every gate that will probably generate new value under unit
	delay model22
Figure 2.13	The complete circuit under unit delay22

Figure 2.14	The sketch map of searching for generating the cyclic input pattern24
Figure 3.1	The fundamental structure of sequential circuit27
Figure 3.2	The modified combinational circuit under test27
Figure 3.3	The PLA circuit which is under test t
Figure 3.4	The general framework sketch of DRAM29
Figure 3.5	The method for testing the DRAM
Figure 3.6	The method for testing the SRAM
Figure 4.1	The plots of number of gates of switchings for the set of burn-in patterns
	and the normal case patterns for C354034
Figure 4.2	The power consumption of C1908
Figure 4.3	The waveform of power versus frequency in burn-in
	and normal situation
Figure 5.1	The BIST signal generator for the cyclic burn-in patterns
Figure 5.2	The BIST circuit applied to burn-in test a combinational circuit
Figure 5.3	The BIST circuit applied to burn-in test a sequential circuit

List of Tables

Table 1.1	Technology Roadmap of Semiconductor Manufacture2
Table 2.1	The form of scheduled event and avtivity at each time15
Table 3.1	The simulation results of power consumption under normal and burn-in
	for the DRAM and SRAM
Table 4.1	Simulation results of the switchings for the generated input patterns for
	benchmark circuits
Table 4.2	Simulation result of the maximum cyclic input pattern set

