

References

- [1] *The National Technology Roadmap for Semiconductors*, Semiconductor Industry Association, 2004 Edition.
- [2] D.J Klinger, Y. Nakada and M. A. Meenedez, *AT&T Reliability Manual*, New York, AT&T, 1990.
- [3] Chuan-Yu Wang, Tan-Li Chou, “Maximum power estimation for CMOS circuit under arbitrary delay model.” *IEEE International Symposium*, vol.4,pp.763-766,May 1996.
- [4] S.Devadas, K. Keutzer, and j. White, “Estimation of power dissipation in CMOS combinational circuits using Boolean function manipulation, ” *IEEE Trans. on Computer-Aided Design*, vol. 11, pp.372-383, March 1992.
- [5] Chuan-Yu Wang and Kaushik Roy, “Maximum power estimation for CMOS circuits using deterministic and statistical approaches,” *in Proceedings of the VLSI Conference*, 1996.
- [6] Chin-Chi Teng, Anthony M.Hill, and sung Mo Kang. “Estimation of maximum transition counts at internal nodes in CMOS VLSI Circuits,” *in Proceedings of the ICCAD*, pages 366-370, November 1995.
- [7] Tohru Furuyama, “Wafer Burn-in Technology for RAM’s,” *in IEDM*,1993.
- [8] K.C. Huang, C.L.Lee and J.E.Chen, “Maximization of power dissipation under random exitation for burn-in testing, ” *in Proceedings of International Test Conference*, October, 1998.

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