國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

以閘極感應與通道感應方法與脈衝電流電壓技術

分析SONOS類型元件中捕捉電荷之特性

Trapped Charge Characterization of SONOS-type Devices Using a Novel Gate-Sensing and Channel-Sensing (GSCS) Method and Pulse-IV Technique

研 究 生 ：杜姵瑩

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摘要

本篇論文主要致力於，利用許多新穎的技術廣泛地研究 SONOS 類型元件之電荷捕捉特性，以求對於 SONOS 類型元件的物理特性有更深入地了解。由於 SONOS 類型元件擁有絕佳的微縮能力及少數電子儲存性等優勢，使它被認為會是在未來微縮時代中，最可能取代快閃(Flash)記憶體的其中一者。縱使如此，人們對於 SONOS 類型元件中，氮化層捕捉電荷行為的了解，仍然是非常有限的。在本篇論文裡，我們首先提出一個新穎的閘極感應與通道感應(gate-sensing and channel-sensing, GSCS)方法。除了傳統通道感應型(CS)電容，我們又多加了另一個閘極感應型(GS)電容。利用這兩種不同感應型態的電容，我們可以得到兩個方程式。而這兩個方程式正好可以讓我們解兩個變數。一個是總電荷密度(Q)，另一個則是電荷的平均垂直位置(x)。這個方法有幾個相當大的優勢，它不需要複雜的儀器設備，也不需要在比較不同樣品時做一些人工的參數調整，以求符合實驗的數據。因此，我們可以說是提出了一個相當簡單且有力的方法，來研究捕捉電荷的特性。透過這方法，我們可以偵測在”真實時間”內捕捉電荷的位置、寫入抹除時氮化層內部電荷傳輸的行為以及各種可靠度的分析。我們也驗証了被捕捉的電子主要是分佈在整個氮化層裡而非在氧化層與氮化層之間的界面。此外，在本篇論文裡，我們也詳盡地描述各種堆疊氮化層的捕獲效率、氮化層內部的電荷傳輸以及各種可靠度問題。基

於GSCS方法，我們也提出了一個系統化的方法來區別SONOS類型元件的抹除機制（是來自於外部電洞的注入或是被捕捉的電子從氮化層逃脫出來）。

除了 GSCS 方法之外，我們也為記憶體未來應用性及其快速缺陷特性化發展出一種新的脈搏電壓電流(Pulse-IV)技術。Pulse-IV 技術最近已經被廣泛地應用在 CMOS 邏輯元件，研究其高介電常數閘極介電層中陷阱的特性。在本篇論文裡，我們進一步改進舊有的 Pulse-IV 技術，使它能夠應用在記憶體的相關研究上。我們研究了 SONOS 電容的瞬間暫態穿隧電流，並且發現穿隧電流的暫態變化是與元件的電荷捕捉行為及其堆疊結構有關。然而，這個 Pulse-IV 技術最值得注意的應用，是在於研究 SONOS 電晶體的超快速穿隧注入。我們的 Pulse-IV 技術可以準確且即刻地描述電晶體在寫入抹除後的行為，而沒有任何讀取干擾問題。我們可以準確地提供在微秒等級內元件的特性。而這個新技術也替研究類似非揮發性記憶體的應用開闢了一條嶄新的道路。

Trapped Charge Characterization of SONOS-type Devices using a Novel Gate-Sensing and Channel-Sensing (GSCS) Method and Pulse-IV Technique

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ABSTRACT

This dissertation is devoted to study the charge trapping characteristics of SONOS-type devices extensively by several new techniques and provide in-depth physical understanding. Although SONOS-type devices are forecasted to be the promising solutions to continue the Flash memory scaling due to their excellent scalability and few-electron storage capability, the fundamental understanding of the nitride-trapping behaviors is still very limited. In this dissertation, we first proposed a novel gate-sensing and channel-sensing (GSCS) method, where an additional GS capacitor is used to compare with the conventional CS one. Sensing in both modes provides two equations that are suitable to solve for two variables — the total trapped charge density (Q) and the average charge vertical location (x). This method does not need complex equipment or artificial fitting in comparing different samples, thus provides a very simple and powerful method to characterize trapped charge. Through this method we could monitor in “real-time” the trapped charge location and intra-nitride behaviors during programming/erasing as well as retention reliability test. We also clarified that the electrons are mainly distributed inside the bulk nitride instead of the interfaces between oxide and

nitride. Furthermore, the capture efficiency of various stacked nitride-trapping layers, intra-nitride transport, and reliability issues were investigated in detail.

Based on GSCS method, we also provided a systematic method to distinguish the erase mechanisms by hole injection from that by electron de-trapping for SONOS-type devices.

In addition to GSCS method, we also developed a new Pulse-IV technique for memory applications and fast trap characterizations. Pulse-IV techniques have been developed recently to characterize traps in high-*k* gate dielectrics of CMOS logic devices. In our work we have improved this technique to apply in memory characterizations. The transient tunneling currents of various SONOS-type capacitors have been studied in detail, and we found that the tunneling current relaxation is well correlated to charge trapping and memory structures. Moreover, the power of this pulse-IV is fully demonstrated when studying SONOS-type transistors with very fast tunneling injection. Our pulse-IV technique can accurately characterize the transistors immediately after programming/erasing without read disturbance and provide accurate device characterizations within microsecond (μs). This new characterization method also opens a new path to study quasi-non-volatile memory applications.

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CHAPTER ONE

INTRODUCTION

OUTLINE

1.1 Non-volatile Memory Review

Generally speaking, semiconductor memory can be split into two main categories: volatile and non-volatile, as illustrated in Fig. 1.1. Volatile memory loses its data as soon as the power is turned off while non-volatile memory does not lose its data even when the power is turned off. Due to this permanent storage characteristic, non-volatile memory has been widely used for data storage in electronic products, and there have been many related studies. In this chapter, we will focus on the non-volatile memory.

According to the storage materials, non-volatile memory can be divided into two classes. For the first class, the injected charges are stored in a conducting or semiconducting material which is completely surrounded by insulators, as shown in Fig. 1.2(a). Since the storage material acts as a completely electrically isolated gate, we call this kind of memory as floating gate (FG) memory [1.1-1.2]. On the other hand, for the second class, the injected charges are stored in "discrete" trapping centers of a dielectric material instead of conducting or semiconducting material, as illustrated in Fig. 1.2 (b). Due to this charge trapping characteristic, we call this kind of memory as charge-trapping (CT) memory [1.3-1.4].

In this section, we will first review the history of non-volatile memory and then introduce the evolution and restrictions of SONOS memory.

1.1.1 Historical Review

The first non-volatile memory device was proposed by D. Kahng and S. M. Sze in 1967 [1.5], and the possibility of non-volatility in MOS-type device was also first recognized. Figure 1.3 illustrates the proposed non-volatile memory. They used layered structure (from bottom to top: thin oxide I_l, floating metal M_1, thick oxide I_2, and metal gate M_2) to replaced the gate dielectric of conventional MOSFET. Since the metal-insulator-metal-insulator-semiconductor structure, it was called MIMIS memory.

The program/write operation can be performed by applying a positive voltage to M_2. The

high e-field in the I_1 could provide sufficient electron tunneling (direct tunneling, DT), and then these injected electrons are "captured" in M_1 since the thick I_2 could block injected electrons from discharging to M_2. When the gate voltage is removed, the electron out-tunneling is blocked by I_1 and I_2, therefore, these captured electrons will stay in floating gate. On the other hand, using the same tunneling mechanism (DT), the captured electrons can be removed from the floating gate by applying a negative voltage to M_2 (erase operation).

However, the operation (DT) of MIMIS memory needs a very thin oxide (< 2.5nm) [1.6-1.7]. It is difficult to fabricate such thin oxide without any defect. Moreover, any pinhole in I_1 will leak all the stored charges in M_1 due to its conductive property. Due to these issues, this MIMIS memory could not be realized at that time. However, MIMIS memory still was a pioneer in the non-volatile memory industry.

There are two possible solutions to solve the issues of MIMIS memory. One is replacing the M_1 by a charge trapping dielectric, and anther is increasing the thickness of I_1.

For the first solution, metal-nitride-oxide-semiconductor (MNOS) memory was introduced in 1967 by Wegener et al [1.8], as illustrated in Fig. 1.4. In the MNOS, the M_1 and I_2 in MIMIS are replaced by nitride which has “discrete” trapping centers, therefore, the pinhole in I_1 will not cause trapped charges to leak out. This device is programmed by applying a high positive voltage to the gate, so electrons tunnel from the Si conduction band to the nitride and are then trapped into the trapping centers. On the other hand, erase is achieved by applying a high negative voltage to the gate, so that holes tunnel from the Si valence band and are then trapped into the trapping centers.

For the second solution, floating gate avalanche injection MOS (FAMOS) was first proposed by Frohman-Bentchkowsky in 1971, as illustrated in Fig. 1.5 [1.9-1.11]. Since the tunnel oxide of FAMOS memory is thicker (~ 100nm), DT is excluded. Therefore, special program and erase are needed. Program is performed by biasing the drain junction to avalanche breakdown (V_D > 30V), such that the electrons in the avalanche plasma can inject

from the drain region into the floating gate. On the other hand, erase is carried out by ultraviolet (UV) or X-ray. FAMOS memory finally evolved into electrically programmable read-only memory (EPROM).

However, FAMOS memory had some drawbacks such as inefficient program and inconvenient erase, and that could be improved by several methods. For example, in stacked gate avalanche injection MOS (SAMOS) memory [1.12-1.13], an external gate is added, as illustrated in Fig. 1.6. The external gate can further improve the programming efficiency. Moreover, electrical erase also became possible by field emission through the top dielectric. Therefore, electrically-erasable programmable read-only memory (EEPROM) products became feasible.

1.1.2 Evolution of SONOS Memory

The first CT memory based on nitride trapping layer was proposed for more than 40 years. The charges (electrons/holes) are injected from channel into nitride by tunneling through an ultra-thin oxide (typically 1.5 to 3nm). Typically, the trapped charges can be maintained in nitride for at least 10 years if the nitride can be isolated perfectly.

The first product level nitride based CT memory was available in 1975 by P-channel MNOS [1.14], as illustrated in Fig. 1.7(a). It consists of aluminum (Al) gate electrode, 45nm nitride charge trapping layer, and 2nm tunnel oxide. However, this memory had several issues. The first one is the high operation voltage (25-30V) because of its thick gate stack. The second one is the large standby current since the p-channel device is in depletion mode when there are electrons stored in the nitride. Moreover, the most important one is the metal gate which is the terribly pollutant in IC fabrication. Therefore, finding other material to replace metal gate was necessary.

The most important breakthrough for CT memory was the development of the Si-gate n-channel silicon-nitride-oxide semiconductor (SNOS) in 1980 [1.15], as illustrated in Fig.

1.7(b). Scaling down the nitride thickness (25nm), the operation voltage can be reduced to 14-18V. However, if we further scale down the nitride thickness, the channel injected charges may directly tunnel out to gate, or the trapped charges may de-trap to gate. Moreover, the gate injected charges may also affect the stored charges in nitride.

These issues can be eliminated d by providing an oxide on top of nitride, as shown in Fig. 1.7(c), and we called it as SONOS (silicon-oxide-nitride-oxide-semiconductor) memory [1.3,1.16]. Due to the insertion of top oxide, the nitride thickness can be further reduced to 5nm, and the operation voltage can be around 10V. Figure 1.8 shows the program/erase operations of SONOS memory. Under +10V (V_G = +10V, V_S = V_D = V_B = 0V) programming, the channel electrons can inject into nitride by DT, and are then trapped into trapping centers. On the other hand, under –10V (V_G = –10V, V_S = V_D = V_B = 0V), the channel holes can inject into nitride to compensate for trapped electrons.

1.1.3 Value and Restrictions of SONOS Memory

The rapidly growing market share of memories has brought about competitive development of memory technologies. Among different types of memories, Flash memory has become extremely attractive due to its significant advantages such as non-volatility, repetitive electrical program/erase capability, high density, low cost, low power consumption, high speed, high endurance, and long data retention [1.17-1.19]. The most particular feature of Flash memory is that the content of the whole chip can be cleared in one step, so called “Flash” memory.

Conventional Flash memory using floating gate (FG) device has become the major product in non-volatile memory since 1990s, however, the high voltage operation and the scaling limitation have prompted the search of new Flash memory design. The most promising structure is SONOS because of the good scalability, simple process, and low voltage operation [1.20-1.22]. Since the nitride has “discrete” charge-trapping characteristic,

the insulating oxide layers can be further scaled down without pinhole effect, and the physically 2-bits-per-cell operation is allowed (NROM concept) [1.23-1.25]. Moreover, it also offers immunity to stress-induced leakage current (SILC) and provides good few-electron storage capability. On the other hand, SONOS is also a candidate for embedded memory applications because its processes are compatible with conventional CMOS technology, except for the formation of the oxide-nitride-oxide (ONO) dielectric stack.

However, the thin tunnel oxide in SONOS still causes some problems due to the considerable direct tunneling leakage under low e-field. This can be explained by the simulated hole tunneling current density (J_h) vs. tunnel oxide e-field (E_{ox}) curves with various oxide thickness, as shown in Fig. 1.9. To enhance required erase current density ($> 10^{-4}A/cm^2$) under reasonable erase field (~ 11MV/cm), a very thin tunnel oxide (< 25Å) is necessary. However, a conflict to data retention performance will be suffered because at low e-field the direct tunneling leakage can not be avoided. This means that there is no single tunnel oxide thickness that can satisfy both fast erase speed and good data retention.

Recently, a novel band-gap engineered SONOS (BE-SONOS) memory was proposed [1.26] to provide high erase speed as well as excellent data retention. Figure 1.10 shows that in BE-SONOS a composite ONO tunneling barrier is applied to replace the traditional tunnel oxide in SONOS. This ONO barrier has different functions for program/erase and data retention, as shown in Fig. 1.11. Under high e-field (Fig. 1.11(a)), the band offset happens so that the barrier height of N1 and O2 are almost screened, then the holes can directly tunnel through the O1 (13Å). On the other hand, at low e- field retention state (Fig. 1.11(b)), both electron de-trapping and hole external tunneling can be completely suppressed by the total barrier stack (O1+N1+O2). Based on such band-offset effect, the thickness of ONO barrier becomes variable and adjustable for the required high-field hole tunneling current and low-field retention criteria, so that the device performance can be further optimized. Therefore, BE-SONOS is promising for next generation non-volatile memory.

1.2 Motivation and Objectives of Research

Although SONOS memory has turned into products, the understanding of trapped charge behaviors is still limited. Since the trapped charge behaviors govern the device performance and reliability of SONOS memory, characterizations of charge-trapping behaviors are the crucial needs to optimize the device performances.

In this dissertation, we proposed several new techniques to extensively investigate the charge trapping behaviors of various SONOS-type devices, including SONOS, BE-SONOS, SONS (SONOS without top oxide), SNOS (SONOS without bottom oxide), SNS (SONOS without top and bottom oxides), and Top BE-SONOS (an upside-down BE-SONOS). We wish to provide in-depth physical understanding of trapped charge behaviors.

1.3 Dissertation Organization

The organization of this dissertation is briefly described below.

Chapter 2 introduces the basic of SONOS-type memory. The basic operating principle and models used in this dissertation are introduced. The main charge transport mechanisms for device operations are also discussed in detail. Moreover, we summarize some papers which investigated the trapped charge locations for both lateral and vertical directions.

In chapter 3, the principle of our novel gate-sensing and channel-sensing (GSCS) method is discussed in detail, including the theoretical equations, sample preparation, basic device characteristics, and method demonstration. We also compare GSCS method with other previous methods for a systematic understanding. Therefore, the results obtained by our method can be double-confirmed, and the advantages of our method can be fully understood. Moreover, several factors that affect the accuracy of our method are also analyzed.

Chapter 4 illustrates the applications of GSCS method on the charge centroids as well as the capture efficiency of various SONOS devices. Using bulk trap model to compare SONOS,

SONS, and SNOS, we can clearly verify that electrons are mainly distributed inside the bulk nitride or the interfaces between oxide and nitride. On the other hand, using two-region approximation model, we can successfully monitor the channel injected charges as well as the gate injected charges for SONS and SNS. Based on the theoretical Q-t model, we can further fit our data with that extracted by GSCS method, and further to obtain the capture efficiency of different nitride layers.

Chapter 5 illustrates the applications of GSCS method on the intra-nitride transport behaviors and the reliability of various SONOS devices. For the first time, we can directly investigate the intra-nitride charge transport behaviors of SONOS-type devices during ±FN injection, FN cycling, and high temperature baking. The electron injection, hole injection, and electron de-trapping behaviors can be accurately monitored.

In chapter 6, we utilize GSCS method to investigate the gate-injection operated SONOS-type devices. Contrary to the conventional channel-injection operated SONOS-type devices, gate-injection operated SONOS-type devices using gate injection program (P) and erase (E) through the top oxide. Since the gate oxide is not stressed by P/E operations, the devices have better cycling endurance. Our method can be successfully applied to this kind of devices without any modification. In this chapter, we track the charge centroids of gate-injection operated “top BE-SONOS” and various SONOS-type devices. Moreover, we also investigate the charge transport for both electron and hole under different situations and the capture efficiency of nitride layers.

Chapter 7 introduces a systematic method, which can be use to distinguish two different erase mechanisms: electron de-trapping and external hole injection. Based on GSCS method, we can accurately extract the erase tunneling current density (J) as a function of tunnel oxide e-field (E_{ox}) from experimental results. J-E curve reflects the physics directly and thus helps understand the detailed erase mechanisms. In this chapter, the erase mechanisms of SONOS-type devices for both channel- and gate-injection operations are studied in detail.

Moreover, for the devices with external hole injection erase mechanism, we also used theoretical tunneling equations to fit the extracted J-E curves, thus double confirmed our results. On the other hand, for the devices with electron de-trapping erase mechanism, we also examined the refill characteristics to double confirm our results. This systematic method can help us to further understand of the erase mechanisms of SONOS-type devices.

In chapter 8, a new pulse-IV technique is developed and used to study the transient charge-trapping behaviors of SONOS-type devices. Using this technique, the transient tunneling currents of various SONOS-type capacitors can be characterized concurrently with the gate pulses. On the other hand, this technique can accurately characterize the transient drain currents of SONOS-type transistors immediately after programming/erasing without disturb. Since this technique has such benefit, it can be further used to investigate the behaviors of quasi-non-volatile memory.

Chapter 9 summarizes the findings and contributions of this dissertation, and provides the suggestions for future works.

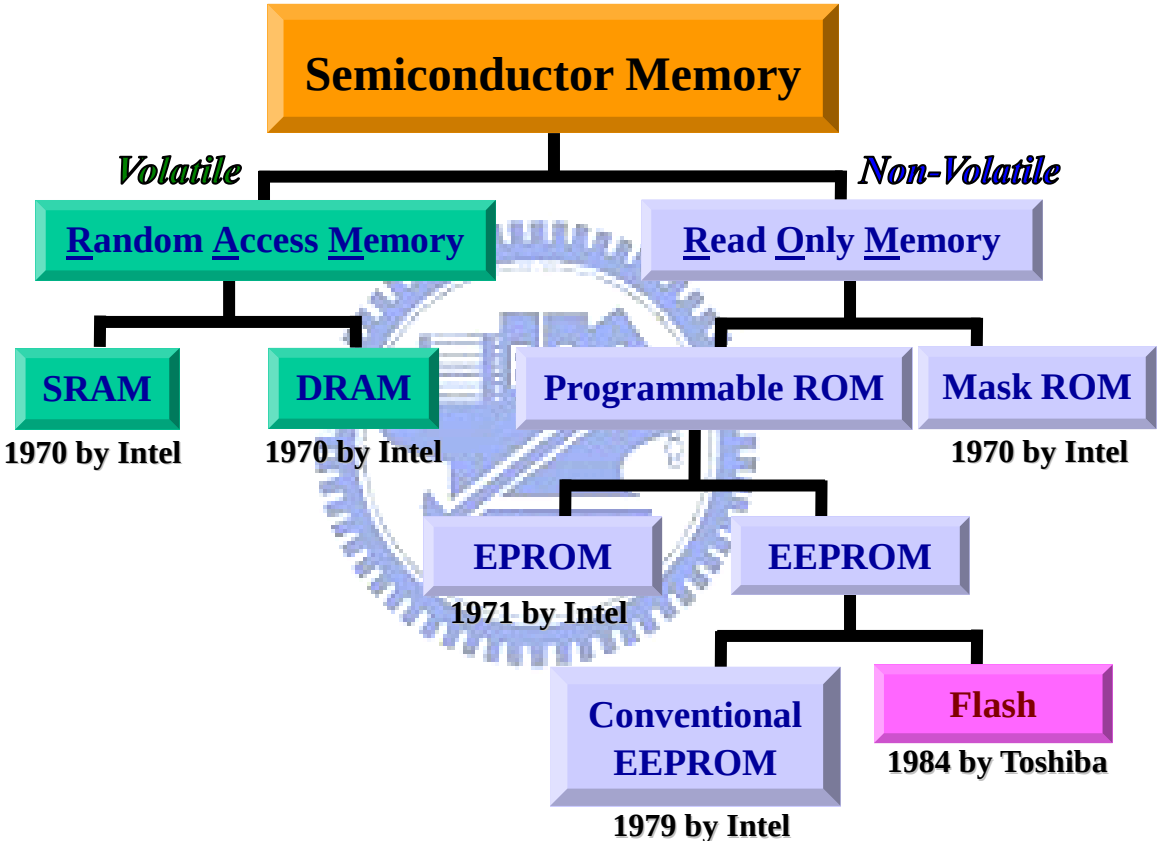


Fig. 1.1 Summary of semiconductor memory.

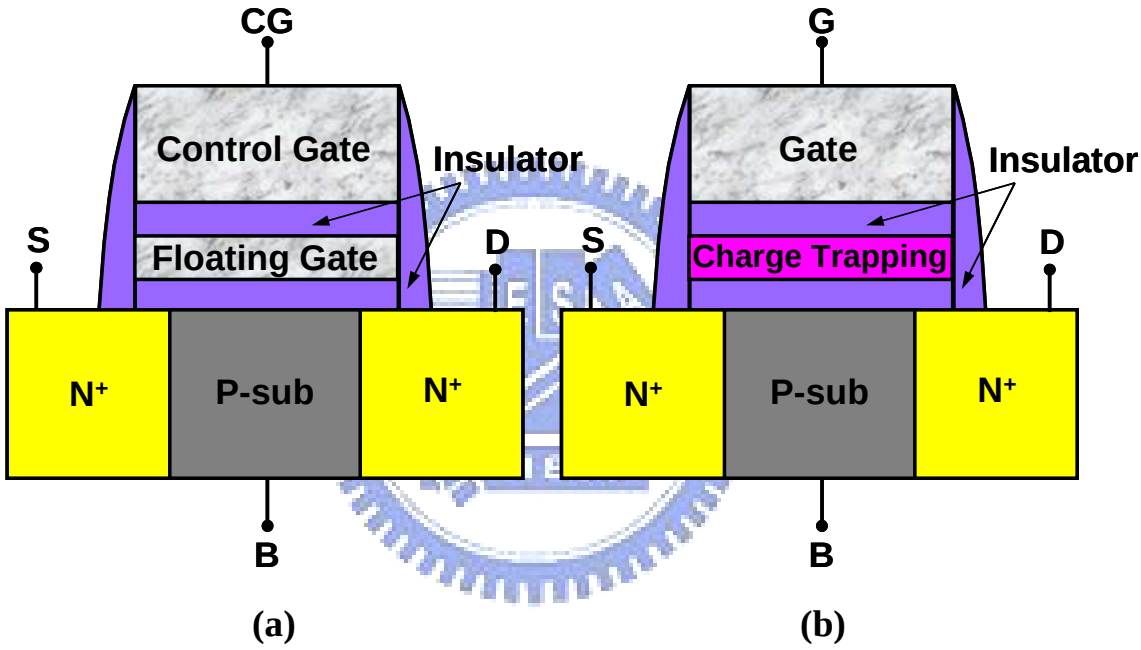


Fig. 1.2 Two classes of non-volatile semiconductor memory: (a) floating gate (FG) memory; (b) charge-trapping (CT) memory.

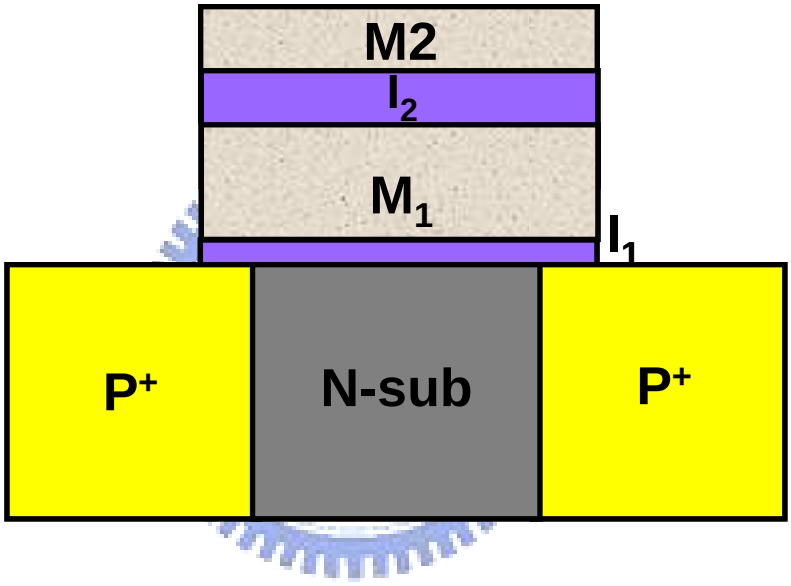


Fig. 1.3 D. Kahng and S. M. Sze proposed first non-volatile memory device in 1967. Program and erase are performed by direct tunneling (DT) of electrons through the thin oxide I_1.

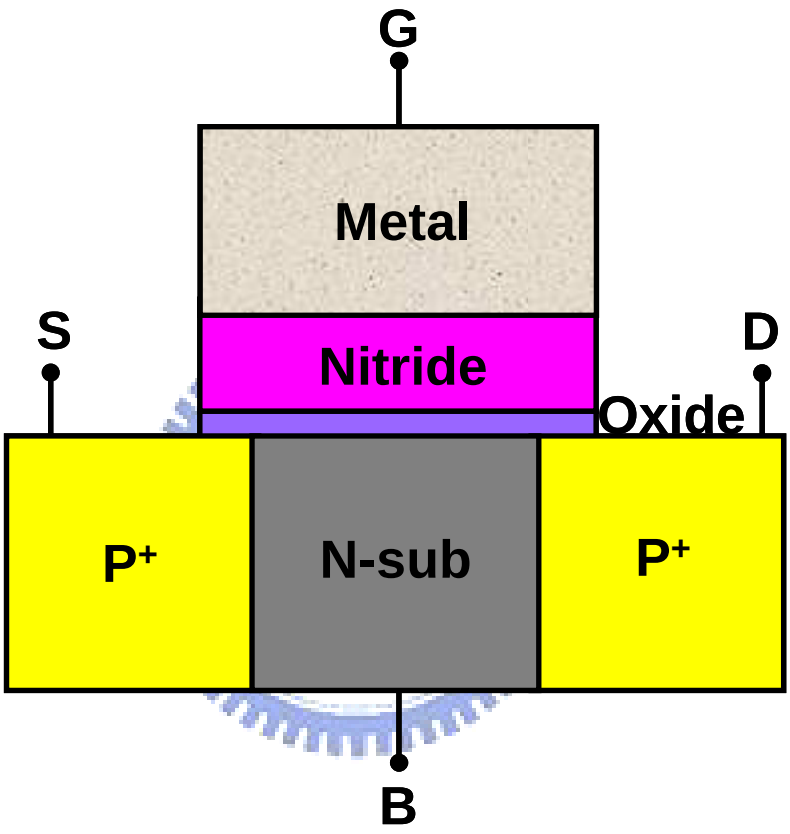


Fig. 1.4 Wegener et al. proposed MNOS memory in 1967. This device is programmed by electrons tunneling from the Si conduction band to nitride trapping centers and erased by holes tunneling from the Si valence band to the nitride trapping centers.

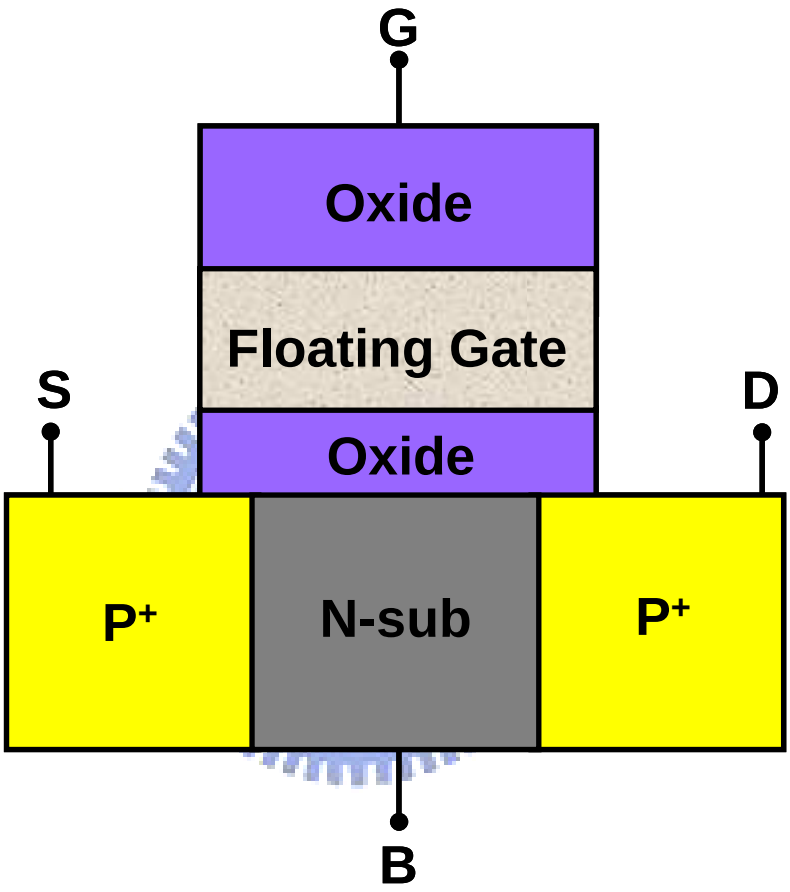


Fig. 1.5 FAMOS (Floating gate Avalanche injection MOS). Program is performed by injection of high energetic electrons created in the drain avalanche plasma while erase is possible by UV or X-ray radiation.

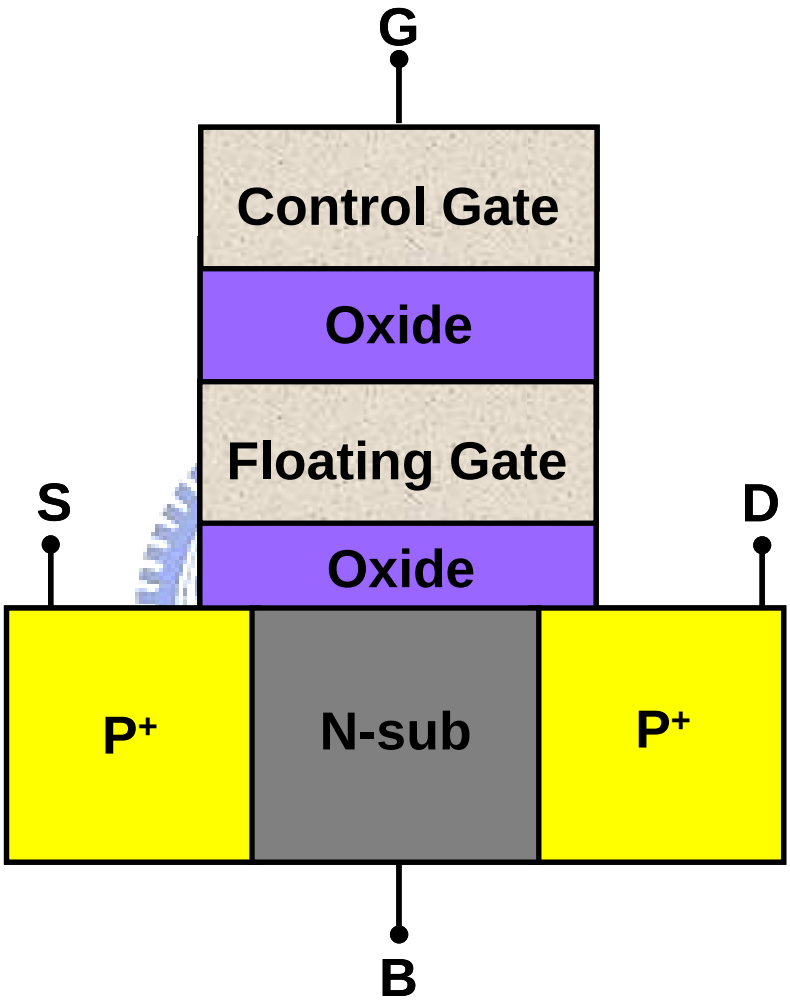


Fig. 1.6 SAMOS (Stacked gate Avalanche injection MOS) memory. Its program speed is higher than FAMOS memory due to the additional external gate. Erase can be achieved by field emission through the top dielectric.

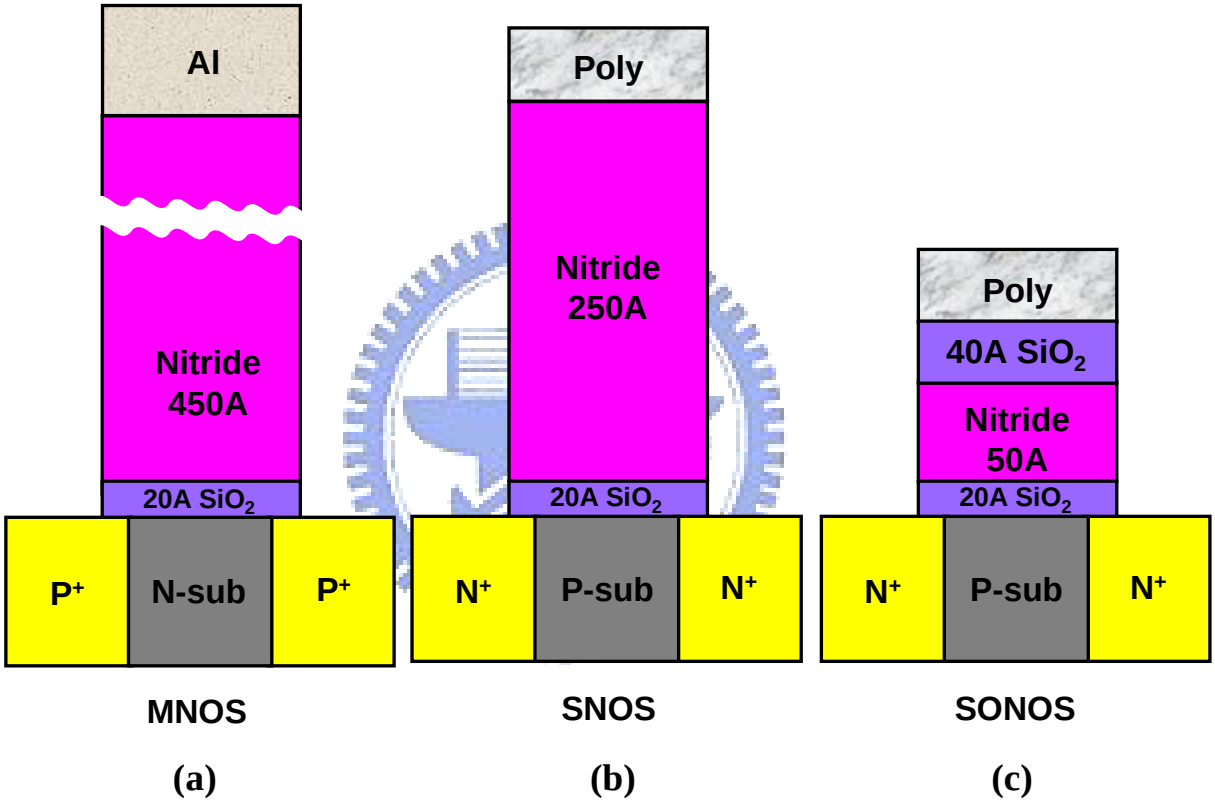


Fig. 1.7 Evolution of SONOS-type memory. (a) P-channel MNOS. (b) N-channel SNOS. (c) N-channel SONOS.

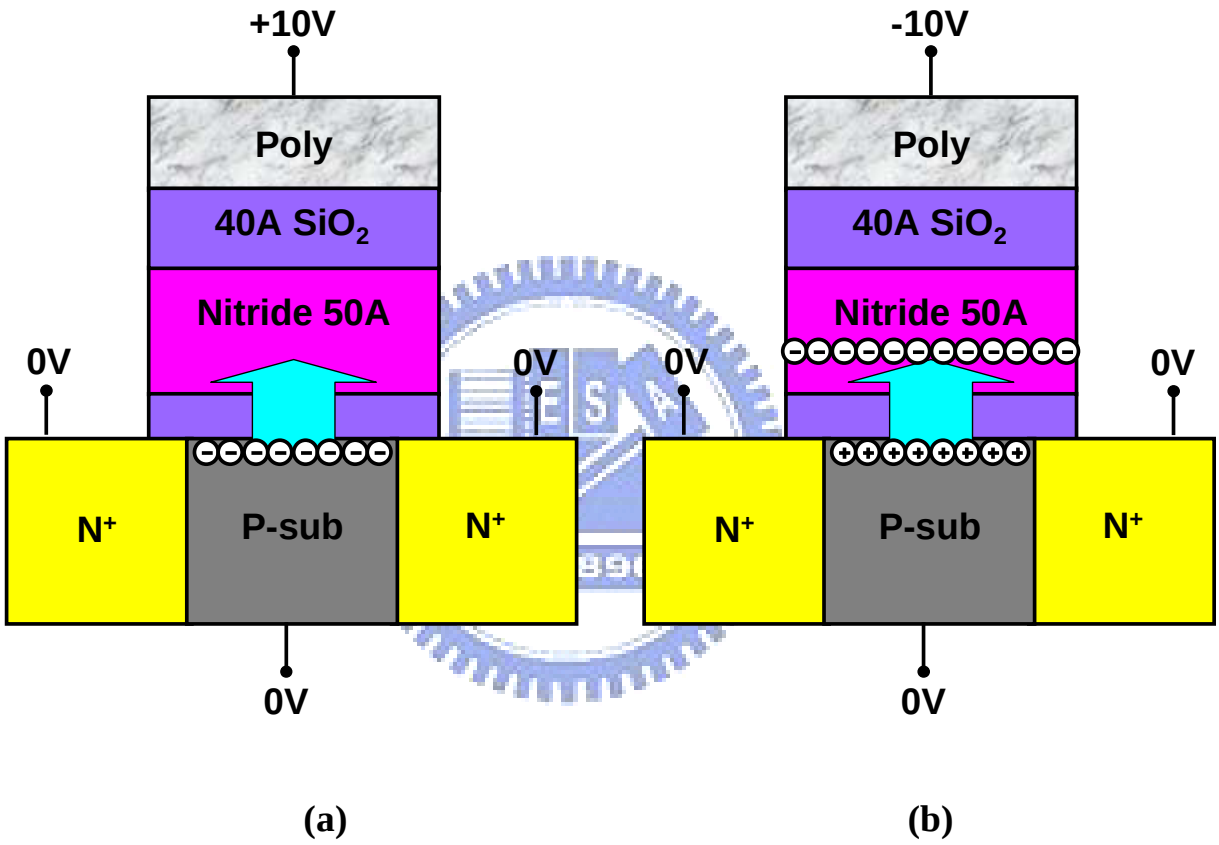


Fig. 1.8 (a) Program (+10V) operation and (b) erase (–10V) operation of SONOS. During programming, the channel electrons inject into nitride. On the other hand, during erasing the channel holes inject into nitride to compensate for trapped electrons.

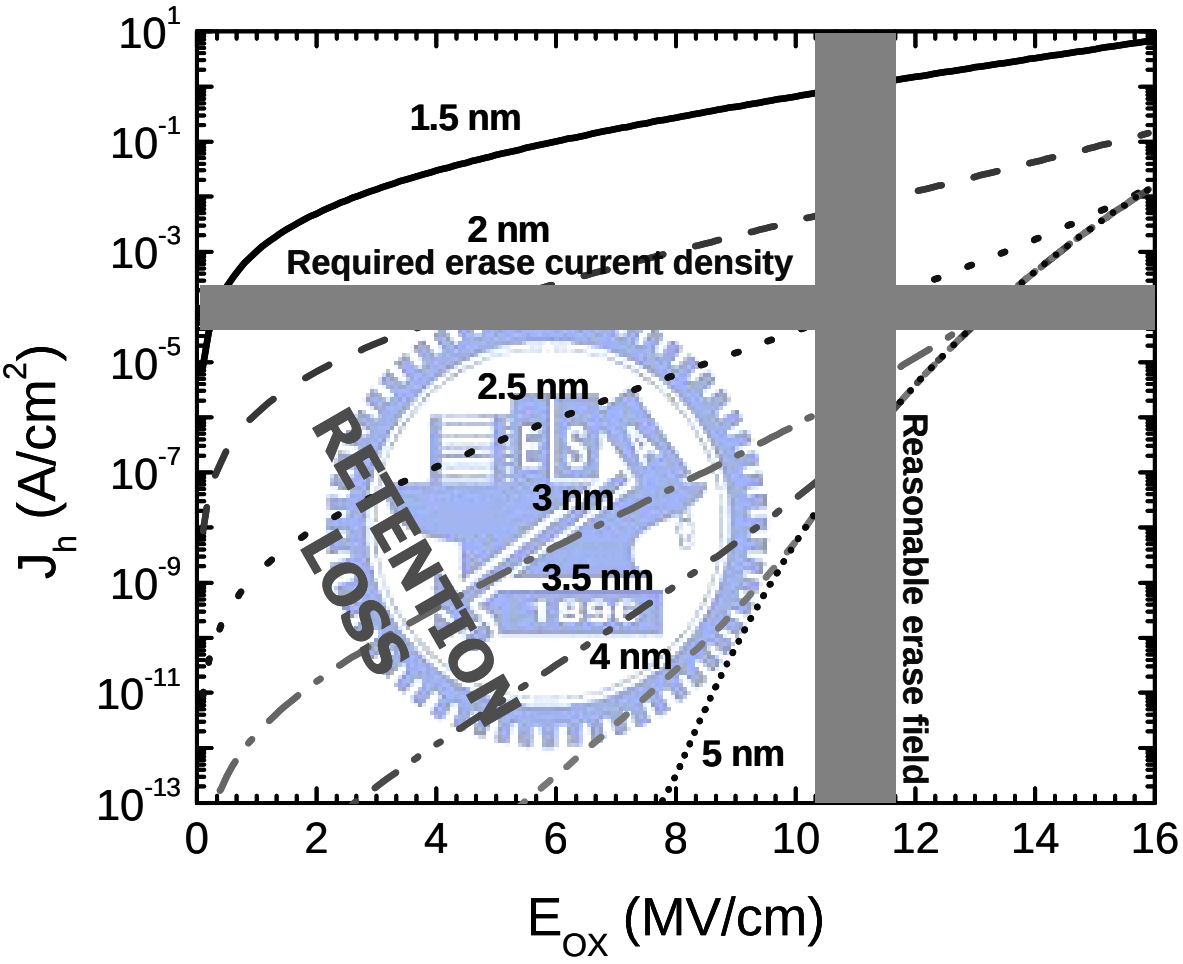


Fig. 1.9 Simulation of hole tunneling current density (J_h) to tunnel oxide electric field (E_{ox}) with various thickness schemes. To enhance required erase current density under reasonable erase field, a very thin tunnel oxide such as 25Å is necessary. However, a conflict to data retention performance will be suffered.

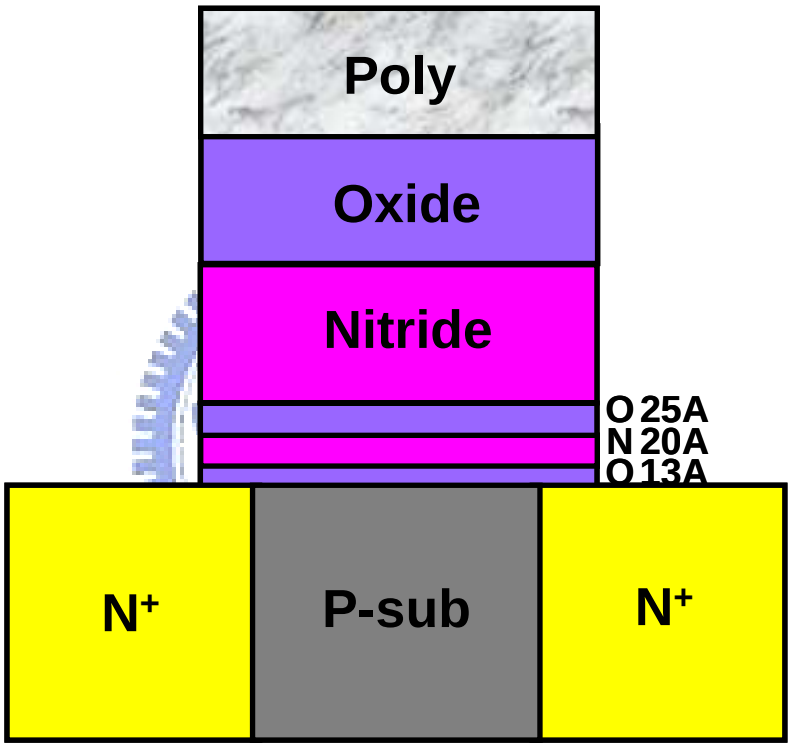


Fig. 1.10 BE-SONOS (band-gap engineered SONOS) memory. A composite ONO tunneling barrier could provide high erase speed as well as excellent data retention.

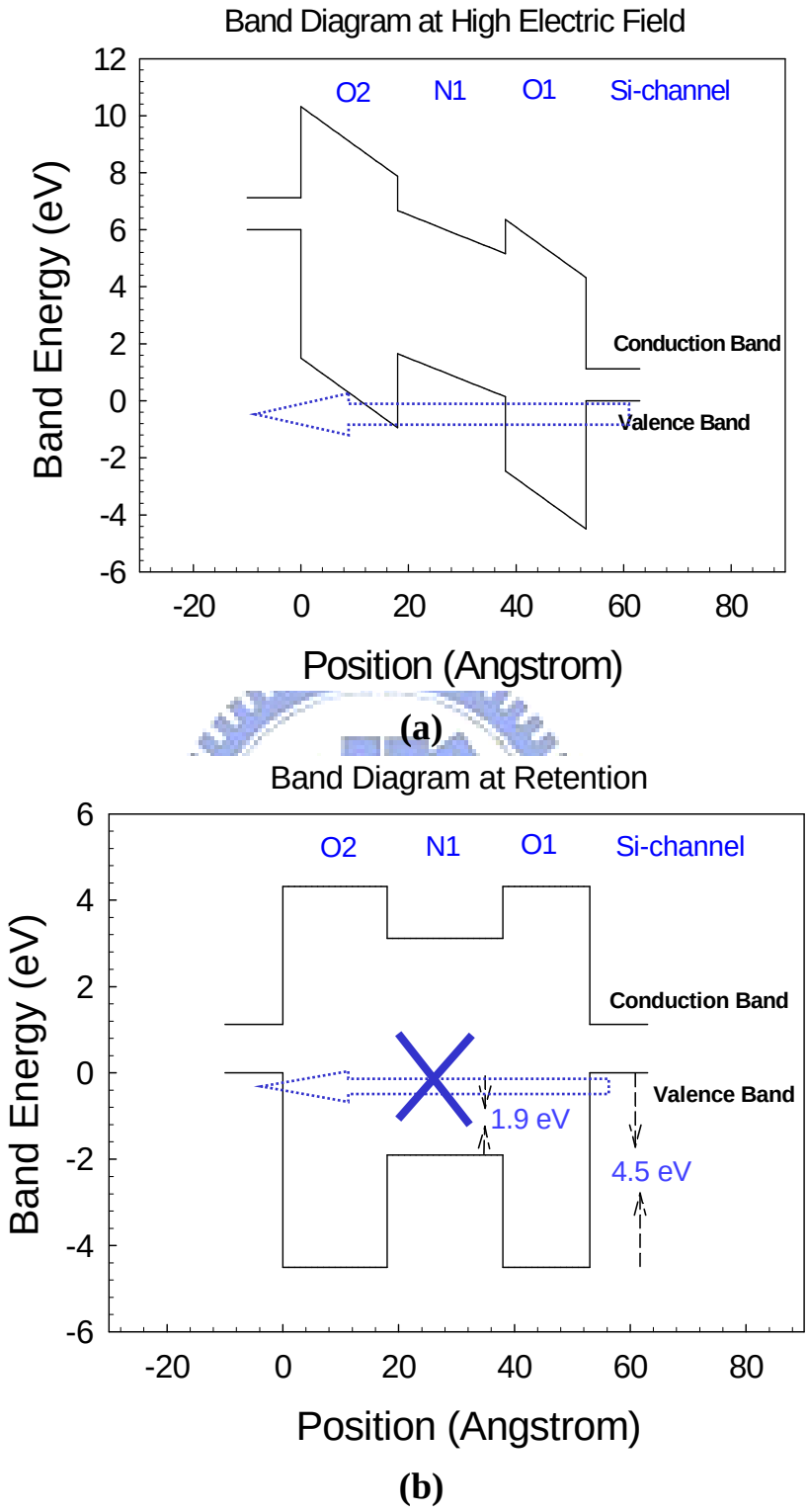


Fig. 1.11 Band-offset effect by using an ONO barrier as tunneling dielectric in BE-SONOS memory. (a) At high e-field, the band offset happens so that the holes directly tunnel through the O1. (b) At low e-field (retention state), both electron de-trapping and hole external tunneling are prohibited by the total O1/N1/O2 barrier stack.

CHAPTER TWO

BASIC OF SONOS-TYPE MEMORY

OUTLINE

2.1 Basic Device Equations and Models

Before further characterizing the trapped charge behaviors, we should first understand the basic operating principle and related models of SONOS-type memory. In this section, we will first introduce the basic operating principle of SONOS. Then, we discuss the e-field of each ONO film for program/erase and the transient currents under different trap location assumptions. From these e-field and transient current models, we can obtain the relation between e-field and transient current. This information can help us further understand the trapped charge behaviors.

2.1.1 Basic Operating Principle [1.3,1.6]

The storage principle of non-volatile memory devices can be simplified as the charges (Q_T) are trapped in the gate insulator of a MOSFET, as illustrated in Fig. 2.1(a). The trapped charges will change the threshold voltage (V_T) of MOSFET and provide two distinct states (0 for erased state and 1 for programmed state), as illustrated in Fig. 2.1(b). Based on the basic theory of the MOSFET, its V_T can be given by

$$V_T = 2\phi_F + \phi_{ms} - \frac{Q_I}{C_I} - \frac{Q_D}{C_I} - \frac{Q_T}{\varepsilon_0 \varepsilon_I} d_I \qquad (2\text{-}1)$$

where ϕ_F is the Fermi-potential of the semiconductor at the surface, ϕ_{ms} is the work function difference between the gate and the bulk material, Q_I is the fixed charge at the silicon/ insulator interface, Q_D is the charge in the silicon depletion layer, Q_T is the charge stored in the gate insulator at a distance d_I from the gate, C_I is the capacitance of the insulator layer, ε_I is the dielectric constant of the insulator, and ε_0 is the permittivity of free space. Therefore, the V_T shift (ΔV_T) caused by the Q_T is given by

$$\Delta V_T = -\frac{Q_T}{\varepsilon_0 \varepsilon_I} d_I \qquad (2\text{-}2)$$

Negative Q_T (electron) will cause positive ΔV_T while positive Q_T (hole) will cause negative ΔV_T.

Applying an appropriate gate voltage (V_{read}) which is between two possible V_T's, as illustrated in Fig. 2.1(b), the stored information can be detected. The detected current is high for erased state but low for programmed state, so that we can easily distinguish the stored states.

2.1.2 Electric Field Model

The ONO energy band diagram of SONOS-type memory under zero bias is shown in Fig. 2.2. T_{Box} is the bottom oxide (B.O.) thickness, T_N is the nitride thickness, and T_{Tox} is the top oxide (T.O.) thickness. The conduction band offset between oxide and nitride is about 1.05eV, and the valence band offset between oxide and nitride is about to 2.85eV [2.1].

Under positive gate bias (V_G), the ONO energy band diagram bends, as illustrated in Fig. 2.3(a). The voltage drop on total ONO is equal to V_G if we ignore the voltage drops on Si-sub and gate. Therefore, the B.O. e-field (E_{Box}) and the T.O. e-field (E_{Tox}) can be easily calculated by

$$E_{Box} = E_{Tox} = \frac{V_G}{EOT} \tag{2-3}$$

where the EOT is the equivalent oxide thickness of total ONO. Since there is no charge at nitride/B.O. interface, from continuity equation [2.2]: $\varepsilon_{ox}E_{BO} - \varepsilon_N E_N = 0$, we can obtain the nitride e-field (E_N).

$$E_N = \frac{\varepsilon_{ox}}{\varepsilon_N} E_{Box} = \frac{\varepsilon_{ox}}{\varepsilon_N} \cdot \frac{V_G}{EOT} \tag{2-4}$$

where ε_{ox} and ε_N is the dielectric constant of oxide and nitride, respectively. From Eq. (2-4), we can know that the material with higher dielectric constant (k) has lower e-field. That is why high-k materials have been proposed to replace the T.O. of SONOS memory to reduce the gate injection and release the erase saturation [2.3-2.4].

If there are charges in the nitride, the e-field of ONO will change. For example, the trapped electrons (holes) at nitride/B.O. interface will cause decreased (increased) E_{Box} but

increased (decreased) E_N, as illustrate in Fig. 2.3(b). Fortunately, the changed e-fields can be simply calculated based on continuity equation and voltage conservation. From Eq. (2-2), the charges trapped in nitride can be extracted from ΔV_T according to

$$Q_T = -\frac{\Delta V_T \cdot \varepsilon_0 \varepsilon_I}{d_I} \tag{2-5}$$

In order to simplify this subject, we first consider three cases: (a) charges at the B.O./nitride interface, (b) charges at the T.O./nitride interface, and (c) charges at the center of nitride.

(a) Charges at the B.O./nitride interface:

Since there is Q_T at B.O./nitride interface, and there is no charge at T.O./nitride interface, the continuity equation gives us

$$\varepsilon_{ox} E_{Box} - \varepsilon_N E_N = Q_T$$

$$\Rightarrow \varepsilon_{ox} E_{Box} - \varepsilon_N E_N = -\frac{\Delta V_T \cdot \varepsilon_{ox}}{T_{Tox} + T_N \frac{\varepsilon_{ox}}{\varepsilon_N}} \tag{2-6}$$

$$\varepsilon_N E_N - \varepsilon_{ox} E_{Tox} = 0 \tag{2-7}$$

From voltage conservation, the summation of voltage drop on each ONO film is equal to the external gate bias.

$$T_{Box} E_{Box} + T_N E_N + T_{Tox} E_{Tox} = V_G \tag{2-8}$$

From Eqs. (2-6)-(2-8), we can directly solve three variables: E_{Box}, E_N, and E_{Tox}.

$$E_{Box} = \frac{V_G - \Delta V_T}{EOT} \tag{2-9}$$

$$E_N = \frac{\varepsilon_{ox}}{\varepsilon_N} \cdot [\frac{V_G - \Delta V_T}{EOT} + \frac{\Delta V_T}{T_{Tox} + T_N \frac{\varepsilon_{ox}}{\varepsilon_N}}] \tag{2-10}$$

$$E_{Tox} = \frac{V_G - \Delta V_T}{EOT} + \frac{\Delta V_T}{T_{Tox} + T_N \frac{\varepsilon_{ox}}{\varepsilon_N}} \tag{2-11}$$

(b) Charges at the T.O./nitride interface:

Since there is no charge at B.O./nitride interface, and there is Q_T at T.O./nitride interface, the continuity equation gives us

$$\varepsilon_{ox}E_{Box} - \varepsilon_N E_N = 0 \tag{2-12}$$

$$\varepsilon_N E_N - \varepsilon_{ox}E_{Tox} = Q_T$$

$$\Rightarrow \varepsilon_N E_N - \varepsilon_{ox}E_{Tox} = -\frac{\Delta V_T \cdot \varepsilon_{ox}}{T_{Tox}} \tag{2-13}$$

From Eqs. (2-8), (2-12), and (2-13), we can directly solve E_{Box}, E_N, and E_{Tox}.

$$E_{Box} = \frac{V_G - \Delta V_T}{EOT} \tag{2-14}$$

$$E_N = \frac{\varepsilon_{ox}}{\varepsilon_N} \cdot \frac{V_G - \Delta V_T}{EOT} \tag{2-15}$$

$$E_{Tox} = \frac{V_G - \Delta V_T}{EOT} + \frac{\Delta V_T}{T_{Tox}} \tag{2-16}$$

(c) Charges at the center of nitride:

The ONO energy band diagram for charges at the center of nitride is shown in Fig. 2.4. The nitride is divided into two equal parts. The bottom nitride e-field is E_{N1} while the top nitride e-field is E_{N2}. The trapped electrons (holes) cause decreased (increased) E_{N1} but increased (decreased) E_{N2}, as illustrated in Fig. 2.4. Since there is no charge at B.O./nitride and T.O./nitride interfaces, and there is Q_T at bottom nitride/top nitride interface, the continuity equation gives us

$$\varepsilon_{ox}E_{Box} - \varepsilon_N E_{N1} = 0 \tag{2-17}$$

$$\varepsilon_N E_{N2} - \varepsilon_{ox}E_{Tox} = 0 \tag{2-18}$$

$$\varepsilon_N E_{N1} - \varepsilon_N E_{N2} = Q_T$$

$$\Rightarrow \varepsilon_N E_{N1} - \varepsilon_N E_{N2} = -\frac{\Delta V_T \cdot \varepsilon_{ox}}{T_{Tox} + \frac{T_N}{2}\frac{\varepsilon_{ox}}{\varepsilon_N}} \tag{2-19}$$

The voltage conservation consists of four films.

$$T_{Box}E_{Box}+\frac{T_N}{2}E_{N1}+\frac{T_N}{2}E_{N2}+T_{Tox}E_{Tox}=V_G \tag{2-20}$$

From Eqs. (2-17)-(2-20), we can directly solve E_{Box}, E_{N1}, E_{N2}, and E_{Tox}.

$$E_{Box}=\frac{V_G-\Delta V_T}{EOT} \tag{2-21}$$

$$E_{N1}=\frac{\varepsilon_{ox}}{\varepsilon_N}\cdot\frac{V_G-\Delta V_T}{EOT} \tag{2-22}$$

$$E_{N2}=\frac{\varepsilon_{ox}}{\varepsilon_N}\cdot[\frac{V_G-\Delta V_T}{EOT}+\frac{\Delta V_T}{T_{Tox}+\frac{T_N}{2}\frac{\varepsilon_{ox}}{\varepsilon_N}}] \tag{2-23}$$

$$E_{Tox}=\frac{V_G-\Delta V_T}{EOT}+\frac{\Delta V_T}{T_{Tox}+\frac{T_N}{2}\frac{\varepsilon_{ox}}{\varepsilon_N}} \tag{2-24}$$

From the results of three cases, we find that they can be simplified as one general case: the trapped charges locate at x from B.O./nitride interface, as illustrated in Fig. 2.5(a), and the e-field of each film can be calculated by

$$E_{Box}=\frac{V_G-\Delta V_T}{EOT} \tag{2-25}$$

$$E_{Tox}=\frac{V_G-\Delta V_T}{EOT}+\frac{\Delta V_T}{EOT_{QG}} \tag{2-26}$$

$$E_{N1}=\frac{\varepsilon_{ox}}{\varepsilon_N}\cdot E_{Box} \tag{2-27}$$

$$E_{N2}=\frac{\varepsilon_{ox}}{\varepsilon_N}\cdot E_{Tox} \tag{2-28}$$

where EOT_{QG} is the equivalent oxide thickness of the distance from Q_T to gate. It should be noted that the E_{Box} is independent of charge location. On the other hand, for the ONO energy band diagram under negative gate bias, as shown in Fig. 2.5(b), we can follow the same procedure as positive gate bias, but total voltage drop on ONO should be equal to $|V_G|$. The e-fields can be simplified as

$$E_{Box} = \frac{|V_G| + \Delta V_T}{EOT} \tag{2-29}$$

$$E_{Tox} = \frac{|V_G| + \Delta V_T}{EOT} - \frac{\Delta V_T}{EOT_{QG}} \tag{2-30}$$

$$E_{N1} = \frac{\varepsilon_{ox}}{\varepsilon_N} \cdot E_{Box} \tag{2-31}$$

$$E_{N2} = \frac{\varepsilon_{ox}}{\varepsilon_N} \cdot E_{Tox} \tag{2-32}$$

Therefore, the e-fields of ONO films under both positive and negative biases for arbitrary charge location (x) can be summarized as Table 2.1.

2.1.3 Transient Current Model

If we assume all the injected charges are trapped in the nitride and contribute to ΔV_T, we can extract the transient hole current or electron current directly from ΔV_T. From Eq. (2-5), we can know that the trapped charges Q_T can be expressed as ΔV_T.

$$Q_T = -\frac{\Delta V_T \cdot \varepsilon_0 \varepsilon_{ox}}{EOT_{QG}} \tag{2-33}$$

The transient injection current during programming or erasing can be expressed as

$$J = \left|\frac{dQ_T}{dt}\right| = \frac{d\Delta V_T}{dt} \cdot \frac{\varepsilon_0 \varepsilon_{ox}}{EOT_{QG}} \tag{2-34}$$

Using Eq.(2-34) and Eqs. in Table 2.1, we can further plot the J vs. E curves of SONOS-type devices. For memory devices, the J vs. E curves can give us a lot of information. For example, compare with theoretical Eqs., we can make sure the detailed transport mechanisms; compare the current and e-field criteria, we can further optimize the operation window.

In this dissertation, we used J vs. E curves to confirm the charge location. Moreover, we also proposed a systematic method to distinguish the erase mechanisms of SONOS-type devices based on the comparison of J vs. E curves.

2.2 Carrier Transport Mechanisms

Charges transport through the tunnel dielectric is the basic mechanism to permit SONOS-type memory device operating. There have been many charge transport mechanisms proposed to explain the operation behaviors of SONOS-type devices. The energy band diagrams of the SONOS-type devices under positive (program) and negative (erase) gate biases, and the main conduction mechanisms are illustrated in Figs. 2.6(a) and (b), respectively [2.5]. Under positive gate bias, the substrate electrons tunnel through the B.O. (J1) will dominate. The injected electrons are trapped and then drift toward the T.O. by the Frenkel-Poole (FP) conduction (J2), moreover, some of them tunnel through T.O. to gate (J3). In general, hole injection from the gate (J4) is negligible due to the thicker T.O. and the larger hole barrier height (> 4eV for oxide to silicon). On the other hand, under negative gate bias either substrate holes inject to nitride (J5) or the trapped electrons de-trap to the Si-sub (J6). Moreover, the electrons and holes may recombine in the nitride (J8). However, it should be noted that the gate electrons are easily injected to nitride (J7) due to the smaller barrier height (~ 3.1eV for N^+ poly-gate). Therefore, the erase saturation is one of the important issues of SONOS-type devices which are needed to be solved.

In the section, we will discuss the most popular transport mechanisms of SONOS-type devices, including Flower-Nordheim (FN) tunneling, direct tunneling (DT), modified Flower-Nordheim (MFN) tunneling, channel hot electron injection (CHEI), band-to-band tunneling induced hot carrier (BBHC) injection, and Frenkel-Poole (FP) tunneling.

2.2.1 Flower-Nordheim (FN) tunneling [2.5-2.6]

Which carrier transport mechanism contributes to device operation depends on the not only on the gate stack compositions but also on the applied voltages. We first consider the transport mechanisms which only relate to vertical e-field (typically, V_G is applied to gate but other terminals are grounded). The energy band diagrams for electron injection and hole

injection from Si-sub to nitride under FN tunneling are shown in Fig. 2.7(a) and (d), respectively. Φ_1 and Φ_2 are the oxide and nitride barrier heights for electron, respectively. Φ_1' and Φ_2' are the oxide and nitride barrier heights for hole, respectively. Under the B.O. e-field

$$qE_{Box} \geq \frac{\Phi_1}{T_{Box}} \quad \text{or} \quad \frac{\Phi_1'}{T_{Box}} \tag{2-35}$$

FN tunneling occurs where the electrons (holes) in the Si conduction band (valence band) see a triangular energy barrier with a width dependent on the applied gate biases. The FN current density can be described as

$$J = \alpha E_{Box}^2 \exp(-\frac{E_C}{E_{Box}}) \tag{2-36}$$

with

$$\alpha = \frac{m_0}{m_{ox}} \frac{q^3}{8\pi h} \frac{1}{\Phi_b} \tag{2-37}$$

and

$$E_C = 4\sqrt{2m_{ox}} \frac{\Phi_b^{3/2}}{3\hbar q} \tag{2-38}$$

where q is the charge of a single electron (1.6×10^{-19}C), h is Planck's constant, Φ_b is Φ_1 for electron injection and Φ_1' for hole injection, m_0 is the mass of a free electron (9.1×10^{-31}kg), m_{ox} is the electron or hole effective mass in SiO_2, and $\hbar = h/2\pi$.

Eq. (2-36) is the simplest form for FN tunneling and is quite adequate for non-volatile memory applications. A complete expression for the FN current density should take into account two second-order effects. One is image force barrier lowering, and another is the influence of temperature. However, if we take into account these two factors, the Eq. (2-36) becomes much more complex [2.6]. Therefore, for both DT and MFN tunneling, we also only consider the simplest forms.

2.2.2 Direct Tunneling (DT) [2.5]

When the gate bias or E_{Box} reduces to

$$\frac{\Phi_1-\Phi_2}{T_{Box}}<qE_{Box}<\frac{\Phi_1}{T_{Box}} \quad \text{or} \quad \frac{\Phi_1'-\Phi_2'}{T_{Box}}<qE_{Box}<\frac{\Phi_1'}{T_{Box}} \tag{2-39}$$

DT occurs, and the corresponding energy band diagrams are shown in Fig. 2.7(b) and (e) for electron injection and hole injection, respectively. Electrons (holes) from the Si conduction band (valence band) tunnel directly into the conduction band (valence band) of the nitride, and they see a trapezoid energy barrier with a width dependent on the B.O. thickness (T_{Box}). The DT current can be written as

$$J=\alpha E_{Box}^2\exp(-\frac{E_C}{E_{Box}}) \tag{2-40}$$

with

$$\alpha=\frac{m_0}{m_{ox}}\frac{q^3}{8\pi h}\frac{1}{[(q\Phi_b)^{1/2}-(q\Phi_b-qE_{Box}T_{Box})^{1/2}]^2} \tag{2-41}$$

and

$$E_C=4\sqrt{2m_{ox}}\frac{(q\Phi_b)^{3/2}-(q\Phi_b-qE_{Box}T_{Box})^{3/2}}{3\hbar q} \tag{2-42}$$

For the SONOS devices with an ultra thin B.O. (< 25Å), the DT is the dominant mechanism. During positive gate bias (programming), the electrons tunnel from Si conduction band to nitride by DT; during negative gate bias (erasing), the holes tunnel from Si valence band to nitride by DT.

2.2.3 Modified Flower-Nordheim (MFN) Tunneling [2.5]

If the gate bias or E_{Box} further reduces to

$$\frac{\Phi_1-\Phi_2}{T_{Box}-\gamma T_N}<qE_{Box}<\frac{\Phi_1-\Phi_2}{T_{Box}} \quad \text{or} \quad \frac{\Phi_1'-\Phi_2'}{T_{Box}-\gamma T_N}<qE_{Box}<\frac{\Phi_1'-\Phi_2'}{T_{Box}} \tag{2-43}$$

, where γ is ratio of the ε_{ox} and ε_N, charges tunnel through the whole B.O. and part of the nitride, as illustrated in Fig. 2.7(c) and (f). The MFN current can be given as

$$J=\alpha E_{Box}^2\exp(-\frac{E_C}{E_{Box}}) \tag{2-44}$$

with

$$\alpha = \frac{m_0}{m_{ox}} \frac{q^3}{8\pi h} \frac{1}{[(q\Phi_b)^{1/2} - (q\Phi_b - qE_{Box}T_{Box})^{1/2} + \gamma\sqrt{\frac{m_N}{m_{ox}}}(q\Phi_b - q\Phi_N - qE_{Box}T_{Box})^{1/2}]^2} \quad (2\text{-}45)$$

and

$$E_C = \frac{4\sqrt{2m_{ox}}[(q\Phi_b)^{3/2} - (q\Phi_b - qE_{Box}T_{Box})^{3/2}] + 4\gamma\sqrt{2m_N}[q\Phi_b - q\Phi_N - qE_{Box}T_{Box}]^{3/2}}{3\hbar q} \quad (2\text{-}46)$$

where m_N is the electron or hole effective mass in the nitride, and Φ_N is Φ_2 for electron injection and Φ_2' for hole injection. For BE-SONOS devices, the electrons and holes tunnel through the whole ONO tunneling barrier, which is much more complex than other SONOS-type devices. Therefore, we sometimes use MFN tunneling to simulate the tunneling behaviors of BE-SONOS devices.

2.2.4 Channel Hot Electron Injection (CHEI)

Since the SONOS-type memory has "discrete" traps in the charge trapping nitride layer, either uniform injection (by FN, DT, or MFN tunneling) or non-uniform injection have been proposed to operate the devices. By separately storing charges at drain side and source side, dual-bits-per-cell operation is allowed [1.23-1.25], so that the memory density becomes double. Due to this reason, non-uniform injection has been widely used for operating SONOS-type devices. In the following two sections, we will introduce the most popular non-uniform injection: CHEI and BBHC injection.

Figure 2.8 illustrates the CHEI phenomena for NMOSFET and PMOSFET [2.7]. Under large drain bias (high lateral e-field) the minority carriers are accelerated in the channel and then gain a lot of energy when they approach to drain. This phenomenon causes impact ionization at the drain, by which both minority and majority carriers are generated. The highly energetic majority carriers are collected at the Si-sub and form the so-called substrate current (I_{SUB}). On the other hand, the minority carriers are collected at the drain and form the

so-called drain current (I_D). Under the vertical oxide e-field favorable for attracting the electrons, a fraction of the heated electrons would surmount the Si-SiO_2 potential barrier and then inject into the gate terminal, which is so-called hot-carrier injection gate current (I_G) [2.7-2.8]. For SONOS-type devices, the injected electrons (I_G in MOSFET) will be locally trapped into the nitride layer near the drain side.

2.2.5 Band-to-band Tunneling Induced Hot Carrier (BBHC) Injection

The BBHC operation conditions and the transport carriers for N- and P-MOSFET are quite different, as illustrated in Fig. 2.9 [2.7]. For NMOSFET (Fig. 2.9(a)), the negative gate bias and positive drain bias lead to the possible hole injection toward the gate. However, for PMOSFET (Fig. 2.9(b)), the positive gate bias and negative drain bias are favorable for electron injection toward the gate. In general, the BBHC injection can be divided into two procedures, (1) band-to-band tunneling, and (2) carriers are accelerated due to lateral e-field and then injected toward the gate due to favorable vertical oxide e-field.

2.2.6 Carrier Transport in Nitride Layer [2.9]

In this section, we discuss the conduction mechanisms inside the nitride layer. Since the nitride film has “discrete” traps and smaller band gap than oxide, the conduction mechanisms are very different.

The conduction current (J) in nitride can be described by three components [2.10]. The first one (J_1) comes from field-enhanced thermal excitation, which is known as Frenkel-Pool (FP) effect [2.11]. The second one (J_2) comes from field ionization of trapped electrons, which is independent of temperature. The third one (J_3) comes from the hopping of thermally excited electrons from one trap to another, which has ohmic I–V characteristic and is exponentially dependent on temperature.

Under different e-fields and temperatures, the J is controlled by different components. J_1

dominates the current conduction at high e-field and high temperature; J_2 is the major contribution at high e-field and low temperature; J_3 becomes the dominant component at lower e-field and moderate temperature.

2.3 Retention Charge Loss Models

In addition to charge transport mechanisms, understanding data retention characteristics and charge loss mechanisms of SONOS-type devices is also critical for successful scaling of the SONOS technology. There have been many retention charge loss models proposed to explain the retention behaviors of SONOS-type devices, and in this section we will discuss some of these models in detail.

The main retention charge loss mechanisms of SONOS-type devices are illustrated in Fig. 2.10 [2.12], including trap-to-band tunneling (T-B), trap-to-trap tunneling (T-T), band-to-trap tunneling (B-T), thermal excitation (TE), and Poole-Frenkel emission (PF). These mechanisms can be classified into two categories according to their temperature dependence. During retention (there is internal self-built e-field), trapped electrons may lose via temperature-independent mechanisms: trapped electrons back-tunnel to the conduction band of Si-sub (T-B) or to the Si-SiO_2 interface traps (T-T), and Si-sub holes tunnel through the tunnel oxide and then be trapped in the nitride (B-T). On the other hand, the trapped electrons may also lose via temperature-dependent mechanisms. For example, trapped electrons may redistribute vertically inside the nitride by PF. At elevated temperatures, trapped electrons can also be thermally excited out of the nitride traps by (TE) and followed by tunneling to Si-sub or poly gate.

For older MNOS devices with a relatively thicker nitride layer (~100nm), since the trapped charges could easily redistribute inside nitride and then move toward the gate, PF was the dominant retention charge loss mechanism [2.13] in these devices. On the other hand, for recently scaled SONOS devices with a relatively thinner nitride layer (5 – 10nm), since the

charge redistribution is limited, the retention charge loss caused by PF can be ignored. Under different situations (different baking temperatures or different amount of storage charges), different retention charge loss mechanisms should be taken into account. Therefore, although there have been many reports [2.14-2.15] investigating the retention behaviors of SONOS devices, their results are not consistent.

For NORM devices, which are operated by CHE program and BBHH erase, both electrons and holes non-uniformly co-exist in the nitride layer. Therefore, in addition to vertical direction charge loss, the lateral charge migration should be taken into account. M. Janai et al [2.16] and A. Shapira et al [2.17] proposed that the retention charge loss of NROM devices mainly came from thermally activated lateral migration of trapped holes in the ONO layer. Moreover, saturation of the retention charge loss was demonstrated at the V_T levels well above the neutral states of the devices. Therefore, NROM devices have excellent retention behavior as compared with SONOS devices.

2.4 Trapped Charge Location Characterization

After understanding the basic equations, models, and carrier transport mechanisms, we will briefly introduce some studies on trapped charge locations of SONOS-type devices for both lateral and vertical directions. Since the trapped charge behaviors determine the characteristics of SONOS-type devices, a deep knowledge of trapped charge distribution is critical for program/erase bias optimization, reliability predictions, and future technology scaling.

2.4.1 Trapped Charge Lateral Location

Some SONOS-type devices use CHE injection for programming and BBHH injection for erase. In these devices, one of the important parameters is the lateral trapped charge profile, which must be determined accurately to predict the overlap of electron/hole profiles during

programming/erasing and the minimum possible gate length for 2-bit storage. Therefore, there have been many works studying the trapped charge lateral profile so far.

H. Pang et al [2.18-2.20] and L. Sun et al [2.21] proposed a new charge pumping (CP) method, which combines both CV_b method : constant V_b (the base level of the gate pulse) and CV_h method: constant V_h (the high level of the gate pulse) to obtain the more precise distribution of injected charges. The standard CP measurement setup is shown in Fig. 2.11(a) [2.22], where the pumping pulse is applied to gate, and the charge pumping current (I_{cp}) can be measured from drain or source side with source or drain floating. For the V_T profile of a CHE programmed charge trapping (CT) memory, as shown in Fig. 2.11(b), where four regions marked are consistent with the I_{cp} curves measured by CV_b and CV_h methods, as shown in Fig. 2.11(c) and (d), respectively. Since only the lower I_{cp} provides the more precise data, combining two methods could acquire the most complete and reliable trapped charge lateral profile. The extracted equations are shown below.

$$x = \frac{LI_{cp}(V_h)}{I_{cp,\max}} \tag{2-51}$$

$$N_{ntr} = \frac{1}{qfW}\frac{d\Delta I_{cp}}{dV_h}\frac{dV_h}{dx} \tag{2-52}$$

where f means the frequency of the pulse, W refers to the effective channel width, L is the channel length, and N_{ntr} is the trapped charge density in nitride. By replacing V_h with V_b, the above equations can be used in CV_h method to get the N_{ntr} curve. Using this new method, they studied the CHE program as well as the BBHH erase of SONOS devices. The program/erase charge profiles and the redistribution for different reliability issues were also discussed extensively. However, the I_{cp} is very sensitive to interface/near interface trapped charges, and this spurious I_{cp} cannot be easily eliminated, especially for the post-damaged devices. Therefore, other methods should be introduced to decompose the contribution of interface/ near interface trapped charges.

P. R. Nair et al [2.23] and P. B. Kumar et al [2.24] put non-uniform trapped charges (maximum near the gate edges, decreasing gradually towards the center of channel) in device simulators and simulated the linear I-V (LIV) and sub-threshold I-V (SIV) of SONOS devices, as shown in Fig. 2.12. They found that for the charges are placed on rectangular packets from the gate edge (Fig. 2.12), channel charges degrade V_T and S.S. (sub-threshold slope) while overlap charges degrade the linear slope of I_D-V_G curves, but do not affect SS significantly. Compared with CP measurement and Monte Carlo simulation, they announced that they could accurately determine the trapped charges in gate/drain overlap and channel (near the drain junction). Nevertheless, their method needs complex device simulation, where the detailed device structure and doping profile should be given. Moreover, the I-V curve is very sensitive to the device geometry such as STI effect. Therefore, the geometry effect should be taken into account.

L. Avital et al [2.25] and A. Padovani et al [2.26] also utilized similar method to investigate the temperature effects on I_D-V_G curves as well as the hole injection for erase. However, their method suffers from the same issues as previous method sine they also needed to simulate the I_D-V_G curves.

2.4.2 Trapped Charge Vertical Location

For the SONOS-type devices which are operated by uniform charge injection, the trapped charge vertical location is more meaningful than lateral location. For example, the NAND Flash, which is the main memory product of the market today, uses uniform FN program and erase. Therefore, there have been a large number of papers investigating the trapped charge vertical location.

E. Suzuki et al [2.27] compared the maximum flat-band voltage shifts (ΔV_{FBmax}), which is extracted from CV hysteresis measurement, of various MONOS (metal-oxide-nitride-oxide-semiconductor) capacitors with different fractions of nitride conversion (γ). From the

relationship between ΔV_{FBmax} and trap density, they could further extract the trap density.

$$\Delta V_{FB\max} = \frac{qN_t}{2\varepsilon_N} T_N^2((1-\gamma)^2 + 2\alpha\beta\gamma(1-\gamma) + \frac{2\alpha\beta\gamma N_{on}}{T_N N_t}) \quad (2\text{-}53)$$

where the T_N is the initial nitride thickness, α is the volume ratio of oxide to nitride, β is the ratio of dielectric constant of nitride to oxide, γ is the fraction of the nitride converted by oxidation, N_t is the trap density which is assumed to be uniformly distributed in the nitride layer, and N_{on} is the trap density which is assumed to be created at the T.O./nitride interface. By comparing the theoretical calculation with the experimental results for different T_N, as shown in Fig. 2.13, they concluded that the electrons are mainly trapped at the T.O./nitride interface, and the number of traps is insensitive to T_N while the bulk trap density could be almost ignored. In this method, the trap density of various MONOS capacitors is assumed to be the same. However, the ΔV_{FBmax} of a capacitor is also a function of applied voltage, thus these results may be equivocal. Moreover, they used MNOS sample to extract the bulk trap density. However, since the MNOS devices do not have T.O. to block the external charge injection, in these devices the gate injection is considerable. That would cause underestimated bulk trap density and wrong results.

T. Ishida et al [2.28] also compared the saturated flat-band voltage shifts (ΔV_{sat}) of various MONOS capacitors. They used a special avalanche charge injection [2.29] to inject the electrons, therefore, in their devices the impurity concentration of Si-sub should be controlled by ion implantation to the order of $10^{17}cm^{-3}$. They assumed three trap regions in the MONOS structure: (1) N_{top}: at the T.O./nitride interface (top interface), (2) $N_{SiNbulk}$: in the bulk nitride, and (3) N_{bottom}: at the nitride/B.O. interface (bottom interface), as shown in Fig. 2.14(a). They also assumed that trap distributions in these three regions were uniform. Under these assumptions, the ΔV_{sat} can be expressed as

$$\Delta V_{sat} = (\frac{qN_{top}}{\varepsilon_{ox}\varepsilon_0} x_{top}) + \frac{q}{\varepsilon_N\varepsilon_0}\int_0^{x_{SiN}} xN_{SiNbulk}(x)dx + \frac{qx_{top}}{\varepsilon_{ox}\varepsilon_0}\int_0^{x_{SiN}} N_{SiNbulk}(x)dx + (\frac{x_{SiN}}{\varepsilon_N\varepsilon_0} + \frac{x_{top}}{\varepsilon_{ox}\varepsilon_0})qN_{bottom}$$

$$= \frac{qN_{SiNbulk}}{2\varepsilon_N\varepsilon_0} x_{SiN}^2 + (\frac{qx_{top}N_{SiNbulk}}{\varepsilon_{ox}\varepsilon_0} + \frac{qN_{bottom}}{\varepsilon_N\varepsilon_0})x_{SiN} + \frac{qx_{top}N_{top}}{\varepsilon_{ox}\varepsilon_0} + \frac{qx_{top}N_{bottom}}{\varepsilon_{ox}\varepsilon_0} \quad (2\text{-}54)$$

However, in Eq. (2-54) there are three variables needed to be solved. In order to diminish the fitting error, three parameters are estimated in two steps. First, they estimated $N_{SiNbulk}$ and N_{bottom} by using MNOS capacitors. In these devices, x_{SiN} is varied by substituting zero for N_{top} and x_{top} in Eq. (2-54).

$$\Delta V_{sat} = \frac{qN_{SiNbulk}}{2\varepsilon_N\varepsilon_0} x_{SiN}^2 + \frac{qN_{bottom}}{\varepsilon_N\varepsilon_0} x_{SiN} \quad (2\text{-}55)$$

Second, they took the results of MNOS capacitors into consideration to analyze the MONOS capacitors and to estimate the N_{top}. By comparison of MNOS and MONOS capacitors with various film stacks, as shown in Fig. 2.14(b) and (c), they also concluded that the electrons are mostly trapped at the interfaces of nitride and oxide while bulk electron traps are negligible. However, this method suffers from the same issues as previous method. Moreover, the fitting of experimental data is artificial, and the results obtained under a special operation may not be practical.

The above two methods only gave an estimation of saturated trap density but not the trapped charges under practical operations. The limitation of above techniques originates from the difficulty of finding both the total trapped charge density (Q) and the mean vertical location (x) using only one equation. Therefore, another equation must be added to solve for both variables.

M. H. White et al [2.30-2.32] proposed a linear voltage ramp technique, which simultaneously measured the flat band voltage shifts (ΔV_{FB}) and the injected charges at different terminals. The measurement system is illustrated in Fig. 2.15, where the linear voltage ramp with a symmetrical triangular form is applied to gate, and the source/bulk currents are measured by electrometers, and are recorded simultaneously as a function of gate voltage. Based on the measured currents (shown in Fig. 2.16) and ΔV_{FB}, the charge centroid can be further extracted from the slope of ΔQ_N vs. ΔV_{FB} curves.

$$\Delta V_{FB} = -\Delta Q_N [T_{TOX} / \varepsilon_{OX} + (T_N - x) / \varepsilon_N] \quad (2\text{-}56)$$

where ΔQ_N is the charge per unit area in the nitride, x is the charge centroid measured from the B.O./nitride interface. They concluded that for SONOS/MONOS devices the charge centroid is deep into the nitride layer at lower injection levels and then moves toward the center of nitride as the injection level is increased.

A. Arreghini et al [2.33-2.34] also proposed a method to directly measure the injection current during DT programming/erasing for a capacitor. For a SONOS device shown in Fig. 2.17(a), where x_C denotes the centroid of the trapped charges measured from the T.O./nitride interface, the threshold-voltage shift (ΔV_T) caused by the charge Q_N (uniformly injected over the device with an area = A) can be calculated as

$$\Delta V_T = -\frac{Q_N}{A}\cdot\frac{t_{TOP}}{\varepsilon_{ox}} - \frac{1}{\varepsilon_N}\int_0^{t_N} x\cdot q(x)dx = -\frac{Q_N}{A}\left(\frac{t_{TOP}}{\varepsilon_{ox}} + \frac{x_C}{\varepsilon_N}\right) \quad (2\text{-}57)$$

where q(x) is the charge density along the nitride depth x, and t_{TOP} and t_N are the T.O. and nitride thickness, respectively. Therefore, if ΔV_T and Q_N are known, the x_C can be determined by

$$x_C = -\varepsilon_N\left(\frac{\Delta V_T \cdot A}{Q_N} + \frac{t_{TOP}}{\varepsilon_{ox}}\right) \quad (2\text{-}58)$$

Hence, in order to determine x_C by using Eq. (2-58), they developed a well-controlled experimental setup to directly measure Q_N and the corresponding $\Delta V_T = (V_{Tfinal} - V_{Tinitial})$, as shown in Fig. 2.17(a). Since the electrons can be detected at source/drain terminals, and the holes can be detected at bulk termial, carrier-separation technique can be well performed. On the other hand, in order to eliminate the displacement currents from the overall current integration, an accurate Q_N measurement with three-level shapes (Fig. 2.17(b)) should be required. Therefore, a complex setup should be needed. They found that the charge centroid is located at the center of nitride, and it is quite insensitive to the program/erase conditions and the gate-stack compositions.

In this method, they also assumed that the injection current is fully captured by SONOS

devices, but it is not practical. Moreover, the x_C in Eq. (2.58) is proportional to $1/Q_N$, therefore, the small error Q_N in will result in incorrect x_C. Moreover, the injection current during DT programming/erasing is a fast transient response (~ μsec), which is difficult to measure accurately. On the other hand, this method cannot be applied to the long-term retention test because the de-trapping current is too small for detecting. These limitations greatly affect the accuracy of this method.

H. T. Lue et al [2.35] proposed a simple transient analysis method to characterize the trap vertical location. This method required only measuring the time dependence of gate injection at various gate voltages on "single" sample. Then, the transient current (J) and the instantaneous T.O. e-field (E_{Tox}) can be directly obtained based on various cases of trap location. Comparisons can be made to check which case has the best consistency for the J vs. E_{Tox} behaviors. The only assumption in this method is that the J vs. E_{Tox} should follow a consistent tunneling relationship at different gate voltages. The experimental results showed unequivocally that electrons are trapped at the interface between T.O. and nitride for oxide grown by thermal conversion, as shown in Fig. 2.18(a). However, for the direct-deposited T.O. (HTO) the electrons are close to the center of nitride, as illustrated in Fig. 2.18(b). Although this method is a simple and convincing tool to detect the nitride trap vertical location, it is only suitable for gate-injection operated SONOS-type devices. That is because for the channel-injection operated SONOS-type devices the B.O. e-field (E_{Box}) is independent of the trapped vertical location. Therefore, comparing different vertical location assumptions becomes invalid.

In this dissertation, we proposed an accurate and unequivocal way to solve the above difficulties. We introduced an additional gate-sensing (GS) capacitor to be compared with the conventional channel-sensing (CS) one. This GSCS method provides two equations to solve total trapped charge density (Q) and mean vertical location (x) simultaneously. Only simple CV measurement is required, and there is no complicated setup or noise compensation.

Moreover, we also provided an effectively “real-time” measurement method since Q and x can be tracked directly during programming/erasing and retention testing. Both channel-injection and gate-injection operated SONOS-type devices can be investigated successfully. In the next chapters, we will discuss this GSCS method in detail.

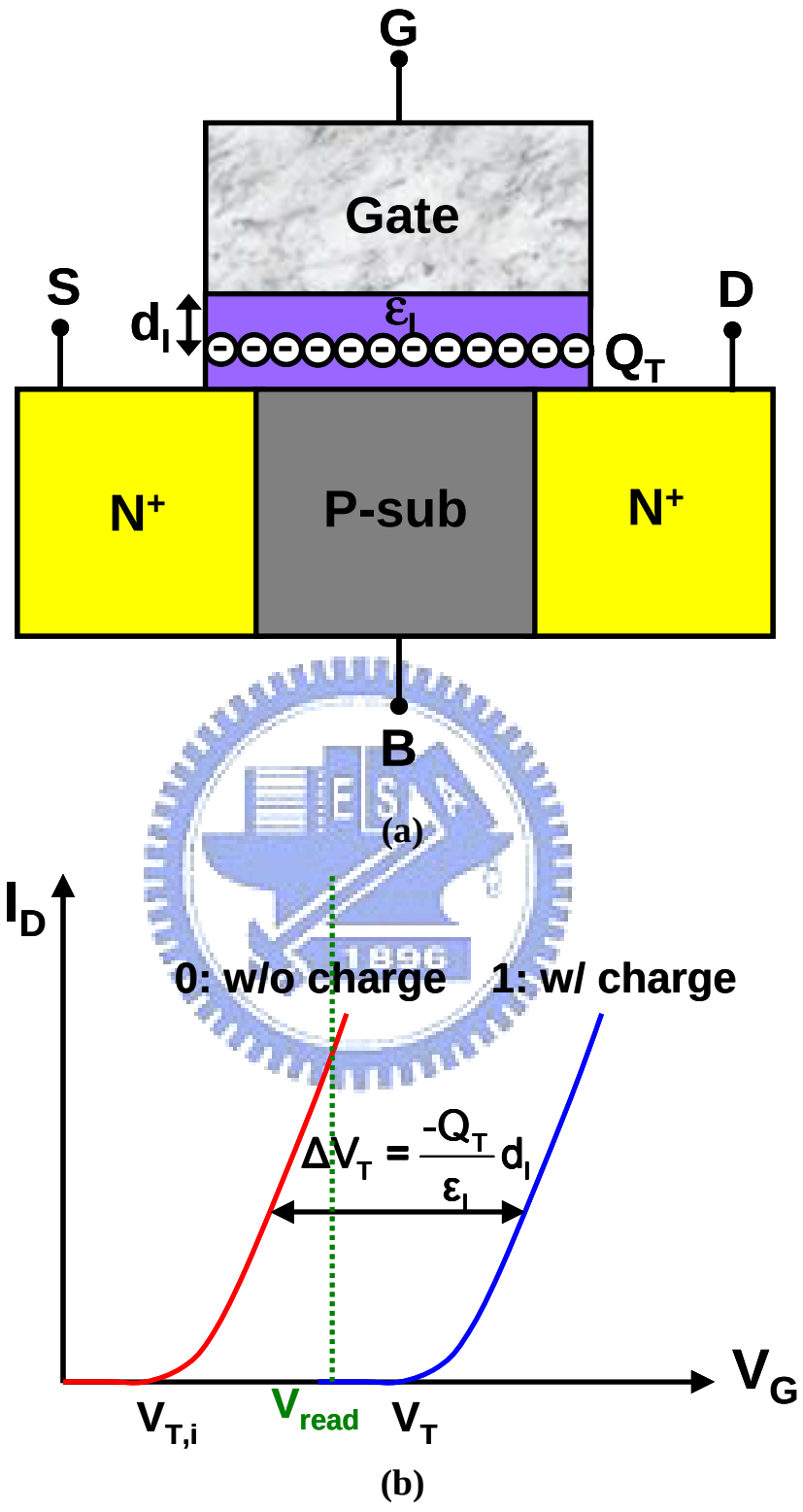


Fig. 2.1 (a) Storage principle of non-volatile memory devices can be simplified as the charges (Q_T) are trapped in the gate insulator of a MOSFET. (b) Influence of trapped charges in the gate insulator on the threshold voltage (V_T) shift of a MOSFET.

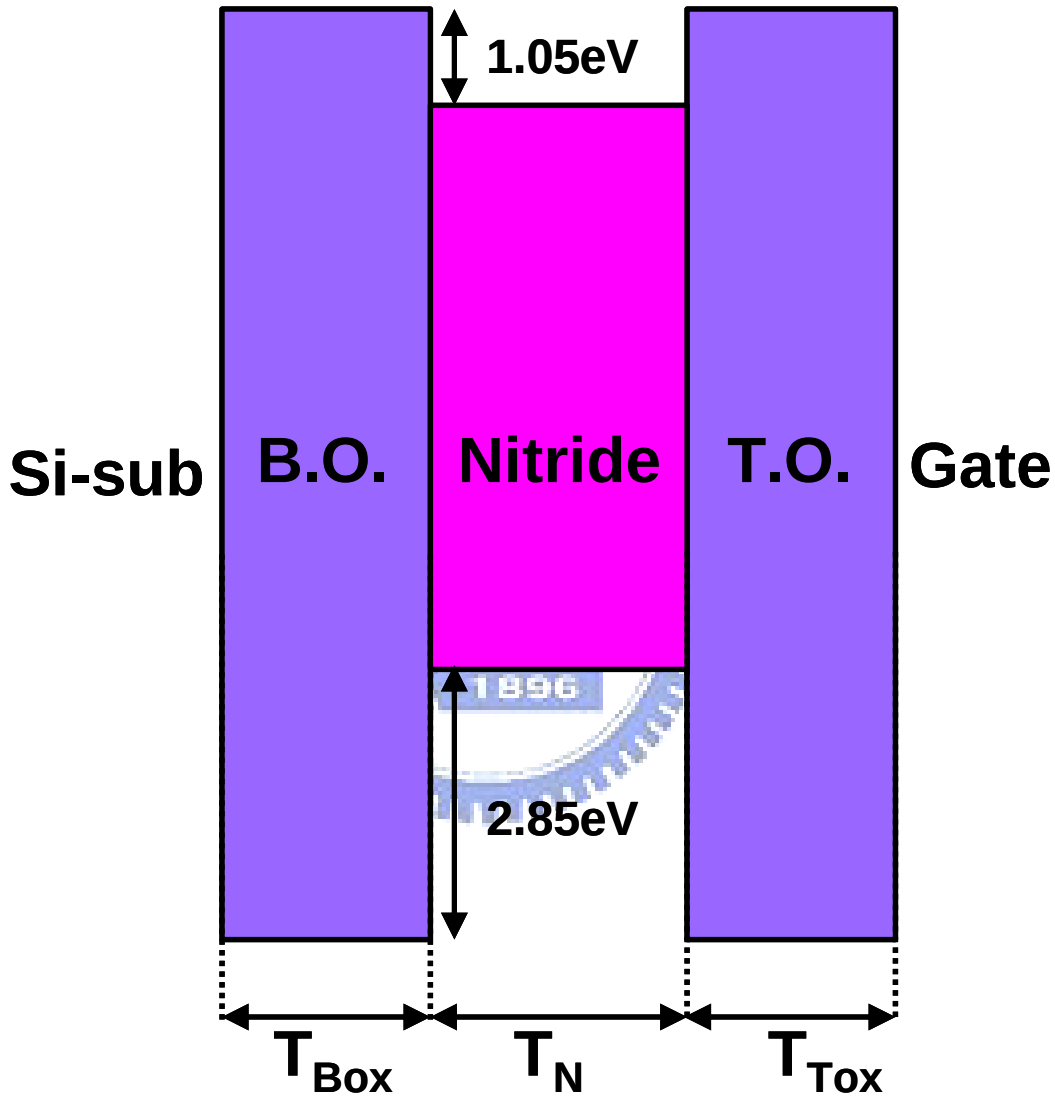


Fig. 2.2 ONO energy band diagram of SONOS memory under zero bias.

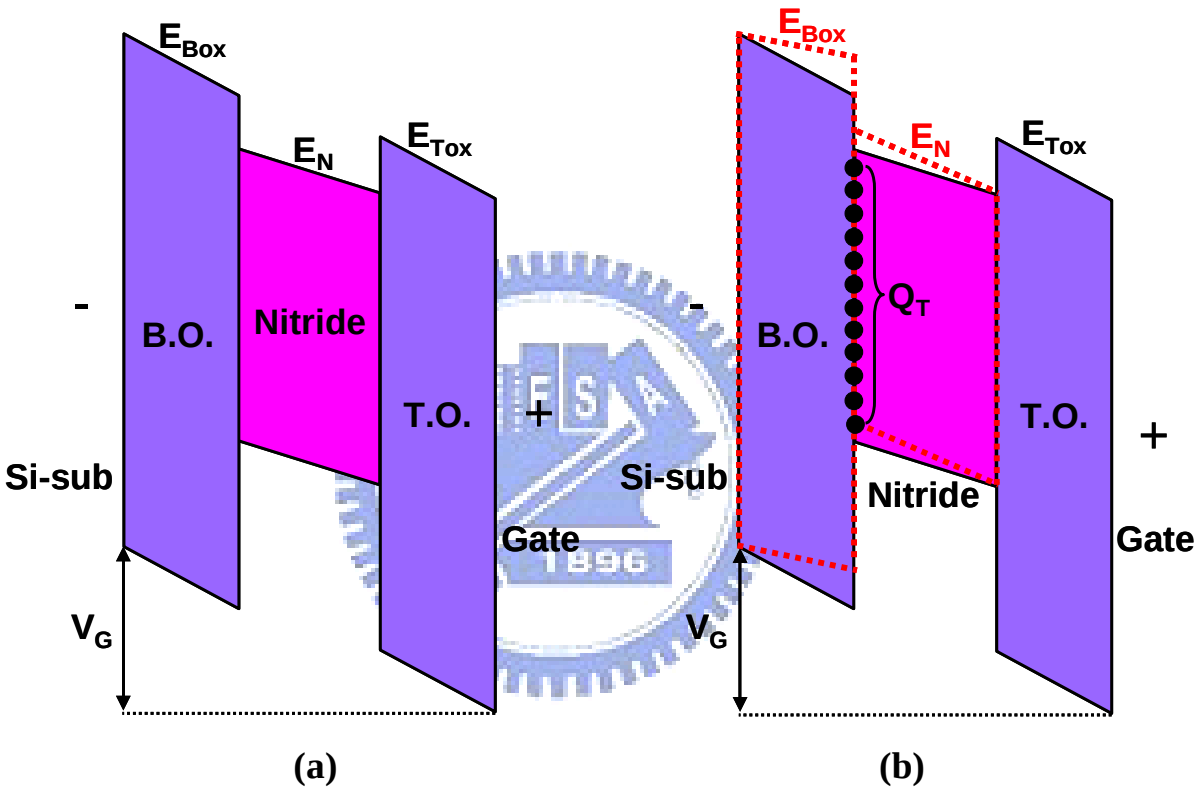


Fig. 2.3 (a) ONO energy band diagram of SONOS memory under positive gate bias. (b) The trapped electrons at nitride/B.O. interface will cause decreased E_{Box} but increased E_N.

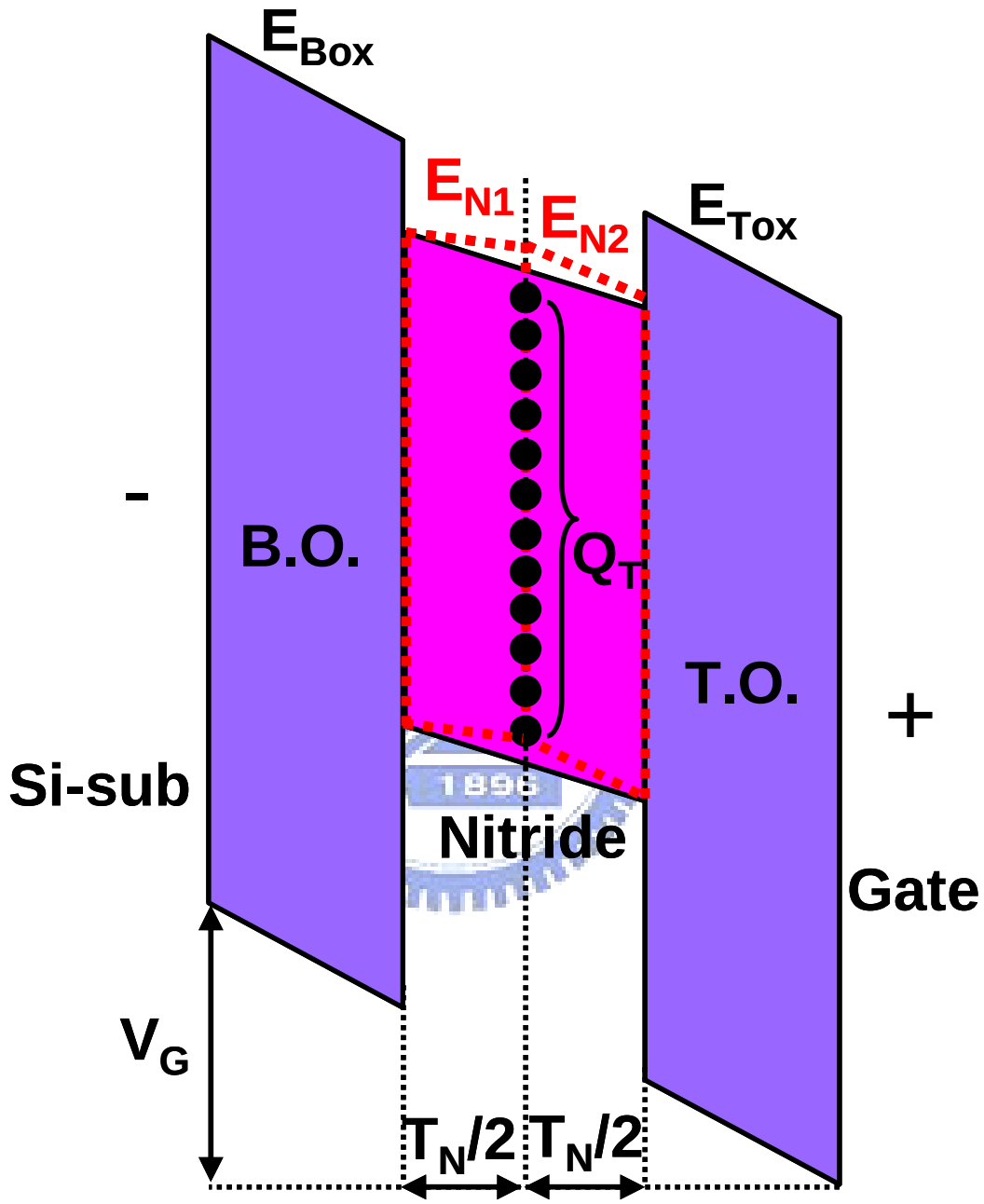


Fig. 2.4 ONO energy band diagram of SONOS memory for the trapped electrons at the center of nitride. The nitride is divided into two equal parts. The bottom nitride e-field is E_{N1} while the top nitride e-field is E_{N2}.

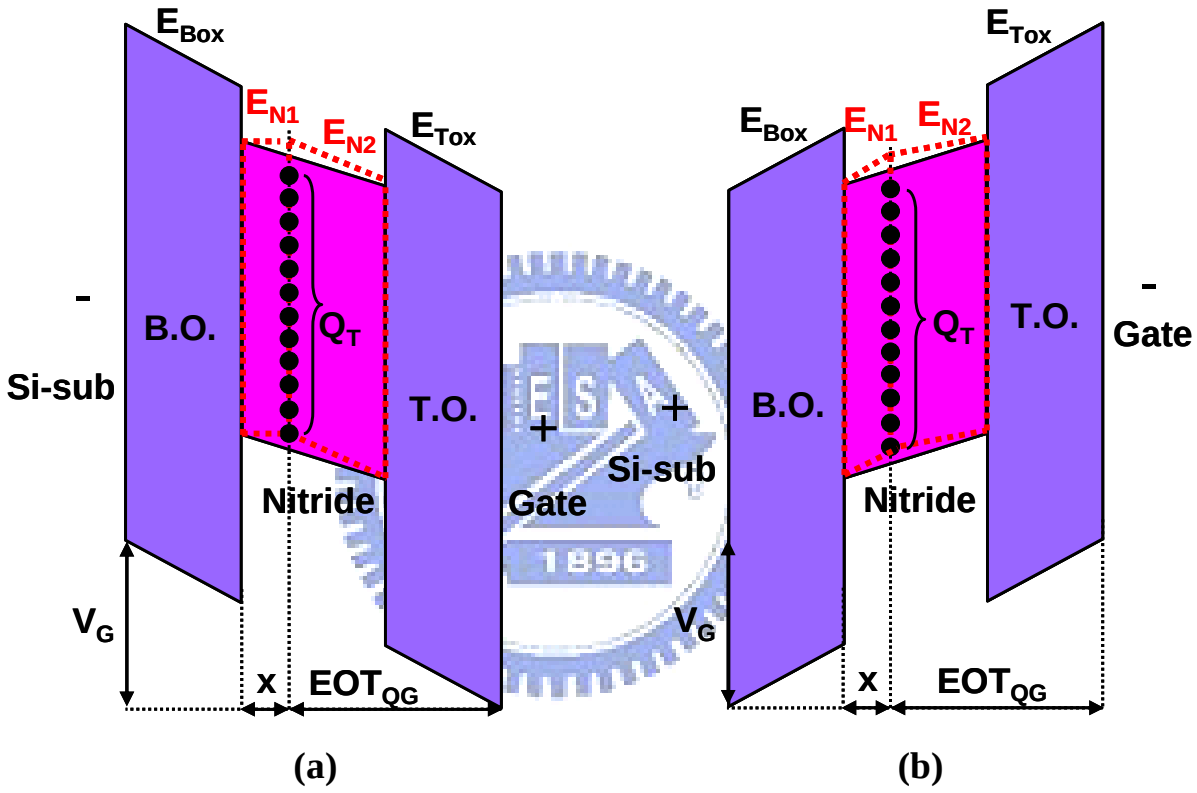


Fig. 2.5 ONO energy band diagram of SONOS memory under (a) positive gate bias, and (b) negative gate bias for the general case: the trapped charges locate at x from B.O./nitride interface.

E-field / Bias	E_{Box}	E_{Tox}	E_{N1}	E_{N2}
$+V_G$	$\frac{V_G - \Delta V_T}{EOT}$	$\frac{V_G - \Delta V_T}{EOT} + \frac{\Delta V_T}{EOT_{QG}}$	$\frac{\varepsilon_{ox}}{\varepsilon_N} E_{Box}$	$\frac{\varepsilon_{ox}}{\varepsilon_N} E_{Tox}$
$-V_G$	$\frac{\lvert V_G \rvert + \Delta V_T}{EOT}$	$\frac{\lvert V_G \rvert + \Delta V_T}{EOT} - \frac{\Delta V_T}{EOT_{QG}}$		

Table 2.1 E-fields of ONO films under both positive and negative gate biases for arbitrary charge location.

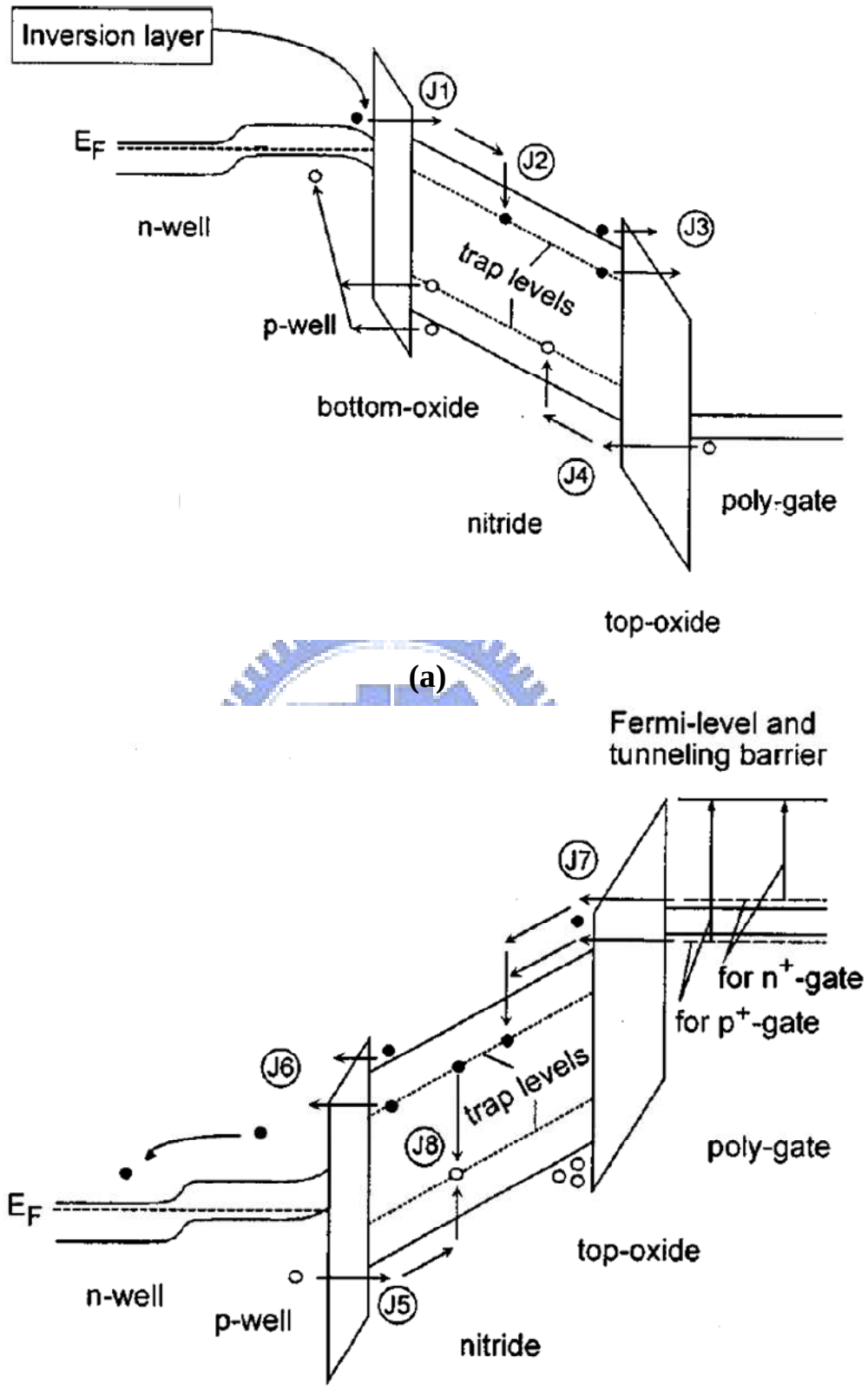


Fig. 2.6 Energy band diagrams of SONOS-type devices under (a) positive and (b) negative gate biases. The main conduction mechanisms are also indicated. Solid circles represent electrons, and hollow circles represent holes [2.5].

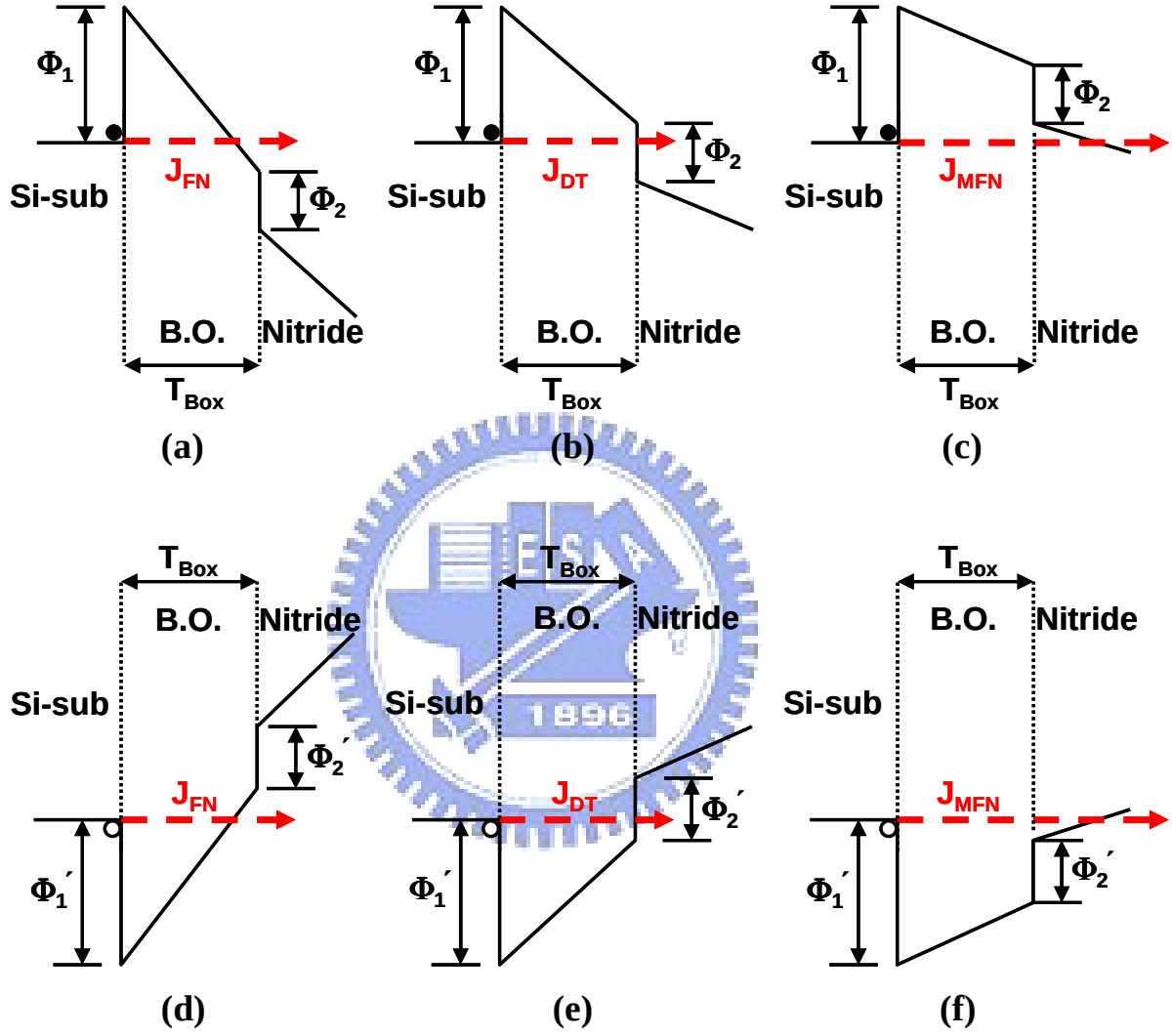


Fig. 2.7 Energy band of diagrams of (a-c) electron injection and (d-f) hole injeciotn from Si-sub to nitride under various gate biases. (a,d) Fowler–Nordheim (FN) tunneling. (b,e) Direct tunneling (DT). (c,f) Modified Fowler–Nordheim (MFN) tunneling. Φ_1 and Φ_2 are the oxide and nitride barrier heights for electron, respectively. Φ_1' and Φ_2' are the oxide and nitride barrier heights for hole, respectively.

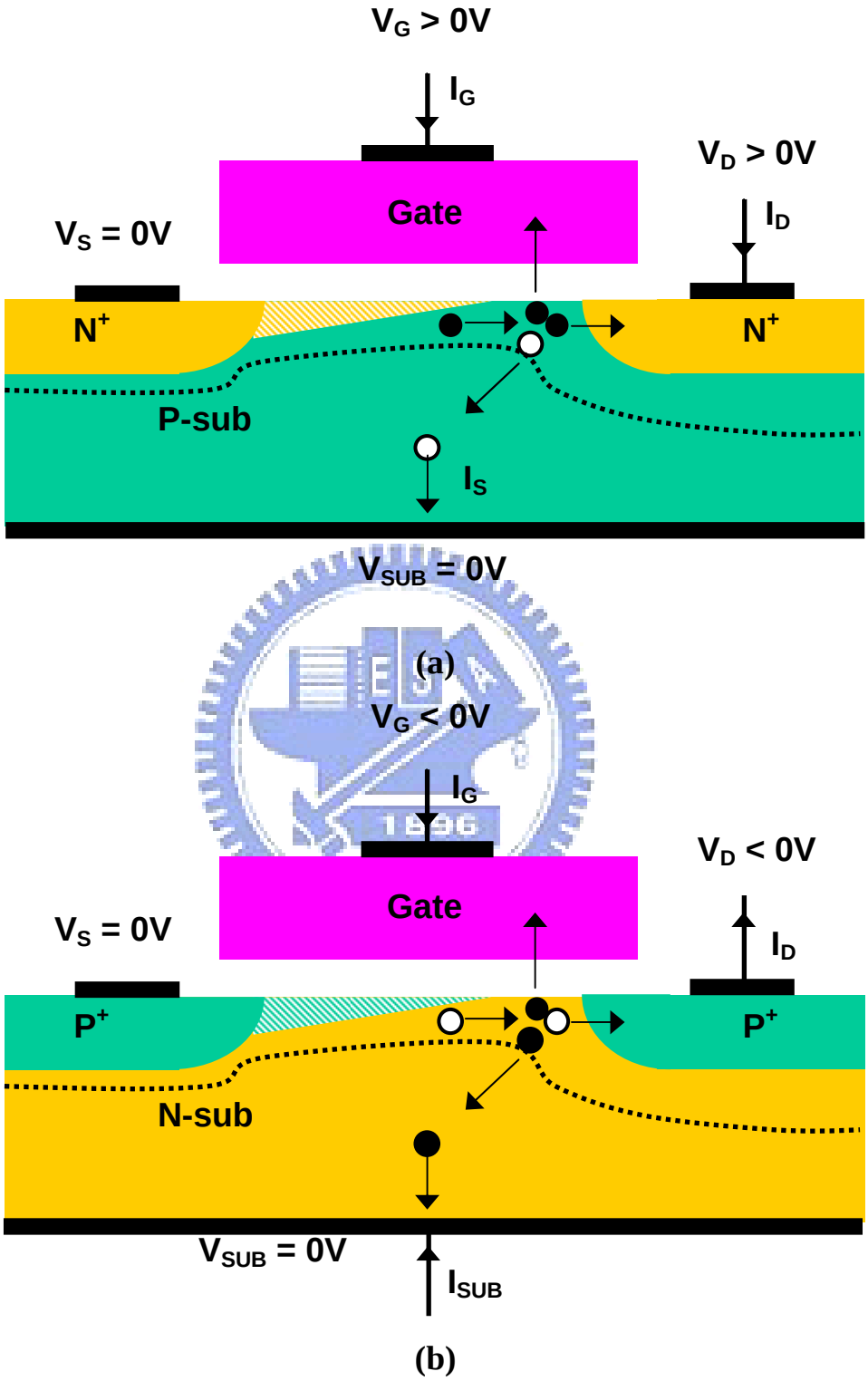


Fig. 2.8 Schematic diagrams of CHEI in (a) NMOSFET and (b) PMOSFET [2.7].

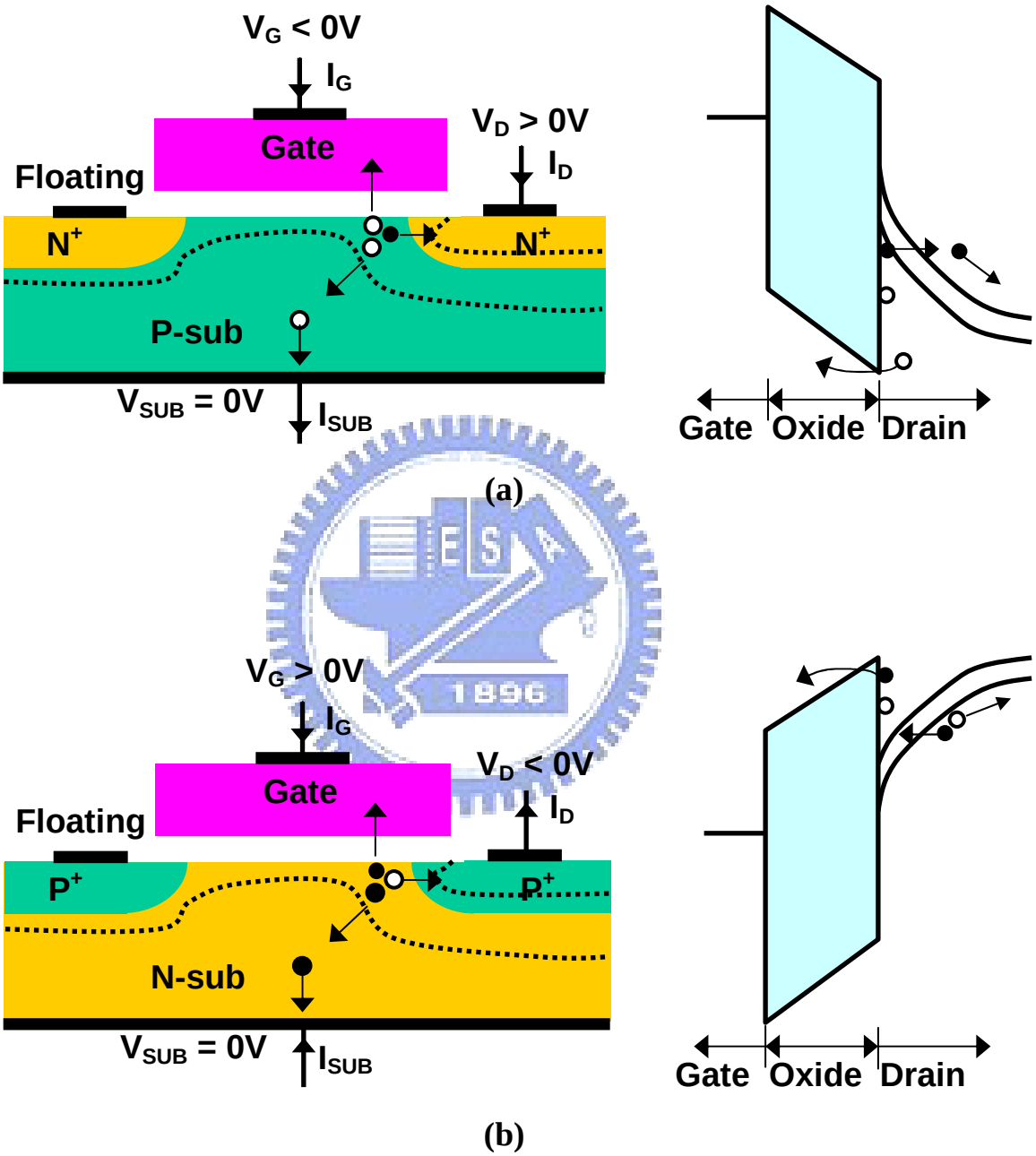


Fig. 2.9 Schematic diagrams of BBHC injection in (a) NMOSFET and (b) PMOSFET [2.7].

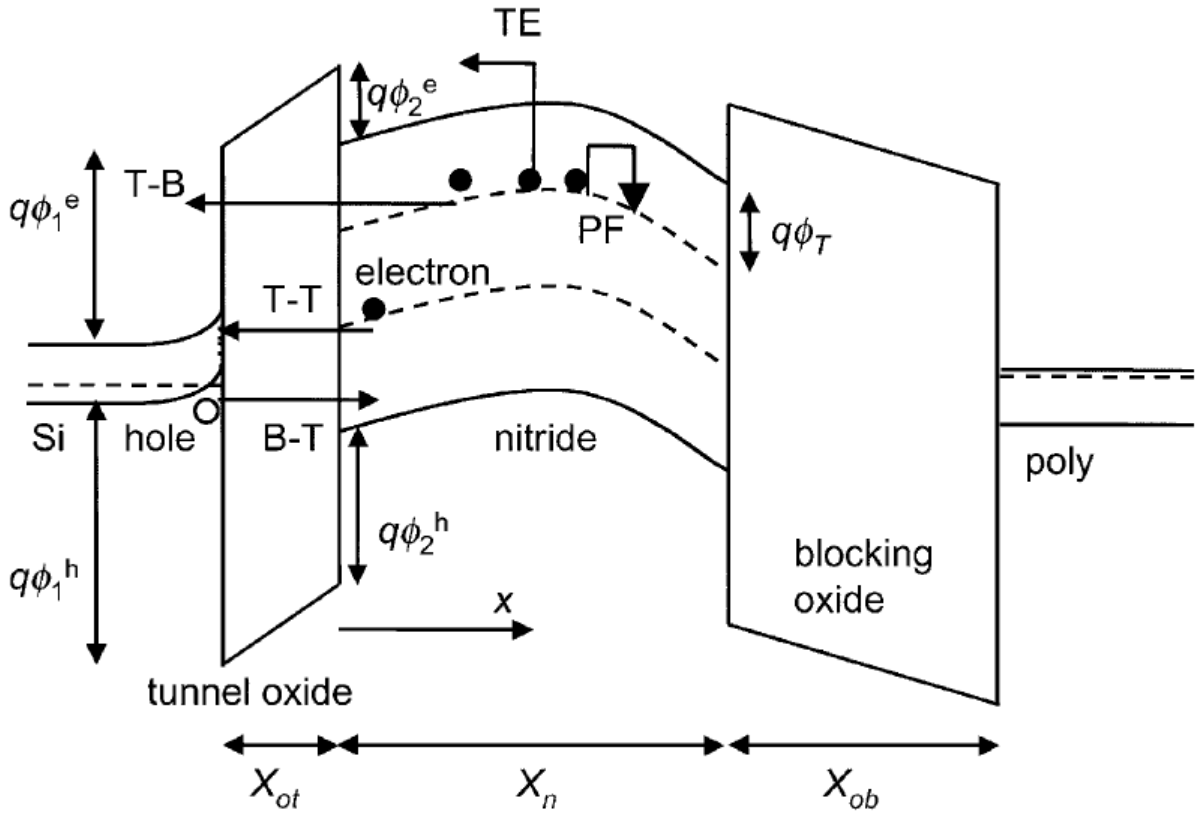


Fig. 2.10 Schematic diagram of retention charge loss mechanisms of SONOS devices: trap-to-band tunneling (TB), trap-to-trap tunneling (T-T), band-to-trap tunneling (B-T), thermal excitation (TE) and Poole-Frenkel emission (PF) [2.12].

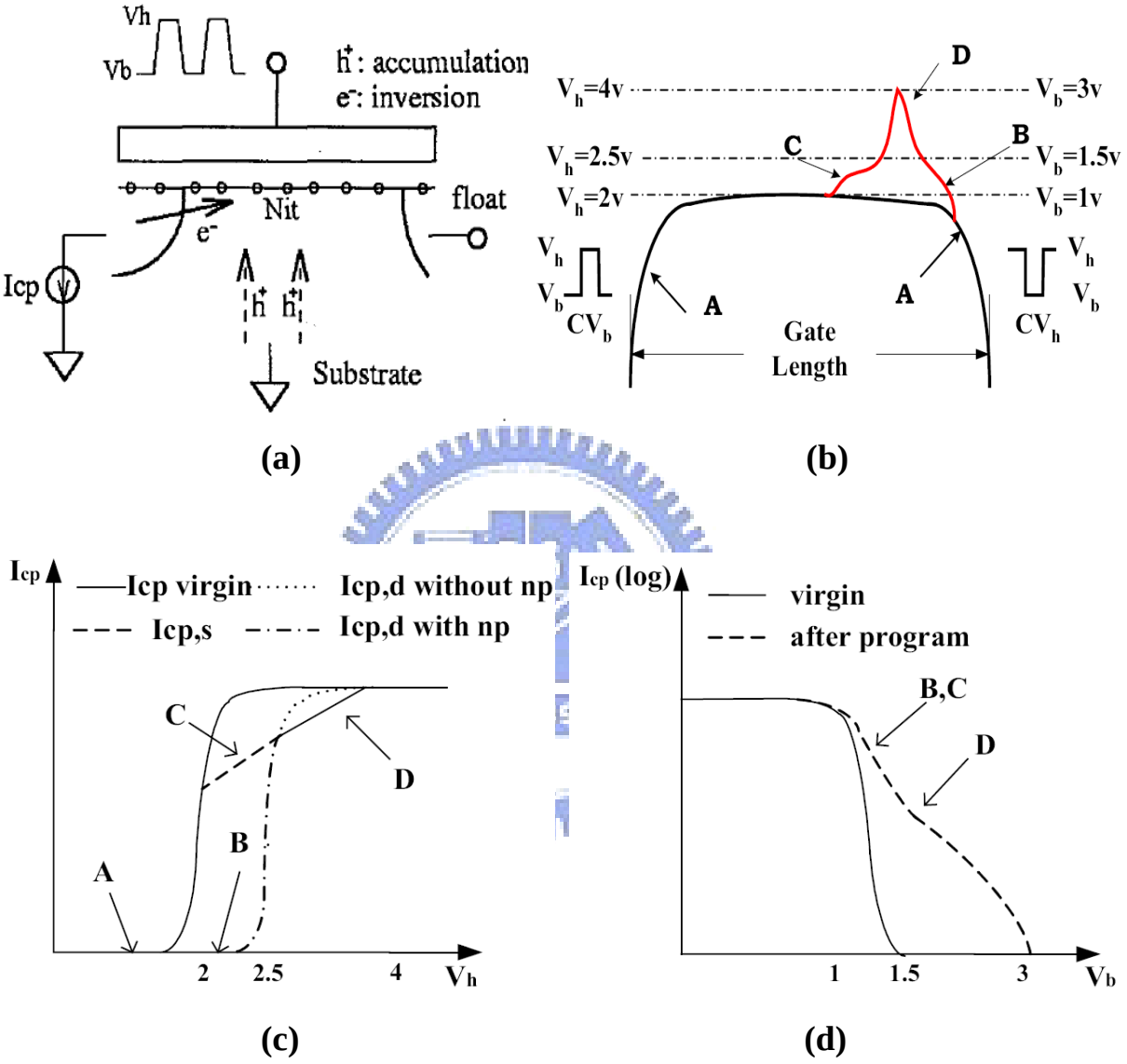


Fig. 2.11 (a) Standard charge pumping (CP) measurement setup. (b) V_T profile in a CHE programmed charge trapping memory. (c) and (d) are measured I_{cp} curves vs. V_h and V_b before and after CHE program using CV_b and CV_h, respectively [2.22].

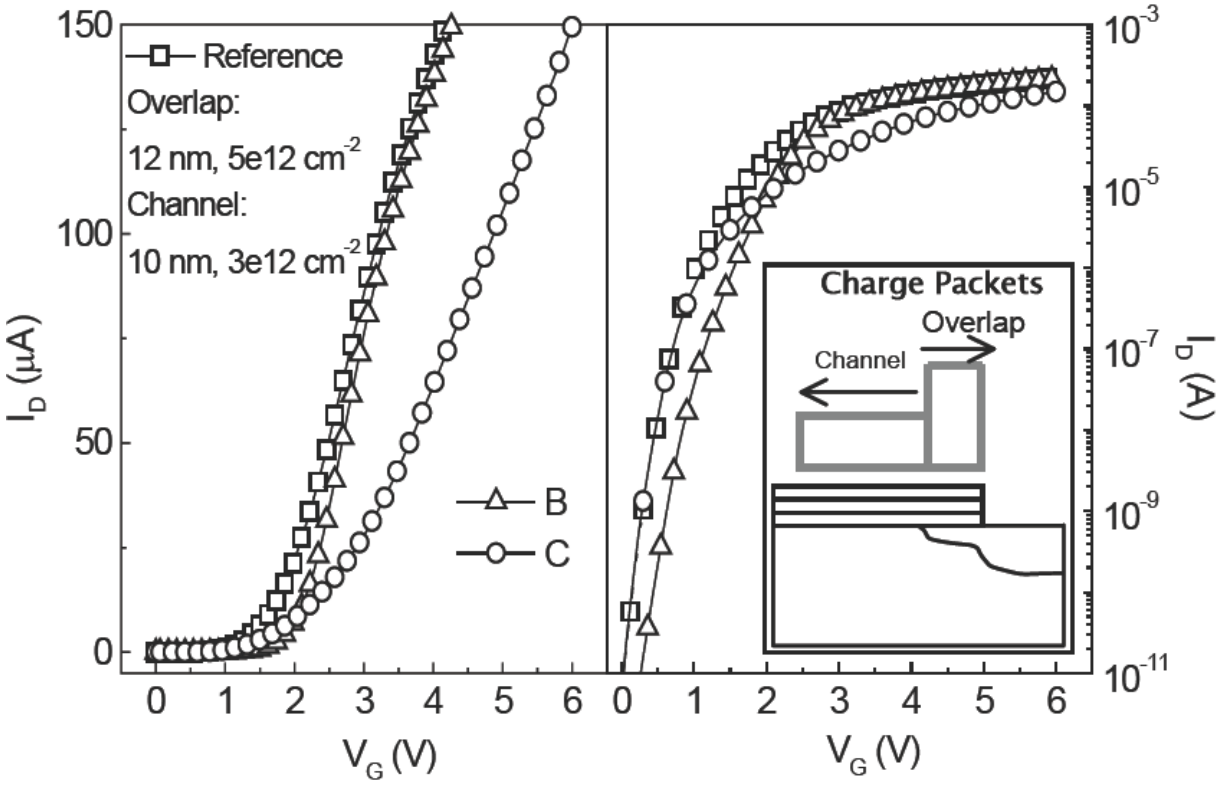


Fig. 2.12 Simulated I_D-V_G with different amount of charge placed in rectangular packets. Increasing channel charge spread (curve B) affects S.S. and V_T. Increasing overlap charge magnitude (curve C) degrades linear slope and V_T but does not affect S.S [2.23].

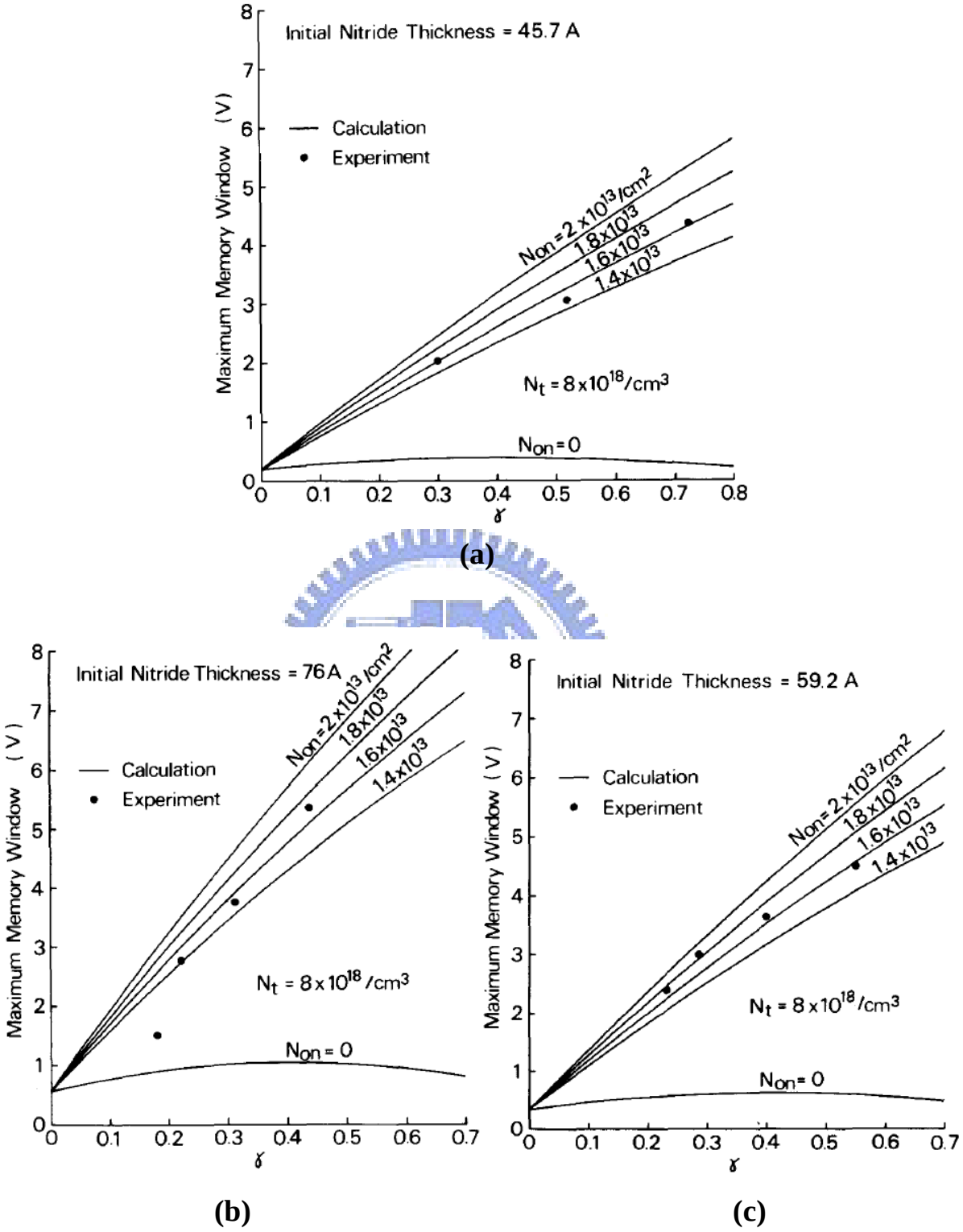


Fig. 2.13 Maximum memory window ΔV_{FBmax} as a function of γ. γ means the fraction of the nitride converted by oxidation. Initial nitride thickness is (a) 45.7Å, (b) 76Å, and (c) 59.2Å [2.27].

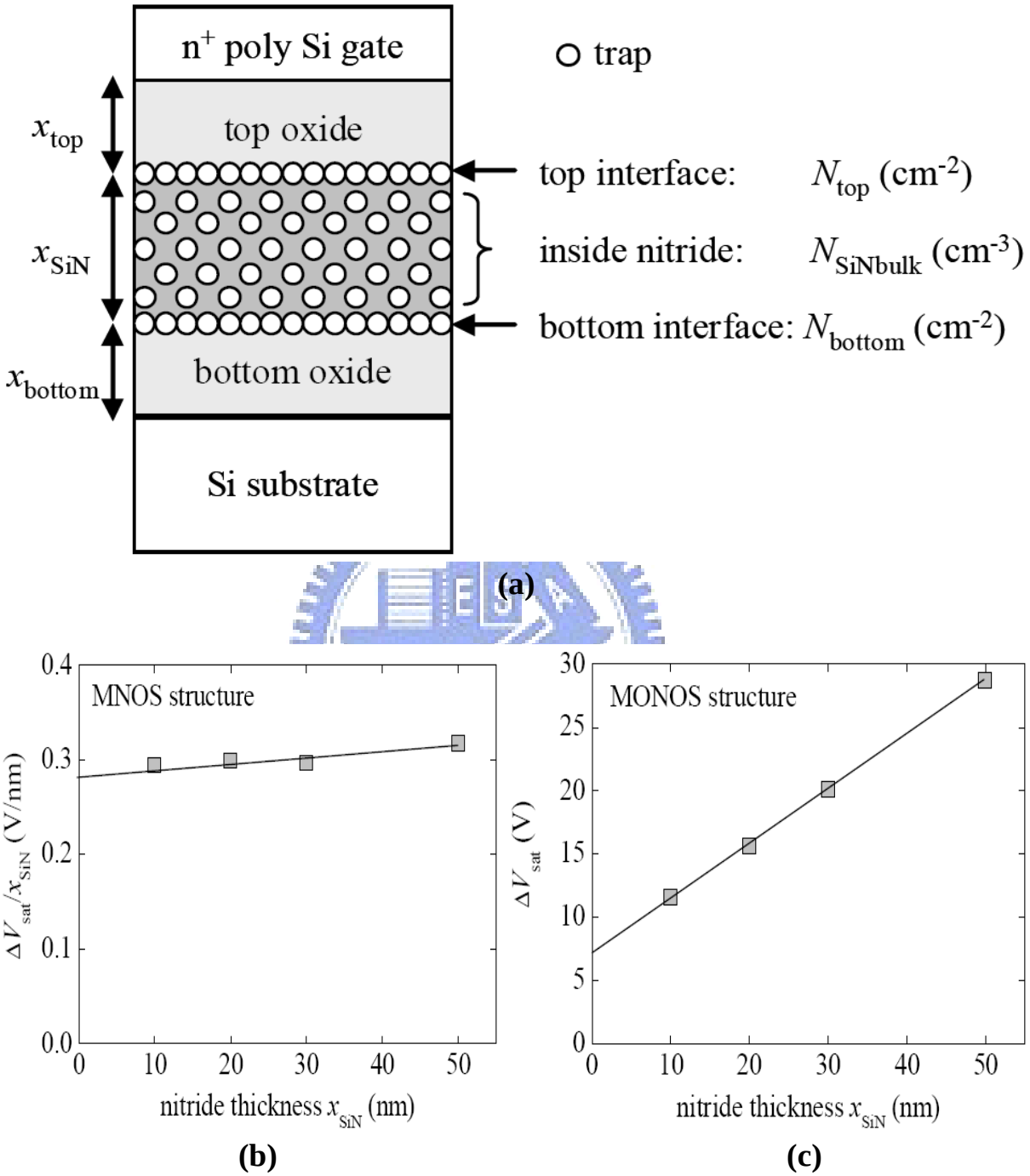


Fig. 2.14 (a) Three trap sites in the MONOS structure. The trap distributions in these three regions were uniform. Analytical results of electron trap density in (b) MNOS and (c) MONOS structures [2.28].

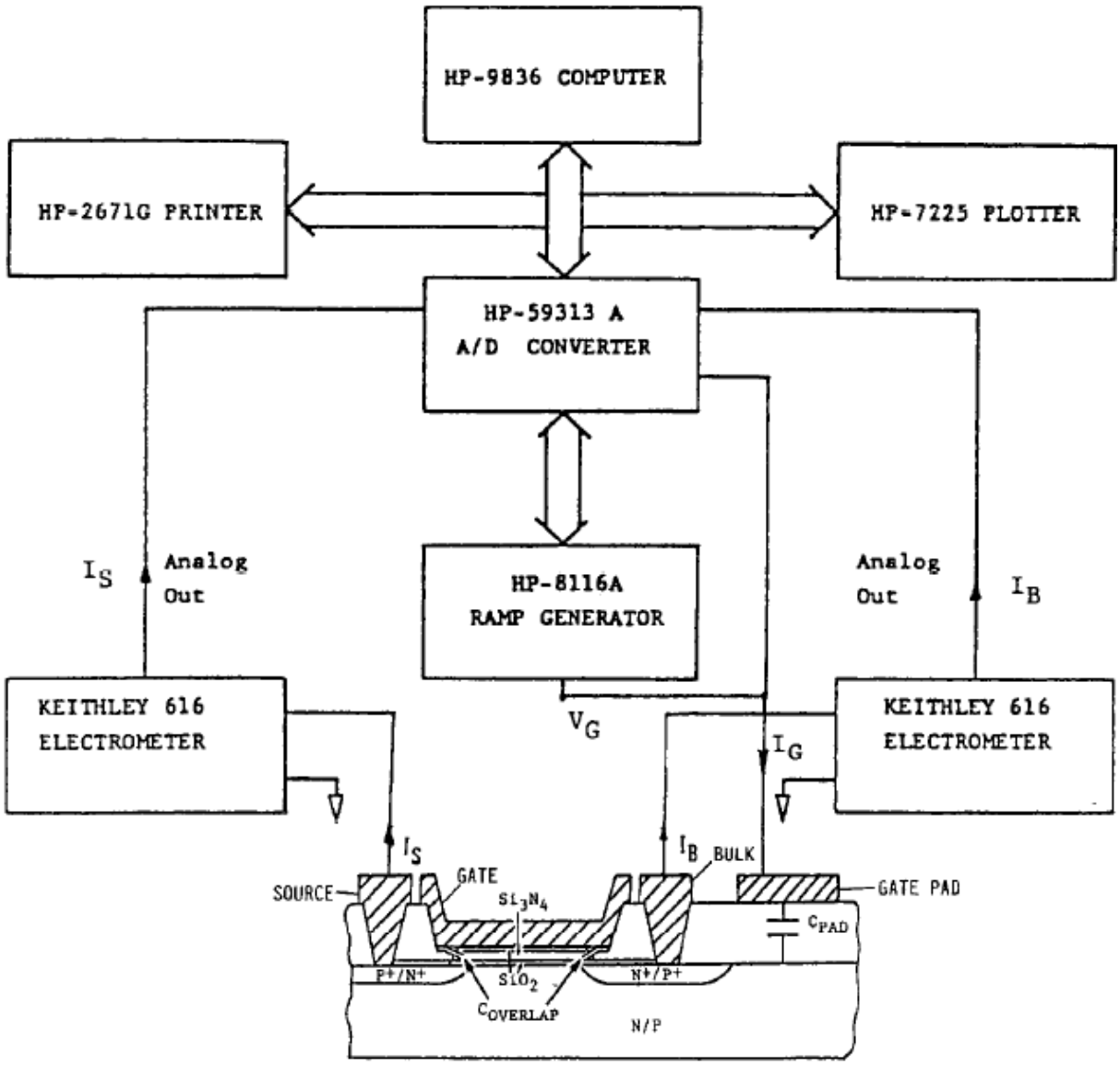


Fig. 2.15 A block diagram of the automated data-acquisition system for the linear voltage ramp technique with charge separation [2.31].

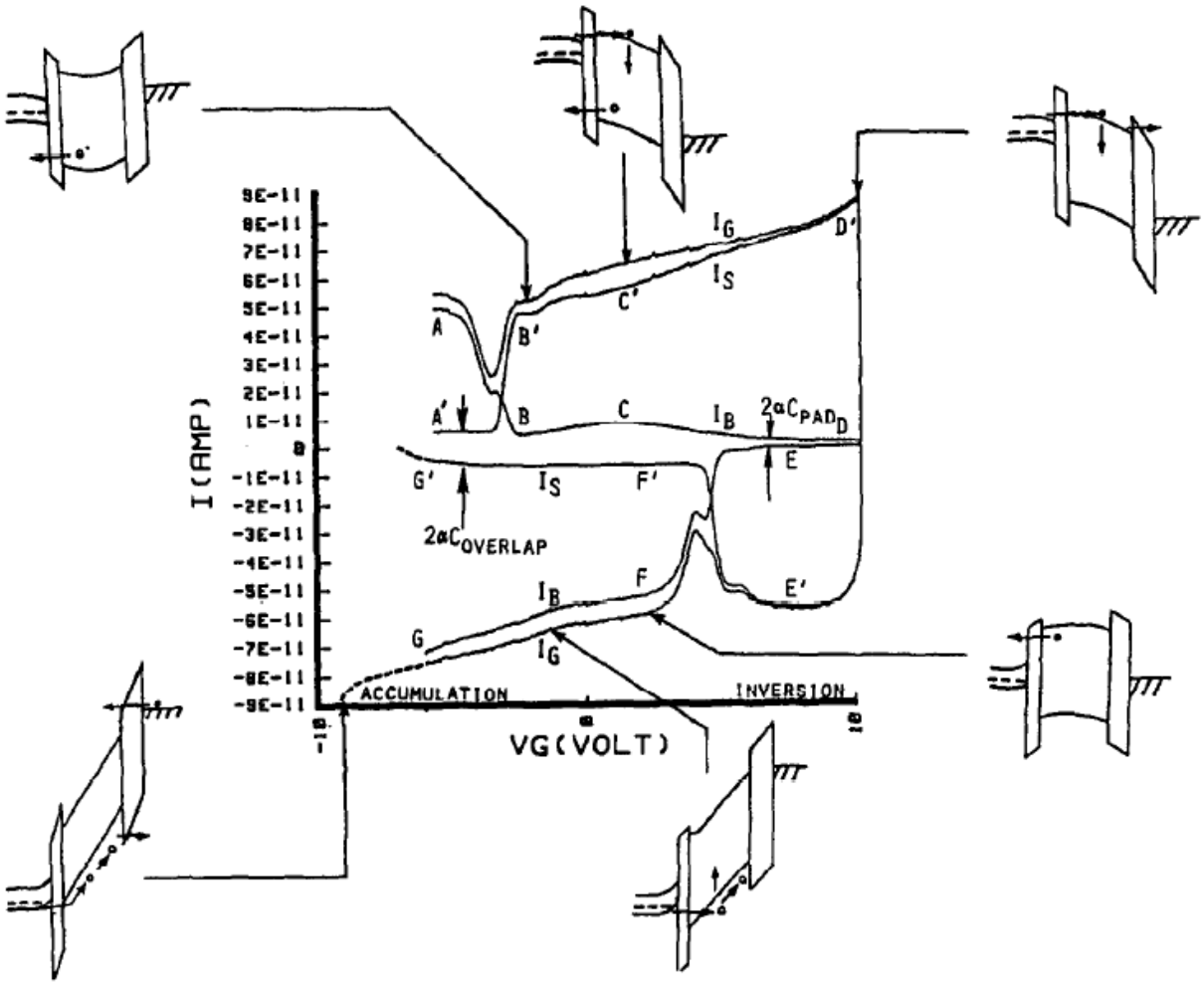


Fig. 2.16 Energy band diagrams and the corresponding currents at various points in the voltage sweep on a MONOS transistor [2.31].

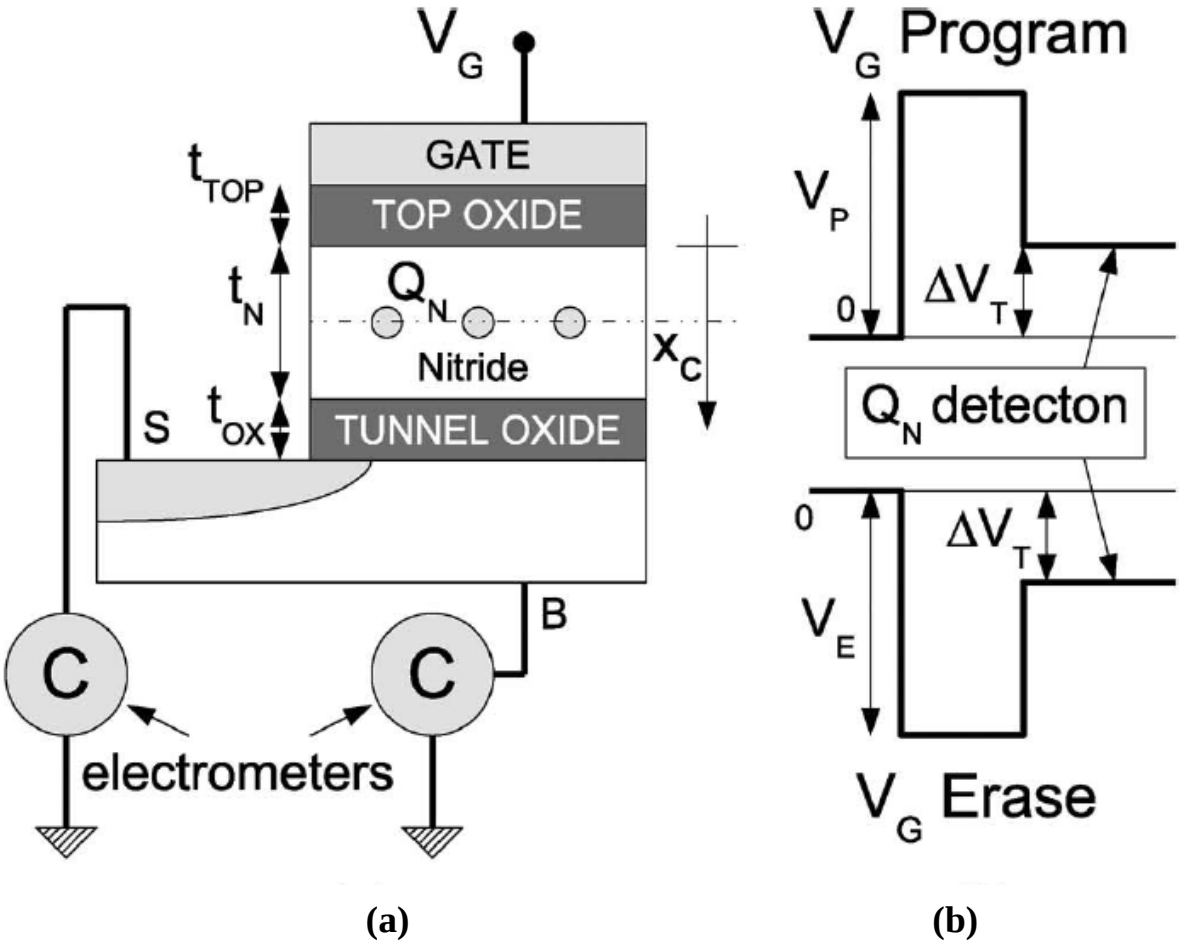
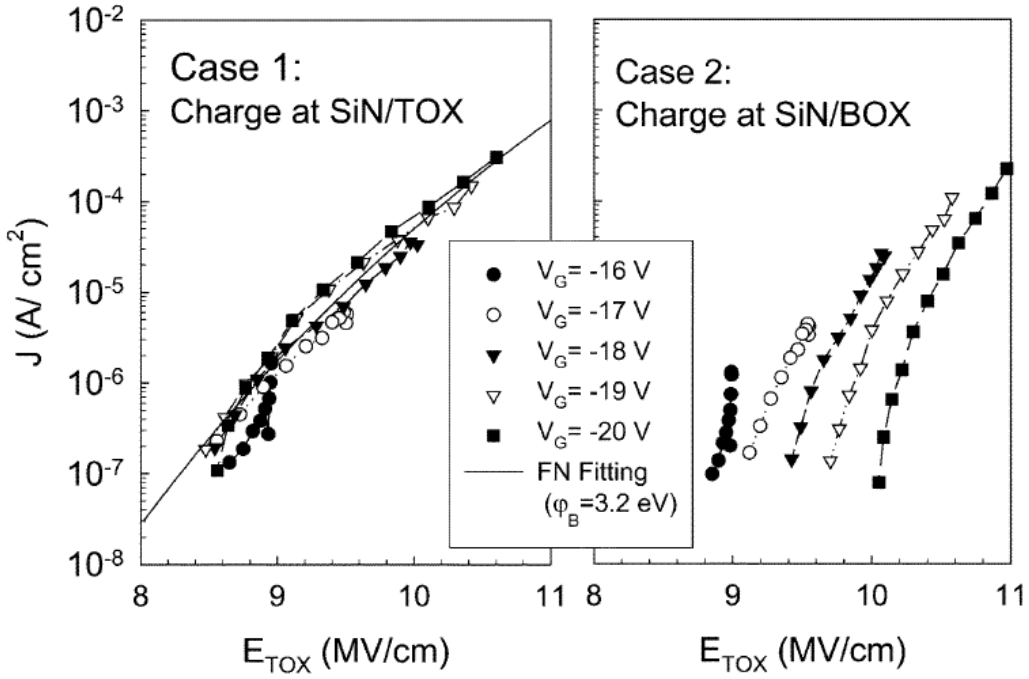
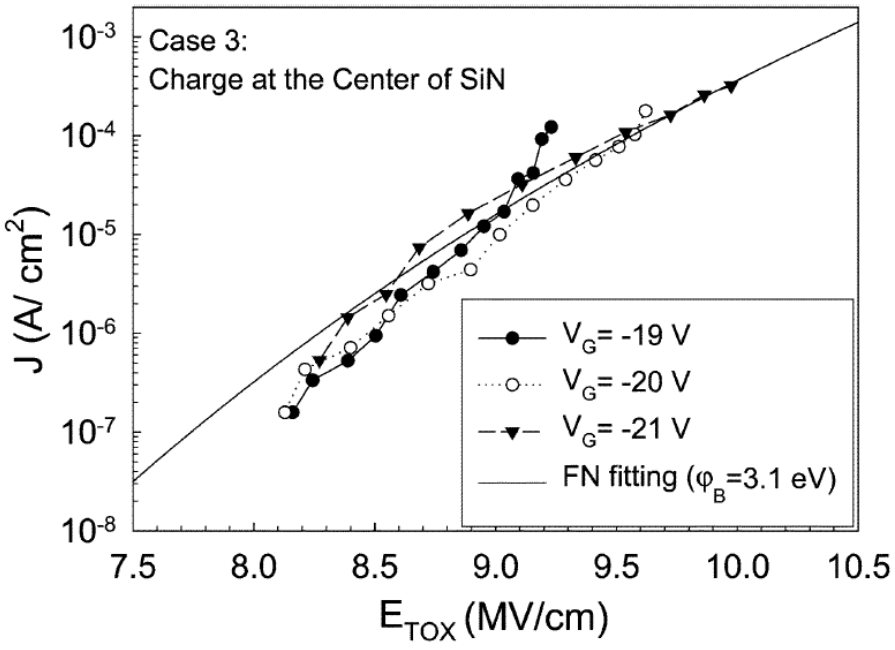


Fig. 2.17 (a) Measurement setup for carrier separation and charge-centroid extraction. (b) Waveforms for the P/E pulses showing the three-level shape used to obtain a null contribution to the overall current integral of the displacement charge in the semiconductor [2.33].



(a)



(b)

Fig. 2.18 Transient analysis of J vs. E_{Tox} for SONOS devices with N^+-poly gate and different T.O. (a) Thermal oxidation T.O. and (b) HTO T.O. [2.35].

CHAPTER THREE

GATE-SENSING AND CHANNEL-SENSING (GSCS) TRANSIENT ANALYSIS METHOD

OUTLINE

3.0 Introduction

As mentioned at the end of chapter 2, although there have been many works investigating on the trapped vertical location, they suffered from many limitations. Therefore, we proposed an novel gate-sensing and channel-sensing (GSCS) method to solve the difficulties. In this chapter, the fundamental theory of this method is introduced. We first introduce two basic models for charge density and vertical location extraction, then this method is demonstrated on one standard SONOS capacitor. Moreover, we also discuss the accuracy and doping effect on this method.

3.1 Theoretical Equations Derivation

GSCS method measures two SONOS-type capacitors; one using “channel sensing” (CS), and the other using “gate sensing” (GS), as illustrated in Fig. 3.1. The two capacitors have identical ONO processes but different doping conditions. The CS capacitor has a lightly doped well and a heavily doped poly gate. Therefore, the depletion mainly occurs in the well, and the V_{FB} shift is sensed by the channel ($\Delta V_{FB,CS}$). On the other hand, the GS capacitor has a lightly doped poly gate and a heavily doped well. Therefore, the depletion mainly happens in the poly gate, and the V_{FB} shift is sensed by the gate ($\Delta V_{FB,GS}$).

For the same charge configuration inside the nitride, these two capacitors give different V_{FB} shifts and provide two equations, thus we can solve two variables. However, if we only have the conventional CS capacitor, only one message can be given. That is why our GSCS method could provide more trapped charge information.

3.1.1 Bulk Trap Model

We first proposed bulk trap model where total charge density (Q) and mean vertical location (x) can be solved simultaneously. In the beginning, we assumed a sheet charge inside the nitride for simplicity. The density of the sheet charge is defined as Q (electron-cm^{-2}) while

the relative vertical location in nitride is defined as x (cm), as illustrated in Fig. 3.2(a). For the CS method, the $\Delta V_{FB,CS}$ is proportional to the charge density multiplied by the distance toward the poly gate [3.1]:

$$\Delta V_{FB,CS} = Q\left(\frac{T_{Tox}}{\varepsilon_0 \varepsilon_{ox}} + \frac{T_N - x}{\varepsilon_0 \varepsilon_N}\right) \tag{3-1}$$

On the other hand, for the GS method, since the channel and gate are effectively reversed, the equation becomes:

$$\Delta V_{FB,GS} = Q\left(\frac{T_{Box}}{\varepsilon_0 \varepsilon_{ox}} + \frac{x}{\varepsilon_0 \varepsilon_N}\right) \tag{3-2}$$

where $\Delta V_{FB,CS}$ and $\Delta V_{FB,GS}$ are defined as the flat-band voltage shifts with respect to the initial (uncharged) flat-band voltages. Several parameters are defined in Fig. 3.2(a) while the others are their usual meanings. It should be noted that in our notation, Q is positive (+) for electron charge while negative (–) for hole charge.

The flat-band voltage shifts can be transformed into Q and x by solving Eqs. (3-1) and (3-2):

$$Q = \varepsilon_0 \varepsilon_{ox} \frac{\Delta V_{FB,CS} + \Delta V_{FB,GS}}{EOT} \tag{3-3}$$

$$x = \frac{\Delta V_{FB,GS}(T_{Tox}\varepsilon_N + T_N \varepsilon_{ox}) - \Delta V_{FB,CS} T_{Box} \varepsilon_N}{\varepsilon_{ox}(\Delta V_{FB,CS} + \Delta V_{FB,GS})} \tag{3-4}$$

EOT is the effective oxide thickness of total ONO films. Although Eqs. (3-3) and (3-4) are derived by assuming a sheet charge density, the equations are also valid even for an arbitrary charge distribution, where

$$Q_{total} = \int_0^{T_N} Q(x)dx \tag{3-5}$$

$$\hat{x} = \frac{1}{Q_{total}} \int_0^{T_N} Q(x)xdx \tag{3-6}$$

Q_{tot} (electron-cm^{-2}) is the total summation of charge density at various vertical locations, and

$\hat{x}$ (cm) is the mean vertical location inside nitride. The reason why Eqs. (3-3) and (3-4) can be transformed to the mean value result is simply due to the principle of linear superposition. A detailed derivation is given in Appendix A.

3.1.2 Two-region Approximation Model

In principle, we have two independent Eqs. (3.1) and (3.2) from CS and GS, and therefore we can solve any two independent variables. Instead of Q and x, we can also solve for the charges inside bottom (Q_1) and top (Q_2) portions of nitride, and we called it as two-region approximation model, as illustrated in Fig. 3.2(b). For simplicity, we assumed the locations of Q_1 and Q_2 are at $¼T_N$ and $¾T_N$, respectively, and the Eqs. (3.1) and (3.2) can be modified as

$$\Delta V_{FB,CS} = Q_1\left(\frac{T_{Tox}}{\varepsilon_0\varepsilon_{ox}} + \frac{¾T_N}{\varepsilon_0\varepsilon_N}\right) + Q_2\left(\frac{T_{Tox}}{\varepsilon_0\varepsilon_{ox}} + \frac{¼T_N}{\varepsilon_0\varepsilon_N}\right) \tag{3-7}$$

$$\Delta V_{FB,GS} = Q_1\left(\frac{T_{Box}}{\varepsilon_0\varepsilon_{ox}} + \frac{¼T_N}{\varepsilon_0\varepsilon_N}\right) + Q_2\left(\frac{T_{Box}}{\varepsilon_0\varepsilon_{ox}} + \frac{¾T_N}{\varepsilon_0\varepsilon_N}\right) \tag{3-8}$$

From Eqs. (3-7) and (3-8), we can directly solve Q_1 and Q_2:

$$Q_1 = \frac{\varepsilon_0[\Delta V_{FB,CS}(T_{Box}\varepsilon_N + ¾T_N\varepsilon_{ox}) - \Delta V_{FB,GS}(T_{Tox}\varepsilon_N + ¼T_N\varepsilon_{ox})]}{½T_N EOT} \tag{3-9}$$

$$Q_2 = \frac{\varepsilon_0[-\Delta V_{FB,CS}(T_{Box}\varepsilon_N + ¼T_N\varepsilon_{ox}) + \Delta V_{FB,GS}(T_{Tox}\varepsilon_N + ¾T_N\varepsilon_{ox})]}{½T_N EOT} \tag{3-10}$$

Contrary to Eqs. (3-3) and (3-4), Eqs. (3-9) and (3-10) are only approximations. It can be used to investigate what type of trapped charges, but the “real” amount of charges cannot be obtained accurately. Two-region approximation model is useful to discriminate the charges inside bottom and top portions of the nitride, especially for SNS and SONS devices, where the channel injection and gate injection happen simultaneously. Therefore, for these devices Q_1 and Q_2 give us clearer understanding of the trapped charge behaviors than Q and x.

3.2 GSCS Method Demonstration

Based on the models in section 3.1, we can directly track the "real-time" trapped charges during programming/erasing and reliability testing. In this section, we will describe in detail the preparation and the basic characteristics of GS and CS samples. The first simple results based on bulk trap model are also demonstrated. Finally, we will compare the results extracted by our method with other methods.

3.2.1 Sample Descriptions

Large area (500μm × 500μm) SONOS-type capacitors with various ONO conditions are fabricated. For each sample, both GS and CS capacitors are made, and we fabricate them at the same time except the poly gate/well doping processes to ensure they have identical ONO thickness. For all samples, the B.O. is grown by in-situ steam generation (ISSG) method which can minimize the impact of different substrate doping because ISSG is a radical-reaction process, but not a thermal-diffusion process. Nitride layers are deposited by the industrial standard LPCVD process, using SiH_2Cl_2 and NH_3 at 680^oC. On the other hand, oxynitride (SiON) is also deposited by the same LPCVD process, but with additional N_2O gas flow. The dielectric constant of SiON is equal to 6.5, and optical index of refraction = 1.8 (nitride is 2.0). For the T.O., both wet oxidation of nitride (wet conversion) and HTO top oxide are used.

In this method, we adopted p-type well and p-type poly gate for both GS and CS capacitors. Typically, p-well doping densities for CS and GS are around $10^{17}cm^{-3}$ and $7\times10^{18}cm^{-3}$, respectively while the p-poly gate doping densities for CS and GS are around $10^{20}cm^{-3}$ and $5\times10^{16}cm^{-3}$, respectively. For all the samples, n^+-doped source/drain regions are formed so that channel inversion layer can be formed during +FN programming.

In this method, the well and poly gate doping do not need to be p-type. N-type well and n-type poly gate can be used as well. We have also used wells and gates with opposite

polarities. For example, a lightly doped p-poly gate with a heavily doped n-well was used for the GS capacitor. However the measured CV curve had a larger distortion, which affected the accuracy of V_{FB} shift extraction. This is because both poly depletion and substrate depletion happened at the same time during $-V_G$ bias for this sample, resulting in a complicated CV curve. Therefore, it is best to use the same polarity for both well and poly gate because only one of them has depletion during +/– V_G biases.

3.2.2 Basic Characteristics of GS and CS Capacitors

We first consider the device characteristics of SONOS (ONO = 54/70/90Å) under +FN programming. Device is programmed by +FN using various biases from the initial fresh state ($V_{FB,GS}$ and $V_{FB,CS}$ ~ 0V), and both the CS and GS capacitors are measured under identical electrical testing procedures. The corresponding CV curves are shown in Fig. 3.3.

In Fig. 3.3(a), the CV curves of CS capacitor are in accumulation at $-V_{Gate}$ (or $+V_{well}$), and become depletion and even inversion at $+V_{Gate}$ (or $-V_{well}$). The inversion layer can be formed because n^+ source/drain regions are introduced. On the other hand, the CV curves of GS capacitor are in accumulation at $-V_{well}$ (or $+V_{Gate}$) and become depletion at $+V_{well}$ (or $-V_{Gate}$). However, the inversion layer cannot be formed because the poly gate does not have source/drain regions hence deep depletion continues at larger $+V_{well}$. Moreover, the CV curves of GS capacitor have much more gradual slope during transition. This is possibly because there are more interfacial states at poly gate and T.O. interface. However, the CV curves still show parallel shift during +FN programming, which is sufficient for V_{FB} shift extraction.

The extracted ΔV_{FB} in Fig. 3.4 shows that the $\Delta V_{FB,CS}$ and $\Delta V_{FB,GS}$ are clearly different. This is because SONOS (ONO = 54/70/90Å) has thicker T.O. and thinner B.O. According to Eqs. (3-1) and (3-2), $\Delta V_{FB,CS}$ should be larger than $\Delta V_{FB,GS}$.

3.2.3 Extracted Trapped Charge Evolution and Vertical Location Evolution

In Fig. 3.4, the two V_{FB} shifts ($\Delta V_{FB,CS}$ and $\Delta V_{FB,GS}$) at a given time can be transformed into Q and x by using Eqs. (3-3) and (3-4), and the results are shown in Fig. 3.5(a) and (b), respectively. The charge evolution (Q-t) and mean vertical location evolution (x-t) can be directly extracted by this GSCS method. In Fig. 3.5(a), Q-t has a similar shape as ΔV_{FB}-t (Fig. 3.4), as expected. On the other hand, x-t in Fig. 3.5(b) shows that injected electrons migrate from the bottom interface toward the top interface.

In order to obtain a clearer idea about the charge evolution, x-Q curves are plotted, as illustrated in Fig. 3.5(c). x-Q is a simple transformation from Q-t and x-t curves. In Fig. 3.5(c), as electron density increases the mean charge vertical location migrates from the bottom interface toward the center of nitride. The final saturated x is around 40Å, which is very close to the center of nitride. Moreover, despite the large dependency of program speed to the program voltage, x-Q plots are independent of the program voltage. This clearly shows that the x-Q plot expresses an intrinsic property of the ONO structure (the charge trapping behavior) and is not affected by external factors such as e-field.

3.2.4 Comparison with Other Methods

In order to verify the charge vertical location in Fig. 3.5, we use two different methods to monitor the vertical location.

The first method is to apply our previous transient analysis method [3.2], as mentioned in section 2.3.2, where J-E_{Tox} curves of gate injection operated SONOS devices are compared with various charge location assumptions. However, for channel-injection operated SONOS devices the tunnel oxide is the bottom oxide instead of the top oxide in the gate-injection operated SONOS devices. Therefore, we should plot the J vs. bottom oxide e-field (E_{Box}) curves, and then compare the J-E_{Box} curves at various program voltages by assuming different charge vertical locations. Since the E_{Box} of CS capacitor is independent of charge vertical

location, the GS capacitor ($\Delta V_{FB,GS}$) should be introduced to extract J-E_{Box} plots, and the detailed equations are shown in Appendix B. For the GS capacitor, since the channel and gate are effectively reversed, the equations to calculate the E_{Tox} in [2.36] can be utilized to calculate the E_{Box} in our case. The calculated results are shown in Fig. 3.6, in which Case 1 represents charges placed at T.O./nitride interface, Case 2 represents charges placed at the B.O./nitride interface, and Case 3 represents charges placed at the center of nitride. The results indicate that Case 3 has better consistency for every program voltage while it is much less consistent for Case 1 and Case 2. These results suggest that the centroid of electrons is more likely located near the center of nitride, which is consistent with Fig. 3.5.

The second method is to directly simulate the ΔV_{FB}-t curves assuming various charge vertical locations. The theoretical calculation can be carried out by integrating the FN tunneling current with respect to time. Appendix C illustrates the detail of this simulation method for ΔV_{FB}-t, and the results are shown in Fig. 3.7. For CS capacitor (Fig. 3.7(a)), it is very interesting that $\Delta V_{FB,CS}$-t are almost the same for various charge vertical locations. Equation (C-4) shows that the E_{Box} is independent of the charge vertical location (for Case 1, Case 2, or Case 3). Therefore, we cannot distinguish the real charge vertical location from $\Delta V_{FB,CS}$-t. On the other hand, for the GS capacitor (Fig. 3.7(b)), since the channel and gate are effectively reversed, the equations of E_{Box} are very different for different vertical locations, as shown in Eqs. (B-2), (B-4), and (B-6). Figure 3.7(b) shows the simulated $\Delta V_{FB,GS}$-t for various charge vertical locations, and only Case 3 (assuming the charges are placed at the center of nitride) is consistent with the measured data. Again, this result supports that the charge centroid is close to the center of nitride after +FN injection.

Although the above two methods can obtain results that are consistent with Fig. 3.5, these methods have limitations and can only provide a rough estimate of charge vertical location. On the other hand, our novel GSCS method is more powerful and provides “real-time” monitoring of trapped charges.

3.3 Accuracy Estimation

In this section, we will discuss the accuracy of our GSCS method. There are two major factors that affect the accuracy of this method. The first one is the error in ONO thickness measurement, and the other is that the injected charges of CS and GS capacitors are not identical.

3.3.1 Error in ONO Thickness Measurement

We first consider the error in ONO thickness measurement. The typical error in thickness measurement is usually less than 5%. For SONOS (ONO = 54/70/90Å), we assume the thickness in B.O., nitride, and T.O. have ±2% and ±5% from the ideal 54Å, 70Å, and 90Å, respectively. We then calculate Q and x from Fig. 3.4 by using Eqs. (3.3)-(3.4). The corresponding x-t and Q-t plots are shown in Fig. 3.8. Figures 3.8(a) and (b) show the B.O. thickness variation while Figs. 3.8(c) and (d) show the nitride thickness variation, and Figs. 3.8(e) and (f) show the T.O. thickness variation. The calculated results show that for all kinds of thickness variation, the mean vertical location (x) remains around the center of nitride with the variation < 7%, and the total charge density (Q) is almost unchanged with the variation < 1.5%. Because both the variation of x and Q is smaller than 10%, the accuracy of our method is excellent even when there is finite (< 5%) error in ONO thickness measurement.

3.3.2 Error in the Amount of Injected Charges

Next, we consider the other errors caused by the difference between the CS and GS capacitors such as the B.O. thickness is not the same for the two capacitors. Different B.O. thickness results in different +FN injection currents and then different injected charges. If the injected charges inside the nitride of the two capacitors are different, they result in inadequate determination of Q and x. In order to estimate this error, we assume two cases. The first one is

that B.O. of the CS capacitor has ±2% and ±5% variation from 54Å while the GS capacitor has exactly 54Å B.O. The second case is that B.O. of the GS capacitor has ±2% and ±5% variation from 54Å while the CS capacitor has exactly 54Å B.O. We estimate the error by calculating theoretical ΔV_{FB}-t for both CS and GS capacitors, taking into account the thickness variation, as mentioned earlier. In the ΔV_{FB}-t calculation, we assume that the x-Q follows a hyperbolic tangent function, which is obtained from fitting the experimental x-Q plot, as shown in Fig. D-1. The detailed equations are shown in Appendix D. The calculated $\Delta V_{FB,CS}$-t and $\Delta V_{FB,GS}$-t are shown in Fig. 3.9(a) and Fig. 3.9(b), respectively.

Using Eqs. (3.3) and (3.4), Fig. 3.9 can be transformed into Q and x, as shown in Fig. 3.10. Figures 3.10(a) and (b) show CS capacitor has ±2% and ±5% variation in B.O. thickness from the GS one, and Figs. 3.10(c) and (d) show GS capacitor has ±2% and ±5% variation in B.O. thickness from the CS one. Both x-t in Figs. 3.10(a) and (c) show large deviation from the ideal case at short programming time ($< 10^{-4}$sec) while they show small deviation at longer programming time. We conjecture that at short programming time, the amount of injected charges is very small, so the x value is sensitive to B.O. thickness variation. On the other hand, at longer programming time, the amount of injected charges is large enough to reveal nitride intrinsic characteristic, so the x value is insensitive to B.O. thickness variation. The final x variation is smaller than 7.2% and 1% for CS and GS capacitors, respectively. For the GS method, because the channel and gate are effectively reversed during sensing, it is less sensitive to B.O. variation. Both Q-t in Figs. 3.10(b) and (d) show small deviation, the variation is smaller than 2.3% and 1% for CS and GS capacitors, respectively. Therefore, we show that in our method, the accuracy of location evolution (x-t) at long time and charge evolution (Q-t) is very high. But if the amount of injected charges is very small, location evolution (x-t) may have larger deviation.

3.4 Doping Concentration Effect

The especial point of GSCS method is the use of GS capacitor which has reversed dopant conditions as compared with conventional CS capacitor. Therefore, the other hot topic is the doping concentration effect on the GSCS method. In this section, we will discuss the gate and well doping effect and further propose the optimized doping concentration. For simplicity, we just pick up two different doping concentrations for comparison. In fact, more than four doping concentrations are taken into account.

3.4.1 Gate/Well Doping Effect on the GSCS Method

We first consider the gate doping effect on GSCS method. For CS capacitor, the poly depletion can be ignored during operations due to the heavy doped poly gate. However, for GS capacitor, the lightly doped poly gate depletes during operations which may result in violating the assumption that GS and CS have identical ONO thickness and charge injection. Fortunately, from the comparison of two GS capacitors (BE-SONOS, ONONO = 13/20/25/60/60Å) with different poly gate doping concentrations ($5\times10^{16}cm^{-3}$ and $1\times10^{17}cm^{-3}$) but the same well doping concentration ($7\times10^{18}cm^{-3}$), we find that the $\Delta V_{FB,GS}$ of two GS capacitors are almost the same for both +FN program (Fig. 3.11(b)) and –FN erase (Fig. 3.11(c)) regardless of the diverse CV curves (Fig. 3.11(a)). This is because the poly gate depletion effect can be ignored under our designed doping concentrations and device operation conditions. Since $\Delta V_{FB,GS}$ is insensitive to poly gate doping concentrations, the poly gate doping concentrations of CS and GS capacitors have a minor effect on the accuracy of GSCS method.

Next, we consider the well doping effect on GSCS method. Two CS capacitors (BE-SONOS, ONONO = 13/20/25/70/90Å) with different well doping concentrations ($10^{17}cm^{-3}$ and $2\times10^{17}cm^{-3}$) but the same poly gate doping concentration ($10^{20}cm^{-3}$) are compared in Fig. 3.12. The capacitor with more heavily doped well can be depleted more hardly than the capacitor with more lightly doped well, as shown in Fig. 3.12(a). Although the

well doping concentrations are not identical, the source/drain regions could still provide the same electron injection during +FN programming, as shown in Fig. 3.12(b). For –FN erasing, both p-wells could provide accumulated holes to inject into nitride, and the variation between different well doping concentrations can be ignored, as shown in Fig. 3.12(c). Therefore, $\Delta V_{FB,CS}$ is insensitive to well doping concentration.

However, for GS capacitors with different well doping concentrations ($7\times10^{18}cm^{-3}$ and $2\times10^{19}cm^{-3}$) but the same poly gate doping concentration ($5\times10^{16}cm^{-3}$), we find different results, as illustrated in Fig. 3.13. The variation in CV (Fig. 3.13(a)) comes from the variation in p-well depletion at $V_{well} < 0V$ (or $V_{Gate} > 0V$). The more heavily doped well has less well depletion, leading to larger capacitance. For the +FN program and –FN erase speeds, shown in Fig. 3.13(b) and (c), we find that the more heavily doped well has slower program speed, but the erase speed keeps almost the same. This may be because the more heavily doped well is harder to be inverted during +FN programming, which results in smaller electron injection (slower program speed). However, during –FN erasing the well is in accumulation mode, therefore, different well doping concentrations still provide the same hole injection. Therefore, the well doping concentration of GS capacitor will affect the accuracy of GSCS method, and we should further optimize it.

3.4.2 Doping Concentration Optimization

By considering the concerns mentioned in section 3.4.1 and keeping the gate sensing and channel sensing concepts, we choose well doping concentrations for CS and GS as $10^{17}cm^{-3}$ and $7\times10^{18}cm^{-3}$, respectively while the poly gate doping concentrations for CS and GS as $10^{20}cm^{-3}$ and $5\times10^{16}cm^{-3}$, respectively. For CS capacitor, the gate doping concentration should be much higher than well doping concentration, on the other hand, for GS capacitor, the gate doping concentration should be much lower than well doping concentration. Moreover, the well doping concentration of GS capacitor should be chosen as smaller than $10^{19}cm^{-3}$ so that

the inversion layer can be formed well, and the assumption that the injected charges are the same for two capacitors can be established without doubt.

3.5 Summary

In this chapter, we provided the detailed discussion of our novel GSCS method. By introducing a new measurable quantity ($\Delta V_{FB,GS}$), two trapped charge messages can be obtained simultaneously during programming/erasing or retention tests.

The detailed equation derivation was also described in this chapter for both bulk trap model, where total charge density (Q) and mean vertical location (x) can be monitored simultaneously, and two-region approximation model, where the charges in the bottom portion of nitride (Q_1) and top portion of nitride (Q_2) can be monitored separately. Based on these models, we could successfully demonstrate our GSCS method on SONOS-type devices. Although the charge centroid results obtained by our method consist with other method, our method is more powerful. The "real time" trapped charge behaviors can be directly monitored by our method.

We also examined the accuracy of this new method extensively. We find that this method has a high accuracy against the thickness error of B.O., nitride, or T.O. thickness. On the other hand, if GS and CS capacitors have finite thickness differences in B.O., it shows a larger error in determining the x at initial programming, however, Q is much less vulnerable to the thickness variation.

At the end of this chapter, we discussed the well/poly gate doping effect on the accuracy of our GSCS method. Only the well doping concentration of GS capacitor will affect the accuracy of our method, and other doping concentrations have minor effect. Based on the evaluation, we finally choose well doping concentrations for CS and GS as $10^{17}cm^{-3}$ and $7\times10^{18}cm^{-3}$, respectively while the poly gate doping concentrations for CS and GS as $10^{20}cm^{-3}$ and $5\times10^{16}cm^{-3}$, respectively.

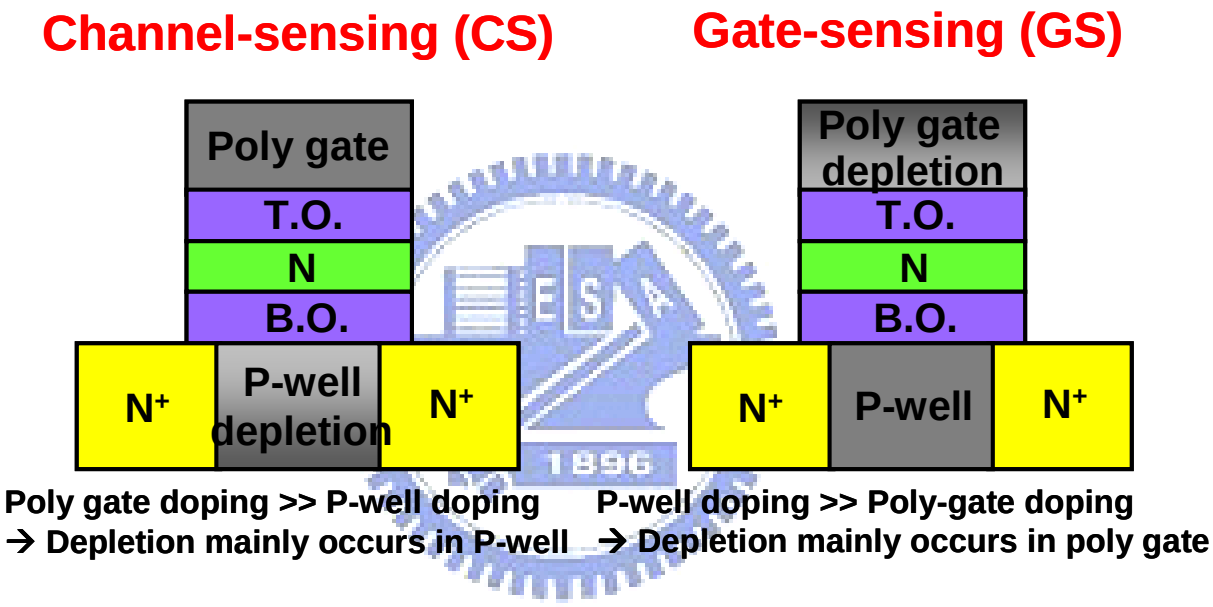


Fig. 3.1 Schematic diagrams that illustrate the gate-sensing (GS) and channel-sensing (CS) transient analysis method.

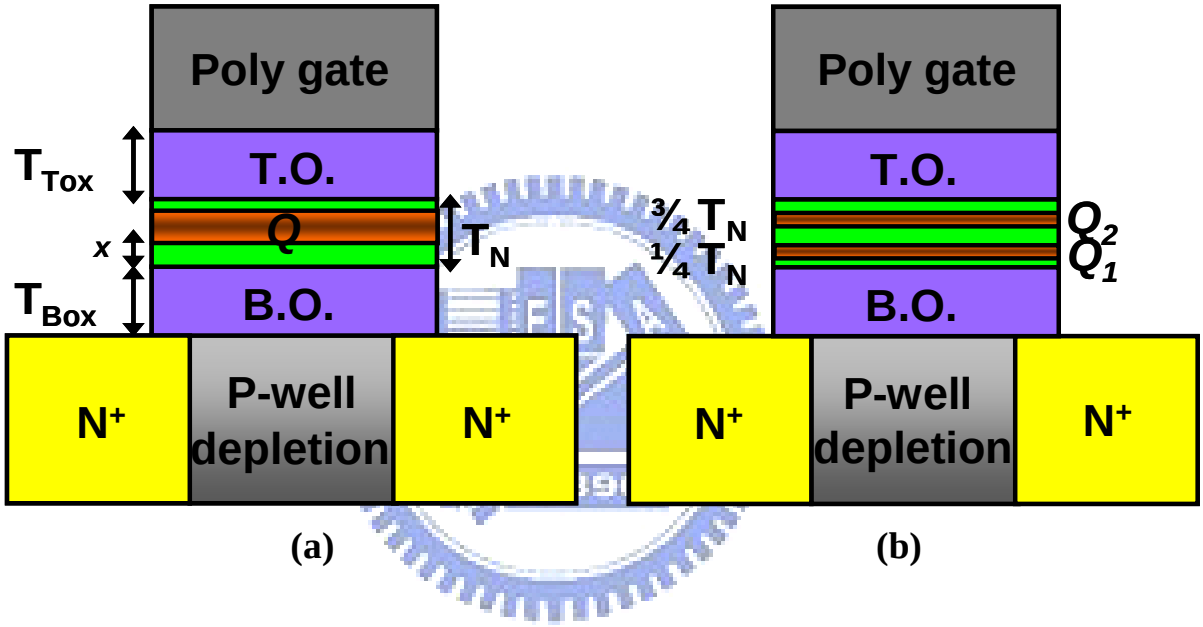


Fig. 3.2 (a) Bulk trap model: definition of the sheet charge density (Q) and vertical location (x). (b) A two-region approximation model: Q_1 and Q_2 are the charges inside the bottom and top portions of nitride, respectively.

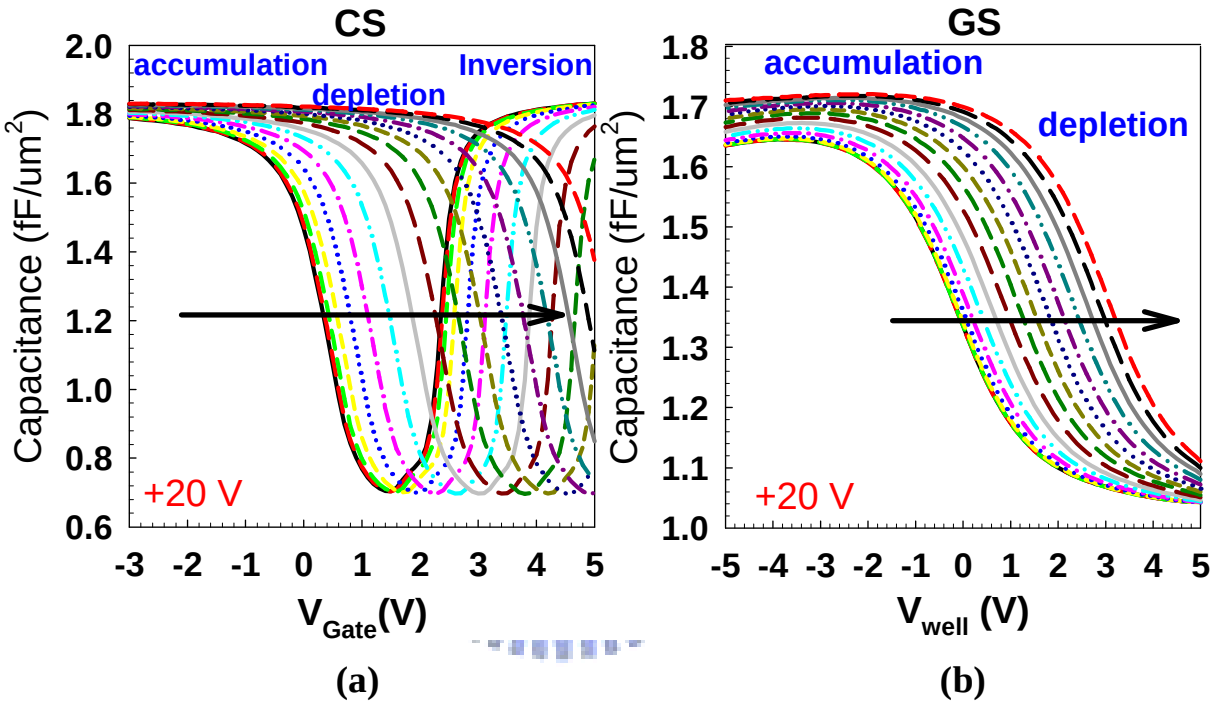


Fig. 3.3 CV curves of SONOS (ONO=54/70/90Å) during +FN programming (a) CS capacitor (b) GS capacitor.

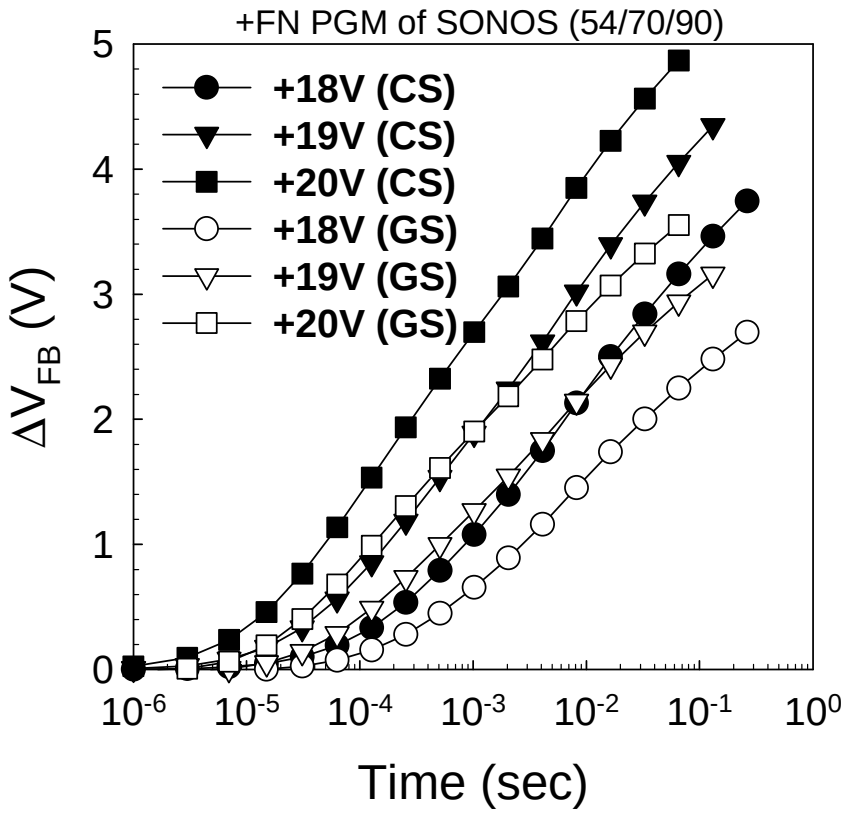


Fig. 3.4 Comparison of the V_{FB} shifts of SONOS (ONO=54/70/90Å) during +FN programming. "GS" indicates the gate-sensing results, and "CS" indicates the channel-sensing results.

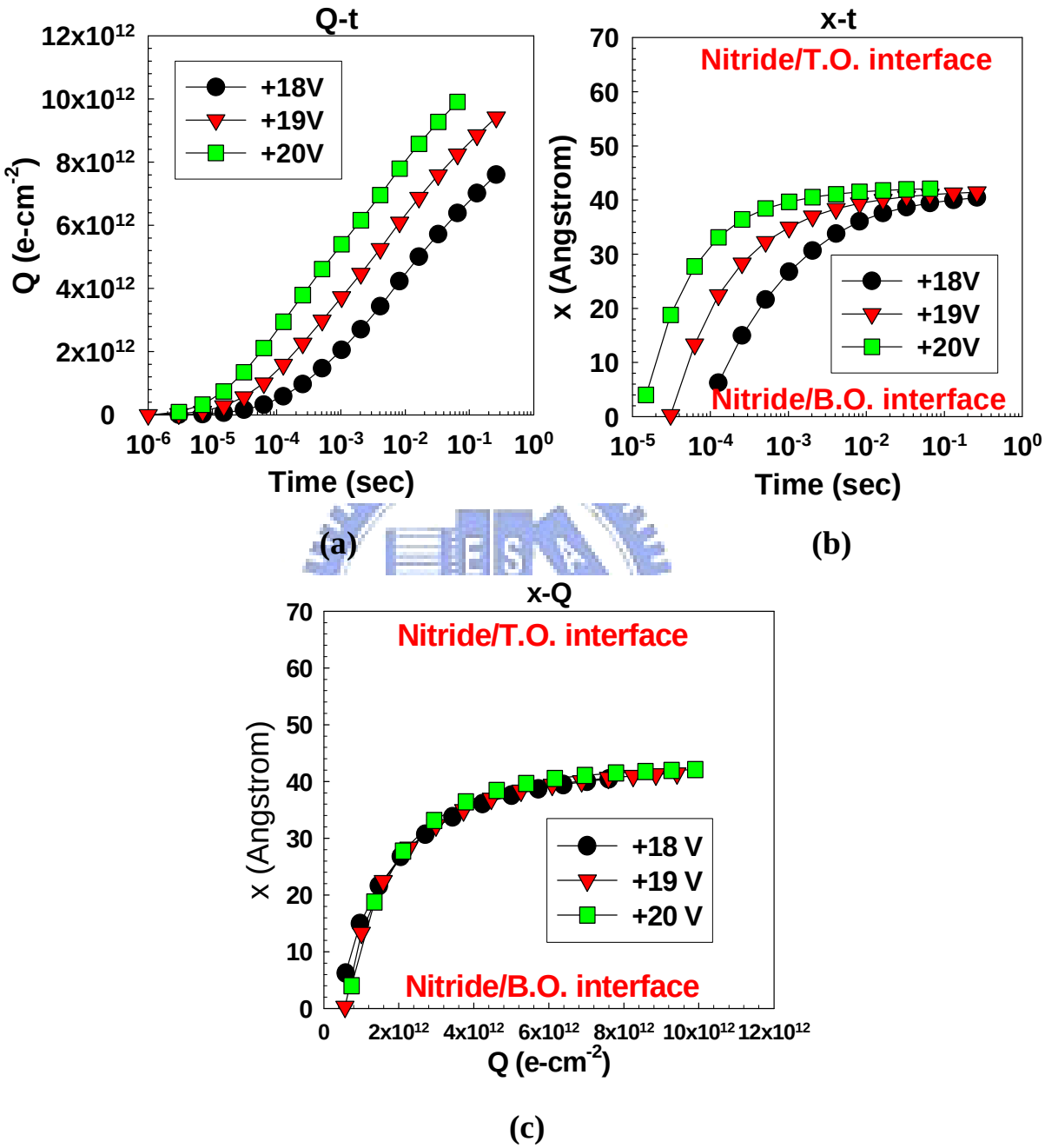


Fig. 3.5 (a) Q-t and (b) x-t of SONOS (ONO=54/70/90Å) transformed from Fig. 3.4 by using Eqs. (3.3) and (3.4). (c) x-Q transformed from Q-t and x-t.

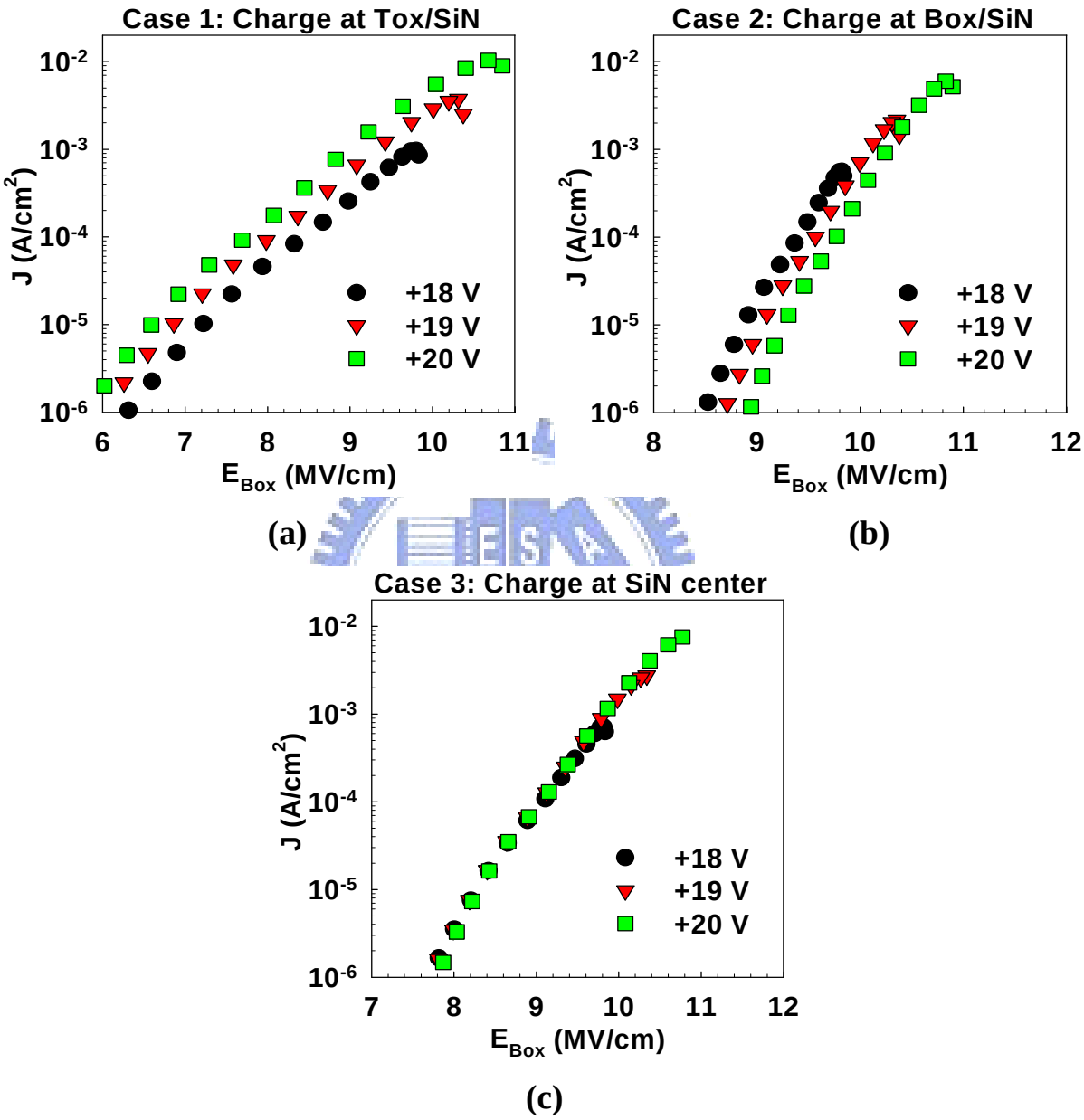
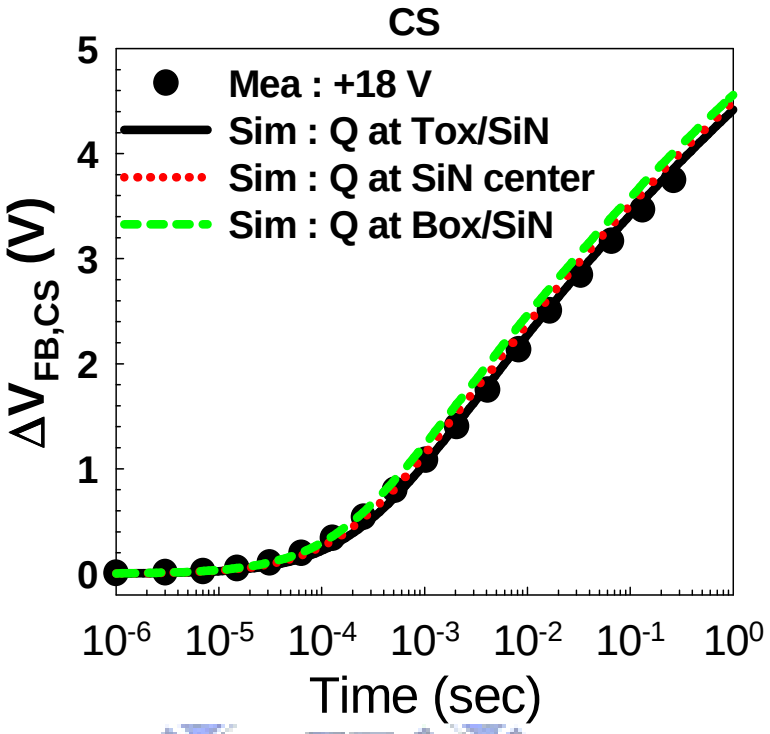
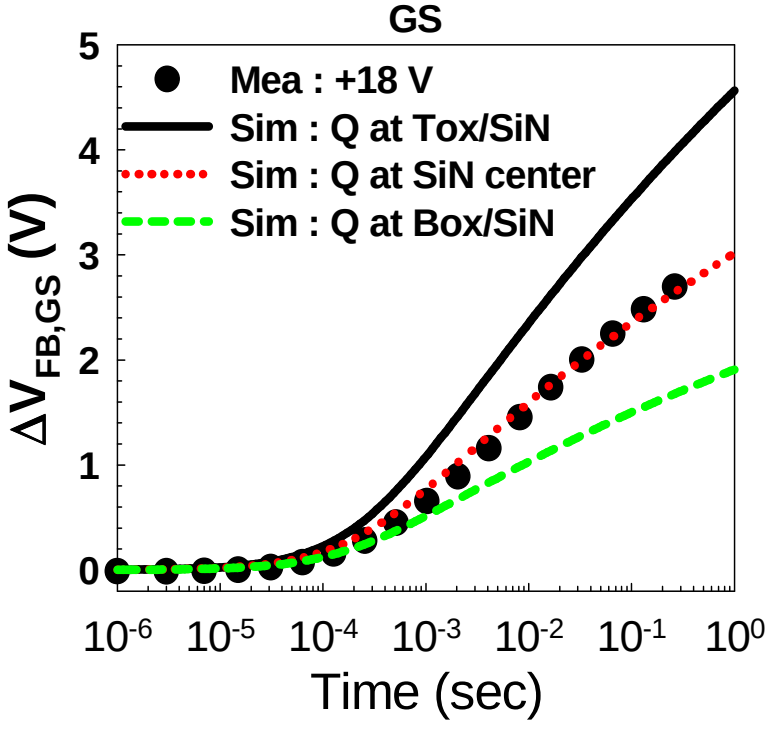


Fig. 3.6 J vs. E_{Box} curves of GS capacitor by assuming different charge vertical locations. (a) Charges are at T.O./nitride interface. (b) Charges are at B.O./nitride interface. (c) Charges are at center of nitride.



(a)



(b)

Fig. 3.7 Comparison of (a) $\Delta V_{FB,CS}$-t and (b) $\Delta V_{FB,GS}$-t with the theoretically calculated results by assuming different charge vertical locations.

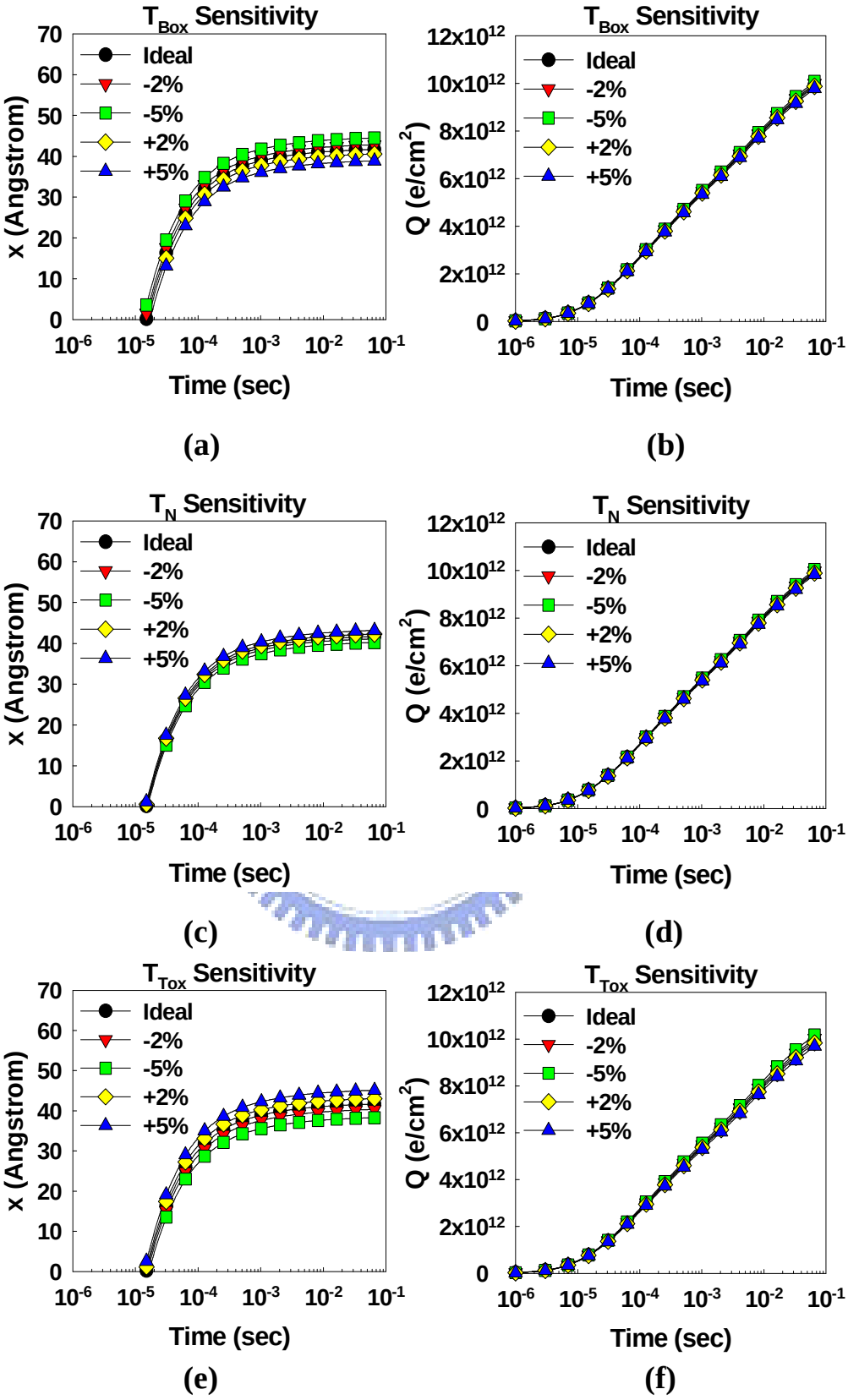


Fig. 3.8 x-t and Q-t plots for different thickness measurement errors. (a) and (b) show the B.O. thickness variation. (c) and (d) show the nitride thickness variation. (e) and (f) show the T.O. thickness variation.

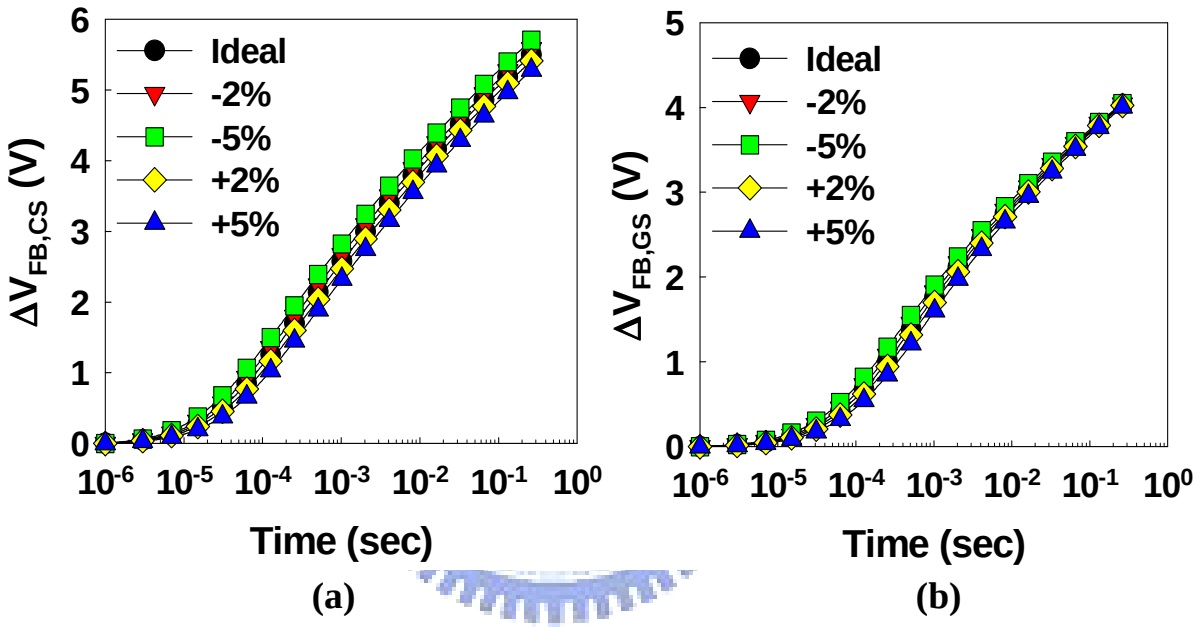


Fig. 3.9 (a) $\Delta V_{FB,CS}$-t and (b) $\Delta V_{FB,GS}$-t for ±2% and ±5% variation in B.O. thickness during +FN programming.

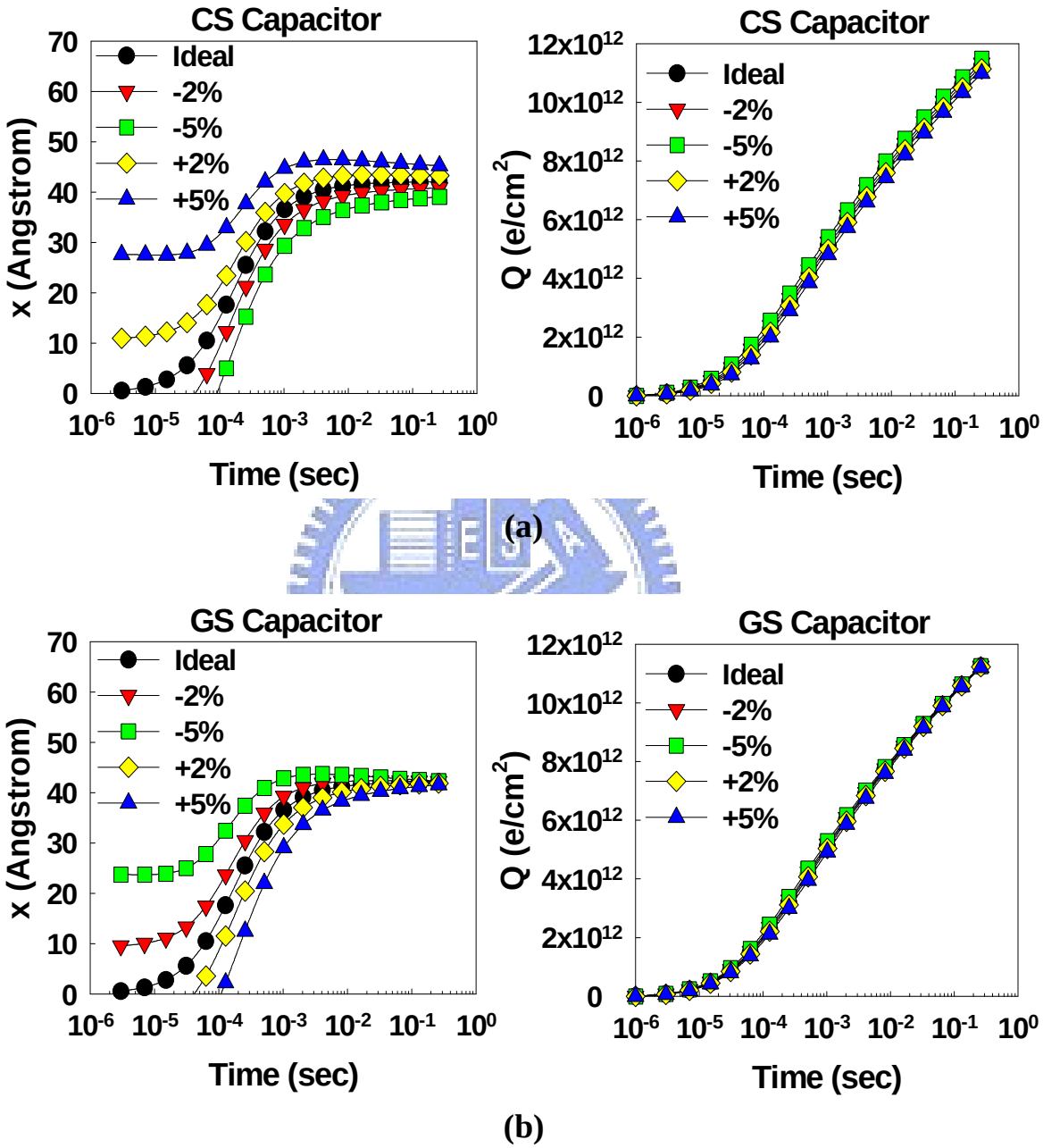


Fig. 3.10 X-t and Q-t plots transformed from Fig. 3.9. (a) and (b) show CS capacitor has ±2% and ±5% variation in B.O. thickness from 54Å. (c) and (d) show GS capacitor has ±2% and ±5% variation in B.O. thickness from 54Å.

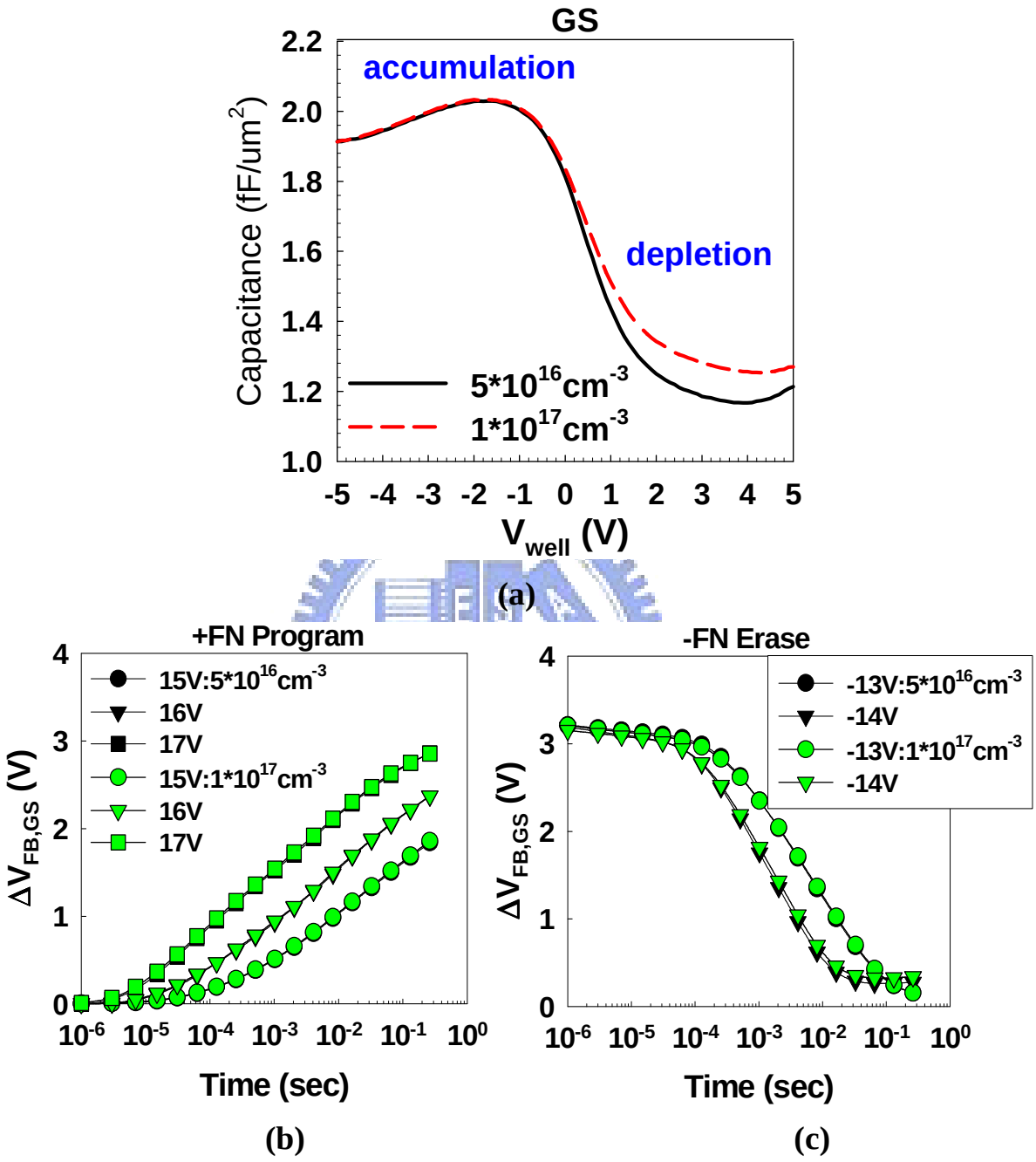


Fig. 3.11 Comparison of GS capacitors (BE-SONOS, ONONO = 13/20/25/60/60Å) with different poly gate doping concentrations. (a) CV curves. (b) $\Delta V_{FB,GS}$ during +FN programming. (c) $\Delta V_{FB,GS}$ during –FN erasing. The $\Delta V_{FB,GS}$ is insensitive to poly gate doping concentrations.

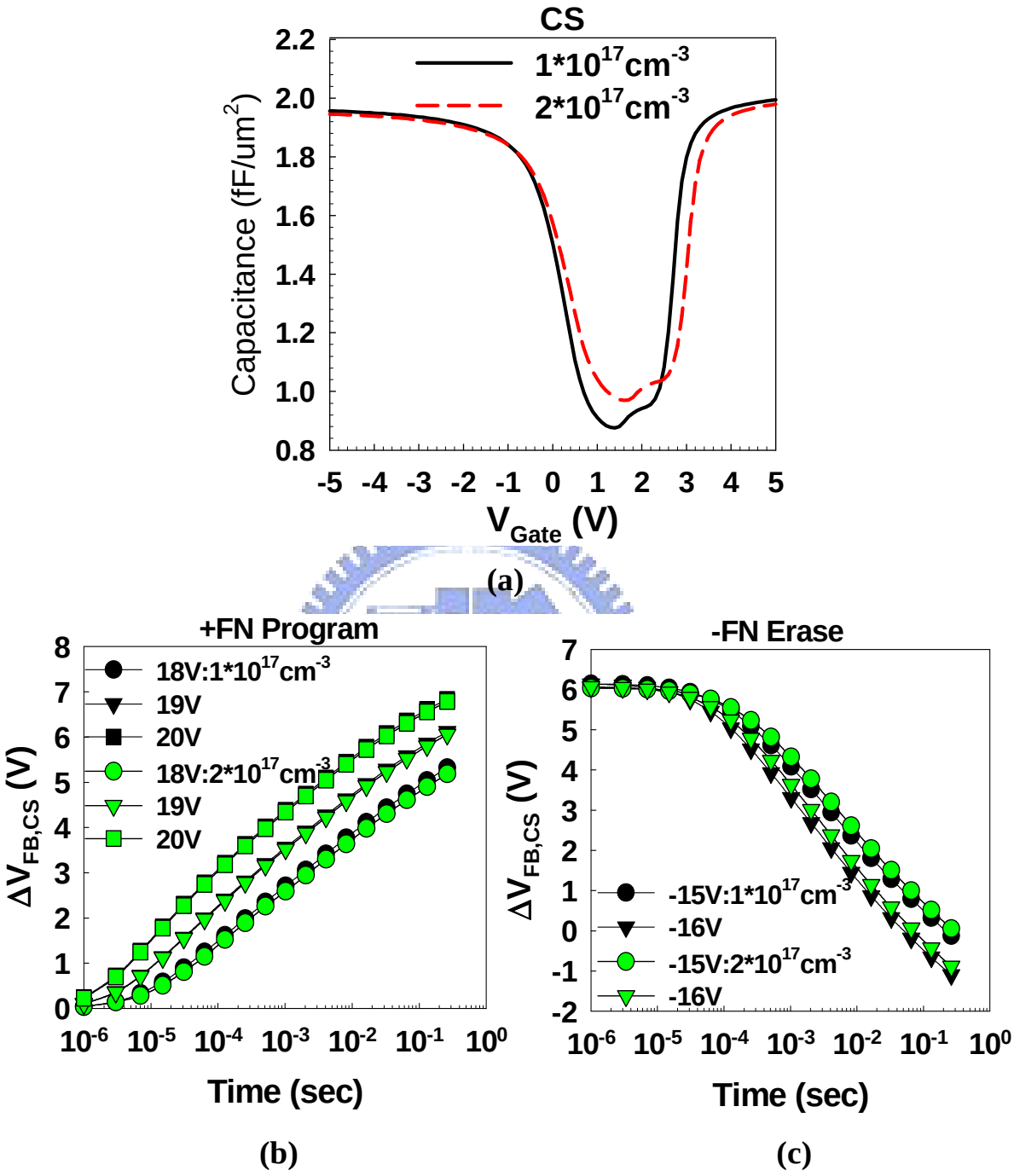


Fig. 3.12 Comparison of CS capacitors (BE-SONOS, ONONO = 13/20/25/70/90Å) with different well doping concentrations. (a) CV curves. (b) $\Delta V_{FB,CS}$ during +FN programming. (c) $\Delta V_{FB,CS}$ during –FN erasing. The $\Delta V_{FB,CS}$ is insensitive to well doping concentrations.

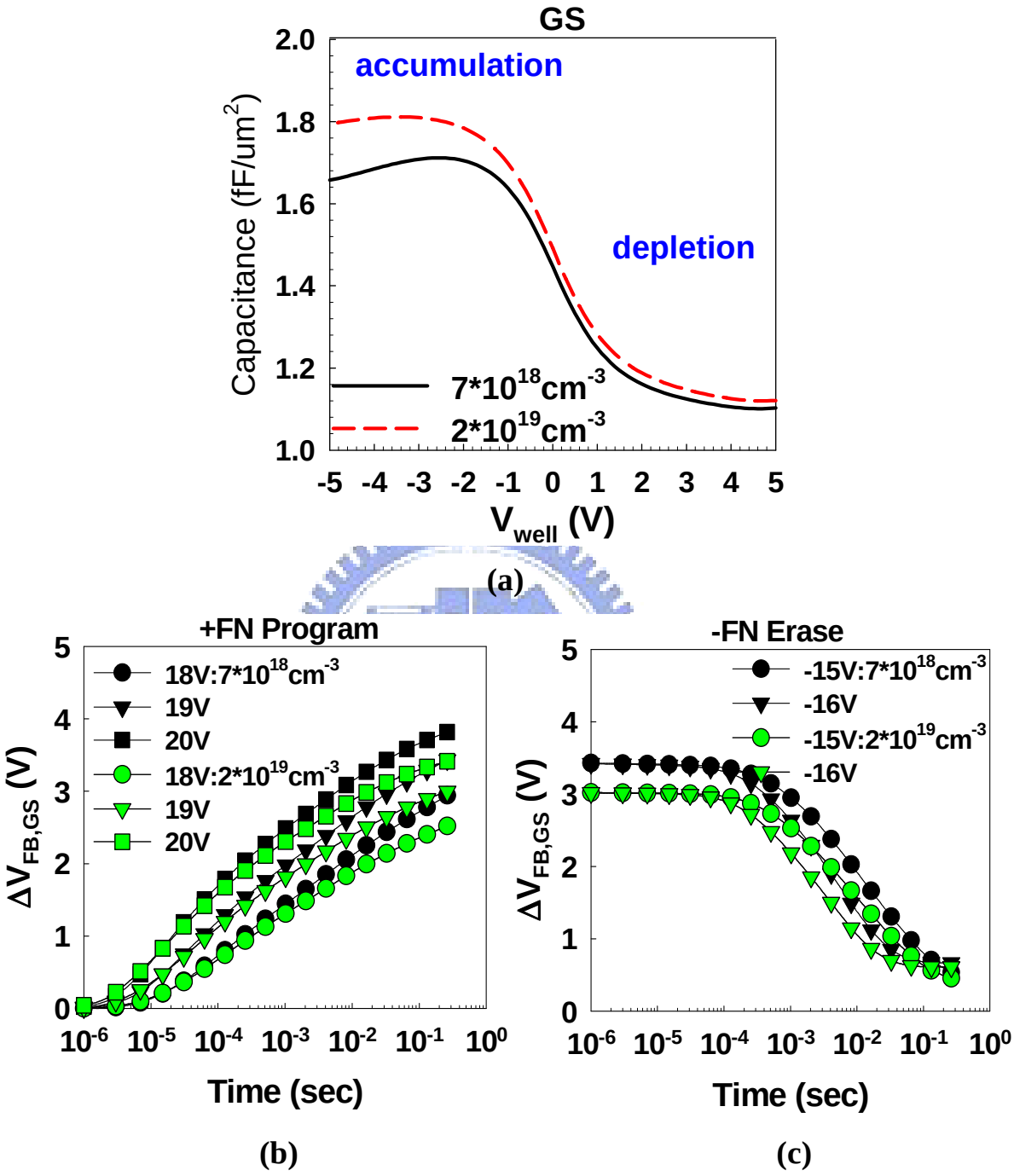


Fig. 3.13 Comparison of GS capacitors (BE-SONOS, ONONO = 13/20/25/70/90Å) with different well doping concentrations. (a) CV curves. (b) $\Delta V_{FB,GS}$ during +FN programming. (c) $\Delta V_{FB,GS}$ during –FN erasing. The more heavily doped well has slower program speed but keeps the same erase speed.

CHAPTER FOUR

GSCS METHOD APPLICATIONS:

STUDY OF THE TRAPPED CHARGE VERTICAL LOCATION AND CAPTURE EFFICIENCY

OUTLINE

4.0 Introduction

Next, we will introduce the applications of GSCS method. In this chapter, we first discuss the trapped charge vertical locations of various SONOS-type devices and the charge capture efficiency of different SONOS structures. Morevoer, our method can also be used to demonstrate where injected charges are trapped (bulk traps or interface traps).

4.1 Charge Vertical Locations of Various SONOS-type Devices

In this section, we will investigate the mean vertical locations of various SONOS-type deivces, including SONOS, BE-SONOS, SONS (SONOS without T.O.), SNOS (SONOS without B.O.), and SNS (SONOS without B.O. and T.O.).

4.1.1 Charge Vertical Locations of SONOS and BE-SONOS

Following the same procedures as mentioned in section 3.2.3., we can extract the x-Q plots of various SONOS and BE-SONOS by using Eqs. (3-3) and (3-4), and the results are shown in Fig. 4.1. Figure 4.1(a) is SONOS with ONO = 54/70/90Å, Fig. 4.1(b) is SONOS with ONO = 70/95/75Å, Fig. 4.1(c) is BE-SONOS with ONONO = 15/20/25/70/90Å, and Fig. 4.1(d) is SONOS with ONO = 20/70/90Å. The results indicate that the x-Q plots for all devices are very similar, irrespective of different nitride thickness and tunnel dielectric. The charge centroid first starts from the nitride bottom interface, and then migrates toward the center of nitride. Although the final charge centroid is close to the center of nitride, there are two possibilities for trapped charge distribution. One is the trapped charges are located at oxide/nitride interfaces, and the other is the trapped charges are distributed inside the bulk nitride. Since our results show the final charge centroids are similar for all devices with a wide range of compositions, we speculate that injected electrons are mainly distributed inside the bulk nitride.

4.1.2 Charge Vertical Locations of SNOS and SONS

In order to further explore the trapped charge location, we particularly fabricated SONS and SNOS, where only one interface of oxide and nitride is present.

Figures 4.2 and 4.3 show the x-Q plots of SNOS devices with NO = 70/90Å and 60/75Å, respectively. SNOS structure has only one interface between T.O. and nitride. If the injected charges are mainly trapped at oxide/nitride interfaces, the charge centroid of SNOS should be very close to the T.O./nitride interface. However, the results in Fig. 4.2 and 4.3 show that the charge centroids are away from the T.O./nitride interface. This is a clear proof that injected charges are mainly trapped at bulk traps. On the other hand, compared Fig. 4.3 with Fig. 4.2, we find that when nitride thickness is thinner (as well as oxide thickness), the charge centroid of SNOS is closer to the T.O./nitride interface. Although this can be interpreted as evidence that the interface still plays a role, however, the argument is equivocal since the distance traveled by electrons (Fig. 4.3) is approximately the same as in the thicker sample (Fig. 4.2). In any case, the charge centroid is still completely within the nitride, and bulk nitride still contributes dominantly in charge trapping.

Figure 4.4(a) shows the ΔV_{FB} of SONS (ON = 54/70Å) during +FN programming. The GS and CS capacitors show significantly different behaviors. The GS capacitor initially shows hole injection ($\Delta V_{FB} < 0$), and then at longer programming time shows electron injection finally ($\Delta V_{FB} > 0$). On the other hand, CS capacitor always shows electron injection ($\Delta V_{FB} > 0$). The extracted Q-t and x-t curves based on Fig. 4.4(a) are shown in Fig. 4.4(b) and (c), respectively. Q-t in Fig. 4.4(b) shows that the SONS device initially traps holes, but finally traps electrons. On the other hand, x-t in Fig. 4.4(c) shows that the charge centroid initially locates at the center of nitride, but moves above the nitride after longer programming. However, the out of range of charge centroid does not mean that the charges are inside the T.O. Since there are electron injection from Si-sub and hole injection from poly gate simultaneously, the Eq. (3-4) for mean vertical location calculation in bulk trap model

becomes invalid. Therefore, we proposed other two-region approximation model to solve this problem. Using two-region approximation model, we can monitor the charges in the top portion and bottom portion of nitride separately.

4.1.3 Two-region Charges of SONS and SNS

Based on the two-region approximation model, we can calculate the charges in the bottom portion (Q_1) and top portion (Q_2) of nitride by using Eqs. (3-9) and (3-10). The extracted results of SONS (ON = 54/70Å) are shown in Fig. 4.5(a). The results indicate a simple fact that the bottom portion traps electrons while the top portion traps holes. The reason of hole trapping under +FN programming can be easily understood since the nitride has a low barrier for hole (~ 2eV), it can therefore induce gate hole injection during +FN programming. Therefore, for SONS (ON = 54/70Å) electrons are injected from the channel while holes are injected from the poly gate simultaneously. Since holes ($Q < 0$) are inside the top portion of nitride while electrons ($Q > 0$) are inside the bottom portion of nitride, then the net charge centroid can be outside of nitride (A simple arithmetic example is: $Q_2 = -2\times10^{12}$ at $¾T_N$ and $Q_1 = +1\times10^{12}$ at $¼T_N$, then $Q_{tot} = -1\times10^{12}$ and $x = 1.25T_N$). In this situation, the two-region approximation model (Q_1 and Q_2) gives a clearer understanding of the detailed trapped charge behaviors rather than bulk trap model (Q and x). It should be mentioned that these two models, Eqs. (3-3)~(3-4) and Eqs. (3-9)~(3-10), are mathematically equivalent and can be transformed to each other.

We also applied two-region approximation model to SNS, as illustrated in Fig. 4.5(b). SNS does not provide any oxide/nitride interfacial traps, and therefore bulk traps dominate. Moreover, there is also hole injection from poly gate due to the absence of T.O. The results show that the bottom portion of nitride traps electrons while the top portion traps holes. These results are similar to SONS. The hole trapping in SONS or SNS during +FN injection can only be detected by the GS capacitor. This is because the hole trapping occurs near the poly

gate, and the gate coupling ratio in CS capacitor approaches to zero. Therefore, the conventional CS capacitor can hardly detect it (channel sensing is more sensitive to the bottom portion of nitride). Through our novel gate sensing measurement, this phenomenon now can be studied successfully.

4.2 Capture Efficiency of Various SONOS-type Devices

After discussing the charge vertical locations of different SONOS-type devices, we next investigate the capture efficiency of nitride trapping layer. Since our GSCS method can accurately extract the total trapped charges vs. time (Q-t) curve, we can examine the electron capture efficiency by comparing the theoretical and experimental Q-t plots.

4.2.1 Theoretical Q-t model

The theoretical Q-t curves can be calculated by the time integration of FN tunneling current. Our model also includes the effect of e-field change after the charges are injected into the nitride. If the injected charges are fully captured by the nitride, the Q-t relationship can be numerically or analytically derived. The detailed mathematical formulas for numerical and analytical derivation are shown below.

(a) Numerical deviation of theoretical Q-t model

The tunneling current through the B.O. follows the FN equation:

$$J = \alpha E_{Box}^2 \exp\left(\frac{-E_C}{E_{Box}}\right) \tag{4-1}$$

where E_{Box} is the B.O. e-field, and

$$\alpha = \frac{q^3}{8\pi h \phi_B} \frac{m_0}{m_{ox}} \tag{4-2}$$

$$E_C = 4\sqrt{2m_{ox}} \frac{\phi_B^{3/2}}{3\hbar q} \tag{4-3}$$

q is the electron charge, ħ is the reduced Planck constant, ϕ_B is the barrier height of oxide for electron tunneling, m_0 is the mass of a free electron, and m_{ox} is the effective mass of an electron in the oxide. The B.O. e-field can be written as:

$$E_{Box} = \frac{V_G - \Delta V_{FB,CS}}{EOT} \tag{4-4}$$

The $\Delta V_{FB,CS}$ can be derived by an iteration method:

$$\Delta V_{FB,CS}^{(i+1)} = \Delta V_{FB,CS}^{(i)} + \delta t \times J \times C_q^{-1} \tag{4-5}$$

where δt is the time interval used in the iteration, and C_q is the capacitance between charge centroid to gate by assuming the charge centroid is located at center of nitride.

$$C_q = \frac{\varepsilon_0 \varepsilon_{ox}}{T_{Tox} + \frac{\varepsilon_{ox}}{\varepsilon_N}\frac{T_N}{2}} \tag{4-6}$$

Therefore, the total injected charge Q can be calculated from Eq. (4-5) according to

$$Q = C_q \cdot \Delta V_{FB,CS} \tag{4-7}$$

(b) Analytical deviation of theoretical Q-t model

By combining Eqs. (4-1, 4-4, and 4-7), we can obtain a differential equation:

$$\frac{dQ(t)}{dt} = J = \alpha \left(\frac{V_G - Q(t)/C_q}{EOT} \right)^2 \exp\left(\frac{-E_C}{\frac{V_G - Q(t)/C_q}{EOT}} \right) \tag{4-8}$$

Fortunately, Eq. (4-8) has analytical solution given by:

$$Q(t) = C_q \left(V_G - \frac{E_C \cdot EOT}{\ell n\left(\exp\left(\frac{E_C \cdot EOT}{V_G} \right) + \frac{E_C \cdot \alpha \cdot t}{C_q \cdot EOT} \right)} \right) \tag{4-9}$$

Equation (4-9) satisfies the initial condition, where Q(0) = 0.

Equation (4-9) is derived by assuming fully-capturing property. On the other hand, if charges are not fully captured, then Eq. (4-8) should be modified by:

$$\frac{dQ(t)}{dt} = R(Q(t), E_{Box}) \cdot J \tag{4-10}$$

where $R(Q(t),E_{Box})$ is the capture rate, which is a complicated function of injected charges Q(t) and tunnel oxide e-field. Equation (4-10) cannot be derived until $R(Q(t),E_{Box})$ is determined.

Using numerical or analytical Q-t model to fit our experimental data, the only required fitting parameters are the barrier height (ϕ_B) and the effective mass of the tunnel oxide (m_{ox}).

4.2.2 Capture Efficiency of SONOS with Thicker Nitride

We first investigate the capture efficiency of SONOS devices with thicker nitride thickness (> 70Å), and the fitting Q-t results are shown in Fig. 4.6. All the Q-t plots can be consistently fitted by almost identical parameters, with barrier height ranges from 3.07 to 3.11eV while effective mass is $0.45m_0$. The experimental data and the theoretical curves show excellent consistency over a wide range of various SONOS devices. Moreover, the barrier height and effective mass are very close to the well-known tunnel oxide properties [4.1-4.2]. This is not a coincidence but rather a clear indication that most of the injected electrons are captured by the nitride since anything less would have caused significant discrepancies.

However, it is observed that at very high injection level ($Q > 10^{13}$electron-cm^{-2}), the experimental Q becomes slightly smaller than the theoretical value. This may suggest that the capture efficiency has some degradation at higher injection level. However, $Q < 10^{13}$electron-cm^{-2} is a typical injection density for most practical applications. This suggests that the capture efficiency for N > 70Å is sufficient for non-volatile memory applications.

4.2.3 Capture Efficiency of SONOS with Various Nitride Thickness

We can use the same oxide parameters $m_{ox} = 0.45m_0$ and $\phi_B = 3.1$eV to analyze the capture efficiency of other SONOS devices with thinner nitride thickness (35Å and 20Å), as illustrated in Fig. 4.7(a) and (b). The results of SONOS with N = 35Å in Fig. 4.7(a) show that

the experimental Q-t has substantial discrepancy from the theoretical model. This indicates that the capture efficiency for this sample is considerably reduced. On the other hand, for SONOS with a very thin nitride (20Å) shown in Fig. 4.7(b), the experimental Q-t is almost negligible as compared with the theoretical one.

The above results indicate that nitride capture efficiency is essentially high enough for N > 70Å, and decreases significantly when N = 35Å, and becomes negligible when N $\leqq$ 20Å. The strong dependence of electron capture rate on nitride thickness suggests that the capture process happens in bulk nitride. Fundamental understanding of electron scattering and capturing during tunneling is not well established yet, and should be an important research subject to fully understand the electron capture process.

4.2.4 Capture Efficiency of SONS and SNS

Except for the nitride thickness limitation, it should be noted that T.O. is necessary in SONOS devices to prevent charge back tunneling from gate. This statement can be further demonstrated by investigating the capture efficiency of SONS and SNS, where the T.O. is absence.

Figure 4.7(c) and (d) show the comparison of theoretical and experimental Q-t plots for SONS (ON = 54/70Å) and SNS (N = 133Å) devices, respectively, and only the electrons in the bottom portion of nitride (Q_1) are taken into account. These devices show much smaller capture efficiency even for a thick nitride (133Å). This is not because nitride does not have high capture efficiency, but because gate hole injection happens such that the injected electrons are compensated, leading to “apparent” lower capture efficiency.

4.2.5 Capture Rate Comparison of Trap-layer Engineered SONOS Devices

The high capture efficiency property of SONOS with N > 70Å suggests that trap-layer engineering cannot further increase the capture efficiency. In order to prove this effect, we

particularly fabricated various multi-layer stacks of nitride-trapping layer such as “SiON” (oxynitride) = 70Å, “SiN+SiON” (nitride at the bottom and oxynitride at the top) = 35+35Å, “SiON+SiN” (oxynitride at the bottom and nitride at the top) = 35+35Å, and “NON” = 20+25 +20Å structures for comparison.

In order to simplify the comparison, we calculate the theoretical electron injection (Q_{the}) and compare with the measured quantity (Q_{mea}). If the nitride-trapping layer is fully capturing, the slope of Q_{mea} vs. Q_{the} curve should be equal to 1. The comparison results for all above samples are shown in Fig. 4.8(a). A 70Å SiON shows comparable capture efficiency with a 70Å SiN. On the other hand, the multi-layer stacks of SiN/SiON show worse capturing property. For the special “NON” with double layers of nitride (N = 20Å), we find that the capture rate is still negligible. These results suggest that multi-layer stacks of nitride, oxynitrde, and oxide cannot further provide more efficient interfacial traps, which can capture injected charges efficiently. Moreover, the capture dynamics is not dominated by the interfacial traps, but by the bulk property of each layer. Therefore, trap-layer engineering cannot further increase the capture efficiency since a 70Å nitride already can capture most of the injected electrons.

In addition to compare the Q_{mea} vs. Q_{the} curve (in which some fitting parameters should by involved), the incremental-step-pulse programming (ISPP) behaviors also can be used to investigate the capture efficiency of SONOS devices [4.3-4.5]. Based on the fully capture assumption, we can derive that the theoretical ISPP slope should be equal to 1 [4.6]. Therefore, we also measured the ISPP characteristics and extracted the corresponding ISPP slopes of various trap-layer engineered SONOS devices, as illustrated in Fig. 4.8(b). The results are consistent with that from Q_{mea} vs. Q_{the} curves.

However, the reason why the multi-layer stacks show lower capture efficiency is not clearly understood. Although the detailed microscopic physics of trap capture process is not completely explained by this work, our results indeed provide more detailed observations on

the trapping behaviors.

4.3 Summary

In this chapter, the applications of GSCS method on trapped charge vertical location and capture efficiency were discussed in detail. GSCS method provides an accurate characterization of charge centroid and the amount of total injected charges. Moreover, through the comparison of theoretical and experimental charge densities, we could provide a rigorous evaluation of capture efficiency for various devices.

By comparisons with various SONOS, SNOS, SONS, and SNS devices, we concluded that bulk traps are the dominant traps. For SONOS structures, the electron centroid is very close to the center of nitride after longer injection. On the other hand, SNS and SONS suffer from hole injection from gate due to the absence of T.O.

We also compared the capture efficiency of various samples, we concluded that SONOS with nitride thicker than 70Å has high enough capture efficiency. On the other hand, the capture efficiency drops significantly when nitride thickness is only 35Å, and becomes negligible for a 20Å nitride.

The impact of trap-layer engineering on capture efficiency was also studied. We found that multi-layer stacks of nitride trapping layers do not create more efficient interfacial traps. This result also supports that interfacial traps are not dominant in SONOS-type devices.

Hence, our GSCS analysis provides not only new observations but also very important understanding of SONOS-type devices. It should be mentioned that this new method is also applicable to study other high-*k* materials.

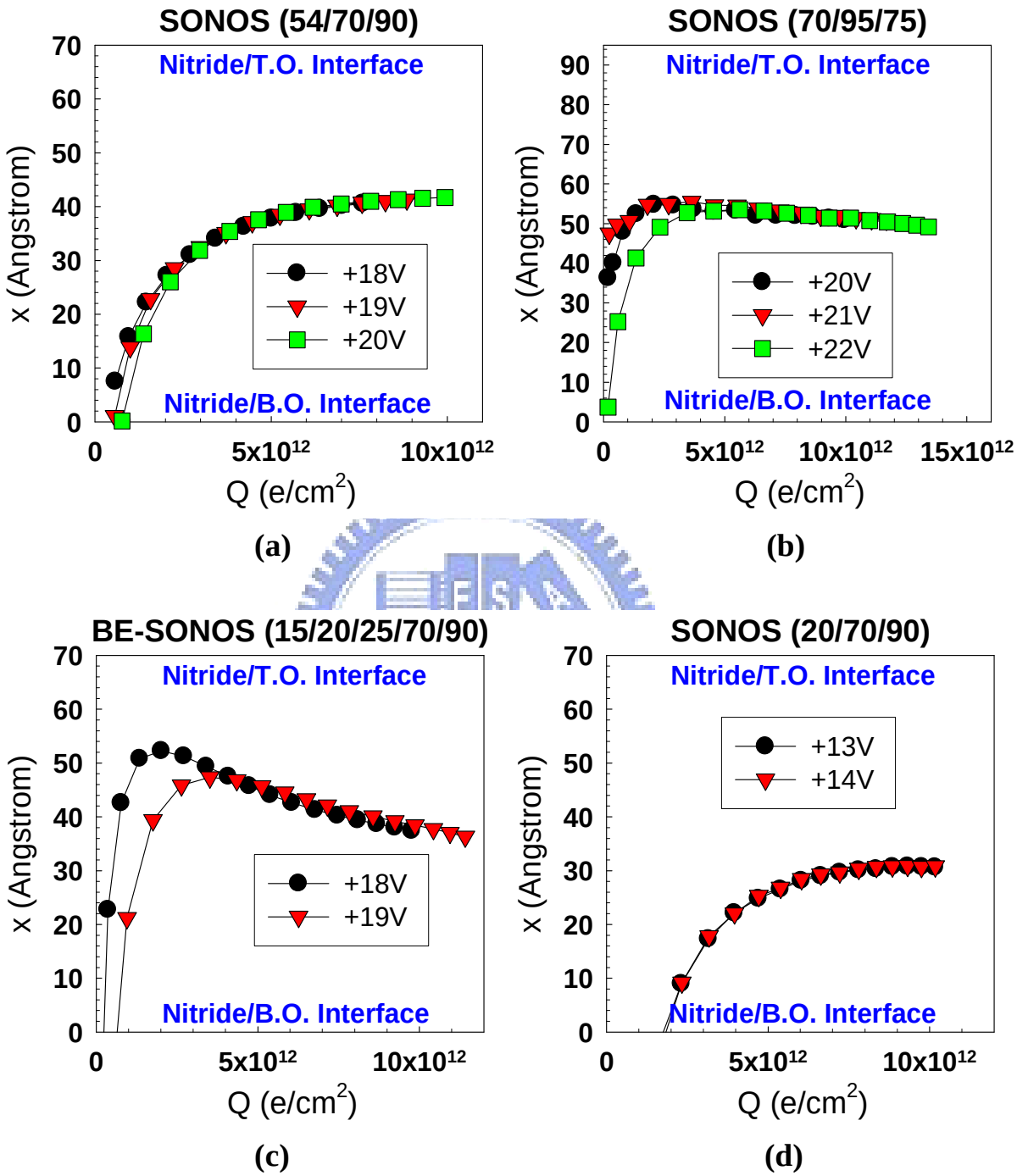


Fig. 4.1 Calculated x-Q plots for various SONOS-type devices. (a) SONOS (54/70/90Å), (b) SONOS (70/95/75Å), (c) BE-SONOS (15/20/25/70/90Å), and (d) SONOS (20/70/90 Å). The final charge centroids of all devices are close to the center of nitride.

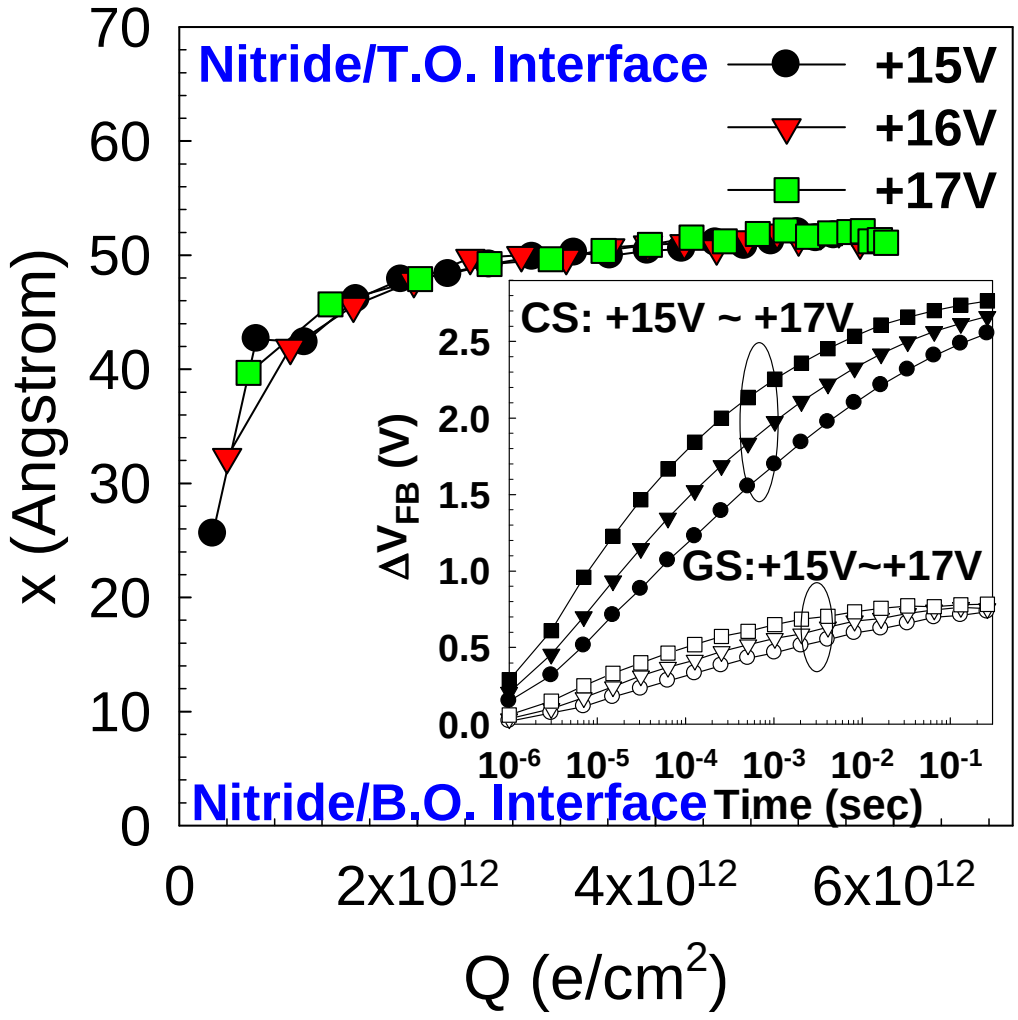


Fig. 4.2 x-Q plot (electron centroid evolution) of SNOS (NO = 70/90Å) calculated from ΔV_{FB}-t (inset).

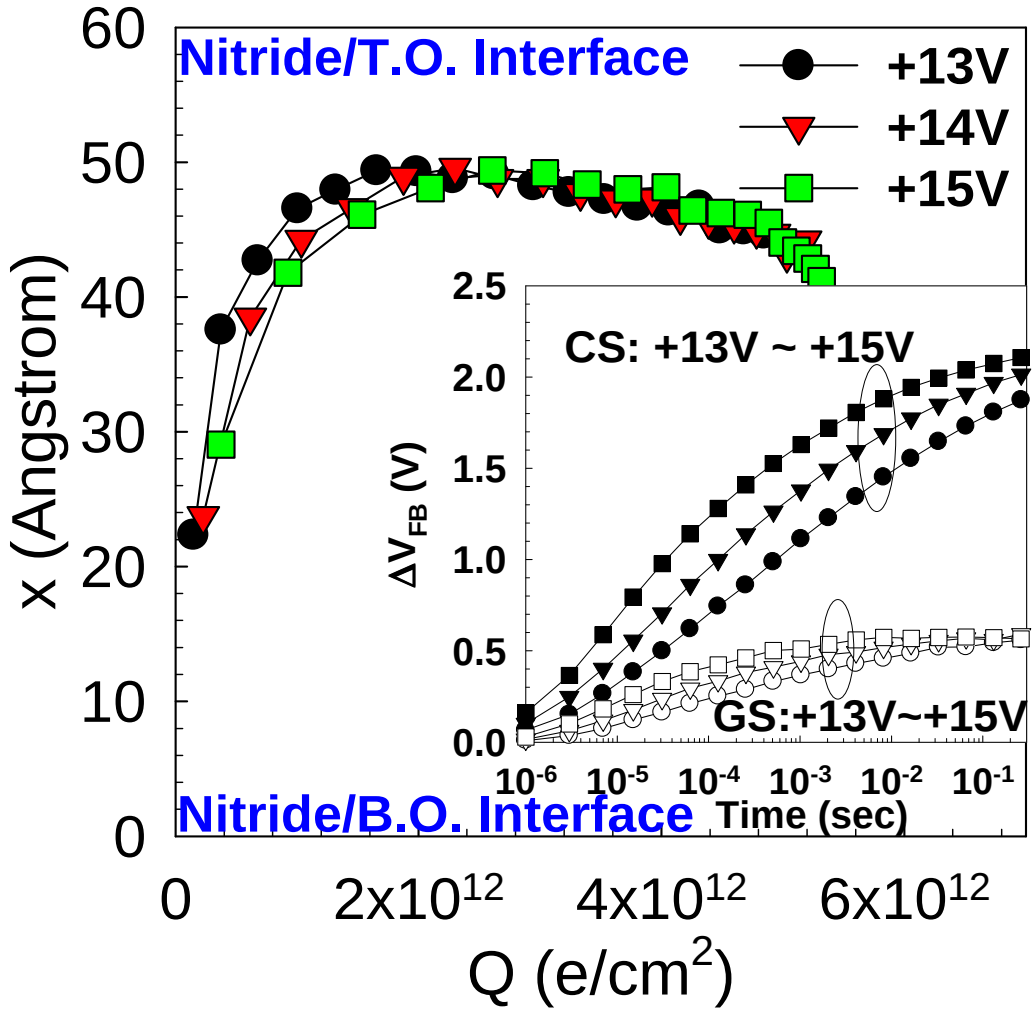


Fig. 4.3 x-Q plot (electron centroid evolution) of SNOS (NO = 60/75Å) calculated from ΔV_{FB}-t (inset). Compared with NO = 70/90Å, the electron centroid is closer to the nitride/T.O. interface.

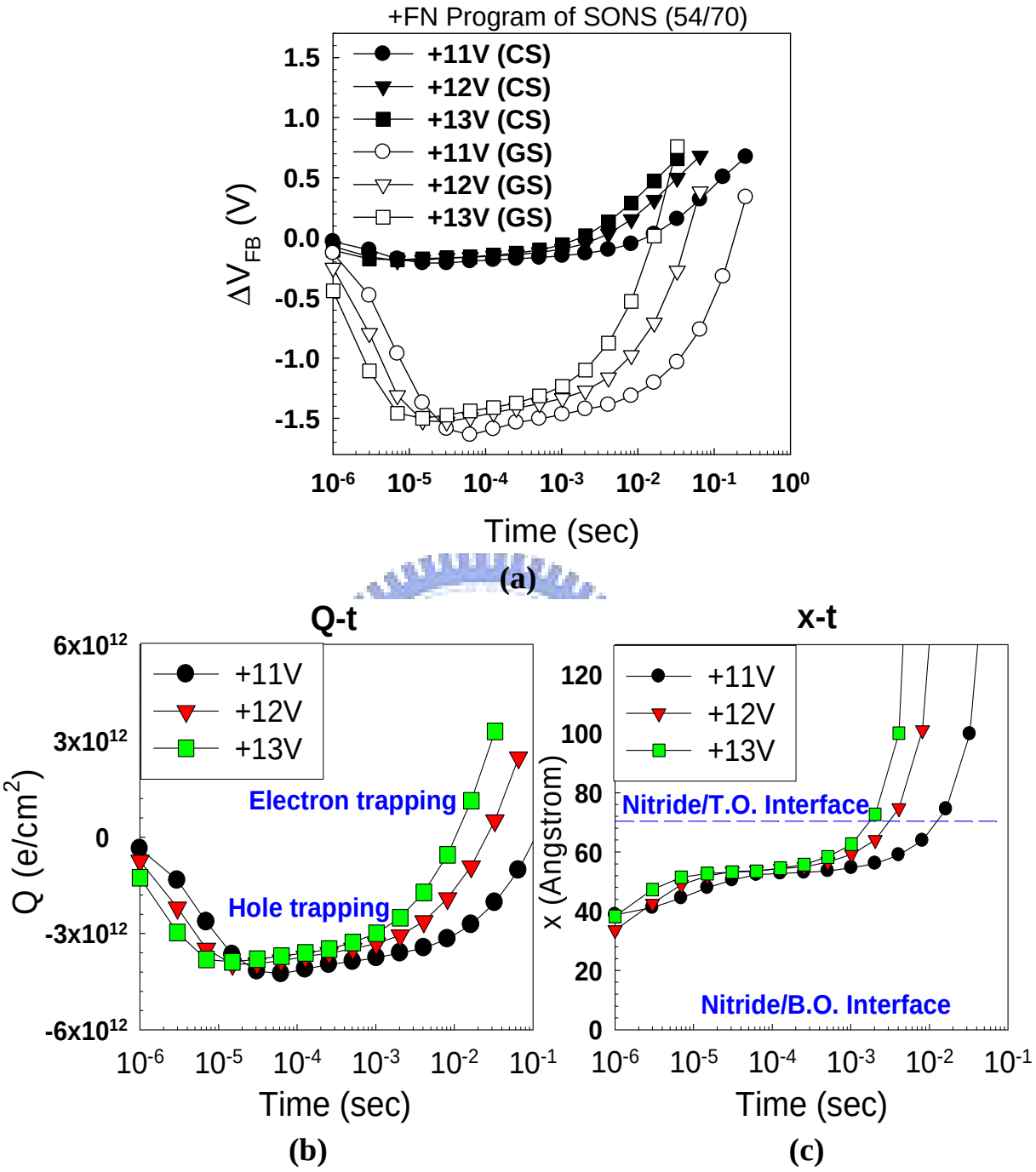


Fig. 4.4 (a) Measured ΔV_{FB} of SONS (ON = 54/70Å) during +FN programming. The GS capacitor initially shows hole injection ($\Delta V_{FB} < 0$), and then shows electron injection after longer time programming ($\Delta V_{FB} > 0$). On the other hand, CS capacitor shows only electron injection ($\Delta V_{FB} > 0$). Calculated (b) Q-t and (c) x-t from (a). The results show that initially SONS has net hole injection, but eventually becomes electron trapping. On the other hand, the charge centroid initially locates at the nitride center, but moves above the nitride afterwards.

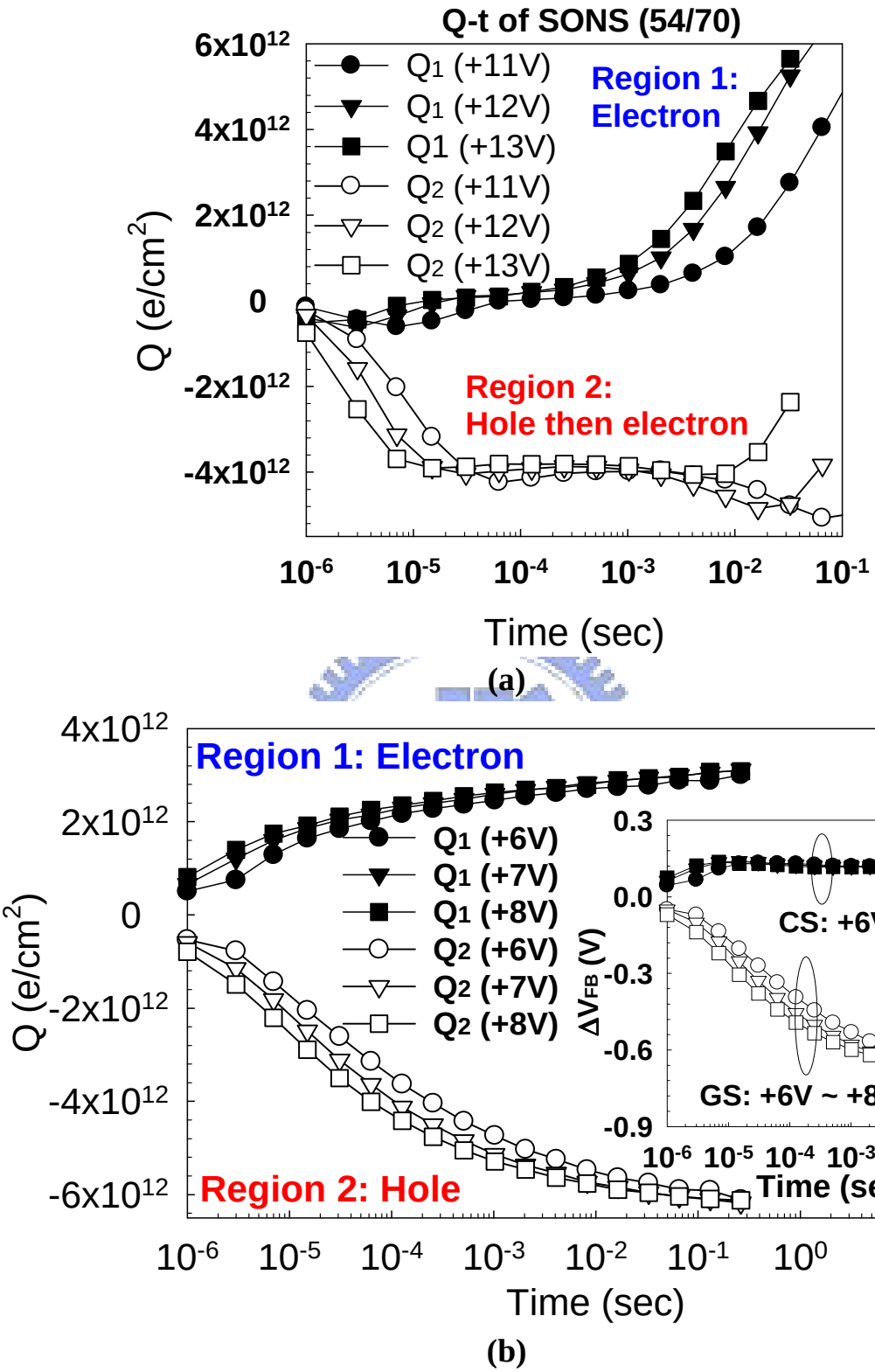


Fig. 4.5 Two-region charges (Q_1-t, Q_2-t) of (a) SONS (ON = 54/70Å) calculated from Fig. 4.4(a) and (b) SNS (N = 70Å) calculated from ΔV_{FB}-t (inset). The hole trapping in Q_2 is caused by the hole injection from poly gate because the nitride has a small hole barrier height (~ 2eV). This hole trap signal can only be detected by the GS capacitor because holes are located near the gate.

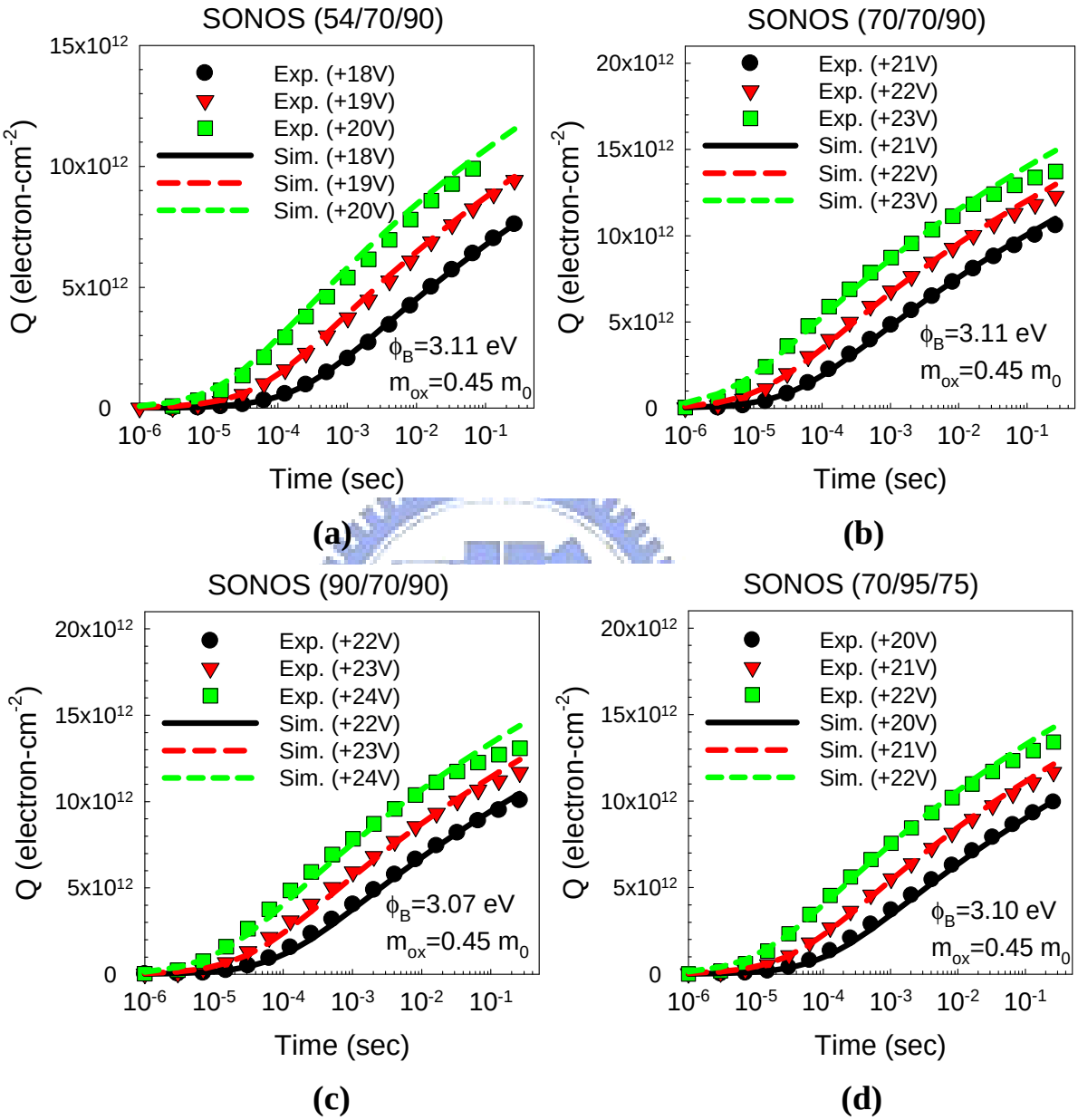


Fig. 4.6 Comparison of the theoretical and experimental injected electron densities (Q-t) for various SONOS. (a) ONO = 54/70/90Å, (b) ONO = 70/70/90Å, (c) ONO = 90/70/90Å, and (d) ONO = 70/95/75Å. All samples show excellent fit with theory, and the fitting parameters are very close. This suggests that the devices with N≧70Å have high enough capture efficiency.

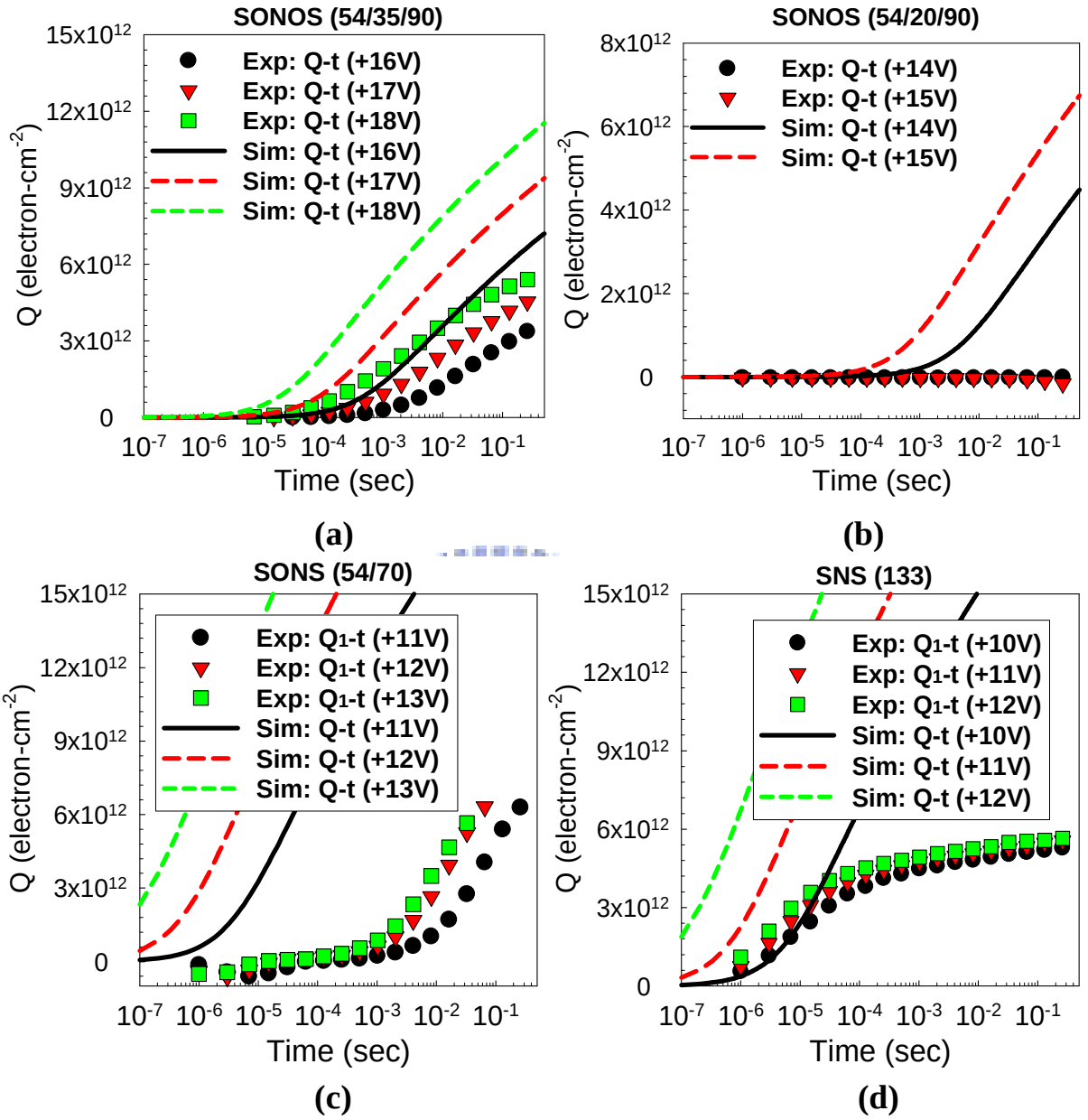
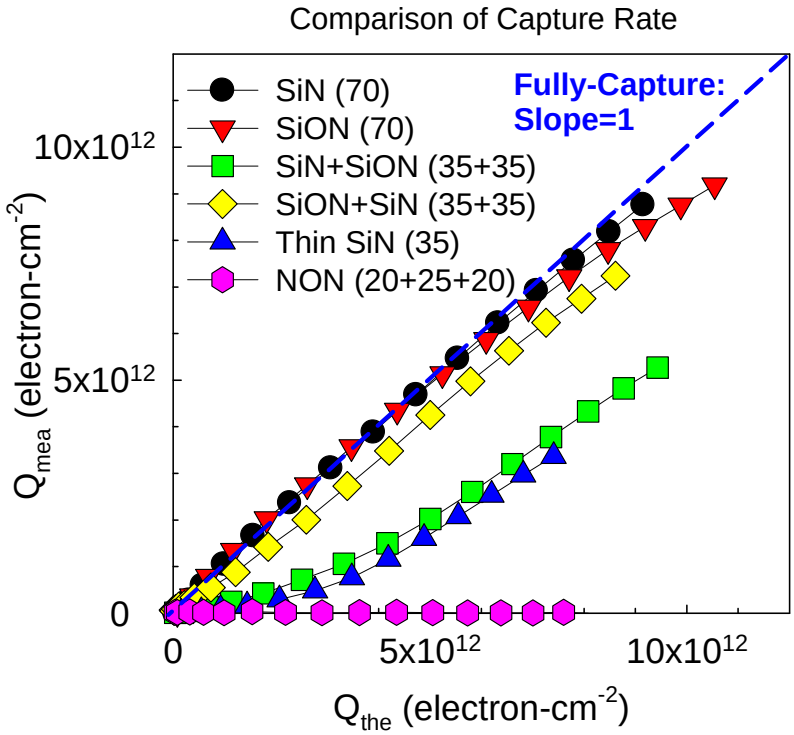
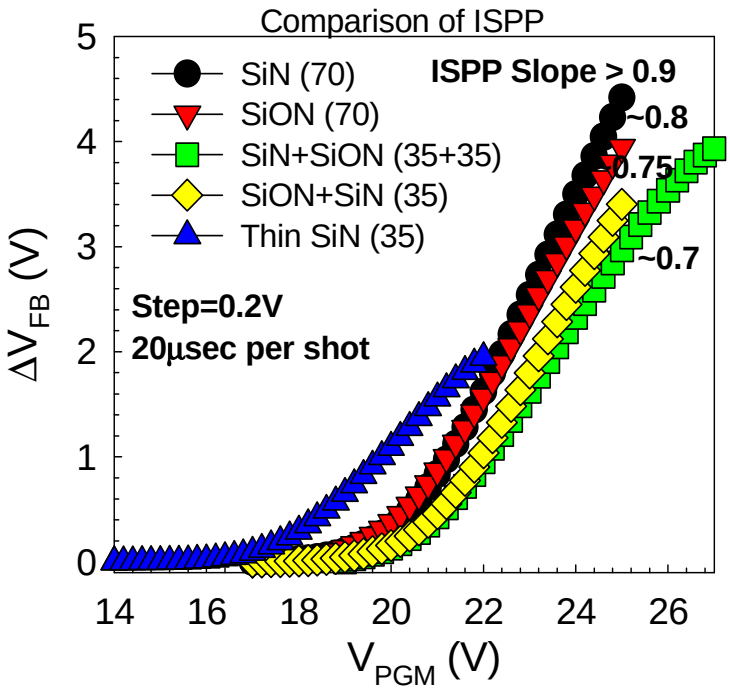


Fig. 4.7 Comparisons of the theoretical and experimental injected electron densities (Q-t) for various SONOS with thinner nitride thickness ((a) ONO = 54/35/90Å and (b) ONO = 54/20/90Å) and injected electron densities (Q_1-t) for (c) SONS (ON = 54/70Å) and (d) SNS (N = 133Å). We used 3.1eV oxide barrier height, 2.2eV nitride barrier height, and $0.45m_0$ effective mass for fitting. The results indicate the capture efficiency drops significantly for N below 35Å and becomes negligible when N is only 20Å. Moreover, the nitride without T.O. has very low "apparent" capture efficiency due to hole injection from gate.



(a)



(b)

Fig. 4.8 (a) Comparison of the theoretical (Q_{the}) and experimental (Q_{mea}) injected electron densities for various trap-layer engineered devices. SiN (70Å), SiON (70Å), SiN+SiON (35+35Å), SiON+SiN (35+35Å), SiN (35Å), and NON (20+25+20Å). The ideal fully-capturing line is also drawn. (b) Comparison of ISPP for various trap-layer engineered devices. The ideal ISPP slope for fully-capturing is 1.

CHAPTER FIVE

GSCS METHOD APPLICATIONS:

STUDY OF INTRA-NITRIDE TRANSPORT

AND RELIABILITY OF SONOS-TYPE DEVICES

OUTLINE

5.0 Introduction

The most important difference of SONOS-type devices from the floating-gate devices is that the injected charges are independently trapped inside the nitride while the injected charges are immediately spread out inside the floating gate. However, previous literatures [5.1-5.3] suggested that charges may migrate inside nitride under high-temperature baking or internal built-in e-field, and this contributes to reliability issues. Therefore, the "intra-nitride" transport is very important in understanding the detailed reliability physics of SONOS-type devices.

In this chapter, the intra-nitride transport behaviors of SONOS-type devices during programming/ erasing, cycling endurance, and reliability tests are examined extensively. Based on GSCS method, the evolution of electron and hole injection can be clearly measured. Moreover, the charge transport under high-temperature baking (from 150 to 250^{o}C), or medium field (< 5MV/cm) at room temperature is also characterized.

5.1 Charge Transport during ±FN Injection

Since the injection mechanisms of SONOS-type devices strongly depend on the tunnel oxide thickness, in this section we will investigate the charge transport of SONOS with a thicker B.O., SONOS with a thin B.O., and BE-SONOS with a tunnel ONO barrier during ±FN Injection. Different injection mechanisms in each structure are also introduced.

5.1.1 SONOS with a Thicker Bottom Oxide (+FN with Electron Injection and −FN with Electron De-trapping)

Figure 5.1(a) and (b) show the +FN program (electron injection) and $-V_G$ stress (electron de-trapping) characteristics, respectively, of SONOS with ONO = 54/70/90Å. Since the B.O. is thick, the hole injection from Si substrate can be completely blocked (due to the large barrier height for hole ~ 4.5eV). Therefore, we expect that the major erase mechanism is

electron de-trapping [5.4-5.5], and its erase speed is often very slow. Although a higher erase voltage may accelerate the de-trapping speed, gate electron injection also takes place under high e-field [5.6]. We therefore must decrease the ease voltage to below –14V to avoid the gate injection. Moreover, a very long time (200sec) is used to get sufficient ΔV_{FB}. As mentioned in section 3.2.2, the CS capacitor always has larger ΔV_{FB} since the T.O. is thicker than the B.O.

The extracted x-Q plots during +FN programming and $-V_G$ stressing are shown in Fig. 5.1(c) and (d), respectively. For +FN program, the electron centroid starts from the B.O./nitride interface, and then migrates toward the center of nitride. Next, the $-V_G$ stress can expel (de-trap) some electrons and decrease ΔV_{FB} (Fig. 5.1(b)). The corresponding x-Q in Fig. 5.1(d) shows that as Q (electron number) is decreased, the charge centroid is also shifted higher. This result is consistent with the simple intuitive model that electron de-trapping happens first from the bottom portion of nitride since out tunneling is the easiest. After longer $-V_G$ stressing, the charge centroid moves up near the nitride/T.O. interface, indicating that most of the bottom portion electrons have been expelled.

Figure 5.2 compares the $-V_G$ stress of various SONOS devices with B.O. equal to 54Å, 70Å, and 90Å. The results show similar behaviors as those for B.O. = 54Å (as Q is decreased the charge centroid is shifted higher) since electron de-trapping is the only possible mechanism for charge loss using such thick tunnel oxide. Also, Fig. 5.2 shows that at first ($Q > 9\times10^{12}e/cm^2$) the x variation becomes smaller (the slope of x-Q plot becomes gentler) for a thicker B.O. On the other hand, at long-term stressing ($Q < 9\times10^{12}e/cm^2$), the x variations are becoming identical for various B.O. thickness. This suggests that the initial de-trapping rate is insensitive to the electron vertical location in the nitride for a thicker B.O. Moreover, the long-term de-trapping rate is independent of the B.O. thickness.

5.1.2 SONOS with a Thin Bottom Oxide (+FN with Electron Injection and −FN with Hole

Injection)

For comparison, we fabricated SONOS with a thin B.O. (20Å) to offer an efficient hole direct tunneling erase. The program/erase characteristics are shown in Fig. 5.3(a) and (b), respectively. Since direct tunneling injection using an ultra-thin tunnel oxide offers much more efficient erase speed, the erase time can be much smaller (< 1sec) than that of SONOS with thicker B.O.

The extracted x-Q plots for +FN program and –FN erase are shown in Fig. 5.3(c) and (d), respectively. After +FN programming, the electron centroid also shows similar behavior as that for Fig. 5.1 (c). During –FN erasing, the charge centroid of total net charges moves upward. Although the x-Q plot in Fig. 5.3(d) is similar to Fig. 5.1(d), the detailed erase mechanisms are completely different. Figure 5.3(d) is consistent with the model that the injected holes first recombine with the trapped electrons in the bottom portion of nitride and then gradually move upward, thus causing the upward motion of the charge centroid. Moreover, the charge centroid moves even above and out of nitride after longer –FN erasing time.

Again, the above nitride charge centroid does not mean the charges are inside the T.O. This is because both holes and electrons exist inside nitride, similar to section 4.1.3. At longer erasing time, more injected holes are accumulated at the bottom portion of nitride while some electrons still remain in the top portion of nitride. Simple arithmetic verifies that it is possible to have the net charge centroid above the nitride. (For example, $Q_e = +3\times10^{12}$ at $¾T_N$, and $Q_h = -2\times10^{12}$ at $¼T_N$, then $Q_{tot} = +1\times10^{12}$ (electron), and $x = 1¾T_N$: out of nitride). Therefore, our results clearly illustrate that the electron and hole injection have vertical mismatch inside nitride.

It should be mentioned that great care must be taken during the measurement of SONOS with such a thin tunnel oxide (20Å) to avoid gate disturb during CV measurement. Gate disturb easily happens even at a low voltage since direct tunneling is induced even at a low

e-field. Gate disturb is another reason why SONOS with a thin tunnel oxide has very poor reliability and is unsuitable for most practical applications. In order to minimize the gate disturb, we limit the V_G sweeping range to be only V_{FB}±1V during CV measurement. During testing, the V_G-sweeping range automatically changes when V_{FB} is shifted during programming/erasing. This minimizes the tunnel oxide e-field during measurement, hence suppresses the gate disturb. We also apply the same measurement methods for the SNS, SONS, and SNOS devices in chapter 4.

5.1.3 BE-SONOS with an Ultra-Thin ONO Barrier (+FN with Electron Injection and −FN with Hole Injection)

We also measure the erase characteristics of BE-SONOS (13/20/25/70/90Å), as shown in Fig. 5.4(a). The ultra-thin ONO barrier in BE-SONOS can offer efficient hole tunneling erase at high e-field while eliminate the direct tunneling leakage at low e-field [5.7]. Therefore, the erase speed of BE-SONOS is competing with SONOS with a thin tunnel oxide (Fig. 5.3(b)). The extracted Q-t, x-t, and x-Q plots during erasing are shown in Fig. 5.4(b) and (c). Similar to SONOS with thin tunnel oxide (Fig. 5.3(d)), the injected holes first recombine with the bottom electrons and then move upward.

In order to further understand the hole injection profile, we plot the hole centroid during injection. The mathematical formulation is simple. We assume that the previous injected electrons are fixed during –FN erasing, therefore, we can subtract their contribution from the as-programmed condition, and then transform $V_{FB,CS}$ and $V_{FB,GS}$ into the hole charge density (Q_h) and hole mean vertical location (x_h). The detailed derivation of Q_h and x_h is shown in Appendix E. The calculated results are shown in Fig. 5.5. Similar to the electron injection, hole centroid also starts at the bottom interface and then migrates upward. For different erase voltages, the x_h-Q_h curves are merged together, which suggests that the x_h-Q_h plot describes the trajectory of hole injection. Compared with Fig. 4.1(c), the hole centroid (~ 20Å) is

considerably lower than the electron centroid (~ 35Å). Thus, after –FN erasing the hole and electron centroids are still unmatched.

5.2 Charge Transport during FN Cycling

Since there is electron and hole vertical mismatch after –FN erasing, which may cause some reliability issues, we next investigate this impact on the P/E cycling endurance. Figure 5.6(a) shows the example of a 10K P/E cycling test of BE-SONOS (15/20/25/70/90Å). BE-SONOS shows excellent cycling endurance. The corresponding x and Q are calculated in Fig. 5.6(b). After +FN programming, the total net charge Q (electrons) increases, and the charge centroid x is close to the center of nitride. After –FN hole injection, total net charge Q (still more electrons since Q > 0) decreases, and the charge centroid x shifts higher. Moreover, at the initial few P/E cycles, the Q and x are slightly varied after P/E cycling, but then soon becomes very stable after many P/E cycling.

Therefore, this mismatch in electron and hole centroids should not be interpreted as accumulation of electrons in the upper portion and holes in the lower portion of nitride, respectively. During P/E cycling, most trapped electrons (holes) are neutralized by the erasing holes (programming electrons). This well explains our observation that Q and x stay unchanged through many P/E cycling. For example, after the (n-1)-th erasing there is a residual population of electrons in the upper portion of the nitride and a population of holes in the lower portion of nitride, and the total charge (Q) is low. During the n-th programming most of the holes are neutralized and the electron distribution is the same as that after the (n-1)-th programming. Similarly, the hole distribution after the n-th erasing is the same as that after the (n-1)-th. Therefore, the mismatch of the electron and hole centroids should be viewed as a snapshot of erased state, and should not be interpreted as two separate pockets of charges co-inhabiting the nitride.

5.3 Charge Transport during High-Temperature Baking

After discussing the charge transport during ±FN operations and FN cycling endurance test, we next investigate the charge transport during short-term (< 1 day) and long-term (> 1 day) high-temperature baking. In addition to charge loss, the intra-nitride transport behaviors are also introduced.

5.3.1 Baking Characteristics of SONOS and BE-SONOS

The 200°C and 250°C baking characteristics of SONOS (54/70/90Å) and BE-SONOS (15/20/25/70/90Å) are shown in Fig. 5.7(a) and (b), respectively. The devices are first programmed by +20V 0.26sec before high-temperature baking. For SONOS, the CS capacitor shows slightly V_{FB} gain while GS capacitor shows slightly V_{FB} loss within 1 day baking. The extracted Q and x are shown in Fig. 5.7(c) and (d). For SONOS, there is almost no real charge loss after baking for ~ 1 day (Q is unchanged), but there is a significant decrease in the charge centroid (x). Therefore, the V_{FB} shift must be caused by trapped electrons move to lower portion of nitride. This is an evidence of intra-nitride transport. However, after long-term baking (> 1 day), significant real charge loss is observed (Q is decreased) while x shifts higher. This indicates that electrons mainly de-trap from the bottom portion of nitride after long-term baking. Since the B.O. of SONOS is thick enough to block the trap to band tunneling and the amount of charge loss increases as the rising temperature, we speculate that this charge loss comes from thermal emission [5.8]. The higher the baking temperature, the more significant charge loss and x shift (temperature dependent de-trapping rate). BE-SONOS also shows similar behaviors as SONOS. However, in the first day of baking, we observe both intra-nitride transport and charge loss simultaneously. This may due to BE-SONOS have more staring stored charges that build a higher internal e-field and cause more charges loss.

It is interesting to note that the x-Q plots in Fig. 5.7(d) are very similar for different baking temperatures, implying that for electrons at location x the tunneling probability is

independent of temperature. Moreover, de-trapping is most efficient near the bottom portion of nitride since the x increases during de-trapping.

We also investigated the post-cycling baking characteristics of BE-SONOS (15/20/25/70/90Å), as shown in Fig. 5.8(a). The devices are first programmed by +19V after different P/E cycles (Fig. 5.6(a)), and then we measure the retention data at 250^{o}C. From Fig. 5.8(a), BE-SONOS shows similar retention behaviors for post-cycled and fresh devices. Within 1 day baking, the devices after P/E cycling have larger initial V_{FB} loss. However, after long-term baking, the V_{FB} loss is almost the same as the fresh state. Therefore, we conclude that the P/E cycling stress only causes more initial charge loss, but it has no effect on the long-term retention characteristics.

The extracted Q-t, x-t, and x-Q are shown in Fig. 5.8(b) and (c). At long-term baking, the Q-t and x-t of different cycle times merge together. On the other hand, the x-Q plots are very similar for different cycling times. This suggests that P/E cycling does not affect electron de-trapping trajectory at high-temperature baking.

5.3.2 Baking Characteristics of SONOS with a Thicker Nitride

In order to enhance the signal of intra-nitride transport, we have investigated the high-temperature baking retention characteristics (250^{o}C) of SONOS with a thicker nitride (O/N/O = 70/95/75Å), as shown in Fig. 5.9(a). Within 1 day baking, CS device shows obvious V_{FB} gain while GS device shows V_{FB} loss. This opposite shift of CS and GS devices clearly implies that there is intra-nitride transport inside nitride.

The extracted Q and x are shown in Fig. 5.9(b) and (c). Q is almost unchanged at $t < 10^{4}$sec while x is significantly decreased. This implies that the total charge inside nitride is unchanged, but the trapped electrons move to lower portion of nitride, i.e. intra-nitride transport. The thicker nitride shows a slightly more significant change in x compared to the

thinner nitride. The exact mechanism still needs to be examined. It should be mentioned that this intra-nitride transport is observable only at very high-temperature baking (> 200^{o}C). At lower baking temperature (150^{o}C), the intra-nitride transport behavior is very minor. Fig. 5.10(a) shows that there is no significant V_{FB} shift for both CS and GS capacitors after long-term baking. The extracted Q and x in Fig. 5.10(b) and (c) also indicates that the change is minor.

We also investigated the room temperature intra-nitride transport under low bias voltage (±5V) and long time (1×10^{5}sec) stress. We first programmed the devices to high V_{FB} states (+21V, 0.26sec), and then applied ±5V stress. The extracted Q and x are shown in Fig. 5.11. The results show that under +5V stressing (< 5MV/cm in B.O.), the Q and x are almost unchanged within 1×10^{5}sec. Moreover, under –5V stressing (> 5MV/cm in B.O.), the x is slightly decreased after 1×10^{3}sec stressing, indicating that charges inside nitride are very stable. Therefore, we conclude that charge spreading inside nitride is not the dominant retention mechanism for SONOS-type devices at lower baking temperature (< 150^{o}C) or under moderate internal e-field. Hence, nitride trap provides a very reliable charge storage material for non-volatile memory applications.

5.4 Summary

In this chapter, we could directly investigate the charge transport and intra-nitride behaviors of SONOS-type devices by using GSCS method. Using this novel method, we could monitor the charge centroid (x) and charge density (Q) during various programming/erasing and reliability tests.

Our results clearly indicate that for the electron injection (+FN program), the electron centroid migrates from the bottom interface toward the center of nitride. For the hole injection (–FN erase) in SONOS with a thin B.O. or BE-SONOS, holes first recombine with the bottom electrons and then gradually move upward. We also proved that electron and hole injection

centroids have vertical mismatch after erasing. However, this mismatch of the electron and hole centroids should be viewed as a snapshot of erased state, and should not be interpreted as two separate pockets of charges co-inhabiting the nitride. During P/E cycling, most trapped electrons/holes are neutralized by the erasing holes/programming electrons. Therefore, SONOS-type devices can still possess excellent P/E cycling endurance.

On the other hand, for the electron de-trapping processes under $-V_G$ stressing (SONOS with a thicker B.O.), the trapped electrons de-trap first from the bottom portion of nitride.

For the high-temperature retention, after short-term baking, the trapped electrons move to lower portion of nitride, and this intra-nitride transport becomes more significant for a thicker nitride. On the other hand, after long-term baking, the charge loss mainly comes from the bottom portion of nitride. It should be mentioned that the intra-nitride transport is significant only at very high-temperature baking (> 200^{o}C). The charge vertical or lateral spreading may not be the dominant retention mechanism at lower storage temperature.

In summary, our GSCS method provides numerous new observations of intra-nitride charge-trapping behaviors, which were never discovered before.

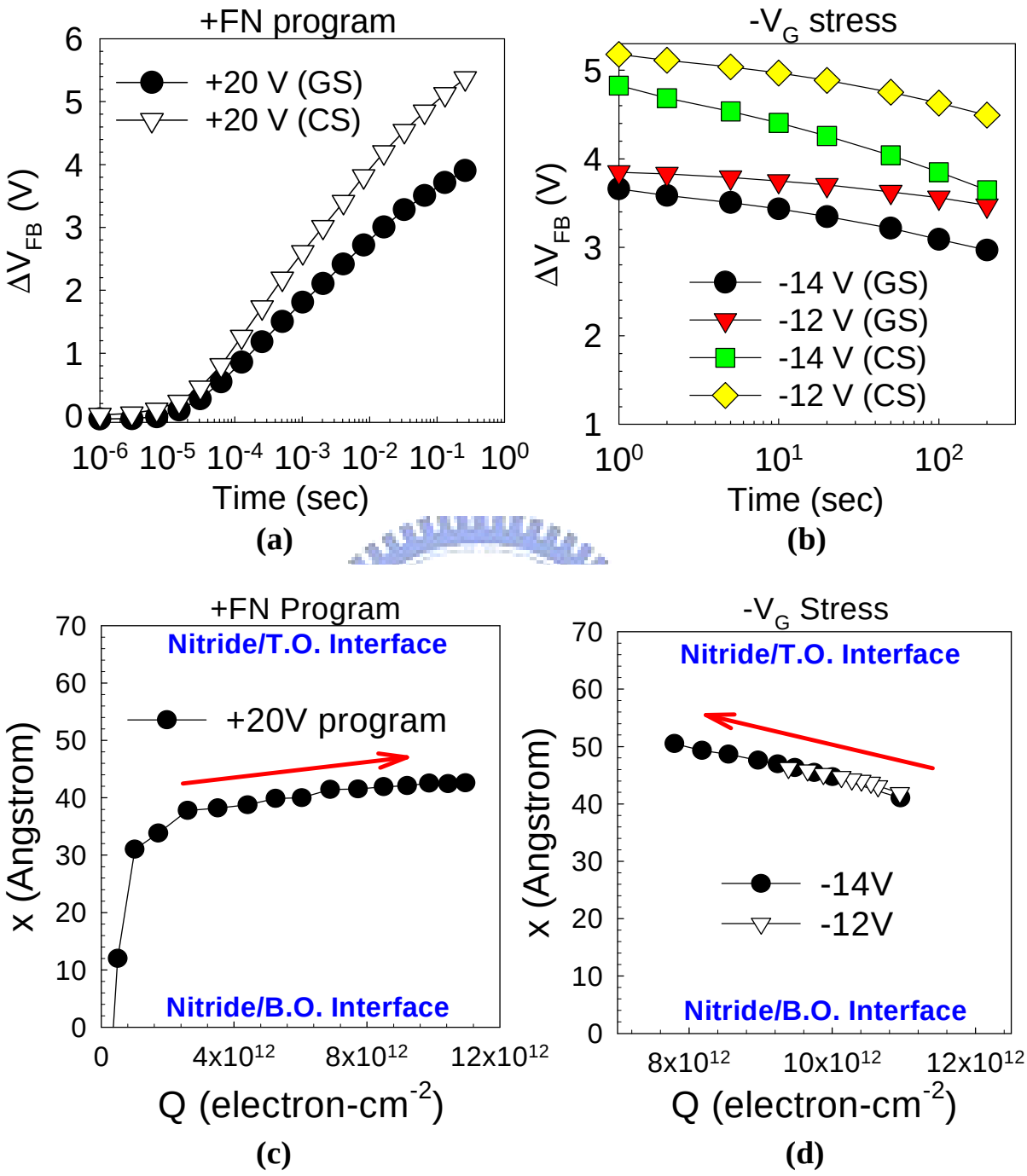


Fig. 5.1 ΔV_{FB} during (a) programming by +20V and (b) erasing by $-V_G$ stress. Calculated Q-x plots for (c) +FN program and (d) $-V_G$ stress. For electron injection (+FN), the electron centroid gradually migrates toward the center of nitride. After $-V_G$ stressing, the electron density decreases while the electron centroid moves upward. It indicates that electrons mainly de-trap from the bottom portion of nitride.

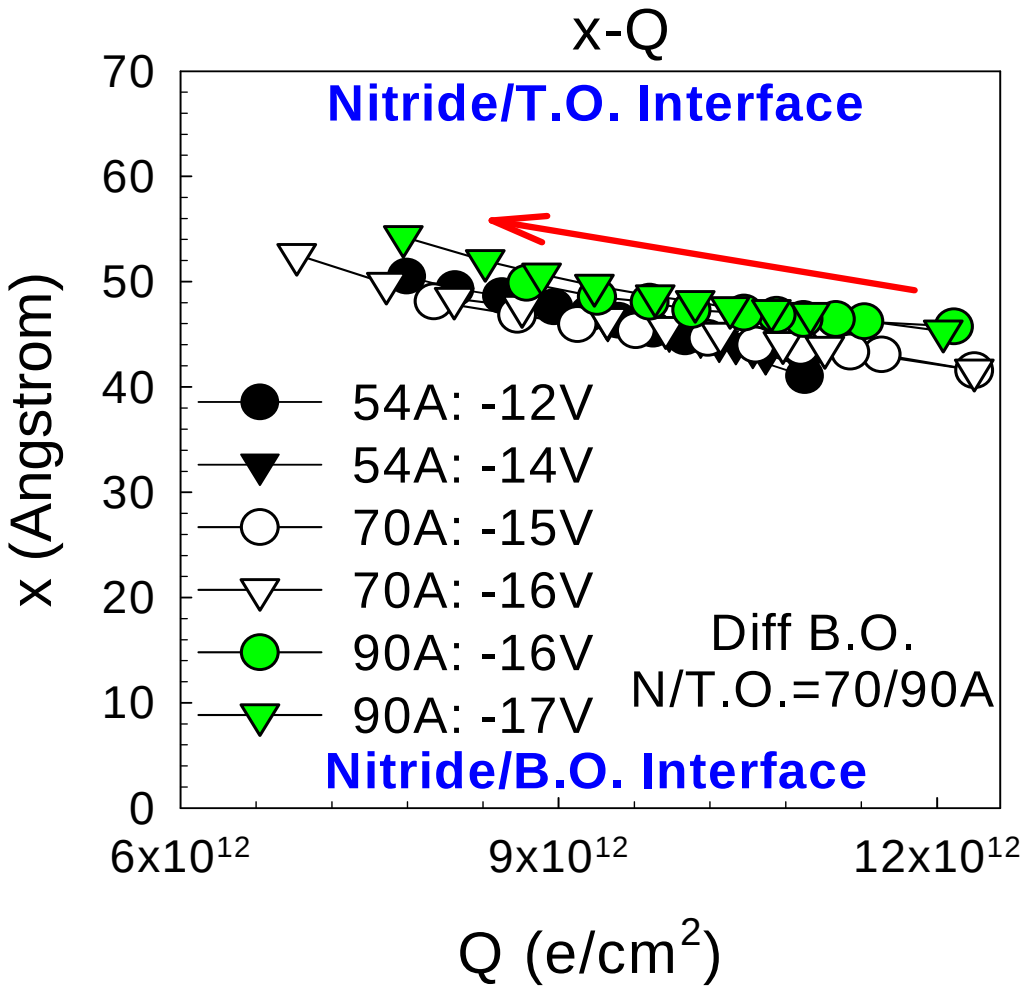


Fig. 5.2 X-Q plots of various SONOS devices (B.O. = 54Å, 70Å, and 90Å) during $-V_G$ stressing. Thicker B.O. shows less x-variation at first. At long-term stress, the x variations are becoming identical for all samples.

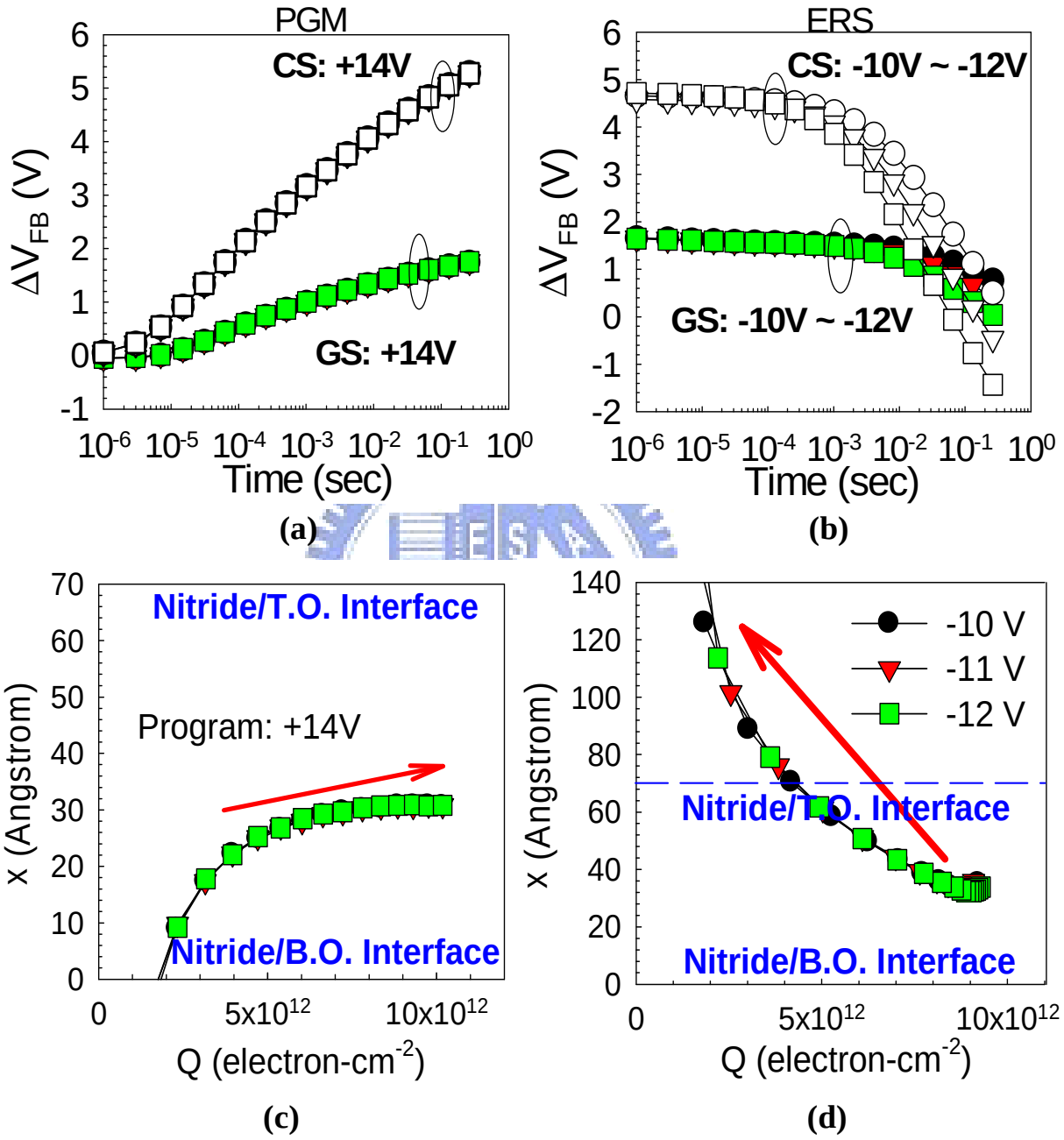


Fig. 5.3 (a) program and (b) erase characteristics of SONOS device with an ultra-thin B.O. (20Å). Calculated x-Q plots for (a) +FN program and (b) –FN erase. During –FN erasing injected holes first recombine with the bottom electrons and then gradually move upward, thus causing the upward motion of the charge centroid.

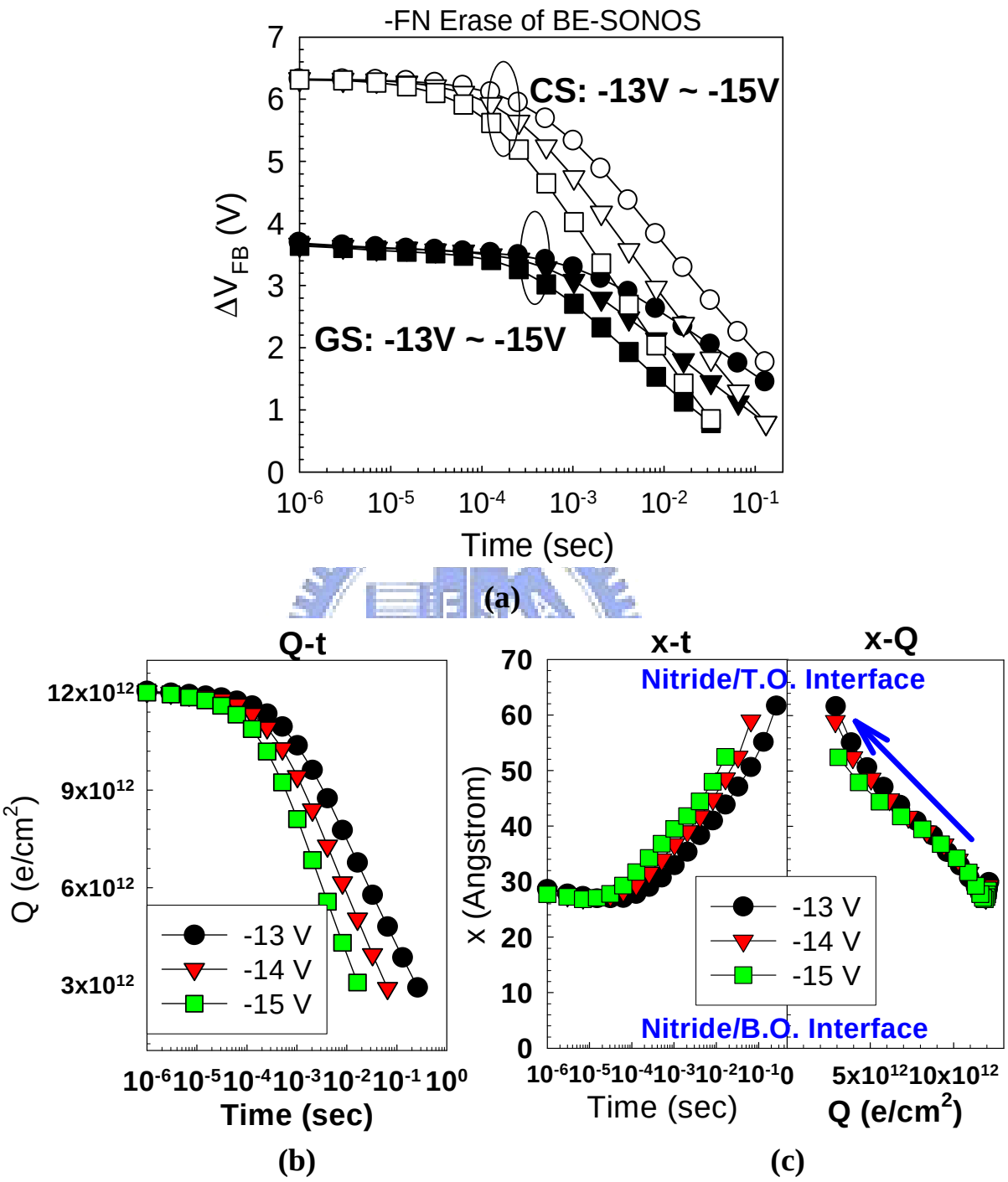


Fig. 5.4 (a) –FN hole injection characteristics of BE-SONOS (13/20/25/70/90Å). (b) Q-t and (c) x-t/x-Q plots. The x-Q plot is transformed by Q-t and x-t plots. The injected holes first recombine with the bottom electrons.

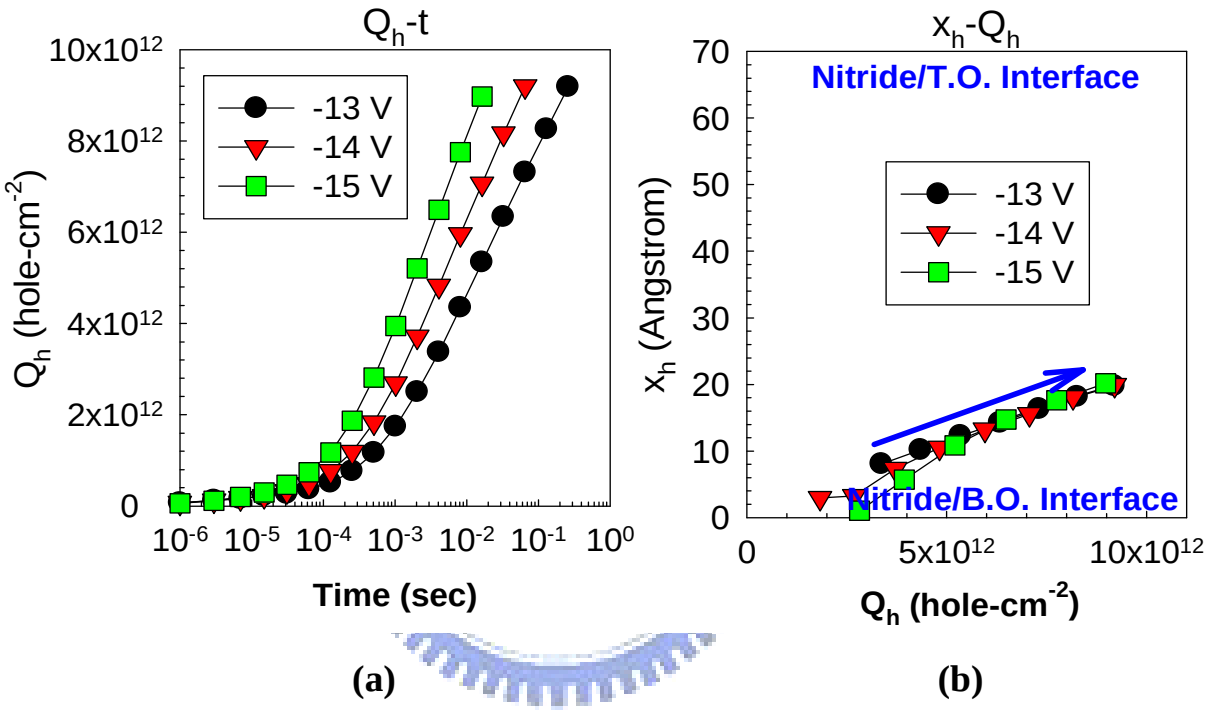


Fig. 5.5 (a) Q_h-t and (b) x_h-Q_h plots of BE-SONOS (13/20/25/70/90Å) during –FN erasing by using Eqs. (E-5, E-6). Hole centroid also starts at the bottom interface. After longer injection, it gradually migrates upward. However, its centroid is much lower than that of trapped electrons.

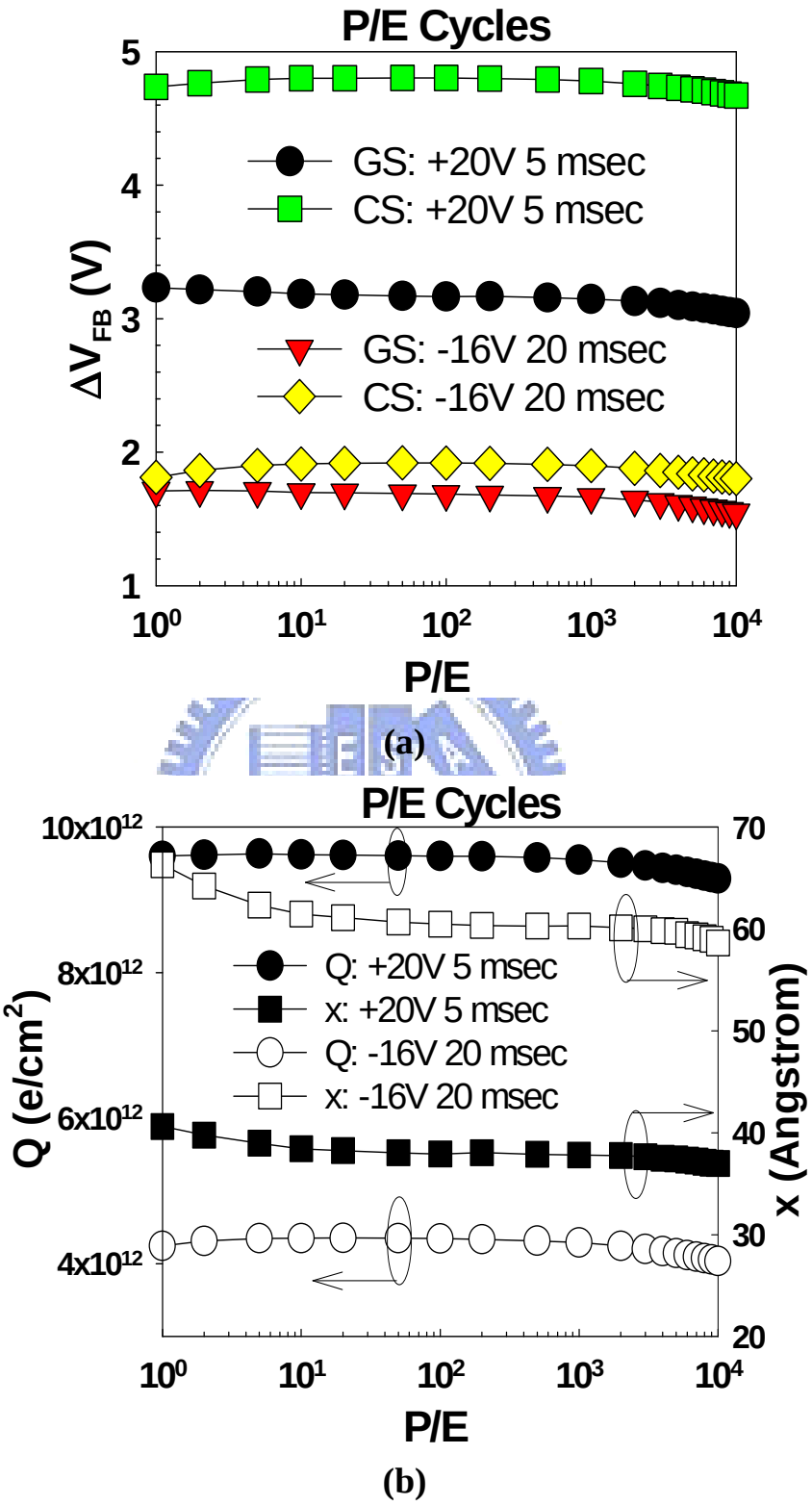


Fig. 5.6 (a) 10K P/E cycling endurance of BE-SONOS (15/20/25/70/90Å). (b) Extracted Q and x. After +FN programming, the Q (electrons) increases, and x is close to the nitride center. After –FN hole injection, Q (still more electrons since Q > 0) decreases, and x shifts higher.

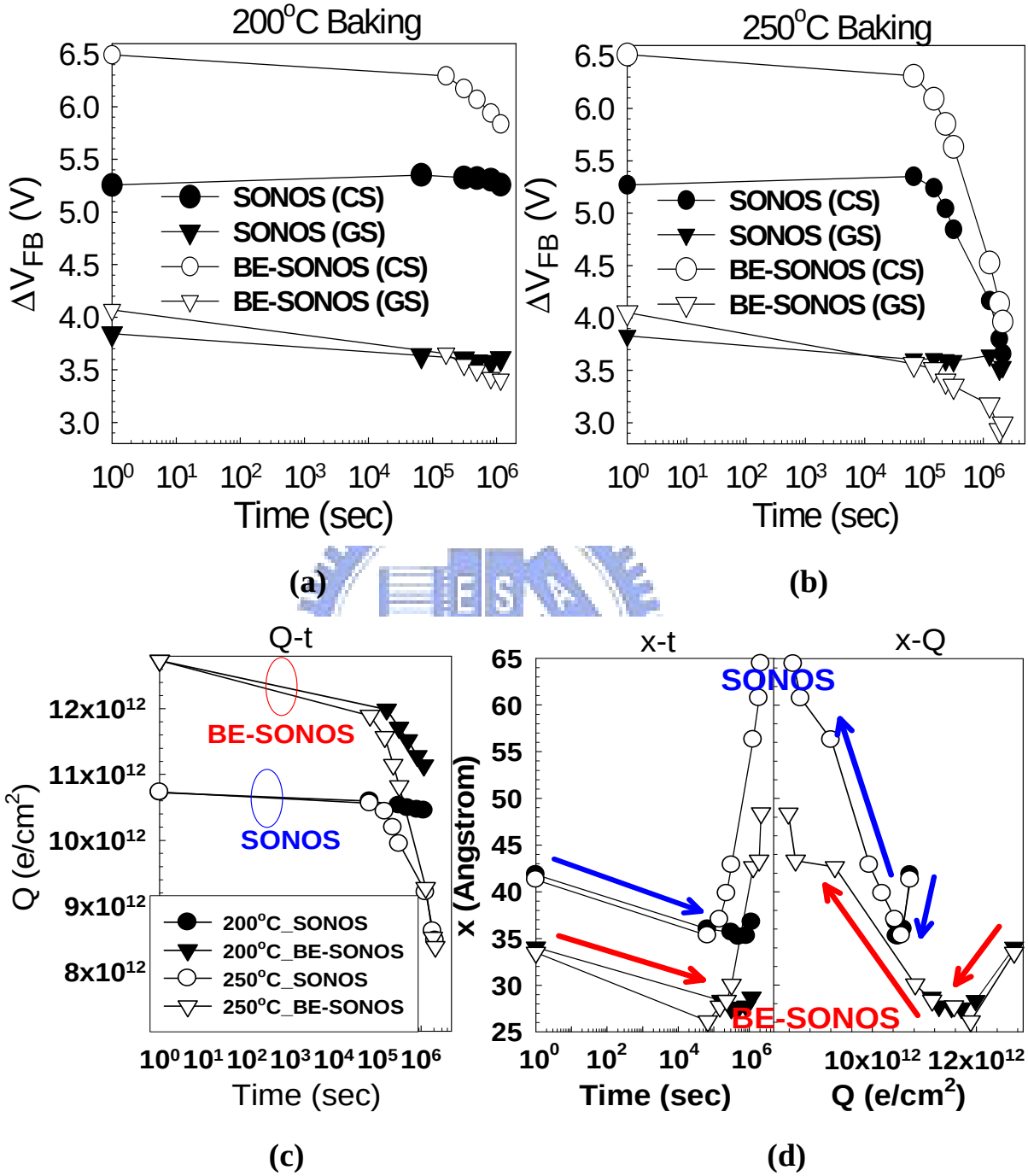


Fig. 5.7 (a) 200°C (b) 250°C baking retention of SONOS (54/70/90Å) and BE-SONOS (15/20/25/70/90Å). The device is first programmed by +20V 0.26sec before high-temperature baking. (c) Q-t and (d) x-t/x-Q plots. x first moves lower within 1-day baking, and then shifts upward after longer time baking. X-Q plots for different baking temperatures are similar.

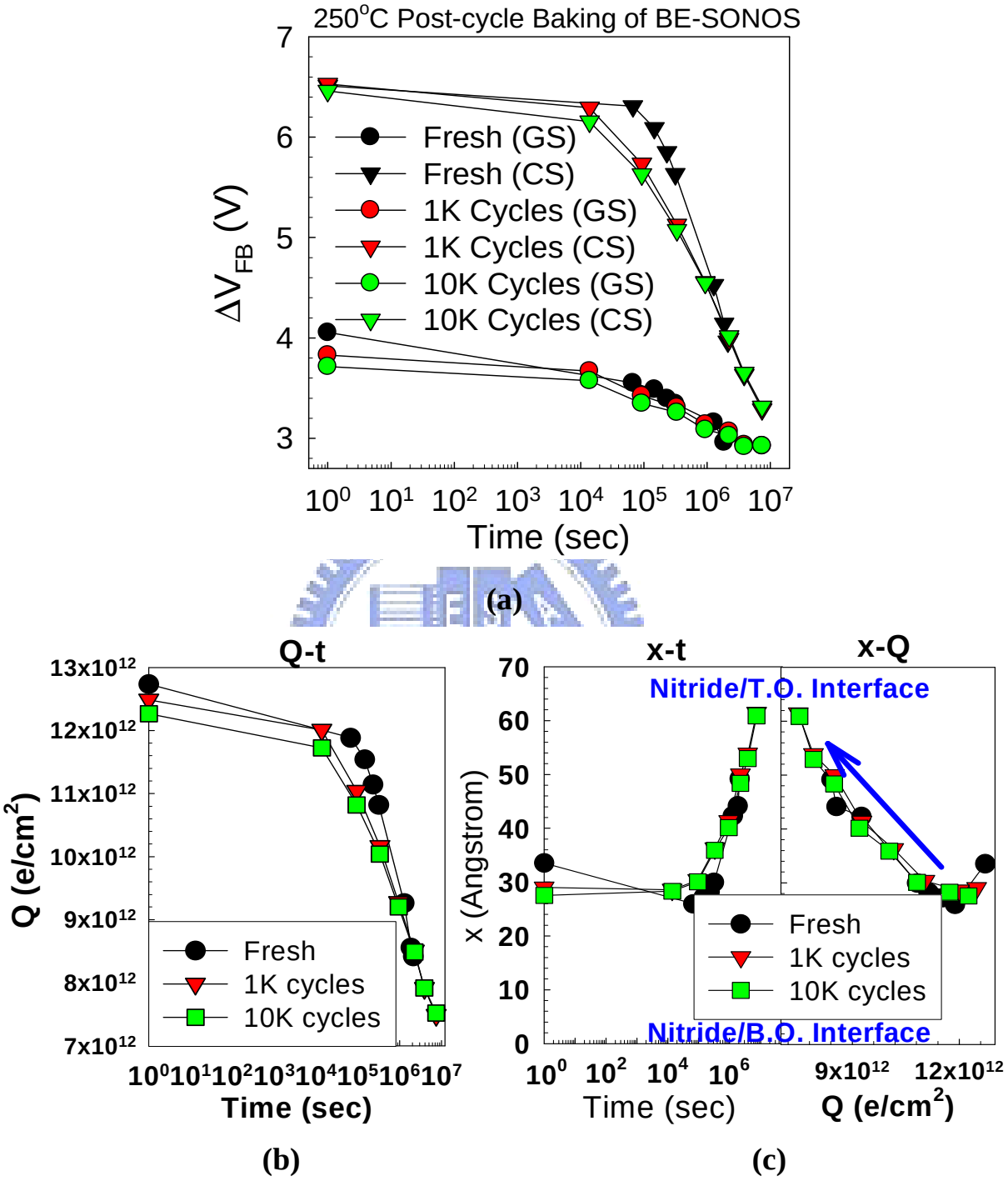


Fig. 5.8 (a) 250°C post-cycling baking characteristics of BE-SONOS (15/20/25/70/90Å). The devices are programmed by +19V before baking. (b) Q-t and (c) x-t/x-Q plots. The x-Q plot is transformed from Q-t and x-t plots. P/E cycling stress only causes more initial charge loss, but it has no effect on the long-term retention.

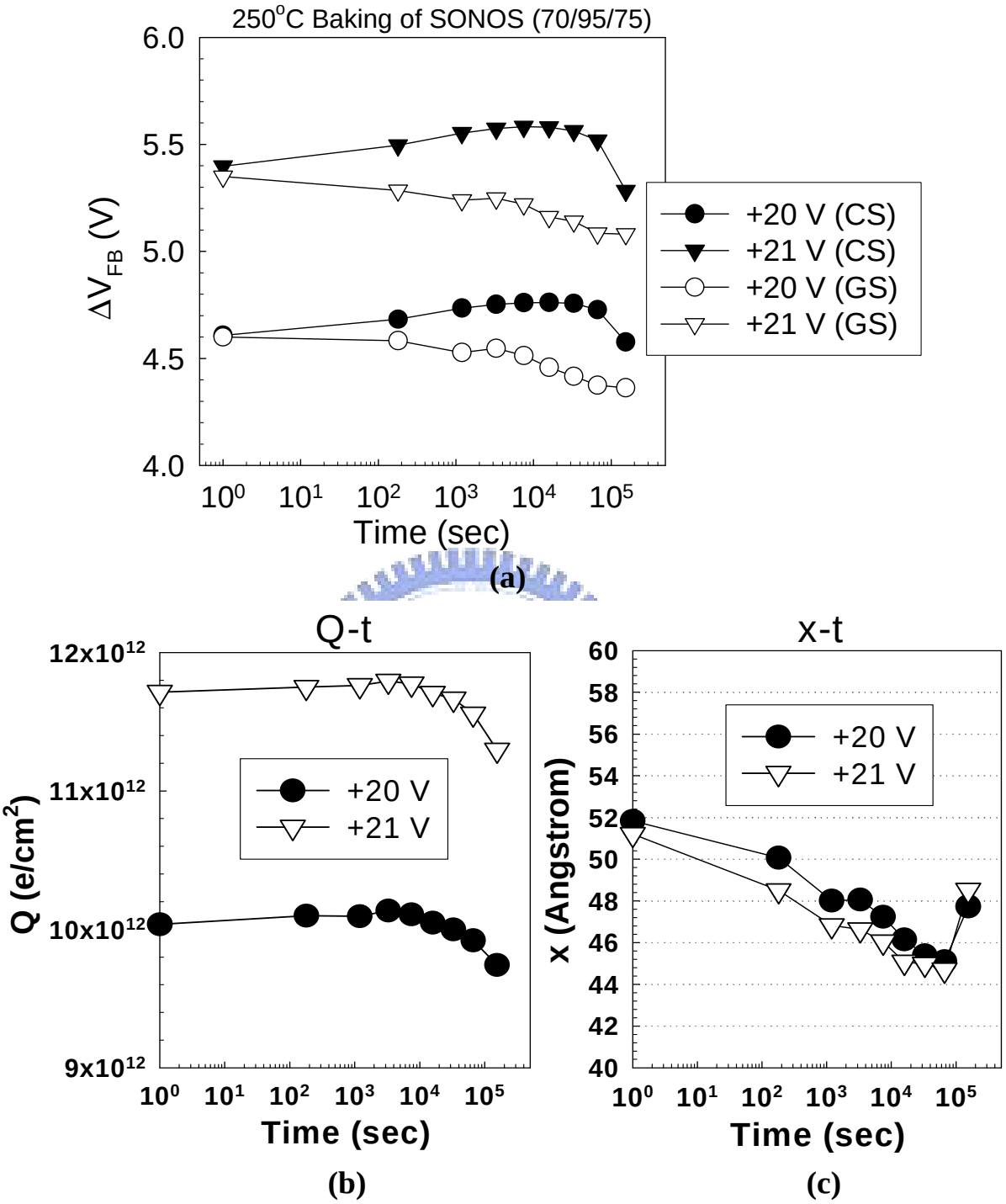


Fig. 5.9 (a) 250°C baking retention of SONOS (ONO = 70/95/75Å). The device is programmed by +20V 0.26sec or +21V 0.26sec before baking. Within 1 day baking, CS device shows obvious V_{FB} gain while GS device shows V_{FB} loss. (b) Q-t and (c) x-t plots. During 1 day baking, Q is almost unchanged while x is significantly decreased. This indicates that electron moves from the top portion toward the bottom portion.

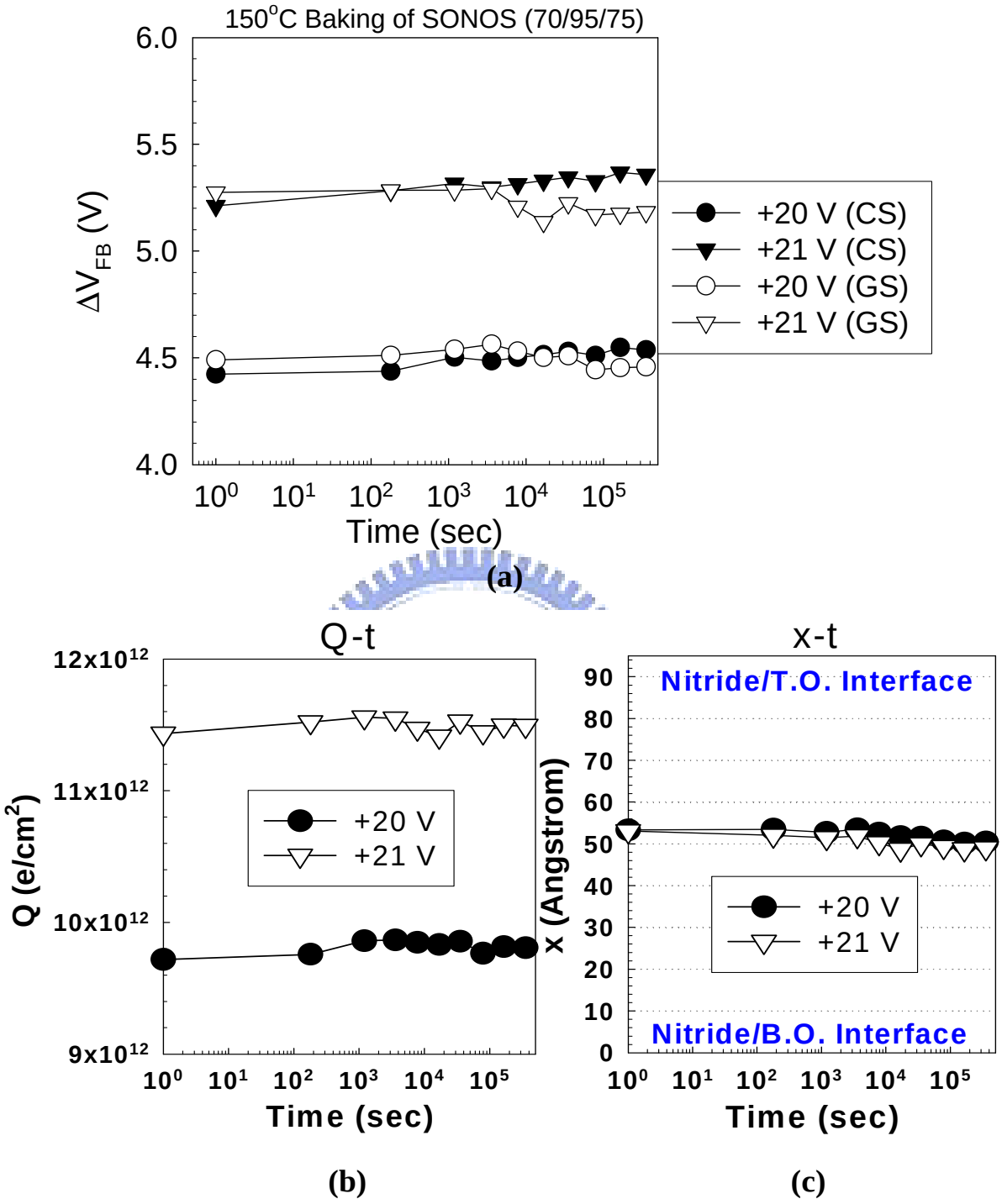


Fig. 5.10 (a) 150°C baking retention of SONOS (ONO = 70/95/75Å). The device is programmed by +20V 0.26sec or +21V 0.26sec before baking. There is no significant V_{FB} gain or V_{FB} loss. (b) Q-t and (c) x-t plots. The amount of change in x is much smaller than that in Fig. 5.9(c).

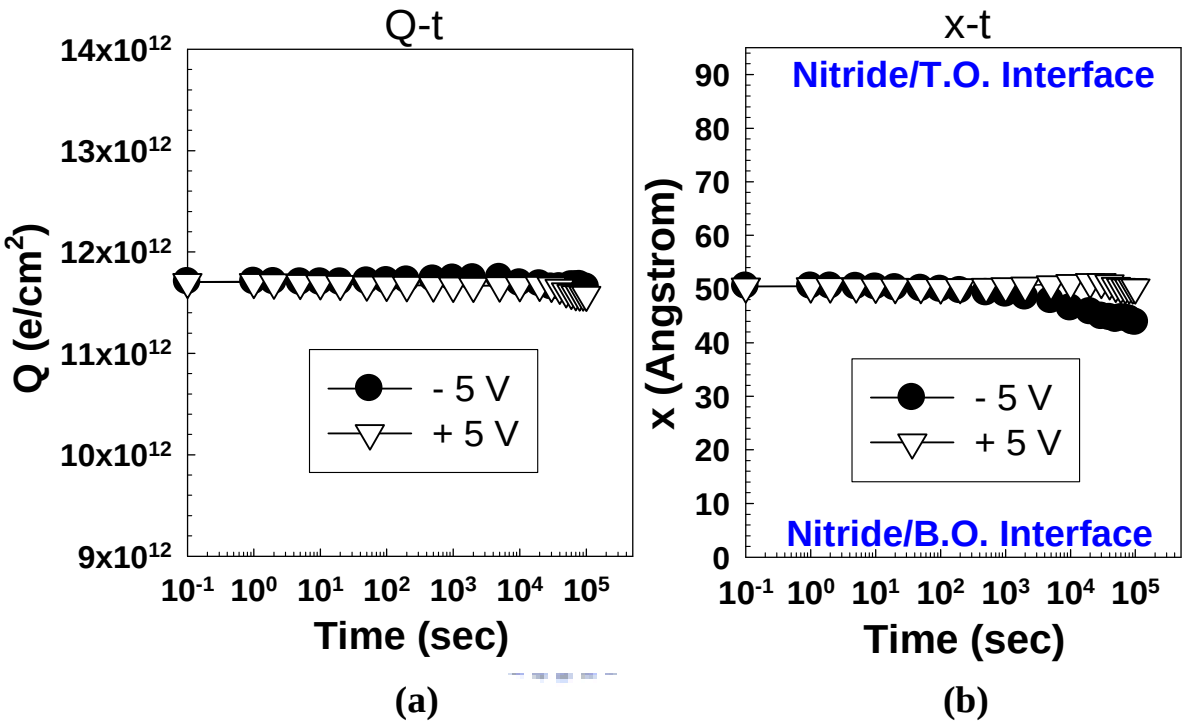


Fig. 5.11 (a) Q-t and (b) x-t plots of SONOS (ONO = 70/95/75Å) during ±5V gate stressing at 25^{o}C. The Q and x are very steady at room temperature.

CHAPTER SIX

GSCS METHOD APPLICATIONS:

STUDY OF GATE-INJECTION OPERATED

SONOS-TYPE DEVICES

OUTLINE

6.0 Introduction

Recently, we proposed a novel device with gate-injection operation “top BE-SONOS” [6.1], as shown in Fig. 6.1(a). This upside-down BE-SONOS structure uses the same principle as BE-SONOS — the top bandgap engineered tunneling dielectric provides easy hole tunneling under high e-field yet good data retention under low e-field. However, both program and erase are by gate injection instead of channel injection. Because the gate oxide is not stressed by P/E operations, this device has shown excellent cycling endurance. Moreover, due to the gate injection operation, this novel device is also insensitive to STI bird’s beak geometry [6.1].

Although the gate-injection operated SONOS-type devices have many excellent characteristics, their trapped charge behaviors are not well understood. Therefore, in this chapter we employed GSCS method to study the trapped charge behaviors of gate-injection operated “top BE-SONOS” and various SONOS-type devices such as SONoS with a thin top oxide (Fig. 6.1(b)). In this chapter, the mean vertical location of trapped charges and charge transport during programming/erasing and reliability tests are investigated extensively. Moreover, charge trapping efficiency is also examined in detail.

6.1 Sample Descriptions and Doping Optimization

Before investigating the trapped charge behaviors of gate-injection operated SONOS-type devices, we should fabricate appropriate devices at first. In this section, we will describe the detailed device fabrication and doping optimization.

6.1.1 Sample Design for Gate-injection Operation

In order to provide efficient electron gate injection, N-type poly gate is used for all samples. As mentioned in section 3.2.1, different poly gate and well dopant types will cause the distorted CV curves for GS capacitor. In order to avoid this issue, we use N-type well for

symmetry. Moreover, p^+-doped source/drain regions are also fabricated to provide inversion layer and equal potential for CS and GS under +FN operation. For all samples, the B.O. is formed by in-situ steam generation (ISSG) while the nitride layer is deposited by LPCVD. The T.O. and top ONO barriers are formed by deposited HTO or ISSG methods.

6.1.2 Doping Concentration Effect and Optimization

From section 3.4, we have known that for channel-injection operated SONOS-type devices, the accuracy of GSCS method will be influenced by well doping concentration of GS capacitor. On the contrary to channel-injection operated SONOS-type devices, the accuracy of GSCS method for gate-injection operated SONOS-type devices is sensitive the poly gate doping conditions. Therefore, we will further investigate the gate doping concentration effect on the GSCS method and optimize the doping concentrations for both CS and GS capacitors.

We first consider the gate doping effect of GS capacitor on GSCS method. From the comparison of two GS capacitors (Top BE-SONOS, ONONO = 94/70/30/20/12Å, oxides in top ONO barrier are formed by HTO method) with different gate doping concentrations ($5\times10^{16}cm^{-3}$ and $10^{17}cm^{-3}$) but the same well doping concentration ($10^{19}cm^{-3}$), we find that the $\Delta V_{FB,GS}$ of two GS capacitors are almost identical for both –FN program (Fig. 6.2(b)) and +FN erase (Fig. 6.2(c)) regardless of the diverse CV curves (Fig. 6.2(a)). Therefore, the poly gate depletion effect in GS capacitor can be ignored under our designed doping concentrations and device operation conditions, and the accuracy of GSCS method is insensitive to gate doping concentration of GS capacitor.

On the other hand, we next consider the gate doping effect of CS capacitor on GSCS method. Two CS capacitors (Top BE-SONOS, ONONO = 94/70/30/20/12Å, oxides in top ONO barrier are formed by HTO method) with different gate doping concentrations ($5\times10^{19}cm^{-3}$ and $10^{20}cm^{-3}$) but the same well doping concentration ($10^{17}cm^{-3}$) are compared in Fig. 6.3. The capacitor with more lightly doped poly gate can be depleted more easily at $+V_G$,

therefore, this device has smaller capacitance at $+V_G$, as shown in Fig. 6.3(a). Although the reason why the device with more lightly doped poly gate has larger $\Delta V_{FB,CS}$ (Fig. 6.3(b) and (c)) is not clear now, we can check the Q-x plots for different combinations of GS and CS capacitors. According to the concepts of GSCS method, the Q-x plots of different gate voltages should merge together. By checking the Q-x plots of CS capacitors with different gate doping concentrations and GS capacitor (well doping = $10^{19}cm^{-3}$ and gate doping = $10^{17}cm^{-3}$), we find that the only the Q-x plots of CS capacitor with gate doping = $10^{20}cm^{-3}$ merge together for different gate voltages.

From above results, we choose well doping concentrations for CS and GS as $10^{17}cm^{-3}$ and $10^{19}cm^{-3}$, respectively while the poly gate doping concentrations for CS and GS as $10^{20}cm^{-3}$ and $10^{17}cm^{-3}$, respectively.

6.2 Charge Vertical Location of Various Gate-injection Operated SONOS-type Devices

After confirming the doping conditions of GS and CS capacitors, in this section we will investigate the mean vertical locations of various gate-injection operated SONOS-type deivces, including SONOS, top BE-SONOS, SONS (SONOS without T.O.). Moreover, we also compare the results extracted by our GSCS method with other methods.

6.2.1 Gate-injected Electron Vertical Location of SONOS

Figure 6.4(a) shows the –FN electron gate injection of SONOS (54/70/90Å). N-type poly gate provides efficient gate electron injection that causes positive ΔV_{FB}. CS capacitor has larger ΔV_{FB} because this device has a thicker T.O. (the weighting factor is larger for CS capacitor). Using Eqs. (3-3) and (3-4), we can directly calculate Q and x of this device from Fig. 6.4(a), as shown in Fig. 6.4(b) and (c). Q-t in Fig. 6.4(b) shows that the electron charge density gradually increases as electrons are injected from gate. X-t and x-Q plots in Fig. 6.4(c) show the charge centroid time evolution and injection trajectory, respectively. Although x

shows larger variation at shorter time and smaller Q, the final x gradually approaches the center of nitride after longer injection, regardless of the program voltages. This result is very similar to that introduced in chapter 4.

In Fig. 6.5, we compare the x-Q plots of various SONOS devices ((a) 54/70/90Å, (b) 54/80/70Å, (c) 54/75/45Å, and (d) 54/80/25Å). The results indicate that the final x is very close to the center of nitride, irrespective of different nitride/T.O. compositions and T.O. processes. On the other hand, the x-Q plots of various top BE-SONOS devices are also compared in Fig. 6.6 ((a) 54/70/25/20/15Å and (b) 54/70/20/20/15Å). Similar to SONOS devices, the final x of top BE-SONOS devices is also close to the center of nitride, implying that the final mean vertical location is independent of tunnel dielectric (top ONO barrier or T.O.).

Although it is possible that the final charge centroid is the average of two interface charges, since the final x is similar for all samples with a wide range of ONO compositions and furthermore does not correspond to any interface, this strongly suggests that the injected electrons are mainly distributed inside the bulk nitride instead of the interfaces of oxide and nitride.

6.2.2 Comparison with Other Methods

We also employ another transient analysis method [6.2], where gate tunneling current (J) vs. T.O. e-field (E_{Tox}) curves are compared assuming various charge locations (nitride center, nitride/T.O. interface, or nitride/B.O. interface) in order to confirm the trapped charge vertical location. The calculated equations for each case are shown below.

Case 1 (Charge at nitride/T.O. interface):

$$E_{Tox} = \frac{|V_G| + \Delta V_{FB,CS}}{EOT} - \frac{\Delta V_{FB,CS}}{T_{Tox}} \tag{6-1}$$

$$J = \frac{d\Delta V_{FB,CS}}{dt}\frac{\varepsilon_0\varepsilon_{ox}}{T_{Tox}} \tag{6-2}$$

Case 2 (Charge at nitride/B.O. interface):

$$E_{Tox} = \frac{|V_G| + \Delta V_{FB,CS}}{EOT} - \frac{\Delta V_{FB,CS}}{T_{Tox} + T_N \dfrac{\varepsilon_{ox}}{\varepsilon_N}} \tag{6-3}$$

$$J = \frac{d\Delta V_{FB,CS}}{dt}\frac{\varepsilon_0\varepsilon_{ox}}{T_{Tox} + T_N \dfrac{\varepsilon_{ox}}{\varepsilon_N}} \tag{6-4}$$

Case 3 (Charge at nitride center):

$$E_{Tox} = \frac{|V_G| + \Delta V_{FB,CS}}{EOT} - \frac{\Delta V_{FB,CS}}{T_{Tox} + \dfrac{T_N}{2}\dfrac{\varepsilon_{ox}}{\varepsilon_N}} \tag{6-5}$$

$$J = \frac{d\Delta V_{FB,CS}}{dt}\frac{\varepsilon_0\varepsilon_{ox}}{T_{Tox} + \dfrac{T_N}{2}\dfrac{\varepsilon_{ox}}{\varepsilon_N}} \tag{6-6}$$

Figure 6.7 shows the comparisons of J vs. E_{Tox} curves of SONOS (54/70/90Å) with different assumed charge locations. Only Case 3 gives consistent results, indicating charges are close to the center of nitride. This is consistent with the results from the GSCS method and serves as a useful cross check.

6.2.3 Gate-injected Electron Vertical Location of SONS

In order to further prove that the electrons are trapped inside the bulk nitride instead of the interfaces of oxide and nitride, we particularly fabricated SONS (ON=54/70Å), where the T.O. is absent. If electrons are mainly located at the O/N interface, the charge centroid should be close to the nitride/B.O. interface for SONS. However, Fig. 6.8 shows that for –FN electron gate injection the electron centroid is still inside the nitride. This is a clear indication that bulk traps are dominant for SONOS-type devices.

6.3 Hole Injection Study of Various Gate-injection Operated SONOS-type Devices

After investigating the electron injection, we next discuss the hole injection. For the SONOS with a thin T.O. (SONoS) or top BE-SONOS with a top ONO barrier, gate holes can tunnel through the top dielectric under +FN erasing. On the other hand, for the SONOS without B.O., the substrate holes can tunnel into nitride during –FN operation. Therefore, in this section we will discuss the hole injection in these devices.

6.3.1 Hole Injection Characteristics of SONoS and Top BE-SONOS

Figure 6.9 shows the calculated Q and x of top BE-SONOS (54/70/20/20/15Å) during +FN erasing. We find that the total electron charge density (Q) in Fig. 6.9(a) decreases since the injected holes recombine with the trapped electrons. The charge centroid (x) in Fig. 6.9(b) shifts lower toward the bottom portion of nitride, indicating that the gate-injected holes first recombine with top electrons and then gradually neutralize bottom electrons. In the x-Q plot, we can clearly see the same mechanism reflected in the relationship between x and Q (as Q decreases x shifts lower).

Moreover, we find that after longer time +FN erasing the x moves even further below and eventually out of nitride. This is not because electrons move out of nitride, but simply due to an electron and hole vertical position mismatch after e^-/h^+ recombination: some residual injected holes are accumulated at the top portion of nitride while some residual electrons still remain in the bottom portion of nitride, leading to a charge centroid outside of nitride.

6.3.2 Two-region Charges of SNOS and SNS

We have also fabricated SNOS (SONOS without B.O.) and SNS (SONOS with neither T.O. nor B.O.) for comparison. The two-region approximation method is used to study the trapped charges since in these devices both electron injection (from gate) and hole injection (from channel) may happen simultaneously under –FN operation. Figure 6.10 shows the calculated Q-t during –FN operation by using Eqs. (3-9) and (3-10). For SNOS in Fig. 6.10(a),

the bottom portion of nitride (Q_1) traps holes ($Q < 0$) while the top portion (Q_2) traps electrons ($Q > 0$). Likewise, for SNS in Fig. 6.10(b) Q_1 traps holes, and Q_2 traps electrons.

Hole charges in the bottom portion of nitride come from hole injection from the Si substrate during –FN operation since nitride has a small hole barrier height (~ 2eV). It should be noted that for these kinds of devices, Q (Eq. (3-3)) and x (Eq. (3-4)) in bulk trap model do not provide meaningful information since charge centroid (x) is outside of the nitride.

6.4 FN Cycling Endurance and Post-cycling Retention Study

Since there is an electron and hole vertical mismatch after +FN erasing, we further investigate this impact on the P/E cycling endurance and data retention.

6.4.1 FN Cycling Endurance Characteristics

Figure 6.11 shows the calculated Q and x during 10K P/E cycling endurance of SONoS (54/80/25Å). After –FN programming (PV state), the total net charge Q (electrons) increases, and mean vertical location x is close to the nitride center (~ 40Å). On the other hand, after +FN hole injection from gate (EV state), total net charge Q (still more electrons since $Q > 0$) decreases, and mean vertical location x shifts lower. Since there are residual holes accumulated in the top portion of the nitride and residual electrons accumulated in the bottom portion of the nitride, thus x at EV state is outside of the nitride ($x < 0$).

We find that at the initial few P/E cycles, the Q and x are slightly varied after P/E cycling, but then soon become very stable after many P/E cycling. This result suggests that although there is an electron and hole vertical mismatch after +FN erasing, this mismatch should be viewed as a snapshot of the EV state, and should not be interpreted as two separate pockets of charges co-inhabiting the nitride. Therefore, the device still has excellent endurance characteristics.

6.4.2 Post-cycling Retention Characteristics

We also investigate the retention characteristics of fresh and 10K cycling for SONoS (54/80/25Å) devices, as shown in Fig. 6.12. The 10K P/E cycling conditions are the same as Fig. 6.11. The devices are first programmed by –15V 0.26sec before the 250^{o}C baking test.

In Fig. 6.12(a), compared with fresh device the post-10K cycled device has larger V_{FB} loss in GS capacitor but smaller V_{FB} loss in CS capacitor, therefore, we cannot obtain reliable trapped charge information from these V_{FB}-t. Very interestingly, however, by using our GSCS method to investigate the trapped charge behaviors we find that in the x-Q plots (Fig. 6.12(b)), the charge centroid (x) shifts lower significantly for the post-10K cycled device. This can be explained as the following. Since the T.O. is damaged after 10K cycling, the charge loss through T.O. is enhanced, and the charge centroid shifts downward with time. This result also suggests that our GSCS method can provide more in-depth understanding of the charge migration during high temperature baking.

6.5 Capture Efficiency of Various Gate-injection Operated SONOS-type Devices

Charge capturing efficiency is analyzed by comparing the experimental and theoretical Q-t curves, as shown in Fig. 6.13. The theoretical Q-t calculation follows the similar approach in section 4.2.1, where we assumed the –FN electron injection follows the Fowler-Nordheim tunneling with fitting parameters of effective barrier height (ϕ_B) and effective mass (m_{ox}) of T.O. However, the E_{Box} in section 4.2.1 should be changed to E_{Tox} (Eq. (6-5) for the assumption that the charges are at the center of nitride).

Figure 6.13 shows that the experimental Q-t is well correlated with the theoretical results for both SONOS with ONO = 54/70/90Å and 54/80/70Å when the total charge is smaller than 6×10^{12}electron-cm^{-2}. Moreover, the fitting parameters of T.O. are quite reasonable to the thermal oxide property (barrier height = 3.1eV and effective mass = $0.5m_0$). This excellent match indicates that most of the gate-injected electrons (< 6×10^{12}electron-cm^{-2}) are captured

by nitride equal to or greater than 70Å. When the total charge density is larger than 6×10^{12}electron-cm^{-2}, the total injected electrons may not capture completely by nitride, and the trapped electrons may out-tunnel through the B.O.

From above results, we demonstrate that for both channel-injection and gate-injection operations, a nitride 70Å or thicker can capture most of the injected electrons.

6.6 Summary

In this chapter, the charge-trapping behaviors of gate-injection operated SONOS-type devices are investigated in detail. Our results show that for –FN electron injection from gate the charge centroid is close to the center of nitride, irrespective of different nitride thickness and tunnel dielectric. On the other hand, for +FN hole injection from gate, after e^-/h^+ recombination the residual holes are accumulated in the top portion of nitride, and the residual electrons are accumulated in the bottom portion of nitride. Therefore, there is an electron and hole vertical mismatch. By comparing SONOS with SONS, we concluded that the major trapped charges are within the nitride bulk instead of the nitride/oxide interfaces. Moreover, two-region approximation model could well monitor electrons and holes simultaneously for SNOS and SNS structures.

Although there is an electron and hole vertical mismatch after +FN hole injection, the devices still have excellent cycling endurance characteristics. By comparing the post-10K cycling retention with fresh-state retention, we found that 10K cycling degrades the T.O. quality and causes more charge loss through the T.O. Moreover, we also demonstrated that nitride 70Å or thicker can capture most of injected charges for both channel- injection and gate-injection operations.

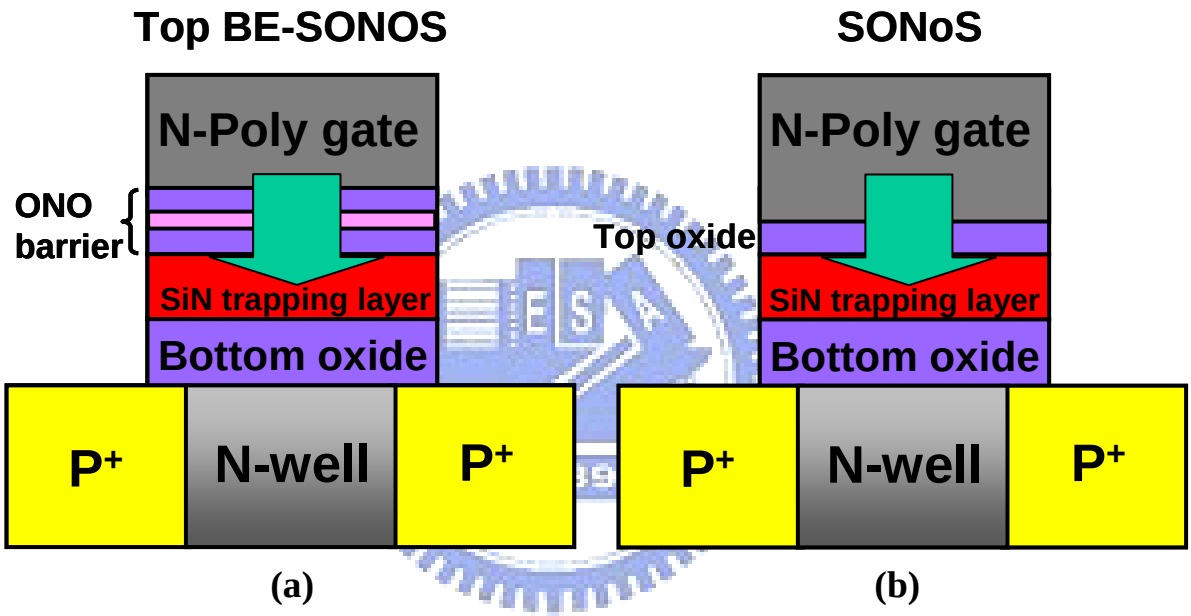


Fig. 6.1 (a) Top BE-SONOS with ONO barrier at the top and (b) SONoS with a thin top oxide. Both program and erase are by gate injection.

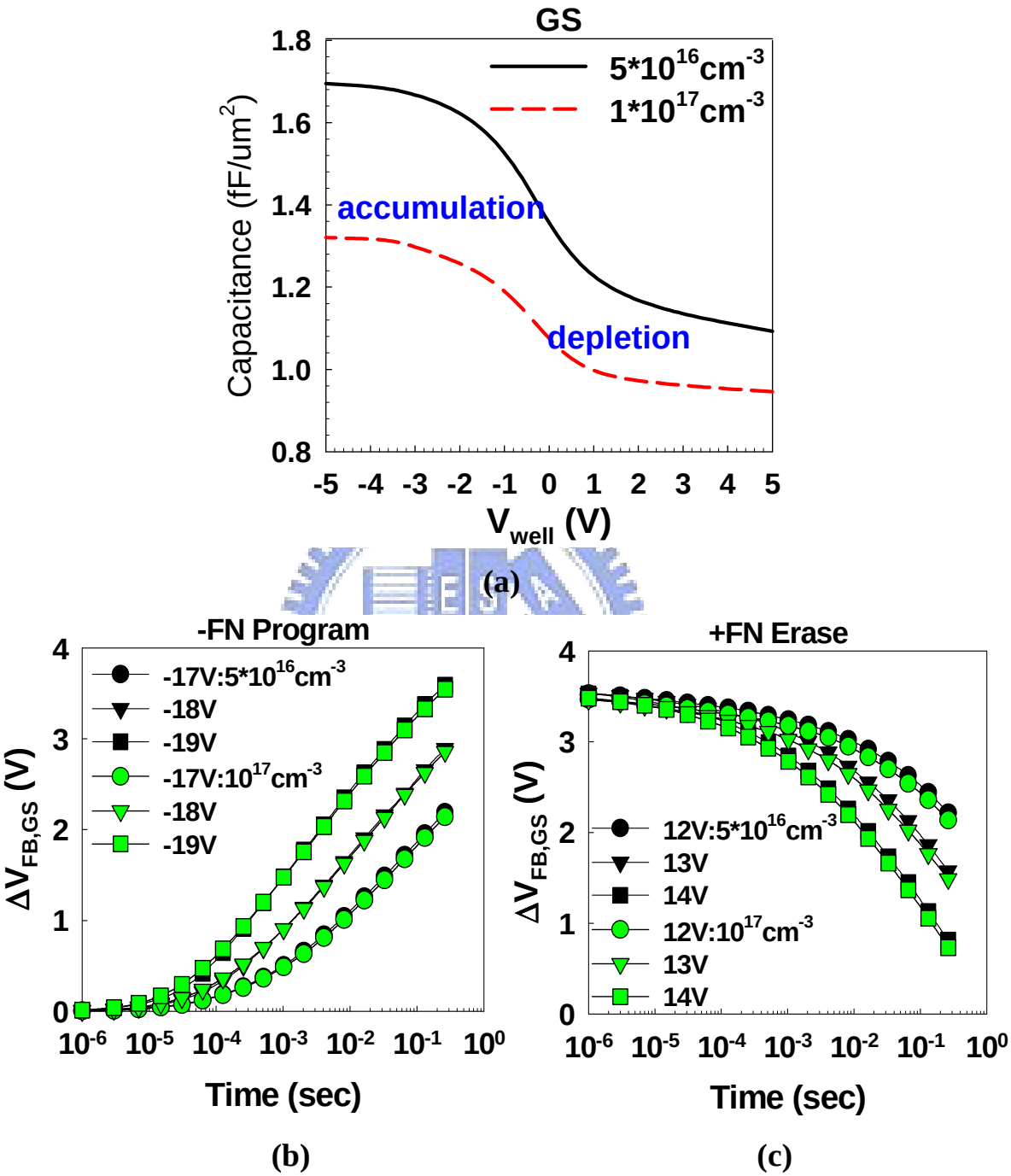


Fig. 6.2 Comparison of GS capacitors (Top BE-SONOS, ONONO = 94/70/30/20/12Å) with different poly gate doping concentrations. (a) CV curves. (b) $\Delta V_{FB,GS}$ during –FN programming. (c) $\Delta V_{FB,GS}$ during +FN erasing. The $\Delta V_{FB,GS}$ is insensitive to poly gate doping concentrations.

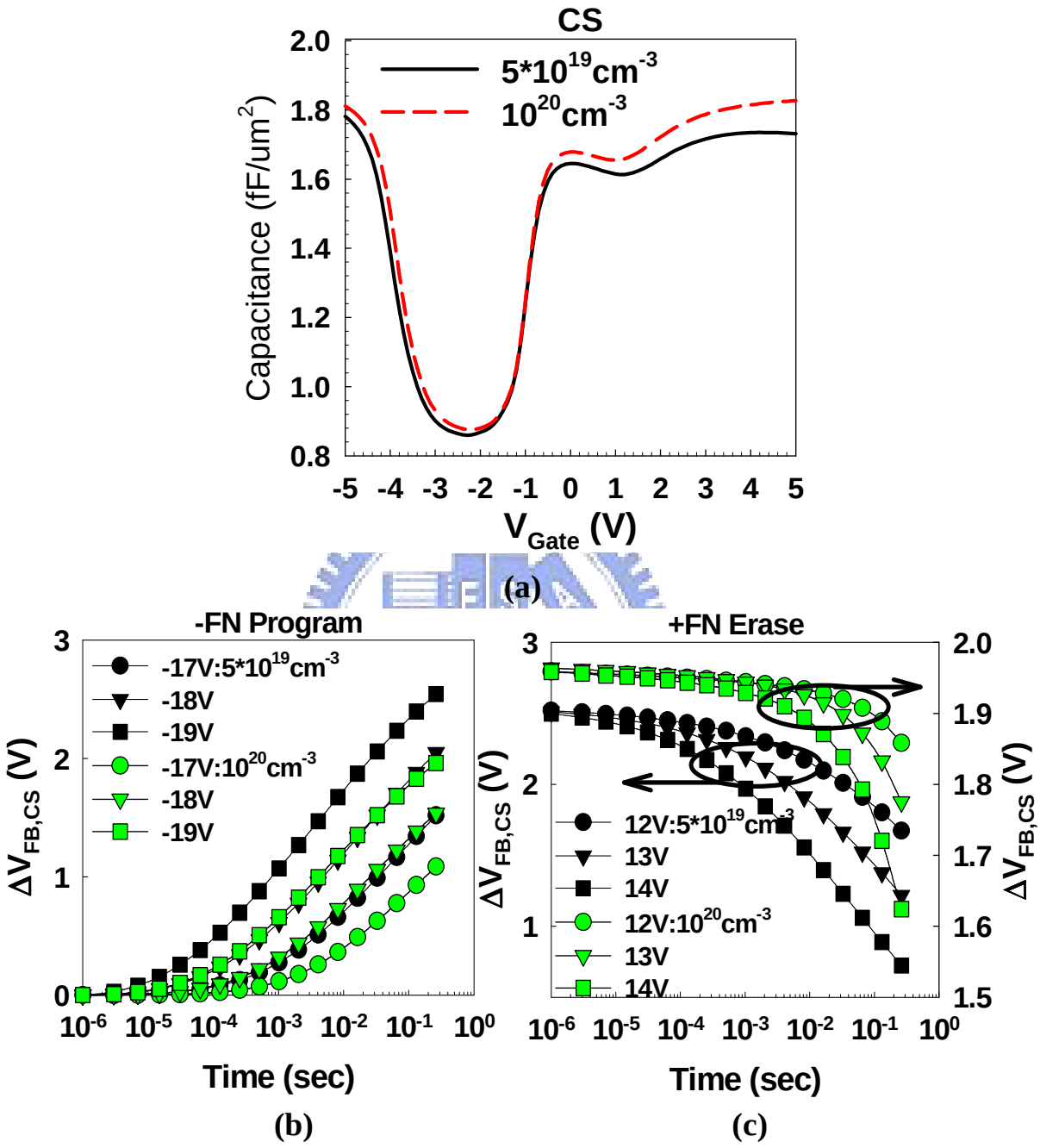


Fig. 6.3 Comparison of CS capacitors (Top BE-SONOS, ONONO = 94/70/30/20/12Å) with different poly gate doping concentrations. (a) CV curves. (b) $\Delta V_{FB,CS}$ during –FN programming. (c) $\Delta V_{FB,CS}$ during +FN erasing. The device with more lightly doped poly gate has larger $\Delta V_{FB,CS}$.

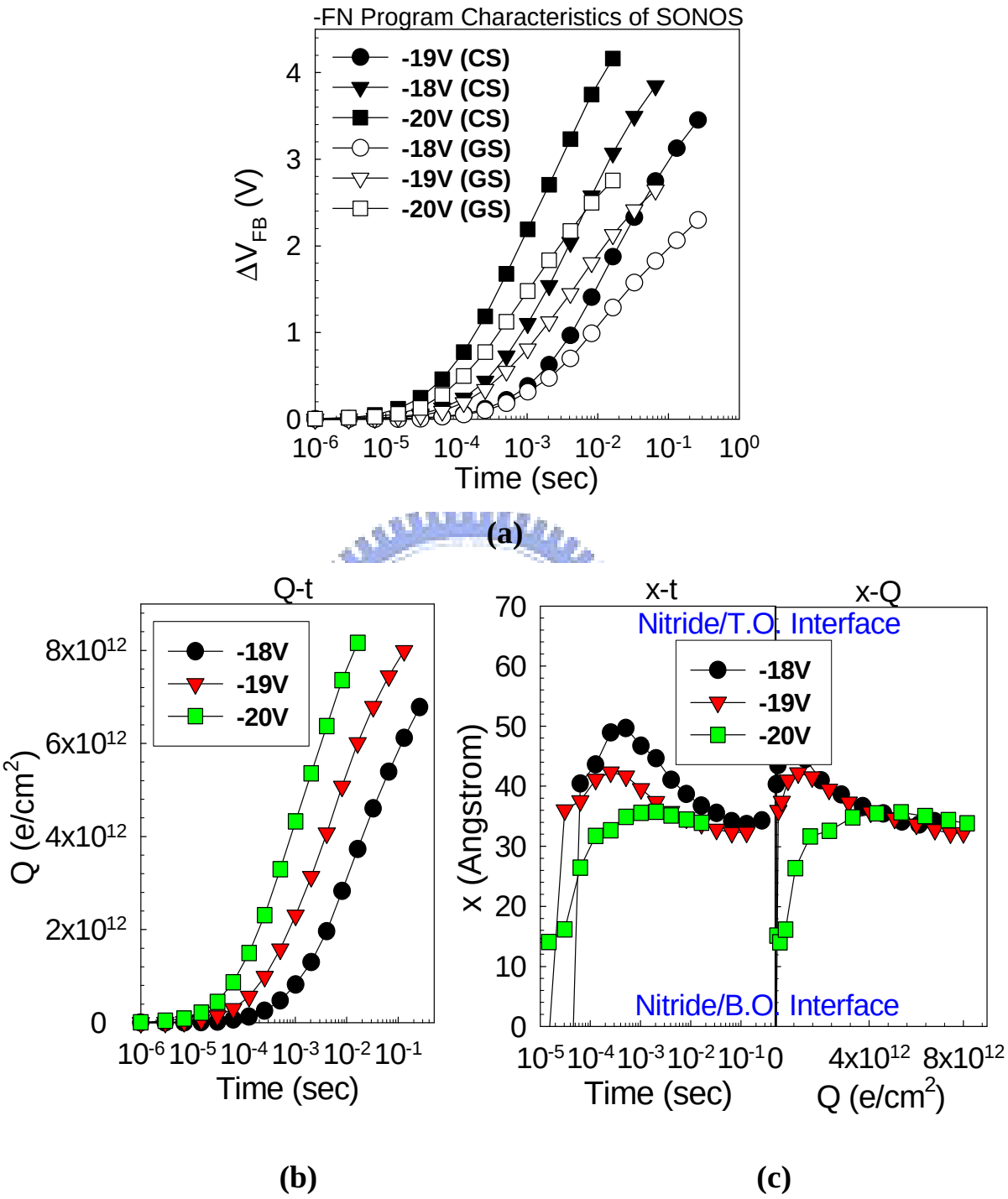


Fig. 6.4 (a) –FN electron gate injection characteristics of SONOS (54/70/90Å). CS capacitor has larger ΔV_{FB} because its T.O. is thicker than B.O. (b) Q-t and (c) x-t/x-Q plots. The x-Q plot is transformed by Q-t and x-t plots. The final mean vertical location is close to nitride center (~ 35Å).

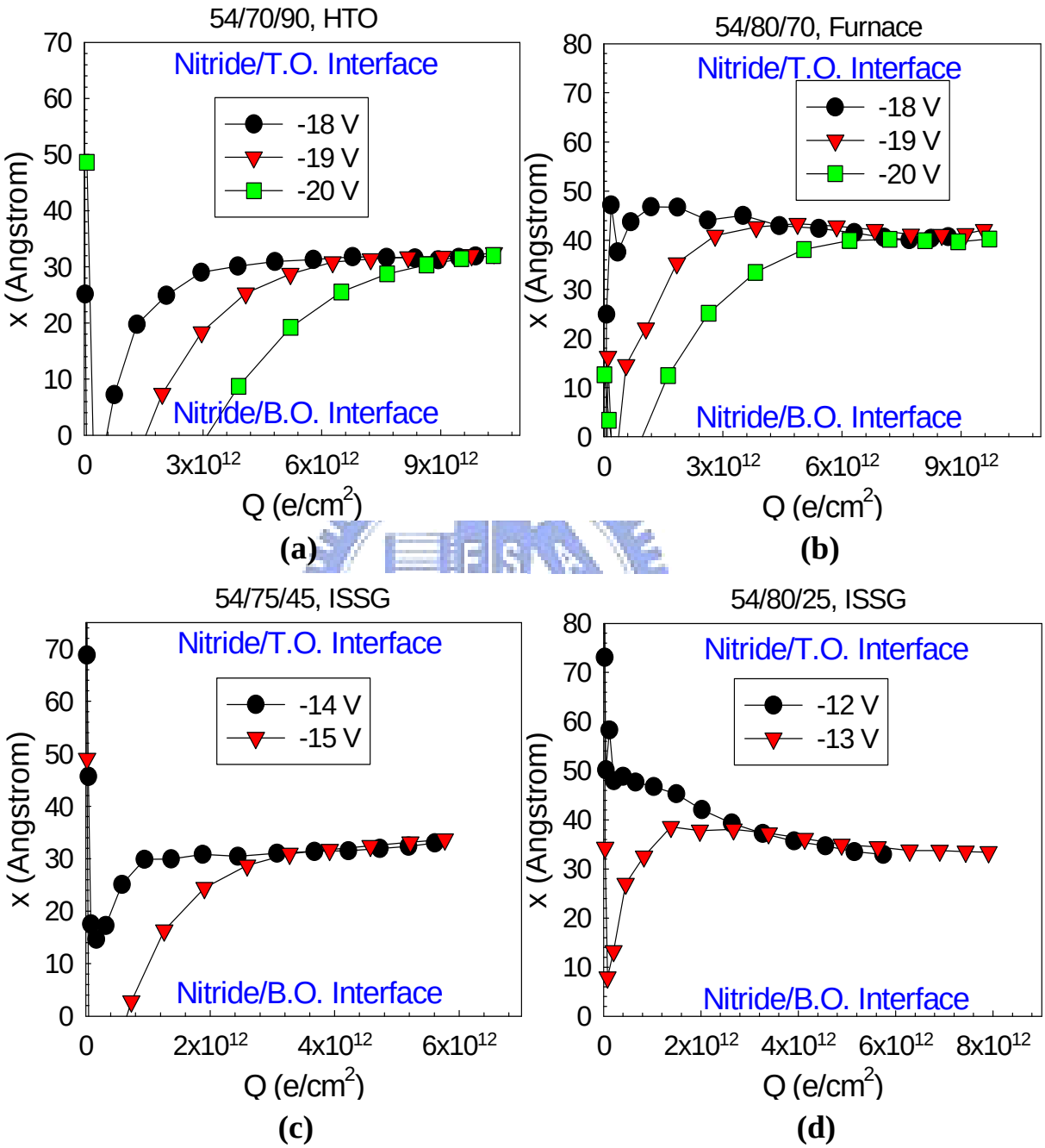


Fig. 6.5 Calculated x-Q plots for various SONOS devices. (a) 54/70/90Å, (b) 54/80/70Å, (c) 54/75/45Å, and (d) 54/80/25Å. For all samples, the final mean vertical locations are close to nitride center.

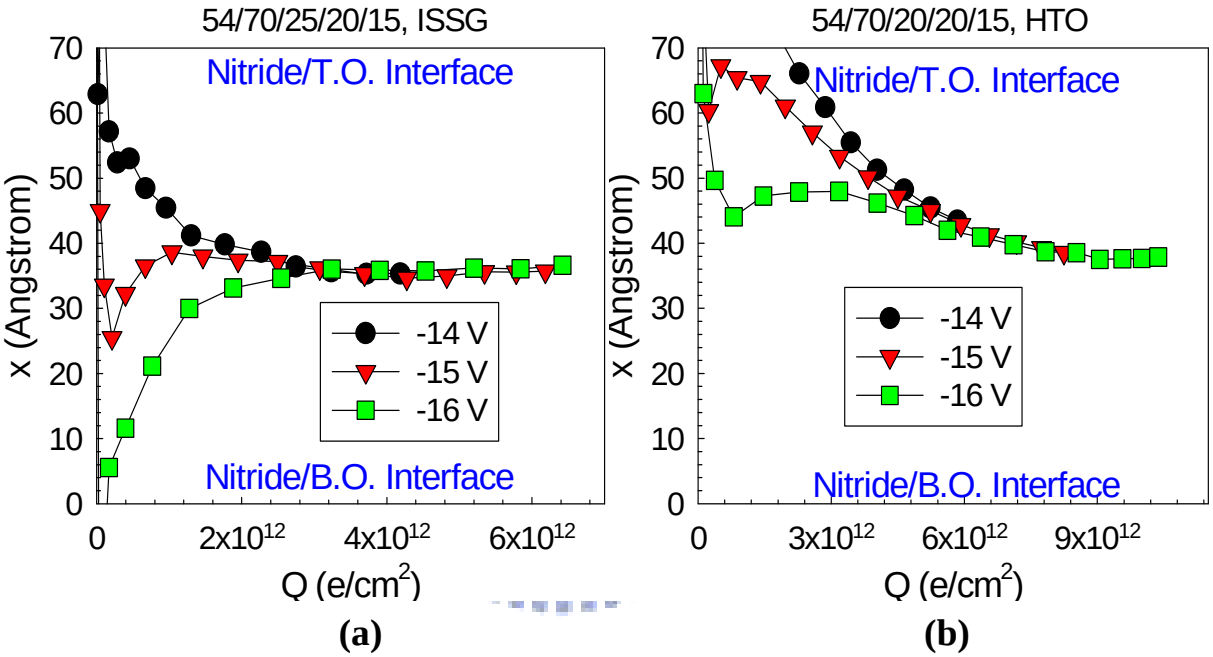


Fig. 6.6 Calculated x-Q plots for various top BE-SONOS devices. (a) 54/70/25/20/15Å and (b) 54/70/20/20/15Å. For all samples, the final mean vertical locations are close to nitride center.

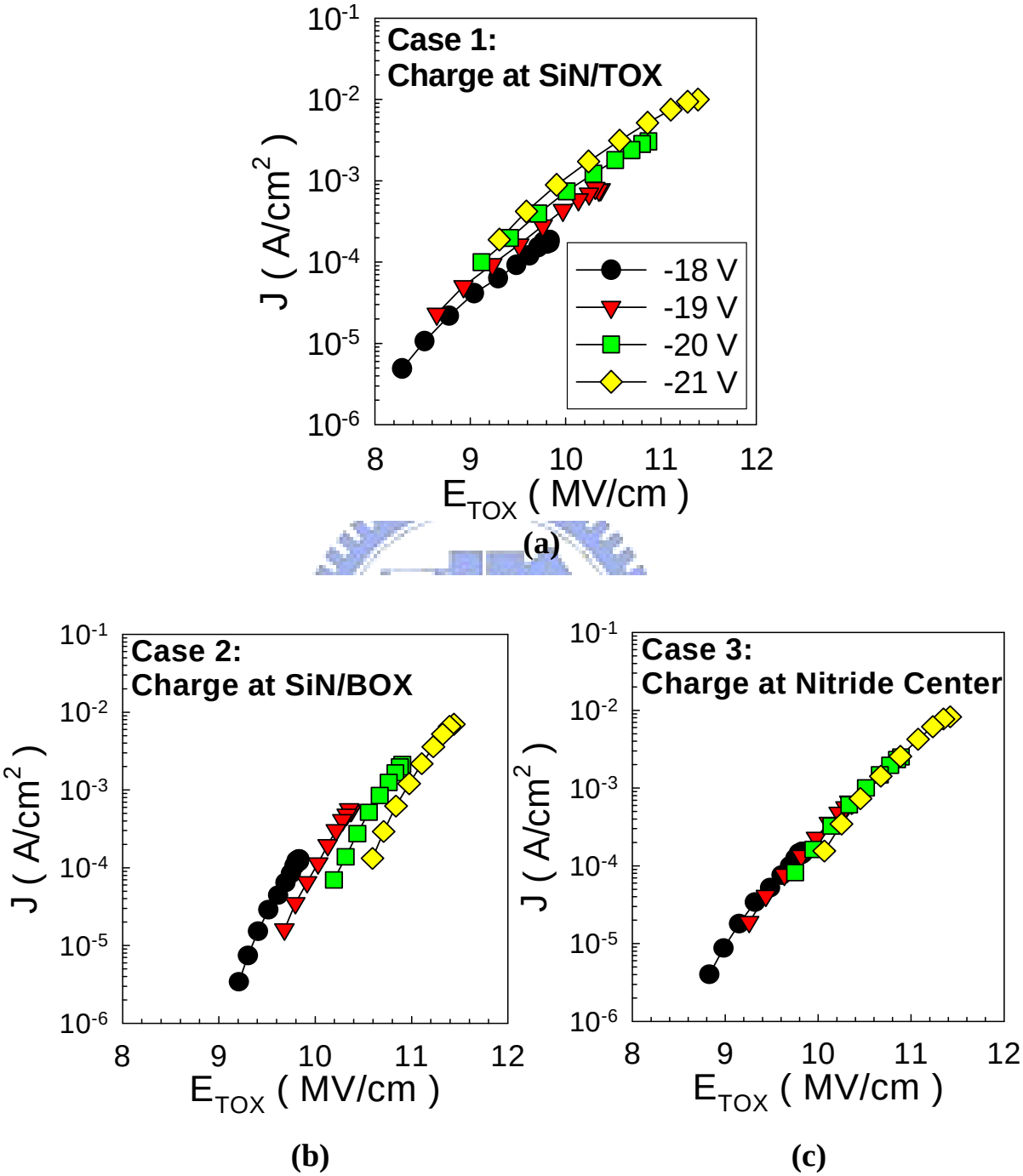


Fig. 6.7 Comparisons of J vs. E_{Tox} curves of SONOS (54/70/90Å) by assuming different charge vertical locations. The charge centroid is more likely located near the nitride center (Case 3 in (c)).

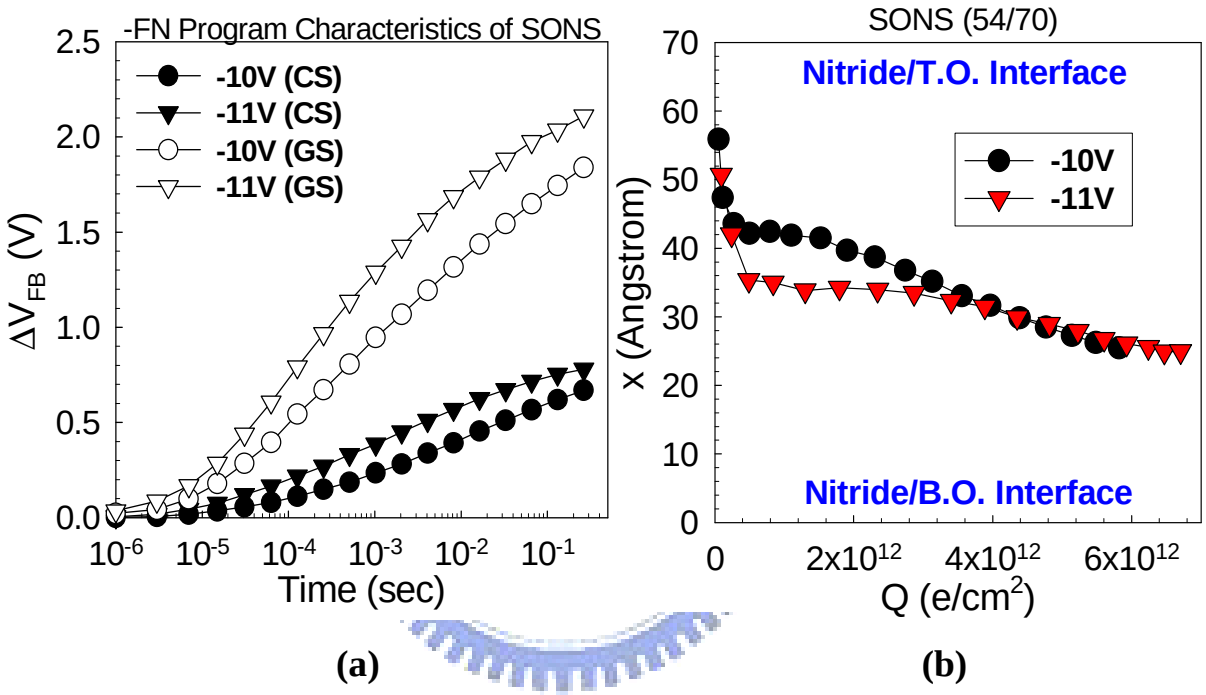


Fig. 6.8 (a) –FN electron injection characteristics of SONS (ON=54/70Å). (b) Calculated x-Q plot. The final mean vertical location is inside nitride instead of accumulating at the nitride/B.O. interface. This suggests that the major charge trapping is not at the O/N interface.

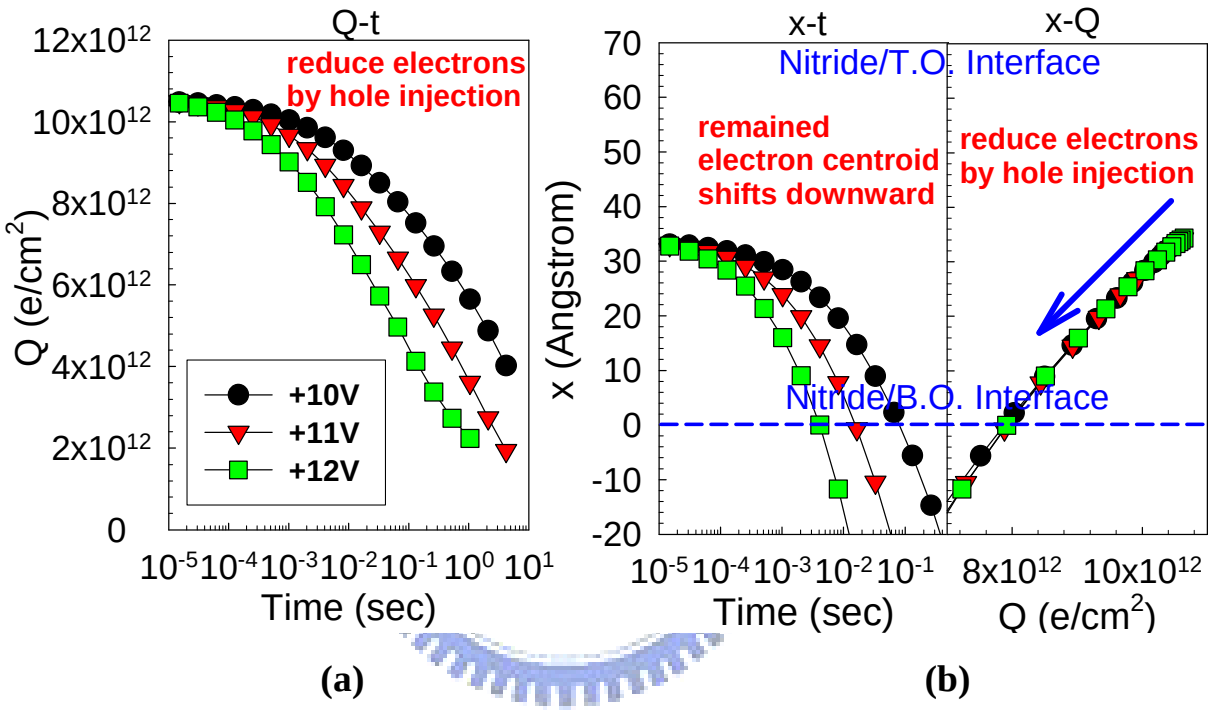


Fig. 6.9 (a) Q-t and (b) X-t/x-Q plots of top BE-SONOS (54/70/20/20/15Å) during +FN erasing. The devices are first programmed by –17V 0.26sec by electron gate injection, and then erased by various +FN voltages. The injected holes first recombine with the top electrons resulting in the downward motion of the charge centroid.

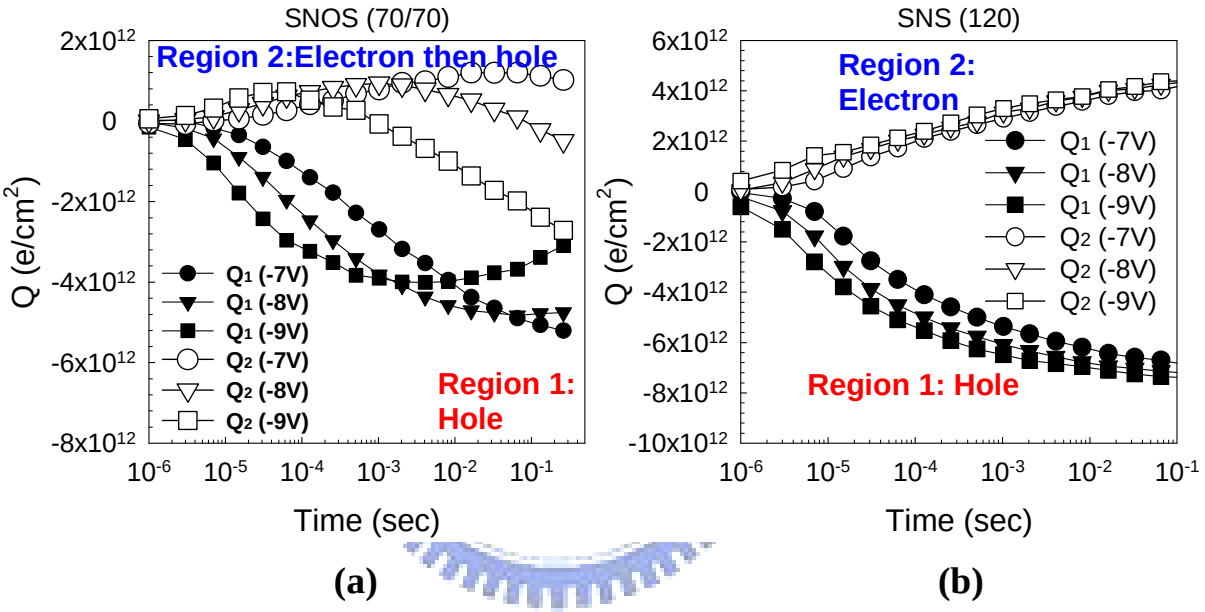


Fig. 6.10 Calculated Q-t results for (a) SNOS (70/70Å) and (b) SNS (120Å) by using two-region approximation method. Q_1 and Q_2 indicate the charges inside the bottom and top portions of nitride, respectively. The polarities of Q_1 and Q_2 are also shown.

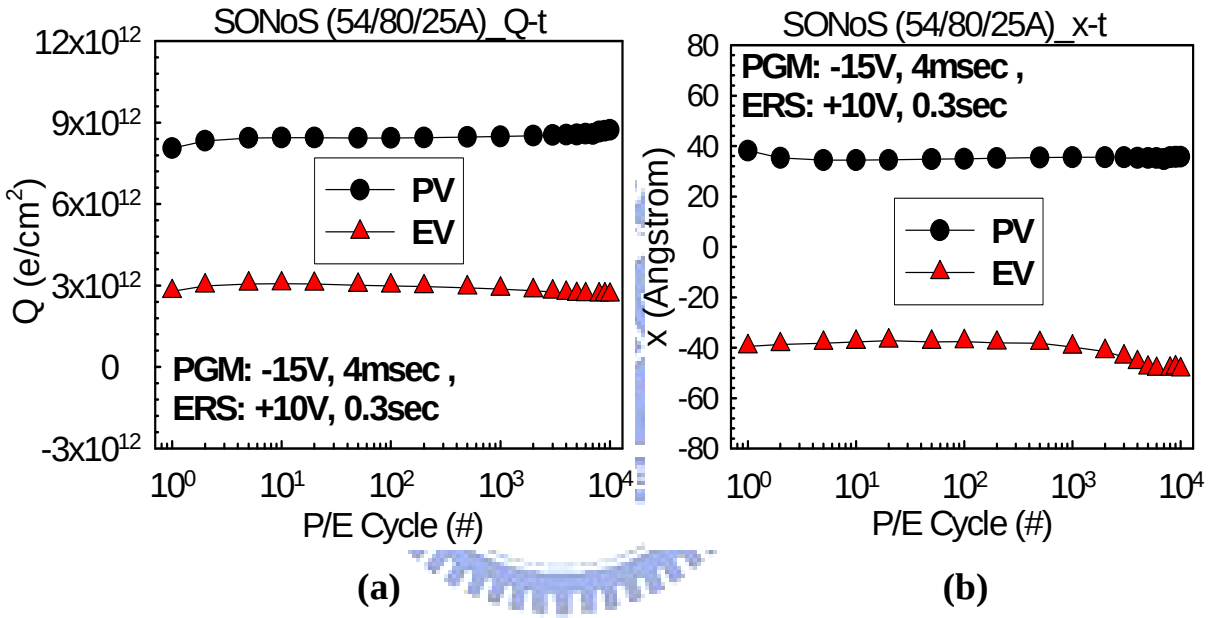


Fig. 6.11 Extracted (a) Q-t and (b) x-t plots during 10K P/E cycling endurance of SONoS (54/80/25Å). The program and erase conditions are –15V 4msec and +10V 0.3sec, respectively. At the initial few P/E cycles, the Q and x are slightly varied, but then soon become very stable after many P/E cycling.

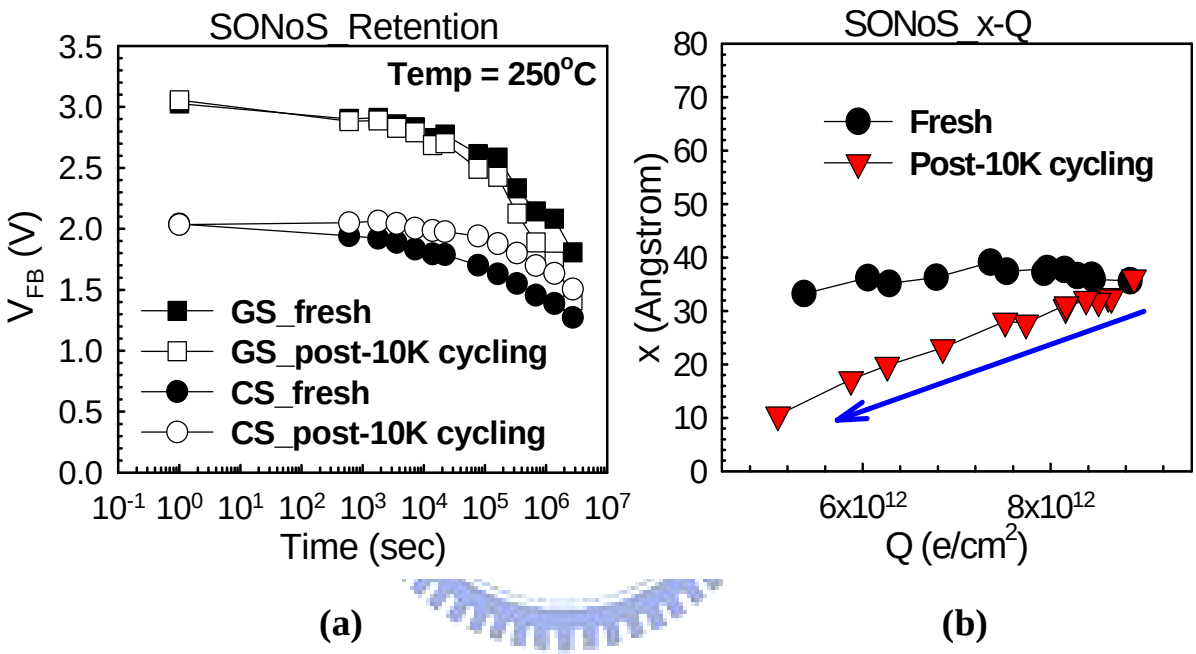
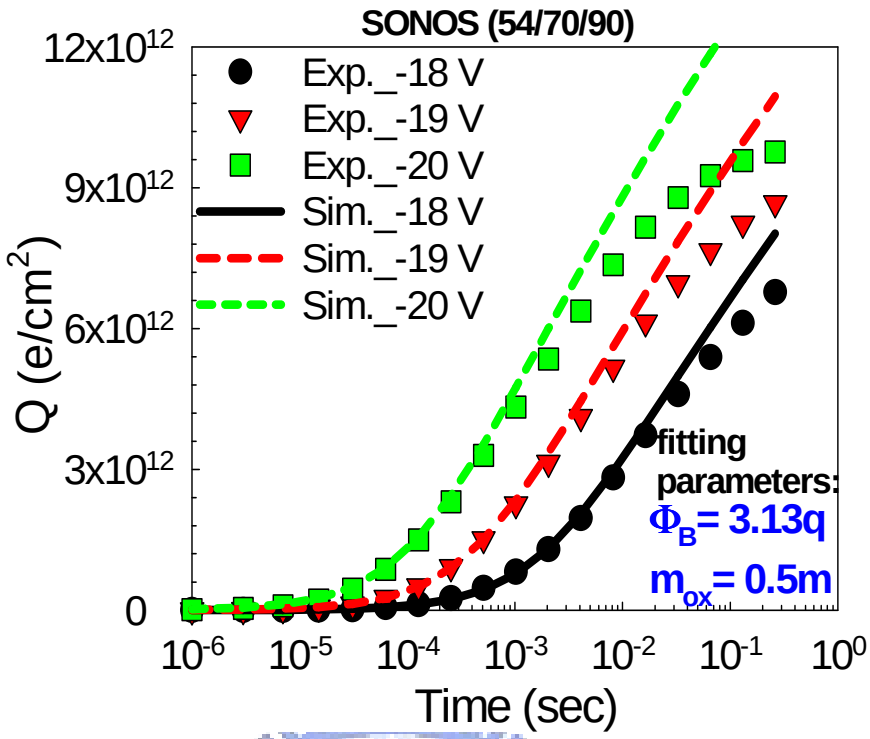
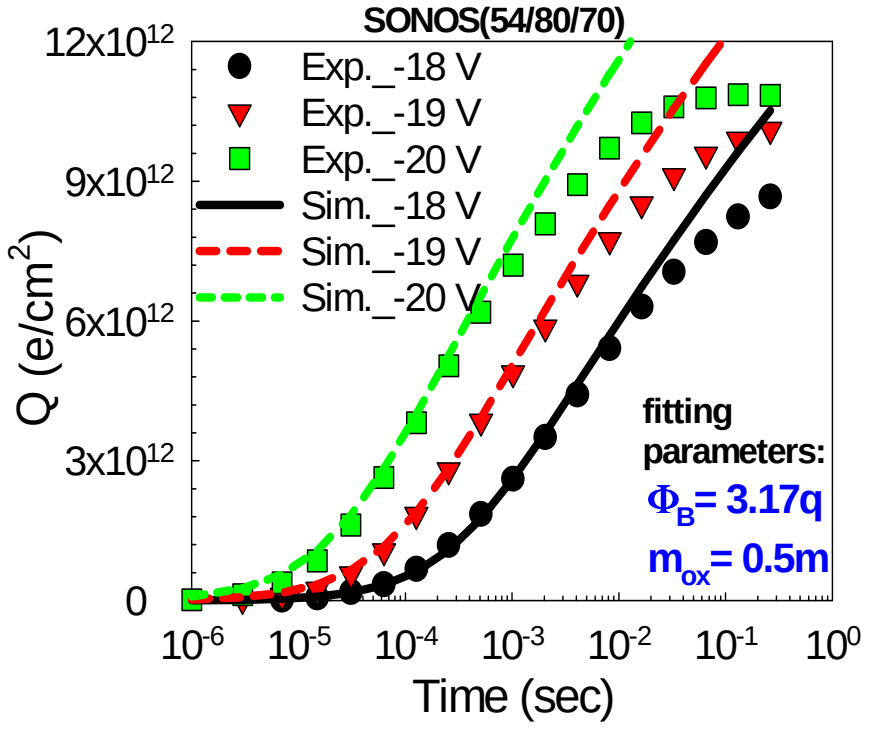


Fig. 6.12 (a) Comparison of 250°C retention characteristics of fresh and post-10K cycling devices. (b) Extracted x-Q curves. The devices are programmed at –15V 0.26sec before baking. As the total charge (Q) decreases with time due to charge loss, the x of fresh device stays almost constant, but the x of post-10K cycling device shifts lower.



(a)



(b)

Fig. 6.13 Comparisons of the experimental and theoretical Q-t for (a) 54/70/90Å and (b) 54/80/70Å at various –FN program voltages. The experimental Q-t is well correlated with the theoretical results.

CHAPTER SEVEN

ERASE MECHANISMS OF SONOS-TYPE DEVICES FOR BOTH CHANNEL-INJECTION AND GATE-INJECTION OPERATIONS

OUTLINE

7.0 Introduction

For charge-trapping (CT) devices, the erase operation is the most challenging. Conventional SONOS has a very slow FN erase speed when tunnel oxide is thick (> 25Å) while a thinner tunnel oxide causes severe retention loss. Therefore, several novel devices have been proposed to overcome this issue [7.1-7.2]. However, there is a lack of fundamental understanding of CT devices, especially for the erase mechanism. In general, the erase operation for all CT devices comes from two possible mechanisms. One is electron de-trapping from charge-trapping layer, and the other is external hole injection to compensate the trapped electrons. Both mechanisms result in the same V_T shift (or V_{FB} shift), and cannot be easily discriminated.

For conventional SONOS devices, the tunnel oxide is simple, and it is easily calculated that when the tunnel oxide thickness is above 25Å, hole direct tunneling is suppressed [7.1]. This is because oxide has a large hole barrier height (~ 4.5eV), hence hole FN tunneling is essentially negligible [7.2]. We have studied SONOS using a thick tunnel oxide (~ 50Å) [7.3-7.4] and found that the FN erase is very slow and mainly comes from the electron de-trapping from nitride. For such simple structure the erase mechanism can be distinguished because the FN or direct tunneling rate can be accurately calculated. However, for novel devices using new materials, it is difficult to discriminate between hole tunneling and electron de-trapping since the charge transport mechanism is unclear. It is therefore necessary to develop a systematic method to identify the erase mechanisms.

In this chapter, we will propose a systematic way to investigate the erase mechanisms of SONOS-type devices for both channel- and gate-injection operations. We adopt GSCS method to determine the total charge density (Q) and mean vertical location (x) during FN erasing. Erase tunneling current density (J) can be directly calculated by the time differentiation of Q, and can be plotted as a function of tunnel oxide electric field (E_{ox}). J-E curve relates directly to the physics of tunneling and can be fairly compared, therefore, the J-E

plots can easily discriminate electron de-trapping and hole injection. In addition, we also exploit the refill method [7.3] to examine the erase and further verify our findings.

7.1 Theoretical Equations for J-E Curve Extraction

To investigate the erase mechanisms of CT devices, we plot the instantaneous erase current density (J) vs. tunnel oxide e-field (E_{ox}) curves. For both channel- and gate-injection operations, we can directly calculate the J by time differentiation of total charge density Q from experimental data.

$$J = \frac{dQ(t)}{dt} \tag{7-1}$$

It should be noted that for different kinds of operations, the E_{ox} is different. For channel-injection operation, the E_{ox} is equal to B.O. e-field (E_{Box}) and independent of charge centroid x.

$$E_{ox} = E_{Box} = \frac{|V_G| + \Delta V_{FB,CS}}{EOT} \tag{7-2}$$

where V_G (negative) is the erase voltage applied to the gate. On the other hand, for gate-injection operation, the E_{ox} is equal to T.O. e-field (E_{Tox}) instead of E_{Box}, and the E_{Tox} depends on the charge centroid x.

$$E_{ox} = E_{Tox} = \frac{\varepsilon_N QT_{Box} + \varepsilon_{ox} Qx + \varepsilon_0 \varepsilon_{ox} \varepsilon_N V_G}{\varepsilon_0 \varepsilon_{ox} \varepsilon_N EOT} \tag{7-3}$$

where V_G is positive for gate-injection operation.

J-E curve is directly related to a certain tunneling mechanism. For example, if the erase mechanism is external hole tunneling, then J-E curves should follow a tunneling equation, where J is only a function of tunnel oxide e-field, and independent of the trapped charge density or trap energy profile. Various J-E curves can be obtained by using different erase voltages or different initial V_{FB}. Since J depends only on e-field, various J-E curves should follow the same curve and merge together. On the other hand, if the erase mechanism is electron de-trapping, then de-trapping current J depends not only on the e-field, but also on

the energy profile of the trapped electrons and the charge density. Then J-E curves from different erase conditions do not overlap.

Therefore, the comparison of J-E curves from different erase conditions provides us a systematic way to identify the erase mechanisms for various CT devices.

7.2 Erase Characteristics for Hole Injection

In this section, we first investigate the J-E curves of various SONOS-type devices with hole injection erase mechanism, including SoNOS (SONOS with a thin B.O.), SONoS (SONOS with a thin T.O.), BE-SONOS, and top BE-SONOS.

7.2.1 SoNOS with a Thin Bottom Oxide

We first examine the erase characteristics of SoNOS (20/70/90Å). The device is programmed by +FN (+14V) from the initial fresh state (V_{FB} ~ 0V) to a high V_{FB}, and then erased by –FN (–10V ~ –12V) to a lower V_{FB}, as shown in Fig. 7.1. In Fig. 7.1(a), the ΔV_{FB} of GS and CS capacitors are clearly different. This is easily understood because the T.O. is much thicker than B.O. for SoNOS.

In Fig. 7.1, the two ΔV_{FB} ($\Delta V_{FB,CS}$ and $\Delta V_{FB,GS}$) at a given time can be transformed into Q(t) and x(t) by using Eqs. (3.3) and (3.4); the results are shown in Fig. 7.2(a)-(b) and (c)-(d) for +FN program and –FN erase, respectively. For the program (Fig. 7.2(a)-(b)), x(t) shows that electron centroid migrates from the bottom interface toward the center of nitride. On the other hand, Q(t) shows a similar shape as ΔV_{FB}-t (Fig. 7.1(a)), as expected. For the –FN erase (Fig. 7.2(c)-(d)), we find that Q decreases (electron number decreases) while the charge centroid of remained electrons moves upward toward the top interface.

The J-E curves of SoNOS during –FN erasing can be simply calculated by Eqs. (7-1) and (7-2). Figure 7.3 shows that the extracted J-E curves for different erase voltages excellently merge together, and the curves almost follow the modified Fowler–Nordheim (MFN) hole

tunneling. The detailed equations about theoretical MFN hole tunneling are shown in Appendix F, and the corresponding fitting parameters are shown in Table F-1. This result implies that the erase mechanism of SoNOS (B.O. = 20Å) should be the hole injection from channel, as expected.

7.2.2 SONoS with a Thin Top Oxide

For gate-injection SONoS (54/80/25Å), the polarities of operation voltages are inversed as compared with channel-injection operated devices. We first apply –FN to program the devices from fresh state, and then erase the devices from program state by using +FN, as shown in Fig. 7.4(a) and (b). Using Eqs. (3-3) and (3-4), we can obtain the x-Q curves during +FN erasing, as shown in Fig. 7.4(c). Contrary to Fig. 7.2(c) where the channel injected holes causes upward x, the gate injected holes first recombine the top electrons and then gradually move toward the bottom portion of nitride (charge centroid of remained electrons moves downward as electron density decreases). Figure 7.4(d) shows the J-E curves calculated by Eqs. (7-1) and (7-3). The J-E curves merge together and follow the MFN hole tunneling (the fitting parameters are shown in Table F-1), which indicates that the erase mechanism of gate-injection SONoS capacitor is hole injection from poly gate.

This result further proves that our systematic method can be successfully applied to investigate the erase mechanisms of charge-trapping devices for both channel- and gate-injection operations.

7.2.3 BE-SONOS

BE-SONOS also allows hole-tunneling erase owing to the band offset effect in the ONO barrier at high e-field [7.5]. We have investigated the program/erase characteristics of BE-SONOS in section 5.1.3, and the results show that the trapped charge behaviors of BE-SONOS are similar to SoNOS. J-E curves during erasing of BE-SONOS (13/20/25/70/

90Å) are shown in Fig. 7.5(a). It also shows that J-E curves for various erase conditions merge together. This suggests that BE-SONOS is erased by hole tunneling mechanism, just likes SoNOS.

In order to further investigate the hole injection of BE-SONOS, we measure the erase characteristics of BE-SONOS (O1/N1/O2/N2/O3) with various N2/O3 thickness. The extracted J-E curves are compared and plotted in Fig. 7.5(b). All J-E curves overlap in one single cluster. This is not a coincidence. Since the tunneling barrier for all the samples is the same, they should follow the same hole tunneling mechanism. It therefore shows identical J-E curves for all samples. The variation in N2/O3 affects the erase speed (because it changes the e-field under the same erase voltage) but not the J-E curves. The above results also indicate that the erase behaviors for various N2/O3 scaling of BE-SONOS are easily predicted since J-E curves are identical. This fact is very useful in the EOT reduction for BE-SONOS NAND Flash scaling.

Since in BE-SONOS the holes tunnel through an ONO barrier instead of a thin tunnel oxide, in MFN modeling we replace the B.O. by the O1 (13Å) of ONO barrier. This MFN modeling can also well fit the J-E curves, as shown in Fig. 7.5(b), and the fitting parameters are shown in Table F-1. This result suggests that the erase mechanism is indeed hole tunneling.

Comparing the J-E curves of SoNOS (Fig. 7.3) and BE-SONOS (Fig. 7.5), we find that at high e-field, BE-SONOS has a larger hole current. On the other hand, at low e-field, BE-SONOS has a much more suppressed hole current. It shows that SoNOS cannot suppress direct tunneling leakage at low e-field, and is built in with retention problems. However, BE-SONOS shows much suppressed leakage at low e-field; it therefore is built in with excellent data retention.

7.2.4 Top BE-SONOS

Since the top BE-SONOS (up-side-down BE-SONOS) has a top ONO barrier, the gate holes can easily tunnel into nitride to erase trapped electrons. The program/erase characteristics of top BE-SONOS are similar to BE-SONOS, as illustrated in section 6.3.1.

J-E curves of top BE-SONOS (54/70/25/20/15Å with ISSG oxides and 54/70/20/20/15Å with HTO oxides) during erasing shown in Fig. 7.6 merge together and can be well fitted by MFN model (the fitting parameters are shown in Table F-1), which suggests that the erase mechanism of top BE-SONOS is really hole injection from poly gate. Similar to BE-SONOS, in MFN modeling we replace the B.O. by the top oxide (15Å) of ONO barrier.

7.3 Erase Characteristics for Electron De-trapping

We next examine the erase characteristics of SONOS with thicker tunnel oxides. For SONOS (26/70/90Å), the erase speed shown in Fig. 7.7(a) is much slower than SoNOS (Fig. 7.1(b)) since the hole tunneling is greatly reduced by thicker B.O.

The J-E curves shown in Fig. 7.7(b) illustrates two kinds of behaviors, at initial erasing (< 0.1s) the J-E curves are slightly scattered as compared with SoNOS, BE-SONOS, SONoS, and top BE-SONOS. However, after long erasing time the J-E curves merge together. It means that the SONOS with B.O. = 26Å has mixed erase mechanisms — initially governed by electron de-trapping (from shallow traps), and then hole tunneling (follow MFN equation, and the fitting parameters are shown in Table F-1). It should be noted that under normal operation (time < 0.1s) the dominant erase mechanism is electron de-trapping. Within this region, the smaller erase voltage results in higher de-trapping current as compared with larger erase voltage under the same E_{ox}. That is because under the same E_{ox}, there are more remained trapped electrons inside nitride for smaller erase voltage, and then contribute to higher de-trapping current.

The erase speed is further reduced for thicker B.O., as shown in Fig. 7.8(a). Figure 7.8(b) shows the J-E curves of 54/70/90Å, 70/70/90Å, and 90/70/90Å, all curves are very scattered

for different B.O. thickness and erase conditions. Moreover, the erase current (electron de-trapping current) in Fig. 7.8(b) is much smaller than that of hole current (Fig. 7.7(b)).

The scattered characteristics of J-E curves for SONOS with B.O. > 54Å is a clear distinction from that of the SoNOS or BE-SONOS. This clearly suggests that the erase mechanism is not hole tunneling but electron de-trapping. Furthermore, the scattered J-E curves indicate that electron de-trapping current density not only depends on the e-field, but also on other parameters. One possible factor is the trapping energy spectra of electrons.

7.4 Refill Characteristics

In order to study the impact of trapping energy on the erase characteristics, we apply the previously discovered refill method [7.3] to study the J-E curves. The refill operation partially erases the device and re-programs to the same V_{FB}, and repeats this sequence for several times. Our previous model indicates that the refill operation can shift the shallowly trapped electrons to deeper traps (blue shift) for SONOS with a thick B.O. (54Å), to give the device better retention even after severe hot-hole erase stressing [7.3-7.4].

We first investigate the refill characteristics of SoNOS (20/70/90Å), BE-SONOS (13/20/25/70/90Å), SONoS (54/80/25Å), and top BE-SONOS (54/70/25/20/15Å). It shows that refill has no effect on the erase speed, and the J-E curves are simply identical after several refill times, as shown in Fig. 7.9. The results indicate that hole-tunneling injection only depends on the e-field in the tunnel oxide, and it is independent of electron trapping energy.

We next examine the refill characteristics of SONOS with a thicker tunnel oxide. For SONOS (26/70/90Å), the V_{FB} shifts slightly decrease after refill treatment, and the corresponding J-E curves are shown in Fig. 7.10. The results show that J slightly decreases after refill treatment. It means that “some” electron de-trapping occurs during erasing, and refill changes the energy level of injected electrons from shallow to deep which results in smaller J. Finally, the erasing current J mainly comes from hole tunneling.

The refill characteristics of SONOS (54/70/90Å) are shown in Fig. 7.11(a). Compared with SONOS (26/70/90Å), the refill characteristics are more significant. This is because its B.O. is thicker such that the electron de-trapping is the dominant mechanism for charge loss while hole tunneling is completely suppressed. Thus, refill characteristics are more obvious. The x-t (Fig. 7.11(b)) and Q-t (Fig. 7.11(c)) show that during erasing the mean charge centroid x slightly increases and the total electron density Q decreases. This suggests that the electron de-trapping first comes from the bottom portion of the nitride. On the other hand, Q-t shows that the charge loss after erasing is significantly decreased after refill treatment. However, the x-t plot is unaffected after the refill sequence. This suggests that the effect of refill does not come from the charge vertical profile modulation, but comes from energy spectrum shift. Moreover, the J-E curves in Fig. 7.11(d) show that the erase current density (J) decreases greatly after refill. That is because there are more deeply trapped electrons (blue shift), therefore, de-trapping speed is slower after refill.

Previously, spectrum blue shift model was proposed to explain this refill process [7.3]. We also use this simple model to simulate the charge loss after refill for various refill times, and the model can fit the experimental data very well, as shown in Fig. 7.12(a). The simulated trapping energy distribution after various refill processes is shown in Fig. 7.12(b). Each refill sequence shifts the trapping energy higher (blue shift) and the distribution tighter, and it finally saturates.

We have also examined the refill characteristics of 70/70/90Å and 90/70/90Å (not shown here). The refill characteristics are similar to that of 54/70/90Å.

7.5 Summary

In this chapter, we provided a detailed understanding of the erase mechanisms of SONOS-type devices for both channel- and gate-injection operations by using the GSCS method. Using this method, we can accurately monitor the charge centroid (x) and charge

density (Q) during erasing. According to the Q and x, we can further plot the J-E curves during erasing. The results show that for the devices we can reasonably expect to erase by hole injection (SoNOS, SONoS, BE-SONOS, and top BE-SONOS), the J-E curves at different erase conditions overlap and are independent of EOT for the same tunnel barrier. Moreover, the extracted J-E curves can be well modeled by theoretical MFN equation. Applying the refill operation does not change the J-E curves. These results suggest that the erase mechanism is indeed simple hole tunneling injection, and electron de-trapping is insignificant.

On the other hand, for SONOS with B.O. $\geqq$ 54Å, hole tunneling is almost entirely blocked, and de-trapping becomes the dominant erase mechanism. The erase speed is much slower since the de-trapping current is much smaller than hole tunneling current. J-E curves are scattered for various erase conditions. Moreover, refill operation further reduces the de-trapping speed. These results suggest that electron de-trapping is not only a function of e-field, but also a function of trapping energy. Spectrum blue shift model can well explain the refill characteristics.

Therefore, this work provided a clearer understanding of the erase mechanisms of SONOS-type devices. Hole tunneling or electron de-trapping can be easily discerned using this systematic method. Moreover, the analysis of J-E curves also provided a fair comparison for various CT devices, as well as further modeling of the tunneling mechanism.

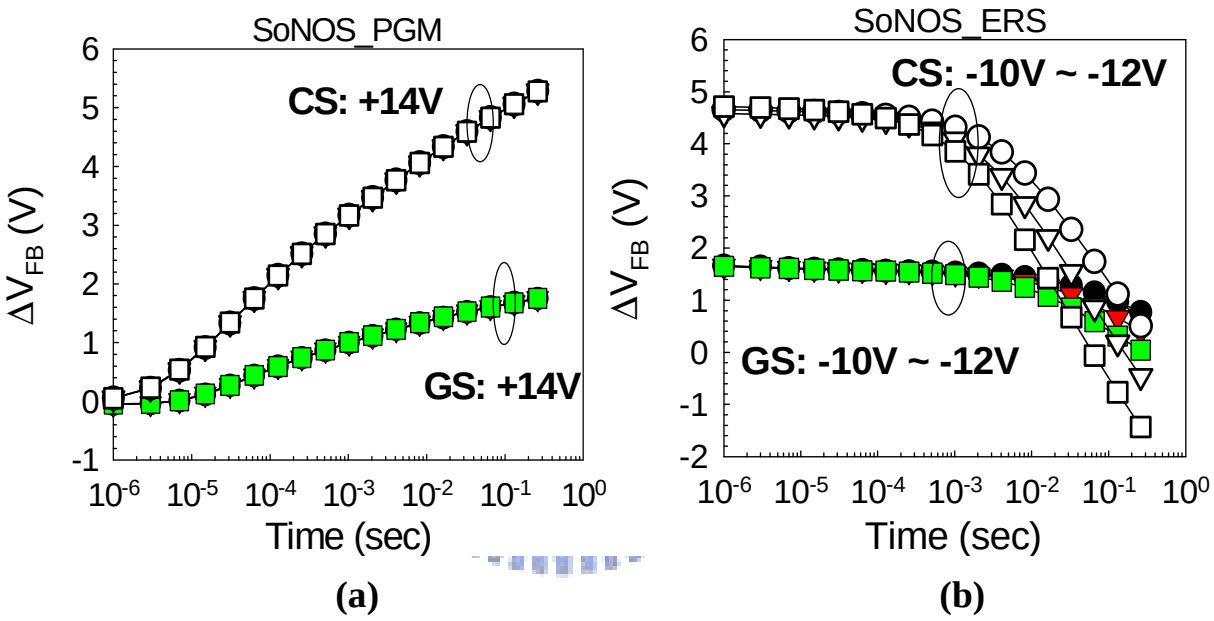


Fig. 7.1 (a) Program and (b) erase characteristics of SoNOS (20/70/90Å).

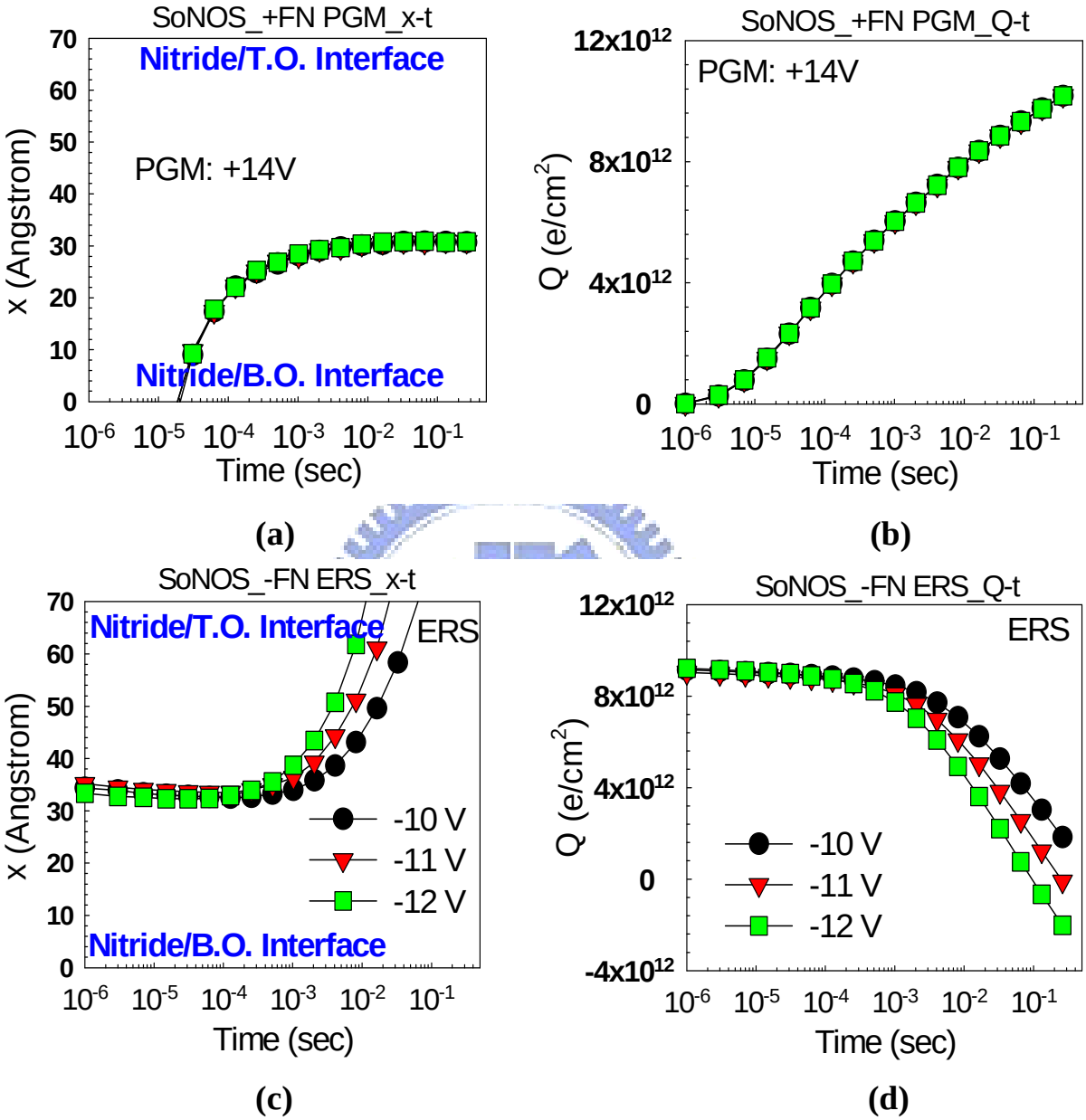


Fig. 7.2 (a) X-t and (b) Q-t of SoNOS (20/70/90Å) during programming transformed from Fig. 7.1(a). X-t shows that electron centroid migrates from the bottom interface toward the center of nitride. On the other hand, Q-t has a similar shape as ΔV_{FB}-t. (c) X-t and (d) Q-t of SoNOS during erasing transformed from Fig. 7.1(b). The charge centroid (remained electron) moves upward toward the top interface, and the electron density decreases.

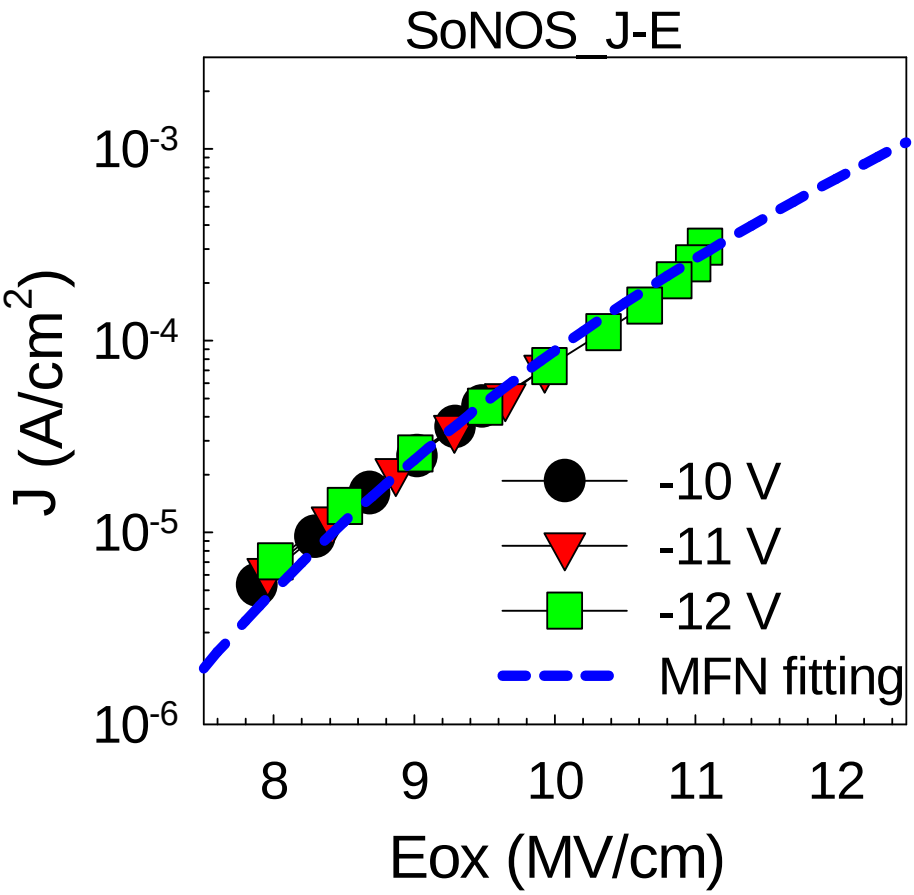


Fig. 7.3 J vs. E_{ox} of SoNOS (20/70/90Å) during erasing by using Eqs. (7-1) and (7-2). Different erase voltages follow the same trend, and they can be well fitted by MFN equation.

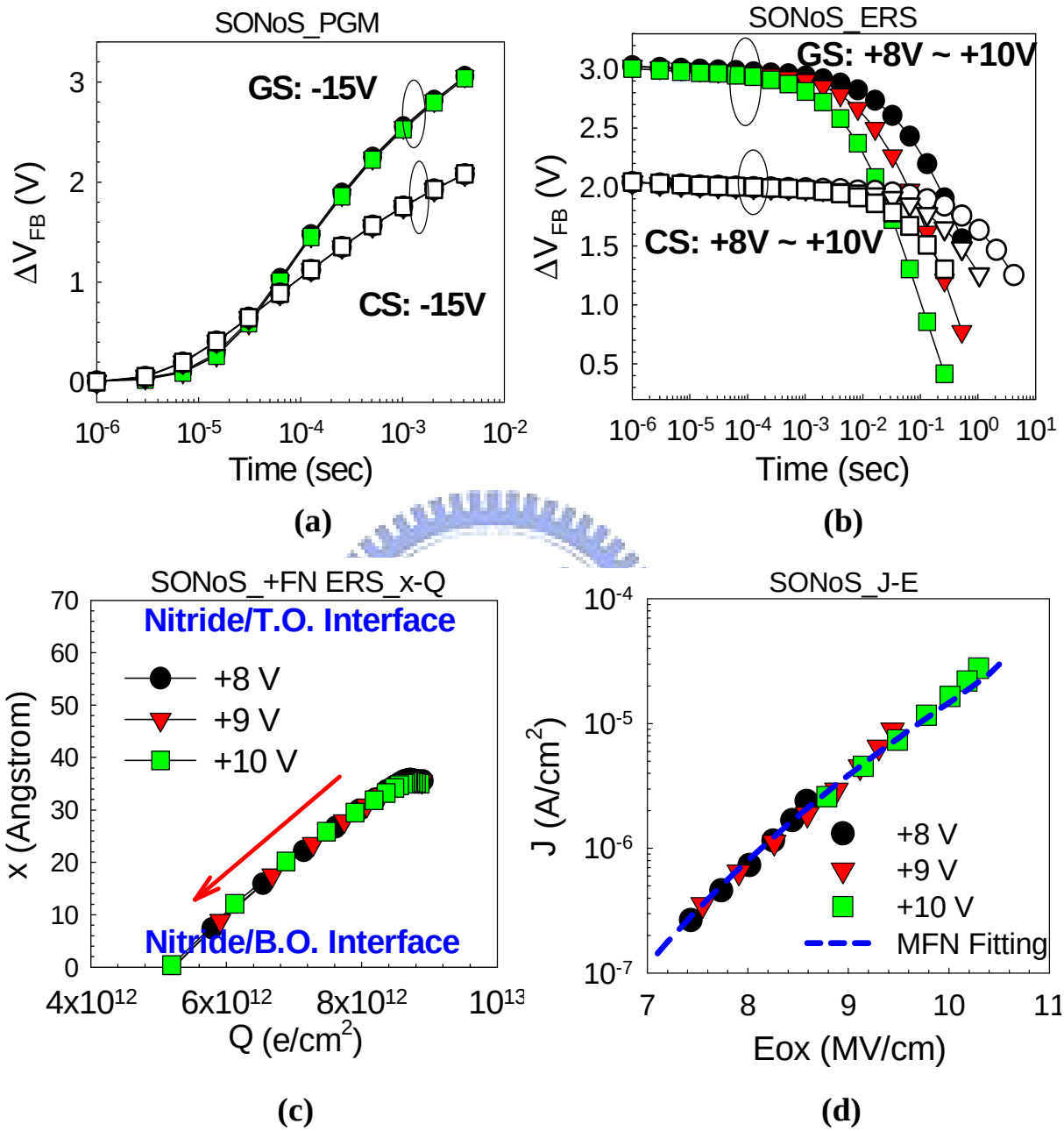


Fig. 7.4 (a) Program and (b) erase characteristics of SONoS. (c) X-Q during erasing transformed from (b). The charge centroid moves downward toward the bottom interface as electron density decreases. (d) J vs. Eox during erasing by using Eqs. (7-1) and (7-3). Different erasing voltages follow the same trend, and they can be well fitted by MFN equation.

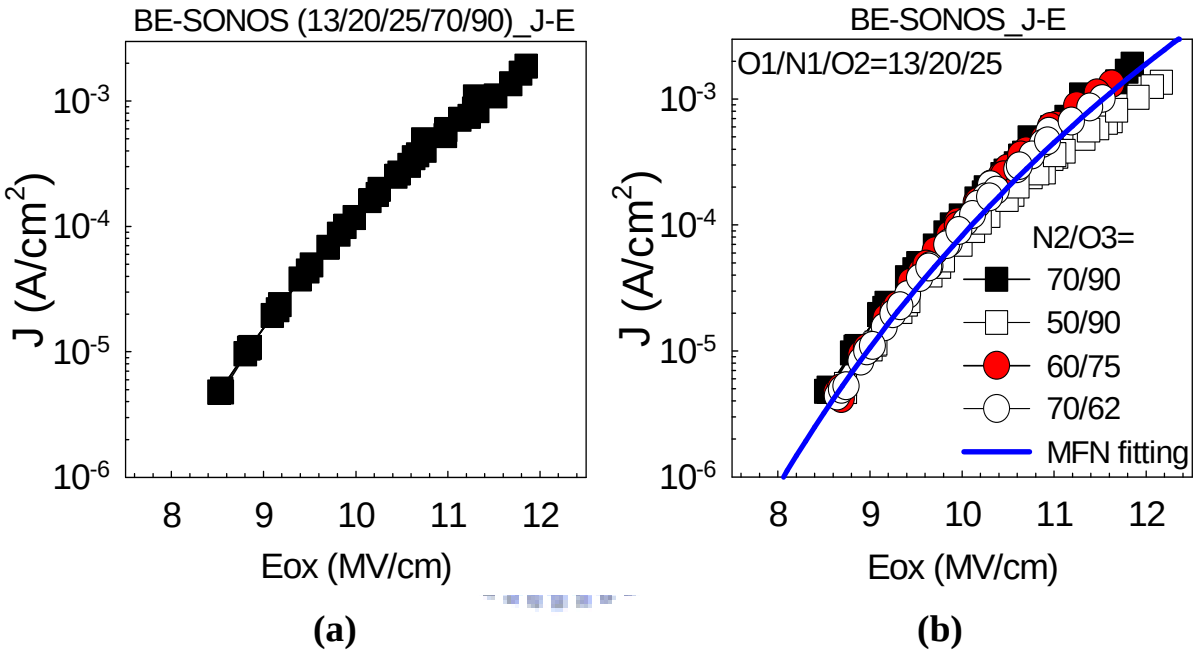


Fig. 7.5 (a) J vs. E_{ox} curves of BE-SONOS (13/20/25/70/90Å). (b) Comparison of J vs. E_{ox} curves for BE-SONOS with various N2/O3 thickness. All J-E curves overlap in one single cluster. Therefore, we can know that the hole injection is independent of N2/O3 compositions. The J-E curves can be well fitted by MFN model.

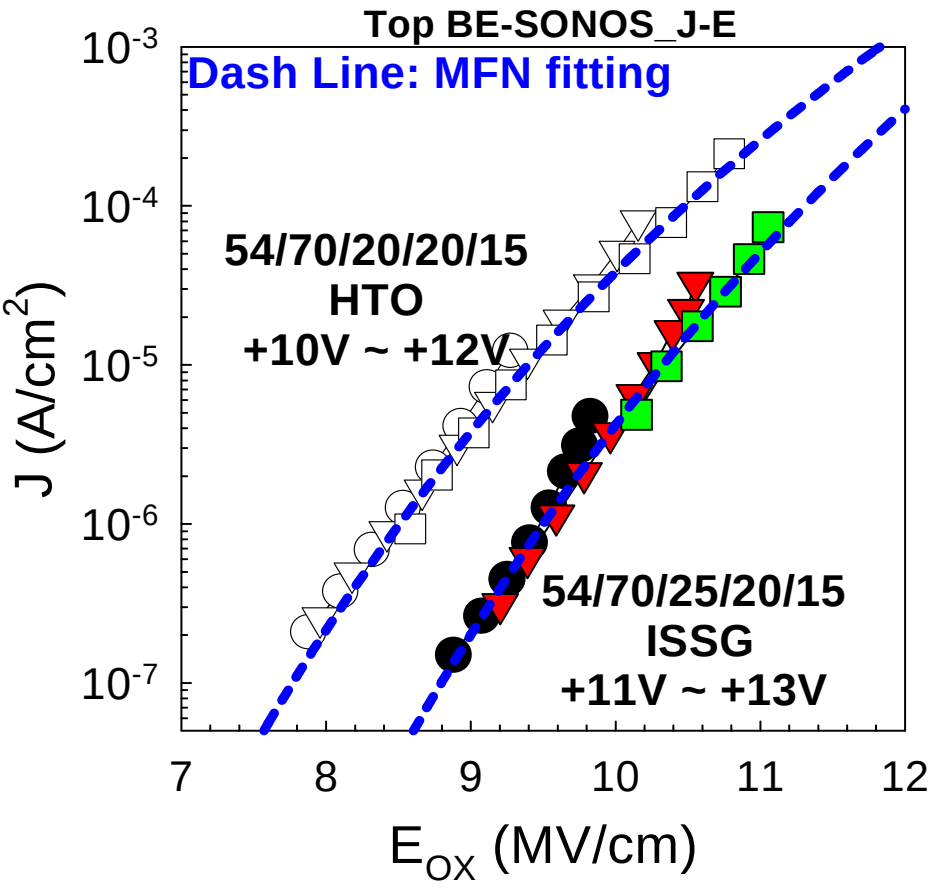


Fig. 7.6 J vs. E_{ox} of top BE-SONOS capacitors during erasing by using Eqs. (7-1) and (7-3). Different erase voltages follow the same trend. Both samples can be well fitted by MFN model.

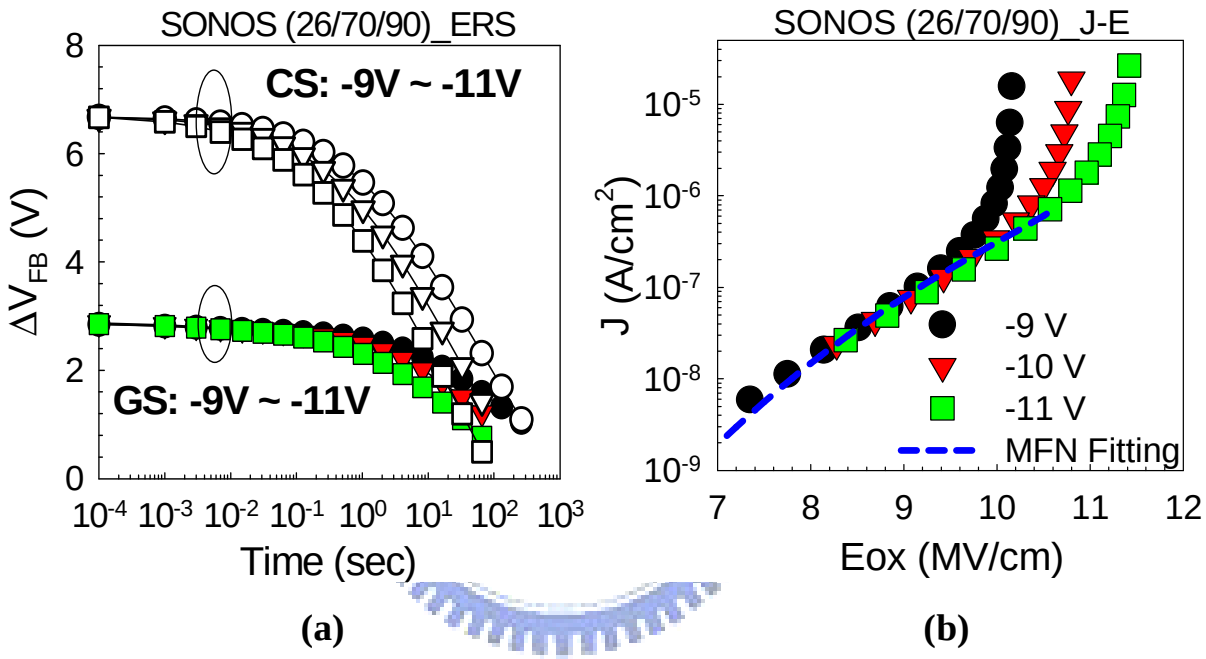


Fig. 7.7 (a) Erase characteristics and (b) J vs. E_{ox} of SONOS (26/70/90Å). The erase speed is much smaller than SoNOS (Fig. 7.1(b)). At initial erasing, the dominant erase mechanism is electron de-trapping while hole tunneling dominates after long erasing time, and the J-E curves follow MFN equation.

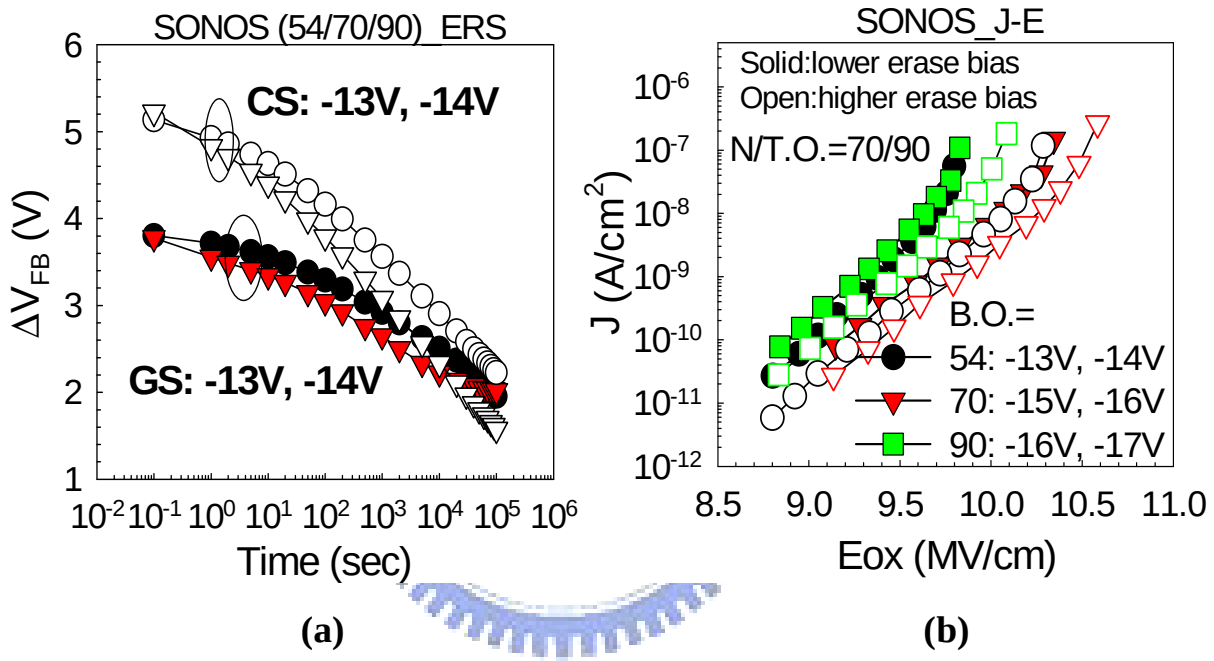


Fig. 7.8 (a) Erase characteristics of SONOS (54/70/90Å). The erase speed is much slower than SONOS with thinner B.O. (b) J vs. E_{ox} of 54/70/90Å, 70/70/90Å, and 90/70/90Å. The J-E curves are very scattered for different B.O. thickness and erase conditions. Electron de-trapping contributes to charge loss.

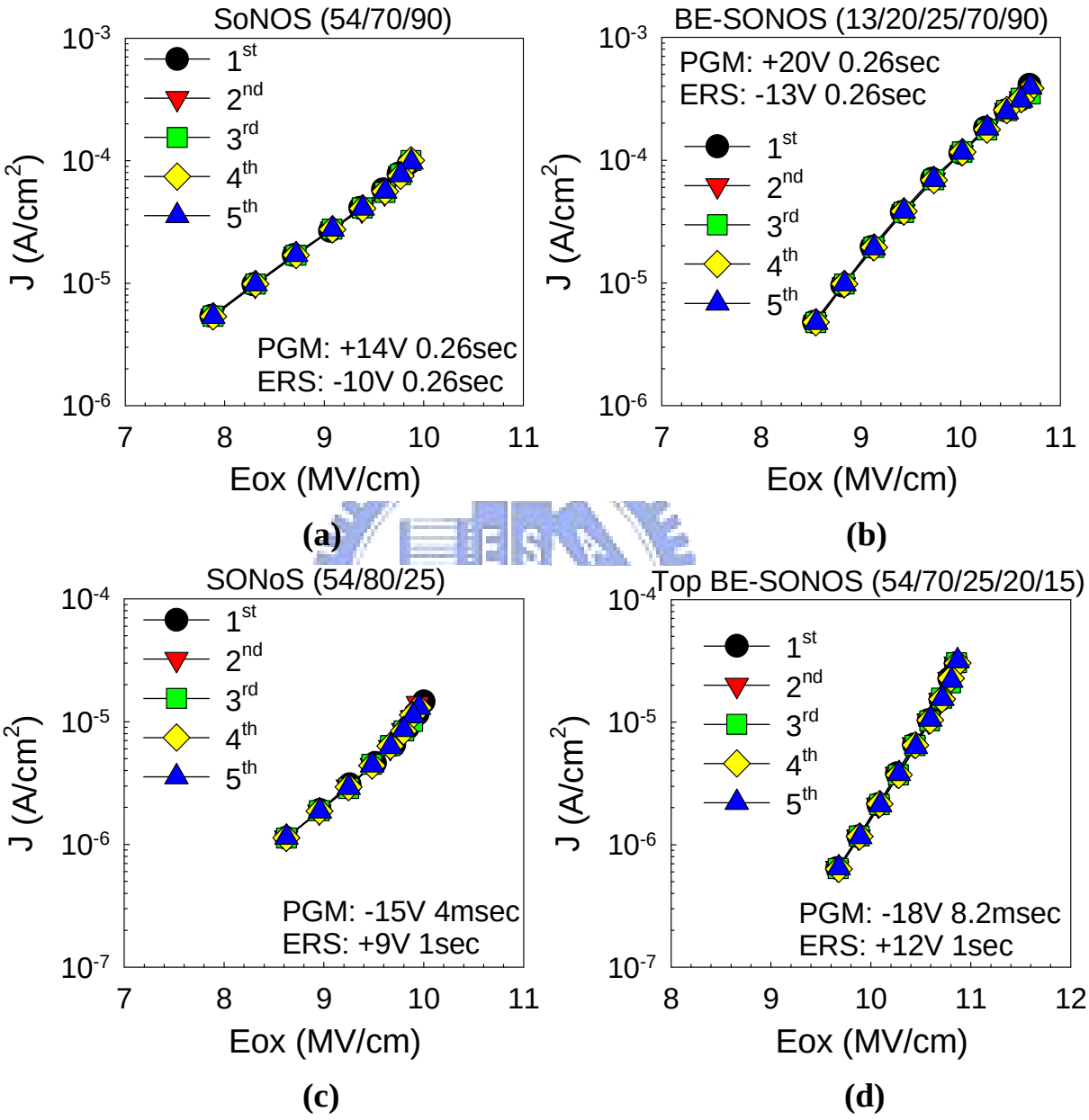


Fig. 7.9 J vs. E_{ox} curves of (a) SoNOS (20/70/90Å), (b) BE-SONOS (13/20/25/70/90Å), (c) SONoS (54/80/25Å), and top BE-SONOS (54/70/25/20/15Å). J-E curves are simply identical after several refill times. Hole-tunneling injection can be repeated continuously.

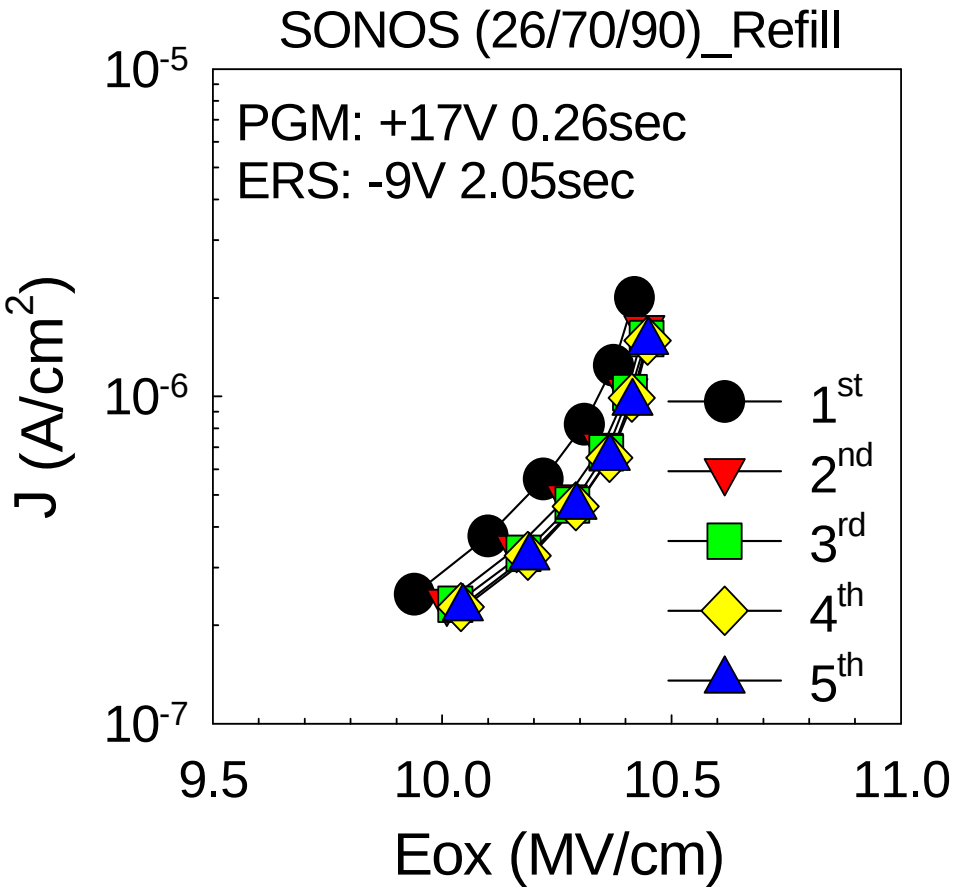


Fig. 7.10 J vs. E_{ox} curves of SONOS (26/70/90Å). The J slightly decreases during refill. Some electron de-trapping occurs during erasing. Finally, the erasing current J mainly comes from hole tunneling.

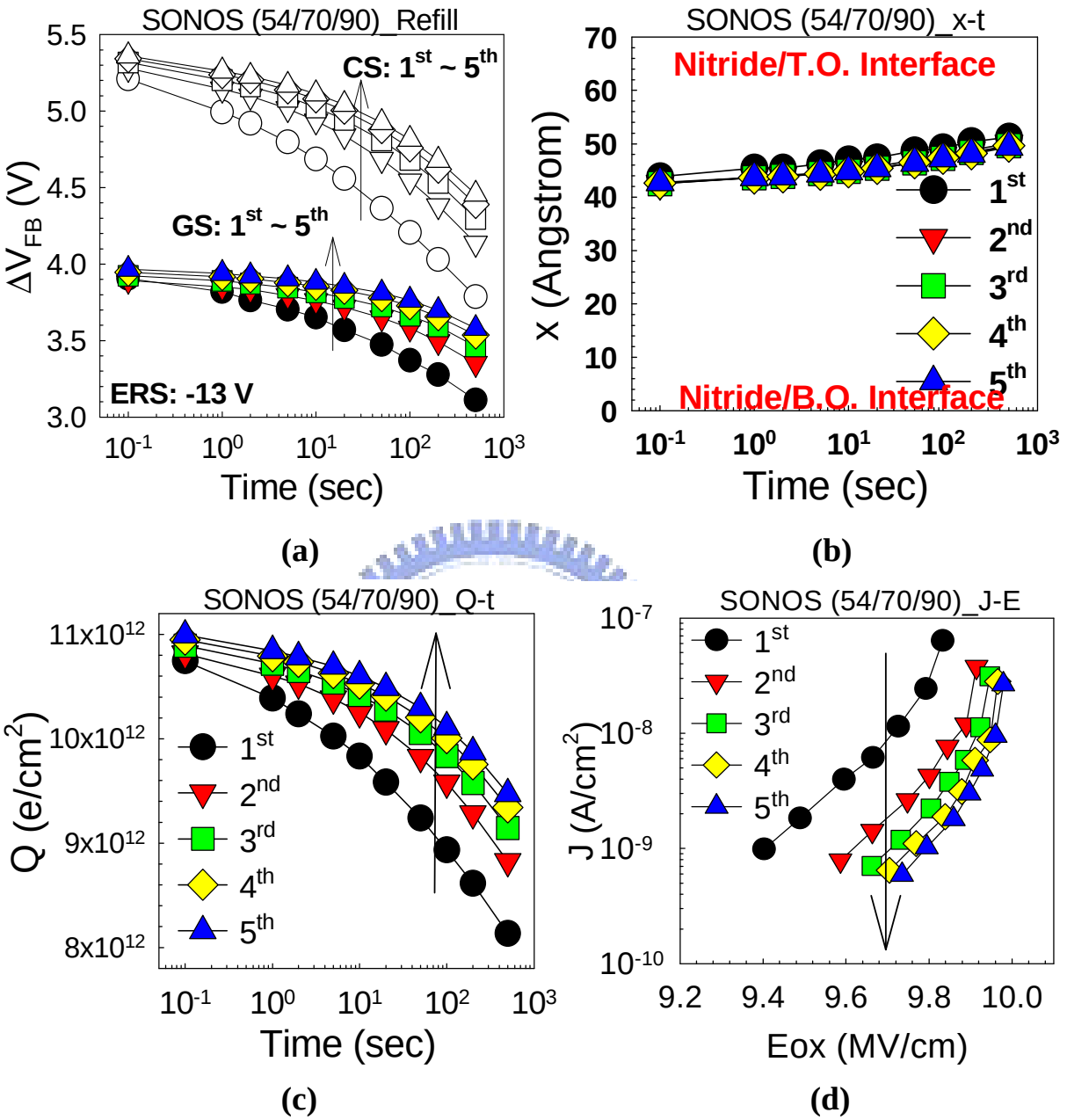


Fig. 7.11 (a) Refill characteristics of SONOS (54/70/90Å). The ΔV_{FB} decreases during refill. (b) X-t and (c) Q-t during refill transformed (a). During $-V_G$ stressing the x is slightly increased, but the Q is decreased. After refill sequence x-t plot is repeated, but charge loss is significantly decreased. It means that the refill characteristic does not come from the charge vertical profile modulation, but comes from energy spectrum shift. (d) J vs. E_{ox} curves. The J decreases during refill. Electron de-trapping occurs during erasing, and the energy level of injected electrons changes from shallow to deep, which results in smaller J.

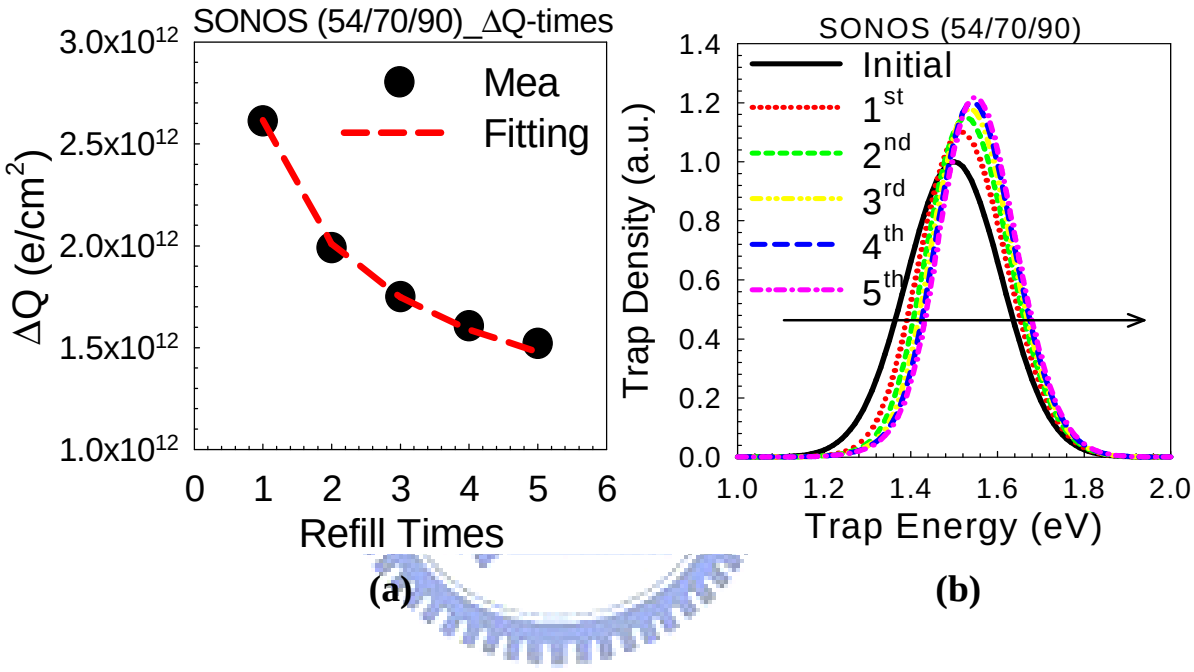


Fig. 7.12 (a) Charge loss vs. refill times of experimental data and mathematical model fitting. The experimental data can be well fitted by mathematical model. (b) Simulated results of energy spectrum. Each refill sequence shifts the trapping energy higher (blue shift) and the distribution tighter, and it finally saturates.

CHAPTER EIGHT

STUDY OF CHARGE TRANSIENT BEHAVIORS OF SONOS-TYPE DEVICES USING PULSE-IV TECHNIQUE

OUTLINE

8.0 Introduction

Charge-trapping (CT) devices have gained great attention in non-volatile memory applications. However, it is hard to monitor the "real" trapped charge behaviors using conventional DC-IV measurement, especially for the memory with serious hysterisis. Recently, pulse-IV techniques have been developed to characterize traps in high-*k* gate dielectrics of CMOS logic devices [8.1-8.4], and they mainly deal with drain current transient response and fast NBTI behaviors. However, few studies talked about the applications on SONOS-type memory.

In this chapter, we developed a memory-like operation with program/erase pulses, together with reading immediately after P/E or concurrently with the applied pulses. The transient tunneling current, fast program/erase/read operations, and fast retention relaxation can be accurately characterized. Using this new technique we have studied the transient behaviors of SONOS-type devices exhaustively. This new characterization method also opens a new pathway to study quasi-non-volatile memory for new applications.

8.1 Pulse-IV Technique and Setup

We designed different pulse-IV setup for characterizing large area (500μm × 500 μm) capacitors (n^+ source/drain, p-well, and p^+ poly gate) and small dimension (L ~ 50nm and W ~ 0.2μm) transistors.

The pulse-IV setup for transistors is shown in Fig. 8.1(a). The pulses are applied to the gate (V_G) and drain (V_D) while source current is measured immediately after P/E. The source current (I_S), which is nearly equal to drain current (I_D), is converted to voltage signal by using a fast current to voltage amplifier. Arbitrary waveforms can be generated to design any specific program/erase/read sequence. The oscilloscope can simultaneously collect V_G and I_D waveforms.

For capacitors, the pulse-IV setup is shown in Fig. 8.1(b). The pulse is only applied to

gate while the drain, source, and body are connected together (capacitors in this study are fabricated with source/drain and body contacts). The total current of source, drain and body is then measured by the oscilloscope.

Detailed cable connection, shielding and impedance matching are carefully arranged to eliminate spurious responses.

8.2 Transient Tunneling Currents of Capacitors

In this section, we first discuss the transient tunneling currents of various capacitors, including SOS, SNS, SONS, and SONOS. In addition to investigate gate voltage and pulse width dependence, we also examine the area and temperature dependence. Therefore, the detailed transient charging behaviors of various SONOS-type capacitors will be discussed extensively.

8.2.1 SOS Capacitor

We first measured transient tunneling current of SOS (25Å) capacitor for a reference and calibration, as shown in Fig. 8.2. This standard gate oxide capacitor with no trapping layer shows no spurious response for various gate voltages (Fig. 8.2(a)) and pulse widths (Fig. 8.2(b)), indicating that our setup does not generate detectable noise. Figure 8.2(c) also shows the corresponding band diagram under $+V_G$ operation. Both substrate electron tunneling current and gate hole tunneling current contribute to total tunneling current.

8.2.2 SNS Capacitor

Next, we measured the transient tunneling current behavior of SNS (133Å) capacitor, which does not have B.O. and T.O., as shown in Fig. 8.3. The tunneling current is initially high but then gradually decreases and saturates. The transient behavior is independent of pulse width (Fig. 8.3(b)), and similar for all gate voltages (Fig. 8.3(a)). The pulse width

independence suggests a transient behavior, such as trapping. A reasonable explanation is that during the tunneling current measurement, some electrons are trapped in the bottom portion while holes are trapped in the top portion of the nitride (section 4.1.3). Therefore, the substrate electron tunneling current decreases as electrons are trapped near the bottom portion of the nitride while gate hole tunneling current also falls at the rate of hole trapping in the top portion of the nitride (the corresponding band diagram is shown in Fig. 8.3(c)). The decreased substrate electron tunneling current and gate hole tunneling current result in decreased transient tunneling current.

8.2.3 SONS Capacitor

The transient tunneling current of SONS (54/114Å) capacitor is shown in Fig. 8.4. Interestingly, it behaves quite differently from the SNS. The tunneling current gradually increases and then saturates. Even though there is no T.O., we still expect the tunneling current of SONS comes mainly from electron tunneling from the substrate. On the other hand, because there is substantial gate hole injection, some hole trapping occurs (section 4.1.3). This hole trapping leads to enhanced electron tunneling and in turn increases transient tunneling current. Figure 8.4(c) shows the corresponding band diagram.

8.2.4 Area and Temperature Dependence

We have successfully demonstrated that the transient behaviors of electron/hole trapping can be directly monitored by our pulse-IV technique. In order to further confirm these transient behaviors we also investigate the area and temperature dependence of SNS and SONS, as shown in Fig. 8.5. For the area dependence (Fig. 8.5(a)), in order to fairly compare the I_{total} is normalized to area ($J_{total} = I_{total}/area$). We find that all transient tunneling currents of different area almost merge together, implying that these transient behaviors are independent of area. For the temperature dependence (Fig. 8.5(b)), the increased temperature enhances the

tunneling current but the transient behaviors are almost the same. Therefore, we further demonstrate that our pulse-IV technique can be adequately used to monitor the “real” charge transient behaviors.

8.2.5 SONOS Capacitor

The transient tunneling current of SONOS (54/77/50Å) capacitor is shown in Fig. 8.6. Figure 8.6(a) shows that the CV curve has a large shift owing to the trapped charges. Contrary to SNS and SONS, the transient tunneling current rises initially but then drops sharply and decreases to almost zero. This very different transient behavior (from SNS and SONS) may be explained by the T.O. in SONOS. The T.O. greatly reduces gate hole injection and thus allows the accumulation of trapped electrons in the nitride. In turn the trapped electrons suppress the tunneling current eventually. On the other hand, both SNS and SONS have simultaneous gate hole injection that limits the trapped electron density. As a result, the tunneling current of SNS and SONS is not limited.

Previously, we have shown that SONOS with thicker nitride (>70Å) exhibits high capture efficiency characteristics [5]. Therefore, we used the theoretical model (based on the fully captured assumption) shown in Table 2 to simulate the transient behavior of SONOS (54/77/50Å). Figure 8.6(b) shows that the experimental I_{total} can be well fitted by using reasonable parameters (ϕ_B = 3.1eV and $m_{ox} = 0.5m_0$). This result further supports that SONOS with sufficient nitride thickness indeed can capture most of the injected electrons.

From above results, we find that the transient tunneling currents are strongly related to the detailed charge trapping behaviors as well as the device structures.

8.3 DC and Transient Characteristics of Transistors

After discussing the transient tunneling currents of various capacitors, we next investigate the DC and transient characteristics of small area transistors. For the practical

applications, we monitor the drain current instead of total tunneling current. Moreover, we intentionally designed SONOS-type devices with or without a thin tunnel oxide to enhance the transient signal, and silicon-rich nitride is used to provide even higher trap density.

8.3.1 DC-IV Characteristics

The conventional DC-IV measurements are carried out by dual-voltage sweeps. The results of SONS (30/50Å) in Fig. 8.7 show that all transistors have very significant hysteresis. This indicates that the devices are easily programmed/erased under low voltages (read disturb). Moreover, silicon-rich nitride shows much larger hysteresis than the standard nitride. This suggests that silicon-rich nitride is more efficient in trapping charges at low voltage [8.5]. Furthermore, p-channel transistors show slightly larger memory window than n-channel transistors. Therefore, we focus on p-channel transistors in this work.

The large hysteresis also suggests that the conventional DC-IV measurement to define threshold voltage [8.6] is not appropriate since these transistors are easily disturbed during DC measurements. As we shall see later pulse-IV is needed to accurately characterize these transistors.

8.3.2 Pulse-IV Characteristics

In Fig. 8.1(a) pulse-IV setup for transistor measurement, arbitrary wave forms can be generated to design any specific program/erase/read sequence. The oscilloscope can simultaneously collect V_G and I_D. Figure 8.8(a) shows the designed V_G and V_D pulses during programming/erasing (P/E) cycling stress. Under P (E) phase, the V_G is positive (negative) while the V_D keeps at 0V. Under reading phase, the V_G is –2V while the V_D is –1V. We measure the I_D immediately (within 1μs) after P/E to monitor the instant current response.

The typical drain current response for the p-channel SONS (30/50Å) is shown in Fig. 8.8(b). Under +FN (+7V 1μs) programming, the gate holes inject into nitride. Therefore, the

programmed state (PV) has smaller drain current (~ 8μA). On the other hand, under –FN (–7V 1μs) erasing the gate electrons inject into nitride to compensate the trapped holes, leading to larger drain current (~ 18μA) at erased state (EV). Large current difference (~ 10μA) can be obtained after P/E.

8.4 Applications in Quasi-Non-Volatile Memory

Since these transistors can be programmed/erased at low voltages, we next consider the applications in quasi-non-volatile memory. In this chapter, the program/erase, endurance, and temperature/e-field dependence retention characteristics will be discussed exhaustively.

8.4.1 Program/Erase Transient Characteristics

Instead of the conventional V_T vs. time measurements, we measure I_D immediately after program/erase pulse because this is what actually measured by the sense amplifier.

The program and erase transient behaviors of SONS (30/50Å), SONoS (30/50/8Å), and SoNOS (13/50/43Å) are shown in Fig. 8.9. Figures 8.9(a)-(c) show that the devices are easily programmed within 1μs at low V_G bias. Moreover, SONS shows much faster program speed than SONoS or SoNOS. The reason is because SONS does not have tunnel oxide, thus provides very fast injection speed (nitride has much lower barrier height than oxide). After programming, I_D decreases because of the hole injection in p-channel transistor. At longer programming time I_D approaches zero. Figures 8.9(d)-(f) show that SONS has much faster erase speed, and its erase speed is comparable with the program speed. This is because nitride has similar tunneling barrier (~ 2eV) for both electron and hole.

In Fig. 8.9, SoNOS needs reverse polarity for program/erase because SoNOS is programmed/erased by channel-injection while SONS and SONoS operate through gate-injection.

8.4.2 Endurance Characteristics

The endurance characteristics of various transistors are compared in Fig. 8.10(a). Under similar external e-field (11 ~ 12MV/cm) SONS shows the largest memory window. This is caused by more efficient injection when the tunnel oxide is removed. Moreover, the introduction of silicon-rich nitride also enhances the charge-trapping characteristics.

Figure 8.10(b) shows endurance characteristics of SONS under different bias voltages and P/E time. The results show that the memory window increases with larger operation voltages. However, the endurance is degraded because higher e-field causes more channel injection through the B.O. that degrades the read current. Therefore, reducing the operation voltage is necessary to improve the endurance. At V_G < 6V, endurance can be greater than 10^{10} cycles, suitable for high-endurance quasi-non-volatile memory applications.

8.4.3 Retention Characteristics

We also measured the e-field and temperature dependence retention characteristics of SONS, SONoS, and SoNOS within very short time (from 1μs to 0.1s), as shown in Fig. 8.11, to further investigate the transient charge relaxation (retention) behaviors.

To monitor the e-field dependence of charge loss (Figs. 8.11(a)-(c)), we applied different external gate voltages (waiting voltage) during retention. We find that the retention characteristics of all devices are strongly dependent on external e-field since the external charges could easily inject into nitride by direct tunneling at low voltages. The larger waiting voltage results in larger e-field and larger injected current. The field dependence of SONS is more significant than SONoS because SONS did not have a tunnel oxide to block the tunneling current. Moreover, for the retention characteristics at 0V waiting voltage, SONS has worse behavior as compared with SONoS. This suggests that inserting a thin oxide between nitride and gate can improve the retention behavior, however, it suffers slower P/E speeds. Therefore, there is a trade-off between retention and P/E behaviors.

On the other hand, we also studied the retention characteristics by using in-situ high-temperature Pulse-IV measurement, and the results are shown in Figs. 8.11(d)-(f). Surprisingly, the retention characteristics of all devices are very insensitive to the measuring temperature (from 25^{o}C to 150^{o}C). Since the thermionic emission processes such as Frenkel-Poole (FP) emission, which is mentioned in section 2.2.6, should be very sensitive to temperature, we suggest that for SONS, SONoS, and SoNOS devices the retention charge loss mainly comes from external charge injection (direct tunneling) to recombine the trapped charges but not from the charge de-trapping through thermionic emission processes. This result also suggests that the nitride traps are indeed very “deep” such that no fast de-trapping occurs within seconds even at high temperatures.

8.5 Summary

Pulse-IV measurements have been successfully applied to study the transient charging behaviors of various SONOS-type capacitors. For SNS, we found that the transient tunneling current decreases during the V_G pulse since the electrons are trapped near the bottom portion of the nitride, and holes are trapped in the top portion of the nitride. On the other hand, the transient gate current of SONS increases during the V_G pulse due to the hole trapping in the top portion of nitride. Besides, their transient behaviors are independent of gate voltage, pulse width, device area, and temperature. Since the T.O. in SONOS can block the gate injection its transient tunneling current rises initially but then drops sharply and decreases to almost zero. Theoretical model based on fully capture assumption could well fit its transient tunneling current.

We also used pulse-IV technique to investigate the fast charge-injection and relaxation of various SONS, SONoS, and SoNOS transistors. Since these transistors suffer from read disturb during V_T extraction by DC-IV measurement, our pulse-IV technique is needed to monitor the instant drain current after all kinds of reliability tests without disturb. We

demonstrated that under lower voltage operations (±6V 1μs) the SONS can provide very high endurance characteristic (10^{10} cycles) for quasi-non-volatile memory applications. We also proved that the major retention mechanism of these transistors comes from direct tunneling leakage but not from thermionic emission of traps. Therefore, the nitride can provide very "deep" traps and promise for good non-volatile memory.

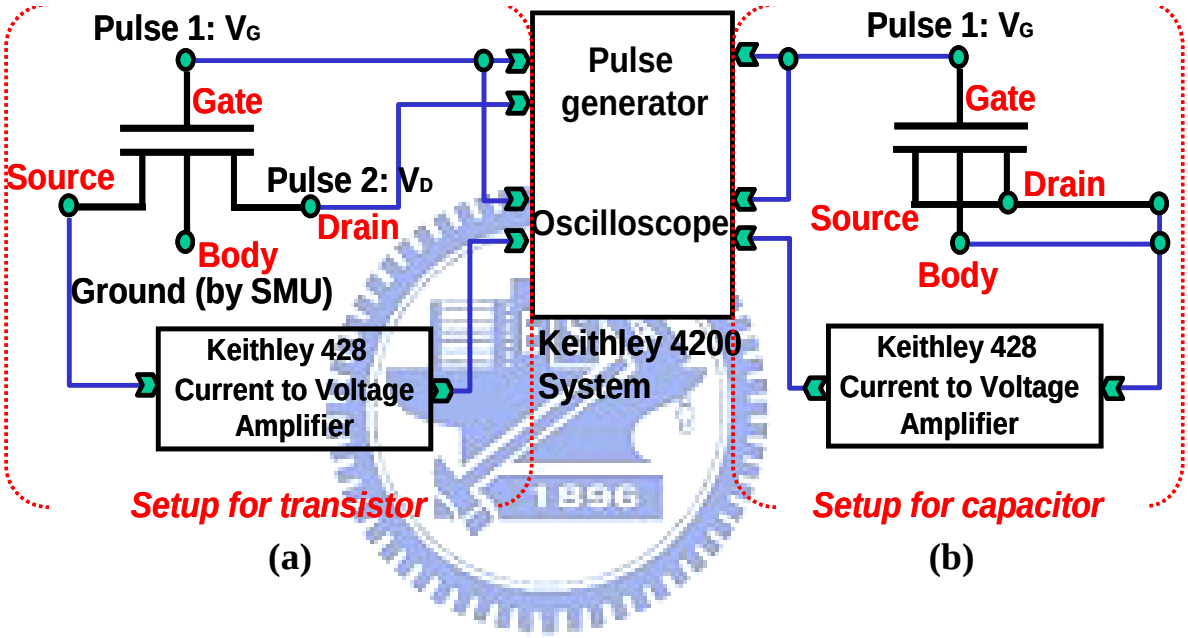


Fig. 8.1 Pulse-IV setup for (a) transistor and (b) capacitor measurements. For transistor, pulses are applied to the gate and drain while source is connected to a current-voltage amplifier. Both gate pulse and source current can be monitored by oscilloscope. For capacitor, pulse is only applied to gate, and source/drain/body are connected together to measure the total tunneling current.

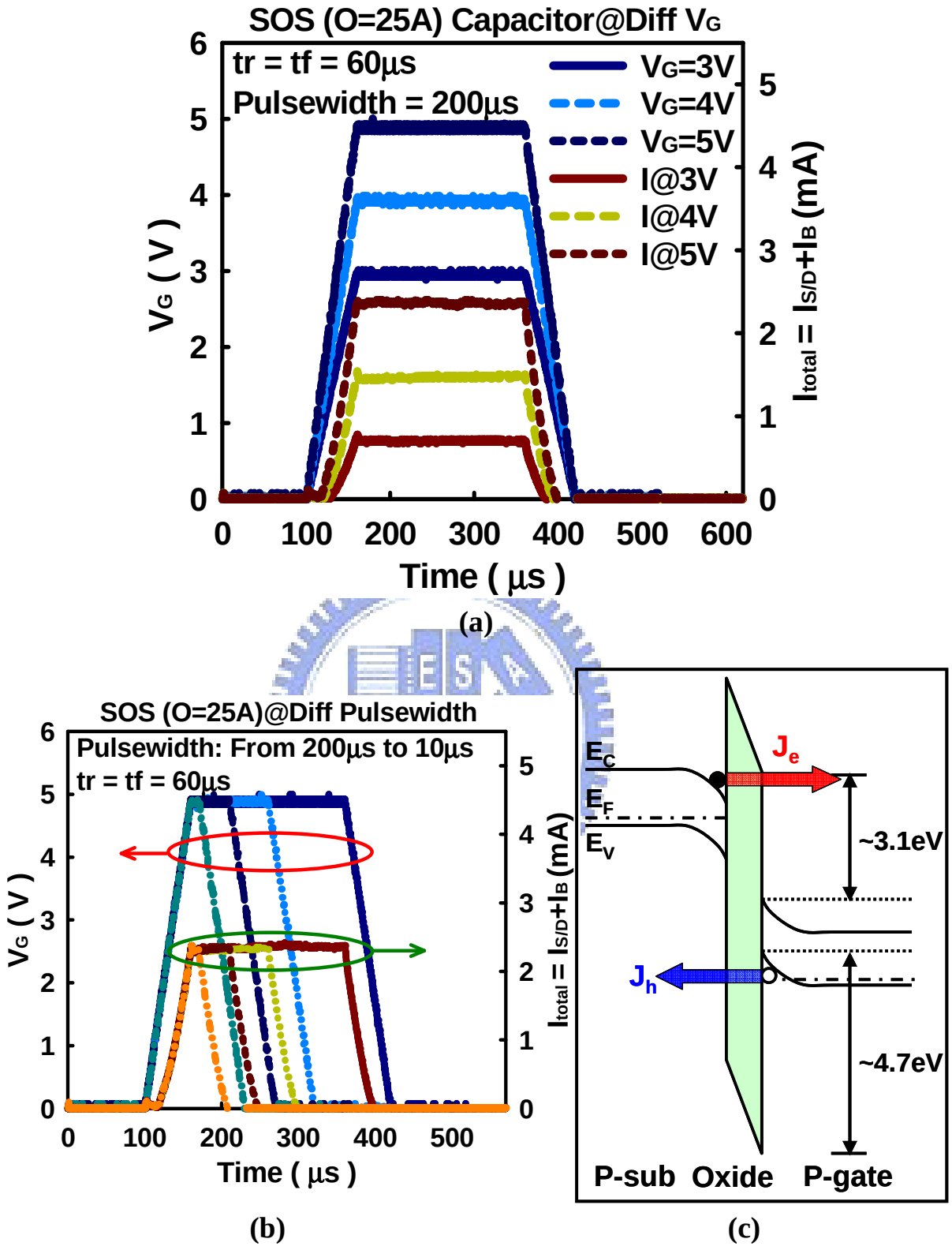


Fig. 8.2 Transient tunneling current of SOS (25Å) capacitor under various (a) gate voltages and (b) pulse widths. The I_{total} stays constant, and there is no transient relaxation for a pure gate oxide. This indicates that our measurement setup does not have spurious responses. (c) The corresponding band diagram under $+V_G$ operation.

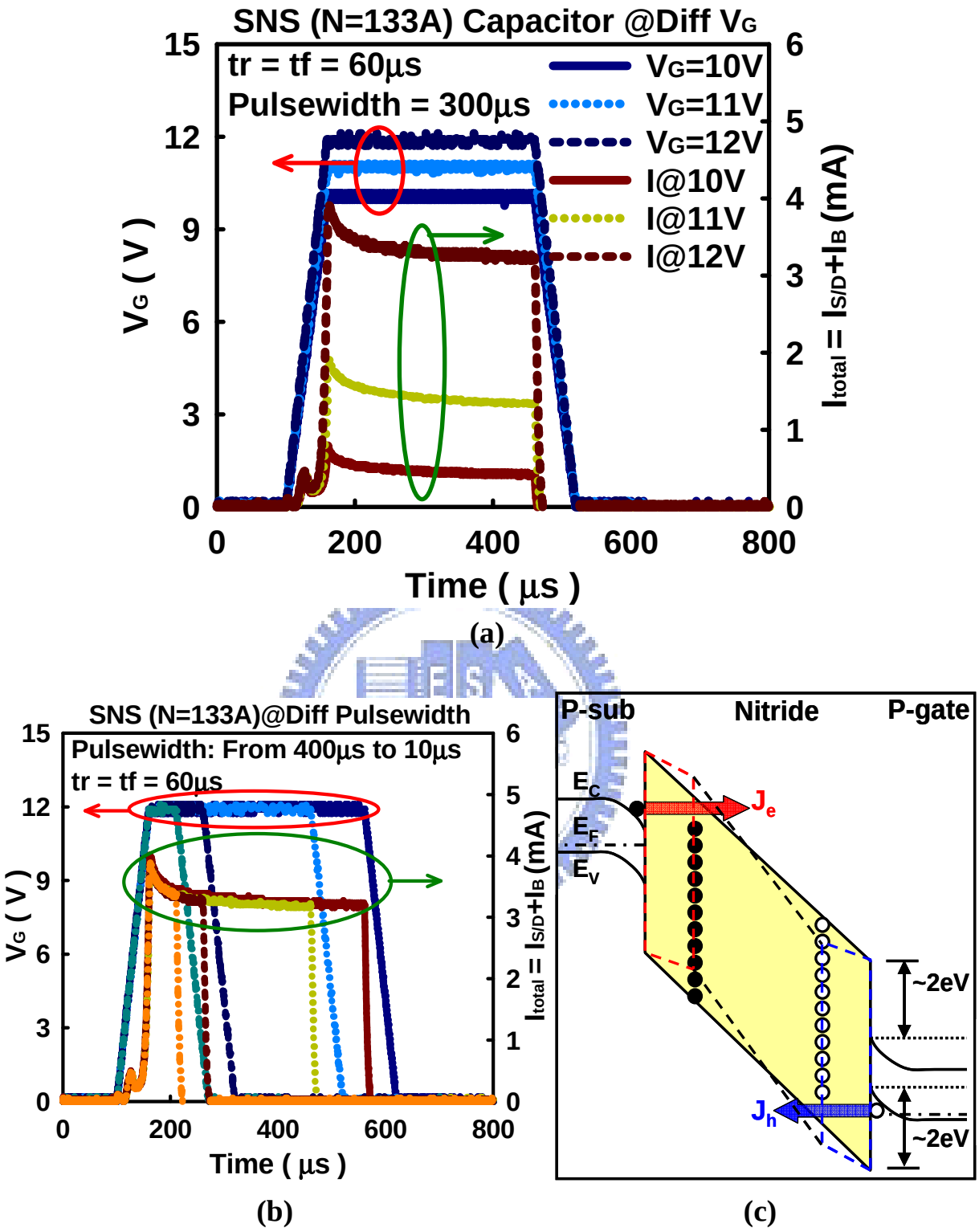


Fig. 8.3 Transient tunneling current of SNS (133Å) capacitor under various (a) gate voltages and (b) pulse widths. The I_{total} drops during the V_G pulse. This can be explained by the net electron trapping that results in decreased electron tunneling current. In (b), longer V_G pulse does not change the I_{total} relaxation behavior. (c) The corresponding band diagram under $+V_G$ operation.

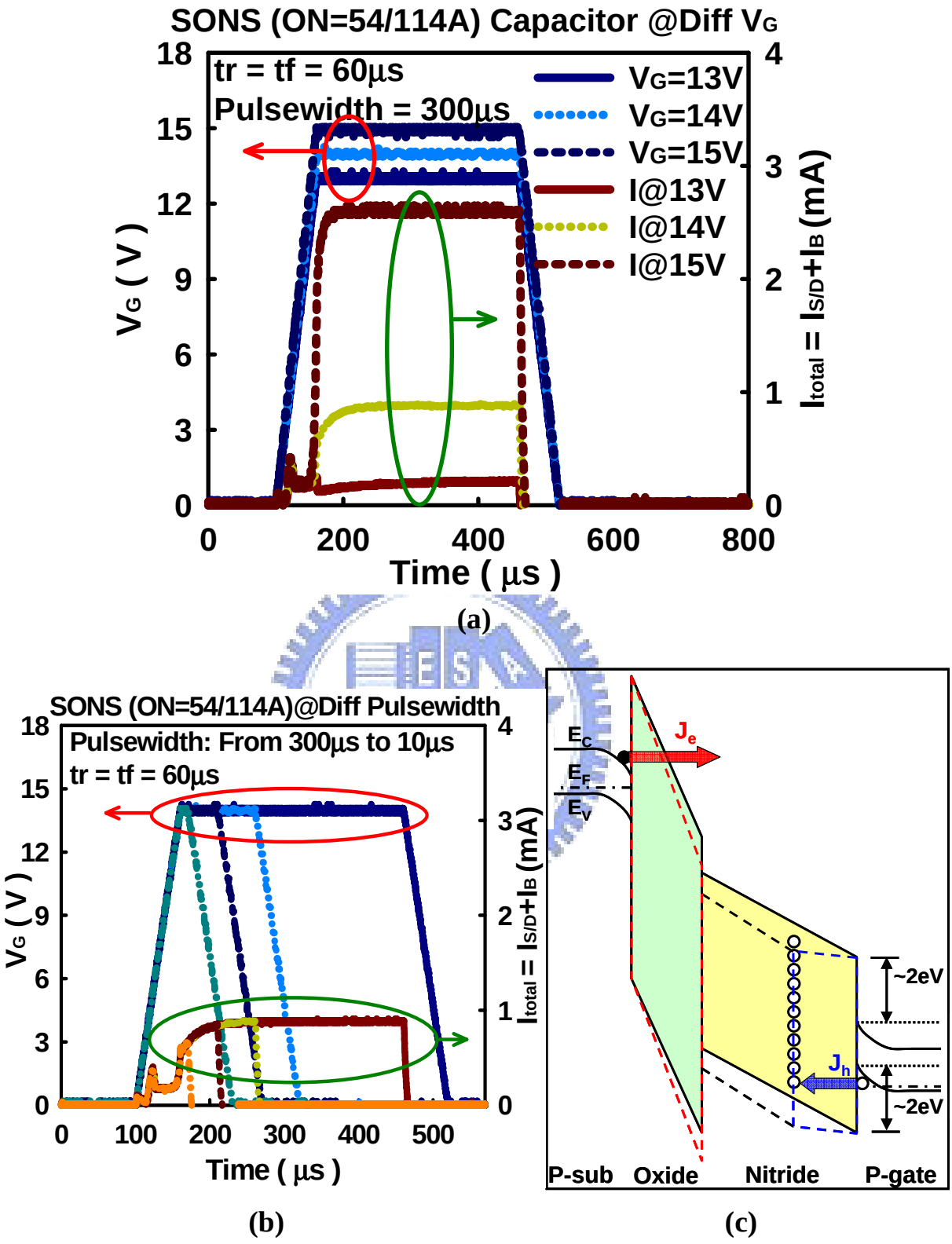


Fig. 8.4 Transient tunneling current of SONS (54/114Å) capacitor under various (a) gate voltages and (b) pulse widths. The I_{total} rises during the V_G pulse. This indicates that there is some hole trapping (coming from gate injection) that increases the substrate electron tunneling. (c) The corresponding band diagram under $+V_G$ operation.

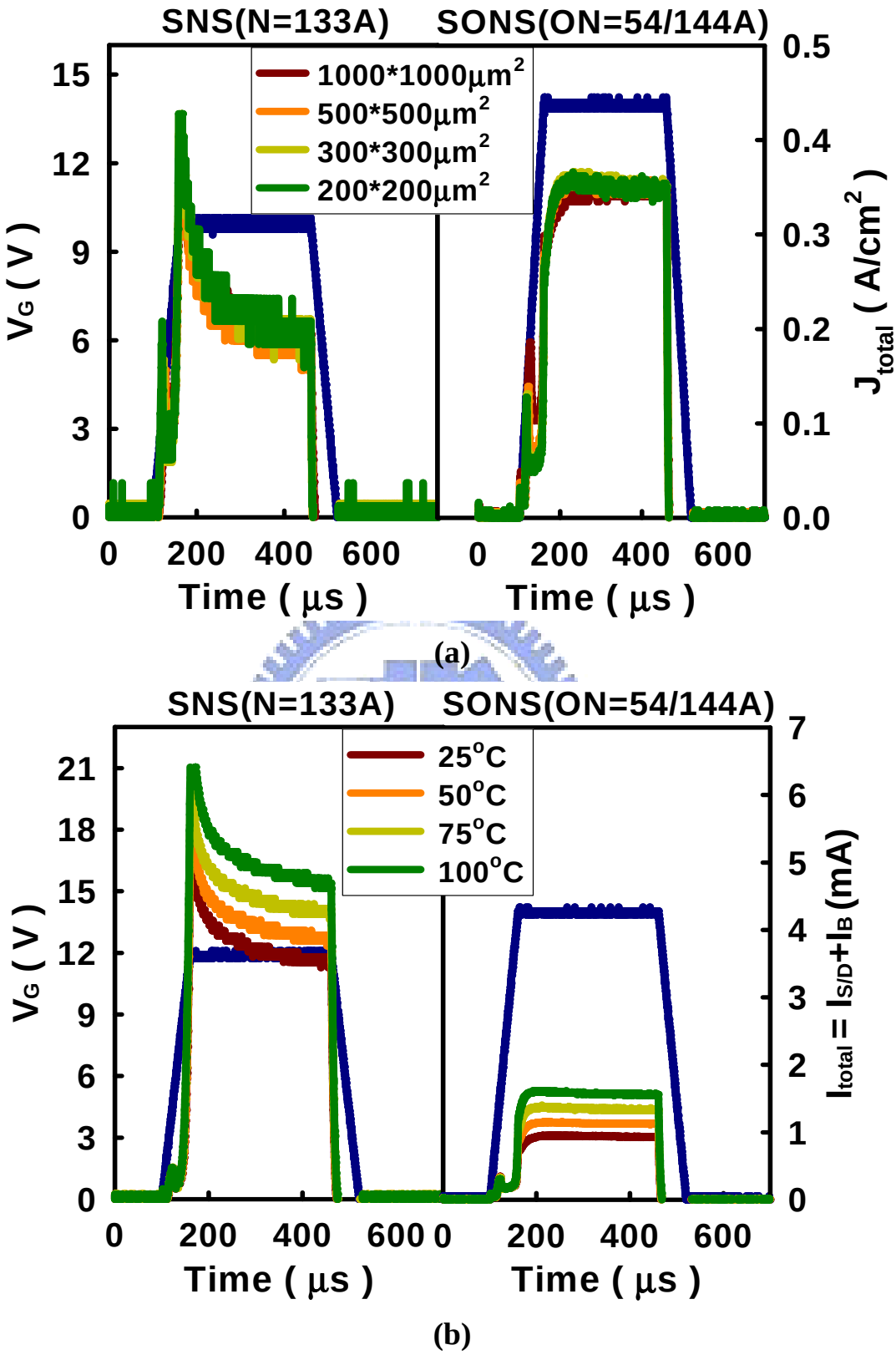
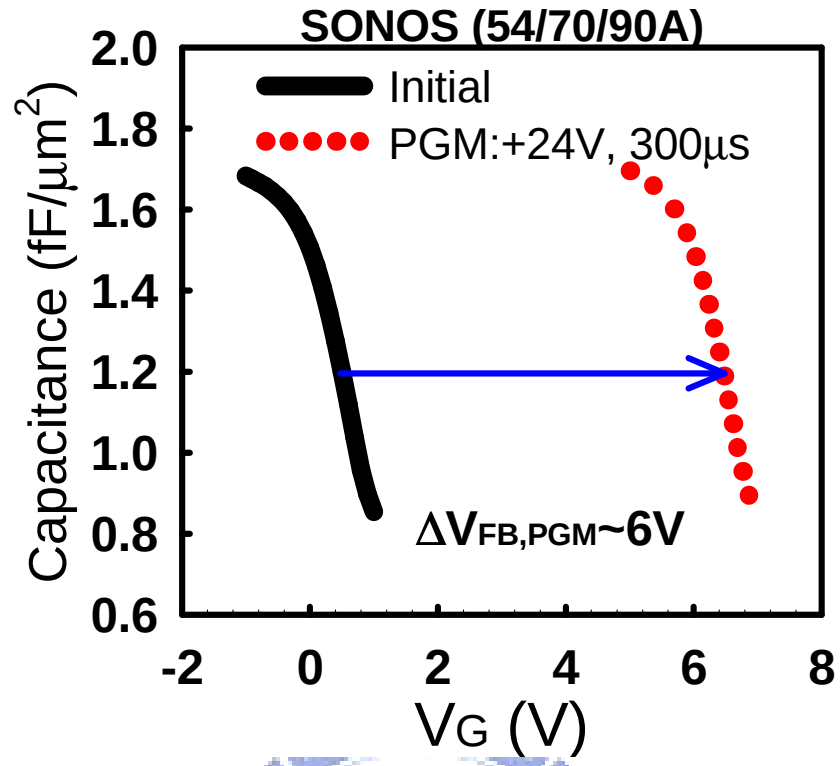
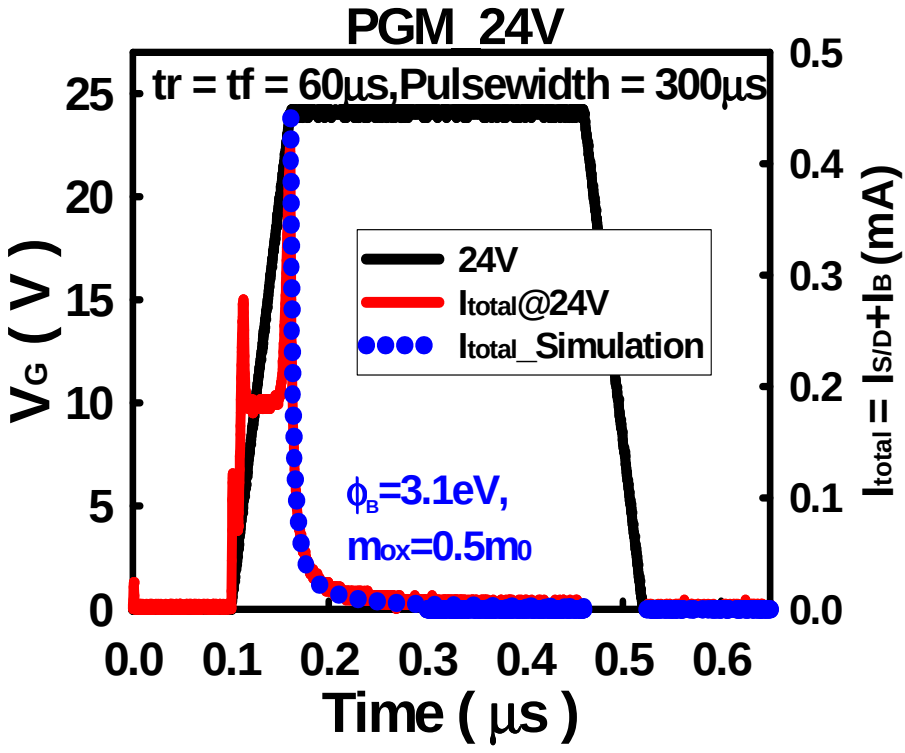


Fig. 8.5 (a) Area and (b) temperature dependence of SNS (133Å) and SONS (54/114Å). The I_{total} in (a) is normalized to area. The transient behaviors are independent of area and temperature.



(a)



(b)

Fig. 8.6 (a) CV curves of SONOS (54/70/90Å) capacitor before and after programming. (b) The transient tunneling current during +FN programming shows a large I_{total} initially but decreases afterwards. Moreover, the measured I_{total} can be well fitted with our model.

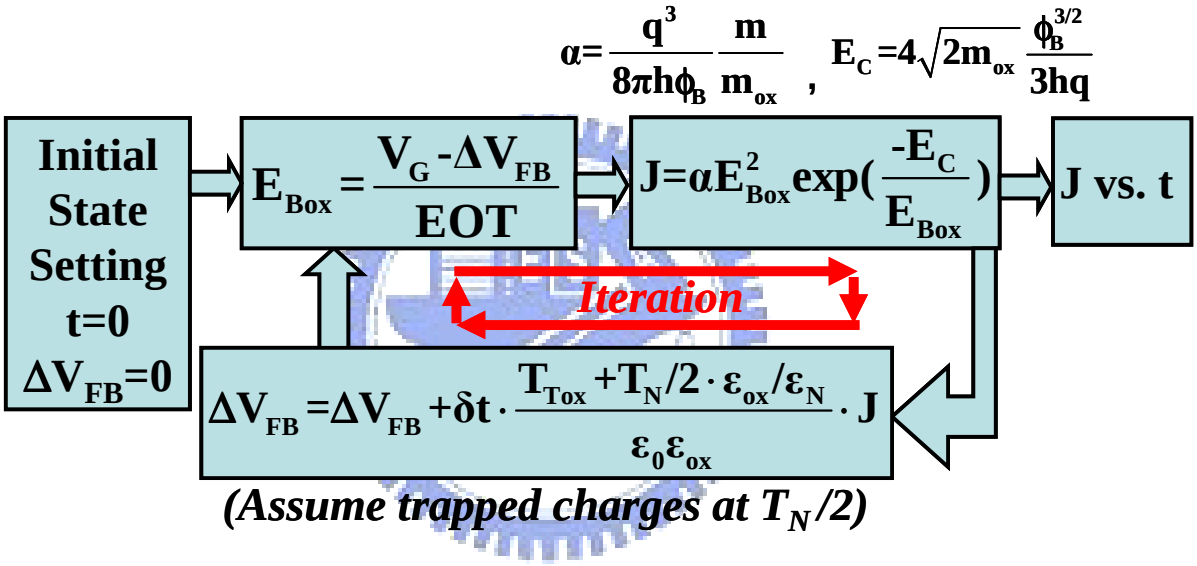


Table 8.1 Theoretical modeling flow chart for transient tunneling current modeling by assuming fully capturing.

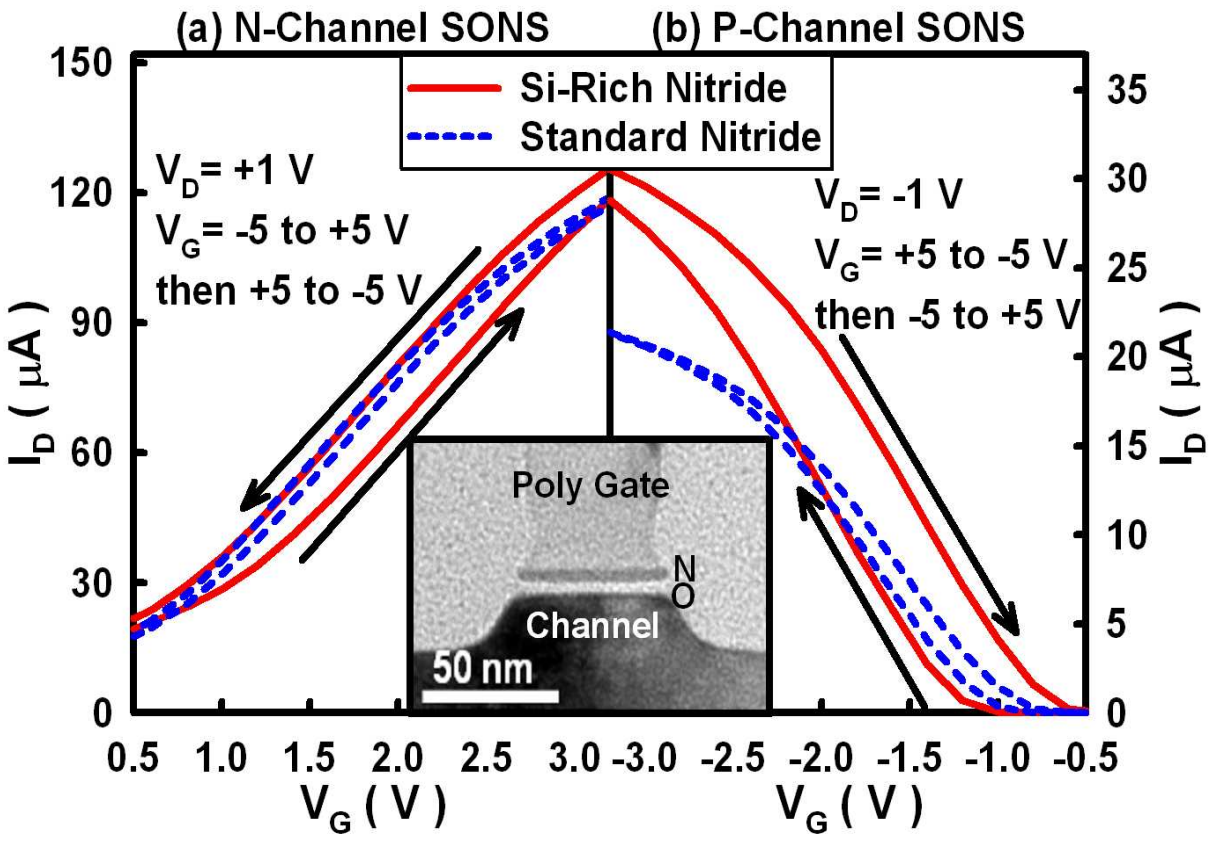
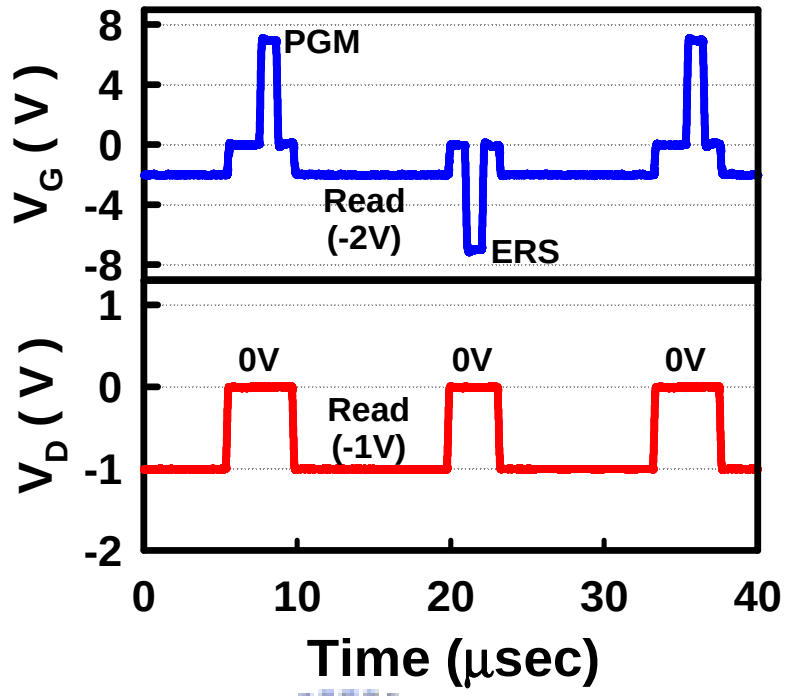
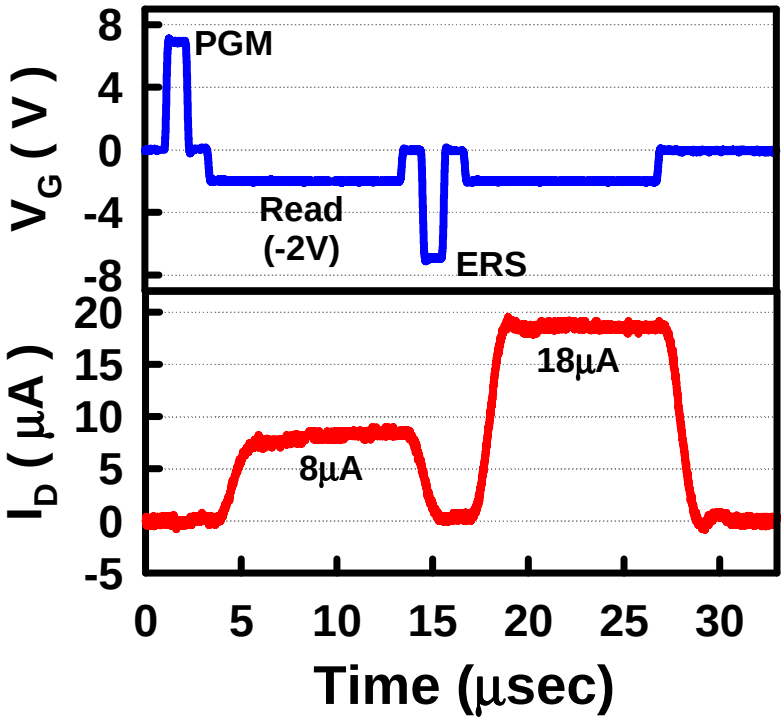


Fig. 8.7 Comparison of dual-sweep DC-IV for SONS with standard and silicon-rich nitride-trapping layer. (a) N-channel transistors. (b) P-channel transistors. Gate voltage sweeps from –5V to +5V, and then +5V to –5V for n-channel, and it sweeps reversely for p-channel. The hysteresis direction is also indicated. The inset is the typical cross-sectional view of SONS device.



(a)



(b)

Fig. 8.8 (a) Designed V_G and V_D pulses for P/E and read. Reading (V_G = –2V and V_D = –1V) is performed immediately after P/E. (b) Typical measured drain current response during a P/E test. Large current difference (~ 10μA) is obtained after programming/ erasing.

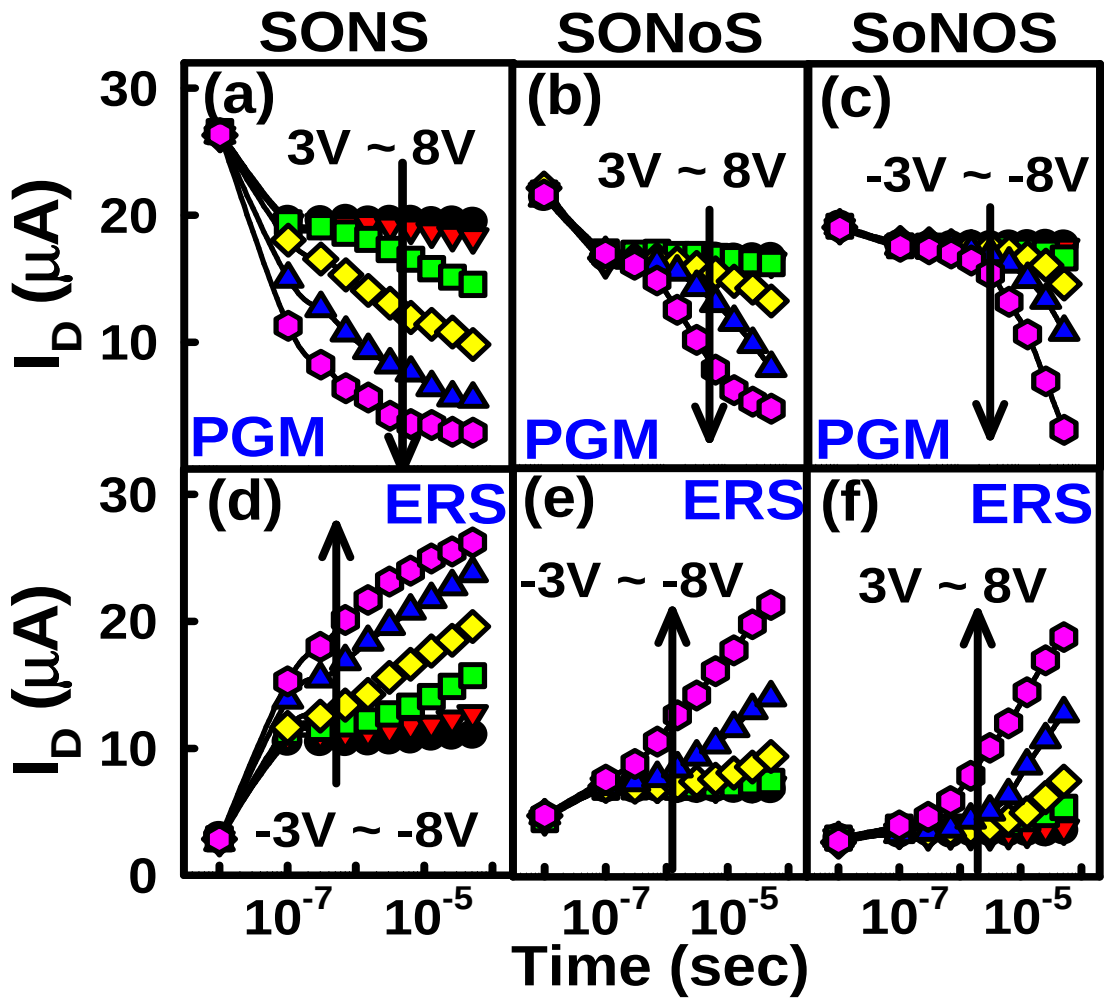


Fig. 8.9 Program and erase transient behavior of SONS ((a) and (d)), SONoS ((b) and (e)), and SoNOS ((c) and (f)) p-channel transistors. SONS shows the fastest program and erase speeds. SoNOS uses inverse polarity ($-V_G$ for the program, and $+V_G$ for the erase) because it is channel-injection mode.

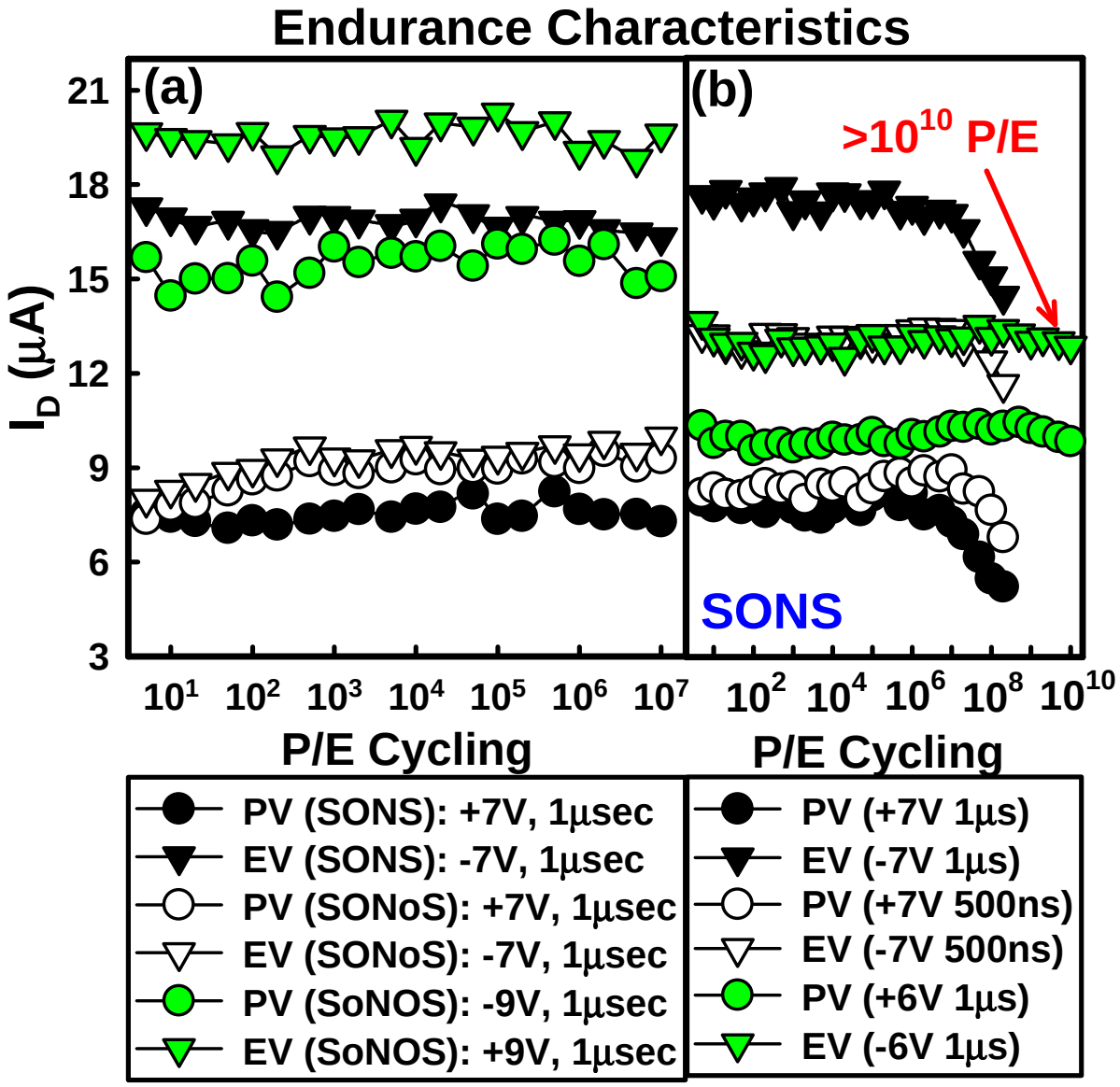


Fig. 8.10 (a) Endurance characteristics of SONS, SONoS, and SoNOS. SONS shows the best memory window. (b) Endurance characteristics of SONS device under different bias voltages and P/E time. At +/–6V operation, more than 10^{10} P/E cycling is achieved.

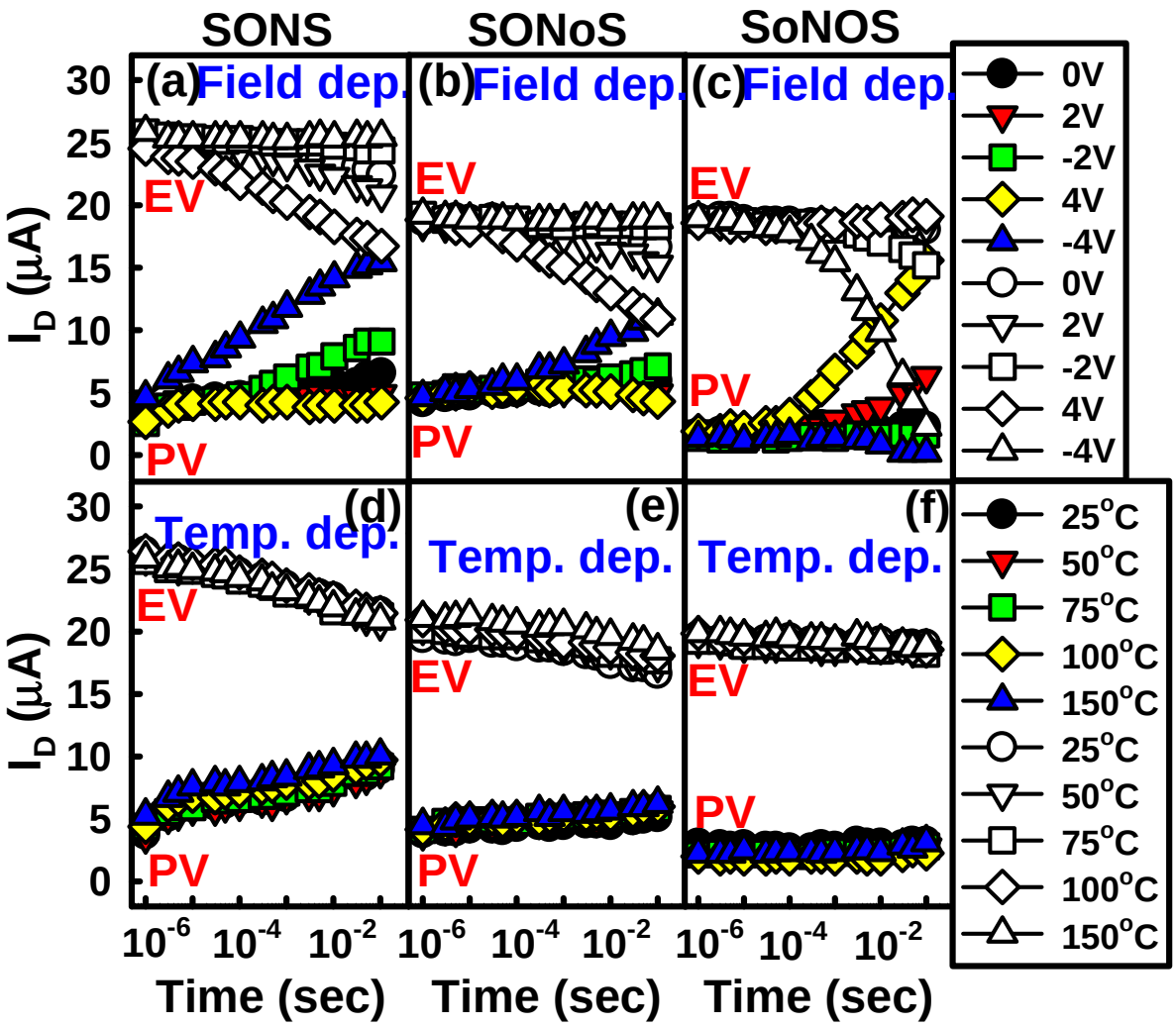


Fig. 8.11 (a)-(c) Field dependence and (d)-(f) temperature dependence of retention characteristics of SONS, SONoS, and SoNOS. SONS and SONoS are P/E by +/–8V 50μs while SoNOS is P/E by –/+8V 50μs before retention test. Different external gate voltages (waiting voltage) are applied for field-dependence retention test while different in-situ baking temperatures are applied for temperature-dependence retention test. The retention characteristics of all devices are sensitive to the waiting voltages, but not on the storage temperatures.

CHAPTER NINE

CONCLUSIONS

OUTLINE

9.1 Summary of Findings and Contributions

In this dissertation, the charge trapping characteristics of SONOS-type devices have been investigated extensively by using gate-sensing and channel-sensing (GSCS) method or pulse-IV technique. Our study provides in-depth physical understanding of trapped charge behaviors of SONOS-type devices.

In chapter 3, we provided the detailed discussion of our novel GSCS method. Both bulk trap model, where total charge density (Q) and mean vertical location (x) can be monitored simultaneously, and two-region approximation model, where the charges in the bottom portion of nitride (Q_1) and top portion of nitride (Q_2) can be monitored separately, are introduced. Based on these two models, we could successfully demonstrate our GSCS method on various SONOS-type devices. This GSCS method has a high accuracy against the thickness error of B.O., nitride, or T.O. Even if GS and CS capacitors have different injected charges due to the finite thickness differences in B.O., our GSCS method still provides high accuracy at high injection level.

In chapter 4, the applications of GSCS method on trapped charge vertical location and capture efficiency have been discussed in detail. By comparisons with various SONOS, SNOS, SONS, and SNS devices, we concluded that nitride bulk traps are the dominant traps. On the other hand, for SONOS and BE-SONOS with different nitride/T.O. compositions, the electron centroid is very close to the center of nitride after longer injection. This result also suggests that the injected charges are mostly trapped inside the bulk nitride instead of oxide/nitride interfaces. Compared the theoretical Q-t model with experimental Q-t data, we found that SONOS with nitride thicker than 70Å is has high enough capture efficiency, and the capture efficiency drops significantly when nitride thickness is only 35Å, then becomes negligible for a 20Å nitride. Therefore, the trap-layer engineering could not further improve the capture efficiency.

In chapter 5, we investigated the intra-nitride charge transport behaviors of SONOS-type

devices by using GSCS method. We found that for the electron injection (+FN program), the electron centroid migrates from the bottom interface toward the center of nitride. For the hole injection (–FN erase) in SONOS with a thin B.O. or BE-SONOS, holes first recombine with the bottom electrons and then gradually move upward, and finally the residual electron and hole centroids have vertical mismatch. However, the mismatch should be viewed as a snapshot of erased state, and should not be interpreted as two separate pockets of charges co-inhabiting the nitride. Since during P/E cycling most trapped electrons/holes are neutralized by the erasing holes/programming electrons, SONOS-type devices could still possess excellent P/E cycling endurance. On the other hand, for the electron de-trapping in SONOS with a thicker B.O., the trapped electrons de-trap first from the bottom portion of nitride, leading to upward charge centroid. For the high-temperature retention, within short-term baking (< 1day), the trapped electrons move to lower portion of nitride (intra-nitride transport); after long-term baking (> 1day), the charge loss mainly comes from the bottom portion of nitride. However, this intra-nitride transport is significant only at very high-temperature baking (> 200^{o}C), and the charge vertical or lateral spreading may not be the dominant retention mechanism at lower storage temperature.

In chapter 6, the charge-trapping behaviors of gate-injection operated SONOS-type devices have been investigated in detail. The results of gate-injection operated SONOS-type devices are very similar with that of channel-injection. For –FN electron injection from gate, the charge centroid is close to the center of nitride; for +FN hole injection from gate, after e^{-}/h^{+} recombination the residual holes are accumulated in the top portion of nitride while the residual electrons are accumulated in the bottom portion of nitride (e^{-}/h^{+} vertical mismatch). Although there is an e^{-}/h^{+} vertical mismatch after +FN hole injection, the devices still have excellent cycling endurance characteristics. However, 10K cycling degrades the T.O. quality and causes more charge loss through the T.O. during high-temperature baking. Moreover, nitride 70Å or thicker also captures most of the injected charges (< 6×10^{12}electron-cm^{-2}).

In chapter 7, we provided a detailed understanding of the erase mechanisms of SONOS-type devices for both channel- and gate-injection operations by using the GSCS method. Using this method, we could monitor the charge centroid (x) and charge density (Q) during erasing. According to these Q and x, we could further plot the J-E curves during erasing. The J-E curves of SoNOS, SONoS, BE-SONOS, and top BE-SONOS at different erase conditions overlap and are independent of EOT for the same tunnel barrier, and they can be well modeled by theoretical MFN hole injection equation. Therefore, the erase mechanism is external hole injection. On the other hand, for SONOS with B.O. $\geqq$ 54Å, the J-E curves are scattered for various erase conditions. Moreover, refill operation further reduces the erase speed. Therefore, the erase mechanism is electron de-trapping from nitride traps, and it is a function of e-field and trapping energy. Using this systematic method, hole tunneling or electron de-trapping can be easily discerned.

In addition to GSCS method, pulse-IV measurements have been successfully applied to study the transient charging behaviors of various SONOS-type devices in chapter 8. For SNS capacitor, since the electrons are trapped near the bottom portion of the nitride, and holes are trapped in the top portion of the nitride under +FN operation, the transient tunneling current decreases during the V_G pulse. Different transient behavior can be found in SONS capacitor, its transient tunneling current increases during the V_G pulse due to the hole trapping in the top portion of nitride. Moreover, the T.O. in SONOS can block the gate injection so that its transient tunneling current rises initially but then drops sharply and decreases to almost zero. By using theoretical model based on fully capture assumption, its transient tunneling current could be well modeled. On the other hand, we also used pulse-IV technique to investigate the fast charge-injection and relaxation of various SONS, SONoS, and SoNOS transistors. Since these transistors suffer from serious read disturb during V_T extraction by DC-IV measurement, our pulse-IV technique is needed to monitor the instant drain current after all kinds of reliability tests without disturb. We demonstrated that under lower voltage operations (±6V

1μs) the SONS can provide very high endurance characteristic (10^{10}cycles) for quasi-non-volatile memory applications. We also proved that the major retention mechanism of these transistors comes from direct tunneling leakage but not from thermionic emission of traps. Therefore, the nitride can provide very "deep" traps and promise for good non-volatile memory.

9.2 Suggestions for Future Works

Although the trapped charge behaviors of SONOS-type devices have been investigated exhaustively in this dissertation, there are still some topics which have not been clearly understood nor verified with strong evidence support. In the following, the topics will be pointed out, and they deserve to be further studied in the future.

1. In GSCS method, we compare two capacitors, one is channel-sensing capacitor which has a lightly doped channel and a heavily doped gate, and the other is gate-sensing capacitor which has a lightly doped gate and a heavily doped channel. Although our method still provides high accuracy when there is variation between these two capacitors, we need to prepare "two" capacitors for comparison. Therefore, the best way is to obtain two independent equations (ex. $\Delta V_{FB,CS}$ and $\Delta V_{FB,GS}$) from "single" capacitor. However, it needs to separate the signals of gate depletion and channel depletion from single CV curve. Thus, other simulation methods should be included to accurately distinguish the signals, but it may complicate the GSCS method.
2. The GS capacitor in GSCS method is operated by poly depletion, and the $\Delta V_{FB,GS}$ is extracted from the CV curves with parallel shifts. Compared with CS capacitor which has excellent interface between oxide/Si substrate and good bulk Si quality, the GS capacitor has poorer interface between T.O./poly gate and worse bulk poly quality. Therefore, the CV curve of GS capacitor will distort at high temperature, and $\Delta V_{FB,GS}$ cannot be extracted accurately at high temperature. Thus, the in-situ temperature related characteristics such as

temperature dependence electron de-trapping behavior cannot be investigated by GSCS method. Due to this reason, the poly gate process of GS capacitor should be further tuned to obtain perfect interface and bulk poly.

3. Using the GSCS method to investigate various SONOS-type capacitors, only the mean vertical location x and the amount of total trapped charges Q can be obtained. Although this method provides in-depth understanding of trapped charge behaviors, some other trapped charge parameters are still unknown such as trap energy, the detailed trapped charge distribution. Therefore, other methods should be developed to obtain the comprehensive understanding of trapped charge behaviors in SONOS-type devices.
4. GSCS method can be used to monitor the "real" time charge evolution and mean vertical location evolution, however, the detailed transport mechanisms during P/E and reliability tests are still unclear. More transport models should be included to further fit our extracted x and Q.
5. In this dissertation, we only employed GSCS method to investigate the "intrinsic" (without any parasitic effects) trapped charge behaviors of SONOS-type capacitors with large area (500μm×500μm). After understanding the "intrinsic" trapped charge behaviors, people would like to know the "real" (with parasitic effects) trapped charge behaviors of small transistors. In order to obtain that information but keep large enough capacitance, we could connect small transistors in series. However, the accuracy of GSCS method should be estimated again (parasitic effects should be taken into account).
6. In this dissertation, we only applied GSCS method to SONOS-type devices. In fact, this method also can be used to investigate other charge trapping materials such as high-*k* materials as long as different doping types can be formed.
7. Pulse-IV technique has been successfully demonstrated on the study of transient tunneling currents of various SONOS-type capacitors. Although the transient charge trapping behaviors of different structures could be well monitored, and the cause of transient

behaviors were also introduced, only the transient tunneling currents of SONOS with high capture rate nitride layer can be well modeled by theoretical model. For SONOS without T.O. or B.O., we did not propose corresponding transport models to fit the experimental data. Moreover, the charge relaxation time for both electron and hole should be extracted from the experimental data through some methodologies.

8. We also used pulse-IV technique to investigate the instant drain current of small transistors just after P/E and reliability tests. Pulse-IV technique could accurately monitor the drain current without read disturb which may be induced by DC-IV measurement. However, in this dissertation we only investigated the device characteristics under +/–FN operations. The device characteristics under different operations, for example CHE program and BBHH erase, should be explored in the future.

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APPENDIX

OUTLINE

A. Detailed Derivation of Equations (3-3) and (3-4)

If the charge vertical distribution function is Q(x), then the flat-band voltage shifts can be written as:

$$\Delta V_{FB,CS} = \int_0^{T_N} Q(x)\left(\frac{T_{Tox}}{\varepsilon_0\varepsilon_{ox}} + \frac{T_N - x}{\varepsilon_0\varepsilon_N}\right)dx \tag{A-1}$$

$$\Delta V_{FB,GS} = \int_0^{T_N} Q(x)\left(\frac{T_{Box}}{\varepsilon_0\varepsilon_{ox}} + \frac{x}{\varepsilon_0\varepsilon_N}\right)dx \tag{A-2}$$

Define the mean vertical location $\hat{x}$ and total charge Q_{total}:

$$Q_{total} = \int_0^{T_N} Q(x)dx \tag{A-3}$$

$$\hat{x} = \frac{1}{Q_{total}}\int_0^{T_N} Q(x)xdx \tag{A-4}$$

$$\Rightarrow \Delta V_{FB,CS} + \Delta V_{FB,GS} = \int_0^{T_N} Q(x)\left(\frac{T_{Tox} + T_{BOX}}{\varepsilon_0\varepsilon_{ox}} + \frac{T_N}{\varepsilon_0\varepsilon_N}\right)dx = Q_{total}\frac{EOT}{\varepsilon_0\varepsilon_{ox}} \tag{A-5}$$

$$\Rightarrow \Delta V_{FB,CS} = \int_0^{T_N} Q(x)\left(\frac{T_{Tox}}{\varepsilon_0\varepsilon_{ox}} + \frac{T_N - x}{\varepsilon_0\varepsilon_N}\right)dx = Q_{total}\left(\frac{T_{Tox}}{\varepsilon_0\varepsilon_{ox}} + \frac{T_N - \hat{x}}{\varepsilon_0\varepsilon_N}\right) \tag{A-6}$$

$$\Rightarrow \Delta V_{FB,GS} = \int_0^{T_N} Q(x)\left(\frac{T_{Box}}{\varepsilon_0\varepsilon_{ox}} + \frac{x}{\varepsilon_0\varepsilon_N}\right)dx = Q_{total}\left(\frac{T_{Box}}{\varepsilon_0\varepsilon_{ox}} + \frac{\hat{x}}{\varepsilon_0\varepsilon_N}\right) \tag{A-7}$$

For an arbitrary charge distribution, we can obtain the Q_{total} and $\hat{x}$ from Eqs. (A-6) and (A-7), and the results are the same as Eqs. (3-3) and (3-4).

B. Theoretical J vs. E_{Box} Calculation Method Using the $\Delta V_{FB,GS}$ of GS Capacitor

Case 1 (charges placed at the T.O./nitride interface):

$$J = \frac{dV_{FB,GS}}{dt}\frac{\varepsilon_0\varepsilon_{ox}}{T_{Box} + T_N\frac{\varepsilon_{ox}}{\varepsilon_N}} \tag{B-1}$$

$$E_{Box} = \frac{V_G + \Delta V_{FB,GS}}{EOT} - \frac{\Delta V_{FB,GS}}{T_{Box} + T_N \frac{\varepsilon_{ox}}{\varepsilon_N}} \quad \text{(B-2)}$$

Case 2 (charges placed at the B.O./nitride interface):

$$J = \frac{dV_{FB,GS}}{dt} \frac{\varepsilon_0 \varepsilon_{ox}}{T_{Box}} \quad \text{(B-3)}$$

$$E_{Box} = \frac{V_G + \Delta V_{FB,GS}}{EOT} - \frac{\Delta V_{FB,GS}}{T_{Box}} \quad \text{(B-4)}$$

Case 3 (charges placed at the center of nitride):

$$J = \frac{dV_{FB,GS}}{dt} \frac{\varepsilon_0 \varepsilon_{ox}}{T_{Box} + \frac{T_N}{2} \frac{\varepsilon_{ox}}{\varepsilon_N}} \quad \text{(B-5)}$$

$$E_{Box} = \frac{V_G + \Delta V_{FB,GS}}{EOT} - \frac{\Delta V_{FB,GS}}{T_{Box} + \frac{T_N}{2} \frac{\varepsilon_{ox}}{\varepsilon_N}} \quad \text{(B-6)}$$

C. Theoretical ΔV_{FB}-t for Different Charge Vertical Locations

The tunneling current through the B.O. follows the FN equation:

$$J = \alpha E_{Box}^2 \exp\left(\frac{-E_C}{E_{Box}}\right) \quad \text{(C-1)}$$

$$\alpha = \frac{q^3}{8\pi h \phi_B} \frac{m_0}{m_{ox}} \quad \text{(C-2)}$$

$$E_C = 4\sqrt{2m_{ox}} \frac{\phi_B^{3/2}}{3\hbar q} \quad \text{(C-3)}$$

q is the electron charge, ħ is the reduced Planck constant, ϕ_B is the barrier height of oxide for electron tunneling, m_0 is the mass of a free electron, and m_{ox} is the effective mass of an electron in the oxide.

(1) CS capacitor:

The E_{Box} can be written as:

$$E_{Box} = \frac{V_G - \Delta V_{FB,CS}}{EOT} \quad \text{(C-4)}$$

which is independent of charge vertical location, x. The $\Delta V_{FB,CS}$ can be derived by an iteration method if the J and charge vertical location x have been known:

$$\Delta V_{FB,CS}^{(i+1)} = \Delta V_{FB,CS}^{(i)} + \delta t \times J \times \left(\frac{\varepsilon_0 \varepsilon_{ox}}{T_{Tox} + (T_N - x)\frac{\varepsilon_{ox}}{\varepsilon_N}} \right)^{-1} \quad \text{(C-5)}$$

where δt is the time interval used in the iteration.

The $\Delta V_{FB,CS}$ for the charges placed at the T.O./nitride interface:

$$\Delta V_{FB,CS}^{(i+1)} = \Delta V_{FB,CS}^{(i)} + \delta t \times J \times \left(\frac{\varepsilon_0 \varepsilon_{ox}}{T_{Tox}} \right)^{-1} \quad \text{(C-6)}$$

The $\Delta V_{FB,CS}$ for the charges placed at the B.O./nitride interface:

$$\Delta V_{FB,CS}^{(i+1)} = \Delta V_{FB,CS}^{(i)} + \delta t \times J \times \left(\frac{\varepsilon_0 \varepsilon_{ox}}{T_{Tox} + T_N \frac{\varepsilon_{ox}}{\varepsilon_N}} \right)^{-1} \quad \text{(C-7)}$$

The $\Delta V_{FB,CS}$ for the charges placed at the center of nitride:

$$\Delta V_{FB,CS}^{(i+1)} = \Delta V_{FB,CS}^{(i)} + \delta t \times J \times \left(\frac{\varepsilon_0 \varepsilon_{ox}}{T_{Tox} + \frac{T_N}{2}\frac{\varepsilon_{ox}}{\varepsilon_N}} \right)^{-1} \quad \text{(C-8)}$$

(2) GS capacitor:

The E_{Box} in all cases are the same as that mentioned in Appendix B. The $\Delta V_{FB,GS}$ for the charges placed at the T.O./nitride interface:

$$\Delta V_{FB,GS}^{(i+1)} = \Delta V_{FB,GS}^{(i)} + \delta t \times J \times \left(\frac{\varepsilon_0 \varepsilon_{ox}}{T_{Box} + T_N \frac{\varepsilon_{ox}}{\varepsilon_N}} \right)^{-1} \quad \text{(C-9)}$$

The $\Delta V_{FB,GS}$ for the charges placed at the B.O./nitride interface:

$$\Delta V_{FB,GS}^{(i+1)} = \Delta V_{FB,GS}^{(i)} + \delta t \times J \times \left(\frac{\varepsilon_0 \varepsilon_{ox}}{T_{Box}} \right)^{-1} \quad \text{(C-10)}$$

The $\Delta V_{FB,GS}$ for the charges placed at the center of nitride:

$$\Delta V_{FB,GS}^{(i+1)} = \Delta V_{FB,GS}^{(i)} + \delta t \times J \times \left(\frac{\varepsilon_0 \varepsilon_{ox}}{T_{Box} + \frac{T_N}{2}\frac{\varepsilon_{ox}}{\varepsilon_N}} \right)^{-1} \quad \text{(C-11)}$$

Figure 3.7 is calculated by assuming $m_{ox}=0.45m_0$ and $\phi_B=3.1eV$.

D. Theoretical ΔV_{FB}-t Considering the Charge Injection Trajectory (x-Q plot)

The tunneling current through the B.O. follows the FN equation C-1. At time zero, we assume the ΔV_{FB} and charge vertical location (x) are zero, and they will increase as the time increases. During +FN programming, the Q and x always follow the relationship:

$$x^{(i+1)} = A\tanh(\frac{Q^{(i)}}{L}) \quad \text{(D-1)}$$

where A and L are fitting parameters. This relationship is obtained from fitting the experimental x-Q plot, as show in Fig. D-1 (A = 42 and L = 2.944×10^{12}).

(1) CS capacitor:

The B.O. e-field is the same as Eq. C-4. The $\Delta V_{FB,CS}$ can be derived by an iteration method:

$$\Delta V_{FB,CS}^{(i+1)} = \Delta V_{FB,CS}^{(i)} + \delta t \times J \times \left(\frac{\varepsilon_0 \varepsilon_{ox}}{T_{Tox} + (T_N - x^{(i)})\frac{\varepsilon_{ox}}{\varepsilon_N}} \right)^{-1} \quad \text{(D-2)}$$

The total injected charges:

$$Q^{(i+1)} = \frac{\varepsilon_0 \varepsilon_{ox}}{T_{Tox} + (T_N - x^{(i)})\frac{\varepsilon_{ox}}{\varepsilon_N}} \cdot \Delta V_{FB,CS}^{(i+1)} \quad \text{(D-3)}$$

(2) GS capacitor:

The B.O. e-field is:

$$E_{Box} = \frac{V_G + \Delta V_{FB,GS}}{EOT} - \frac{\Delta V_{FB,GS}}{T_{Box} + x\frac{\varepsilon_{ox}}{\varepsilon_N}} \quad \text{(D-4)}$$

The $\Delta V_{FB,GS}$ can be derived by an iteration method:

$$\Delta V_{FB,GS}^{(i+1)} = \Delta V_{FB,GS}^{(i)} + \delta t \times J \times \left(\frac{\varepsilon_0 \varepsilon_{ox}}{T_{Box} + x^{(i)} \frac{\varepsilon_{ox}}{\varepsilon_N}} \right)^{-1} \quad \text{(D-5)}$$

The total injected charges:

$$Q^{(i+1)} = \frac{\varepsilon_0 \varepsilon_{ox}}{T_{Box} + x^{(i)} \frac{\varepsilon_{ox}}{\varepsilon_N}} \cdot \Delta V_{FB,GS}^{(i+1)} \quad \text{(D-6)}$$

Fig. 3.9 is calculated by assuming $m_{ox}=0.485m_0$ and $\phi_B=3.1eV$.

E. Detailed Derivation of Hole Charge Density and Mean Vertical Location

We assume the flat-band voltage shift during –FN erasing only comes from the hole injection while the electrons are fixed. Therefore, we can define the hole flat-band voltage shifts by:

$$\Delta V_{FBh,CS}(t) = V_{FB,CS}(t) - V_{FB,CS}(as-programmed) \quad \text{(E-1)}$$

$$\Delta V_{FBh,GS}(t) = V_{FB,GS}(t) - V_{FB,GS}(as-programmed) \quad \text{(E-2)}$$

Similar to Eqs. (3-1) and (3-2), the hole flat-band voltage shifts are given by:

$$\Delta V_{FBh,CS} = Q_h \left(\frac{T_{Tox}}{\varepsilon_0 \varepsilon_{ox}} + \frac{T_N - x_h}{\varepsilon_0 \varepsilon_N} \right) \quad \text{(E-3)}$$

$$\Delta V_{FBh,GS} = Q_h \left(\frac{T_{Box}}{\varepsilon_0 \varepsilon_{ox}} + \frac{x_h}{\varepsilon_0 \varepsilon_N} \right) \quad \text{(E-4)}$$

where the x_h is the hole mean vertical location. From Eqs. (E-3) and (E-4), we can obtain the Q_h and x_h, as shown below:

$$Q_h = \varepsilon_0 \varepsilon_{ox} \frac{\Delta V_{FBh,CS} + \Delta V_{FBh,GS}}{EOT} \quad \text{(E-5)}$$

$$x_h = \frac{\Delta V_{FBh,GS}(T_{Tox}\varepsilon_N + T_N \varepsilon_{ox}) - \Delta V_{FBh,CS} T_{Box} \varepsilon_N}{\varepsilon_{ox}(\Delta V_{FBh,CS} + \Delta V_{FBh,GS})} \quad \text{(E-6)}$$

Equations (E-5) and (E-6) are also valid even for an arbitrary hole distribution, and the

detailed derivation is similar to Appendix A.

F. Theoretical MFN Hole Tunneling Equation

Holes tunnel through the oxide potential barrier and part of the nitride potential barrier, and the MFN equation can be written as:

$$J = \alpha E_{ox}^2 \exp(-\frac{E_c}{E_{ox}}) \tag{F-1}$$

E_{ox} is the tunnel oxide electric field, and

$$\alpha = \frac{m}{m_s} \frac{q^3}{16\pi\hbar(\phi_b^{1/2} - \phi^{1/2} + \gamma\sqrt{m_N / m_s}(\phi - \phi_2)^{1/2})^2} \tag{F-2}$$

$$E_c = \frac{4\sqrt{2m_s}(\phi_b^{3/2} - \phi^{3/2}) + 4\gamma\sqrt{2m_N}(\phi - \phi_2)^{3/2}}{3\hbar q} \tag{F-3}$$

$$\phi = \phi_b - qE_{ox}T_{Box} \tag{F-4}$$

m is the mass of a free hole, m_s is the effective mass of a hole in the oxide, m_N is the effective mass of a hole in the nitride, q is the electron charge, ħ is the reduced Planck constant, ϕ_b is the barrier height of oxide for hole tunneling, ϕ_2 is the energy difference between the oxide conduction band edge and the nitride conduction band edge and is referred to as the nitride barrier height, γ is ratio of the oxide and nitride dielectric constants $\gamma = \varepsilon_N/\varepsilon_{ox}$, and T_{Box} is the thickness of the B.O.

The fitting parameters of the samples with hole tunneling erase are shown in Table F-1.

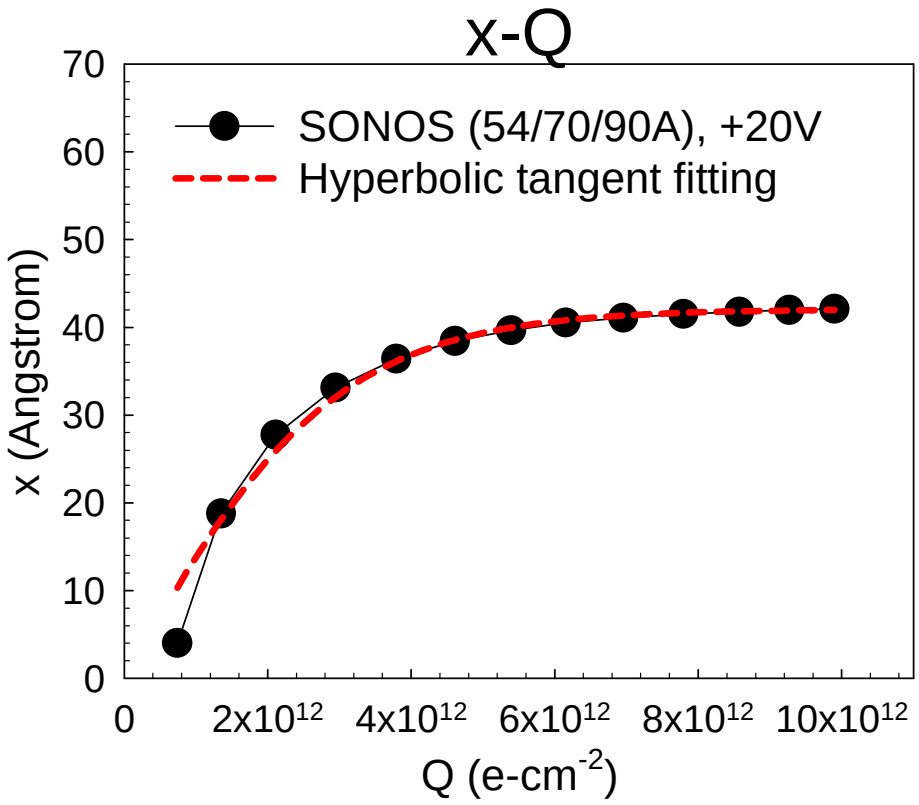

Fig. D.1 Curve fitting of the experimental x-Q plot (Fig. 3.5). Hyperbolic function is used to fit the experimental data. This fitting x-Q curve is used to theoretically calculate V_{FB}-t for both CS and GS capacitors.

Parameters / Samples	ϕ_b (eV)	ϕ_2 (eV)	m_s (m_0)	m_N (m_0)
SoNOS (20/70/90)	4.88	2.1	0.48	0.025
SONoS (54/80/25)	4.33	1.7	0.48	0.025
BE-SONOS	4.98	1.7	0.58	0.05
Top BE-SONOS (54/70/25/20/15)	4.95	1.85	0.5	0.08
Top BE-SONOS (54/70/20/20/15)	4.8	1.7	0.48	0.15
SONOS (26/70/90)	4.88	2.1	0.48	0.025

Table F.1 MFN fitting parameters of SoNOS, SONoS, BE-SONOS, top BE-SONOS, and SONOS.

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Journal Paper:

1. ［3點, 長文］P. Y. Du, H. T. Lue, S. Y. Wang, E. K. Lai, T. Y. Huang, K. Y. Hsieh, R. Liu, and C. Y. Lu, "Study of gate-sensing and channel-sensing transient analysis method for monitoring the charge vertical location of SONOS-type devices," *IEEE Transactions on Device and Materials Reliability (T-DMR)*, pp. 407-419, 2007.
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Chapter 6, Solid-State Electronics Research Advances, invited by Nova Publishers.

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