國立交通大學

電子工程學系 電子研究所

博士論文

射頻電路與高速輸入輸出界面電路之靜電放電防護設計

ON-CHIP ESD PROTECTION DESIGNS FOR RADIO-FREQUENCY INTEGRATED CIRCUITS AND HIGH-SPEED I/O INTERFACE CIRCUITS

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中華民國九十七年九月

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摘要

隨著近年來通訊技術與積體電路製程的持續演進，無線與有線通訊裝置已經成為生活中不可或缺的重要設備。藉由無線通訊傳輸資料，使用者可更機動地收發各種訊息，此演進大幅提昇了資料傳輸的方便性。有線傳輸技術的發展，加速無線接取點與伺服器間的資料傳輸速度。積體電路製程技術的發展，降低了無線與有線通訊裝置的製造成本，更激起使用者對通訊裝置的需求與使用意願。

所有電子產品，包含積體電路產品，必須於量產時符合可靠度的規範，以便讓使用者用得安心，並提供該產品足夠的耐用年限。靜電放電(Electrostatic Discharge, ESD)是積體電路可靠度中最重要的一環，大多數電子產品的故障與損壞均與遭受靜電放電轟擊有關。為對積體電路提供有效的靜電放電防護，所有積體電路與外界接觸的銲墊(Pad)皆須搭配靜電放電防護設計，包含電源銲墊與輸入輸出銲墊，而輸入輸出銲墊上的靜電放電防護電路會在訊號路徑上產生寄生效應。無線通訊裝置中的射頻(Radio- Frequency, RF)前端電路，亦需要搭配靜電放電防護設計，因為他們連接射頻收發機與外接之濾波器或天線。由於射頻電路的工作頻段高達數 GHz 至數十 GHz，如此高頻的工作頻率對於訊號路徑上的寄生效應有極嚴格的限制，若訊號路徑上的寄生效應過大，將導致射頻電路性能的嚴重衰減。除了無線通訊之前端電路，有線傳輸系統中的前端電路，近年來也在新型傳輸標準中提昇其傳輸速率，故有線傳輸系統中的輸入輸出界面電路對訊號路徑上的寄生效應要求也日趨嚴格。以上情況引發射頻電路與高速輸入輸出界面電路之靜

電放電防護設計的挑戰：如何在最低程度性能衰減的前提下達成最高的靜電放電耐受度，亦即如何將靜電放電防護元件的寄生效應最小化。

除此之外，互補式金氧半製程的演進，更進一步提昇靜電放電防護設計的困難度。對核心電路性能而言，使用先進的積體電路製程，電晶體的工作頻率可以提昇，並可降低元件的雜訊、功率損耗。隨著積體電路製程的進步，電晶體的元件尺寸可以大幅微縮，故可整合更多電路功能於單一晶片內，此舉開啟了系統單晶片(System on Chip, SoC)的應用。然而靜電放電轟擊的強度並未隨著積體電路元件微縮而降低，隨著積體電路製程的演進，電晶體閘極氧化層的崩潰電壓逐漸降低，使電晶體愈容易遭受靜電放電轟擊而損壞，因此另一個挑戰隨之產生：如何在先進製程中降低靜電放電轟擊時於靜電放電防護元件上產生的跨壓，以有效保護內部電路。上述兩個挑戰為本論文的研究動機，本論文由積體電路周圍的銲墊設計開始，循序漸進至積體電路內部的全晶片靜電放電防護設計與射頻前端電路設計；由單一晶片的電路設計，延伸至整個電子系統的電路板層級元件充電模式(Board-Level Charged Device Model)靜電放電防護探討。本論文的研究方向包括：(1)分析目前已發表的射頻電路與高速輸入輸出界面電路之靜電放電防護設計相關文獻、(2)超低寄生電容的銲墊設計、(3)寬頻分散式放大器之靜電放電防護設計、(4)搭配全晶片靜電放電防護設計之差動式低雜訊放大器(Low-Noise Amplifier, LNA)、(5)高速輸入輸出界面電路之靜電放電防護設計、(6)電路板層級元件充電模式靜電放電(Board-Level Charged-Device-Model ESD)對積體電路產品之影響。

本論文第二章針對目前已發表的射頻電路與高速輸入輸出界面電路之靜電放電防護設計進行分析，將各種設計分門別類，並歸納各種設計的優缺點與成效。本章首先以量測結果說明靜電放電防護元件的寄生效應，並闡述靜電放電防護元件對電路性能造成之負面影響。除寄生效應外，靜電放電防護元件於積體電路遭受靜電放電轟擊時的元件特性亦相當重要，因為這關係該積體電路的靜電放電耐受度。本章將目前已發表的射頻電路與高速輸入輸出界面電路之靜電放電防護設計分為三種方式，第一種為使用電路技巧降低靜電放電防護元件寄生效應的設計方式，使用電路技巧，可將靜電放電防護元件的寄生效應透過阻抗匹配或阻抗隔絕的方式大幅降低，但額外的元件可能提高晶片面積或製作成本。第二種方式藉由改變元件佈局以降低靜電放電防護元件的寄生效應，雖然寄生效應的改善幅度較使用電路技巧的方式小，但由於不需外加元件，故晶片面積與製作成本亦小於使用電路技巧的方式。第三種方式藉由改變製程降低靜電放電防護元件的寄生效應，改變半導體的摻雜濃度，可改變接面的寄生電容值，此法雖可以最直觀的方

式降低靜電放電防護元件的寄生效應，但改變製程的可能性在一般應用中並不常見。本章後段比較各種設計的複雜度、改善後之寄生效應、靜電放電耐受度、與面積使用效率。

除了靜電放電防護元件以外，銲墊也會在訊號路徑上對射頻訊號造成負面影響，為了提昇射頻電路之性能，銲墊的寄生電容值也必須盡量降低。本論文第三章提出一種新型具有超低電容值的銲墊架構，可於一般互補式金氧半製程中實現，不需修改製程。在此新型銲墊架構中藉由使用電感，可抵銷銲墊本身的寄生電容值，以大幅降低整個銲墊的等效寄生電容值。本研究於 130 奈米互補式金氧半製程中實現三種新型設計，分別在傳統銲墊的區域中，以一層、三層、五層金屬實現三種電感，故此新型設計不需增加銲墊面積。藉由不同電感值，可產生不同共振頻率，也可達成不同程度的銲墊電容改善量。實驗結果顯示，藉由銲墊下方電感產生的共振效應，等效銲墊電容可於特定頻段內大幅降低。以五層金屬實現電感的銲墊架構，在 4.3 GHz 至 4.8 GHz 的頻段內，等效銲墊電容值可降低至接近 0 fF。利用此新型銲墊架構，將可降低因傳統銲墊電容造成的訊號延遲與訊號損耗，進而提昇射頻電路性能。

本論文第四章提出新型分散式靜電放電防護架構，並將其應用於寬頻分散式放大器，且以 0.25 微米互補式金氧半製程實現。當所有靜電放電防護元件的總電容為 300 fF 時，搭配傳統等尺寸式分散式靜電放電防護架構的分散式放大器，其人體放電模式(Human Body Model, HBM)與機械放電模式(Machine Model, MM)靜電放電耐受度分別為 5.5 kV 與 325 V，且於 1 GHz 至 10 GHz 的頻段內擁有 4.7 ± 1 dB 的增益；搭配新型遞減尺寸式分散式靜電放電防護架構的分散式放大器，人體放電模式與機械放電模式靜電放電耐受度可大幅提昇至 8 kV 與 575 V，且於 1 GHz 至 9.2 GHz 的頻段內擁有 4.9 ± 1.1 dB 的增益。這兩種分散式靜電放電防護架構均可與分散式放大器共同設計，以達成符合要求的射頻性能與靜電放電耐受度。

除了搭配靜電放電防護設計的寬頻射頻前端電路外，本論文第五章提出窄頻射頻前端電路與靜電放電防護電路的共同設計。本章使用 130 奈米互補式金氧半製程設計一個工作於 5 GHz 的差動式低雜訊放大器，並將數種新型靜電放電防護架構應用至該差動式低雜訊放大器。本研究為目前相關研究中，率先探討差動式低雜訊放大器接點對接點(Pin to Pin)靜電放電耐受度的研究。所有差動式低雜訊放大器的功率消耗皆為 10.3 mW。沒有搭配靜電放電防護設計的差動式低雜訊放大器，在 5 GHz 的功率增益與雜訊指數分別為 16.2 dB 與 2.16 dB。本章亦實現傳統雙二極體(Double Diode)靜電放電防護架構的差動式低雜訊放大器，此設計於各輸入銲墊至電源線與接地線間分別放置靜電放

電防護二極體，其人體放電模式與機械放電模式靜電放電耐受度分別為 2.5 kV 與 200 V，在 5 GHz 的功率增益與雜訊指數分別為 17.9 dB 與 2.43 dB。第一個新提出的靜電放電防護設計使用雙矽控整流器(Silicon-Controlled Rectifier, SCR)，此設計於各輸入銲墊至電源線與接地線間分別放置矽控整流器提供靜電放電防護功能，其人體放電模式與機械放電模式靜電放電耐受度分別為 6.5 kV 與 500 V，搭配此設計的差動式低雜訊放大器在 5 GHz 的功率增益與雜訊指數分別為 17.9 dB 與 2.54 dB。第二個新提出的靜電放電防護設計於兩個差動輸入銲墊間插入靜電放電匯流排(ESD Bus)，藉此於兩個差動輸入銲墊間提供有效的靜電放電路徑，其人體放電模式與機械放電模式靜電放電耐受度分別為 3 kV 與 100 V，搭配此設計的差動式低雜訊放大器在 5 GHz 的功率增益與雜訊指數分別為 18 dB 與 2.62 dB。第三個新提出的靜電放電防護設計於兩個差動輸入銲墊間使用交叉耦合(Cross Couple)的矽控整流器，除了可提供單一輸入銲墊至電源線與接地線的靜電放電防護外，更可在不增加元件的情況下，額外提供兩個差動輸入銲墊間的接點對接點模式靜電放電防護功能，其此設計的人體放電模式與機械放電模式靜電放電耐受度分別為 1.5 kV 與 150 V，搭配此設計的差動式低雜訊放大器在 5 GHz 的功率增益與雜訊指數分別為 19.2 dB 與 3.21 dB。另一個靜電放電防護設計搭配雙二極體與交叉耦合矽控整流器，可達成 4 kV 人體放電模式與 300 V 機械放電模式的靜電放電耐受度，搭配此設計的差動式低雜訊放大器在 5 GHz 的功率增益與雜訊指數分別為 19.1 dB 與 3.05 dB。除了比較靜電放電耐受度外，搭配各種靜電放電防護設計的差動式低雜訊放大器之射頻性能，亦於第五章內比較與討論。

本論文第六章提出高速輸入輸出界面電路之靜電放電防護設計。首先量測在 130 奈米互補式金氧半製程中 P 型擴散區與 N 井接面(P+/N-well)及 N 型擴散區與 P 井接面(N+/P-well)兩種二極體在不同尺寸下的靜電放電耐受度與寄生電容值。為了確保能提供一般商用規範的 2 kV 人體放電模式靜電放電耐受度，靜電放電防護二極體需使用 40 微米以上的周長實現。接著利用仿製接收級電晶體(Dummy Receiver NMOS)架構，將電晶體的閘極連接至輸入銲墊，並將電晶體的汲極、源極、基底接地，搭配選定之靜電放電防護二極體尺寸與電源箝制靜電放電防護電路，可量測此仿製接收級電晶體的靜電放電耐受度。由於仿製接收級電晶體的連接方式近似於一般接收級內電晶體的連接方式，故可由仿製電晶體的靜電放電耐受度推估一般接收級的靜電放電耐受度。此靜電放電防護設計亦應用至 2.5 GHz 的高速接收級界面電路，在 250 fF 寄生電容的限制下，此靜電放電防護設計可達成 3 kV 的人體放電模式靜電放電耐受度。此外本論文第六章提出一種

新型設計，將原本置於輸入銲墊與接地線間的 N 型擴散區與 P 井接面(N+/P-well)二極體置換為矽控整流器，藉由與電源箝制靜電放電防護電路共用靜電放電偵測電路，輸入輸出接點的寄生電容可有效降低，並可藉由使用矽控整流器提昇靜電放電耐受度。本研究將靜電放電防護元件與部分靜電放電偵測電路置於輸入銲墊下方，可節省晶片面積，並降低訊號路徑上的寄生電容值。

完成單一積體電路晶片的靜電放電防護設計後，每個晶片皆須安裝至電子產品的模組內並進行功能測試，此時可能引發電路板層級元件充電模式靜電放電，導致晶片損毀。本論文第七章探討電路板層級元件充電模式靜電放電對積體電路產品造成的威脅，首先簡介晶片層級與電路板層級元件充電模式靜電放電的成因，並說明數個積體電路晶片遭受電路板層級元件充電模式靜電放電損壞的實例。由於電路板層級元件充電模式靜電放電的電流峰值與電子模組中的電路板尺寸有密切關係，第七章第二部分量測不同電路板尺寸所產生的電路板層級元件充電模式靜電放電電流波形，實驗結果顯示較大的電路板尺寸或將電路板充電至較高電壓，將導致較大的電路板層級元件充電模式靜電放電電流峰值，為了降低此電流峰值，以免損壞模組內的積體電路晶片，在放電路徑上可放置串聯電阻，實驗結果顯示此舉可大幅降低電路板層級元件充電模式靜電放電的電流峰值。第七章亦對數個以互補式金氧半製程製作的測試元件與測試電路進行晶片層級與電路板層級元件充電模式靜電放電測試，測試結果發現電路板層級元件充電模式靜電放電耐受度較低，且造成較嚴重的損壞情形，故電路板層級元件充電模式靜電放電對積體電路晶片的威脅比晶片層級元件充電模式靜電放電更為嚴重。

第八章總結本論文的研究成果，並提出數個接續本論文研究方向的研究題目。由於目前對電路板層級的靜電放電測試方式尚未有明確規範，本論文於附錄提出「積體電路之電路板層級元件充電模式靜電放電測試標準」提案，提案中詳細定義電路板層級靜電放電測試的各項測試條件與量測方式。

本論文所提出的各項新型設計，均搭配實驗晶片量測結果以驗證設計之理論，且有相對應的國際期刊與國際研討會論文發表。本論文中數個創新設計已提出專利申請。

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Abstract

With the continuous evolution of communication technology and integrated circuit (IC) process, wireless and wireline communication devices had become essential in daily life. By using the wireless communication devices to transmit data, users can access any information more conveniently. Advance wireline communication technology speedups the data transmission rate between the access points (AP) and the server. The continuous scaling of IC process technology further stimulates the demand for communication devices.

All microelectronic products, including IC products, must meet the reliability specifications during mass production in order to be safely used and provide moderate life time. Electrostatic discharge (ESD), which has become one of the most important reliability issues in IC products, must be taken into consideration during the design phase of all IC products. Most of the failures and damages found in ICs were demonstrated to be related to ESD. To provide effective ESD protection for the IC, all pads which connect the IC and the external world need to be equipped with ESD protection circuits, including the input/output (I/O) pads, VDD pads, and VSS pads. However, the ESD protection devices at the I/O pads inevitably cause parasitic effects on the signal path. The radio-frequency (RF) front-end circuits in wireless communication devices need ESD protection design as well because they connect the RF transceiver to the external antenna or band-select filter. Since the RF

front-end circuits operate in the frequency band ranging from several gigahertzes to tens of gigahertz, such a high operating frequency leads to strict limitations for the parasitic effects on the signal path. If the parasitic effects on the signal path are too large, RF circuit performance will be seriously degraded. Besides RF front-end circuits, the data rates of recent wireline communication standards also increase, so the parasitic effects on the signal paths of high-speed I/O interface circuits in wireline communication systems also need to be watched. The situation introduces the challenge in ESD protection design for RF circuits and high-speed I/O interface circuits, which is to achieve the highest ESD robustness with the smallest performance degradation. In other words, the parasitic effects of the ESD protection devices need to be minimized.

Furthermore, the evolution of CMOS process increases the difficulty of ESD protection design. Advanced CMOS technologies not only increase the operating frequency of transistors but also reduce the noise of active devices and power consumption. With the continuous scaling of CMOS technology, the dimensions of CMOS devices are reduced, so more function blocks can be integrated into a single chip. This is the application of system on chip (SoC). However, ESD was not scaled down with the CMOS technology. MOS transistors fabricated in advanced CMOS processes have thinner gate oxide and thus lower gate-oxide breakdown voltage, so they are more vulnerable to ESD. Here comes the other design challenge, which is to reduce the voltage across the ESD protection devices under ESD stresses in advanced CMOS processes. The two aforementioned design challenges form the motivation of this dissertation. This dissertation begins at the design in the periphery of the IC, which is the bond pad, and enters the co-design of RF front-end and ESD protection circuits. Besides, this dissertation covers the whole-chip ESD protection design within a single chip and the investigation of board-level charged-device-model (CDM) ESD issue in IC products. The research topics including: (1) overview of previous works on ESD protection design for RF and high-speed I/O interface circuits, (2) ultra low-capacitance bond pad design, (3) ESD protection design for wideband distributed amplifier, (4) differential low-noise amplifier (LNA) with whole-chip ESD protection design, (5) ESD protection design for high-speed I/O interface circuits, and (6) investigation on board-level CDM ESD issue in IC products.

In chapter 2, the published ESD protection designs for RF front-end circuits and high-speed interface circuits are overviewed. The designs are categorized with their individual advantages and disadvantages clearly analyzed. The RF performance degradation caused by ESD protection devices are illustrated with measured results. Besides, the characteristics of ESD protection devices under ESD stress conditions are quite important, because it determines the ESD robustness. The designs are categorized into three groups, which are the circuit solution, layout solution, and process solution. With the circuit technique, the impacts of parasitic effects caused by ESD protection devices on circuit performance can be significantly mitigated by impedance matching or impedance isolation. However, the increased chip area due to the extra components increases the fabrication cost. With the layout modification, the parasitic effects and dimensions of ESD protection devices can be moderately reduced. Since no extra component is used, the fabrication cost is lower than that with circuit technique. The third group is process modification. By modifying the doping concentration, the junction capacitance can be adjusted to reduce the parasitic effects of ESD protection devices. However, process modification is uncommon in general IC products. The design complexity, improved parasitic effect, ESD robustness, and area efficiency of all reported designs are compared in this chapter.

Besides ESD protection devices, bond pads also cause impacts on circuit performance because of their parasitic capacitance. To mitigate the performance degradation, bond-pad capacitance needs to be minimized as well. A new low-capacitance bond pad structure in CMOS technology for RF applications is proposed in chapter 3. Three kinds of inductors stacked under the pad are used in the proposed bond pad structure. Experimental results in a 130-nm CMOS process have verified that the bond-pad capacitance is reduced due to the cancellation effect provided by the inductor embedded in the proposed bond pad structure. The bond-pad capacitance is reduced to almost 0 fF from 4.3 to 4.8 GHz. The proposed bond pad structure is fully compatible to general CMOS processes without any extra process modification.

In chapter 4, two distributed ESD protection schemes are proposed and applied to protect distributed amplifiers against ESD stresses. Fabricated in a 0.25-μm CMOS process, the distributed amplifier with the first protection scheme of the equal-sized distributed ESD (ES-DESD) protection scheme, contributing an extra 300 fF parasitic capacitance to the circuit, can sustain the human-body model (HBM) ESD level of 5.5 kV and machine-model (MM) ESD level of 325 V, while exhibits the flat-gain of 4.7 ± 1 dB from1 to 10 GHz. With the same total parasitic capacitance, the distributed amplifier with the second protection scheme of the decreasing-sized distributed ESD (DS-DESD) protection scheme achieves better ESD robustness, where the HBM ESD level is over 8 kV and MM ESD level is 575 V, and has the flat-gain of 4.9 ± 1.1 dB over the 1 to 9.2-GHz band. With these two proposed ESD protection schemes, the wideband RF performances and high ESD robustness of the distributed amplifier can be successfully co-designed to meet the application specifications.

Besides ESD protection design for wideband RF frond-end circuits, co-design of narrow band LNA and ESD protection circuit is proposed in chapter 5. A 5-GHz differential LNA is implemented in a 130-nm CMOS process, and several new ESD protection schemes are applied to this differential LNA. This is the first work which investigates the pin-to-pin ESD robustness of differential LNAs. All of the fabricated differential LNAs consume 10.3 mW from the 1.2-V power supply. The reference differential LNA without ESD protection has 16.2-dB power gain and 2.16-dB noise figure at 5 GHz. The conventional double-diode ESD protection scheme is realized for the differential LNA, which has 2.5-kV HBM and 200-V MM ESD robustness. The differential LNA with the double-diode ESD protection scheme has 17.9-dB power gain and 2.43-dB noise figure at 5 GHz. With the proposed double silicon-controlled rectifier (SCR) ESD protection scheme, the HBM and MM ESD levels are significantly improved to 6.5 kV and 500 V, respectively. Besides, the differential LNA with the double-SCR ESD protection has 17.9-dB power gain, and 2.54-dB noise figure at 5 GHz. Another proposed design uses an ESD bus between the differential input pads, which has 3-kV HBM and 100-V MM ESD robustness. The differential LNA with the proposed ESD bus has 18-dB power gain and 2.62-dB noise figure at 5 GHz. The ESD protection design using cross-coupled SCR devices between the differential input pads is also proposed. Besides providing ESD protection for a single input pad, pin-to-pin ESD protection is also achieved without adding any extra devices. This ESD protection scheme achieves 1.5-kV HBM and 150-V MM ESD levels, respectively. The power gain and noise figure of this differential LNA are 19.2 dB and 3.2 dB, respectively. By using other diodes beside the cross-coupled SCR devices, the turn-on efficiency of ESD protection devices can be enhanced. With the double diodes and the cross-coupled SCR devices, the ESD-protected differential LNA achieves 4-kV HBM and 300-V MM ESD robustness, and exhibits 19.1-dB power gain and 3-dB noise figure at 5 GHz.

Chapter 6 presents the ESD protection design for high-speed I/O interface circuits. The ESD levels and parasitic capacitances of P+/N-well and N+/P-well ESD protection diodes with different dimensions are characterized in the beginning. Then the double-diode ESD protection scheme is applied to the dummy receiver NMOS and the dummy transmitter NMOS. Since the connection of the dummy receiver NMOS (dummy transmitter NMOS) is similar to that of the NMOS transistor in a receiver (transmitter) interface circuit, the ESD robustness of the dummy receiver NMOS (dummy transmitter NMOS) can be used to predict the ESD robustness of the high-speed interface circuit with this ESD protection scheme. This whole-chip ESD protection scheme is also applied to a 2.5-Gb/s high-speed I/O interface circuit, and the ESD robustness is larger than 3 kV in HBM with the parasitic capacitance of less than 250 fF. Moreover, a new ESD protection scheme is proposed in chapter 6. By replacing the N+/P-well diode between the input pad and VSS with the SCR, the ESD robustness can be further improved. In the ESD protection schemes in chapter 6, the ESD protection devices and part of the ESD detection circuit is placed under the I/O pad to reduce the chip area and the parasitic capacitance on the signal path.

After finishing ESD protection design for a single chip, the chip needs to be installed in a module and module function test will be performed. At this time, board-level CDM ESD events may occur to damage the ICs. In chapter 7, the impacts caused by board-level CDM ESD events on IC products are investigated. The mechanism of board-level CDM ESD event is introduced first. Based on this mechanism, an experiment has been performed to investigate the board-level CDM ESD current waveforms under different sizes of printed circuit boards (PCBs), different charged voltages, and different series resistances in the discharging path. Experimental results have shown that the discharging current strongly depends on the PCB size, charged voltage, and series resistance. Moreover, chip-level and board-level CDM ESD levels of several test devices and test circuits fabricated in CMOS processes have been characterized and compared. Test results have shown that the board-level CDM ESD level of the test circuit is lower than the chip-level CDM ESD level, which demonstrates that the board-level CDM ESD event is more critical than the chip-level CDM ESD event. In addition, failure analysis reveals that the failure on the test circuit under the board-level CDM ESD test is much severer than that under the chip-level CDM ESD test.

Chapter concludes the achievement in this dissertation, and suggests several future works in this field. Since the standard for the board-level CDM ESD test is not established so far, the proposal of the “Test standard for board-level charged-device-model electrostatic discharge robustness of integrated circuits” (in Chinese) is presented in the appendix. In the proposal, the test methodology and test conditions are clearly defined.

In this dissertation, several novel designs have been proposed in the aforementioned research topics. Measured results of fabricated test chips have demonstrated the performance improvement. The achievements of this dissertation have been published in several international journal and conference papers. Several innovative designs have been applied for patents.

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蕭淵文
誌於竹塹交大
九十七年 夏

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Chapter 1

Introduction

In this chapter, the background and the organization of this dissertation are discussed. First, the considerations of electrostatic discharge (ESD) protection design for radio-frequency (RF) front-end circuits and high-speed (input/output) I/O interface circuits in complementary metal-oxide-semiconductor (CMOS) processes are discussed. Secondly, the board-level charged-device-model (CDM) ESD issue of CMOS integrated circuit (IC) products is introduced. Finally, the organization of this dissertation is described.

1.1. Background of ESD Protection Design for High-Frequency I/O Interfaces

With the advantages of high integration and low cost for mass production, high-frequency (input/output) I/O interfaces operating in gigahertz (GHz) frequency bands have been widely designed and fabricated in CMOS processes. Such high-frequency applications include RF front-end circuit in wireless communications and high-speed I/O interface circuits in wireline communications. Electrostatic discharge (ESD), which has become one of the most important reliability issues in integrated circuit (IC) products, must be taken into consideration during the design phase of all ICs [1]–[4], including the radio-frequency (RF) front-end circuits and high-speed I/O interface circuits. Without ESD protection circuits at all I/O pads, the RF performance of a wireless transceiver can be easily damaged by ESD stresses, because RF front-end circuits are always fabricated in advanced CMOS processes. Usually the I/O pads are connected to the gate terminal of MOS transistor or silicided drain/source terminal, which leads to a very low ESD robustness if no ESD protection design is applied to the I/O pad. Once the RF front-end circuit is damaged by ESD, it can not be recovered and the RF functionality is lost. Besides ESD caused threats to RF front-end circuits, the effects of ESD-induced damage in the high-speed I/O interface circuits had also been studied. It had been demonstrated that the termination resistance of high-speed I/O interface circuits is changed after ESD stresses. The impedance mismatch after ESD stresses causes significant waveform distortion on the I/O signals, which seriously degrades the performance of high-speed I/O interface circuits [5]. Therefore, on-chip ESD protection circuits must be provided for all I/O pads in ICs. Two common chip-level (or component-level) ESD test standards are human-body-model (HBM) and machine-model (MM) ESD test standards [6], [7]. HBM and MM ESD tests are used to evaluate the ESD robustness of the IC when it is touched by the charged human body or charged machine. The equivalent circuits of HBM and MM ESD tests are shown in Fig. 1.1(a) and (b), respectively. In order to protect the internal circuits against ESD stresses, ESD protection circuits must be provided at all I/O pads. The concept of whole-chip ESD protection design is illustrated in Fig. 1.2.

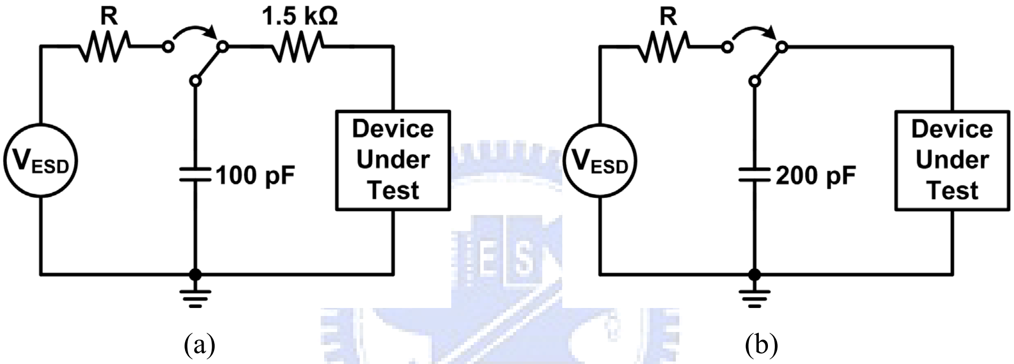


Fig. 1.1. Equivalent circuits of (a) HBM and (b) MM ESD tests.

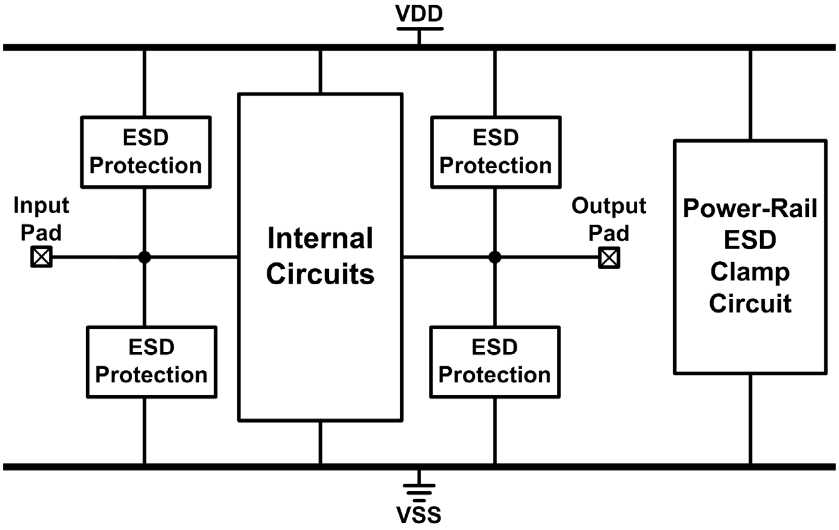
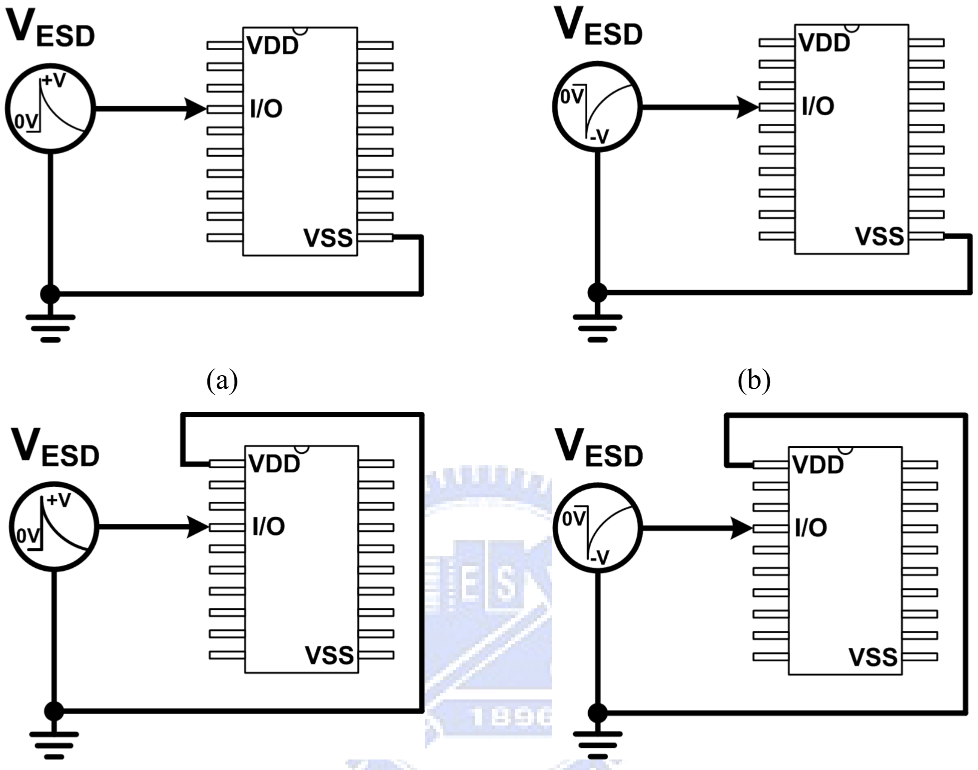


Fig. 1.2. Whole-chip ESD protection scheme for ICs.

The ESD-test pin combinations are shown in Fig. 1.3. ESD stresses may have positive or negative voltages on an I/O pin with respect to the grounded VDD or VSS pin. The typical

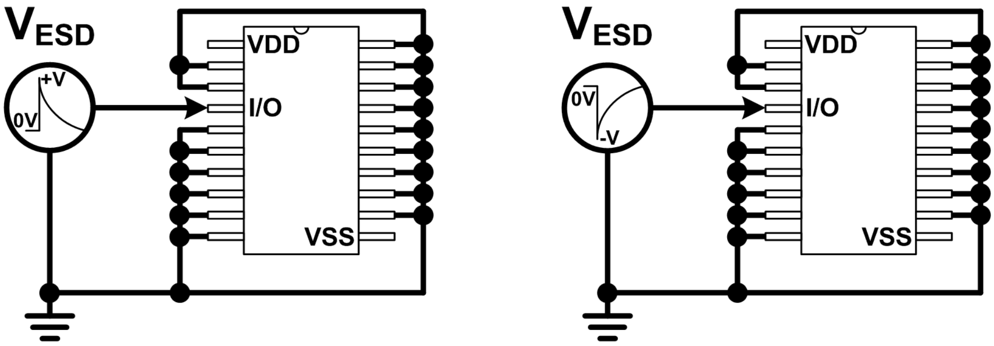
ESD specifications for commercial IC products in HBM and MM are 2 kV and 200 V, respectively. For comprehensive ESD verification, the pin-to-pin ESD stresses and VDD-to-VSS ESD stresses had also been specified to verify the whole-chip ESD robustness, which are shown in Fig. 1.4 and 1.5, respectively.



(a) (b)

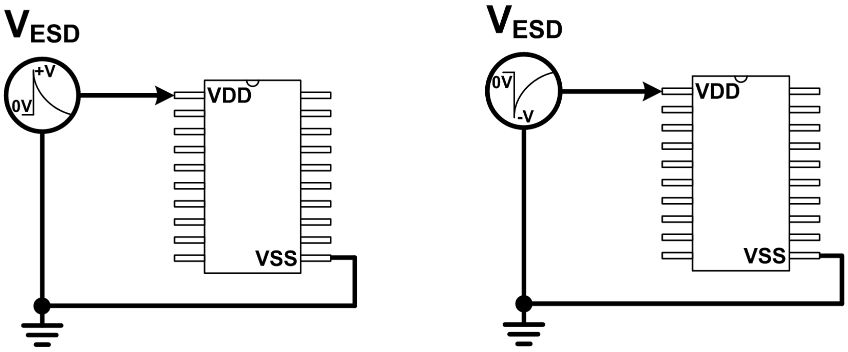
(c) (d)

Fig. 1.3. Four ESD-test pin combinations for the IC products: (a) positive-to-VSS mode (PS-mode), (b) negative-to-VSS mode (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode).



(a) (b)

Fig. 1.4. Pin combinations in pin-to-pin ESD tests: (a) positive mode, and (b) negative mode.



(a) (b)

Fig. 1.5. Pin combinations in VDD-to-VSS ESD tests: (a) positive mode, and (b) negative mode.

Fig. 1.6 shows the typical on-chip double-diode ESD protection scheme in which two ESD diodes at I/O pad are co-designed with the power-rail ESD clamp circuit to prevent internal circuits from ESD damage [8]. In Fig. 1.6, a P+/N-well diode (D_P) and an N+/P-well diode or an N-well/P-substrate diode (D_N) are placed at input pad or output pad. When the D_P and D_N are under forward-biased condition, they can provide discharge paths from I/O pad to VDD and from VSS to I/O pad, respectively.

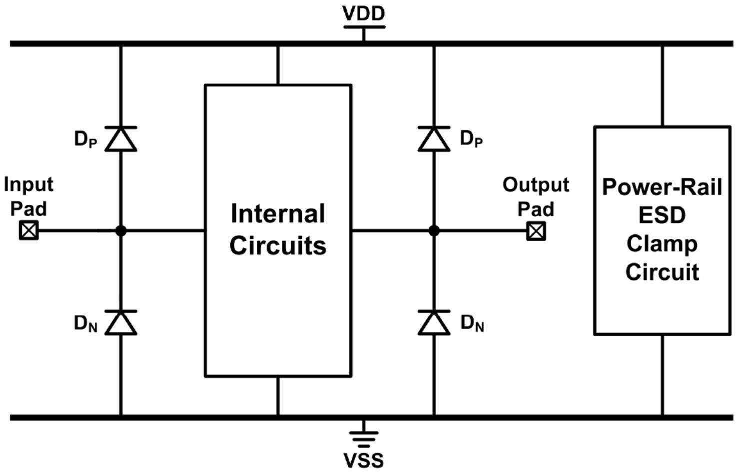
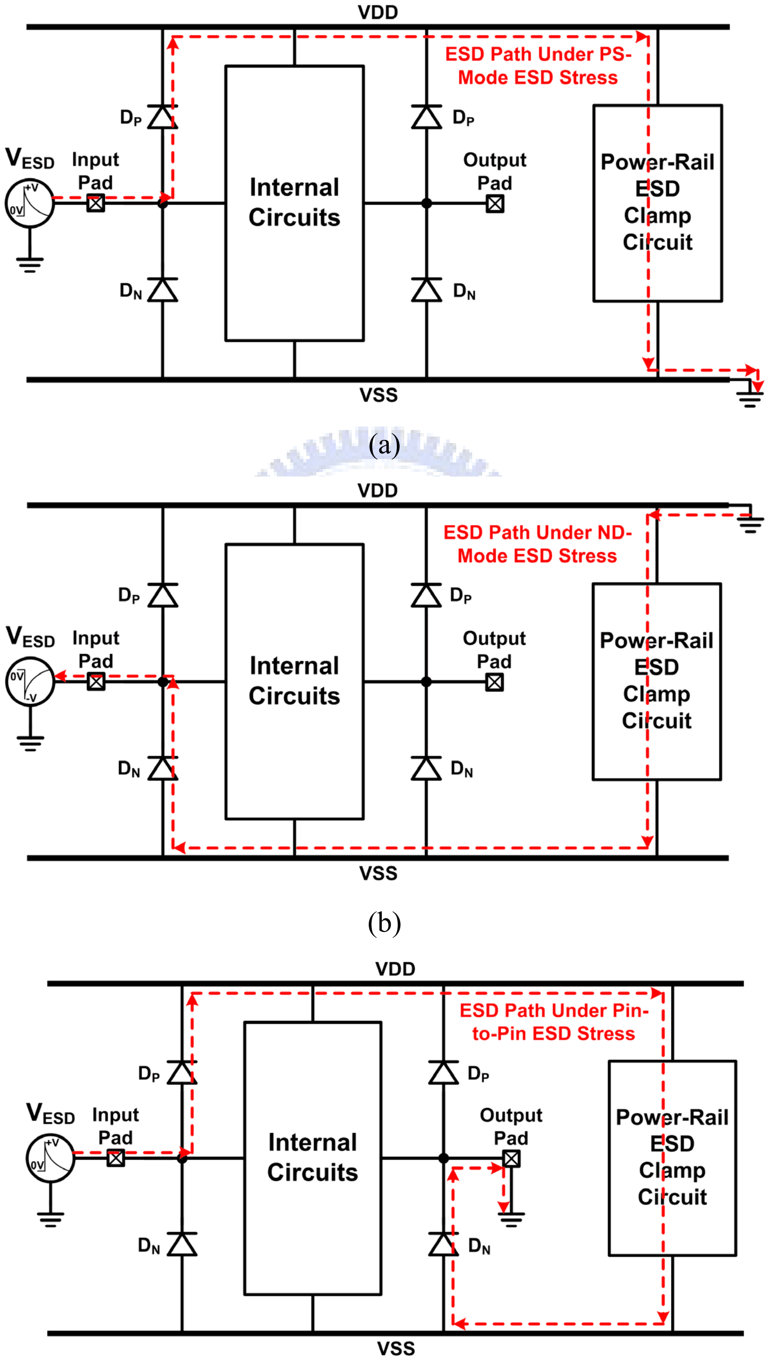


Fig. 1.6. Typical double-diode ESD protection scheme.

During the positive-to-VDD (PD) mode and negative-to-VSS (NS) mode ESD stresses, ESD current is discharged through the forward-biased D_P and D_N, respectively. To avoid the ESD diodes from being operated under breakdown condition during the positive-to-VSS (PS) mode and negative-to-VDD (ND) mode ESD stresses, which results in a substantially lower ESD robustness, the power-rail ESD clamp circuit is used between VDD and VSS to provide ESD current paths between the power rails [9]. Thus, ESD current is discharged from the I/O pad through the forward-biased D_P to VDD, and discharged to the grounded VSS pin through the turn-on efficient power-rail ESD clamp circuit during PS-mode ESD stresses, as shown in Fig. 1.7(a). Similarly, ESD current is discharged from the VDD pin through the turn-on efficient power-rail ESD clamp circuit and the forward-biased D_N to the I/O pad during ND-mode ESD stresses, as shown in Fig. 1.7(b).



(a)

(b)

(c)

Fig. 1.7. ESD current paths in the typical double-diode ESD protection scheme under (a) PS-mode ESD stresses, (b) ND-mode ESD stresses, and (c) pin-to-pin ESD stresses.

During pin-to-pin ESD stresses, ESD current flows from the zapped I/O pad through the forward-biased D_P, the power-rail ESD clamp circuit, and the forward-biased D_N to the grounded I/O pad, as shown in Fig. 1.7(c). Under VDD-to-VSS ESD tests, ESD current flows through the power-rail ESD clamp circuit between VDD and VSS. Since the power-rail ESD clamp circuit works independently between VDD and VSS, its parasitic effects do not have any impact on the internal circuits. With the turn-on efficient power-rail ESD clamp circuit, the ESD diodes can be assured to be operated in the forward-biased condition under all ESD test modes, which leads to higher ESD robustness.

1.1.1. Standards of Commercial Wireless and Wireline Communications

With the evolution of communication technologies, more and more applications become available. To successfully transmit the signals without interfering with other applications in the free space, every wireless communication standard is allocated with some specific frequency bands. Table 1.1 lists the allocated frequency bands of the wireless communication standards. The operating frequency bands ranges from less than 1 GHz to more than 10 GHz. The front-end circuits in the transmitters or receivers are operated at the specified frequency to handle the RF signal. The mixers perform the conversion between the RF signal and the

Table 1.1

Allocated Frequency Bands of the Wireless Communication Standards

Standard	**Frequency Band**
UMTS over W-CDMA	**850 MHz, 1.9, 1.9/2.1, and 1.7/2.1 GHz**
UMTS-TDD	**450, 850 MHz, 1.9, 2, 2.5, and 3.5 GHz**
CDMA2000	**450, 850, 900 MHz, 1.7, 1.8, 1.9, and 2.1 GHz**
EDGE/GPRS	**850, 900 MHz, 1.8, and 1.9 GHz**
WiMAX (802.16)	**2.3, 2.5, 3.5, 3.7, and 5.8 GHz**
802.11a	**5 GHz**
802.11b/g	**2.4 GHz**
802.11n	**2.4 and 5 GHz**
802.11y	**3.7 GHz**
Bluetooth	**2.4 GHz**
GPS	**1.5 GHz**
Zigbee	**868, 915 MHz, and 2.4 GHz**
Ultra-Wideband	**3.1 to 10.6 GHz**
Wireless USB	**3.1 to 10.6 GHz**

Table 1.2

Data Rates of the Wireline Communication Standards

Standard	Data Rate
HyperTransport 1.0/1.1	12.8 GB/s
HyperTransport 2.0	22.4 GB/s
HyperTransport 3.0	41.6 GB/s
DDR2-800	6.4 GB/s
DDR3-1066	8.533 GB/s
DDR3-1333	10.667 GB/s
DDR3-1600	12.8 GB/s
USB 3.0	4.8 Gb/s
SATA 1.5 Gb/s	1.5 Gb/s
SATA 3 Gb/s	3 Gb/s
SATA 6 Gb/s	6 Gb/s
PCI-Express 1.0/1.1	2.5 Gb/s
PCI-Express 2.0	5 Gb/s
PCI-Express 3.0	8 Gb/s
DVI	3.96 Gb/s (Single Link) 7.92 Gb/s (Double Link)
DisplayPort	6.48 or 10.8 Gb/s
HDMI 1.0/1.1/1.2	4.95 Gb/s
HDMI 1.3	10.2 Gb/s

Note: GB/s and Gb/s denote gigabytes per second and gigabits per second, respectively.

baseband signal. Similarly, the standards of the wireline communication standards also specified the maximum data rates of each standard, as listed in Table 1.2. The high-speed I/O interface circuits are used to transmit or receive the high-speed signals between the I/O buses. With the multiplexer (MUX) and demultiplexer (DEMUX), the high-speed signals are transmitted on the I/O buses, while the digital signals are processed in the transceiver. Unfortunately, ESD protection circuits are required to be applied to the I/O pads of the transceiver, including the I/O pads transmitting or receiving the high-speed or RF signals. Thus, ESD protection circuits are required to protect the transceiver against ESD damages without degrading the performance of the transceiver.

1.1.2. Considerations of ESD Protection Design for Radio-Frequency (RF) Front-End Circuits and High-Speed I/O Interface Circuits

Although using power-rail ESD clamp circuit between VDD and VSS does not cause any effect on the internal circuits, applying ESD protection devices at the I/O pads inevitably introduce some negative impacts to circuit performance due to their parasitic effects. The main parasitic effect caused by ESD protection devices which deteriorates the high-frequency performance is the parasitic capacitance. Since the input signal swing is small at the RF input pad, it is sensitive to the shunt parasitic capacitance of ESD protection devices. Therefore, the parasitic capacitance of the ESD protection device at the RF input pad is strictly limited. For the RF transmitter, the devices in the output stage are implemented with large dimensions to transmit the output signals with large enough signal power. With proper design, the devices in the RF output stage can be used to protect the RF output pad against ESD stresses. Thus, ESD protection design for the input pad of the RF receiver is more challenging than that for the output pad of the RF transmitter.

A typical request on the maximum loading capacitance of ESD protection device for a 2-GHz RF input pin was specified as only ~200 fF, which includes the parasitic capacitances of bond pad and ESD protection device [10]. Recently, the negative impacts of ESD protection devices to RF circuit performance had been investigated [11], [12], which had demonstrated that the RF performance such as power gain and noise figure are significantly degraded by the parasitic capacitance of ESD protection devices. The impacts become more serious as the operating frequency of RF front-end circuits and high-speed I/O interface circuits increases. Thus, the parasitic capacitance of ESD protection device must be minimized in ESD protection design for high-frequency applications. Generally, ESD protection circuits cause RF performance degradation with several undesired effects, which are will be discussed in the following.

Parasitic capacitance is one of the most important design considerations for RF ICs and high-speed I/O interface circuits operating in gigahertz frequency bands. Conventional ESD protection devices with large dimensions have the parasitic capacitance which is too large to be tolerated for RF front-end circuits. As shown in Fig. 1.8, the parasitic capacitance of ESD protection devices causes signal loss from the pad to ground. Moreover, the parasitic capacitance also changes the input matching condition. Consequently, the noise figure is deteriorated and the power gain is decreased.

Noise figure is one of the most important merits for RF receivers. Since the RF receiver is a cascade of several stages, the overall noise figure of the RF receiver can be obtained in terms of the noise figure and power gain of each stage in the receiver. For example, if there are m stages cascaded in the RF receiver, the total noise figure of the RF receiver can be expressed as [13]

$$NF_{total} = 1 + \left(NF_1 - 1\right) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \cdots A_{p(m-1)}} \tag{1.1}$$

where NF_i and A_{pi} are the noise figure and the power gain of the i-th stage, respectively. According to (1.1), the noise figure contributed by the first stage is the dominant factor to the total noise figure of the RF receiver (NF_{total}). With the ESD protection circuit added at the input pad to protect the RF receiver IC against ESD damages, the ESD protection circuit becomes the first stage in the RF receiver IC, which is shown in Fig. 1.9. For simplicity, only the first two stages, which are the ESD protection circuit and the low-noise amplifier (LNA), are taken into consideration, as shown in Fig. 1.10. The overall noise figure (NF_{LNA_ESD}) of the LNA with ESD protection circuit is

$$NF_{LNA\_ESD} = NF_{ESD} + \frac{NF_{LNA} - 1}{L^{-1}} = L + \left(NF_{LNA} - 1\right)L = L \cdot NF_{LNA} \tag{1.2}$$

where L is the power loss of the ESD protection circuit, and NF_{LNA} and NF_{ESD} denote the noise figures of the LNA and ESD protection circuit, respectively. Since the ESD protection circuit is a passive reciprocal network, NF_{ESD} equals L. This implies that if the ESD protection circuit has 1-dB power loss, the noise figure of the LNA with ESD protection will directly increase 1 dB as well. Thus, the power loss of the ESD protection circuit must be minimized, because it directly increases the total noise figure of the RF receiver and the increased noise figure can not be suppressed by the power gains of succeeding stages. Moreover, the signal loss due to the ESD protection circuit would also cause power gain degradation in RF circuits.

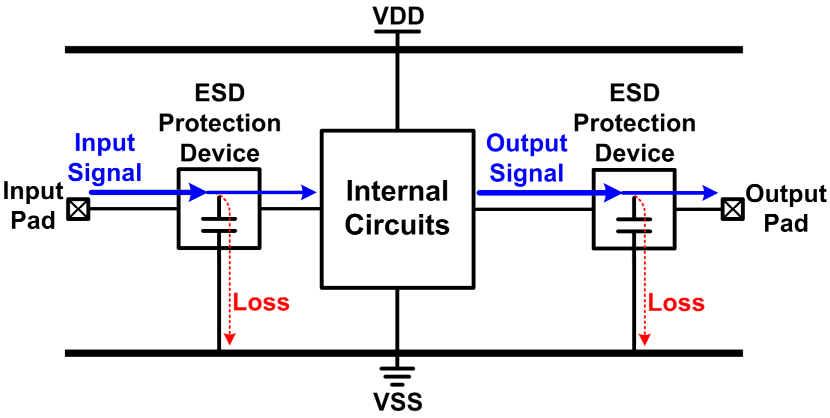


Fig. 1.8. IC chip with ESD protection devices at the input and output pads.

Another negative impact caused by the ESD protection circuit is the input impedance mismatching, which is particularly critical for narrow band RF circuits. With the ESD protection circuit added at the input node, the original input matching condition is changed by the parasitic capacitance from the ESD protection circuit. As a result, the center frequency of the narrow band RF circuit is shifted and the power gain is decreased due to impedance mismatching. The impedance mismatching due to ESD protection devices can be mitigated by co-designing the ESD protection circuit and the input matching network. With the co-design of ESD protection scheme and input matching network, the operating frequency can be tuned to the desired frequency. However, the noise figure is definitely increased after ESD protection circuit is added because more devices indicate more noise sources.

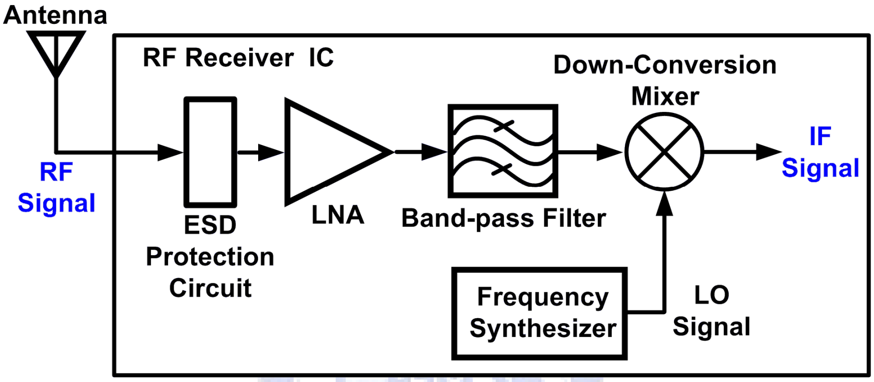


Fig. 1.9. Block diagram of an ESD-protected RF receiver.

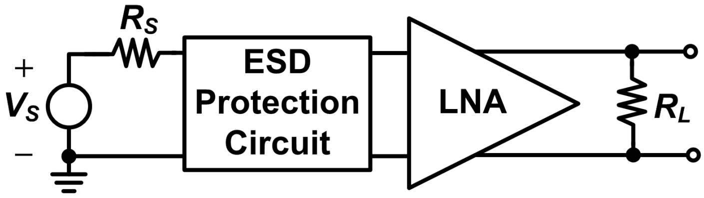


Fig. 1.10. Block diagram of an LNA with ESD protection circuit. V_S, R_S, and R_L denote the source voltage, source resistance, and load resistance, respectively.

Besides the impacts caused by ESD protection device on RF front-end circuits, the parasitic capacitance of the ESD protection device lowers the operating speed of the high-speed I/O interface circuits, because it takes more time to charge or discharge the input or output nodes to the predefined level. Moreover, the parasitic capacitance of ESD protection devices causes signal loss from the pad to ground, which decreases the signal swings. Moreover, RC delay is another impact caused by the ESD protection circuit. With the ESD protection circuit added to the input and output pads, the parasitic capacitance and parasitic resistance from the ESD protection device and the interconnection introduce RC delay to the input and output signals. Thus, the rising and falling time of the signals at the I/O pads with ESD protection become longer. As a result, the eye closure is reduced and the inter-symbol interference (ISI) is deteriorated [14].

In addition to parasitic capacitance, the requirements of ESD protection device characteristics under ESD stresses introduce some design considerations. To provide effective ESD protection, the voltage across the ESD protection device during ESD stresses should be carefully designed. First, the trigger voltage and holding voltage of ESD protection device must be designed lower than the gate-oxide breakdown voltage of MOS transistors to prevent the internal circuits from damage before the ESD protection device is turned on during ESD stresses. Second, the trigger voltage and holding voltage of the ESD protection device must be higher than the power-supply voltage of the IC to prevent the ESD protection devices from being mis-triggered under normal circuit operating conditions. Moreover, the turn-on resistance of ESD protection device should be minimized in order to reduce the joule heat generated in the ESD protection device and the voltage across the ESD protection device during ESD stresses. As CMOS process is continuously scaled down, the power-supply voltage is decreased and the gate oxide becomes thinner, which leads to reduced gate-oxide breakdown voltage of MOS transistor. Typically, the gate-oxide breakdown voltage is decreased to only ~5 V in a 90-nm CMOS process with gate-oxide thickness of ~15 Å. As a result, the ESD design window, defined as the difference between the gate-oxide breakdown voltage of the MOSFET and the power-supply voltage of the IC, becomes narrower in nanoscale CMOS technologies [15]. Furthermore, ESD protection circuits need to be quickly turned on during ESD stresses in order to provide efficient discharge paths in time. In summary, ESD protection design in nanoscale CMOS technologies has encountered more challenges.

1.2. Board-Level Charged-Device-Model (CDM) ESD Issue

Besides HBM and MM ESD tests, the CDM ESD test had been also specified in the chip-level ESD test standards [16], [17]. The equivalent circuit of chip-level CDM ESD test is shown in Fig. 1.11. In the CDM ESD test, the IC chip is charged first, and then the IC is discharged through the tested pin. During the chip-level CDM ESD test, the charges stored in the substrate or package of the IC chip is suddenly discharged to ground, which leads to huge discharging current flowing through the tested pin. Therefore, CDM becomes more critical among the three component-level ESD test standards because of the thinner gate oxide in nanoscale CMOS devices and the larger die size for the application of system on chip (SoC).

The thinner gate oxide causes a lower gate-oxide breakdown voltage, which makes the MOS transistor more sensitive to ESD. Moreover, an IC with larger die size can store more static charges, which leads to larger discharging current during CDM ESD events. CDM ESD current has the features of huge peak current and short duration. Furthermore, CDM ESD current flows from the chip substrate to the external ground, whereas HBM and MM ESD currents are injected from the external ESD source into the zapped pin. Thus, effective ESD protection design against CDM ESD stresses has gotten more requests in IC industry.

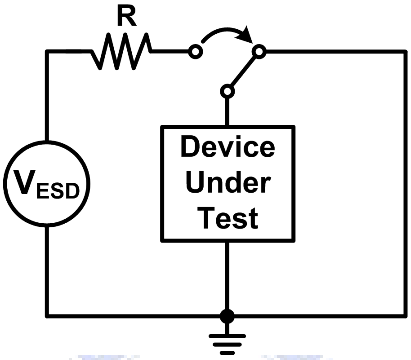


Fig. 1.11. Equivalent circuit of CDM ESD test.

Besides chip-level CDM ESD issue, board-level CDM ESD issue becomes more important recently, because it often causes the ICs to be damaged after the IC is installed to the circuit board of electronic system. For example, board-level CDM ESD events often occur during the assembly of microelectronic modules or module function test on the circuit board of electronic system. Even though the IC has been designed with good chip-level ESD robustness, it would still be very weak in board-level CDM ESD test. The reason is that the discharging current during the board-level CDM ESD event is significantly larger than that of the chip-level CDM ESD event. There are several papers addressing the phenomenon of the board-level CDM ESD events on real IC products [18], [19]. In these two previous works, the ICs which already passed the component-level ESD specifications were still returned by customers because of ESD failure. After performing the field-induced CDM ESD test on the ICs which have been mounted on the printed circuit board (PCB), the failure is the same as that happened in the customer returned ICs. This indicates that the real-world charged-board-model (CBM) ESD damage can be duplicated by the board-level CDM ESD test. These previous works have demonstrated that the board-level CDM ESD events indeed exist, which should be taken into consideration for all IC products.

1.3. Organization of This Dissertation

To solve the challenges in ESD protection design for RF front-end circuits, several new designs are proposed and verified in this dissertation. This dissertation consists of eight chapters and an appendix. In Chapter 2, the published ESD protection designs for RF front-end circuits and high-speed I/O interface circuits are overviewed to analyze the features of each design. The bond pad is the most peripheral devices of the IC, and its parasitic capacitance affects the signal. Thus, the bond-pad capacitance needs to be reduced to mitigate the high-frequency performance degradation. In Chapter 3, a new ultra low-capacitance bond pad structure is proposed to reduce the bond-pad capacitance. Novel distributed ESD protection design for a 1-to-10 GHz distributed amplifier is proposed in Chapter 4. Chapter 5 proposes the co-design of 5-GHz differential LNA and ESD protection circuit. Several new ESD protection schemes for differential I/O pads are proposed and verified. Besides ESD protection design for RF front-end circuits, ESD protection design methodology for gigahertz high-speed I/O interface circuits is presented in Chapter 6. Board-level CDM ESD issue in IC products is investigated in Chapter 7. Chapter 8 gives the conclusions and future works of this dissertation. The outlines of each chapter are summarized below. In the appendix, a draft of the test standard for board-level CDM ESD robustness of ICs is proposed.

Chapter 2 overviews the published ESD protection designs for high-frequency applications, including RF front-end circuits and high-speed I/O interface circuits. The designs are categorized with their individual advantages and disadvantages clearly analyzed. The RF performance degradation caused by ESD protection devices are illustrated with measured results. Besides, the I-V curves of ESD protection devices in the high-current regime are also characterized. The measured device characteristics show that there is a trade-off between ESD robustness and RF performance. The published low-capacitance ESD protection designs are categorized into three groups, which are the circuit solution, layout solution, and process solution. The design complexity, improved parasitic effect, ESD robustness, and area efficiency of all reported designs are compared in this chapter.

In Chapter 3, a new ultra low-capacitance bond pad structure is proposed in a 130-nm CMOS process. The equivalent bond-pad capacitance has been verified to be reduced due to the parallel LC resonant network formed by the added inductor and the overlapped capacitance between the bond-pad metal plate and substrate. Three kinds of stacked inductors under the pad are used to realize different inductances. By designing the inductance and capacitance in the proposed bond pad structure, the frequency band in which the bond-pad capacitance is reduced can be adjusted. Experimental results have shown that the extracted bond-pad capacitance is reduced to almost 0 fF from 4.3 to 4.8 GHz. The new proposed bond pad structure is fully process-compatible to general CMOS processes without any extra process modification.

In Chapter 4, two distributed ESD protection schemes are proposed to protect distributed amplifiers against ESD stresses. Fabricated in a 0.25-μm CMOS process, the distributed amplifier with the equal-sized distributed ESD (ES-DESD) protection scheme, contributing an extra 300 fF parasitic capacitance to the circuit, can sustain the HBM ESD level of 5.5 kV and MM ESD level of 325 V, while exhibits the flat-gain of 4.7 ± 1 dB from1 to 10 GHz. With the same total parasitic capacitance, the distributed amplifier with the proposed decreasing-sized distributed ESD (DS-DESD) protection scheme achieves better ESD robustness, where the HBM ESD level is over 8 kV and MM ESD level is 575 V. The flat-gain of 4.9 ± 1.1 dB over the 1 to 9.2-GHz band is achieved. With these two proposed wideband ESD protection schemes, good wideband RF performances and high ESD robustness of the distributed amplifier can be successfully achieved simultaneously.

In Chapter 5, several new ESD protection schemes are proposed and applied to a 5-GHz differential LNA in a 130-nm CMOS process. This is the first work which investigates the pin-to-pin ESD robustness of differential LNAs. The differential LNA with the conventional double-diode ESD protection scheme has also been designed and fabricated, and it has 2.5-kV HBM and 200-V ESD robustness. Experimental results have demonstrated that the pin-to-pin ESD test is the most critical ESD test mode for the differential LNA with the conventional ESD protection scheme. With the proposed double silicon-controlled rectifier (SCR) ESD protection scheme, the HBM and MM ESD levels are significantly improved to 6.5 kV and 500 V, respectively. Another proposed design uses an ESD bus between the differential input pads, which has 3-kV HBM and 100-V ESD robustness. Besides, a novel design using cross-coupled SCR devices between the differential input pads has been proposed. By applying the cross-coupled SCR devices, not only ESD protection for a single input pad but also pin-to-pin ESD protection can be achieved without adding any extra devices. Its HBM and MM ESD levels are 1.5 kV and 150 V, respectively. By using other diodes beside the cross-coupled SCR devices, the turn-on efficiency of ESD protection devices can be enhanced. With the double diodes and the cross-coupled SCR devices, the ESD-protected differential LNA achieves 4-kV HBM and 300-V MM ESD robustness. Both ESD robustness and RF performance of all fabricated LNAs with and without ESD protection have been measured and compared and in this chapter.

Chapter 6 presents the ESD protection design for gigahertz high-speed I/O interface circuits. After investigating the ESD levels and parasitic capacitances of the ESD protection diodes with different dimensions, the double-diode ESD protection scheme is applied to the dummy receiver NMOS and the dummy transmitter NMOS. Since the connection of the dummy receiver NMOS (dummy transmitter NMOS) is similar to that of the NMOS transistor in a receiver (transmitter) interface circuit, the ESD robustness of the dummy receiver NMOS (dummy transmitter NMOS) can be used to predict the ESD robustness of the high-speed interface circuit with this ESD protection scheme. This whole-chip ESD protection scheme is also applied to a 2.5-Gb/s high-speed I/O interface circuit, and the ESD robustness is larger than 3 kV in HBM with the parasitic capacitance of less than 250 fF. By replacing the N+/P-well diode between the input pad and VSS with the SCR, the ESD robustness can be further improved. In the ESD protection schemes in Chapter 6, the ESD protection devices and part of the ESD detection circuit is placed under the I/O pad to reduce the chip area and the parasitic capacitance on the signal path.

The board-level CDM ESD issues in IC products are investigated in Chapter 7. The mechanism of board-level CDM ESD event is introduced first. Based on this mechanism, an experiment has been performed to investigate the board-level CDM ESD current waveforms under different sizes of PCBs, charged voltages, and series resistances in the discharging path. Experimental results have shown that the discharging current strongly depends on the PCB size, charged voltage, and series resistance. Moreover, chip-level and board-level CDM ESD levels of several test devices and test circuits fabricated in CMOS processes have been characterized and compared. Test results have shown that the board-level CDM ESD level of the test circuit is lower than the chip-level CDM ESD level, which indicates that the board-level CDM ESD event is more critical than the chip-level CDM ESD event. In addition, failure analysis reveals that the failure on the test circuit under board-level CDM ESD test is much severer than that under chip-level CDM ESD test. To provide board-level CDM ESD protection, the solution using the ESD discharger has been proposed. The ESD discharger, which consists of series resistances in the order of MΩ, can be used to slowly discharge the static charges in the module and to prevent the IC chips from being damaged by board-level CDM ESD events.

Chapter 8 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter. Since the standard for the board-level CDM ESD test is not established so far, the proposal of the “Test standard for board-level charged-device-model electrostatic discharge robustness of integrated circuits” (in Chinese) is presented in the appendix. In the proposal, the test methodology and test conditions are clearly defined.

Chapter 2

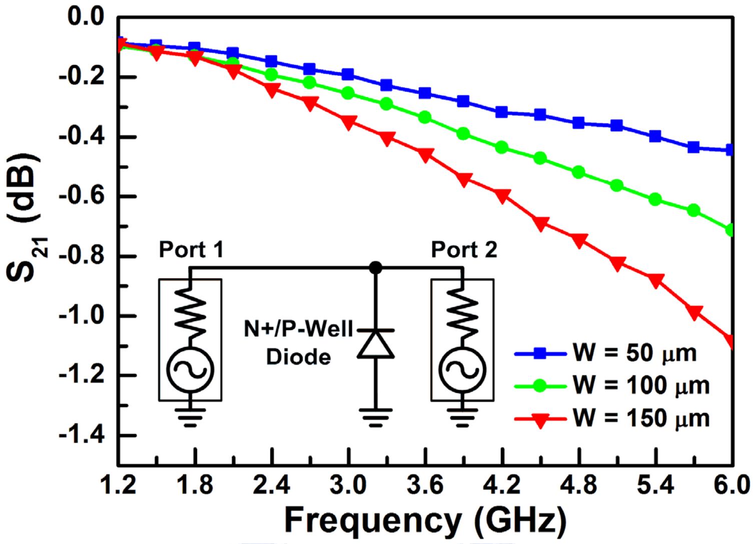
Overview on ESD Protection Design for Radio-Frequency/High-Speed I/O Interfaces

As discussed in Chapter 1, the performance of radio-frequency (RF) front-end circuits and high-speed input/output (I/O) interface circuits is degraded by the parasitic effects of the electrostatic discharge (ESD) protection devices on the signal path. If the ESD protection device is realized by the PN-junction, MOS transistor, BJT, or silicon-controlled rectifier (SCR), it is capacitive. For the RF front-end circuits, the parasitic capacitance causes signal loss from the I/O pads to the AC ground nodes. Consequently the power gain is lowered and the noise figure is increased. If an inductor is used as the ESD protection device, it exhibits inductive impedance under normal circuit operating conditions. Therefore, the impedance matching conditions are changed. As a result, the center frequency will be shifted if the inductive impedance is not considered in the impedance matching network design. For the high-speed I/O interface circuit, the ESD protection devices are mainly realized with capacitive devices. To mitigate the high-speed performance degradation, the parasitic capacitance of ESD protection devices must be as low as possible. After explaining the trade-off between ESD robustness and high-frequency circuit performance, the reported low-capacitance ESD protection designs are overviewed in this chapter [20], [21].

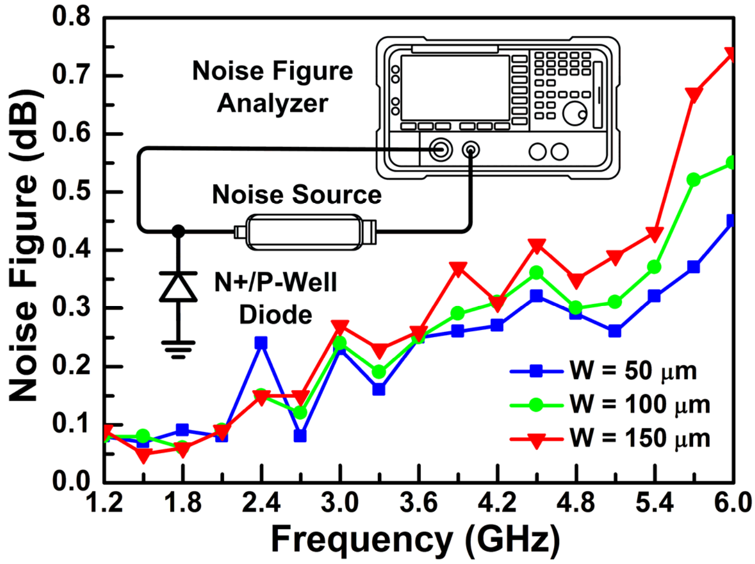
2.1. Trade-Off Between ESD Robustness and High-Frequency Circuit Performance

To apply the electrostatic discharge (ESD) protection devices to radio-frequency (RF) front-end circuits, the RF performance degradation caused by the ESD protection devices should be characterized carefully. To practically investigate the negative impacts caused by the ESD diode on RF performance, three shallow-trench-isolation (STI) N+/P-well diodes with different device dimensions had been fabricated in a 0.25-μm CMOS process [22]. The N+ diffusion (cathode) and P+ diffusion (anode) are separated by the STI. When the

N+/P-well diode is used as the ESD protection device, the N+ diffusion and the P+ diffusion are connected to the I/O pad and VSS, respectively. The N+/P-well diodes with different N+ diffusion widths of 50 μm, 100 μm, and 150 μm were fabricated in the test chip to investigate their impacts on power gain and noise figure. The measured power gains (S_{21}-parameters) and noise figures of the STI N+/P-well diodes with different device dimensions in the frequency band of 1.2–6 GHz are compared in Fig. 2.1(a) and (b), respectively. The measurement setups of S-parameter and noise figure measurements are also illustrated in the insets of Fig. 2.1.



(a)



(b)

Fig. 2.1. Measured (a) power gains (S_{21}-parameters) and (b) noise figures of the STI N+/P-well diodes with different device dimensions in a 0.25-μm CMOS process.

The measured results showed that the power gain of the STI diode with the same device dimension is decreased when the operating frequency increases. The power gain is decreased drastically by the STI diodes with larger device dimensions in higher frequency bands. Moreover, the differences of the power gain loss of the STI diodes between different device dimensions become larger in higher frequency bands. This demonstrated that the parasitic capacitance of the ESD protection device losses RF signal to ground and degrades power gain. Since the power gain loss is larger for larger STI diodes, the larger STI diodes exhibit higher noise figure, as shown in Fig. 2.1(b). On the other hand, ESD robustness is higher as the size of STI diode is increased. The HBM ESD robustness of the stand-alone STI diode is improved from 5.8 kV to over 8 kV as the width is increased from 50 µm to 100 µm. The STI diodes with 50-µm and 100-µm width have the MM ESD robustness of 125 V and 250 V, respectively.

The measured results demonstrated the trade-off between the ESD robustness and RF performance. Devices with larger dimensions have higher ESD level, but they cause more performance degradation. Therefore, how to design an effective on-chip ESD protection circuit for RF front-end and high-speed I/O interface circuits operating in gigahertz frequency bands with minimum performance degradation is a challenge, which must be solved. If high ESD robustness with very slight high-frequency performance degradation is preferred, several low-capacitance ESD protection strategies were reported to be effective. The reported designs are overviewed in the following sections.

2.2. ESD Protection Designs by Circuit Solutions

To mitigate the performance degradation due to ESD protection circuits, circuit design techniques had been used to reduce the parasitic capacitance from the ESD protection device. With the extra circuit design, the parasitic capacitance of the ESD protection device can be significantly reduced or even cancelled. Furthermore, no process modification is needed by using the circuit design techniques to reduce the parasitic capacitance. However, the silicon area may be increased due to the additional components of extra circuit design. In this section, the ESD protection designs by circuit solutions in standard CMOS processes are overviewed.

2.2.1. Stacked ESD Protection Devices

Although conventional double-diode ESD protection design shown in Fig. 1.6 can be applied to RF frond-end circuits, it is only suitable for small ESD protection devices [23]. In order to reduce the performance degradation caused by the parasitic capacitances from the ESD diodes at I/O pad, the device dimensions of ESD diodes should be reduced to reduce the parasitic capacitance. However, the minimum device dimensions of ESD diodes can not be shrunk unlimitedly because ESD robustness needs to be maintained. In order to further reduce the parasitic capacitance from ESD diodes without sacrificing ESD robustness, the ESD diodes in stacked configuration had been proposed, as shown in Fig. 2.2 [24], [25]. If the parasitic capacitance of each ESD protection device is C_{ESD} and n ESD protection devices are stacked, the overall equivalent parasitic capacitance will theoretically becomes C_{ESD} / n Thus, more stacked ESD devices lead to the more significant parasitic capacitance reduction. Besides reducing parasitic capacitance, the leakage current of ESD diodes under normal circuit operating conditions can be also reduced by using the stacked configuration. Although stacked ESD protection devices can reduce the parasitic capacitance and leakage current, the overall turn-on resistance and the voltage across the stacked ESD protection devices during ESD stresses are increased as well, which is adverse to ESD protection.

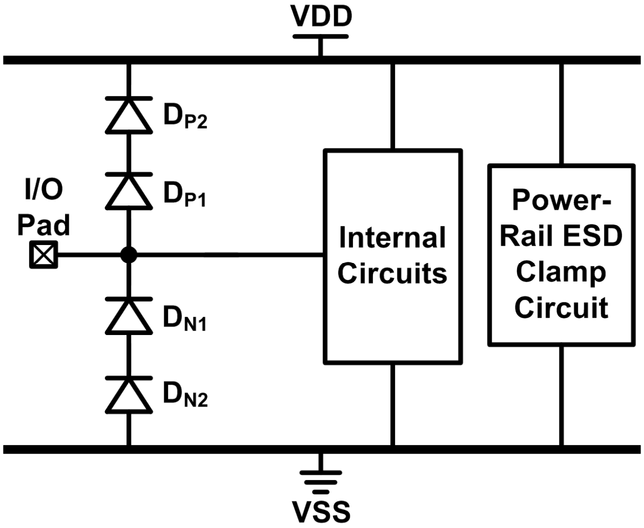


Fig. 2.2. ESD protection design with stacked ESD diodes to reduce the capacitance from I/O pad to AC ground nodes.

2.2.2. Impedance Cancellation Technique

Besides, several ESD protection designs with inductor to reduce or cancel the equivalent parasitic capacitance of ESD protection devices had been proposed. Fig. 2.3 shows an ideal parallel LC resonator and the simulated S_{21}-parameter under different frequencies. In a parallel LC resonator composed of the inductance L and capacitance C, the resonant frequency (ω_0) is

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{2.2}$$

At the resonant frequency, the signal loss is ideally zero, which denotes that the equivalent capacitance is infinite. Based on this concept, the ESD protection circuit with a parallel inductor had been proposed, as shown in Fig. 2.4 [26]–[30]. The inductance of L_1 was designed to resonate with the parasitic capacitance of the ESD protection device at the operating frequency of the RF front-end circuit. With the parallel LC network resonating at the operating frequency, the shunt impedance of L_1 and the ESD protection device becomes very large, which can effectively suppress signal loss. Therefore, the ESD protection design using impedance-cancellation technique can mitigate the impacts on circuit performance for circuits operating in a narrow frequency band. L_1 can be realized either by the on-chip spiral inductor or by utilizing the bond wire in the package [26]–[29]. Furthermore, the inductor L_1 can not only resonates with the parasitic capacitance of the ESD protection device but also serves as an ESD protection device by itself. In this configuration, the DC biases must be equal on both sides of L_1. Otherwise, there will be steady leakage current flowing through L_1 under normal circuit operating conditions.

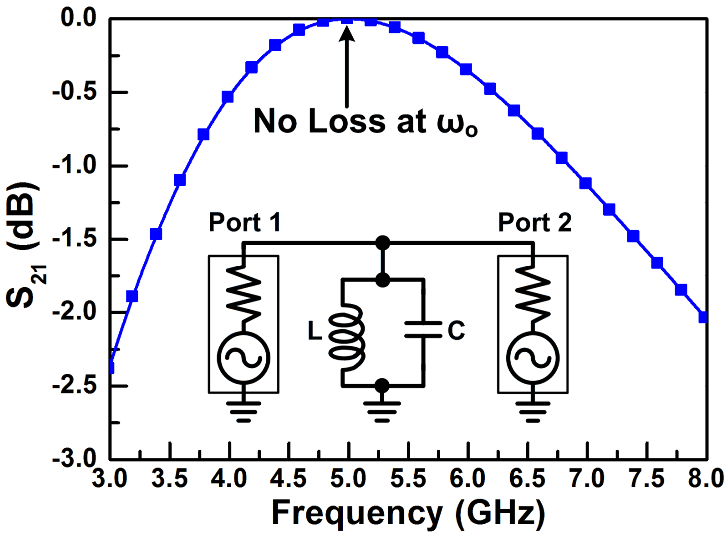


Fig. 2.3. Simulated S_{21}-parameter of an ideal parallel LC resonator under different frequencies.

Another ESD protection design using a parallel inductor to cancel the parasitic capacitance of the ESD diode is shown in Fig. 2.5 [31]. Since VDD is an AC ground node, the inductor L_P is connected between the I/O pad and VDD to form a parallel LC resonator with the ESD protection device between the I/O pad and VSS. The inductor L_P also serves as an ESD protection device between I/O pad and VDD. The inductor and the parasitic capacitance of the ESD protection device are designed to resonate at the operating frequency of the RF front-end circuit to minimize performance degradation caused by the ESD protection device. With an inductor directly connected between the I/O pad and VDD, the ESD protection device is reverse biased with the largest possible DC voltage under normal circuit operating conditions, which leads to the minimum the parasitic PN-junction capacitance in the ESD protection device. The placement of the inductor and the ESD protection device can be interchanged to provide the same function. In this design, a DC blocking capacitor C_{block} is required to provide a separated DC bias for the internal circuits.

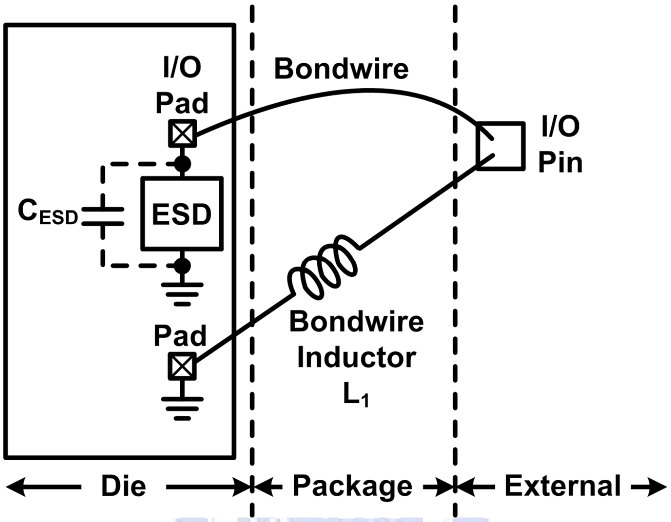


Fig. 2.4. ESD protection design with the parallel LC resonator.

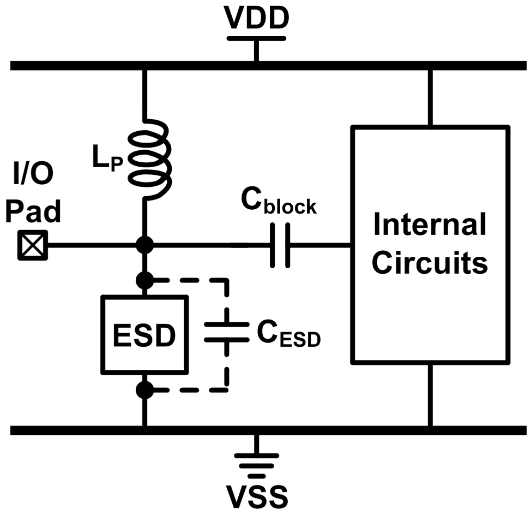


Fig. 2.5. ESD protection circuit using the impedance-cancellation technique. The inductor L_P cancels the parasitic capacitance from ESD protection device and provides ESD current path between VDD and the I/O pad.

2.2.3. Impedance Isolation Technique

The low-capacitance ESD protection design utilizing the impedance isolation technique had been reported [22], [32]–[36]. As shown in Fig. 2.6, an LC-tank, which consists of the inductor L_P and the capacitor C_1, is placed between the I/O pad and VDD. Another LC-tank consisting of the inductor L_N and the capacitor C_2 is placed between the I/O pad and VSS. The ESD diodes D_P and D_N are used to block the steady leakage current path from VDD to VSS under normal circuit operating conditions. At the resonant frequency of the LC-tank, there is ideally infinite impedance from the signal path to the ESD diode. Consequently, the parasitic capacitances of the ESD diodes are isolated, and the impacts of the ESD diodes can be significantly reduced. During ESD stresses, ESD current is discharged through the inductors and the ESD diodes. With the power-rail ESD clamp circuit providing a discharge path between VDD and VSS, the ESD diodes are operated in the forward-biased condition to achieve high ESD robustness under all ESD test modes. Furthermore, the capacitors C_1 and C_2 can also be directly realized with ESD protection devices to provide other ESD paths apart from the inductors.

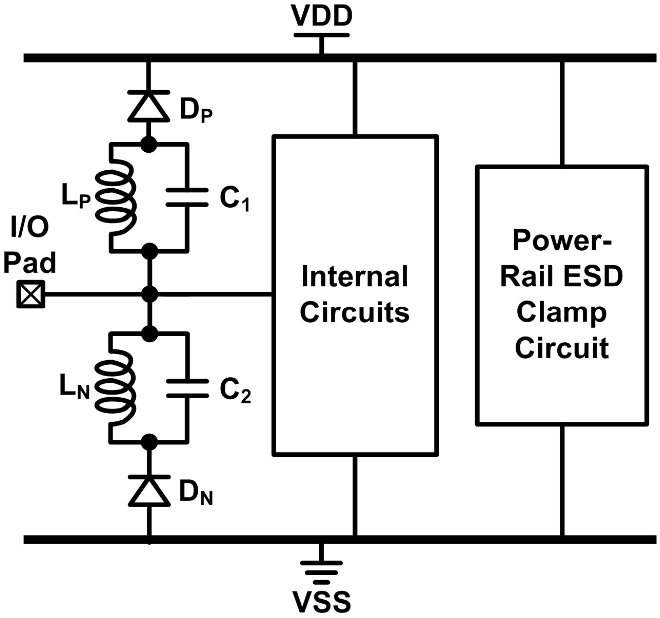


Fig. 2.6. ESD protection design with LC-tanks.

Besides only one LC-tank, the modified design with stacked LC-tanks connected between the signal path and the ESD diode had also been proposed, as shown in Fig. 2.7 [32]–[35]. In Fig. 2.7, two or more LC-tanks are stacked to provide better impedance isolation at resonance, which can further mitigate the parasitic effects from the ESD diodes.

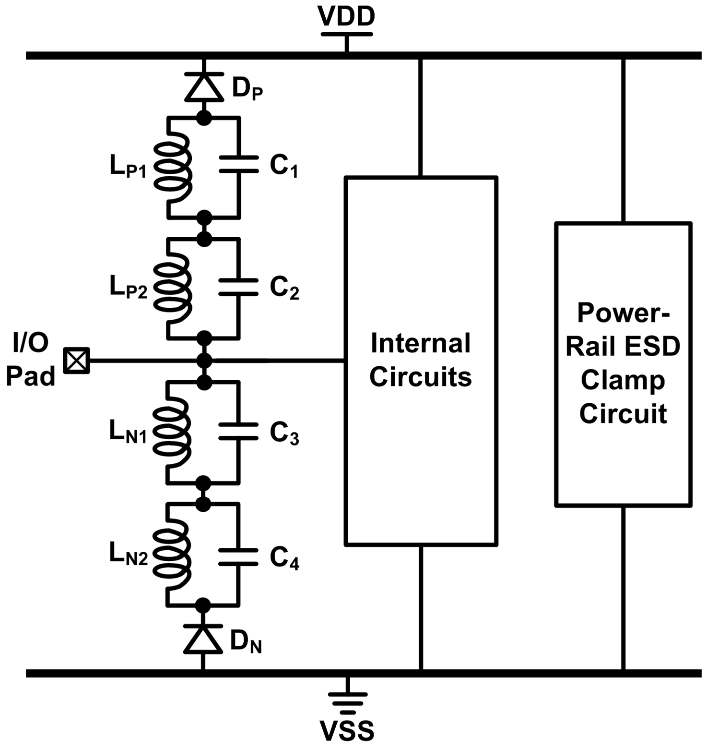


Fig. 2.7. ESD protection design with stacked LC-tanks.

2.2.4. Series LC Resonator

It was mentioned in the previous section that narrow band ESD protection design can be achieved by using the parallel LC resonator. For the wideband RF front-end circuits, the series LC resonator can be used for ESD protection. The simulated S_{21}-parameter of an ideal series LC resonator under different frequencies is shown in Fig. 2.8. With inductance L and capacitance C in the series LC resonator, the resonant frequency (ω_0) is identical to that shown in (2.2). At the resonant frequency, there is a notch where the signal loss is very large, which means that the signal at the notch frequency will be totally lost. However, at frequencies above the resonant frequency, the impedance of the series LC resonator becomes inductive, so the magnitude of impedance increases (which means the signal loss becomes much smaller) with frequency until the self-resonant frequency of the inductor is reached. Thus, wideband ESD protection can be achieved by designing the application band of the series LC resonator to cover the frequency band of the RF signal. Fig. 2.9 shows the ESD protection design proposed in [26]–[29], which utilizes the series LC resonator. The inductance of L_1 and the parasitic capacitance of the ESD protection device (C_{ESD}) are designed to resonate at the image frequency, which provides very low impedance at the image frequency. Thus, the image signal can be filtered out by the notch filter formed by the inductor L_1 and the ESD protection device. During ESD stresses, the inductor L_1 and the ESD protection device provide ESD current path.

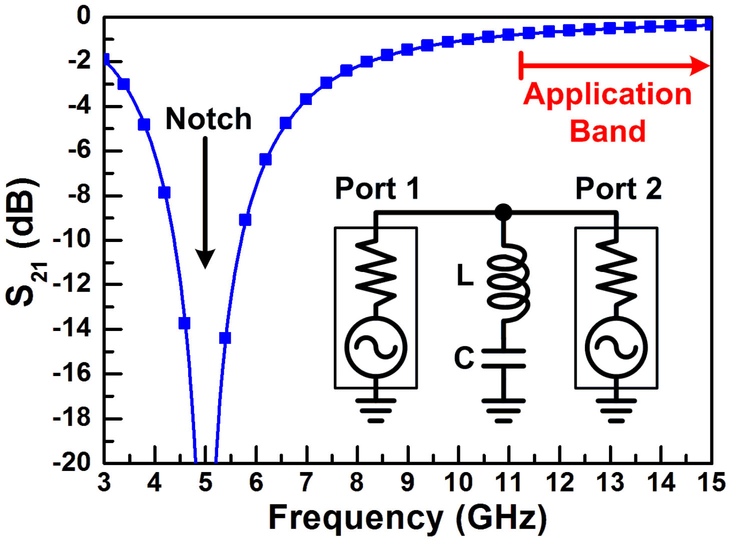


Fig. 2.8. Simulated S_{21}-parameter of an ideal series LC resonator under different frequencies.

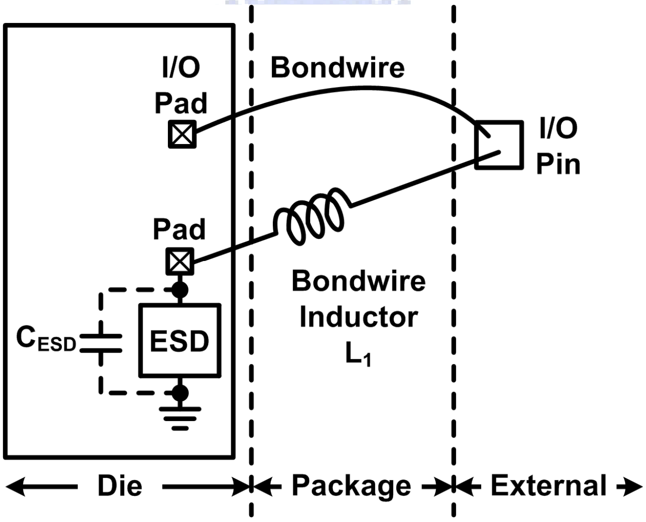


Fig. 2.9. Wideband ESD protection design with the series LC resonator.

Another design utilizing the series LC resonator is shown in Fig. 2.10 [37]–[39]. In Fig. 2.10, two series LC resonators are placed between the I/O pad and VSS, and between the I/O pad and VDD, respectively. In this design, ESD current paths from the I/O pad to both VDD and VSS are provided by the inductors and the ESD protection devices. The modified design, which uses only one inductor connected in series with the two ESD protection devices connected to VDD and VSS, is shown in Fig. 2.11 [37]–[39]. In Fig. 2.11, the capacitance in the series LC resonator is the sum of the parasitic capacitances of the two ESD protection devices. Therefore, the inductance used in Fig. 2.11 is smaller than that used in Fig. 2.10

under the same resonant frequency. Therefore, the chip area and the cost can be reduced by using the modified design.

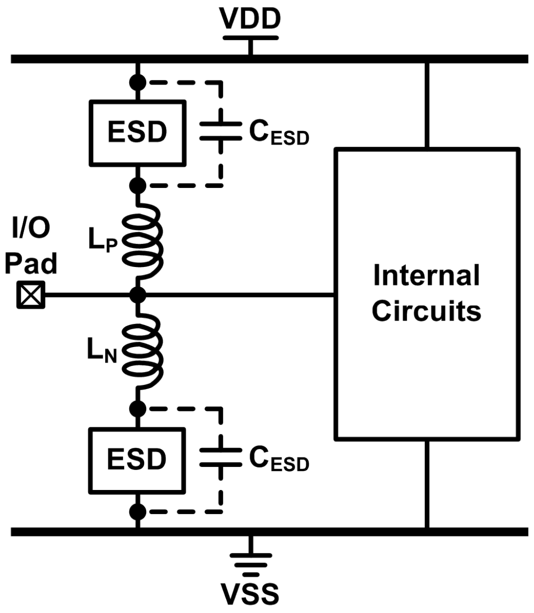


Fig. 2.10. Another wideband ESD protection design with the series LC resonator.

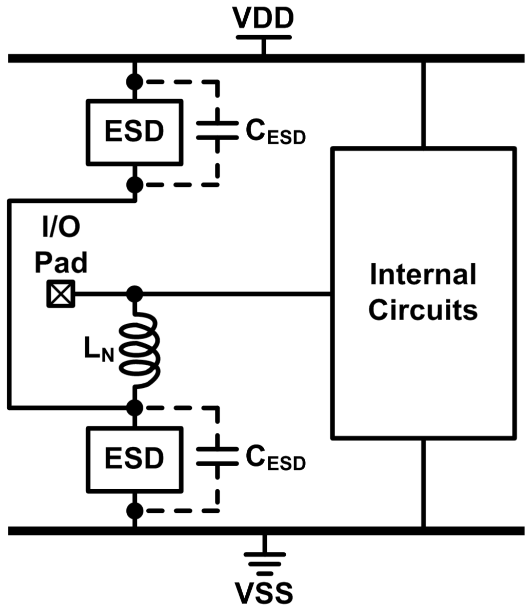


Fig. 2.11. Modified wideband ESD protection design with the series LC resonator. Only an inductor is connected in series with two ESD protection devices.

2.2.5. Impedance Matching

Conventionally, ESD protection devices were realized with small device dimensions to minimize the parasitic effects. However, ESD robustness declines with smaller device dimensions. To solve this dilemma, ESD protection devices can be treated as a part of the impedance matching network. By co-designing the ESD protection circuit and the impedance matching network, large ESD protection devices can be used to achieve high ESD robustness with their parasitic capacitance matched. The techniques of matching the parasitic capacitance of ESD protection device had been proposed [40]–[43].

In the ESD protection circuit shown in Fig. 2.12, ESD current is discharged from the I/O pad through the ESD protection devices to VDD and VSS. The combined impedance of the shunt and series impedance is designed to provide impedance matching at the I/O pad with ESD protection [40], [41]. Various circuit components can be used to realize the shunt and series impedance.

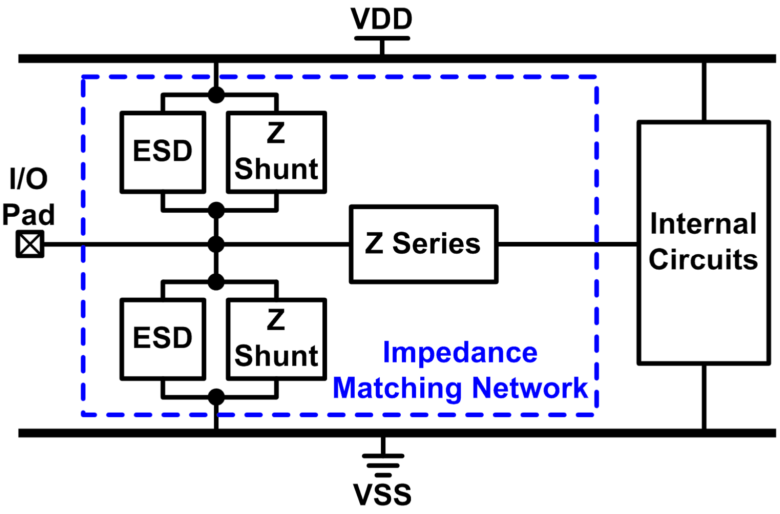


Fig. 2.12. ESD protection design with shunt and series components to achieve impedance matching.

The ESD protection design using inductance to match the parasitic capacitances of ESD protection devices is shown in Fig. 2.13 [42]. In Fig. 2.13, the ESD protection devices are placed next to the I/O pad, and provide ESD protection for the IC. The transmission line (T-Line) connects the IC and the external components. The inductive component L, which can be an inductor or a transmission line, is connected in series with the signal line, and matches the parasitic capacitances of the ESD protection devices, internal circuit, bond pad, and termination element (R_T). The small-signal equivalent circuit model of this matching network is shown in Fig. 2.14, where the inductive component L separates the two parasitic capacitances C_1 and C_2. C_1 and C_2 are

$$C_1 = C_{\text{int}} + C_{RT} \tag{2.3}$$

$$C_2 = C_{Pad} + C_{ESD} \tag{2.4}$$

where C_{int}, C_{RT}, C_{Pad}, and C_{ESD} denote the parasitic capacitance at the input node of the internal circuit, the parasitic capacitances of the termination element, bond pad, and ESD protection devices, respectively. The inductance of L is designed to neutralize the reactance of C_1 and C_2 at the operating frequency. Namely, the design goal is

$$X_{C1} + X_{C2} + X_L = 0 \tag{2.5}$$

where X_{C1}, X_{C2}, and X_L are the reactances of C_1, C_2, and L, respectively. Once (2.5) holds, the overall impedance matching is achieved.

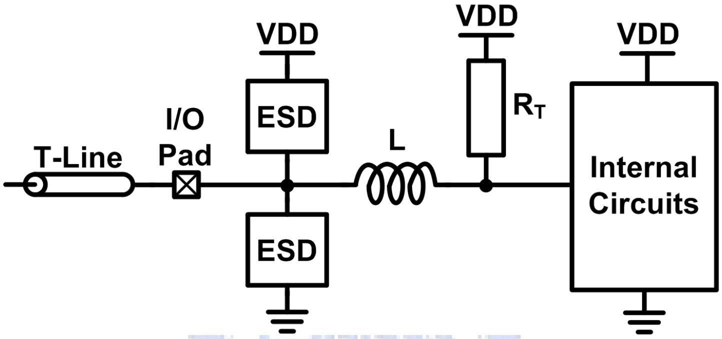


Fig. 2.13. ESD protection design using the series inductor to match the parasitic capacitances.

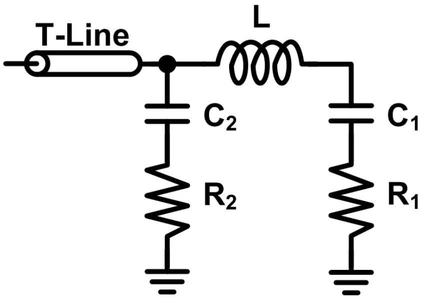


Fig. 2.14. Small-signal equivalent circuit model of the schematic shown in Fig. 2.13.

Another ESD protection design with impedance matching is shown in Fig. 2.15 [43]. The capacitors C_1, C_2, and C_3 provide impedance matching with the balun, which converts the signals between single-ended and differential modes. The ESD protection devices include diodes D_1 to D_4 and inductor L_1. Under ESD stresses, the voltage corresponding to the ESD event is divided between the capacitors C_1, C_2, and C_3. The voltage across C_2 is transposed from the first winding to the second winding of the balun, and is clamped to VDD by the diodes D_3 and D_4. Besides, the diode D_1 and the inductor L_1 provide the ESD path from the I/O pad to VDD and VSS, respectively.

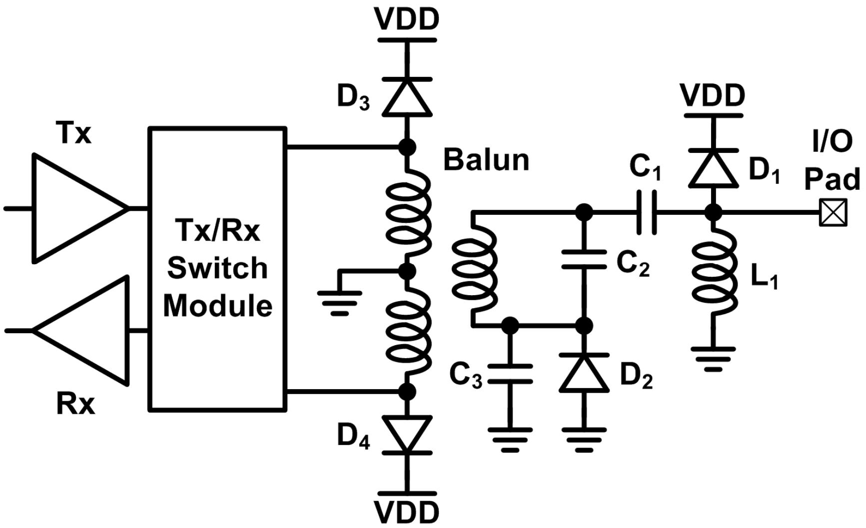


Fig. 2.15. ESD protection design with a balun and the impedance matching network.

2.2.6. *Inductive ESD Protection*

Besides capacitive ESD protection devices, the ESD protection designs for LNA using inductor as the ESD protection device had been reported [44], [45], as shown in Fig. 2.16. The ESD protection inductor (L_{ESD}) is placed between the input pad and VSS. Inductors exhibits higher impedance at higher frequencies. Since the frequency component of ESD is much lower than that of the RF signal, the inductor can pass the ESD currents while block the RF signal. In the inductor-based ESD protection design, L_{ESD} was selected to resonate with the parasitic capacitances at the RF operating frequency. Therefore, the parasitic effects of the ESD protection inductor are compensated. In this design, an AC coupling capacitor C_c is needed to avoid the steady leakage current through the ESD protection inductor. To efficiently sink the ESD current, the metal width of the ESD protection inductor should be wide enough to enhance the current handling capability and the parasitic series resistance. However, inductors realized very wide metal traces occupy large chip area. This is the main design concern in the inductor-based ESD protection.

Since most of the LNAs need a gate inductor connected between the input pad and the gate terminal of the input MOS transistor, the ESD protection inductor can be merged with the gate inductor to save the chip area [46]. As shown in Fig. 2.17, the ESD protection inductor is placed under the gate inductor to form a transformer. Consequently, there is no area penalty for the ESD protection inductor. The transformer-based ESD protection design provides not only ESD protection for the input pad but also the gate inductor in the impedance matching network.

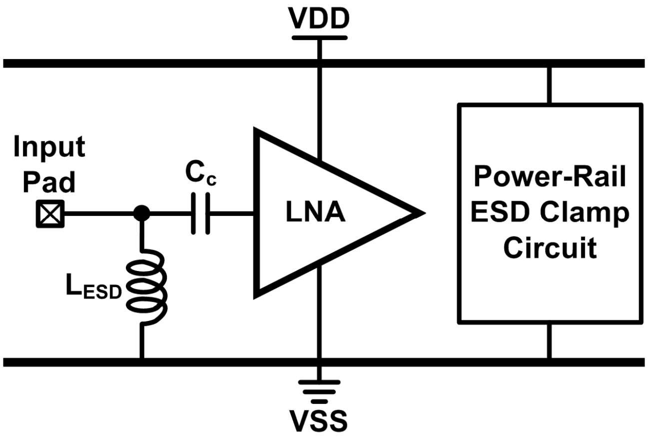


Fig. 2.16. Inductor-based ESD protection design for LNA.

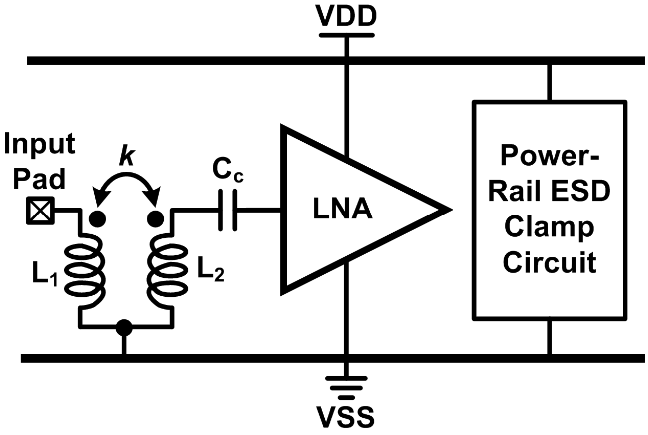


Fig. 2.17. Transformer-based ESD protection design for LNA.

2.2.7. T-Coil

With a transformer in the architecture, the wideband ESD protection design with T-coil had been reported, as shown in Fig. 2.18 [47]. With proper impedance matching design, this circuit can provide a purely resistive input impedance of R_T, which is independent of frequency and parasitic capacitance of the ESD protection device. The input impedance Z_{in} remains resistive at all frequencies as long as the following conditions hold:

$$L_1 = L_2 = \frac{C_L R_T^2}{4}\left(1 + \frac{1}{4\zeta^2}\right) \tag{2.6}$$

$$C_B = \frac{C_L}{16\zeta^2} \tag{2.7}$$

$$k = \frac{4\zeta^2 - 1}{4\zeta^2 + 1} \tag{2.8}$$

where ζ is the damping factor of the network transfer function V_X / I_{in}. When the T-coil is used for ESD protection design, C_L is realized by the parasitic capacitance of ESD protection device. Therefore, large ESD protection device can be used without degrading the RF performance. In the first ESD protection design with T-coil, the NMOS and PMOS transistors with gate-coupled technique is used. Recently, the SCR has been used as the ESD protection device in the T-coil-based ESD protection design for a high-speed transmitter [48]. With the T-coil to compensate the parasitic effects of the SCR, the return loss of the transmitter was improved.

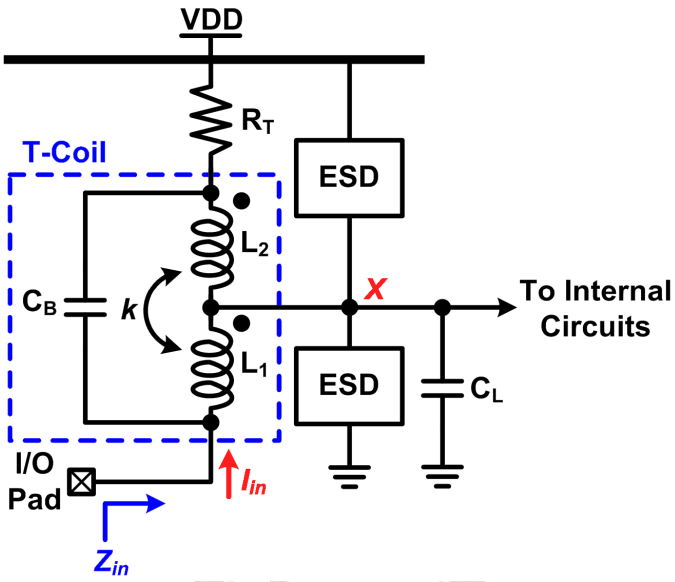


Fig. 2.18. Wideband ESD protection design with T-coil.

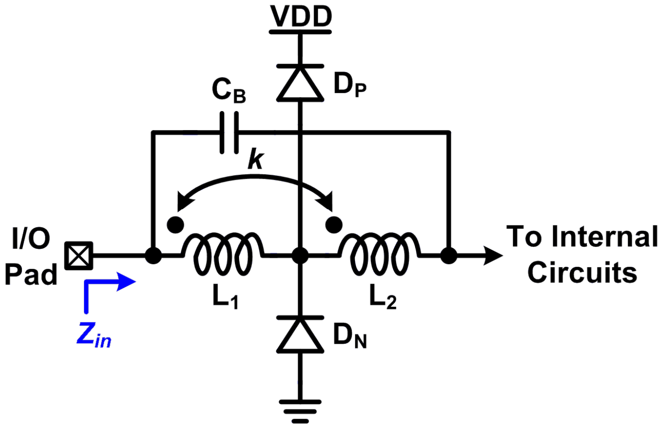


Fig. 2.19. Wideband ESD protection with T-diode.

Another T-coil-based ESD protection design was reported for the wideband LNA [49]. As shown in Fig. 2.19, the transformer plus diode (T-diode) is used to protect the wideband LNA. In this design, the capacitor C_B in the T-diode was realized with the parasitic capacitance between the inductors L_1 and L_2. Since the T-coil and the T-diode can overcome the band-limiting problems in the narrow band ESD protection circuits, they are suitable for wideband RF front-end circuits.

2.2.8. Distributed ESD Protection

To achieve wideband impedance matching with ESD protection devices, the distributed ESD protection scheme had been proposed [50]–[52]. As shown in Fig. 2.20, the ESD protection devices are divided into several sections with the same device dimensions and are impedance matched by the transmission lines (T-lines) or inductors. The number of ESD protection devices can be varied to optimize the high-speed circuit performance. Each ESD protection device is connected to VDD or VSS, which is an equivalent AC ground node. The distributed ESD protection devices are impedance matched by the transmission lines under normal circuit operating conditions. With the ESD protection devices divided into small sections and matched by the transmission lines, such a distributed ESD protection scheme can achieve wideband impedance matching. The first reported distributed ESD protection scheme is the equal-size distributed ESD (ES-DESD) protection scheme with diodes, as shown in Fig. 2.21. In the ES-DESD protection scheme, the ESD protection diodes are equally divided into four sections. However, most of ESD current is expected to flow through the section which is closest to the I/O pad.

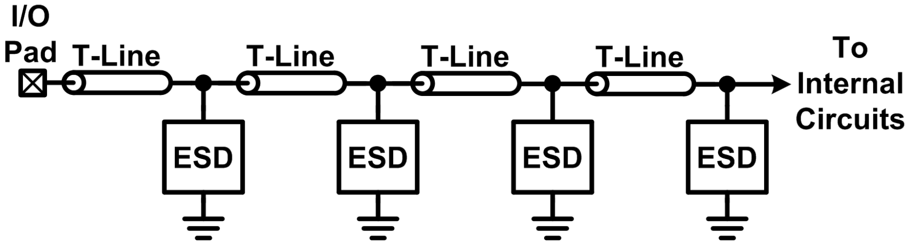


Fig. 2.20. Distribute ESD protection scheme.

To improve ESD robustness of distributed ESD protection scheme, the modified design of decreasing-size distributed ESD (DS-DESD) protection scheme had been proposed, as shown in Fig. 2.22 [53]. The DS-DESD protection scheme allocates the ESD protection devices with decreasing sizes from the I/O pad to the internal circuit. Under the same total parasitic capacitance of the ESD protection devices, the DS-DESD protection scheme had been proven to have higher ESD robustness than that of the ES-DESD protection scheme, because the first section of the ESD protection devices in the DS-DESD protection scheme is larger than that in the ES-DESD protection scheme. With larger ESD protection devices close to the I/O pad, ESD robustness is improved. Moreover, it had also been verified that good wideband impedance matching is still maintained in the DS-DESD protection scheme.

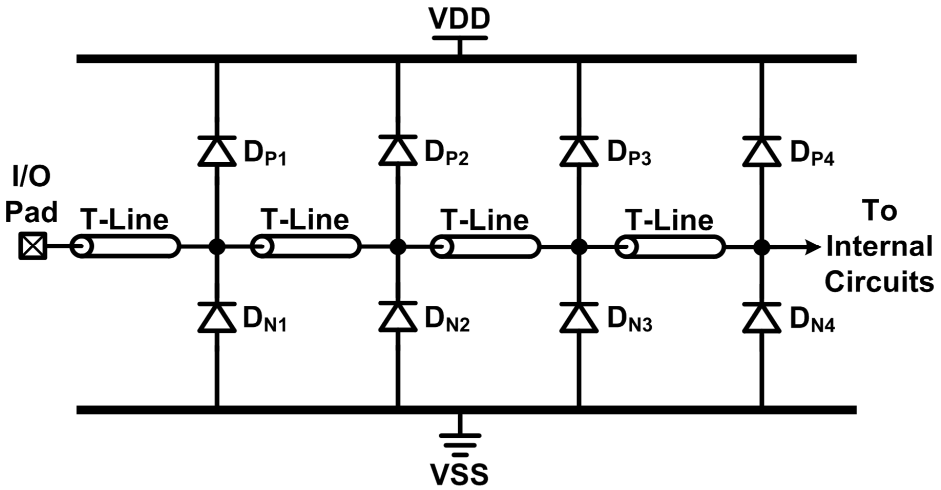


Fig. 2.21. Equal-size distributed ESD (ES-DESD) protection scheme.

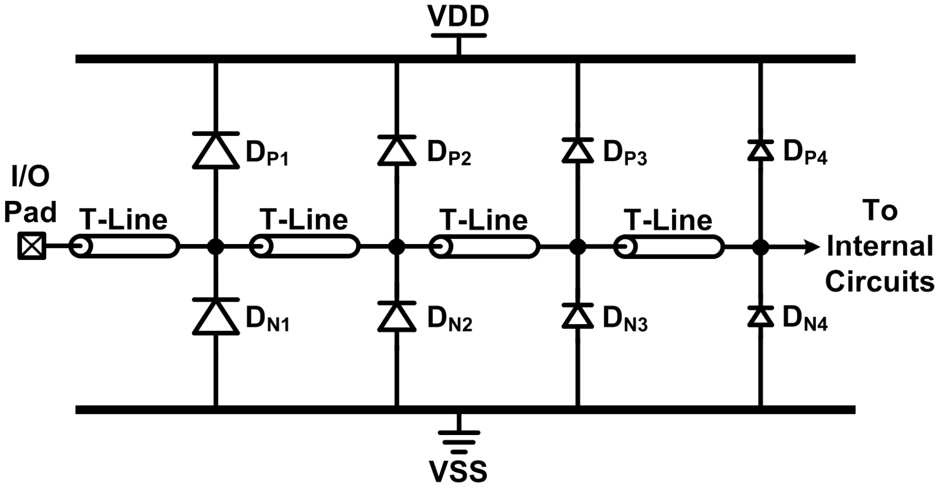


Fig. 2.22. Decreasing-size distributed ESD (DS-DESD) protection scheme.

Another distributed ESD protection design is the π-model distributed ESD (π-DESD) protection scheme, as shown in Fig. 2.23 [54]. Composed of one pair of ESD protection diodes close to the input pad, the other pair close to the internal circuits, and a transmission line matching these parasitic capacitances, the π-DESD protection scheme can also achieve both good wideband impedance matching.

The matching loci of ES-DESD, DS-DESD, and π-DESD protection schemes in Smith chart are shown in Fig. 2.24(a), (b), and (c), respectively. Since the ESD protection devices are divided into several sections and are matched individually in the distributed ESD protection schemes, the matching loci do not deviate from the real axis substantially. Low-quality-factor (low-Q) matching with wideband impedance matching are achieved in the distributed ESD protection schemes.

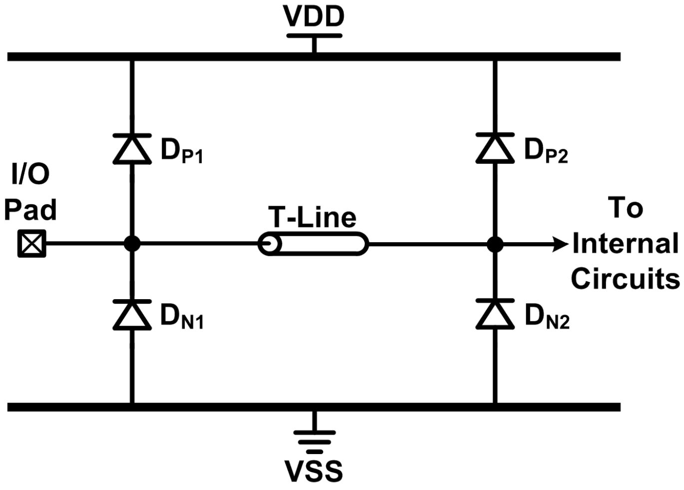
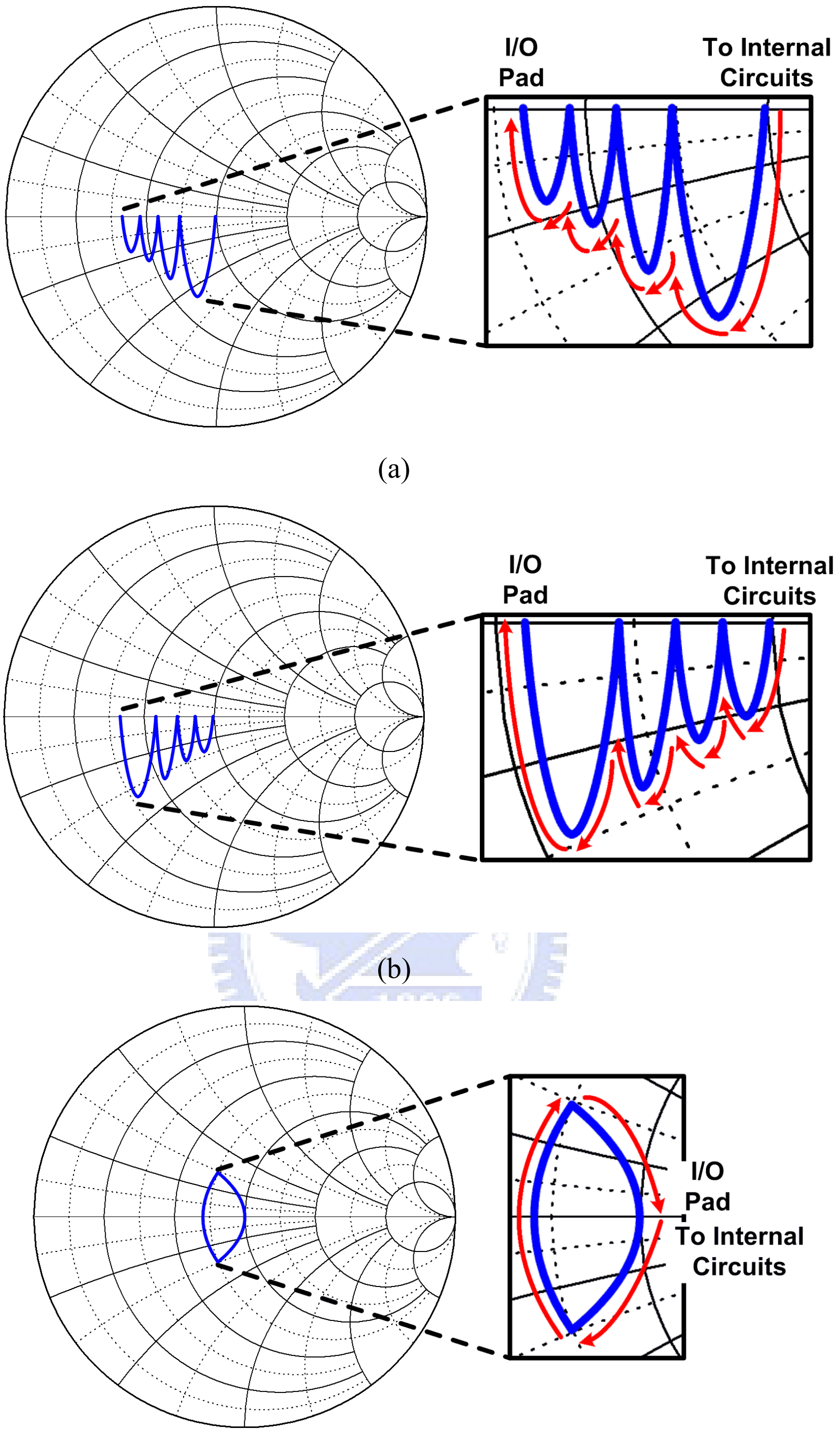


Fig. 2.23. π-model distributed ESD (π-DESD) protection scheme.

2.2.9. Biasing Technique

In the conventional I/O buffers, the gate-grounded NMOS (GGNMOS) and gate-VDD PMOS (GDPMOS) are used to provide ESD protection, as shown in Fig. 2.25. To reduce the parasitic capacitance, the ESD protection design with increased reverse-biased voltages across the PN-junctions in the ESD protection devices had been proposed, as shown in Fig. 2.26 [55]. In Fig. 2.26, the PMOS M_{P2} is used instead of the GGNMOS M_{N1} in Fig. 2.25. The four diodes D_{SP1}, D_{DP1}, D_{SP2}, and D_{DP2} denote the parasitic source-to-well and drain-to-well PN-junction diodes in M_{P1} and M_{P2}, respectively. Since the source and gate terminals of M_{P1} and M_{P2} are at equal potentials, M_{P1} and M_{P2} are kept off under normal circuit operating conditions. During PD-mode ESD stresses, M_{P1} is turned on as a diode-connected PMOS to discharge ESD current, and the parasitic diodes D_{DP1} and D_{SP2} are forward biased to provide ESD path from the I/O pad to VDD. During NS-mode ESD stresses, M_{P2} is turned on as a diode-connected PMOS to discharge ESD current. As compared with the GGNMOS M_{N1} in Fig. 2.26, the parasitic PN-junction diodes of M_{P2} are reversed biased with larger voltages, which results in smaller parasitic junction capacitance. This is because the cathodes of the parasitic PN-junction diodes are biased to the highest potential in the circuit under normal circuit operating conditions.



(a)

(b)

(c)

Fig. 2.24. Matching loci of (a) ES-DESD, (b) DS-DESD, and (c) π-DESD protection schemes in the Smith chart.

If the voltage across a capacitor can be kept at zero, the effective capacitive loading effect can be ideally eliminated. An ESD protection design utilizing the feedback technique to keep the voltage across the parasitic capacitance to zero had been proposed [56]. As shown in Fig. 2.27, an amplifier in unity-gain configuration is used to keep the voltages across the base-emitter junctions of Q_1 and Q_2 to zero. During PD-mode ESD stresses, the base-emitter junction Q_1 is forward biased to provide ESD current. During NS-mode ESD stresses, ESD current is discharged from VSS through D_2 and the base-emitter junction of Q_2. Since the amplifier provides unity-gain feedback across the I/O pad and the bases of Q_1 and Q_2, ideally a zero voltage is kept across the base-emitter junctions of Q_1 and Q_2. Thus, the effective parasitic capacitances of the base-emitter junction diodes of Q_1 and Q_2 are ideally eliminated from the I/O pad.

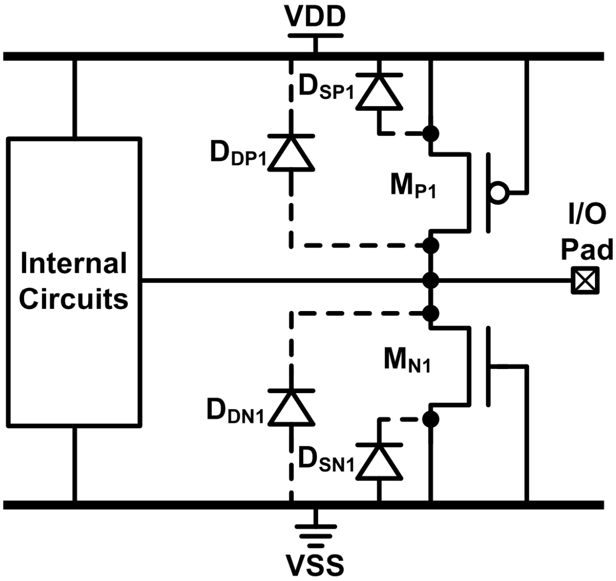


Fig. 2.25. Traditional ESD protection circuit with GDPMOS and GGNMOS.

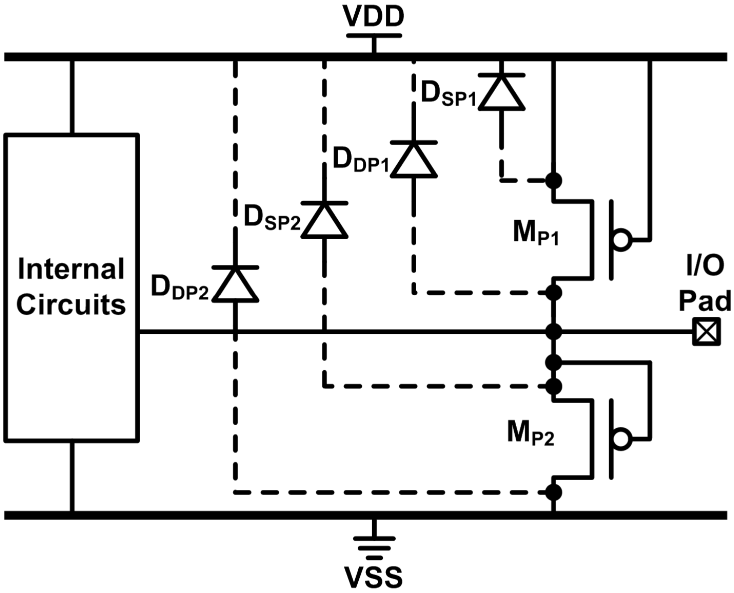


Fig. 2.26. ESD protection circuit with increased reverse-bias voltage to reduce the parasitic PN-junction capacitance.

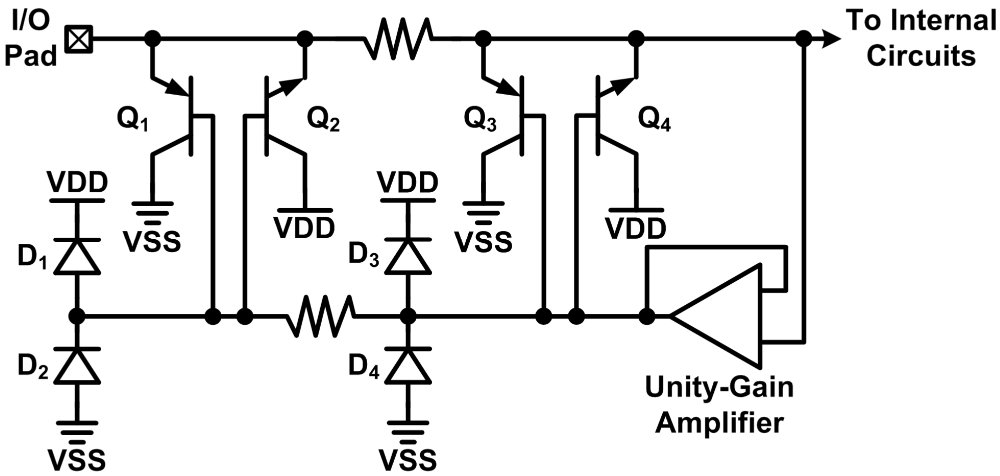


Fig. 2.27. ESD protection circuit utilizing the unity-gain amplifier to keep the voltage across the parasitic capacitance to zero.

2.2.10. Substrate-Triggering Technique

If no extra trigger circuit is added, the parasitic BJTs in MOSFET and SCR are turned on when the avalanche breakdown occurs in the PN-junction. Devices with such a slow turn-on speed and high trigger voltage can not efficiently protect the internal circuit against ESD stresses. To solve the problem, the substrate-triggering technique had been proposed to turn on the ESD protection devices quickly [57]–[59]. The substrate-triggering current is injected into the base of the parasitic BJT in the ESD protection device, which is the substrate or well region in an integrated circuit. Fig. 2.28 shows a low-capacitance ESD protection design utilizing the substrate-triggering technique [60], [61]. During PS-mode ESD stresses, a large current proportional to the transient voltage change flows through the MOS capacitor M2, which can be expressed as

$$I_{M2} = C_{M2} \frac{dv}{dt} \tag{2.9}$$

where I_{M2} is the current flow through the MOS capacitor M_2, and C_{M2} is the capacitance of MOS capacitor M_2. The current I_{M2} boosts the gate potential of M_6, and turns on M_6. With the drain current of M_6 flowing into the bulk of M_1, the voltage across R_{well} rises. When the voltage across R_{well} exceeds the cut-in voltage of the bulk-to-source junction diode (which is the base-emitter junction diode of the parasitic BJT), the parasitic BJT in the multi-finger NMOS M_1 is uniformly turned on to discharge ESD current. M_4 and M_5 are used to prevent M_6 from being turned on under normal circuit operating conditions. R_3 and M_7 form the secondary ESD protection circuit, which clamps the voltage at the I/O pad during ESD stresses. In order to eliminate non-linear capacitive load on the I/O pad under different signal voltages, the diode D_l is added. D_l with a positive coefficient and M_6 and M_7 with negative voltage coefficients can be co-designed to obtain a constant capacitive load on the I/O pad. In this design, the parasitic junction capacitance of M_l is isolated by D_l, so the noise from substrate is significantly reduced. Moreover, adding D_l also reduces capacitive load on the I/O pad because the parasitic capacitances of D_l and M_l are in series configuration.

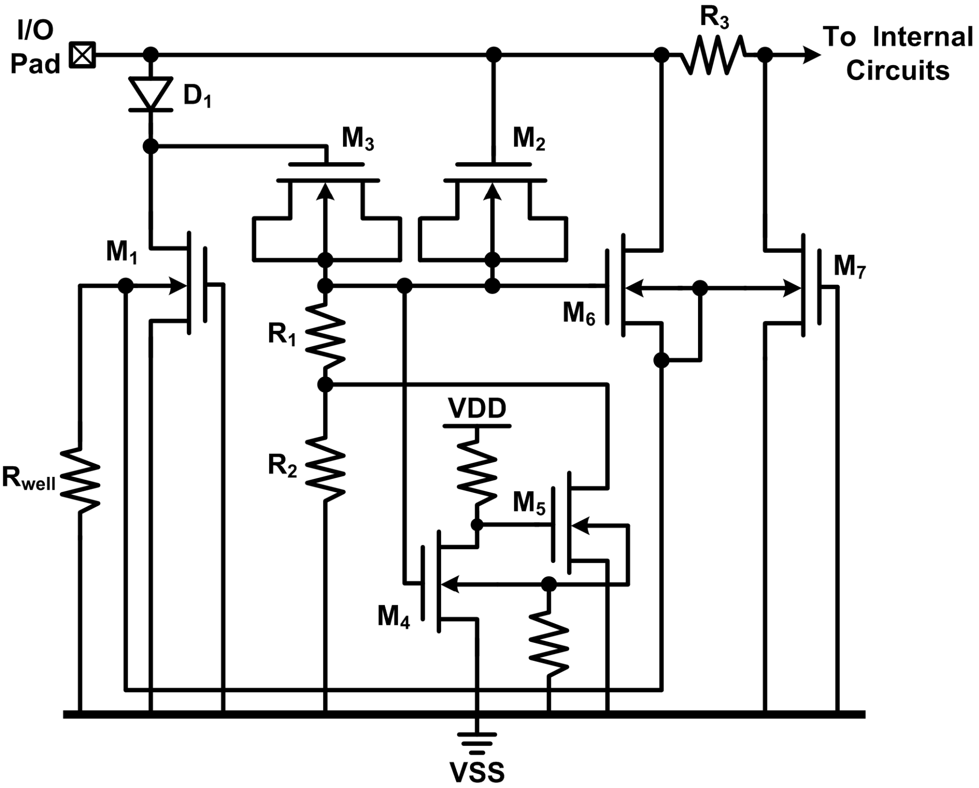


Fig. 2.28. ESD protection design with the substrate-triggering circuit to turn on the ESD protection device.

Apart from substrate-triggered MOSFET, the whole-chip ESD protection circuit with substrate-triggered SCRs had been proposed, as shown in Fig. 2.29 [62]. As mentioned in section 2.2.1, since the ESD protection diodes between the I/O pad and the power-rails are in series configuration, the parasitic capacitance is reduced. Fig. 2.30 shows the equivalent circuit of Fig. 2.29, in which the SCR is replaced by a PNP and a NPN BJT. During PS-mode ESD stresses, D_{P2}, D_{1b}, the base-emitter junction diode of the NPN BJT in SCR_1, and D_{1a} are forward biased, injecting trigger current into the NPN BJT in SCR_1. Consequently, SCR_1 is turned on, and ESD current is bypassed through two current paths. The first ESD path is through D_{P2}, D_{1b}, the base-emitter junction diode of the NPN BJT in SCR_1 and D_{1a}. The second ESD path is through D_{P2}, D_{P1}, SCR_1, and D_{1a}. Similarly, the base-emitter junction

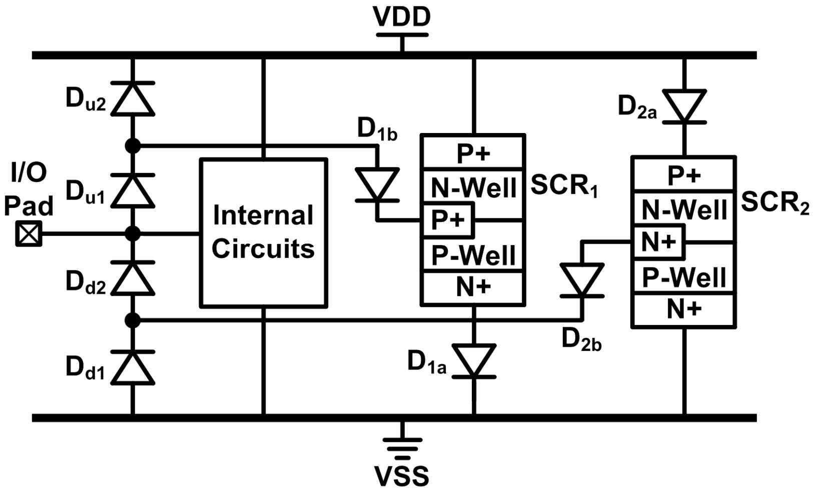


Fig. 2.29. Whole-chip ESD protection scheme with the substrate-triggered SCRs and series diodes.

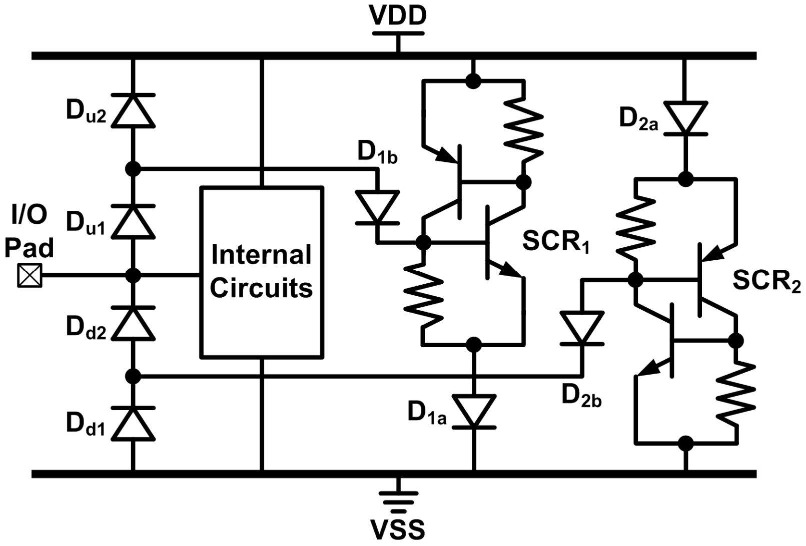


Fig. 2.30. Equivalent circuit of the whole-chip ESD protection scheme of Fig. 2.29.

diode of the PNP BJT in SCR$_2$, D$_{2b}$, and D$_{N1}$ are forward biased during ND-mode ESD stresses, injecting trigger current into the PNP BJT in SCR$_2$. With the turned-on SCR$_2$, two ESD current paths are formed during ND-mode ESD stresses. The first ESD path is through D$_{2a}$, the base-emitter junction diode of PNP BJT in SCR$_2$, D$_{2b}$, and D$_{N1}$. The second ESD path is through D$_{2a}$, SCR$_2$, D$_{N2}$, and D$_{N1}$. When the IC is under VDD-to-VSS ESD stresses, eight forward-biased diodes form the discharge path from VDD to VSS, which includes D$_{2a}$, the base-emitter junction diode of the PNP BJT in SCR$_2$, D$_{2b}$, D$_{N1}$, D$_{P2}$, D$_{1b}$, the base-emitter junction diode of the NPN BJT in SCR$_1$, and D$_{1a}$. If the holding voltage of SCR is lower than the power-supply voltage, diodes (D$_{1a}$ and D$_{2a}$ in this design) can be connected in series with the SCR to increase the holding voltage. Otherwise, lachup issue will exist in this circuit.

2.3. ESD Protection Designs by Layout Solutions

Besides circuit solutions, layout solutions had also been utilized to reduce the parasitic capacitance of ESD protection devices. By utilizing layout solutions, some silicon area might be shared to lower the total chip area. Furthermore, no process modification is needed and the ESD protection scheme does not need to be changed by using layout solutions.

2.3.1. Low-Capacitance Layout Structure for MOSFET

The layout structure for MOSFET with low parasitic capacitance had been proposed [63]. The layout top view is shown in Fig. 2.31. The P-well region is defined between the two dotted rectangles in Fig. 2.31. Fig. 2.32 shows the cross-sectional view of the low-capacitance MOSFET.

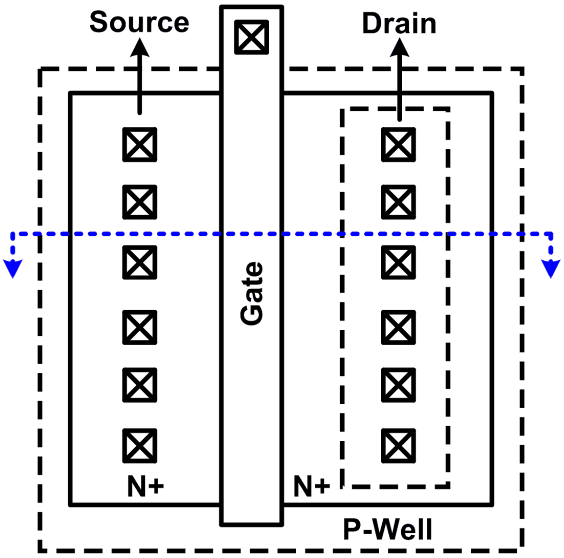


Fig. 2.31. Layout top view of the low-capacitance NMOS transistor.

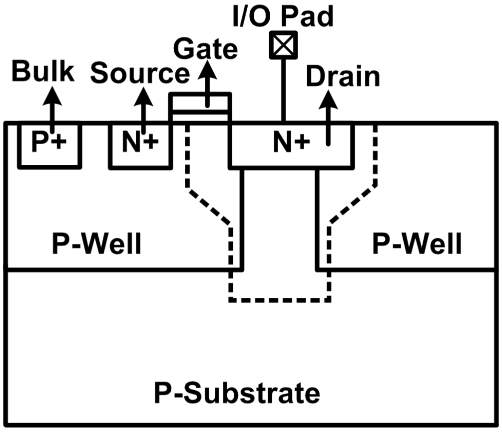
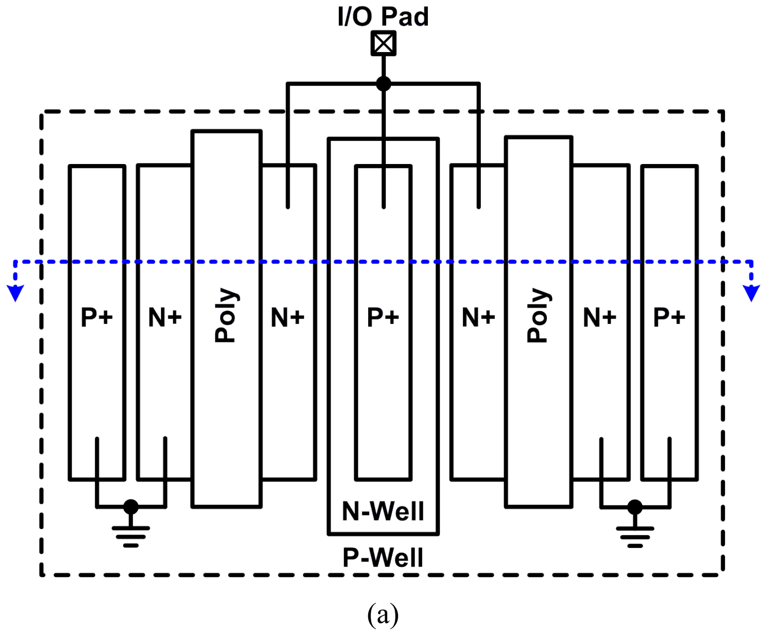


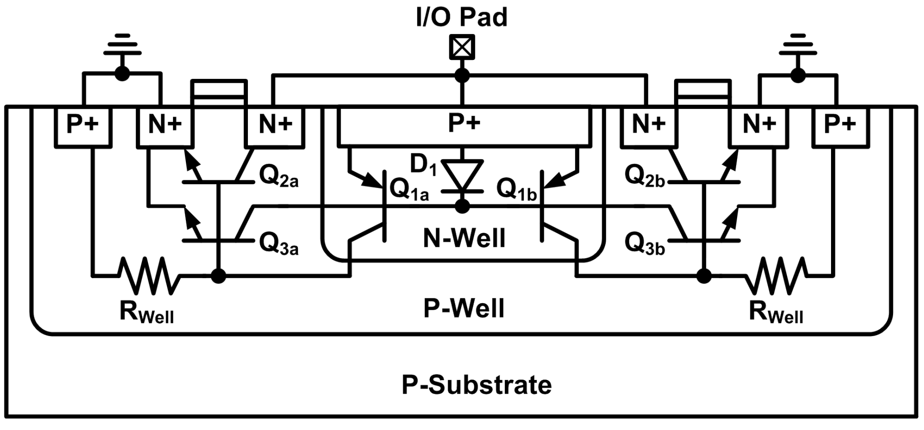
Fig. 2.32. Cross-sectional view of the low-capacitance NMOS transistor.

The dotted line in Fig. 2.32 denotes the depletion region edge of the PN-junction under the drain region. The P-well is designed not to lie below most of the drain area, which is connected to the I/O pad. Since the P-well does not exist under the N+ drain region of the NMOS transistor, the space charge region between the N+ drain diffusion and the P-substrate is larger than that of the N+/P-well junction. Thus, the parasitic capacitance is reduced by eliminating the P-well from existing under the drain region. During ESD stresses, the snapback breakdown occurs in the NMOS transistor, which turns on the parasitic NPN BJT in the NMOS transistor to sink ESD current. Because of the relatively low doping level in the PN-junction, the breakdown voltage of the drain-to-substrate junction is higher than that of the drain-to-well junction, resulting in degraded ESD robustness. Thus, a tradeoff exists between the parasitic capacitance and ESD robustness in this design.

2.3.2. Low-Capacitance Layout Structure for SCR

SCR had been demonstrated to be suitable for ESD protection for high-frequency applications, because it has both high ESD robustness and low parasitic capacitance under a small layout area [64], [65]. Layout structures which can reduce the parasitic capacitance of SCR had been investigated [66]–[69]. The layout top view and cross-sectional view of the low-capacitance SCR proposed in [66]–[68] are shown in Fig. 2.33(a) and (b), respectively. The SCR structure in Fig. 2.33(b) is similar to that of the low-voltage triggering SCR (LVTSCR) [70], [71]. With a low trigger voltage, the LVTSCR can be quickly turned on to protect the internal circuits against ESD damage. During PS-mode ESD stresses, the snapback breakdown occurs in the embedded NMOS, which turns on the parasitic NPN BJTs Q_{2a} and Q_{2b} (formed by the N+ diffusion, P-well, and N+ diffusion) in the embedded NMOS. The current boosts the base voltage of Q_{2a} and Q_{2b} because of the voltage drop across the P-well resistance (R_{Well}). As the voltage across R_{Well} exceeds the cut-in voltage of the base-emitter junction diodes in the parasitic NPN BJTs Q_{3a} and Q_{3b}, which are formed by the N-well, P-well, and N+ diffusion, Q_{3a} and Q_{3b} are turned on. Consequently, Two SCRs composed of Q_{1a} and Q_{3a}, and Q_{1b} and Q_{3b} are turned on to sink ESD current. With some area overhead, the ESD protection capability can be ideally doubled by splitting the current paths. The parasitic capacitance of the SCR primarily comes from the N-well/P-well junction and from the N+ diffusion (drain of the NMOS) to P-well junction. In order to reduce the parasitic capacitance, the shallow-trench isolation (STI) has been utilized in the modified design [69]. As shown in Fig. 2.34, the inserted STI reduces the drain-to-well sidewall area and the N-well-to-P-well boundary area, which leads to reduced parasitic capacitance.





(b)

Fig. 2.33. Low-capacitance SCR: (a) layout top view, and (b) cross-sectional view.

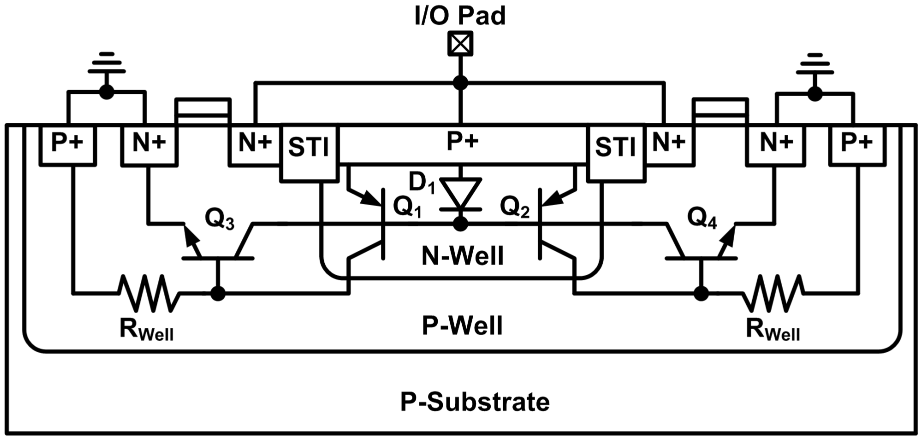
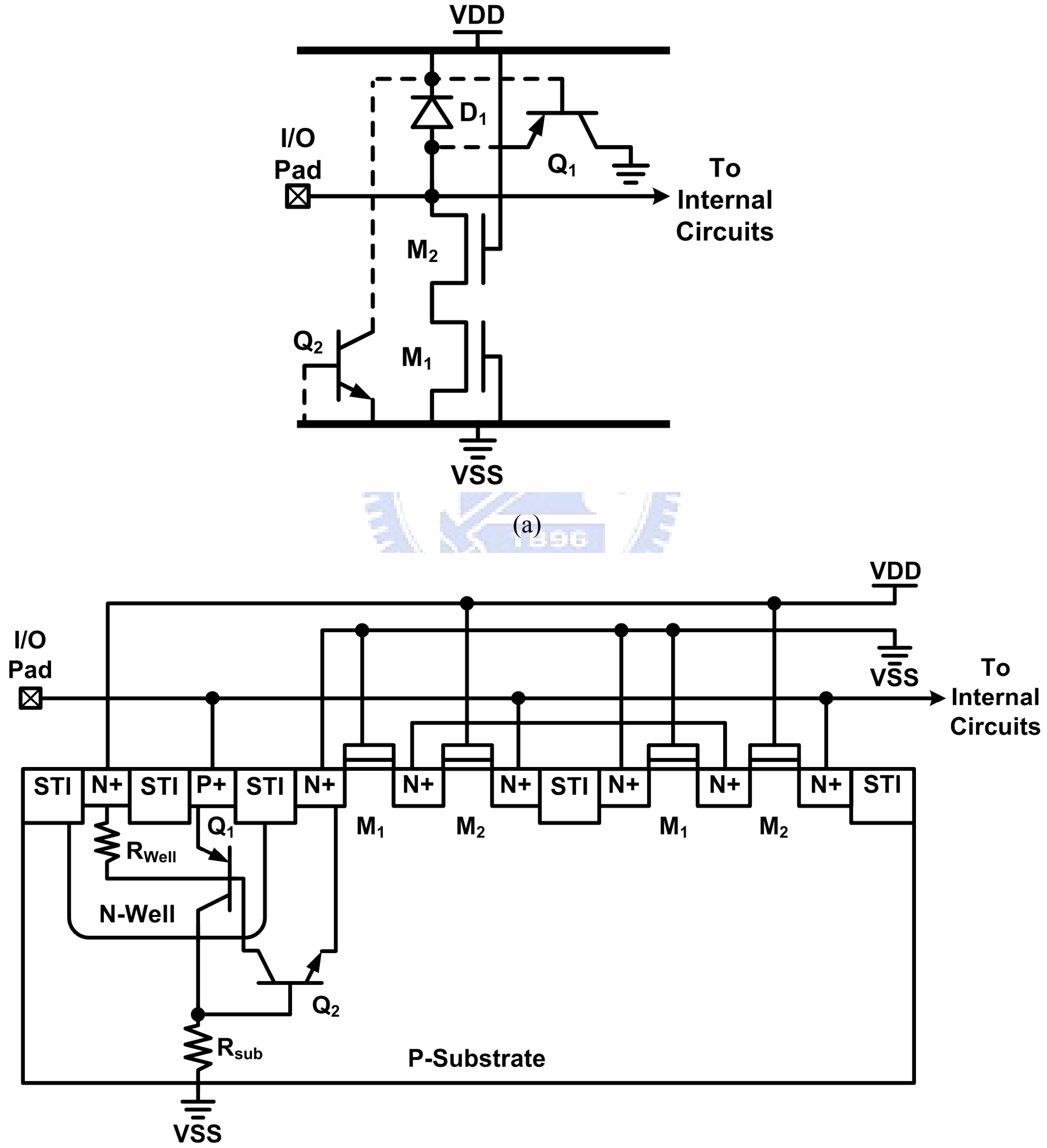


Fig. 2.34. Cross-sectional view of the modified low-capacitance SCR with STI.

Another ESD protection design utilizing the parasitic SCR is shown in Fig. 2.35(a) [72]. The cascoded NMOS transistors M_1 and M_2 are used for mixed-voltage I/O applications, which can receive 2×VDD input signal by using only 1×VDD devices without the gate-oxide reliability issue [73], [74]. The diode D_1 is used to provide ESD current path from the I/O pad to VDD. The cross-sectional view of this ESD protection design is shown in Fig. 2.35(b), where the NMOS transistors M_1 and M_2 are realized with multi-finger structure. The P+



(a)

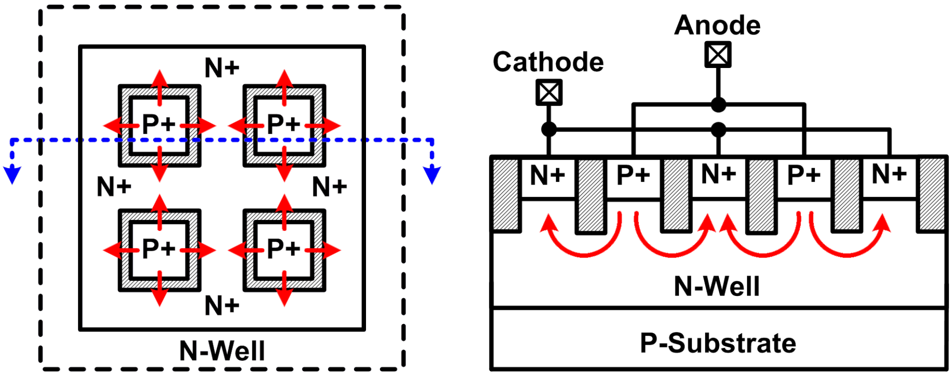
(b)

Fig. 2.35. ESD protection design with a parasitic SCR: (a) circuit schematic, and (b) cross-sectional view.

diffusion, N-well, and P-substrate form the vertical PNP BJT Q_1, and the N-well, P-substrate, and N+ diffusion form the lateral NPN BJT Q_2. In such a layout structure, the P+ diffusion, N-well, P-substrate, and N+ diffusion form the parasitic SCR to provide ESD current path from the I/O pad to VSS. Since the base terminal of Q_1 is biased to VDD, which is the highest potential in the IC, the reverse-biased base-emitter junction capacitance of Q_1 is reduced. Moreover, the emitter, base, and collector and base terminals of Q_2 are connected to the AC ground nodes VDD or VSS. Thus, the parasitic capacitance of Q_2 does not have any impact to the internal circuits.

2.3.3. *Waffle Layout Structure*

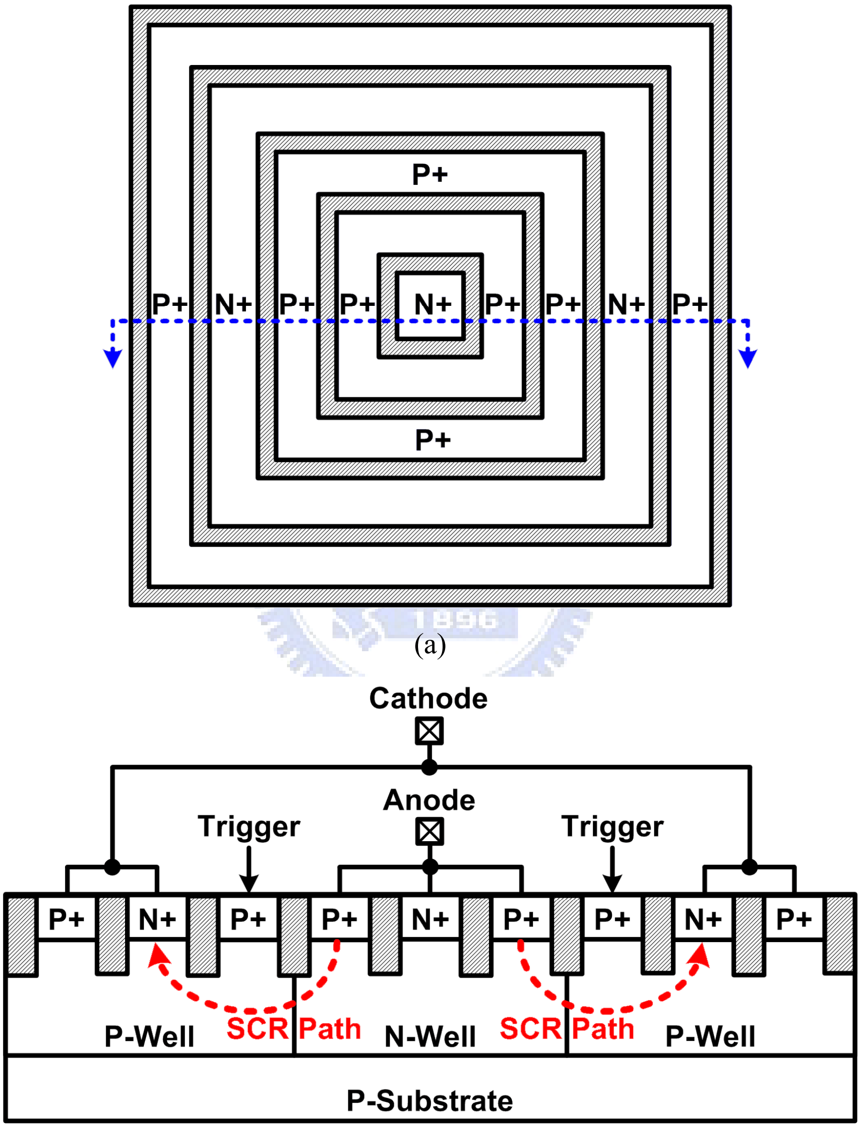
To save the silicon area and reduce the parasitic capacitance, the MOSFETs realized with the waffle structure had been studied [75]. Similarly, the ESD protection devices had been realized with the waffle structure to optimize ESD robustness [76]–[81]. The ESD protection device with the maximum ratio of perimeter to area is preferred, because it has the maximum ratio of ESD robustness to parasitic capacitance. The ESD protection diode realized with the waffle structure had been proposed [77]–[79]. To maximize the ratio of perimeter to area, small square diffusions are used. The layout top view and cross-sectional view of the P+/N-well waffle diode are shown in Fig. 2.36(a) and (b), respectively. The arrows in Fig. 2.36 show the ESD current paths. The P+ diffusion is implemented in the N-well region and surrounded by the N+ diffusion. Thus, ESD current can be discharged through four directions from the P+ diffusion. To scale the ESD protection capability, multiple P+ diffusions can be connected in parallel to form the waffle diode structure. Under the same ESD robustness, the waffle diode has the reduced parasitic capacitance than that of the traditional ESD diode.



(a) (b)

Fig. 2.36. P+/N-well waffle diode: (a) layout top view, and (b) cross-sectional view.

Besides waffle diodes, SCR with waffle layout structure had been reported [80], [81]. The layout top view and cross-sectional view of the substrate-triggered SCR are shown in Fig. 2.37(a) and (b), respectively. Compared with the waffle diode, the layout of waffle SCR is more complicated, especially the metal routing with multiple waffle SCRs in parallel. It had been verified that the waffle SCR can achieve smaller parasitic capacitance under the same ESD robustness.



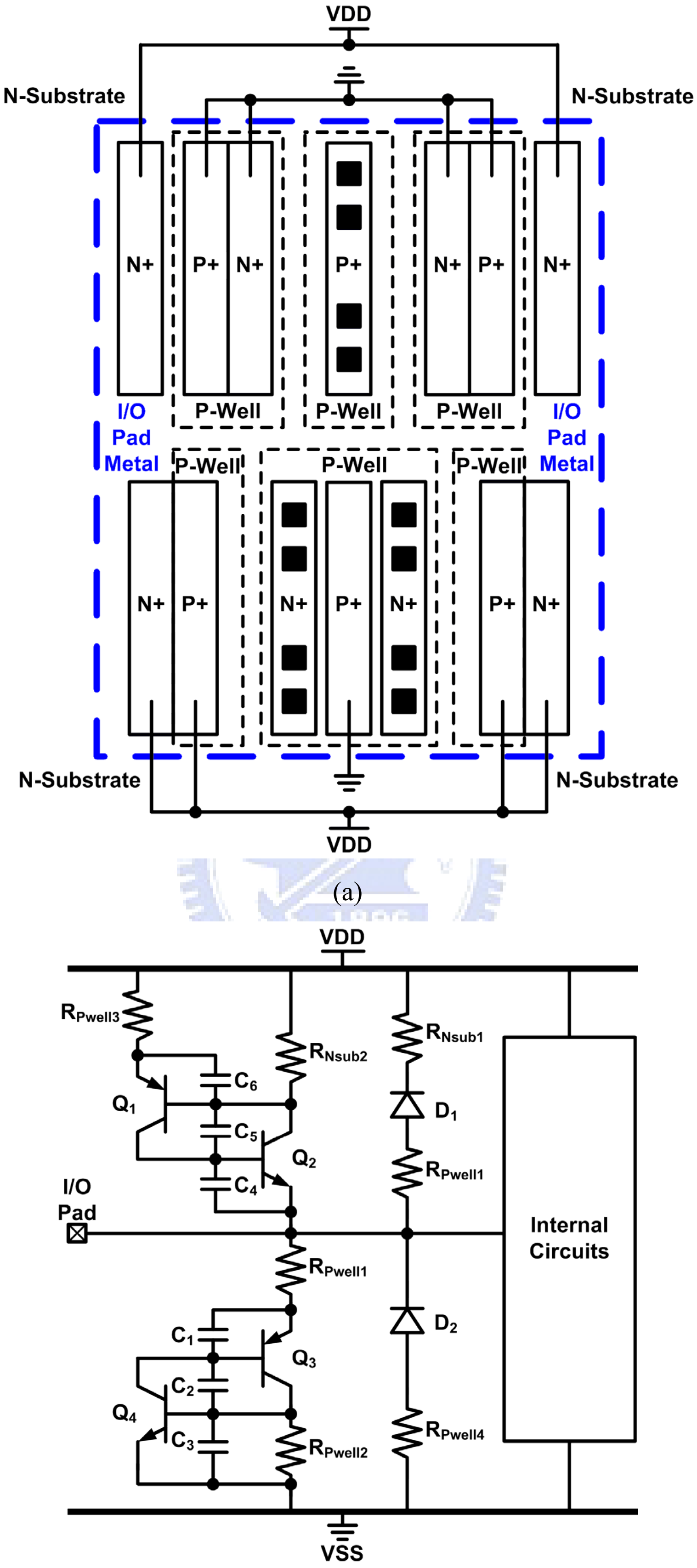
(a)

(b)

Fig. 2.37. Waffle SCR: (a) layout top view, and (b) cross-sectional view.

2.3.4. ESD Protection Device Under I/O Pad

To reduce the chip area, ESD protection devices can be placed under the I/O pad, as shown in Fig. 2.38(a) [82]. The contacts in Fig. 2.38(a) connect the diffusion regions to the



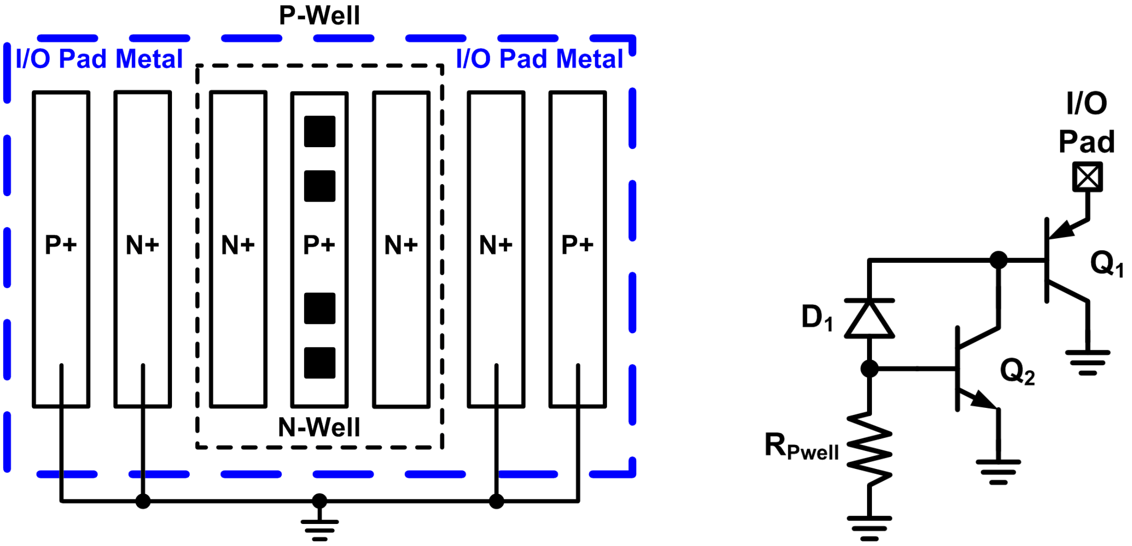
(a)

(b)

Fig. 2.38. ESD protection device under the I/O pad proposed in [82]: (a) layout top view, and (b) schematic circuit diagram.

I/O pad. Fig. 2.38(b) illustrates the schematic circuit diagram. The parasitic diodes D_1 and D_2 provide ESD current paths during PD- and NS-mode ESD stresses, respectively. During PS-mode ESD stresses, the BJT Q_3 is turned on when breakdown occurs in the reverse-biased base-collector junction. After Q_3 is turned on, the SCR formed by Q_3 and Q_4 is turned on to discharge ESD current. Similarly, the SCR composed of Q_1 and Q_2 is turned on during ND-mode ESD stresses to provide ESD protection. With the ESD protection circuit under the bond pad, the parasitic capacitances of the bond pad and ESD protection circuit are series connected from the I/O pad to substrate, resulting in reduced equivalent parasitic capacitance. Thus, the total parasitic capacitance of the I/O pad and ESD protection circuit is reduced, as compared with the ESD protection device placed beside the I/O pad.

Another ESD protection circuit under the bond pad had been proposed, with its layout top view shown in Fig. 2.39(a) [83]. Fig. 2.39(b) shows the schematic circuit diagram. The diode D_1 is formed by the P-well/N-well junction. The PNP BJT Q_1 is formed by the P+ diffusion, N-well and P-well, and the NPN BJT Q_2 is formed by the N-well, P-well, and N+ diffusion. Q_1 and Q_2 form an SCR from the I/O pad to VSS. During PS-mode ESD stresses, the junction breakdown occurs in D_1, which turns on the SCR to discharge ESD current. The parasitic capacitance connected to the I/O pad is only the P+/N-well junction capacitance, which is the base-emitter junction capacitance of Q_1. Moreover, the parasitic capacitance from the I/O pad to the grounded P-well region is reduced because the ESD protection circuit is placed under the bond pad.



(a) (b)

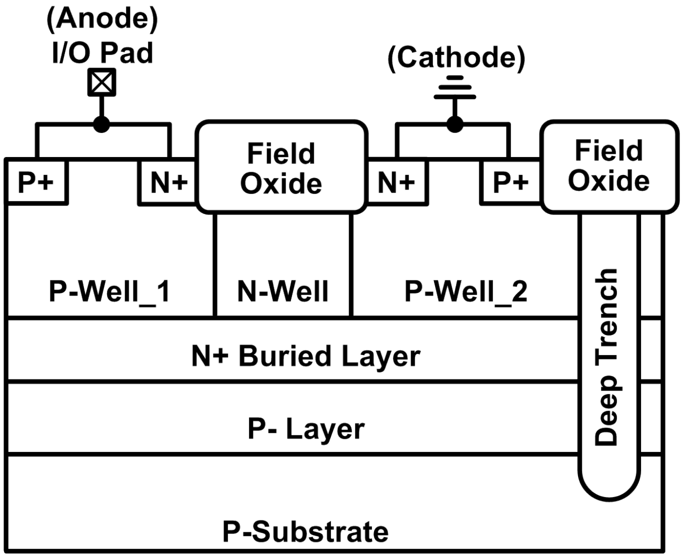
Fig. 2.39. ESD protection device under the I/O pad proposed in [83]: (a) layout top view, and (b) schematic circuit diagram.

2.4. ESD Protection Designs by Process Solutions

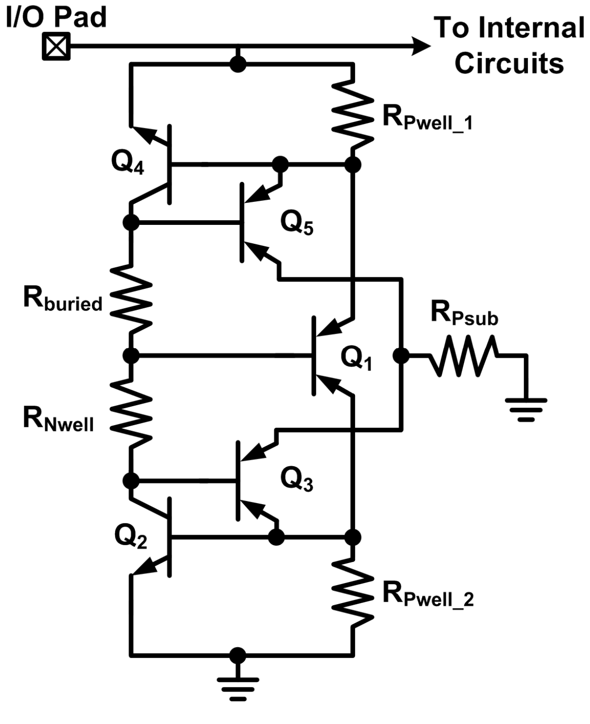
The third approach to reduce the parasitic capacitance from the ESD protection device is to modify the fabrication process. Besides standard CMOS processes, ESD protection devices fabricated in some modified processes had been reported to reduce the parasitic capacitance. However, chip fabrication cost will be increased because of process modification.

2.4.1. Symmetrical SCR Structure

Fig. 2.40(a) shows the cross-sectional view of a symmetrical SCR structure in the process with the N+ buried layer and P- layer [84]. With the high-concentration N+ buried layer, the clamping voltage of the SCR is reduced, which leads to more efficient ESD protection. Moreover, the deep-trench isolation separates the symmetrical SCR structure from the internal circuits, which is beneficial for latchup prevention. In the ESD protection device, the anode and cathode sides are junction-isolated, which reduces the parasitic capacitance. The overall reduction in parasitic capacitance is due to its smaller junction area and the series-connected parasitic capacitances of the two P-well/N+ buried layer junctions. Fig. 2.40(b) shows the schematic circuit diagram of this ESD protection device, in which the anode is connect to the I/O pad, and the cathode is connected to VSS. P-Well_1, N+ buried layer, P-Well_2, and N+ diffusion form the first SCR from anode to cathode. P-Well_2, N+ buried layer, P-Well_1, and N+ diffusion form the second SCR from cathode to anode. The N+ diffusion which is connected to anode, P-Well_1, and N+ buried layer form the NPN BJT Q_4. The N+ diffusion which is connected to cathode, P-well_2, and N+ buried layer form the NPN BJT Q_2. The N+ buried layer and N-well form the base of the BJT Q_1, and the P-Well_1 and P-Well_2 form the emitter and collector of the BJT Q_1, respectively. The first vertical BJT Q_5 is formed by the P- layer, N+ buried layer, and P-Well_1. The second vertical BJT Q_3 is formed by the P- layer, N+ buried layer, and P-Well_2. During PS-mode ESD stresses, The avalanche breakdown occurs at the N+ buried layer/ P-Well_2 junction in Q_1, increasing current through Q_1. As current flows through the parasitic resistance in P-Well_2 (R_{Pwell_2}), the voltage across the base-emitter junction of Q2 increases. When the voltage across the base-emitter junction of Q_2 exceeds its cut-in voltage, Q_2 is turned on, and the SCR composed of Q_1 and Q_2 is turned on to sink ESD current. Similarly, the SCR composed of Q_1 and Q_4 is turned on to sink ESD current during NS-mode ESD stresses.



(a)



(b)

Fig. 2.40. ESD protection device with symmetrical SCR: (a) cross-sectional view, and (b) schematic circuit diagram.

2.4.2. Low-Capacitance MOSFET

In section 2.3.1, it has been mentioned that the parasitic capacitance can be reduced by lowering the concentration of the PN-junction. The similar idea using an extra mask to lower the concentration at the drain-to-well junction had been proposed [85]. The cross-sectional view of the low-capacitance PMOS transistor is shown in Fig. 2.41. The drain and source regions are surrounded by the lightly-doped P-type (P-) regions. The N- region under the drain is counter-doped with P-type material to reduce the effective N-type concentration. Since the depletion region of the P+/N- junction is larger than that of the P+/N-well junction, the parasitic capacitance is reduced.

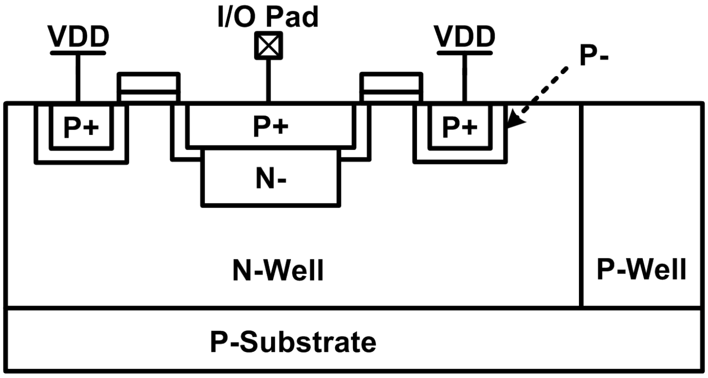


Fig. 2.41. Cross-sectional view of the low-capacitance PMOS proposed in [85].

2.5. Discussion and Comparison

The comparison among various ESD protection designs for RF front-end circuits and high-speed I/O interface circuits is summarized in Table 2.1. The evaluated parameters are explained as following.

- Design Complexity:
  - "Low": The stand-alone ESD protection device is the ESD protection circuit without extra auxiliary component.
  - "Moderate": The stand-alone ESD protection device is the ESD protection circuit without extra auxiliary component, but the layout of the ESD protection device needs careful consideration.
  - "High": Besides the ESD protection device, extra auxiliary components are needed, and the auxiliary components should be carefully designed.
- Parasitic Capacitance:
  - "Small": The parasitic capacitance of the ESD protection circuit at the I/O pad can be very small with proper design.
  - "Moderate": The parasitic capacitance of the ESD protection circuit at the I/O pad is moderate for high-frequency applications.

  - “Large”: The parasitic capacitance of the ESD protection circuit at the I/O pad is large for high-frequency applications.
- ESD Robustness:
  - “Poor”: ESD robustness of the ESD protection design is poor.
  - “Moderate”: ESD robustness of the ESD protection design is moderate.
  - “Good”: ESD robustness of the ESD protection design is good.
  - “Adjustable”: For some ESD protection designs by circuit solutions, ESD robustness can be adjusted by using different ESD protection devices and dimensions.
- Area Efficiency:
  - “Poor”: The area efficiency of the ESD protection design is poor.
  - “Moderate”: The area efficiency of the ESD protection design is moderate.
  - “Good”: The area efficiency of the ESD protection design is good.

Table 2.1

Comparison Among the ESD Protection Designs for RF Front-End Circuits and High-Speed I/O Interface Circuits

ESD Protection Design		Design Complexity	Parasitic Capacitance	ESD Robustness	Area Efficiency
Circuit Solutions	**Stacked ESD Protection Devices**	**Low**	**Moderate**	**Moderate**	**Good**
	Impedance Cancellation Technique	**High**	**Small**	**Adjustable**	**Poor**
	Impedance Isolation Technique	**High**	**Small**	**Adjustable**	**Poor**
	Series LC Resonator	**High**	**Small**	**Adjustable**	**Poor**
	Impedance Matching	**High**	**Small**	**Adjustable**	**Poor**
	Inductive ESD Protection	**High**	**Small**	**Moderate**	**Poor**
	T-Coil	**High**	**Small**	**Adjustable**	**Poor**
	Distributed ESD Protection	**High**	**Small**	**Moderate**	**Poor**
	Biasing Technique	**Low**	**Large**	**Poor**	**Moderate**
	Substrate-Triggering Technique	**High**	**Moderate**	**Moderate**	**Good**
Layout Solutions	**Low-C Layout Structure for MOSFET**	**Moderate**	**Large**	**Poor**	**Moderate**
	Low-C Layout Structure for SCR	**Moderate**	**Moderate**	**Good**	**Good**
	Waffle Layout Structure	**Moderate**	**Moderate**	**Moderate**	**Good**
	ESD Protection Device Under I/O Pad	**Moderate**	**Moderate**	**Moderate**	**Good**
Process Solutions	**Symmetrical SCR Structure**	**Low**	**Small**	**Good**	**Good**
	Low-C MOSFET	**Low**	**Moderate**	**Poor**	**Moderate**

According to Table 2.1, most of the reported ESD protection designs utilize circuit solutions to mitigate the impacts caused by the ESD protection circuit. By utilizing the circuit solutions, the ESD protection device can be realized with large device dimensions to achieve good ESD robustness, because the parasitic capacitance from the ESD protection device can be compensated or cancelled. However, circuit solutions often need additional components. As a result, the chip area is substantially increased, which in turn increases the fabrication cost. Moreover, characteristics of the ESD protection device and the additional components need to be carefully investigated to minimize the undesired effects.

Among the ESD protection devices, SCR is a promising device because it has both good ESD robustness and low parasitic capacitance under a small layout area. Besides, the holding voltage and turn-on resistance of SCR are quite low. As the power-supply voltage of ICs decreases to be less than SCR's holding voltage, the latchup issue is avoided. These factors reveal the advantages of SCR devices. With suitable trigger circuit to enhance the turn-on speed and to reduce the trigger voltage, SCR could be the most promising component in the ESD protection design for high-frequency applications in the future.

2.6. Summary

In this chapter, a comprehensive overview on the reported works in the field of ESD protection design for RF front-end circuits and high-speed I/O interface circuits has been presented. The requirements on ESD protection design for high-frequency I/O applications include low parasitic capacitance, low loss, and high ESD robustness. To optimize both high-frequency circuit performance and ESD robustness simultaneously, the undesired parasitic effects from ESD protection devices must be minimized or cancelled. Furthermore, the ESD protection circuits and RF front-end circuits should be co-designed to achieve both good circuit performance and high ESD robustness. As the operating frequencies of RF front-end circuits and high-speed I/O interfaces are further increased, on-chip ESD protection design for high-speed/high-frequency I/O applications will continuously be an important design task.

Chapter 3

Ultra Low-Capacitance Bond Pad for Radio-Frequency Applications in CMOS Technology

In this chapter, an ultra low-capacitance bond pad for gigahertz (radio-frequency) RF applications is proposed and verified in a 130-nm CMOS process. Three kinds of on-chip stacked inductors embedded under the bond-pad metal plate are used to compensate bond-pad capacitance. Experimental results have verified that the bond-pad capacitance can be significantly reduced in a specific frequency band due to the cancellation effect provided by the embedded inductor in the proposed bond pad. The proposed bond pad is fully compatible to general CMOS processes without any process modification [86], [87].

3.1. Background

With the advantages of high integration capability and low cost for mass production, radio-frequency integrated circuits (RF ICs) operating in gigahertz frequency bands have been widely implemented in CMOS technology. However, the undesired parasitic capacitances at the I/O pads of silicon chips often limit the high-frequency performance of RFICs. To mitigate the RF performance degradation caused by the I/O pad, bond-pad capacitance should be minimized first. Moreover, on-chip electrostatic discharge (ESD) protection devices are also placed around the I/O pads, which further decrease the design budget because of the extra parasitic capacitance from the ESD protection devices [10]. Although the evolution of CMOS technology enables the device dimensions to shrink substantially, the bond pad size is still kept at a large enough size to ensure the bonding reliability. Therefore, the parasitic capacitance resulted from the bond-pad metal plate and the overlapped substrate can not be reduced with the evolution of CMOS technology. In some CMOS integrated RF front-end circuits, the bond-pad capacitance can be incorporated as a part of the matching network. Recently, several techniques had been reported to reduce the bond-pad capacitance [88]–[90]. A bond pad structure realized with special layout patterns, which have smaller overlapped area between different metal layers and additional diffusion layers, had been demonstrated to have smaller bond-pad capacitance [88]. Another bond pad structure using the depletion-insulation structure to improve cross-talk isolation and quality factor had been presented [89]. Besides, a bond pad structure realized with semi-insulating porous silicon had been reported to reduce the bond-pad capacitance [90].

In this chapter, a new bond pad structure with embedded inductor is proposed to reduce the equivalent bond-pad capacitance. Verified in a 130-nm CMOS process, the proposed bond pad structure possesses several features. First, it is fully compatible to standard CMOS processes without any extra process modification. Second, the proposed bond pad has exactly the same dimensions as that of the traditional bond pad without any extra area consumption. Third, the proposed bond pad has much lower parasitic capacitance than that of the traditional bond pad, which is suitable for gigahertz RF applications. The proposed low-capacitance bond pad and its equivalent circuit model are presented in Sections 3.2 and 3.3, respectively. The experimental results among the fabricated bond pads and discussion are presented in Section 3.4.

3.2. Proposed Ultra Low-Capacitance Bond Pad

In this chapter, a 130-nm one-poly eight-metal (1P8M) CMOS process is used. The typical bond pad provided by the foundry is implemented with eight metal layers (from metal 1 to metal 8). Since the parasitic capacitance between the bottom metal layer (metal 1) and the overlapped substrate is too large for gigahertz RF applications, the lower metal layers were often removed from the bond pad to reduce the bond-pad capacitance in some RF ICs. Smaller bond-pad capacitance can be achieved by removing more metal layers within the bond pad. However, using only the top metal layer (metal 8) to implement bond pads causes some concerns in bonding reliability. To compromise the dilemma between bond-pad capacitance and bonding reliability, the reference bond pad used in this chapter for comparison is realized with only the top three metal layers, which are metals 8, 7, and 6 in the 130-nm CMOS process.

In the proposed bond pad structure, a stacked spiral inductor is embedded between the bond-pad metal plate and the overlapped substrate. The embedded inductor is implemented within the region of the bond-pad metal plate. The reference bond pad, the proposed bond pad with the one-layer inductor (implemented with metal 5), the three-layer stacked inductor (implemented with metals 5, 4, and 3), and the five-layer stacked inductor (implemented with metals 5, 4, 3, 2, and 1) are illustrated in Fig. 3.1(a)–(d), respectively. In the proposed bond

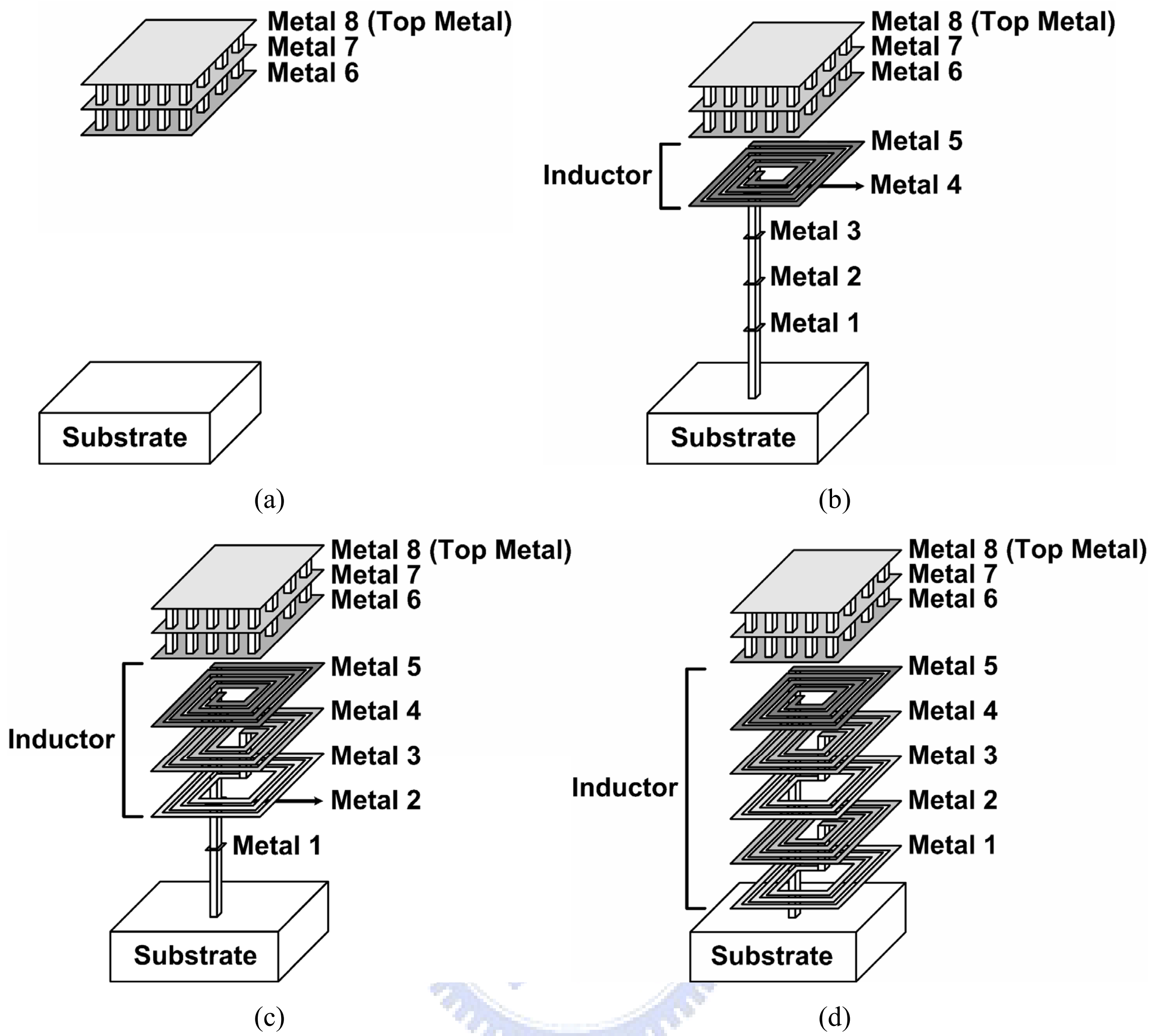


Fig. 3.1. (a) Reference bond pad. (b) Proposed bond pad with the 1-layer inductor. (c) Proposed bond pad with the 3-layer stacked inductor. (d) Proposed bond pad with the 5-layer stacked inductor.

pad structure, the on-chip stacked inductor [91] is embedded under the metal plates of the reference bond pad, which are metals 8, 7, and 6. In the stacked inductor, the metal tracks in different metal layers were wound in the same direction. Since the on-chip stacked inductor is implemented within the region of the metal plate of the reference bond pad, the proposed bond pad occupies exactly the same chip area as the reference one, which is 70 μm × 57 μm in this work. The bond pads with three kinds of inductors, which are one-layer inductor, three-layer stacked inductor, and five-layer stacked inductor, have been designed in the experimental test chip to investigate capacitance reduction. Since the area of the embedded inductor is limited, the dimensions of the embedded inductor are somewhat reduced. The inductors are realized with the metal-track width of 4 μm, metal-track spacing of 1 μm, and 5 turns. The inductor designed in such architecture is used to increase the inductance within the pre-specified region (the region of the reference bond pad) to cancel the bond-pad capacitance resulted from the metal plate and the overlapped substrate.

Fig. 3.2 is the basic circuit schematic of the proposed bond pad structure, which can be used to illustrate the idea of bond-pad capacitance cancellation. C_P denotes the parasitic capacitance between the bond-pad metal plate and the overlapped substrate, and L_S denotes the embedded inductance. L_S is designed to resonate with C_P at the desired frequency band. L_S can not be directly connected to the bond-pad metal plate because it is a short path at dc. If L_S is directly connected to the bond-pad metal plate, the DC component at the bond pad will be lost. Therefore, an extra capacitor C_C is need between L_S and the bond-pad metal plate. The Y-parameter from the top bond-pad metal plate to ground can be derived to obtain the equivalent bond-pad capacitance (C_{eq}) of the proposed structure:

$$Y = j\omega C_P + \left(\frac{\dfrac{C_C}{L_S}}{j\omega C_C + \dfrac{1}{j\omega L_S}} \right) = j\omega C_{eq} \tag{3.1}$$

where ω is the angular frequency. C_{eq} is then given by

$$C_{eq} = \frac{L_S - \dfrac{1}{\omega^2 C_P} - \dfrac{1}{\omega^2 C_C}}{\dfrac{L_S}{C_P} - \dfrac{1}{\omega^2 C_P C_C}} . \tag{3.2}$$

When ω approaches the resonant frequency, namely

$$\omega \to \sqrt{\frac{1}{L_S}\left(\frac{1}{C_P} + \frac{1}{C_C}\right)} , \tag{3.3}$$

C_{eq} becomes very small, which is ideally zero and given by

$$C_{eq} \to \frac{0}{\dfrac{L_S}{C_P} - \dfrac{L_S}{C_P + C_C}} = 0 . \tag{3.4}$$

This derivation explains the effectiveness of bond-pad capacitance cancellation in the proposed structure. This is just a basic analysis. Besides the components shown in Fig. 3.2, there are some extra parasitic effects in the fabricated bond pad structure, which will be addressed in the following section.

Fig. 3.3 shows the layout top view of the test pattern used to extract the bond-pad capacitance. The layout pattern of ground-signal-ground (G-S-G) pads with 150-μm pitch was adopted to facilitate on-wafer two-port S-parameter measurement. The guard ring is implemented to encircle the proposed bond pad and connected to a signal pad for measurement. With the guard ring connected to the substrate, the equivalent bond-pad capacitance between the bond-pad top metal plate and substrate can be characterized. The guard ring is implemented for measurement purpose, and it is not necessary when the proposed bond pad is used for applications. Besides the three proposed bond pads, the reference bond pad is also fabricated to compare their bond-pad capacitances.

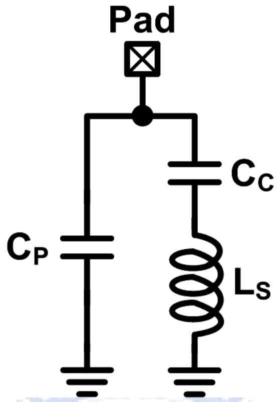


Fig. 3.2. Basic circuit schematic to illustrate the idea of bond-pad capacitance cancellation.

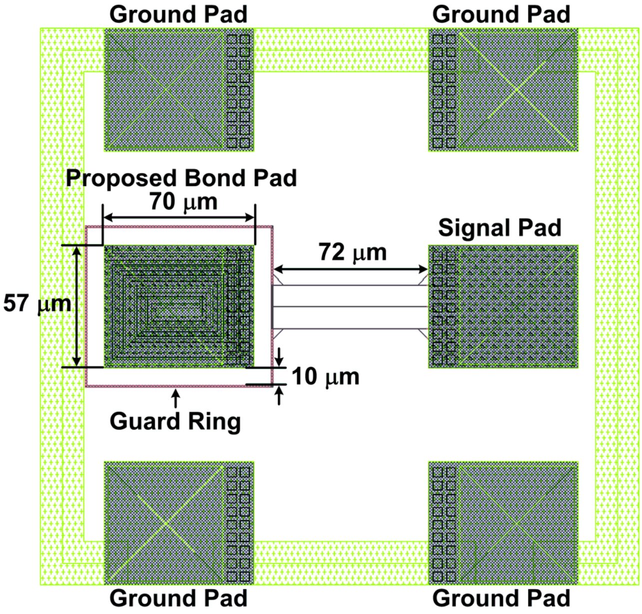


Fig. 3.3. Layout top view of the test pattern to extract the bond-pad capacitance.

3.3. Equivalent Circuit Model for the Proposed Bond Pad

In order to acquire the characteristics of the proposed bond pad in the circuit design phase, the equivalent circuit model for the proposed bond pad has been developed, as shown in Fig. 3.4. The equivalent circuit model for the proposed bond pad consists of three parts, which are the parasitic capacitance between the bond-pad metal plate and the overlapped substrate (C_P in Fig. 3.2), the coupling effect between the metal plate and the stacked inductor (C_C in Fig. 3.2), and the stacked inductor model (L_S in Fig. 3.2). Besides the desired components, the parasitic effects also exist, which also need to be taken into account. In the first part, C_P includes the parasitic capacitance between the bottom bond-pad metal plate and the overlapped substrate, as well as the fringing capacitance between the sidewall of the bond-pad metal plate and the substrate. In the second part, C_{C1}, C_{C2}, R_1, and R_2 denote the coupling effect between the bond-pad metal plate and the stacked inductor. The third part is the stacked inductor model. C_F denotes the parasitic capacitance between the metal layers in the stacked inductor. L_S and R_S are the inductance and parasitic series resistance of the stacked inductor, respectively. C_{ox1} and C_{ox2} represent the parasitic capacitances between the stacked inductor and the substrate. C_{SUB} and R_{SUB} denote the parasitic capacitance and parasitic resistance of the substrate, respectively. With the equivalent circuit model for the proposed bond pad, the high-frequency characteristics of the proposed bond pad can be obtained and adjusted by simulation.

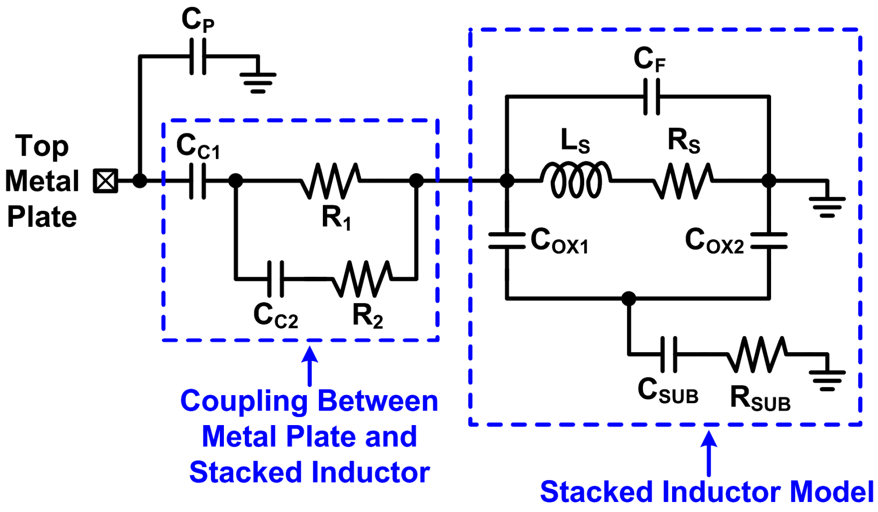


Fig. 3.4. Equivalent circuit model for the proposed bond pad.

3.4. Experimental Results and Discussion

The proposed bond pads with the one-, three-, and five-layer stacked inductors, as well as the reference bond pad, were fabricated in the same silicon chip in a 130-nm CMOS process. The two-port S-parameters of the fabricated bond pads were characterized by on-wafer measurement with the Cascade Air Coplanar G-S-G microwave probes and the

Agilent 8510C network analyzer.

3.4.1. Extracted Bond-Pad Capacitance

The connection in two-port S-parameter measurement is shown in Fig. 3.5. Port 1 and port 2 of the network analyzer were connected to the proposed bond pad/reference bond pad and the signal pad in Fig. 3.3, respectively. After measuring the two-port S-parameters, the Y_{11}-parameter can be obtained by the following equation [92].

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{Z_0\left[(1+S_{11})(1+S_{22})-S_{12}S_{21}\right]} \tag{3.5}$$

where Z_0 is the termination resistance and is 50 Ω. With the conversion between two-port S-parameters and Y-parameters, the bond-pad capacitance (C_{pad}) was extracted as

$$C_{pad} = \frac{\mathrm{Im}(Y_{11})}{\omega} = \frac{\mathrm{Im}(Y_{11})}{2\pi f} \tag{3.6}$$

where Y_{11}-parameter is the admittance seen from port 1 with port 2 grounded.

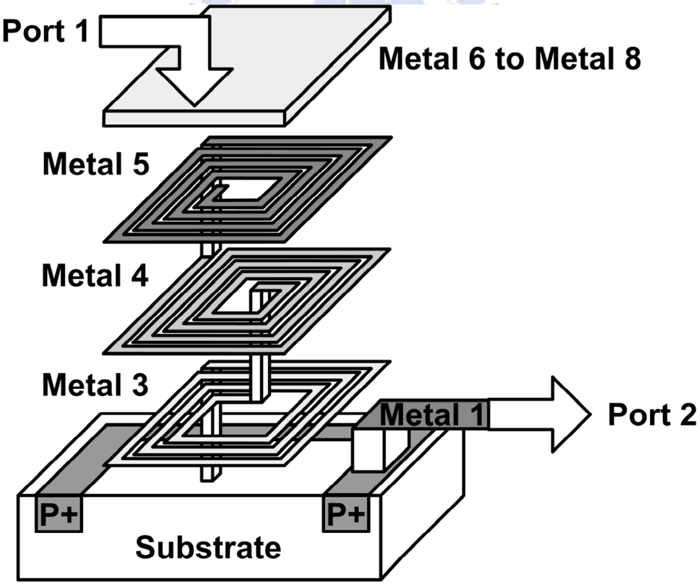


Fig. 3.5. Two-port S-parameter measurement setup.

Fig. 3.6 shows the extracted bond-pad capacitances among the fabricated bond pads under different frequencies. As shown in Fig. 3.6, the reduction of the bond-pad capacitance is more significant when the stacked inductor with larger inductance is embedded in the proposed bond pad. With a five-layer stacked inductor in the proposed bond pad, the bond-pad capacitance can be even reduced to almost 0 fF in the frequency band of 4.3 to 4.8 GHz. The bond-pad capacitance is reduced due to the positive reactance contributed from the embedded inductor. For example, the bond-pad capacitance of the proposed structure with one-, three-, and five-layer stacked inductors can be reduced by 2.9%, 58.9%, and 49.3% from the original value (the reference pad) at 6.5 GHz, respectively. The frequency band in which the bond-pad capacitance is reduced can be adjusted or extended by designing the embedded inductor. With larger inductance embedded in the proposed bond pad structure, the frequency band in which the bond-pad capacitance is reduced becomes lower. Since the guard ring near the proposed bond pad is not necessary in practical applications, the substrate resistance will be larger when the proposed bond pad is used without the guard ring in practical applications. Thus, the bandwidth in which the bond-pad capacitance is reduced will be slightly larger due to the lower quality factor.

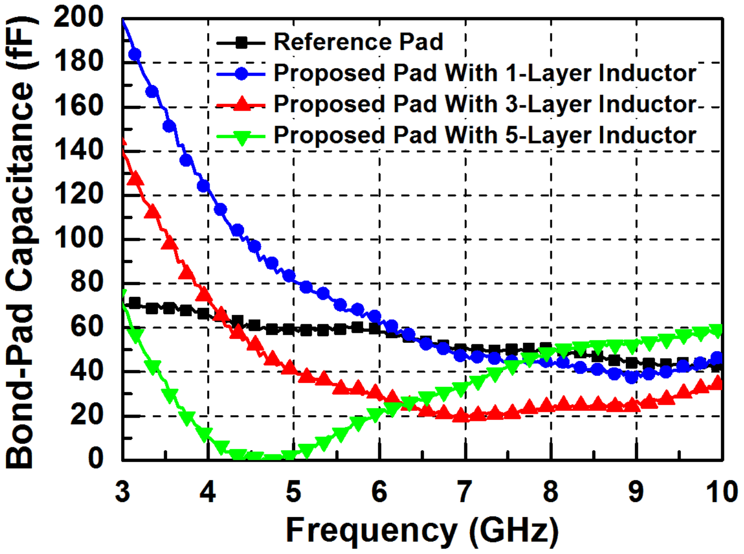


Fig. 3.6. Extracted bond-pad capacitances among the fabricated bond pads under different frequencies.

3.4.2. *Extracted Bond-Pad Insertion Loss*

Besides bond-pad capacitance, the bond-pad insertion loss is another important metric because it identifies the loss when the signal passes through the bond pad. Fig. 3.7 illustrates the insertion loss caused by the bond pad. To extract the bond-pad insertion loss, the *ABCD* matrix of the two-port network is utilized. As shown in Fig. 3.8, the *ABCD* matrix is defined for a two-port network in terms of the total voltages and currents by the following relations [92]:

$$V_1 = AV_2 + BI_2 \tag{3.7}$$

$$I_1 = CV_2 + DI_2 \tag{3.8}$$

or in the matrix form as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}. \tag{3.9}$$

One of the basic two-port networks shown in Fig. 3.9 is identical to that shown in Fig. 3.7. Therefore, the *ABCD* matrix of Fig. 3.9, which is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y_{11} & 1 \end{bmatrix}, \tag{3.10}$$

can be used to extract the bond-pad insertion loss. The bond-pad insertion loss is the S_{21}-parameter of the two-port shown in Fig. 3.9. With the Y_{11}-parameter converted from the measured S-parameters, the bond-pad insertion loss is given by

$$Insertion\ Loss = \frac{2}{A + \dfrac{B}{Z_0} + CZ_0 + D} = \frac{2}{1 + \dfrac{0}{Z_0} + Y_{11}Z_0 + 1} = \frac{2}{2 + Y_{11}Z_0}. \tag{3.11}$$

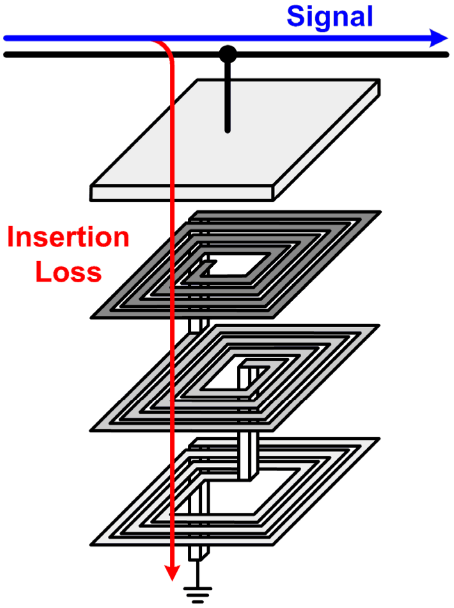


Fig. 3.7. Diagram to shown the bond-pad insertion loss.

The extracted insertion losses of the fabricated bond pads under different frequencies are shown in Fig. 3.10. Since the impedance of the five-layer stacked inductor is higher than those of the one- and three-layer stacked inductors due to the larger inductance, the proposed bond pad with the five-layer stacked inductor has the least loss, while the proposed bond pad with the one-layer inductor has the most insertion loss among the three proposed bond pads. From 3 to 10 GHz, the proposed bond pad with the five-layer stacked inductor has the loss of less than 0.65 dB. The insertion loss of the reference bond pad is less than 0.1 dB up to 10 GHz. Since the embedded inductor was connected to the substrate in the proposed bond pad structure, the proposed bond pads have more insertion loss than that of the reference bond pad. However, since all I/O pads need to be accompanied with ESD protection circuits, the insertion loss of the proposed bond pad will not be the critical part at the input or output nodes because of the larger signal loss caused by the on-chip ESD protection devices.

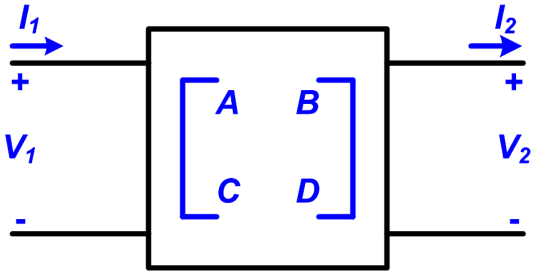


Fig. 3.8. Two-port network represented by the *ABCD* matrix.

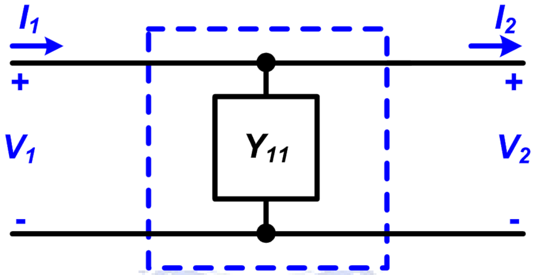


Fig. 3.9. The basic two-port network used to extract the bond-pad insertion loss.

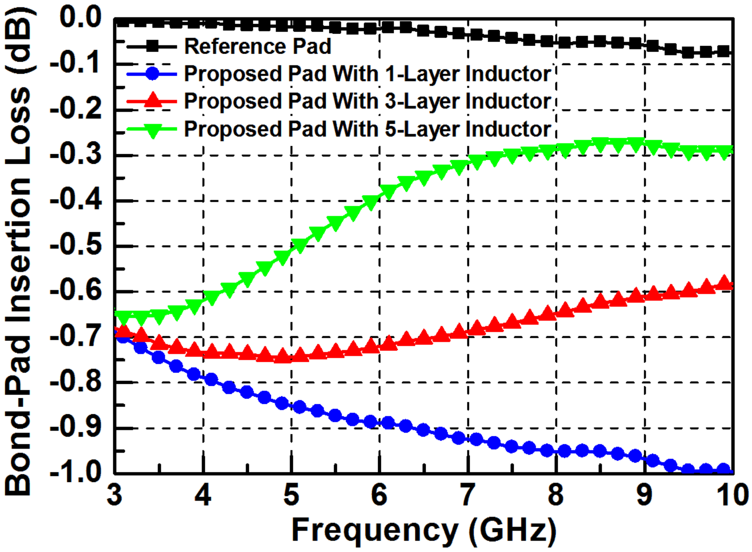


Fig. 3.10. Extracted insertion losses of the fabricated bond pads under different frequencies.

3.4.3. Comparison Among Simulated and Measured Results

To verify the equivalent circuit model for the proposed bond pad shown in Fig. 3.4, the simulated bond-pad capacitance using the equivalent circuit model has been compared with the extracted bond-pad capacitance. The dimensions of the passive components used in the circuit model for the proposed bond pad with 5-layer inductor are listed in Table 3.1. The simulated and extracted bond-pad capacitances of the proposed bond pad with the 5-layer stacked inductor are compared in Fig. 3.11. The simulation tool used to simulate the bond-pad capacitance is Ansoft Designer/Nexxim.

Table 3.1

Dimensions of Passive Components Used in the Bond-Pad Model With 5-Layer Stacked Inductor

Component	**C_P**	**C_{C1}**	**C_{C2}**	**R_1**	**R_2**	**L_S**
Dimension	**45 fF**	**232 fF**	**10 fF**	**220 Ω**	**250 Ω**	**8.695 nH**
Component	**C_F**	**R_S**	**C_{OX1}**	**C_{OX2}**	**C_{SUB}**	**R_{SUB}**
Dimension	**21 fF**	**53 Ω**	**27.5 fF**	**74 fF**	**480 fF**	**16.42 Ω**

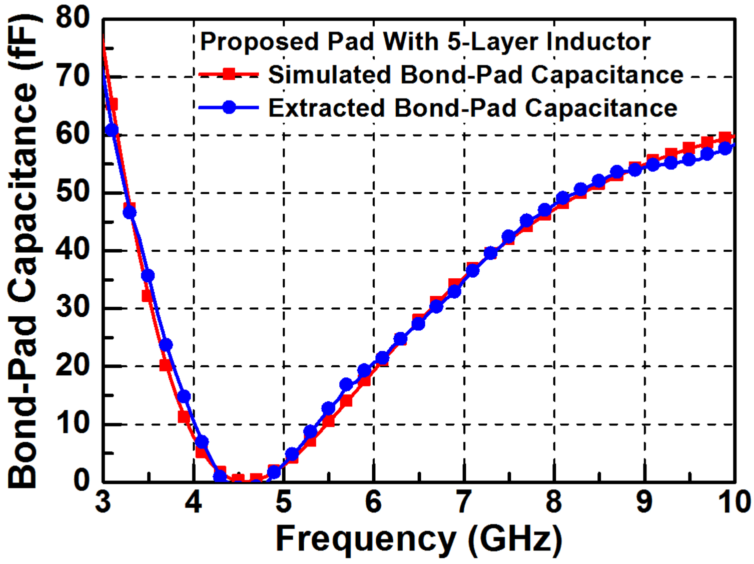


Fig. 3.11. Comparison of the simulated and extracted bond-pad capacitance.

As shown in Fig. 3.11, the extracted bond-pad capacitance agrees very well with the simulated bond-pad capacitance from 3 to 10 GHz. Thus, the circuit model for the proposed bond pad structure is appropriate to model the bond-pad capacitance. To refine the circuit model for the proposed bond pad comprehensively, more test devices are needed to enhance the accuracy of this circuit model for different frequency bands. Different device dimensions can be used in the simulation to further reduce the bond-pad capacitance or to adjust the frequency band in which the bond-pad capacitance is reduced. In the three proposed bond pad structure, metal 5, which is closest to the bond-pad metal plate (metal 6), was used to realize the stacked inductor. As a result, the coupling capacitance C_{C1} is large. To reduce C_{C1}, the stacked inductor can be realized with lower metal layers to increase the distance between the bond-pad metal plate and the stacked inductor.

3.5. Summary

In this chapter, an ultra low-capacitance bond pad is proposed and verified in a 130-nm CMOS process. By inserting a stacked inductor under the conventional bond-pad metal plate, the proposed bond pad performs much lower parasitic capacitance. The experimental results have proven that the embedded inductor can be used to reduce the bond-pad capacitance. At 5 GHz, the capacitance of the proposed bond pad with the five-layer stacked inductor is only 3.15 fF, which is quite small. Therefore, the proposed bond pad is suitable for gigahertz RF applications. Moreover, the frequency at which the capacitance of the proposed bond pad is minimum can be adjusted by changing the dimensions of the stacked inductor and the metal plates of the bond pad. To further reduce the chip area and the parasitic capacitance at the I/O pad, the ESD protection device can be co-designed with the proposed bond pad. For example, the impedance isolation technique can be used to optimize the RF characteristics at the input and output nodes, which include the bond pad and the on-chip ESD protection devices [36]. Besides, the ESD protection device can be placed under the bond pad, which had been demonstrated to be feasible [93], [94]. With the bond-pad model developed in this chapter, the capacitance of the proposed bond pad can be taken into consideration during the design phase of the RF front-end circuits. The proposed low-capacitance bond pad structure, achieved by only layout modification, is fully compatible to general CMOS processes for RF applications.

Chapter 4

ESD Protection Design for 1-to-10 GHz Distributed Amplifier in CMOS Technology

In this chapter, on-chip electrostatic discharge (ESD) protection schemes are proposed for wideband radio-frequency (RF) applications. Two Distributed ESD protection schemes are presented and applied to protect the distributed amplifiers against ESD stresses. Fabricated in a 0.25-μm CMOS process, the distributed amplifier with the first protection scheme of equal-sized distributed ESD (ES-DESD) protection scheme, which contributes an extra 300-fF parasitic capacitance to the signal path, can sustain the human-body-model (HBM) ESD level of 5.5 kV and machine-model (MM) ESD level of 325 V, while exhibits the power gain of 4.7 ± 1 dB from 1 to 10 GHz. With the same total parasitic capacitance from the ESD protection devices, the distributed amplifier with the second protection scheme of decreasing-sized distributed ESD (DS-DESD) protection scheme achieves better ESD robustness of over 8-kV HBM ESD level and 575-V MM ESD level, while exhibits the power gain of 4.9 ± 1.1 dB over the 1 to 9.2-GHz band. The design methodologies of the distributed ESD protection schemes are addressed in this chapter. Moreover, both the RF and ESD performance of the distributed amplifiers with these two proposed ESD protection schemes are compared. With these two proposed ESD protection schemes, wideband RF performance and ESD robustness of the distributed amplifier can be successfully co-designed to meet the application specifications [95], [96].

4.1. Background

Wideband distributed amplifiers have many applications, such as television, pulsed radars, and broadband optical communication. Distributed amplifiers employ a topology where the shunt capacitances contributed by each gain stages are separated, but the output currents are combined together. Inductive elements are used to separate and compensate the capacitances at the input and output nodes of each gain stage. The combination of series inductive elements and shunt capacitances forms a lumped artificial transmission line with the specific characteristic impedance. The characteristic impedance of the artificial transmission line can be adjusted to match the termination resistance to improve the RF performance over a very wide bandwidth.

Early distributed amplifiers were implemented by using vacuum tubes and high-speed GaAs MESFETs [97]–[102]. Recently, distributed amplifiers have been realized in CMOS technology and reported for the advantages of a lower cost and a higher integration capability [103]–[109]. A distributed amplifier utilizing parasitic packaging and bondwire inductors had been realized in a 0.8-μm CMOS process to achieve the power gain of 5 ± 1.2 dB over the 300-kHz to 3-GHz band [103]. Implemented in a 0.6-μm CMOS process, a fully integrated distributed amplifier using on-chip planar square inductors has achieved a pass-band power gain of 6.1 dB from 0.5 to 4 GHz with 5.5-GHz unity-gain frequency [104]. Besides, a fully differential distributed amplifier in the same process has performed 5.5-dB pass-band power gain from 0.5 to 7.5 GHz and 8.5-GHz unity-gain frequency [105]. A three-stage distributed amplifier designed with coplanar strip lines has achieved a low-frequency gain of 5 dB and the unity-gain frequency of 15 GHz in a 0.18-μm CMOS process [106]. Two distributed amplifiers employing high-impedance coplanar waveguides as inductive elements have exhibited 8-dB and 10-dB power gains up to 10 GHz, respectively [107]. Using the cascade topology, two wideband CMOS distributed amplifiers fabricated in a 0.18-μm CMOS process had been reported with 7.3 ± 0.8 dB power gain from 0.6 to 22 GHz [108], and 10.6 ± 0.5 dB power gain over the 0.5 to 14-GHz bandwidth [109], respectively. The operating frequency and power gain of distributed amplifiers have become higher and higher. However, (electrostatic discharge) ESD protection, which has become one of the most important reliability issues in IC fabrication, is neither considered nor mentioned in those works.

The reported ESD protection schemes for wideband RF applications have been overviewed in Chapter 2. In this chapter, the distributed amplifiers co-designed with two new ESD protection schemes are proposed and verified in a 0.25-μm CMOS process. By dividing the large ESD protection device into several equal-sized sections and placing each of them before each gain stage, the first ESD protection scheme is called the equal-sized distributed ESD (ES-DESD) protection scheme. Applied in the distributed amplifier, the second ESD protection scheme, which is called the decreasing-sized distributed ESD (DS-DESD) protection scheme, divides one large ESD protection device into several parts with different sizes, and allocates them from the input pad to the last gain stage with descending sizes. The wideband RF performance and ESD robustness of the reference distributed amplifier without ESD protection and the distributed amplifiers with ES-DESD and DS-DESD protection schemes have been verified and compared in this chapter.

4.2. Distributed Amplifier Design

4.2.1. Basic Distributed Amplifier Structure

The basic distributed amplifier structure is shown in Fig. 4.1. To be fabricated in a 0.25-µm CMOS process with high ESD robustness, this distributed amplifier is co-designed with the distributed ESD protection scheme. A three-stage distributed amplifier with a flat gain of 5 dB over a 10 GHz bandwidth was set as the specification. The number of stages was decided according to the consideration of the layout area, the inductor loss, and the power consumption. The input and output were matched to the source resistance of 50 Ω, and the phase shift was designed to be approximately linear over the passband. The power-supply voltage in this 0.25-µm CMOS process is 2.5 V.

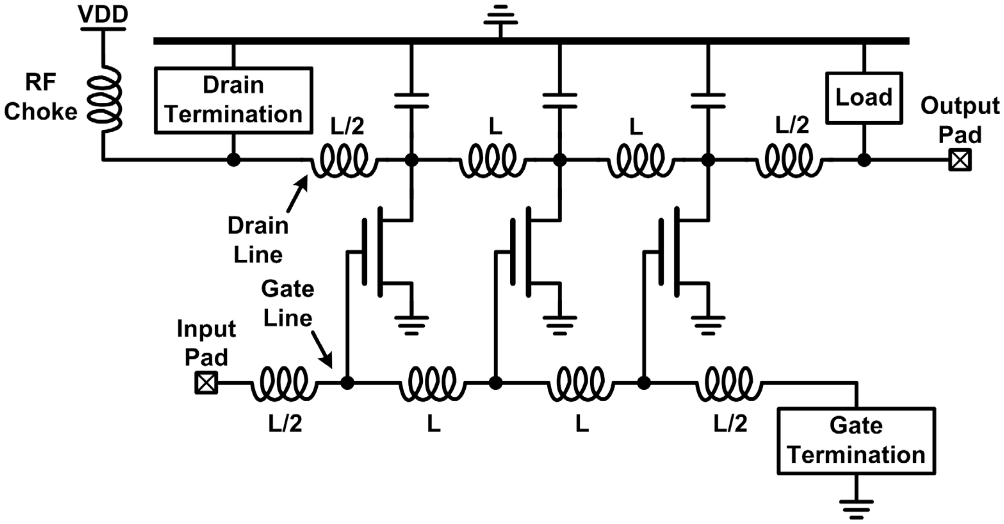


Fig. 4.1. Basic distributed amplifier.

The added gate inductors and the parasitic gate capacitances form the artificial transmission line (gate line). Similarly, the added drain inductors and the drain capacitances form another artificial transmission line (drain line). The cutoff frequency of the artificial transmission line is defined as

$$\omega_c = \frac{2}{\sqrt{LC}}\,. \tag{4.1}$$

According to the circuit structure shown in Fig. 4.1, a peak in the gain response appears near the cutoff frequency of the transmission line. Since a flat gain response across the passband is preferred, this effect should be reduced. The staggering technique was employed in this design. The dependence of the gain response of the distributed amplifier on the staggering factor is shown in Fig. 4.2. Defined as the ratio of the drain-line to the gate-line cutoff frequencies, the staggering factor (r) of about 0.7 has been analyzed as the optimum value from Fig. 4.2 [110].

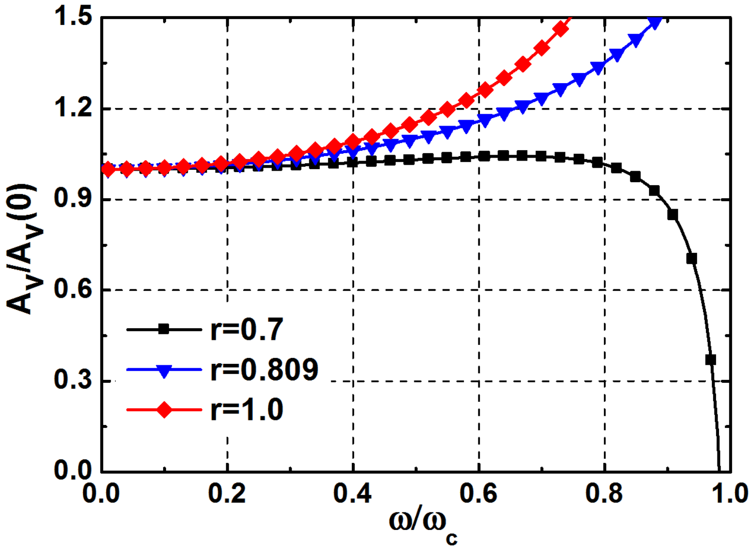


Fig. 4.2. Normalized gain response of the distributed amplifier with different staggering factors. r = 1 corresponds the unstaggered case.

The impedance looking into the termination of the L-C artificial transmission line (Z_{oT}) can be expressed as

$$Z_{oT} = \sqrt{\frac{L}{C}\left(1 - \frac{\omega^2 LC}{4}\right)} = \sqrt{\frac{L}{C}\left(1 - \frac{\omega^2}{\omega_c{}^2}\right)}. \tag{4.2}$$

The L, C, and ω_c are the inductance, capacitance, and cutoff frequency of the L-C artificial transmission line, respectively. The impedance looking into the L-C artificial transmission line exhibits a strong deviation from the nominal impedance near the cutoff frequency. One way to improve the impedance match is to insert the m-derived half sections between the artificial transmission line and each termination as well as between the artificial transmission line and each port [92]. The m-derived half circuit is illustrated in Fig. 4.3, where the optimum value of m = 0.6 is applied to the distributed amplifier in this chapter. With the combination of the staggering technique and the m-derived half section, the modified distributed amplifier is shown in Fig. 4.4.

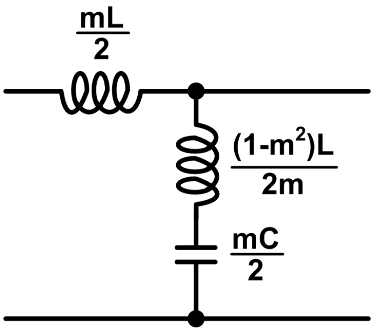


Fig. 4.3. Low-pass m-derived half section.

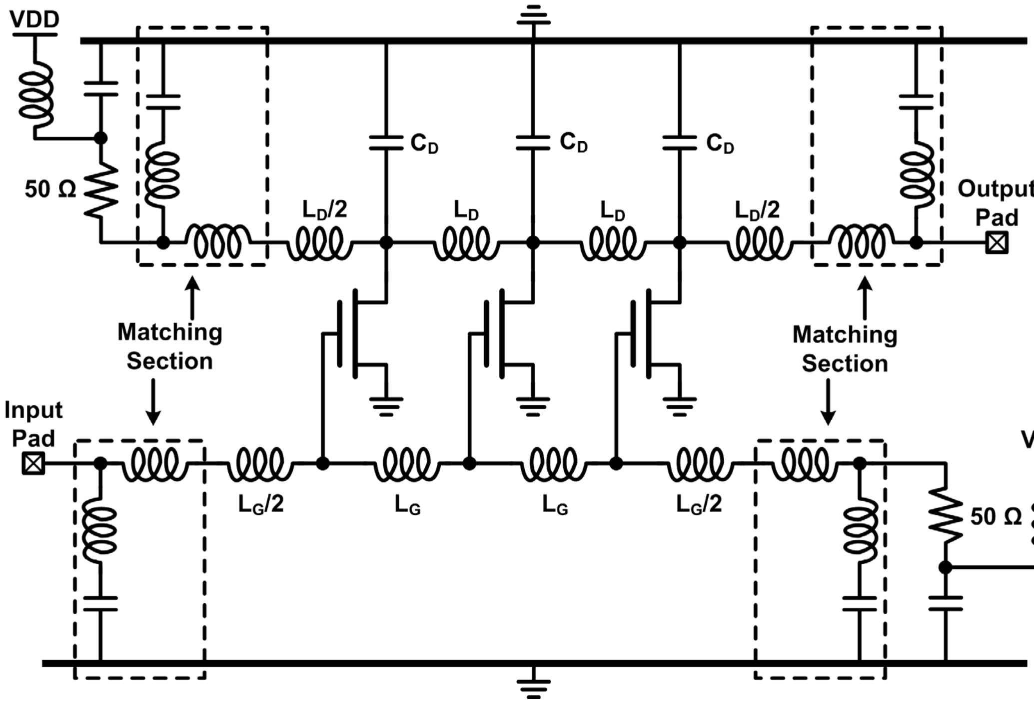


Fig. 4.4. Modified distributed amplifier with staggering technique and m-derived half section.

4.2.2. Ideal Distributed Amplifier

With the given topology and specifications, the circuit parameters can then be obtained. After some minor tuning based on those component values in this 0.25-μm CMOS process, the distributed amplifier schematic is shown in Fig. 4.5 with the dimensions of the matching component. The dimensions of the NMOS transistors in each stage are 110 μm/ 0.24 μm. The additional capacitance has been added to fulfill the required C_D value in Fig. 4.4. The simulated S-parameters of this distributed amplifier are shown in Fig. 4.6, where it performs the power gain (S_{21}-parameter) of 5.1 ± 0.3 dB from DC to 16 GHz. The simulated S_{11}-, S_{22}-, and S_{12}-paremeters are almost below -10 dB from DC to 16 GHz, as shown in Fig. 4.6. As shown in Fig. 4.7, the simulated phase shift of S_{21}-parameter is approximately linear, which means that the time delay is almost constant throughout the bandwidth from 0.5 to 18 GHz. As observed, the simulated results agree well with the conventional theory. However, with the consideration for the parasitic effects of the passive devices, especially the on-chip spiral inductors, the situation could be different.

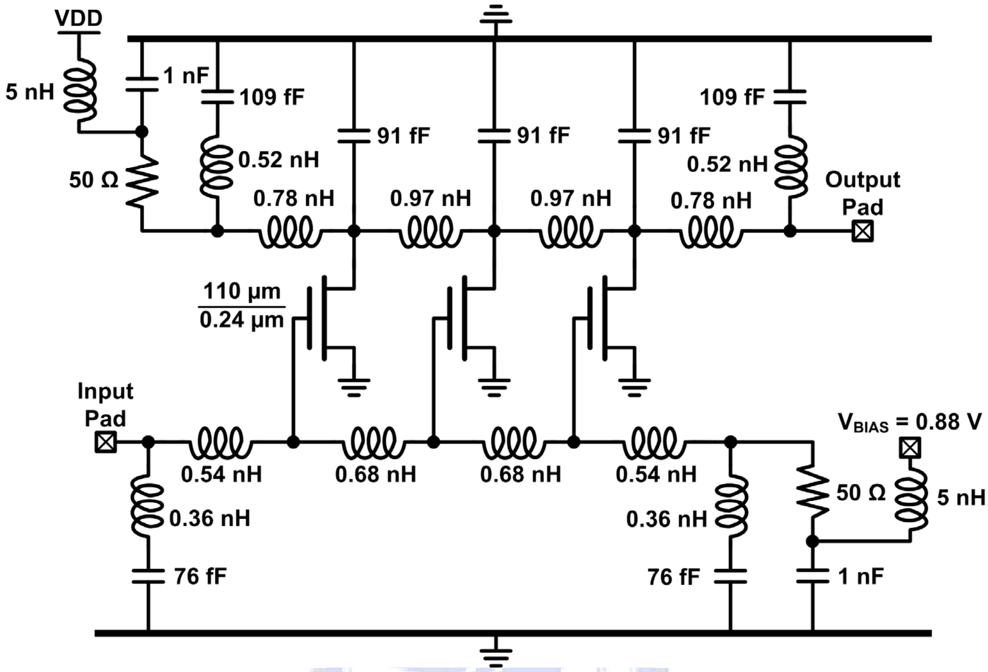


Fig. 4.5. Ideal distributed amplifier according to the design theorems.

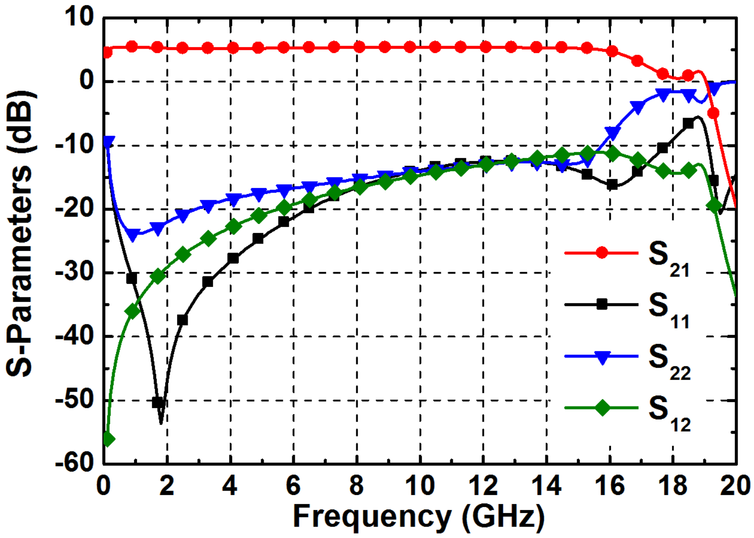


Fig. 4.6. Simulated S-parameters of the ideal distributed amplifier shown in Fig. 4.5.

4.2.3. *Inductor Modeling*

Due to the mutual influences among the components, to optimize a distributed amplifier with physical components becomes complicated design iterations. Because of the complexities, an auto-optimization solution is employed. To utilize this solution, the passive device models need to be established. Among those passive devices, on-chip spiral inductors are the most important and critical for the complicated parasitic effects. Thus, an on-chip spiral inductor library is built up first.

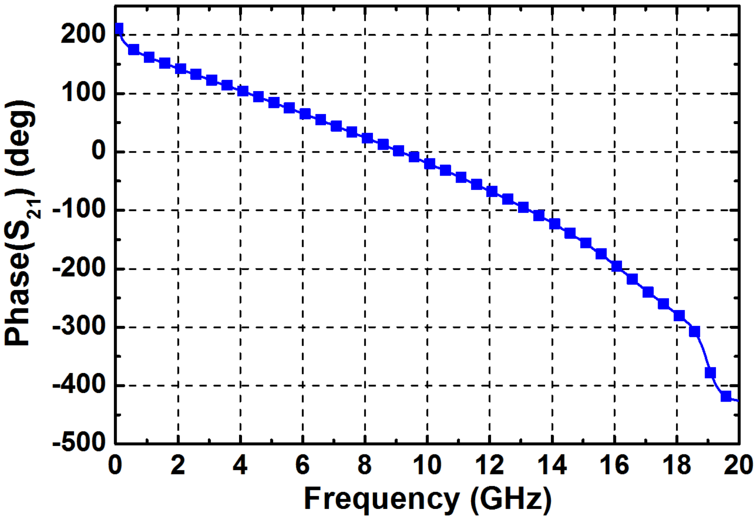


Fig. 4.7. Simulated phase shift of S_{21}-parameter of the ideal distributed amplifier shown in Fig. 4.5.

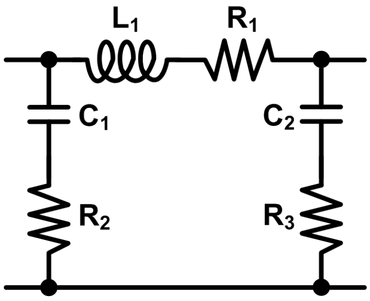


Fig. 4.8. Frequency-dependent π-model for on-chip inductors.

The method to generate inductor models is a combination of the analytic methods, measured data, simulated data, and some other techniques [111], [112]. In this chapter, six on-chip spiral inductors have been generated by the lumped π-model shown in Fig. 4.8 and modeled from 1 to 3.5 turns with the step of 0.5 turn. The basic parameters, including the inner radius of 55 μm, top metal width of 10 μm, and the track spacing of 2 μm, of these inductors were kept identical. The inductance curve of the lumped model, which is shown in Fig. 4.9, fits well to the simulated result of the on-chip spiral inductor up to 16 GHz. Therefore, these lumped models can be employed to replace the spiral inductors during the design optimization for the distributed amplifier.

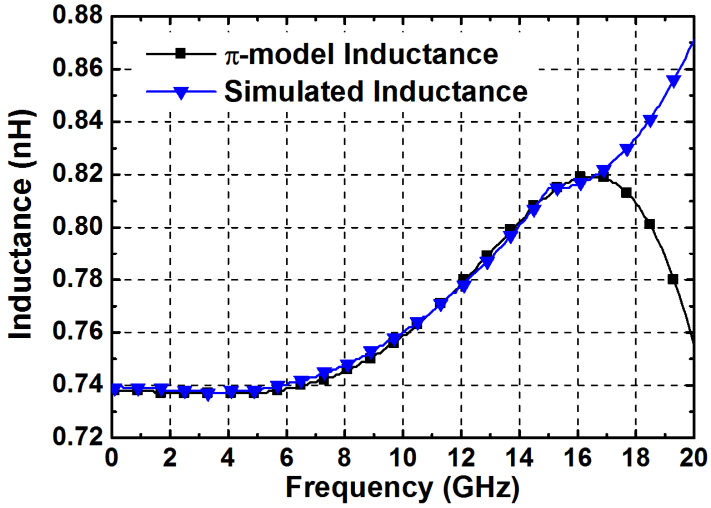


Fig. 4.9. Comparison of inductance between the lumped π-model and the simulated spiral inductor.

4.2.4. *Optimized Distributed Amplifier*

After building an on-chip spiral inductor library, the auto-optimization can be operated by the ADS simulator. The distributed amplifier structure was set up as that shown in Fig. 4.5, with all variable passive component values. Then, the optimization targets were set in the

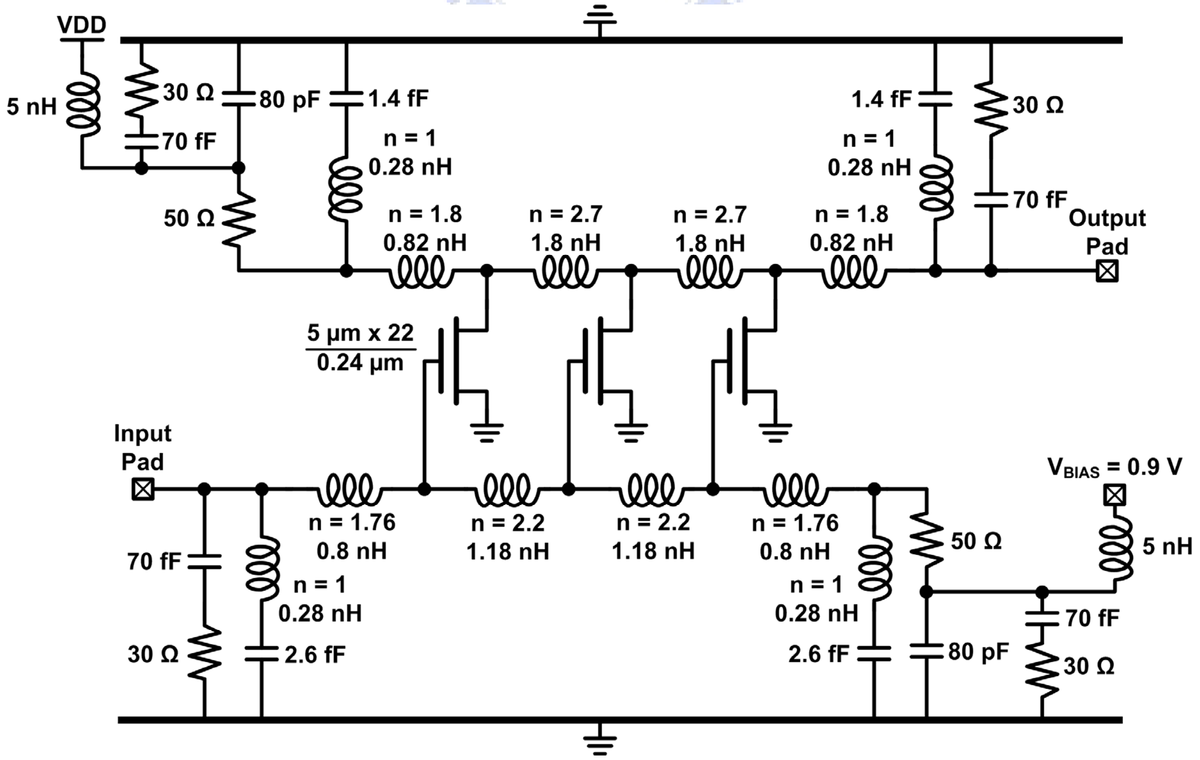


Fig. 4.10. Arbitrarily optimized distributed amplifier.

simulator. First, the S-parameters except S_{21}-parameter were chosen to be less than -10 dB up to 16 GHz. The power gain (S_{21}-parameter) was kept more than 5 dB throughout the same bandwidth of DC to 16 GHz. Second, the difference of the time delay over the 16-GHz bandwidth was minimized. The inductance can be adjusted by changing the number of turns. The distributed amplifier is kept in optimization iterations until these goals can not be further approached. The optimized distributed amplifier with the component values is shown in Fig. 4.10. In the optimized distributed amplifier, the turns of the inductors were random values between 1 and 3.5, which can not be implemented in silicon chips. Thus, the re-optimization is needed to set the inductors with the feasible turn values, which are between 1 and 3.5 with the step of 0.5. After replacing the ideal inductors with the feasible on-chip spiral inductors, the feasible distributed amplifier is shown in Fig. 4.11. The m-derived half sections were removed because the on-chip inductors could not be realized with the arbitrary turns required in the primary optimization.

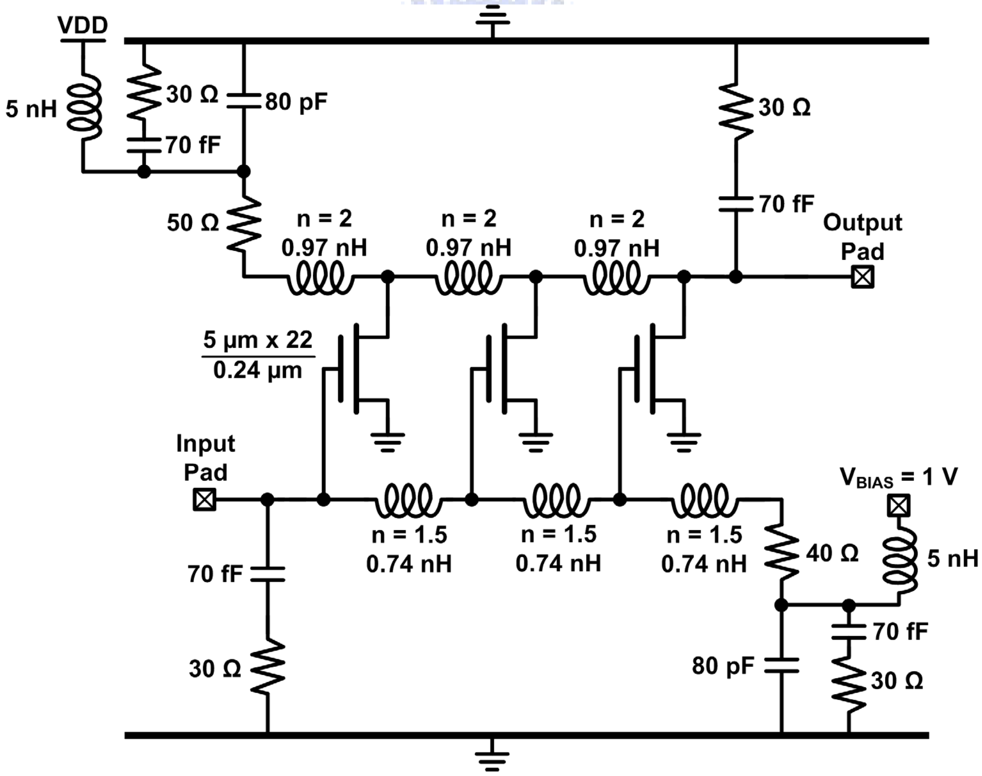


Fig. 4.11. Feasible distributed amplifier.

Fig. 4.12 shows the S_{21}-parameters of the distributed amplifier with ideal inductors, the arbitrarily optimized distributed amplifier, and the feasible distributed amplifier. Without the m-derived half sections, the S_{21}-parameter of the feasible distributed amplifier does not degraded significantly around the cutoff frequency compared with the distributed amplifier with ideal inductors and the arbitrarily optimized distributed amplifier. The performance of the feasible distributed amplifier in the 0.25-μm CMOS process was acceptable, and it will be equipped with different ESD protection schemes for comparison.

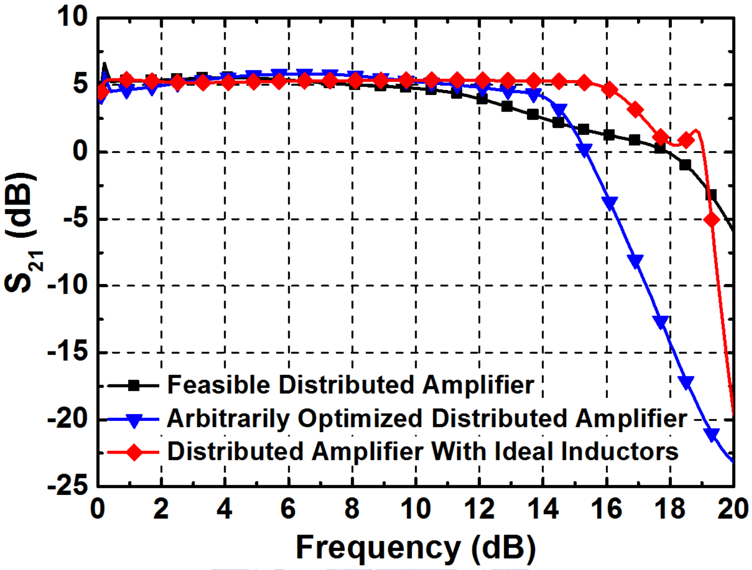


Fig. 4.12. Comparison of S_{21}-parameters among the feasible distributed amplifier, the arbitrarily optimized distributed amplifier, and the distributed amplifier with ideal inductors.

4.3. ESD Protection Design for Distributed Amplifier

4.3.1. Concept of Distributed ESD Protection

Since the distributed amplifier is the front-end of the RF system, ESD protection is indispensable. The parasitic capacitance and parasitic resistance from the ESD protection devices inevitably degrade the RF performance of distributed amplifier in impedance match and noise figure. To mitigate the impacts caused by ESD protection devices, ESD protection devices should be realized with low parasitic capacitances and high quality factors (Q). The shallow-trench-isolated (STI) diodes meet these two requirements [113]. Besides, they can sustain a very high ESD protection level with the cooperation of the power-rail ESD clamp circuit [9]. However, wideband impedance matching throughout the frequency band from DC to 10 GHz can not be achieved by using the traditional double-diode ESD protection scheme, which is shown in Fig. 1.6 [8]. To achieve a comparable wideband input matching of the distributed amplifier after inserting the ESD protection circuit, the ESD protection device at the input pad must be separated as the MOS transistors in the distributed amplifier. The extra parasitic capacitance of each ESD protection section can be absorbed into the capacitive elements in the artificial gate line. Hence, the value of the characteristic impedance in each gate-line section can be kept unchanged and the matching condition can still be maintained after the ESD protection devices are applied to the distributed amplifier.

4.3.2. Proposed Distributed ESD Protection Scheme

According to the distributed ESD protection scheme reported in [51], the first distributed amplifier is co-designed with the equal-sized distributed ESD (ES-DESD) protection scheme, as shown in Fig. 4.13. The power-rail ESD clamp circuit consists of the ESD clamp NMOS (M_{NESD}) and the ESD detection circuit, which is formed by an RC timer and an inverter. [9]. During normal circuit operating conditions, the node between R_1 and C_1 is charged to high potential (VDD). Since NMOS M_N is turned on and PMOS M_P is turned off, M_{NESD} is kept off during normal circuit operating conditions. During ESD stresses, the ESD energy is coupled to VDD quickly. With the RC delay provided by R_1 and C_1, the gate voltages of M_P and M_N are initially at low potential (~0 V). Therefore, M_P is turned on to boost the gate potential of M_{NESD}. Consequently, M_{NESD} is turned on to provide ESD current paths between VDD and VSS. In this chapter, M_{NESD} with the size of 800 μm/0.35 μm is used in all of the ESD-protected distributed amplifiers.

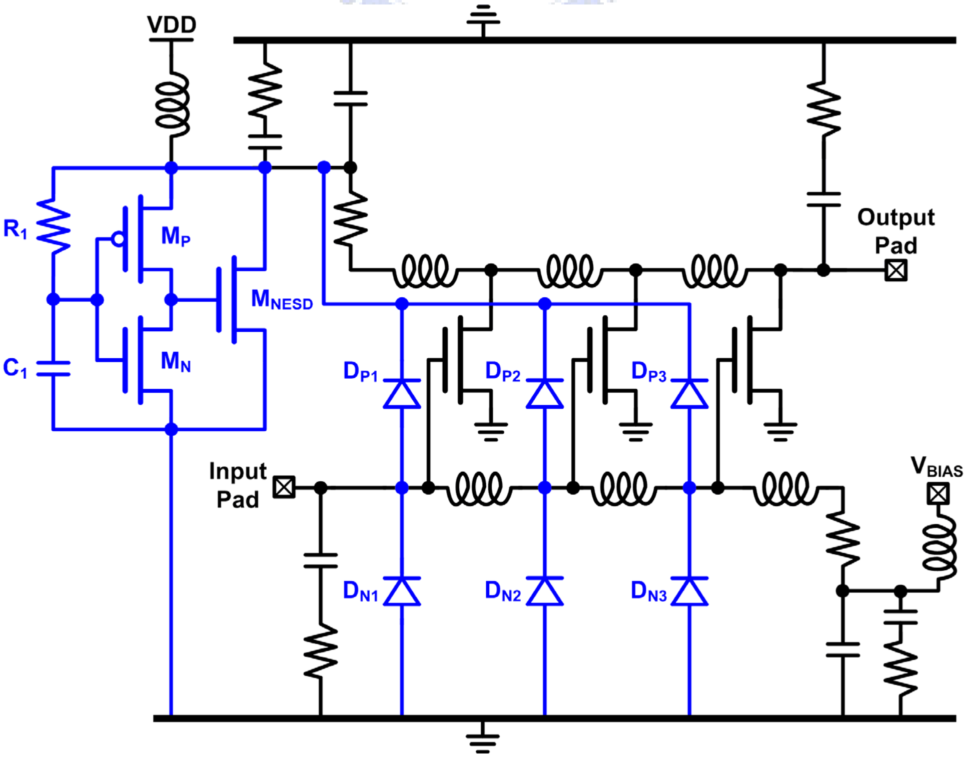


Fig. 4.13. Distributed amplifier with distributed ESD protection scheme.

The STI diodes, used as ESD protection devices on the signal path, were divided into three sections with equal sizes and applied to each gain stage in the distributed amplifier. Each ESD protection section contains the P+/N-well diode (D_P) and the N+/P-well diode (D_N). By applying the ES-DESD protection scheme, each gain stage is protected during ESD stresses. With the power-rail ESD clamp circuit, the distributed amplifier with the ES-DESD protection scheme is expected to sustain high ESD robustness. During ESD stresses, the distributed amplifier with the ES-DESD protection scheme can be approximately modeled as a resistive ladder [51], as shown in Fig. 4.14, where R_L denotes the parasitic series resistance of the spiral inductor and R_{ESD} is the equivalent turn-on resistance of the ESD protection diode. Larger R_L and R_{ESD} degraded the ESD robustness, because joule heat is generated when ESD current flows through them. To enhance the ESD robustness, R_L and R_{ESD} should be minimized. According to this consideration, the decreasing-sized distributed ESD (DS-DESD) protection scheme is proposed [53]. Since the first ESD protection section is closest to the input pad, most ESD current is expected to flow through it. By enlarging the dimensions of the ESD protection devices in the first section, the proposed DS-DESD protection scheme can reduce the R_{ESD} of the first ESD protection section, which reduces the joule heat when ESD current flows through the first ESD protection section. With a relatively large device in the first ESD protection section, ESD current can be more efficiently bypassed through the first ESD protection section, as compared with the ES-DESD protection scheme. Under the same total parasitic capacitance from the ESD protection devices, the distributed amplifier with the proposed DS-DESD protection scheme is expected to sustain better ESD robustness than that of the distributed with the ES-DESD protection scheme.

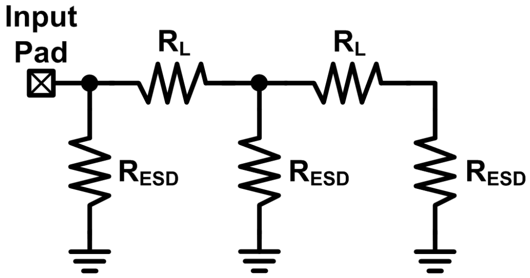


Fig. 4.14. Resistive ladder model of the distributed ESD protection scheme during ESD stresses.

4.3.3. RF Performance of Distributed Amplifier Without and With ESD Protection

For a wideband RF circuit, the S-parameters, noise figure, and phase shift are the main factors to determine its performance. Simulations of the distributed amplifier without ESD protection and the distributed amplifiers with the two distributed ESD protection schemes were performed to investigate the performance degradation caused by the ESD protection devices.

In this work, the total parasitic capacitances of 300 fF and 600 fF are allocated to the ESD protection devices in both distributed ESD protection schemes. After the total parasitic capacitance is assigned, the dimensions of ESD protection diodes in each section can be determined. The reference distributed amplifier without ESD protection is named DA0. With 300-fF parasitic capacitance from the ESD protection devices, the distributed amplifiers DA1 and DA2 are equipped with the ES-DESD and DS-DESD protection schemes, respectively. Distributed amplifiers DA3 and DA4 are equipped with the 600-fF ES-DESD and DS-DESD protection schemes, respectively. Moreover, the ES-DESD protection scheme with 900-fF parasitic capacitance is applied to the distributed amplifier DA5. The parasitic capacitances in each ESD protection section of the five ESD-protected distributed amplifiers are listed in Table 4.1. A pair of a P+/N-well diode (with the size of 5.5 μm × 1.2 μm) and an N+/P-well diode (with the size of 5.5 μm × 1.2 μm) contributes 25-fF parasitic capacitance. The specified parasitic capacitance is realized by multiple pairs of P+/N-well and N+/P-well diodes. In the DS-DESD protection scheme, the percentage of the parasitic capacitance realized in each ESD protection section can be further optimized with the consideration for wideband impedance match and ESD protection capability.

Table 4.1

Parasitic Capacitance in Each ESD Protection Section of the ESD-Protected Distributed Amplifiers

ESD-Protected Distributed Amplifier	ESD Protection Scheme	$D_{P1} + D_{N1}$ (fF)	$D_{P2} + D_{N2}$ (fF)	$D_{P3} + D_{N3}$ (fF)
DA1	ES-DESD	100	100	100
DA2	DS-DESD	200	75	25
DA3	ES-DESD	200	200	200
DA4	DS-DESD	400	150	50
DA5	ES-DESD	300	300	300

To investigate the effects caused by the 300-fF parasitic capacitance from the ESD protection devices, the simulated S_{21}-parameters and the phase shifts of DA0, DA1 (distributed amplifier with 300-fF ES-DESD protection scheme), and DA2 (distributed amplifier with 300-fF DS-DESD protection scheme) are compared in Fig. 4.15 and 4.16, respectively. As shown in Fig. 15, DA0 has the best performance among these three circuits because it has no ESD protection device on the signal path. However, the difference of the passband gain among these three circuits is small. The simulated phase shifts of DA0, DA1, and DA2 are compared in Fig. 4.16. There are three straight lines from low frequency to 14 GHz with no apparent difference.

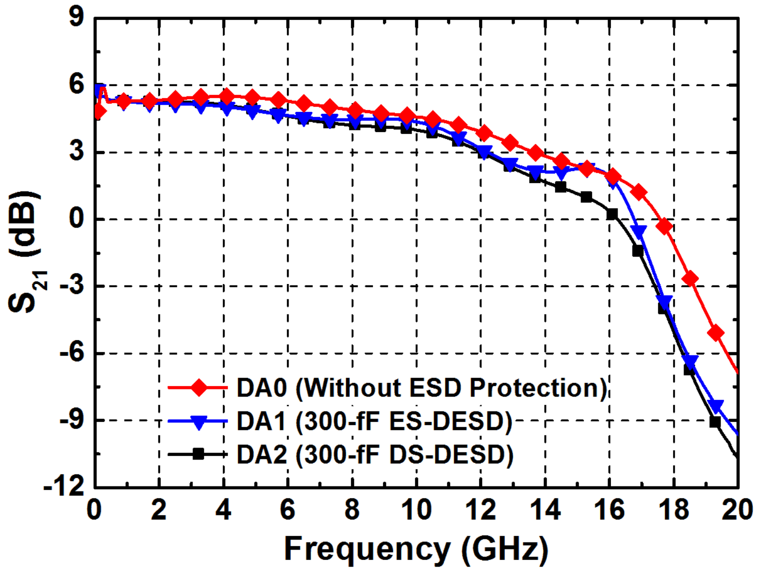


Fig. 4.15. Simulated S_{21}-parameters of the distributed amplifiers without and with distributed ESD protection schemes. The total parasitic capacitance of ESD protection devices are 300 fF.

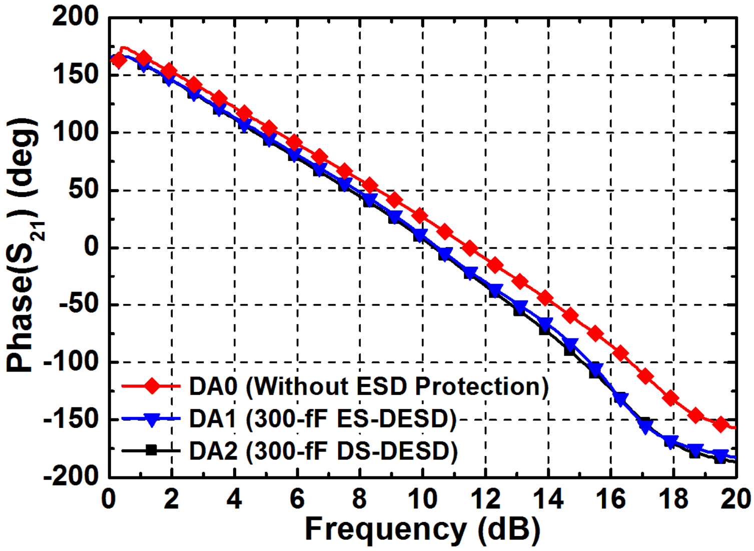


Fig. 4.16. Simulated phase shifts of the distributed amplifiers without and with distributed ESD protection schemes. The total parasitic capacitance of ESD protection devices are 300 fF.

With larger parasitic capacitance from the ESD protection devices, the RF performance can be degraded more significantly. The simulated S_{21}-parameters of DA0, DA3 (with 600-fF ES-DESD protection scheme), and DA4 (with 600-fF DS-DESD protection scheme) are compared in Fig. 4.17. DA3 and DA4 have lower power gains than those of DA1 and DA2. Similarly, the distributed amplifier with the DS-DESD protection scheme (DA4) has the lowest power gain under the same parasitic capacitance from the ESD protection devices.

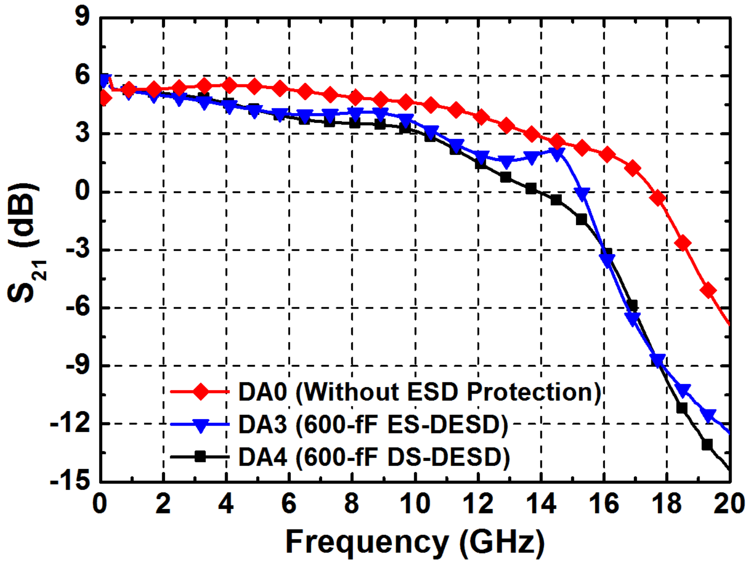


Fig. 4.17. Simulated S_{21}-parameters of the distributed amplifiers without and with distributed ESD protection schemes. The total parasitic capacitance of ESD protection devices are 600 fF.

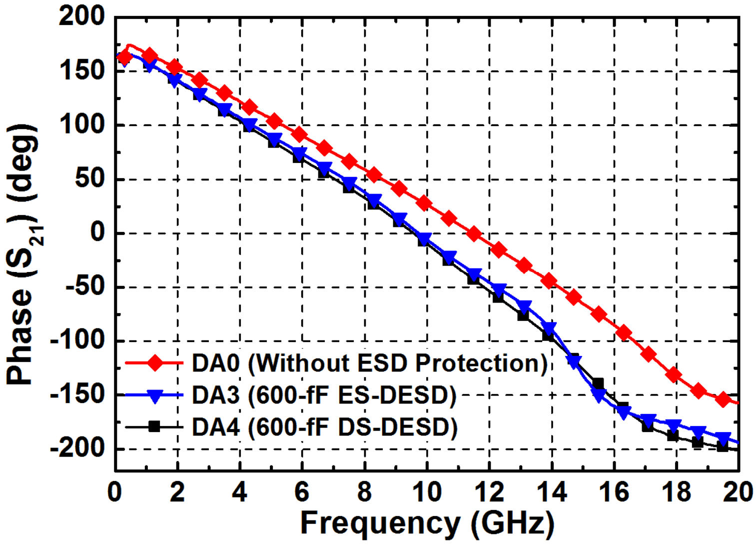


Fig. 4.18. Simulated phase shifts of the distributed amplifiers without and with distributed ESD protection schemes. The total parasitic capacitance of ESD protection devices are 600 fF.

The simulated phase shifts of DA0, DA3, and DA4 are compared in Fig. 4.18. The phase shifts of DA3 and DA4 were less linear than those of DA1 and DA2 because of the larger parasitic capacitances from the ESD protection devices. From the simulation results, to provide the distributed ESD protection for the distributed amplifier without degrading wideband RF performance simultaneously, the dimensions of the ESD protection devices can not be too large.

4.4. Experimental Results

The reference distributed amplifier without ESD protection (DA0) and five distributed amplifiers with distributed ESD protection schemes (DA1–DA5) had been fabricated in a 0.25-μm CMOS process. The chip micrograph of these fabricated distributed amplifiers is shown in Fig. 4.19. In the following sub-sections, the wideband RF performances, including S-parameters, noise figures, and phase shifts of these fabricated distributed amplifiers will be measured and compared. The ESD robustness of these six distributed amplifiers will also be characterized and compared with failure analysis.

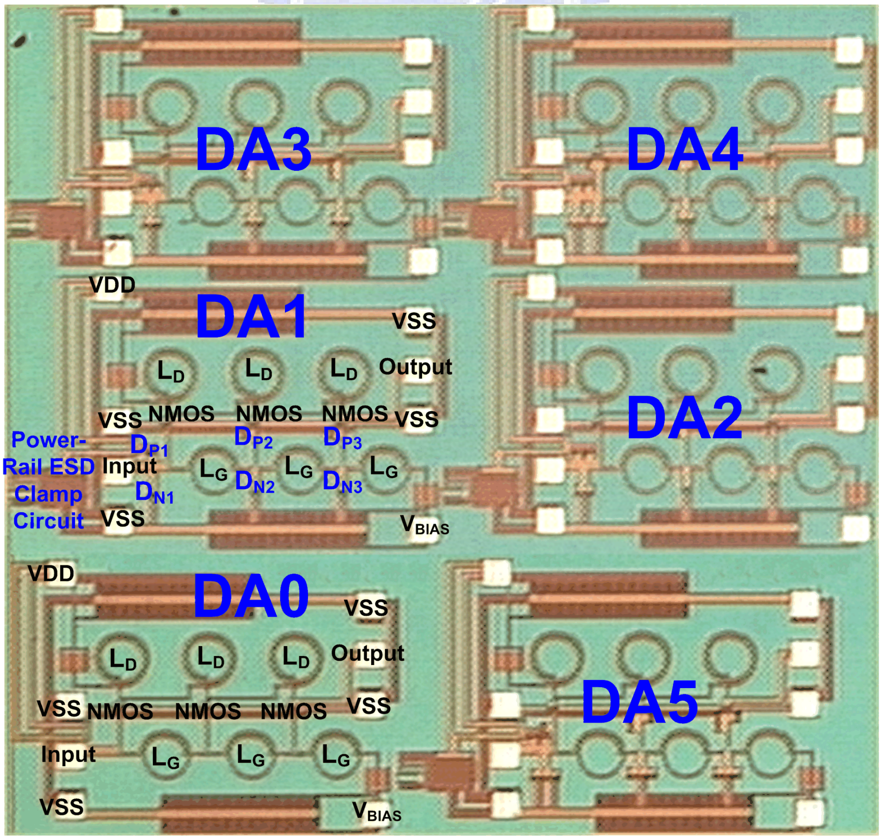


Fig. 4.19. Chip micrograph of the fabricated distributed amplifiers in a 0.25-μm CMOS process.

4.4.1. Measured Wideband RF Performance

The S-parameters of these six distributed amplifiers had been measured on-wafer with two-port ground-signal-ground (G-S-G) probes from 1 GHz to 18 GHz. The 20-GHz S-parameter measurement system (HP 85122A) is used to characterize the behavior of the circuits. The simulated and measured S_{21}-parameters of the reference distributed amplifier without ESD protection (DA0) is shown in Fig. 4.20. The measured result correlates well with the response of the post-layout simulation result, but still little difference exists. The post-layout simulation was performed with the addition of the parasitic effects from the interconnections in layout. The parasitic effects of the interconnections were obtained from the EM simulator of ADS momentum. The simulated S_{21}-parameter is 5 ± 1 dB from 1 to 10 GHz with the unity-gain frequency of 15.1 GHz. The measured S_{21}-parameter is 5 ± 1 dB from 1 to 11.4 GHz with the unity-gain frequency of 16.7 GHz. The deviation of the RF performance is attributed to several reasons, including the inaccuracy of the on-chip spiral inductor model, the temperature coefficients of the resistors, and the imprecise estimation of the bond-pad effects, etc.

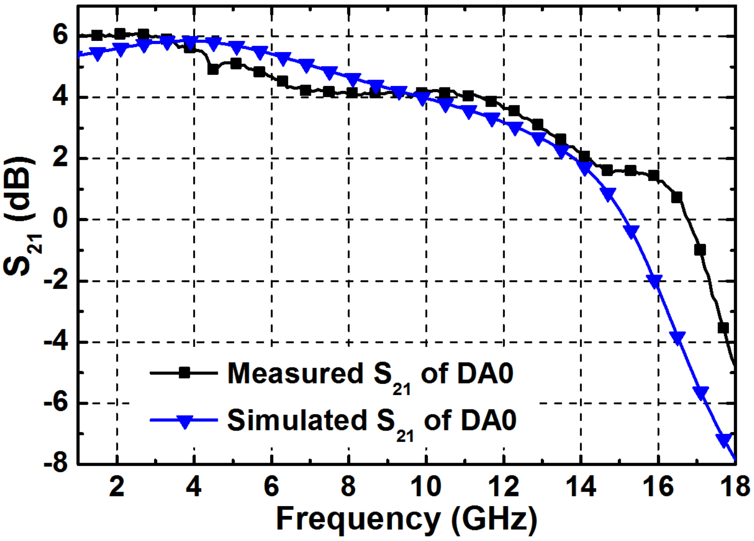


Fig. 4.20. Measured and simulated S_{21}-parameter of the reference distributed amplifier without ESD protection (DA0).

During the design phase, the coupling between the inductors was not considered. Since the inductances used in this circuit are quite small, the coupling between the inductors is also rather small and negligible. Although there is a slight difference between the simulated and measured RF performances of the distributed amplifiers, the degradation is fairly slight below

14 GHz. Thus, the coupling between the inductors can be ignored without causing design errors in the target of 1-to-10 GHz distributed amplifier. Besides, it was found that the passive devices at the input pad, output pad, drain termination, and gate termination were not necessary.

According to the simulated S_{21}-parameters in Fig. 4.15 and Fig. 4.17, the distributed amplifier without ESD protection achieves the best power gain among all distributed amplifiers. With the same total parasitic capacitance contributed by the ESD protection devices, the distributed amplifiers with the ES-DESD protection scheme perform better in S_{21}-parameter than the distributed amplifiers with the DS-DESD protection scheme. The measured S_{21}-parameters of the six distributed amplifiers, as compared in Fig. 4.21, conform to the simulated results except that DA2 achieves better gain response than DA1 below 9 GHz. With increased total parasitic capacitance from the ESD protection devices, the S_{21}-parameters of DA3, DA4, and DA5 are degraded. Only DA1 and DA2 have comparable performance to DA0.

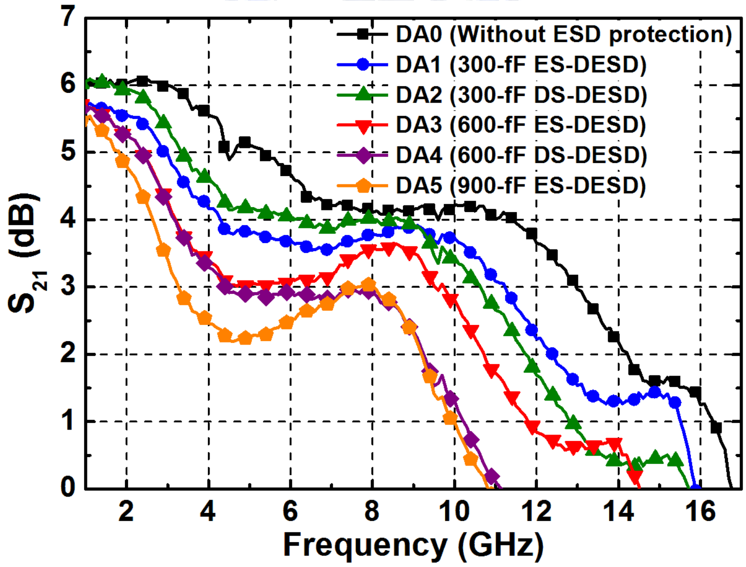
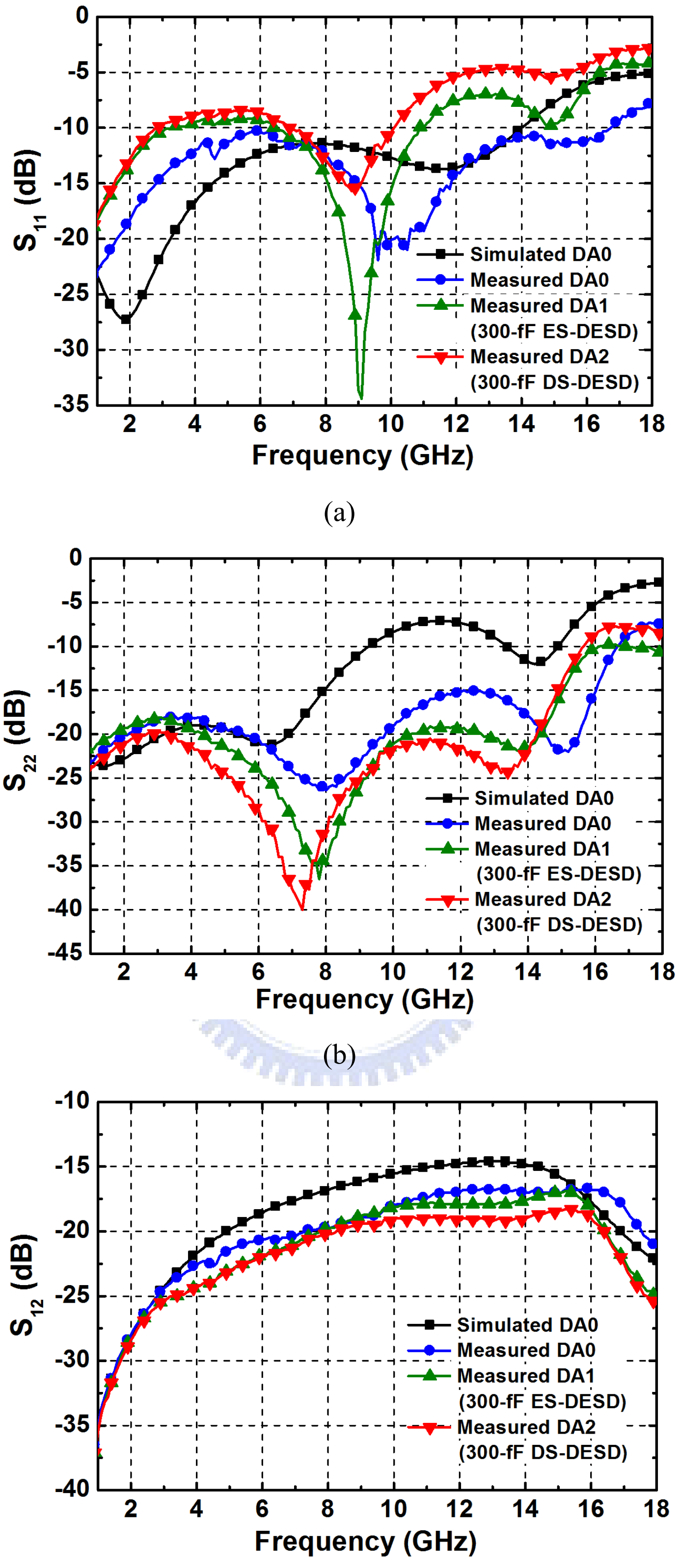


Fig. 4.21. Measured S_{21}-parameters of the distributed amplifiers with and without ESD protection.

The S_{11}-, S_{22}-, and S_{12}-parameters of DA0, DA1, and DA2 compared in Fig. 4.22(a)–(c). The measured S_{11}-parameter of DA0 corresponds well with the simulation result and is less than -10 dB. Applied with ESD protection schemes, DA1 and DA2 have higher S_{11}-parameters, which indicates that the input matching is somewhat degraded by the ESD protection devices.

As shown in Fig. 4.22(b) and (c), the measured S_{22}- and S_{12}-parameters of DA1–DA2



(a)

(b)

(c)

Fig. 4.22. (a) S_{11}-parameters, (b) S_{22}-parameters, and (c) S_{12}-parameters among the simulated and fabricated distributed amplifiers without ESD protection (DA0), distributed amplifier with the ES-DESD protection scheme (DA1), and distributed amplifier with the DS-DESD protection scheme (DA2).

are different from those of DA0. The output matching and reverse isolation are changed after the ESD protection devices are inserted. As shown in Fig. 4.23, the simulated and measured phase shifts of DA0 both present roughly linear curves from 1 to 16 GHz, whereas DA1 and DA2 only maintain linear phase shift up to 14 GHz.

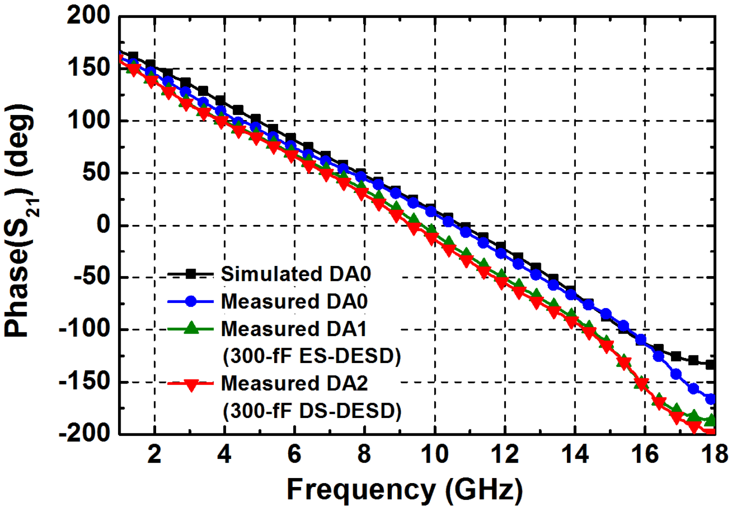


Fig. 4.23. Phase shifts among the simulated and fabricated distributed amplifiers without ESD protection (DA0), distributed amplifier with the ES-DESD protection scheme (DA1), and distributed amplifier with the DS-DESD protection scheme (DA2).

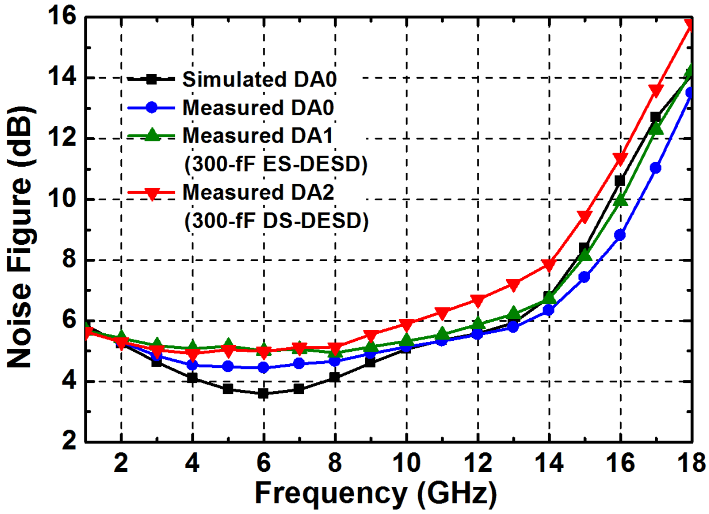


Fig. 4.24. Noise figures among the simulated and fabricated distributed amplifiers without ESD protection (DA0), distributed amplifier with the ES-DESD protection scheme (DA1), and distributed amplifier with the DS-DESD protection scheme (DA2).

The noise figure was measured by the high frequency modeling system (HP85122A) and the noise parameters extraction software (ATN NP5B) from 1 to 18 GHz. The measured noise figures are compared in Fig. 4.24. The simulated noise figure of DA0 achieves the lowest value of 3.6 dB at 6 GHz, where the measured noise figure is 4.4 dB. For DA1 and DA2, the lowest measured noise figures are 0.5- and 0.6-dB higher than that of DA0. Adding ESD protection devices to the distributed amplifier introduces extra noise, which degrades the noise figure.

4.4.2. ESD Robustness

To compare the ESD robustness, the distributed amplifier without ESD protection (DA0) and five ESD-protected distributed amplifiers were tested according to the criterion of 30% I-V curve shift at 1-μA current. The measured human-body-model (HBM) and machine-model (MM) ESD levels are listed in Table 4.2. The ESD tests were performed at room temperature, as specified in the ESD test standards. The distributed amplifier (DA0) without ESD protection only sustains a very low ESD level, which is far below the ESD specifications for commercial ICs (2 kV in HBM and 200 V in MM).

Table 4.2

HBM and MM ESD Robustness of the Distributed Amplifiers

Distributed Amplifier	**PS-Mode**		**ND-Mode**	
	HBM	**MM**	**HBM**	**MM**
DA0 (Without ESD Protection)	**250 V**	**20 V**	**200 V**	**20 V**
DA1 (300-fF ES-DESD)	**5.5 kV**	**325 V**	**7.5 kV**	**400 V**
DA2 (300-fF DS-DESD)	**> 8 kV**	**575 V**	**> 8 kV**	**650 V**
DA3 (600-fF ES-DESD)	**> 8 kV**	**575 V**	**> 8 kV**	**675 V**
DA4 (600-fF DS-DESD)	**> 8 kV**	**750 V**	**> 8 kV**	**850 V**
DA5 (900-fF ES-DESD)	**> 8 kV**	**800 V**	**> 8 kV**	**1000 V**

The ESD robustness of the distributed amplifier is substantially improved after inserting the distributed ESD protection scheme. The distributed amplifier with the 300-fF ES-DESD protection scheme (DA1) has the HBM ESD level of 5.5 kV and the MM ESD level of 325 V. With the same total parasitic capacitance from ESD protection diodes, the distributed amplifier with the 300-fF DS-DESD protection scheme (DA2) sustains even higher ESD levels, which are more than 8 kV in HBM and 575 V in MM. With larger ESD protection diodes and thus larger parasitic capacitances, the ESD robustness of the ESD-protected distributed amplifier is further improved. Under the same total parasitic capacitance from the ESD protection diodes, distributed amplifier with the DS-DESD protection scheme exhibits higher ESD robustness than the distributed amplifiers with the ES-DESD protection scheme. This measured result has verified that the proposed DS-DESD protection scheme can provide more efficient ESD protection for the distribute amplifier than the ES-DESD protection scheme.

Table 4.3 summarizes the performances of the published CMOS distributed amplifiers compared with the distributed amplifier without ESD protection (DA0), the distributed amplifier with the 300-fF ES-DESD protection scheme (DA1), and the distributed amplifier with the 300-fF DS-DESD protection scheme (DA2). DA1 and DA2 exhibit satisfactory broadband performances and have high ESD robustness simultaneously.

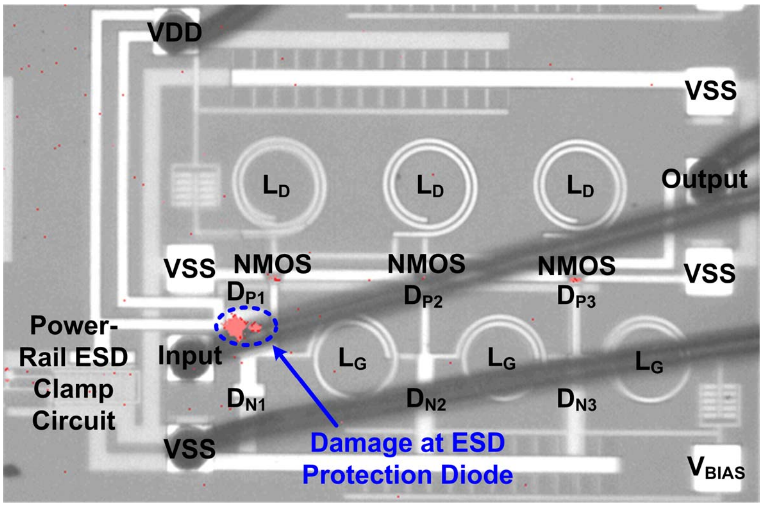
Table 4.3

Comparison With Prior CMOS Distributed Amplifiers

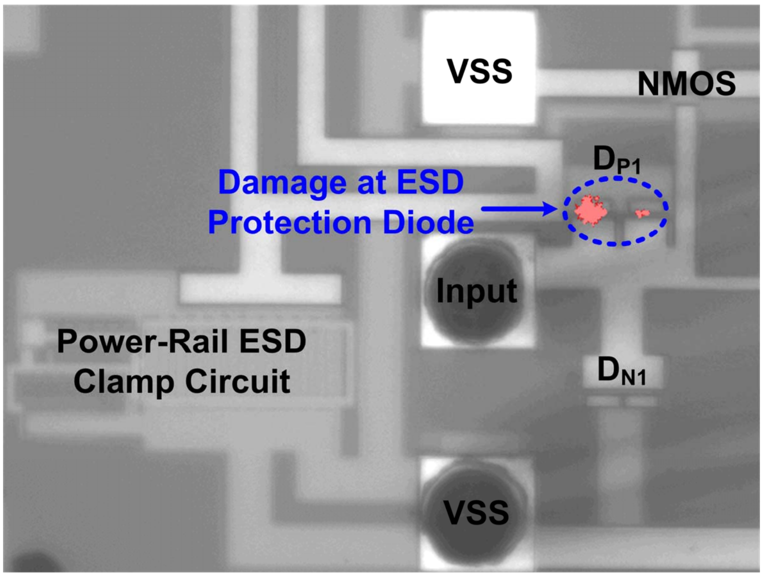
	Technology	Bandwidth (GHz)	S_{21} (dB)	NF (dB)	S_{11} (dB)	S_{22} (dB)	HBM ESD Level (kV)	MM ESD Level (V)
DA0 (Without ESD Protection)	0.25-μm CMOS	1 - 11.4	5 ± 1	4.4 - 5.6	< -10	< -15	0.2	20
DA1 (300-fF ES-DESD)	0.25-μm CMOS	1 - 10	4.7 ± 1	4.9 - 5.7	< -9	< -18	5.5	325
DA2 (300-fF DS-DESD)	0.25-μm CMOS	1 - 9.2	4.9 ± 1.1	5 - 5.6	< -8.5	< -19.5	> 8	575
Ref. [103]	0.8-μm CMOS	0.3 - 3	5 ± 1.2	5.1 - 7	< -6	< -9	N/A	N/A
Ref. [104]	0.6-μm CMOS	0.5 - 4	6.5 ± 1.2	5.3 - 8	< -7	< -10	N/A	N/A
Ref. [105]	0.6-μm CMOS	0.5 - 7.5	5.5 ± 1.2	8.7 - 13	< -6	< -9.5	N/A	N/A
Ref. [106]	0.18-μm CMOS	N/A	5	N/A	< -14	N/A	N/A	N/A
Ref. [107]	0.18-μm CMOS	1 - 10	8 ± 1	N/A	N/A	N/A	N/A	N/A
Ref. [108]	0.18-μm CMOS	0.6 - 22	7.3 ± 0.8	4.3 - 6.1	< -8	< -9	N/A	N/A
Ref. [109]	0.18-μm CMOS	0.5 - 14	10.6 ± 0.9	3.4 - 5.4	< -11	< -12	N/A	N/A

4.4.3. Failure Analysis

After the ESD-protected distributed amplifier was damaged by ESD, failure analysis was performed to investigate the failure mechanism. The photon-emission-microscope (EMMI) pictures in Fig. 4.25 have confirmed that the ESD damage, indicated by the arrow, is located at the first P+/N-well diode D_{P1} after PS-mode ESD stress. During PS-mode ESD tests, ESD current flows through the P+/N-well diodes and the power-rail ESD clamp circuit. During the ESD event, most ESD current flows through the first section of ESD protection circuit, which is the shortest path. This evidence explains why the DS-DESD scheme achieves higher ESD robustness than the ES-DESD scheme.



(a)



(b)

Fig. 4.25. EMMI pictures to show the failure location of ESD damage in the distributed amplifier with the DS-DESD protection scheme (DA2) after 575-V MM PS-mode ESD test. (a) Whole view of DA2. (b) Zoomed-in view of the damaged location at the first P+/N-well D_{P1} in the first ESD protection section.

4.5. Summary

In this chapter, two wideband ESD protection schemes used to protect the distributed amplifier have been reported and successfully verified in a 0.25-μm CMOS process. From the experimental results, the distributed amplifier, employing the ES-DESD protection scheme with 300-fF total parasitic capacitance from the ESD protection diodes on the signal path, has high ESD robustness (5.5-kV HBM ESD level and 325-V MM ESD level) with only little degradation on the wideband RF performance. With the 300-fF DS-DESD protection scheme applied to the distributed amplifier, the ESD robustness is further improved to over 8 kV in HBM and 575 V in MM. Besides, the wideband RF performance is only slightly deteriorated. Hence, the two distributed ESD protection schemes are useful and feasible to co-design the RF performance and ESD robustness of the distributed amplifier for wideband RF applications.

Chapter 5

5-GHz Differential Low-Noise Amplifier With High Pin-to-Pin ESD Robustness in CMOS Technology

In this chapter, on-chip electrostatic discharge (ESD) protection schemes are proposed for narrowband radio-frequency (RF) applications. Five ESD-protected 5-GHz differential low-noise amplifiers (LNAs) are presented with consideration of pin-to-pin ESD protection. The pin-to-pin ESD issue for differential LNAs is addressed for the first time in the literature. The total parasitic capacitances of the ESD protection devices are 300 fF for all ESD protection schemes in this chapter. Fabricated in a 130-nm CMOS process, all LNAs without and with ESD protection consume 10.3 mW under 1.2-V power supply. The reference differential LNA (LNA0) without ESD protection has 16.2-dB power gain and 2.16-dB noise figure at 5 GHz. The first differential LNA (LNA1) with the conventional double-diode ESD protection scheme exhibits the power gain of 17.9 dB and noise figure of 2.43 dB at 5 GHz. The human-body-model (HBM) and machine-model (MM) ESD levels are 2.5 kV and 200 V, respectively. With the same total parasitic capacitance from the ESD protection devices, the second differential LNA (LNA2) with the proposed double silicon-controlled rectifier (SCR) ESD protection scheme achieves 6.5-kV HBM and 500-V MM ESD robustness, 17.9-dB power gain, and 2.54-dB noise figure at 5 GHz. With the proposed ESD bus between the differential input pads, the third ESD-protected differential LNA (LNA3) has 3-kV HBM and 100-V MM ESD robustness, and exhibits 18-dB power gain and 2.62-dB noise figure at 5 GHz. With the proposed cross-coupled SCR ESD protection scheme, the fourth ESD-protected differential LNA (LNA4) has 1.5-kV HBM and 150-V MM ESD robustness, 19.2-dB power gain, and 3.2-dB noise figure at 5 GHz. To improve the whole-chip ESD robustness of the cross-coupled SCR ESD protection scheme, extra double diodes are added with the total parasitic capacitance at each input pad unchanged. With such a design, the fifth ESD-protected differential LNA (LNA5) has 4-kV HBM and 300-V MM ESD robustness, and exhibits 19.1-dB power gain and 3-dB noise figure at 5 GHz. The ESD test results have shown that the pin-to-pin ESD test is the most critical ESD-test pin combination for the conventional double-diode ESD protection scheme. With the proposed ESD protection schemes, the whole-chip ESD robustness, including the pin-to-pin ESD robustness, is significantly improved without degrading RF performance. Experimental results have shown that the ESD protection circuit for LNA can be co-designed with the input matching network to achieve high ESD robustness and excellent RF performance simultaneously [114], [115].

5.1. Background

Radio-frequency integrated circuits (RF ICs) are necessary for all portable electronics devices used for wireless communications. Early RF front-end circuits were implemented by using SiGe or GaAs technologies because of their superior high-frequency characteristics. Recently, the feature size of MOS transistor in CMOS technology has been continuously scaled down to improve its high-frequency characteristics, which makes CMOS processes more attractive to implement RF ICs. With the advantages of high integration capability and low cost for mass production, RF ICs operating in gigahertz frequency bands have been fabricated in CMOS technology. In an RF receiver, low-noise amplifier (LNA) plays a very important role because it is the first stage in the RF receiver. There are several requirements for the performance of LNA. First, the noise figure (NF) of LNA should be minimized because the noise figure of LNA dominates the overall noise figure of the RF receiver. Second, the power gain of LNA should be high enough to suppress the negative effects caused by the noise figures of the following stages in the RF receiver. Moreover, the power consumption of all components in the RF receiver, including LNA, should be minimized to make the RF receiver suitable for portable use.

Differential configuration is popular for LNA design because differential LNA has the advantages of common-mode noise rejection, less sensitivity to substrate noise, supply noise, and bond-wire inductance variation [116]–[122]. In addition, the differential output signals of the differential LNA can be directly connected to the differential inputs of the double balanced mixer.

Electrostatic discharge (ESD), which has become one of the most important reliability issues in IC fabrication, is getting more attention in nanoscale CMOS technology [1]. With the advances of CMOS processes, ESD robustness of CMOS ICs becomes worse and worse because of the thinner gate oxide of MOS transistors. Therefore, ESD protection should be taken into consideration during the design phase of all commercial ICs, especially for RF ICs [2]. Since the LNA is usually connected to the external of RF receiver chip such as the off-chip antenna, on-chip ESD protection circuits are needed for all input pads of the LNA. However, applying ESD protection circuits at the input pads introduce impacts to RF performance. As the operating frequency of RF circuits increases, degradation on RF performance due to the parasitic effects from ESD protection devices/circuits becomes serious. Therefore, the LNA and the ESD protection circuit have to be co-designed to simultaneously optimize the RF performance and ESD robustness.

To characterize the ESD robustness of the IC, several ESD-test pin combinations are specified. Besides PD-mode, PS-mode, ND-mode, and NS-mode ESD-test pin combinations, the pin-to-pin ESD test had been explicitly specified in the ESD-test standards to verify ESD robustness of the differential input stages. During the pin-to-pin ESD test, the ESD stress is applied to one input pin with the other input pin relatively grounded, and all the other pins including all VDD and VSS pins are floating. To provide efficient pin-to-pin ESD protection, the ESD protection device should be turned on quickly with low enough clamping voltage during ESD stresses to protect the thin gate oxides of the differential input transistors. As the gate oxide becomes much thinner in nanoscale CMOS processes, robust ESD protection design against all ESD-test pin combinations, including pin-to-pin ESD stresses, becomes more challenging. However, pin-to-pin ESD protection was not mentioned in the previous works of differential LNA.

In this chapter, six 5-GHz differential LNAs were designed and verified in a 130-nm CMOS process. The reference LNA (LNA0) was designed and fabricated without ESD protection for comparison. The other five differential LNAs were co-designed with the on-chip ESD protection schemes. The first ESD-protected differential LNA (LNA1) is equipped with the conventional double-diode ESD protection scheme. Four novel ESD protection schemes are proposed and applied to the other differential LNAs (LNA2–LNA5). In the differential LNA (LNA2) with the proposed double silicon-controlled rectifier (SCR) ESD protection scheme, a P-type substrate-triggered SCR (P-STSCR) and an N-type substrate-triggered SCR (N-STSCR) are used at each input pad. With the proposed ESD bus between the differential input pads, an ESD clamp device is placed between the ESD bus and VSS in the ESD-protected differential LNA LNA3. Another ESD-protected differential LNA LNA4 utilizes the proposed cross-coupled SCR ESD protection scheme, where the cross-coupled SCR devices are placed between the differential input pads. In the ESD-protected differential LNA LNA5, the double diodes are added along with the cross-coupled SCR devices. The total parasitic capacitances from the ESD protection devices are 300 fF in all the ESD-protected differential LNAs. The pin-to-pin ESD issue for differential LNAs is specially studied clearly in this paper with failure analysis pictures after ESD stresses. Section 5.2 is focused on the LNA design and derivation of equations describing the effects from ESD protection devices on LNA. On-chip ESD protection design for the differential LNA is presented in section 5.3. The experimental results are reported in section 5.4. Moreover, the measured results of the fabricated LNAs in this work are compared with those of the prior CMOS differential LNAs.

5.2. Differential LNA Design

The circuit schematic of the reference differential LNA without ESD protection is shown in Fig. 5.1. The architecture of common-source inductive degeneration is applied to match the source impedance (R_S = 50 Ω) at resonance. The operating frequency of the LNA was originally targeted at 5.2 GHz. Good isolation between the input and output is achieved by using the cascode configuration. Moreover, cascode configuration provides good stability and reduces the Miller effect [123]. The dimensions of the input NMOS transistors M_1 and M_3 (40 μm/0.12 μm) were designed according to the compromise between noise figure and power consumption. For the ESD-protected LNAs, the ESD protection devices were placed at the input pads.

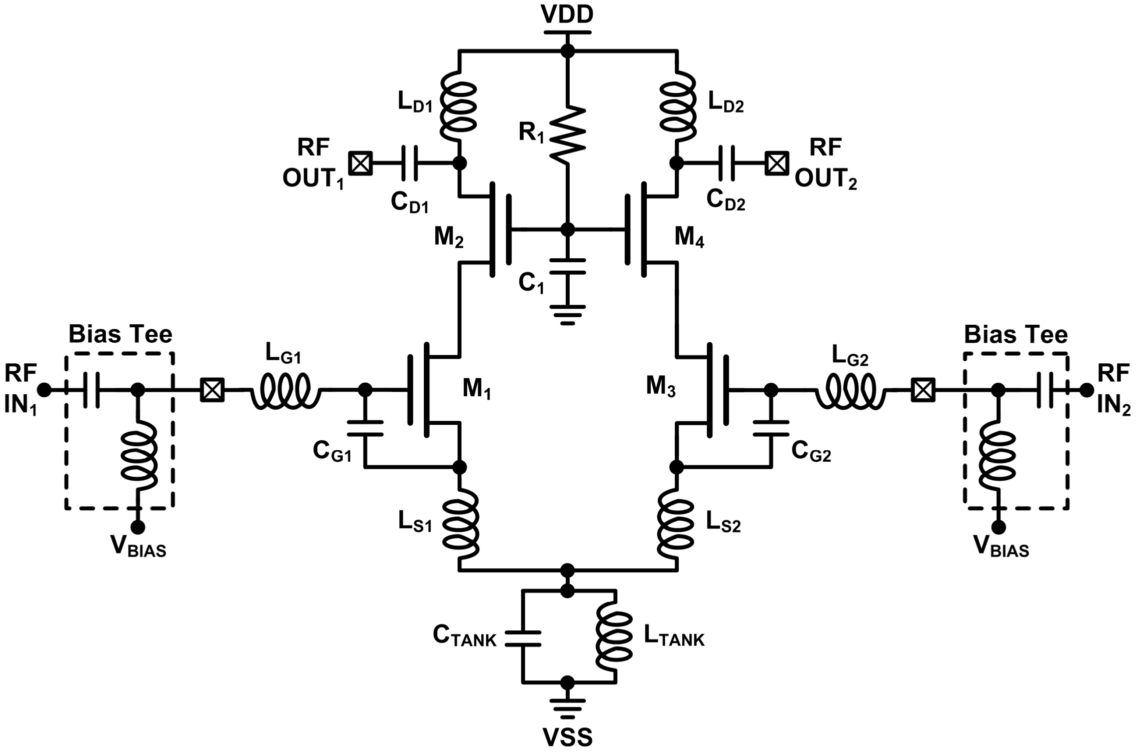
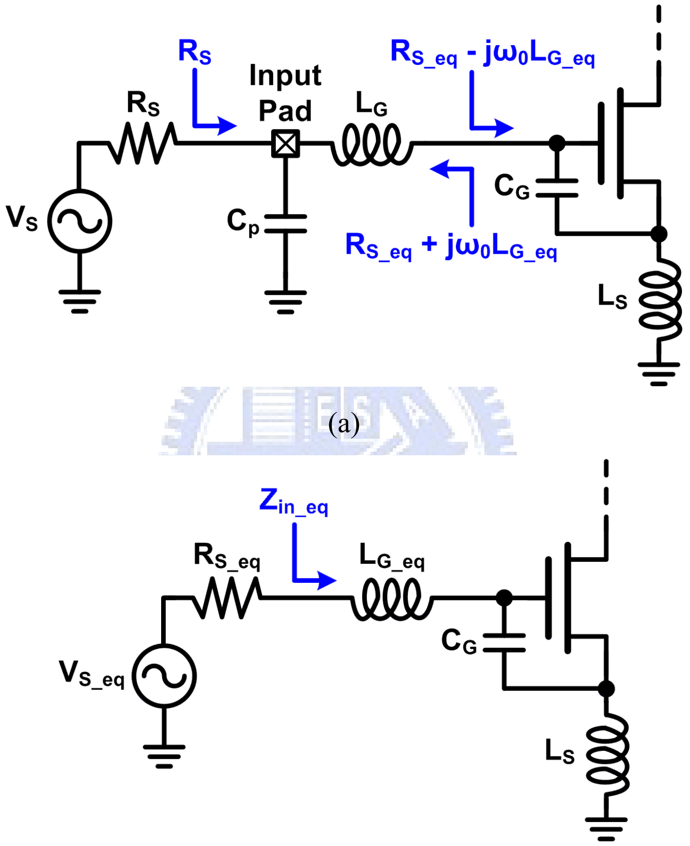


Fig. 5.1. Reference differential LNA (LNA0) without ESD protection.

Fig. 5.2(a) illustrates the input network of the half circuit of the differential ESD-protected LNA under the impedance-matched condition, in which the input pads are equipped with the ESD protection devices. By modeling the parasitic capacitances of the bond pad (C_{pad}) and the ESD protection device (C_{ESD}) as a capacitor (C_p) between the input pad and ground, the input impedance, power gain, and noise figure of the ESD-protected LNA can be derived [124]. C_p is given by

$$C_p = C_{pad} + C_{ESD}\,. \tag{5.1}$$



(b)

Fig. 5.2. (a) Input network of the ESD-protected LNA. (b) Equivalent input network of the ESD-protected LNA at the operating frequency.

By designing the input matching network to resonate at the RF operating frequency ($\omega = \omega_0$), the impedance transformation can be performed to facilitate the analysis. Consequently, the equivalent input network at the operating frequency is obtained and shown in Fig. 5.2(b). The equivalent source impedance seen from the gate terminal of the input NMOS can be expressed by $R_{S\_eq} + j\omega_0 L_{G\_eq}$, where R_{eq} and L_{eq} are

$$R_{S\_eq} = \frac{R_S}{1+\omega_0^2 R_S^2 C_p^2}. \tag{5.2}$$

$$L_{G\_eq} = \frac{L_G - R_S^2 C_p + \omega_0^2 R_S^2 C_p^2 L_G}{1+\omega_0^2 R_S^2 C_p^2}. \tag{5.3}$$

The equivalent input impedance Z_{in_eq} in Fig. 5.2(b) is given by

$$Z_{in\_eq} = \frac{1}{j\omega(C_{gs}+C_G)} + j\omega(L_{G\_eq}+L_S) + \omega_T L_S + r_{g\_NQS}. \tag{5.4}$$

where C_{gs} is the gate-source capacitance of the input NMOS M_1 and M_3, ω_T is the unity-gain angular frequency of M_1 and M_3, and r_{g_NQS} denotes the non-quasi-static (NQS) gate resistance [125]. r_{g_NQS} is expressed by

$$r_{g\_NQS} = \frac{1}{\kappa g_m}. \tag{5.5}$$

where κ is the Elmore constant and g_m is the transconductance of the input NMOS (M_1 and M_3). Input matching is achieved by choosing the source inductance L_S to make the real part of Z_{in_eq} equal to R_{S_eq} at the RF operating frequency. Besides, the imaginary part of Z_{in_eq} needs to be zero, so L_S and gate inductance L_G are used to compensate the capacitance at the gate terminal of M_1 and M_3. After L_S is determined, the remaining capacitive impedance needs to be cancelled by the gate inductance L_G. However, the small C_{gs} of M_1 and M_3 leads to intolerable large inductance for L_G. Therefore, an extra capacitor C_G is added in parallel with C_{gs} to reduce the required L_G.

In Fig. 5.1, the drain inductor L_{D1} (L_{D2}) and drain capacitor C_{D1} (C_{D2}) form the output matching network. After derivation, the power gain (G_T) of the ESD-protected LNA can be expressed by

$$G_T = \frac{R_{load}}{4R_{S\_eq}^2}\left(\frac{\omega_T}{\omega_0}\right)^2. \tag{5.6}$$

where R_{load} is the equivalent load resistance of the LNA, which mainly consists of the equivalent parallel resistance of the drain inductor after impedance transformation. From (5.2) it is known that R_{S_eq} decreases as C_p increases, so the power gain of LNA can be slightly higher with larger C_p at the input node. After the ESD protection devices are added at the input pad, the impedance matching network is re-designed to match the input of the LNA to the source impedance. Therefore, the S-parameters of the ESD-protected differential LNAs will not be degraded as compared with those of the reference differential LNA without ESD protection.

The approximate expression for the noise figure (*NF*) of the ESD-protected LNA is given by

$$NF \simeq 1+\left(\frac{\omega_0}{\omega_T}\right)^2 \frac{\gamma}{\alpha} g_m R_{S\_eq} + \left(\frac{\omega_0}{\omega_T}\right)^2 \frac{\gamma}{\alpha}\frac{2}{\kappa} + \frac{\alpha\delta}{\kappa g_m R_{S\_eq}} . \tag{5.7}$$

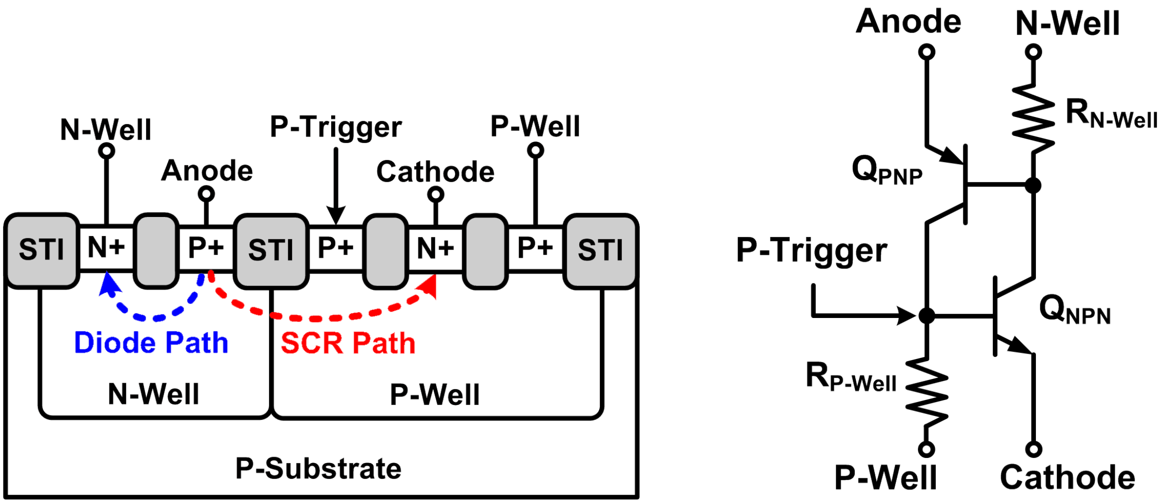
where α, γ, and δ are transistor parameters. With larger C_p and thus smaller R_{S_eq}, the last term can not be neglected and it becomes larger to increase the noise figure of LNA. Thus, the noise figure will be increased after the ESD protection devices are added at the input pads.

In this work, M_1–M_4 utilize multi-finger layout structure to reduce the gate resistance, which leads to better noise performance. The gate voltages of M_2 and M_4 are biased to VDD through the resistor R_1. The capacitor C_1 acts as a decoupling capacitor. The LC-tank consisting of L_{TANK} and C_{TANK} is used to enhance the common-mode rejection. All of the inductors are the on-chip spiral inductors implemented by the top metal, and all of the capacitors are realized by the on-chip metal-insulator-metal (MIM) capacitors. The aforementioned active and passive devices are fully integrated in the experimental test chip fabricated in a 130-nm CMOS process. In order to verify the effectiveness of the on-chip ESD protection circuits at the input pads, the AC coupling capacitor between the input pad and the gate inductor is not realized in the test chip, because the AC coupling capacitor connected to the input pad can block some ESD energy when the input pad is stressed by ESD. Thus, the off-chip bias tee is needed to combine the RF input signal and the DC bias (0.65 V) at the input node during RF performance measurement.

5.3. ESD Protection Design for Differential LNA

5.3.1. Substrate-Triggered Silicon-Controlled Rectifier (SCR)

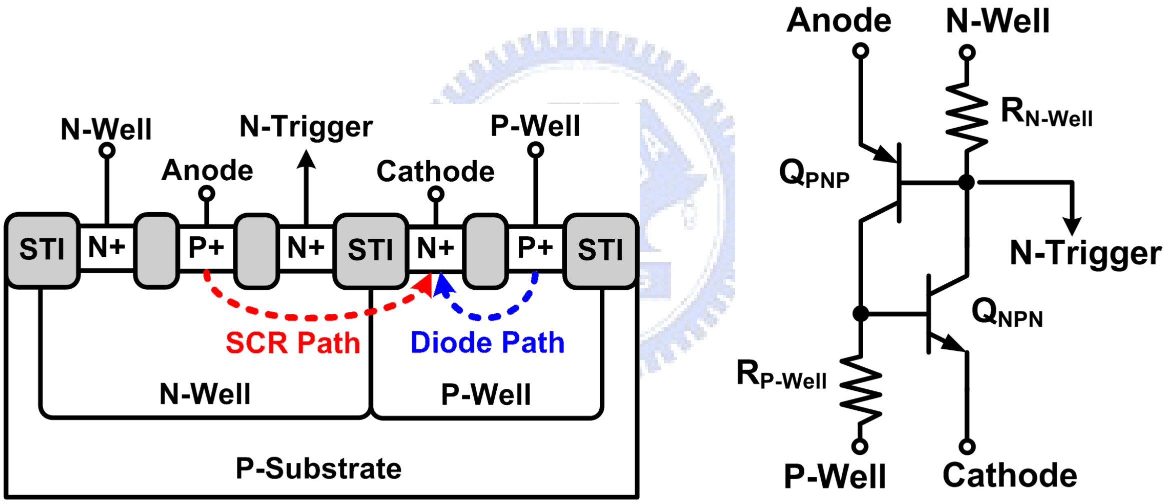
Silicon-controlled rectifier (SCR) had been demonstrated to be suitable for ESD protection design for RF ICs, because it has both high ESD robustness and low parasitic capacitance under a small layout area [65], [81], [122], [126]. Besides, SCR had been demonstrated to be the optimum ESD protection device for high-speed differential I/O pads [127]. The P-type substrate-triggered SCR (P-STSCR) and N-type substrate-triggered SCR (N-STSCR) are utilized in this chapter to protect the LNA against ESD stresses. The cross-sectional view of the P-STSCR is shown in Fig. 5.3(a). The SCR path exists among the P+ diffusion (anode), N-well, P-well, and N+ diffusion (cathode). The equivalent circuit of the P-STSCR is shown in Fig. 5.3(b), which consists of a parasitic vertical PNP BJT and a parasitic lateral NPN BJT. The PNP BJT Q_{PNP} is formed by the P+ diffusion (anode), N-well, and P-well. The NPN BJT Q_{NPN} is formed by the N-well, P-well, and N+ diffusion (cathode). When the P-STSCR is used as the ESD protection device at the input pad, the cathode and P-well are connected to VSS, while the anode and N-well are connected to the input pad and VDD, respectively. In this configuration, the P+/N-well junction can be used to protect the input pad against PD-mode ESD stresses, and its parasitic capacitance is added at the input pad. To quickly turn on the P-STSCR during ESD stresses, the P+ trigger diffusion (in the P-well region) was added between the anode and cathode. An extra ESD detection circuit is designed to inject trigger current to the P-trigger node during ESD stresses. During PS-mode ESD stress, the trigger current is designed to be injected to the P-trigger node from the ESD detection circuit. After the voltage drop across the P-well resistance ($R_{P\text{-}Well}$) is larger than the cut-in voltage of the base-emitter junction of Q_{NPN}, Q_{NPN} is turned on to conduct ESD current. The collector current of Q_{NPN} leads to voltage drop across the N-well resistance ($R_{N\text{-}Well}$). When the voltage drop across $R_{N\text{-}Well}$ is larger than the cut-in voltage of the base-emitter junction of Q_{PNP}, Q_{PNP} is turned on to conduct ESD current, which causes more collector current of Q_{NPN} due to the current gain of BJT. The regenerative positive-feedback mechanism results in the great current handing capability of SCR, and makes SCR very robust against ESD stresses. With the low clamping voltage of SCR, the ESD current path between the input pad and VSS is provided to efficiently protect the gate oxide of MOS transistors.



(a) (b)

Fig. 5.3. (a) Cross-sectional view of P-type substrate-triggered silicon-controlled rectifier (P-STSCR). (b) Equivalent circuit of P-STSCR.

The cross-sectional view and equivalent circuit of the N-STSCR are shown in Fig. 5.4(a) and (b), respectively. The SCR path exists among the P+ diffusion (anode), N-well, P-well, and N+ diffusion (cathode). When the N-STSCR is used to protect the input pad, the anode and N-well are connected to VDD, while the cathode and P-well are connected to the input pad and VSS, respectively. In this configuration, the N+/P-well junction can be used to protect the input pad against NS-mode ESD stresses, and its parasitic capacitance is added at the input pad. To quickly turn on the N-STSCR during ESD stresses, the N+ trigger diffusion (in the N-well region) was added between the anode and cathode. During ND-mode ESD stress, the trigger current is design to be drawn from the N-trigger node by an extra ESD detection circuit to turn on the N-STSCR. The N-STSCR also has low clamping voltage, and is quite robust against ESD stresses. Hence, the input pad is protected by the N-STSCR under ND-mode ESD stresses.



(a) (b)

Fig. 5.4. (a) Cross-sectional view of N-type substrate-triggered silicon-controlled rectifier (N-STSCR). (b) Equivalent circuit of N-STSCR.

The latchup issue must be eliminated when SCR is used as the ESD protection device. The DC I–V curves of the stand-alone SCR device in this 130-nm CMOS process were measured using Tektronics 370B curve tracer under different temperatures. As shown in Fig. 5.5, the holding voltages of the stand-alone SCR device under 25 °C, 85 °C, and 125 °C are 2.84 V, 2.58 V, and 2.38 V, respectively. Since the holding voltage of the SCR device is higher than the power-supply voltage of 1.2 V, the SCR device can be safely used for ESD protection without latchup issue. Fig. 5.5 shows that the stand-alone SCR device has the trigger voltage of more than 10 V, which is too high to protect the LNA. Thus, the trigger voltage needs to be reduced by injecting trigger current into the P-STSCR or drawing trigger current from the N-STSCR. With the ESD detection circuit in this work, the trigger voltage of SCR devices can be substantially reduced to efficiently protect the LNA against ESD damages.

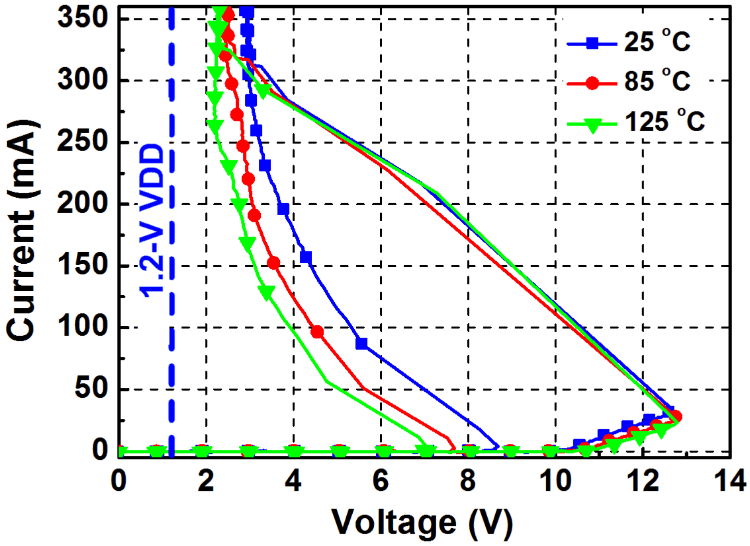


Fig. 5.5. Measured DC I–V curves of the stand-alone SCR device in a 130-nm CMOS process under different temperatures.

5.3.2. Power-Rail ESD Clamp Circuit With SCR

In the ESD-protected differential LNAs, the power-rail ESD clamp circuits are used to provide ESD current paths between VDD and VSS. As shown in Fig. 5.6, the power-rail ESD clamp circuit includes the P-STSCR and the ESD detection circuit. The anode and N-well of the P-STSCR are connected to VDD, while the cathode and P-well of the P-STSCR are connected to VSS. The ESD detection circuit consists of an RC timer and an inverter. The resistor R_2 and capacitor C_2 form the RC timer with the time constant of 0.3 μs, which can distinguish the ESD transients from the normal circuit operating conditions. During normal circuit operating conditions, the node between R_2 and C_2 is charged to high potential (VDD). Since NMOS M_N is turned on and PMOS M_P is turned off, the P-trigger node is tied to VSS and no trigger current is injected. Thus, the P-STSCR is kept off during normal circuit operating conditions. During ESD stresses, the ESD energy is coupled to VDD quickly. With the RC delay provided by R_2 and C_2, the gate voltages of M_P and M_N are initially biased at low potential (~0 V). Therefore, M_P is turned on to inject trigger current into the P-trigger node. As a result, the P-STSCR is turned on to provide ESD current path between VDD and VSS. Moreover, the voltage between VDD and VSS is clamped by the P-STSCR.

The power-rail ESD clamp circuit is placed between VDD and VSS, which does not contribute any parasitic capacitance to the input nor output pads of RF ICs. Thus, the size of the P-STSCR in the power-rail ESD clamp circuit is not limited by the specification of parasitic capacitance at the RF I/O pad.

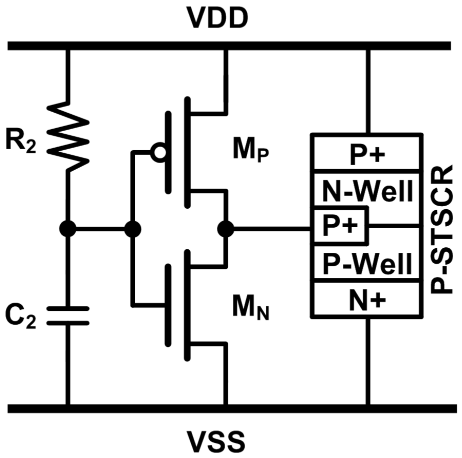


Fig. 5.6. Power-rail ESD clamp circuit realized with P-STSCR.

5.3.3. Conventional Double-Diode ESD Protection Scheme

In the five ESD-protected differential LNAs, the total parasitic capacitances at each input pad are all 300 fF to investigate their ESD robustness. With the same total parasitic capacitance from ESD protection devices at the input pad, the RF performance and ESD robustness of these five differential LNAs with different ESD protection schemes can be compared.

The ESD protection schemes for each differential LNA in this chapter are listed in Table 5.1. The first ESD-protected differential LNA (LNA1) is equipped with the conventional double-diode ESD protection scheme, whose schematic is shown in Fig. 5.7. The double-diode ESD protection scheme includes a P+/N-well diode (D_P) between each differential input pad and VDD, and an N+/P-well diode (D_N) between VSS and each differential input pad. To achieve the total parasitic capacitance of 300 fF contributed by these two ESD protection diodes at each input pad, two parallel P+/N-well diodes with the dimensions of 16 μm × 5 μm and two parallel N+/P-well diodes with the dimensions of 19.2 μm × 5 μm were used. To co-design the LNA and ESD protection circuit, the source inductances (L_{S1} and L_{S2}) and gate inductances (L_{G1} and L_{G2}) were adjusted to achieve input matching at RF operating frequency after the addition of ESD protection diodes.

Table 5.1

ESD Protection Scheme of Each Differential LNA

Differential LNA	300-fF ESD Protection Scheme
LNA0	No ESD Protection
LNA1	Double Diode
LNA2	Double SCR
LNA3	ESD Bus
LNA4	Cross-Coupled SCR
LNA5	Double Diode + Cross-Coupled SCR

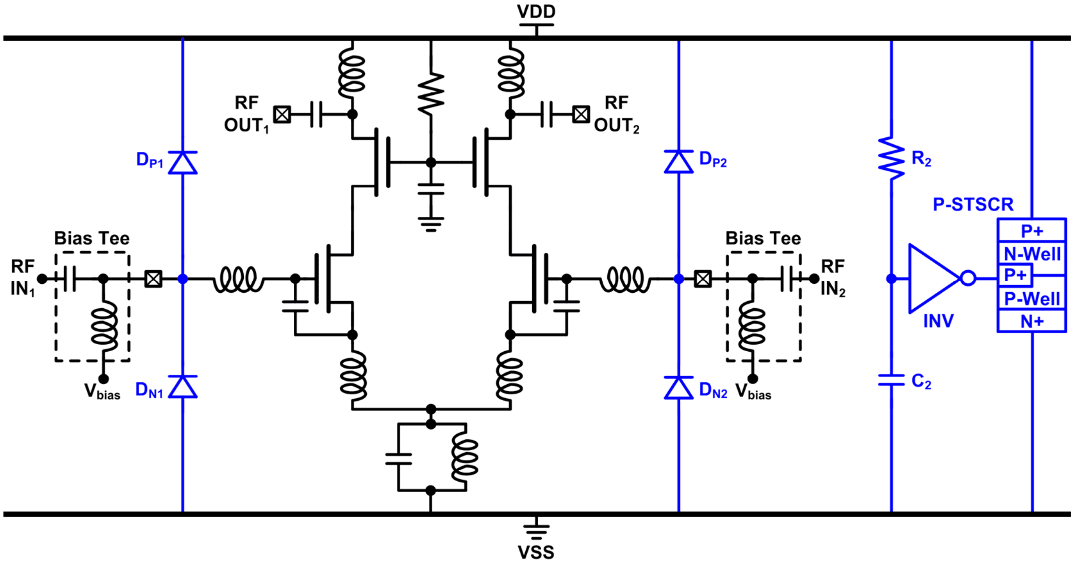


Fig. 5.7. Differential LNA (LNA1) with the conventional double-diode ESD protection scheme.

5.3.4. Proposed Double-SCR ESD Protection Scheme

The circuit schematic of the LNA (LNA2) with the proposed double-SCR ESD protection scheme is shown in Fig. 5.8. The P+/N-well diodes and N+/P-well diodes in LNA1 with double-diode ESD protection scheme are replaced with the N-STSCRs and P-STSCRs, respectively. To meet the requirement of 300-fF total parasitic capacitance at each input pad, the anode diffusion size of the P-STSCR and the cathode diffusion size of the N-STSCR are 60 μm × 2.4 μm and 60 μm × 2.7 μm, respectively. Similarly, the input matching network was co-designed with the SCRs to accomplish satisfaction on RF performance after ESD protection circuit was inserted. Since the P-STSCR$_1$ and P-STSCR$_2$ are the same type of device as that used in the power-rail ESD clamp circuit, the ESD detection circuit in the power-rail ESD clamp circuit can also serve as the ESD detection circuit for the P-STSCRs at each input pad. To realize the ESD detection circuit for the N-STSCR, the inverter INV_2 was cascaded to the inverter INV_1, which is a part of the ESD detection circuit for P-STSCR. With the RC delay provided by the RC timer at the input node of INV_1, the input of INV_1 is initially at low potential (~0 V), which leads to the high potential (VDD) at the input of INV_2 during ESD stresses. Thus, the NMOS in INV_2 is turned on to draw trigger current to turn on the N-STSCR during ESD stresses. During normal circuit operating conditions, the outputs of INV_1 and INV_2 are at low potential (0 V) and high potential (1.2 V), respectively. Consequently, the five substrate-triggered SCRs in LNA2 are kept off.

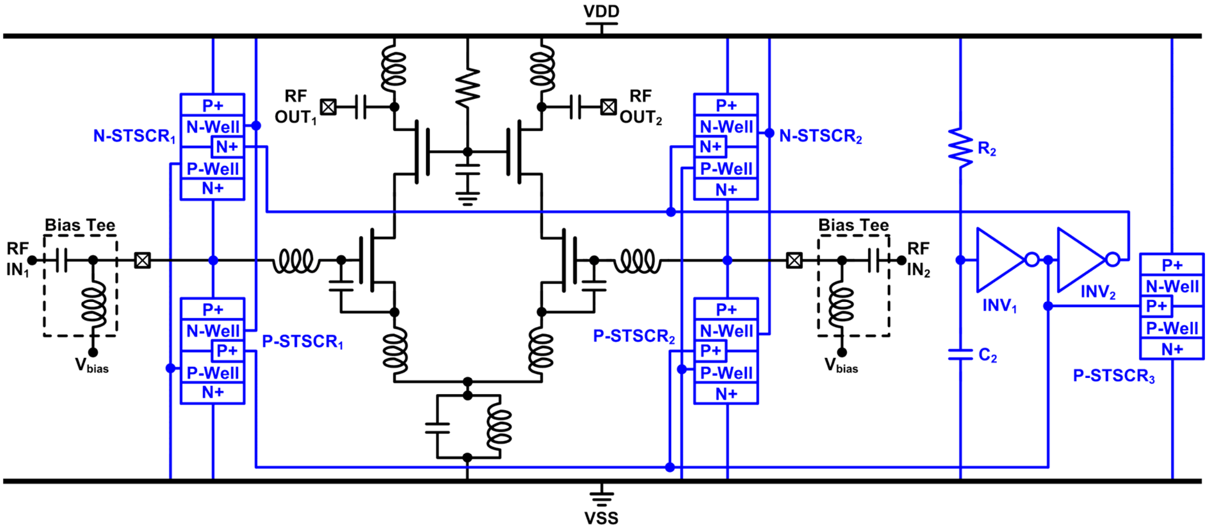


Fig. 5.8. Differential LNA (LNA2) with the proposed double-SCR ESD protection scheme.

5.3.5. Proposed ESD Protection Design With ESD Bus

The circuit schematic of differential LNA (LNA3) with the proposed ESD bus is shown in Fig. 5.9. An ESD bus and the $P\text{-}STSCR_1$ are inserted between the differential input pads and VDD. The anode of $P\text{-}STSCR_1$ is connected to the ESD bus with its cathode grounded. Since the power-rail ESD clamp circuit is usually not be able to be realized nearby the internal circuits, applying the ESD bus with an ESD clamp device next to the differential input pads can effectively reduce voltage across the routing resistances along the VDD and VSS lines during ESD stresses. With lower clamp voltage along the ESD current path, the differential LNA can be protected more efficiently. A P+/N-well diode (D_P) is connected between each input pad and the anode of $P\text{-}STSCR_1$, whereas an N+/P-well diode (D_N) is connected between VSS and each input pad. With the N-well of $P\text{-}STSCR_1$ directly connected to VDD, ESD current paths from the input pads to VDD can be established by

D_{P1}/D_{P2} and the P+/N-well diode in P-STSCR$_1$. Besides, a power-rail ESD clamp circuit was also designed to provide ESD current path between VDD and VSS to achieve comprehensive whole-chip ESD protection. To meet the requirement of 300-fF total parasitic capacitance at each input pad, two parallel P+/N-well diodes with the dimensions of 16 μm × 5 μm and two parallel N+/P-well diodes with the dimensions of 19.2 μm × 5 μm were used. The dimensions of P+/N-well diodes and N+/P-well diodes are identical to those in LNA1 because the ESD bus is an AC ground node during normal circuit operating conditions. Therefore, the parasitic capacitance of P-STSCR$_1$ is not contributed to the input pad. The anode diffusion size of P-STSCR$_1$ is 60 μm × 2.4 μm. During ESD stresses, when ESD voltage is coupled to VDD, the ESD detection circuit will inject trigger current to turn on P-STSCR$_1$ and P-STSCR$_2$. Under normal circuit operating conditions, the output of inverter is kept at low potential (0 V) to turn off P-STSCR$_1$ and P-STSCR$_2$.

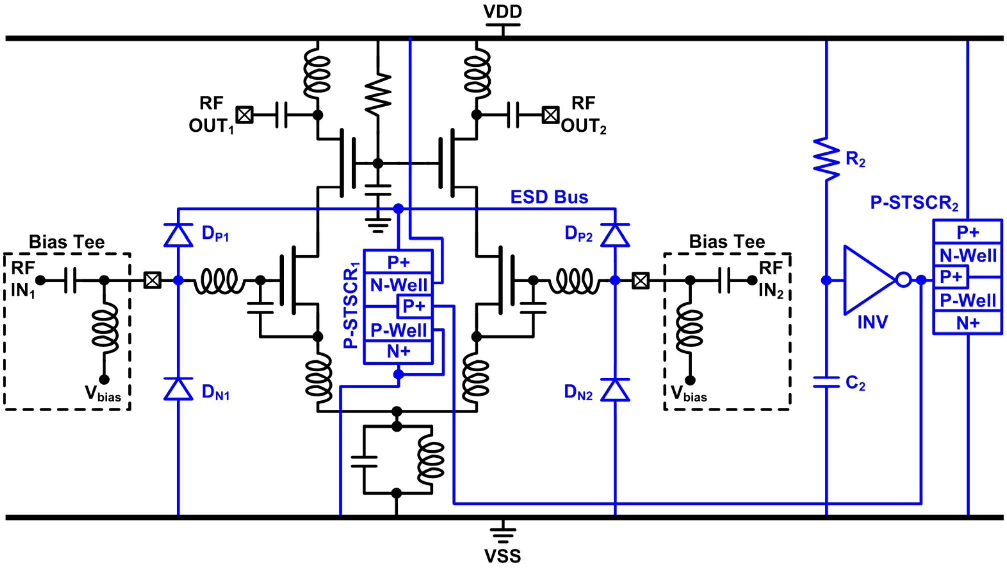


Fig. 5.9. Differential LNA (LNA3) with the proposed ESD bus.

5.3.6. Proposed ESD Protection Design With Cross-Coupled SCR

The fourth ESD-protected differential LNA (LNA4) is realized with the cross-coupled SCR devices. In the conventional double-diode ESD protection scheme, a P+/N-well diode (D_P) and an N+/P-well diode (D_N) is used for each input pad. As shown in Fig. 5.10, when the P+/N-well diode for input pad RF IN$_1$ is put together with the N+/P-well diode for input pad RF IN$_2$, an SCR path P-STSCR$_1$ can be established from RF IN$_1$ to RF IN$_2$ without any cost. Similarly, another SCR path P-STSCR$_2$ can be established from RF IN$_2$ to RF IN$_1$ by putting the other P+/N-well diode and N+/P-well diode together.

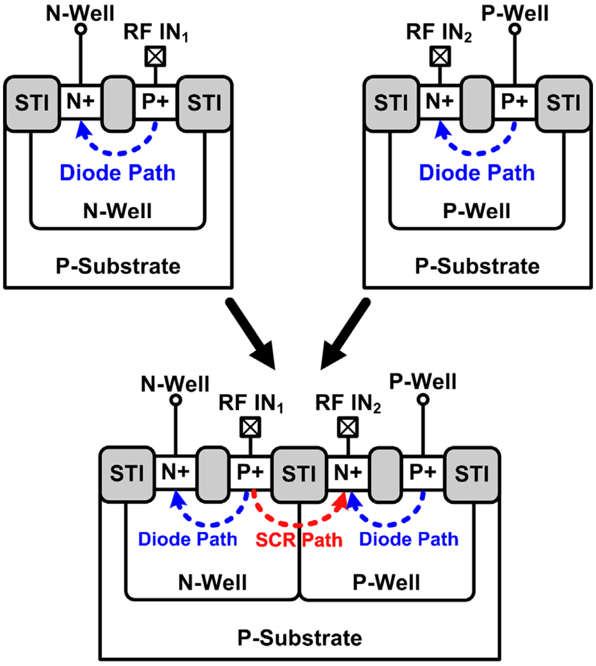


Fig. 5.10. Establishing the SCR path between the differential input pads by putting the P+/N-well diode for one input pad and the N+/P-well diode for the other input pad together.

Fig. 5.11 shows the circuit schematic of the ESD-protected differential LNA (LNA4) with the proposed cross-coupled SCR devices. To meet the requirement of 300-fF total parasitic capacitance at each input pad, the anode and cathode diffusion sizes of P-STSCR$_1$ and P-STSCR$_2$ are all 60 µm × 2.4 µm. In this ESD protection scheme, the ESD current paths under PD-, NS-, PS-, and ND-mode ESD tests are provided by the P+/N-well diode, N+/P-well diode, and the power-rail ESD clamp circuit. During the pin-to-pin ESD tests, the ESD current paths between the differential input pads are provided by the cross-coupled SCR devices P-STSCR$_1$ and P-STACR$_2$. The only effort needed is inserting the P+ trigger diffusions into the P-STSCRs between the differential input pads and connecting them to the output of the ESD detection circuit in the power-rail ESD clamp circuit. By layout modification, extra ESD current paths against pin-to-pin ESD stresses are formed in this ESD protection scheme without any parasitic capacitance overhead at the input pad.

In another design of LNA5, the 300-fF parasitic capacitance is divided into two parts. Based on the design concept of LNA4, 150-fF parasitic capacitance is allocated to the cross-coupled SCR devices between the differential input pads. The other 150-fF parasitic capacitance is realized by the conventional double diodes at each input pad. Fig. 5.12 shows the circuit schematic of LNA5. Even though the P-STSCR as the input pad is separated from the D_P and D_N, the parasitic P+/N-well and N+/P-well diodes within it can still provide ESD current path in parallel with D_P and D_N, respectively. For each input pad, D_P is realized with the dimensions of 16 μm × 5 μm, whereas D_N is realized with the dimensions of 19.2 μm × 5 μm were used. The anode and cathode diffusion sizes of P-STSCR$_1$ and P-STSCR$_2$ are all 30 μm × 2.4 μm. Since two of ESD protection schemes are merged in LNA5, the dimensions of D_P, D_N, and P-STSCR at the input pad are only half of those in LNA1 and LNA4.

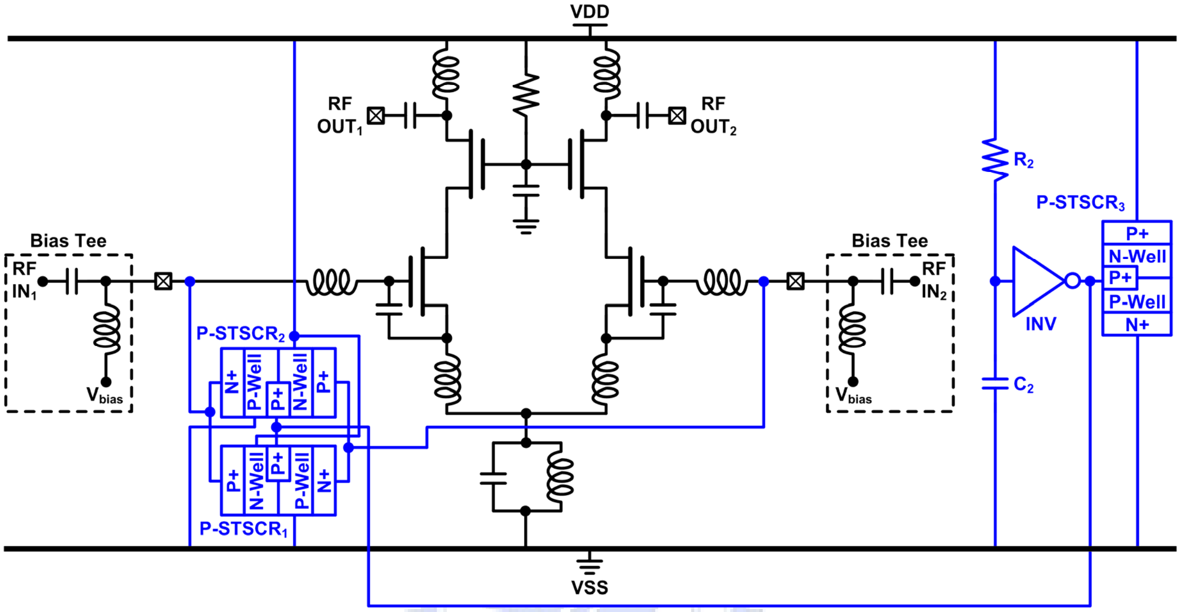


Fig. 5.11. Differential LNA (LNA4) with the proposed cross-coupled SCR devices.

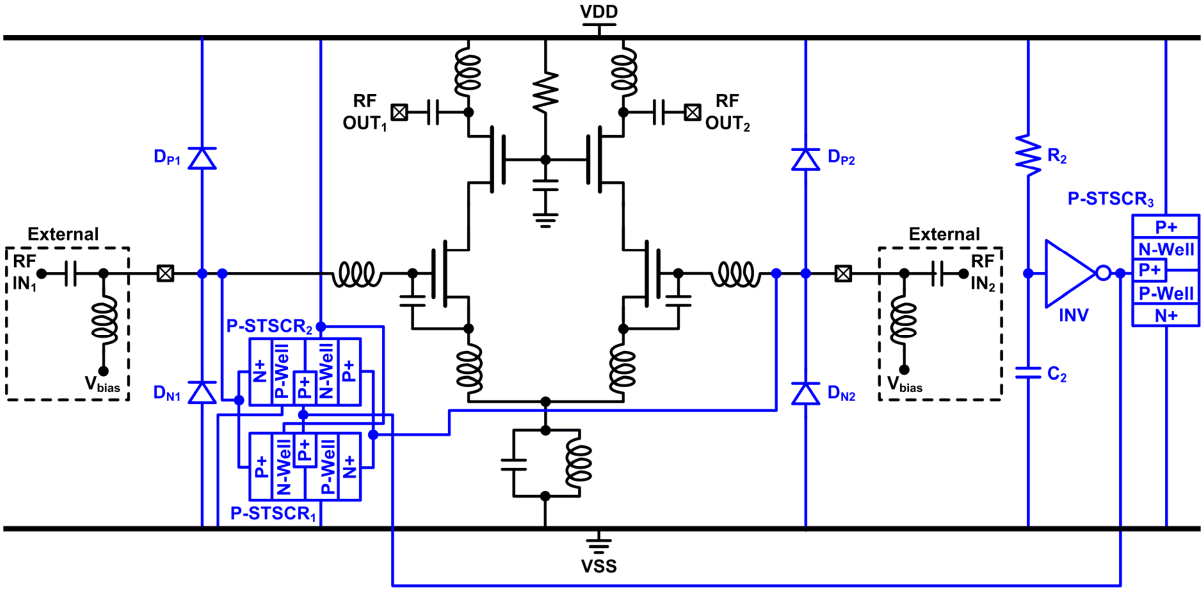


Fig. 5.12. Differential LNA (LNA5) with the proposed cross-coupled SCR devices and double diodes.

With the properly designed ESD protection schemes, all of the SCRs can be kept off during normal circuit operating conditions. When the ESD-protected LNA is zapped by ESD, ESD detection circuits can effectively turn on the SCRs in time to protect the core LNAs.

5.3.7. Simulated RF Performance of LNA Without and With ESD Protection

After the ESD protection scheme is applied to the differential LNA, the passive impedance matching network is re-designed to match the input and output of the LNA to the source impedance (50 Ω) with the matching structure unchanged. The dimensions of the cascoded NMOS transistors in the six LNAs are identical. Only the dimensions of the passive devices in the matching networks are fine tuned. For the LNA, the S-parameters and noise figure are the main factors to determine RF performance. The simulations on RF performance metrics of the LNAs with and without ESD protection were performed to acquire preliminary insight into the effects of ESD protection circuit on RF performance. Since the ESD protection devices are realized at both differential input pads, the common-mode rejection ratio (CMRR) will not be degraded after the ESD protection scheme is applied to the differential LNA.

The simulated S_{21}-parameters (power gain) of these six LNAs are compared in Fig. 5.13. At 5.2 GHz, the reference differential LNA (LNA0) without ESD protection exhibits the power gain of 17.7 dB, whereas the five ESD-protected differential LNAs have the power gains of more than 19 dB. The slight increase in power gain can be explained by (5.6). Adding the ESD protection device increases C_p in (5.1), and R_{S_eq} in (5.2) decreases as C_p increases. Thus, the power gain of LNA can be slightly higher after the capacitive ESD protection devices are added at the input pad.

The simulated S_{11}-parameters (input reflection) of the six LNAs are shown in Fig. 5.14. The reference differential LNA (LNA0) achieves the best input matching, where the S_{11}-parameter is less than -40 dB at 5.2 GHz. The five ESD-protected differential LNAs (LNA1–LNA5) still exhibit good input matching (S_{11} < -24 dB) after the ESD protection devices are added at each input pad. By incorporating the parasitic capacitance of the ESD protection device into the input matching network, the input of the ESD-protected LNA can be matched to the source impedance without altering the operating frequency. Fig. 5.15 shows the simulated S_{22}-parameters (output reflection) of the six LNAs. Since the output of the LNA is usually connected to the succeeding stage within the RF receiver, ESD protection is not required for the output of the LNA. Without ESD protection scheme at the output node, the output matching of the six LNAs are almost identical. The S_{22}-parameters of the six LNAs are less than -23 dB at 5.2 GHz.

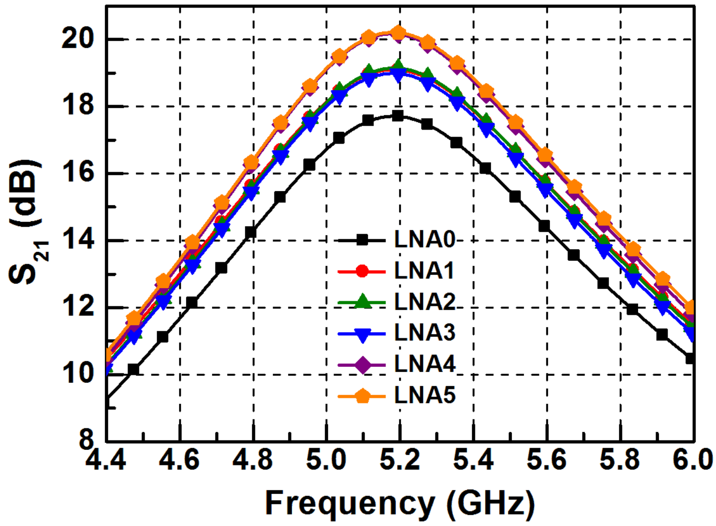


Fig. 5.13. Simulated S_{21}-parameters (power gain) of the reference differential LNA (LNA0) and the five ESD-protected differential LNAs (LNA1–LNA5).

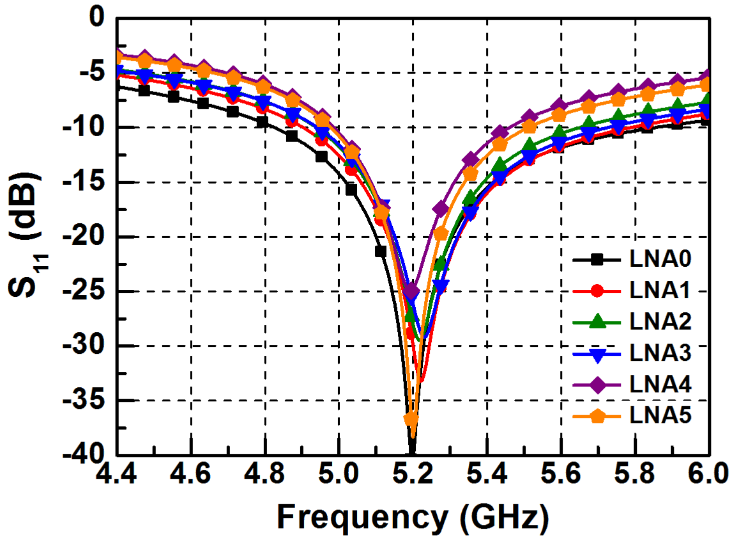


Fig. 5.14. Simulated S_{11}-parameters (input reflection) of the reference differential LNA (LNA0) without ESD protection and the five ESD-protected differential LNAs (LNA1–LNA5).

As shown in Fig. 5.16, the simulated S_{12}-parameters (reverse isolation) of the six LNAs are all less than -31 dB, because good reverse isolation one of the features in cascode configuration. With the LNA and ESD protection co-designed, excellent S-parameters can be maintained after the ESD protection circuit is applied.

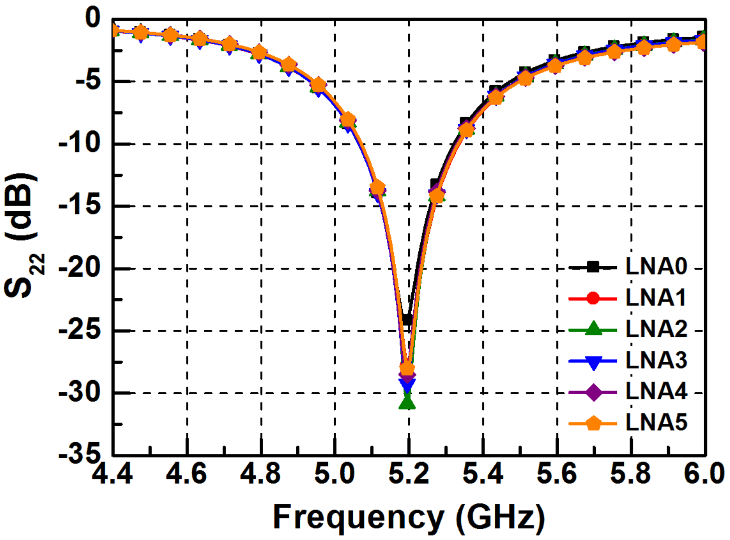


Fig. 5.15. Simulated S_{22}-parameters (output reflection) of the reference differential LNA (LNA0) without ESD protection and the five ESD-protected differential LNAs (LNA1–LNA5).

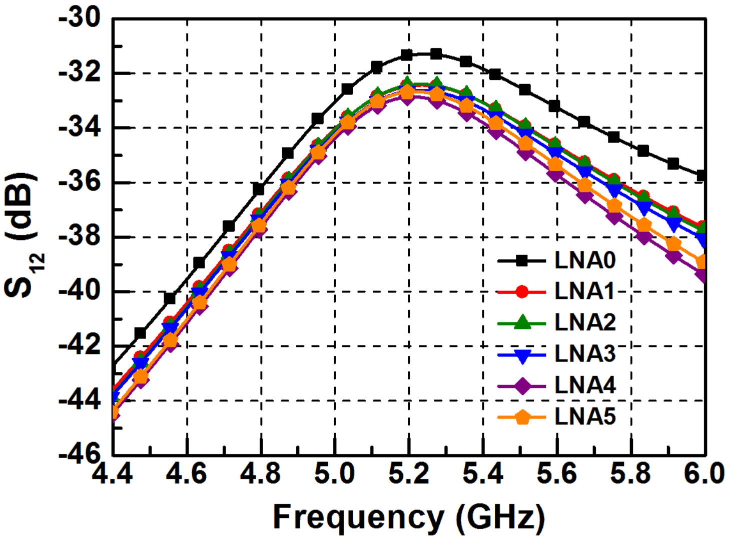


Fig. 5.16. Simulated S_{12}-parameters (reverse isolation) of the reference differential LNA (LNA0) without ESD protection and the five ESD-protected differential LNAs (LNA1–LNA5).

Fig. 5.17 compares the simulated noise figures of the six differential LNAs. After the ESD protection devices are placed at the input pad, the noise figure is increased 0.5 dB or more. The reference LNA (LNA0) exhibits the noise figure of only 1.48 dB at 5.2 GHz. Among the ESD-protected differential LNAs, LNA1 has the lowest noise figure, which is 2.03 dB at 5.2 GHz. The highest noise figure appears in LNA4, which is 2.3 dB at 5.2 GHz. Although good S-parameters can be achieved by LNA and ESD protection co-design, the noise figure is inevitably degraded and can not be compensated in the ESD-protected LNA.

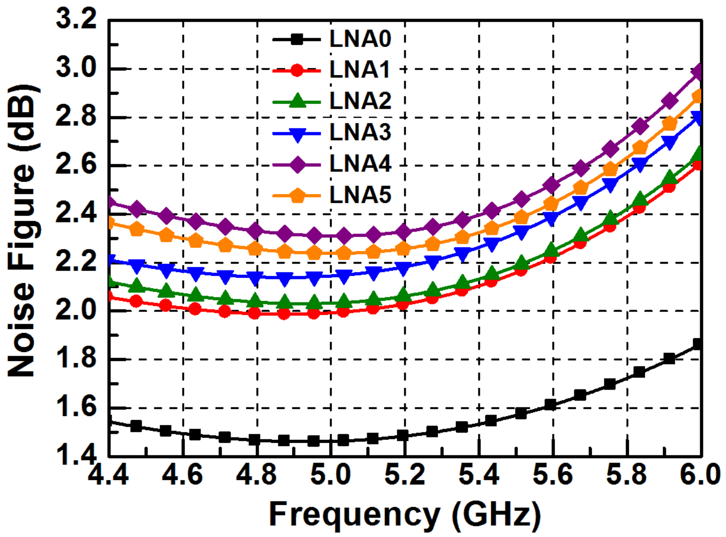


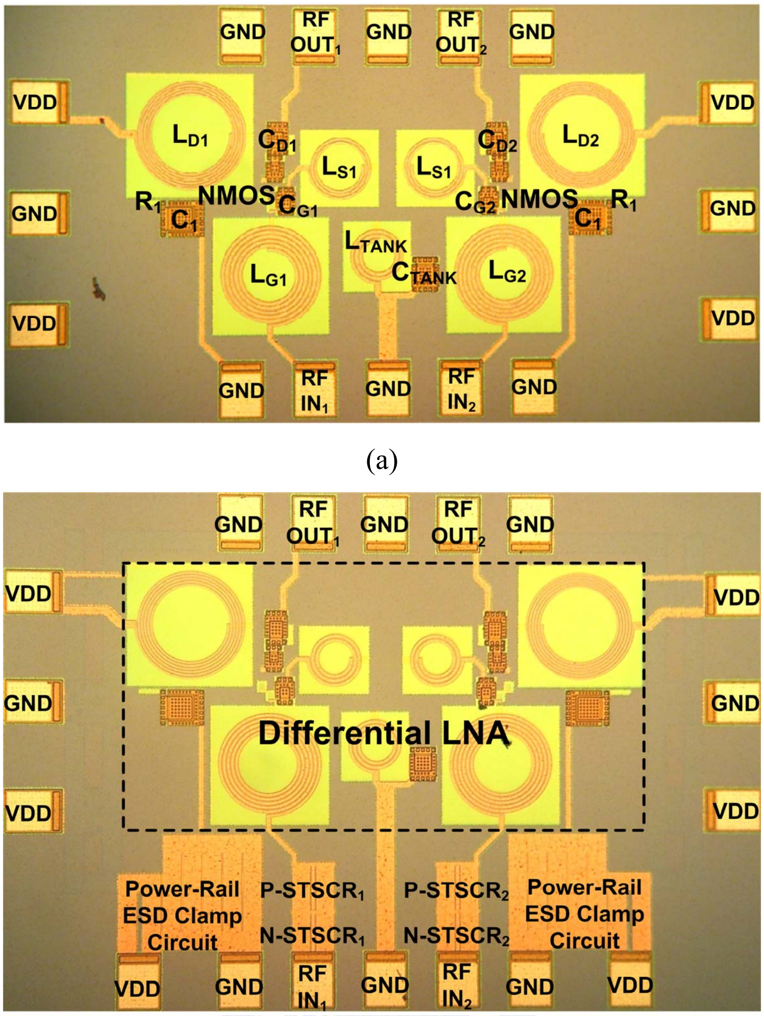
Fig. 5.17. Simulated noise figures of the reference differential LNA (LNA0) without ESD protection and the five ESD-protected differential LNAs (LNA1–LNA5).

5.4. Experimental Results

The reference differential LNA (LNA0) without ESD protection and the other five ESD-protected differential LNAs (LNA1–LNA5) had been fabricated in the same experimental test chip in a 130-nm CMOS process. The chip micrographs of LNA0 and LNA2 are shown in Fig. 5.18(a) and (b), respectively. The reference LNA differential occupies the area of 1070 μm × 630 μm, and the circuit area of each ESD-protected LNA is 1090 μm × 750 μm. The chip micrographs of the six LNAs (LNA0–LNA5) are shown in Fig. 5.19. On-wafer measurements were performed to characterize the RF performance and ESD robustness. Each LNA consumes 10.3 mW under 1.2-V power supply. Since the five whole-chip ESD protection schemes do not consume any DC power, the reference differential LNA and the ESD-protected differential LNAs have identical power consumption. In the following subsections, the measured RF performances, including the S-parameters, noise figures, and third-order intercept points (IP3) of the six fabricated LNAs will be reported and compared. Moreover, the human-body-model (HBM) and machine-model (MM) ESD levels of the LNAs will be evaluated and discussed. The failure mechanism under ESD stresses will also be investigated with failure analysis.

5.4.1. Measured RF Performance

To measure the S-parameters of the fabricated differential LNAs, four-port S-parameter measurement was performed by using the ground-signal-ground-signal-ground (G-S-G-S-G)



(a)

(b)

Fig. 5.18. Chip micrographs of (a) the reference differential LNA (LNA0) without ESD protection, and (b) the differential LNA (LNA2) with the proposed double-SCR ESD protection scheme.

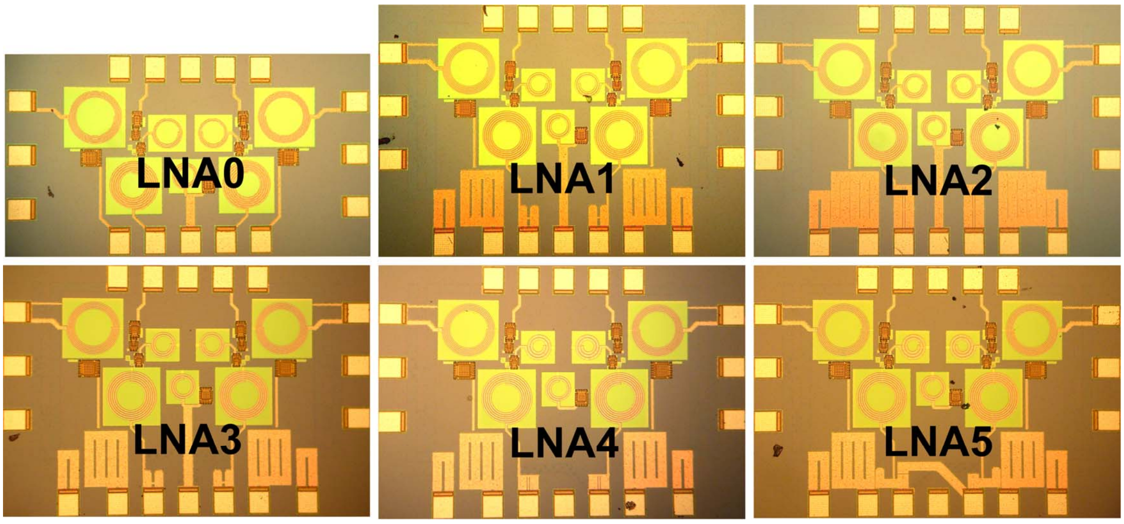


Fig. 5.19. Chip micrographs of the reference differential LNA (LNA0) without ESD protection and the five ESD-protected differential LNAs (LNA1–LNA5).

probes and Agilent E8361A network analyzer. The measurement system is capable of converting the measured four-port S-parameters to the differential two-port S-parameters. Fig. 5.20 compares the measured S_{21}-parameters (power gains) of the six fabricated LNAs. According to the measured results, the six fabricated differential LNAs have their best S-parameters at about 5 GHz. The shift in the operating frequency is attributed to the inaccuracy of the spiral inductor model. Compared with the simulated results, the measured power gains are slightly lower. The power gain of the reference differential LNA (LNA0) is 16.2 dB at 5 GHz. The five ESD-protected differential LNAs exhibit higher power gains than that of LNA0. Among the ESD-protected LNAs, the lowest power gain of 17.9 dB is observed in LNA1. At 5 GHz, LNA4 has the highest power gain of 19.2 dB. The increase on power gain after ESD protection devices are added can be explained by (5.6) with the decreased R_{S_eq}.

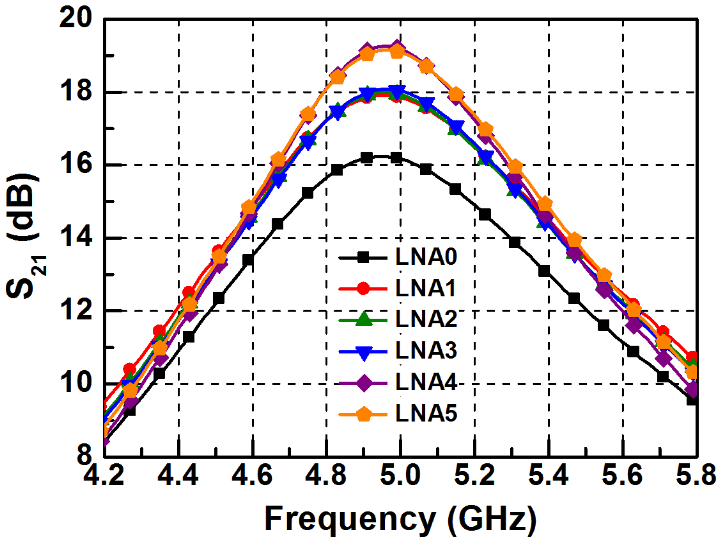


Fig. 5.20. Measured S_{21}-parameters (power gain) of the reference differential LNA (LNA0) and the five ESD-protected differential LNAs (LNA1–LNA5).

The measured S_{11}-parameters are compared in Fig. 5.21. All of the fabricated LNAs have the S_{11}-parameters of less than -18.7 dB at 5 GHz, which is a satisfactory input matching. The reference LNA and the ESD-protected LNAs achieve best input matching at the same frequency. The measured results have demonstrated that the same operating frequency can be maintained after adding the ESD protection circuits as long as the parasitic effects from the ESD protection devices can be well characterized.

As shown in Fig. 5.22, the measured S_{22}-parameters have larger difference from the simulated results (Fig. 5.15) as compared with the other S-parameters. Since the designed drain capacitance C_{D1} (C_{D2}) is quite small, it is sensitive to the parasitic effects at the output node and the drain inductor. Therefore, the parasitic effects degrade output matching. The reference differential LNA exhibits the S_{22}-parameter of -9.3 dB at 5 GHz, whereas the five ESD-protected differential LNAs all have the S_{22}-parameters of less than -10.3 dB. To investigate the reverse isolation, the S_{12}-parameters of the fabricated LNAs are measured and shown in Fig. 5.23. At 5 GHz, the S_{12}-parameter of better than -28.3 dB is achieved in all of the fabricated differential LNAs, because good reverse isolation is one of the features in the cascode configuration.

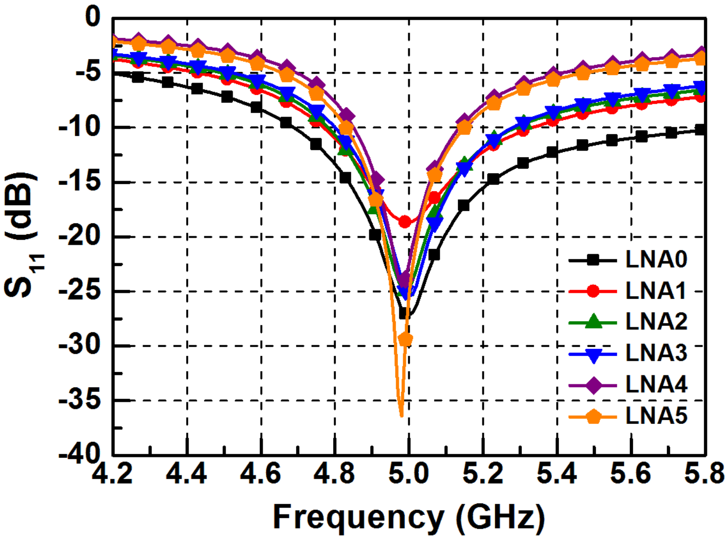


Fig. 5.21. Measured S_{11}-parameters (input reflection) of the reference differential LNA (LNA0) without ESD protection and the five ESD-protected differential LNAs (LNA1–LNA5).

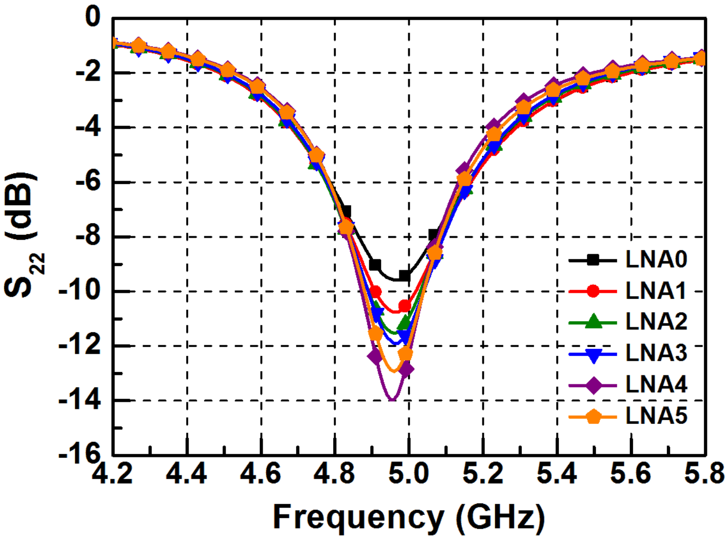


Fig. 5.22. Measured S_{22}-parameters (output reflection) of the reference differential LNA (LNA0) without ESD protection and the five ESD-protected differential LNAs (LNA1–LNA5).

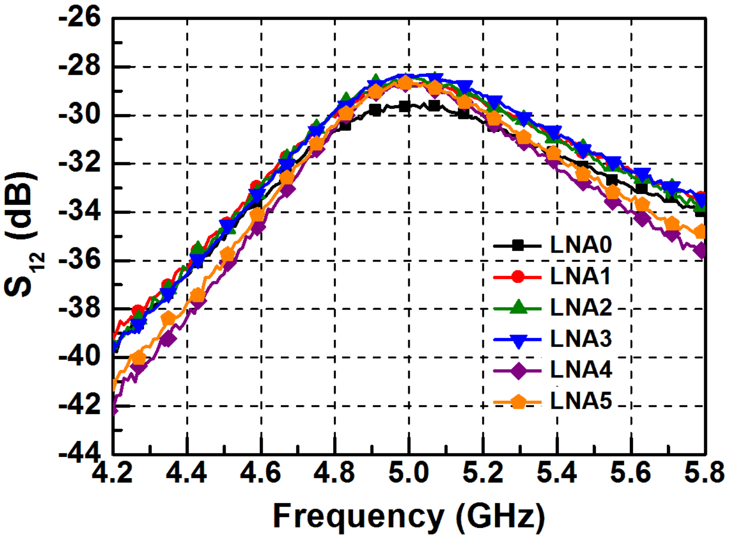


Fig. 5.23. Measured S_{12}-parameters (reverse isolation) of the reference differential LNA (LNA0) without ESD protection and the five ESD-protected differential LNAs (LNA1–LNA5).

The noise figures were measured by using Agilent N8975A noise figure analyzer and Agilent 346C noise source. The measured noise figures are shown in Fig. 5.24. The reference differential LNA (LNA0) has the best noise figure, which is 2.16 dB at 5 GHz. With the ESD protection schemes, the noise figure is degraded in the five ESD-protected LNAs (LNA1–LNA5). At 5 GHz, LNA4 has the highest noise figure, which is 3.22 dB. The increase in the noise figures of the ESD-protected LNAs is caused by the addition of ESD protection devices.

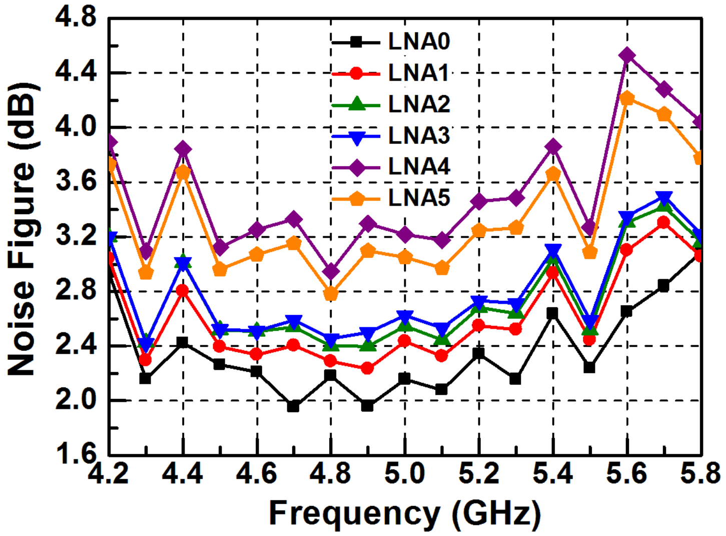


Fig. 5.24. Measured noise figures of the reference differential LNA (LNA0) without ESD protection and the five ESD-protected differential LNAs (LNA1–LNA5).

To investigate the linearity of the LNA, the third-order intercept point was measured by the two-tone test with 5- and 5.005-GHz signals. Agilent E8247C signal generator and Agilent E4407B spectrum analyzer were used in the two-tone test. The input-referred third-order intercept (IIP3) values range from -12.5 dB to -13 dB for the six fabricated differential LNAs. There is no significant difference on RF performances except noise figure among these three fabricated LNAs, which demonstrates the effectiveness of the co-design with LNA and ESD protection.

5.4.2. ESD Robustness

With different ESD protection schemes, the ESD levels of these three LNAs are expected to be different even though the total parasitic capacitances of ESD protection devices are identical. To compare the ESD levels of the six fabricated differential LNAs, the HBM and MM ESD tests have been performed [6], [7]. The failure criterion is 30% voltage shift under 1-μA current bias. The measured HBM and MM ESD levels of the six LNAs are listed in Table 5.2. When the input pin was tested, the reference LNA (LNA0) was very vulnerable to ESD, which failed at 50 V and 10 V ESD stresses in HBM and MM ESD tests, respectively. The LNA (LNA1) with the double-diode ESD protection scheme has HBM and MM ESD levels of 2.5 kV and 200 V, respectively. The ESD test results have shown that the pin-to-pin ESD test is the most critical ESD-test pin combination for the conventional double-diode ESD protection scheme. Among the ESD-protected LNAs, LNA2 achieves the highest ESD robustness. With the proposed double-SCR ESD protection scheme applied to LNA2, the HBM and MM ESD levels of the LNA are significantly improved to 6.5 kV and 500 V, respectively. Moreover, the pin-to-pin ESD test is no longer the most critical ESD-test pin combination for the LNA with the proposed double-SCR ESD protection scheme. The VDD-to-VSS ESD test was also used to verify the power-rail ESD clamp circuit. All of the ESD-protected LNAs can sustain the VDD-to-VSS ESD stress of over 8 kV and over 1 kV in HBM and MM ESD tests, respectively.

In LNA1 and LNA5, the positive (negative) ESD voltage is coupled from the input pad to VDD (VSS) through D_P (D_N) to enable the ESD detection circuit to turn on the power-rail ESD clamp circuit during PS-mode (ND-mode) ESD stresses. The ESD current path consists of a diode and an SCR in these two ESD protection schemes. In LNA3, the positive ESD voltage is coupled from the input pad to VDD through D_P and the parasitic P+/N-well diode in P-$STSCR_1$ to turn on the power-rail ESD clamp circuit during PS-mode ESD stresses. The ESD current path consists of two diodes and an SCR in LNA3. The ESD test results show that the MM ESD level does not correlate with the HBM ESD level In LNA3. Since the ESD voltage is coupled from the input pad to VDD through two diodes (D_P and the parasitic P+/N-well diode in P-STSCR$_1$), the coupling efficiency is lowered. As a result, the P-STSCRs are not quickly turned on during the MM ESD stress, which has faster rise time than that of the HBM ESD stress.

Table 5.2

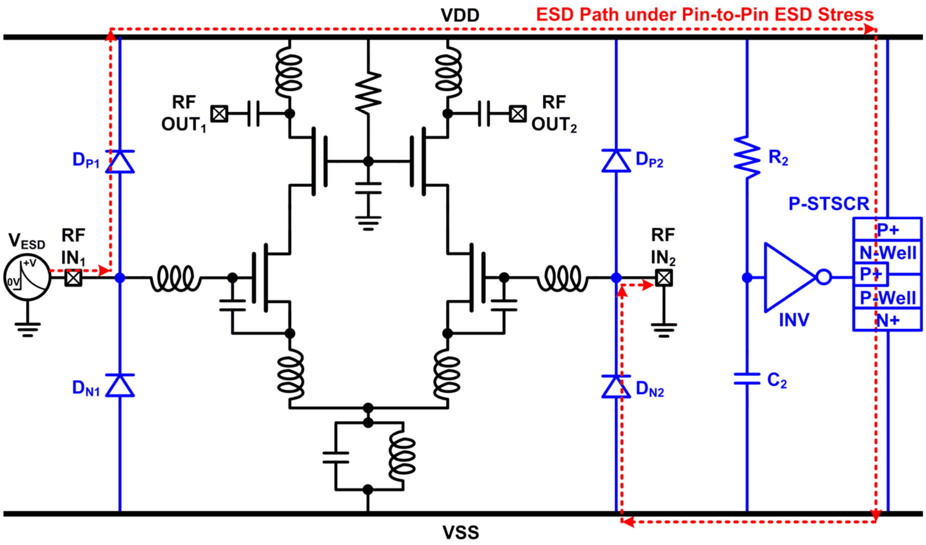
HBM and MM ESD Robustness of the Differential LNAs

Low-Noise Amplifier	PS-Mode		ND-Mode		Pin to Pin		VDD to VSS	
	HBM	MM	HBM	MM	HBM	MM	HBM	MM
LNA0	< 50 V	< 10 V	< 50 V	< 10 V	< 50 V	< 10 V	0.5 kV	< 10 V
LNA1	3 kV	250 V	7 kV	400 V	2.5 kV	200 V	> 8 kV	> 1000 V
LNA2	6.5 kV	500 V	7.5 kV	700 V	> 8 kV	550 V	> 8 kV	> 1000 V
LNA3	3 kV	100 V	7 kV	450 V	6.5 kV	150 V	> 8 kV	> 1000 V
LNA4	1.5 kV	150 V	7.5 kV	400 V	4.5 kV	300 V	> 8 kV	> 1000 V
LNA5	4 kV	300 V	> 8 kV	650 V	6 kV	500 V	> 8 kV	> 1000 V

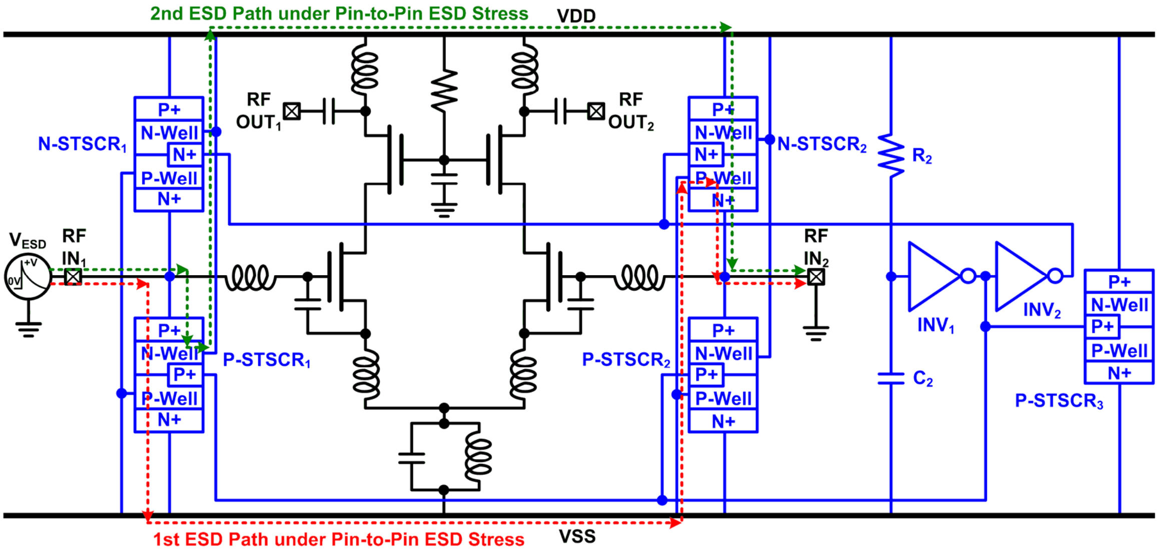
In LNA2, the positive (negative) ESD voltage is coupled from the input pad to VDD (VSS) through the parasitic P+/N-well diode in the P-STSCR (parasitic N+/P-well diode in the N-STSCR) to turn on the P-STSCR (N-STSCR) during PS-mode (ND-mode) ESD stresses. The ESD current paths during PS- and ND-mode ESD stresses consist of only an SCR. Fewer ESD protection devices along the ESD current path indicates lower ESD clamping voltage and higher ESD robustness. This is the reason why LNA2 has higher PS- and ND-mode ESD levels.

When the input pad RF IN$_1$ in LNA4 is stressed by ESD, the positive (negative) ESD voltage is coupled from the RF IN$_1$ to VDD (VSS) through the parasitic P+/N-well diode in P-STSCR$_1$ (parasitic N+/P-well diode in P-STSCR$_2$) to turn on the power-rail ESD clamp circuit during PS-mode (ND-mode) ESD stresses. However, LNA4 does not achieve comparable PS-mode ESD robustness with LNA1 and LNA5. Lower PS-mode ESD robustness in LNA4 is attributed to the unoptimized placement and routing of the ESD protection devices, which leads to slow coupling of the ESD voltage from the input pad to VDD during PS-mode ESD tests.

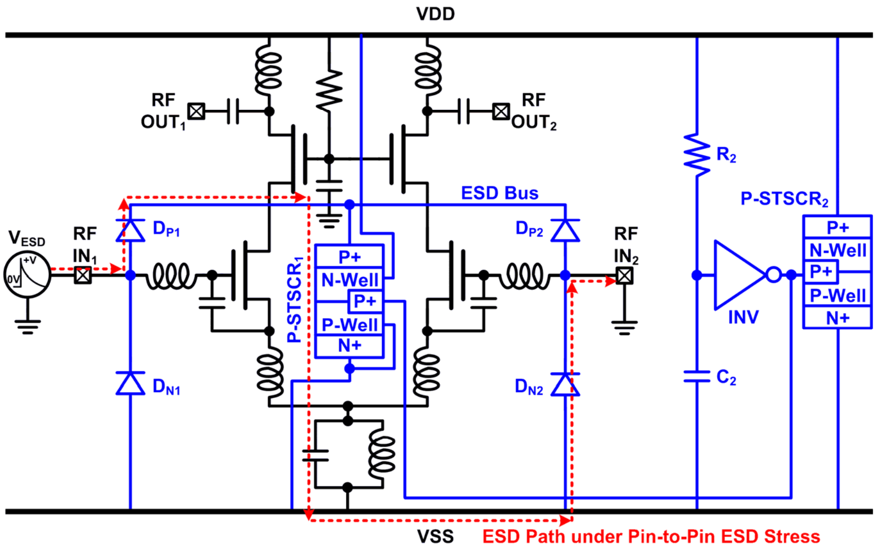
During pin-to-pin ESD stresses, the ESD pulse is applied to one differential input pad with the other differential input pad grounded. Both VDD and VSS pads are floating. The ESD current paths in the five ESD-protected differential LNAs are shown in Fig. 5.25(a)–(e).


VDD
ESD Path under Pin-to-Pin ESD Stress
RF OUT$_1$
RF OUT$_2$
D$_{P1}$
D$_{P2}$
R$_2$
P-STSCR
V$_{ESD}$
+V
0V
RF IN$_1$
RF IN$_2$
P+
N-Well
P+
P-Well
N+
INV
D$_{N1}$
D$_{N2}$
C$_2$
VSS

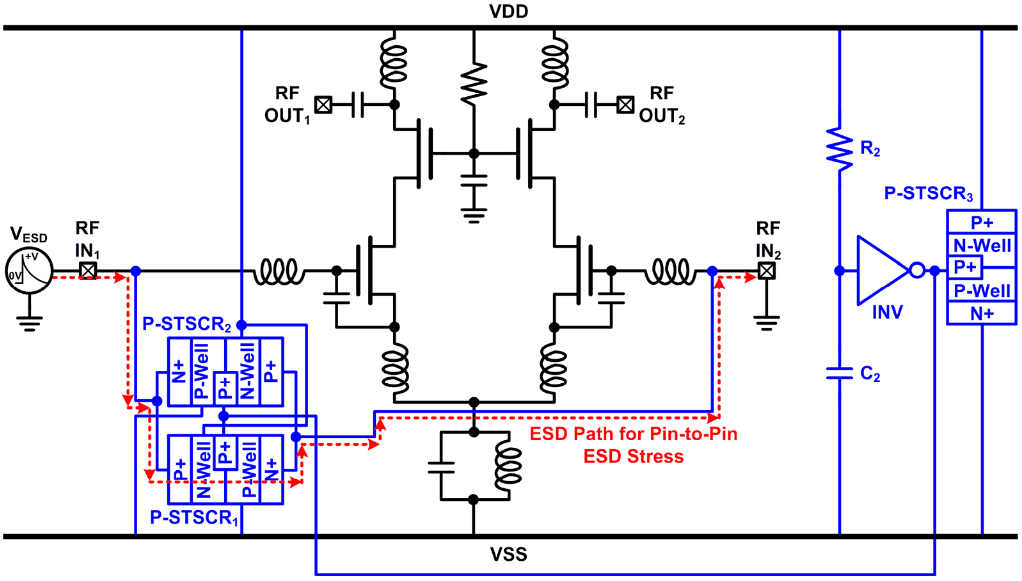
(a)


2nd ESD Path under Pin-to-Pin ESD Stress
VDD
RF OUT$_1$
RF OUT$_2$
P+
N-Well
N+
P-Well
N+
N-STSCR$_1$
N-STSCR$_2$
R$_2$
V$_{ESD}$
+V
0V
RF IN$_1$
RF IN$_2$
INV$_1$
INV$_2$
P-STSCR$_1$
P-STSCR$_2$
P-STSCR$_3$
C$_2$
1st ESD Path under Pin-to-Pin ESD Stress
VSS

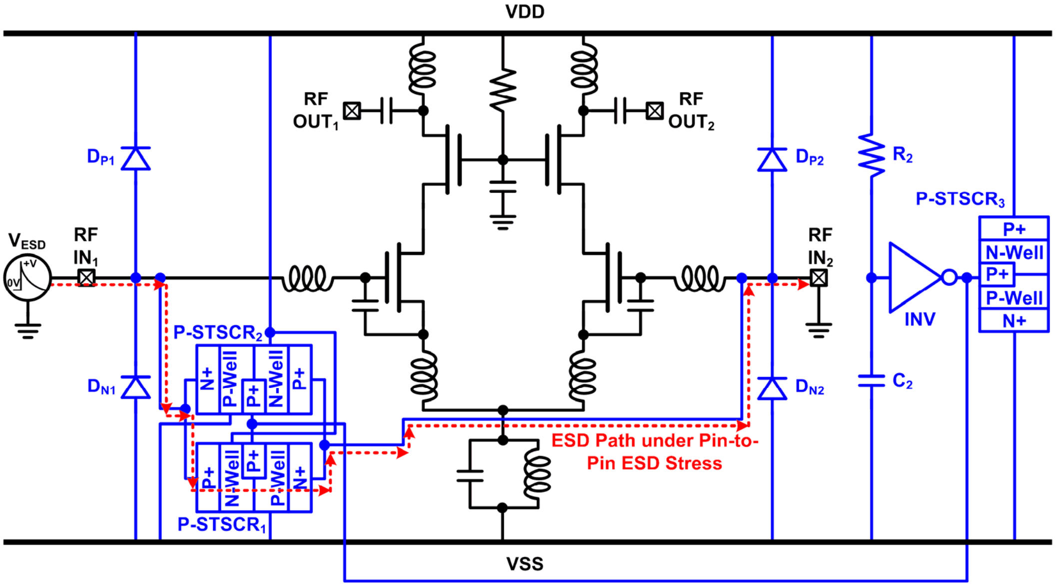
(b)


VDD
RF OUT$_1$
RF OUT$_2$
R$_2$
ESD Bus
P-STSCR$_2$
V$_{ESD}$
+V
0V
RF IN$_1$
D$_{P1}$
D$_{P2}$
RF IN$_2$
P-STSCR$_1$
P+
N-Well
P+
P-Well
N+
INV
D$_{N1}$
D$_{N2}$
C$_2$
VSS
ESD Path under Pin-to-Pin ESD Stress

(c)



(d)



(e)

Fig. 5.25. ESD current paths under pin-to-pin ESD stress in (a) LNA1 with the conventional double-diode ESD protection scheme, (b) LNA2 with the proposed double-SCR ESD protection scheme, (c) LNA3 with the proposed ESD bus, (d) LNA4 with the proposed cross-coupled SCR, and (e) LNA5 with the double diodes and the proposed cross-coupled SCR.

In Fig. 5.25(a), the pin-to-pin ESD current is first conducted from the zapped pad to VDD through D_{P1} in LNA1. Besides, VSS initially has a voltage level near to ground because it is connected to the grounded input pad through D_{N2}. Thus, the pin-to-pin ESD-stress voltage across these two differential pins becomes across VDD and VSS, and the power-rail ESD clamp circuit is turned on to conduct ESD current from VDD to VSS. Consequently, the

ESD current path consists of D_{P1}, P-STSCR, and D_{N2} in LNA1 with the conventional double-diode ESD protection scheme [128].

In LNA2 with the proposed double-SCR ESD protection scheme, all of the SCR devices are turned on during pin-to-pin ESD stresses, as shown in Fig. 5.25(b). There are two ESD current paths with lower clamping voltage which includes only the voltage drop across a diode and an SCR. The first ESD current path is through P-STSCR$_1$ and the parasitic N+/P-well diode in N-STSCR$_2$, and the second one is through the parasitic P+/N-well diode in P-STSCR$_1$ and N-STSCR$_2$. Except lower clamping voltage along the current path, the proposed double- SCR ESD protection scheme has more ESD current paths than the double-diode ESD protection scheme. Therefore, LNA2 sustains higher pin-to-pin ESD robustness (>8 kV in HBM and 550 V in MM) than other ESD-protected differential LNAs.

The ESD current path in LNA3 with the proposed ESD bus under pin-to-pin ESD stresses is shown in Fig. 5.25(c). Similar to the situation under PS-mode ESD tests, the P-STSCRs are not quickly turned on because two series diodes between the input pad and VDD. ESD voltage must pass these two diodes when it is coupled from the input pad to VDD. As a result, the pin-to-pin ESD robustness in MM is lower than expected.

Fig. 5.25(d) illustrates the ESD current path in LNA4 under pin-to-pin ESD stresses. ESD voltage is coupled from the input pad to VDD through the parasitic P+/N-well diode in P-STSCR$_1$. After the ESD detection circuit turns on the P-STSCRs, the pin-to-pin ESD current path consisting of P-STSCR$_1$ is established. The ESD current path in LNA5 is shown in Fig. 5.25(e), where P-STSCR$_1$ is used to discharge the pin-to-pin ESD current. With the extra P+/N-well diodes (D_P) and N+/P-well diodes (D_N) beside the cross-coupled SCR devices, the ESD voltage can be coupled from the input pad to VDD (VSS) more efficiently when the input pad is zapped by positive (negative) ESD stresses. Hence, LNA5 has higher ESD robustness than LNA4 in all ESD-test pin combinations.

Table 5.3 summarizes the measured performances of the six fabricated differential LNAs and compares the performances with those of the prior CMOS differential LNAs. In this work, the pin-to-pin ESD robustness of the differential LNA is first investigated. The five ESD-protected LNAs in this chapter exhibit satisfactory RF performances, while providing excellent ESD protection as compared with the other published differential LNAs.

5.4.3. Failure Analysis

Compared with the stand-alone ESD protection device, the ESD-protected LNAs still have lower ESD levels. It is expected that the failure could be located at the gate oxide of the

Table 5.3

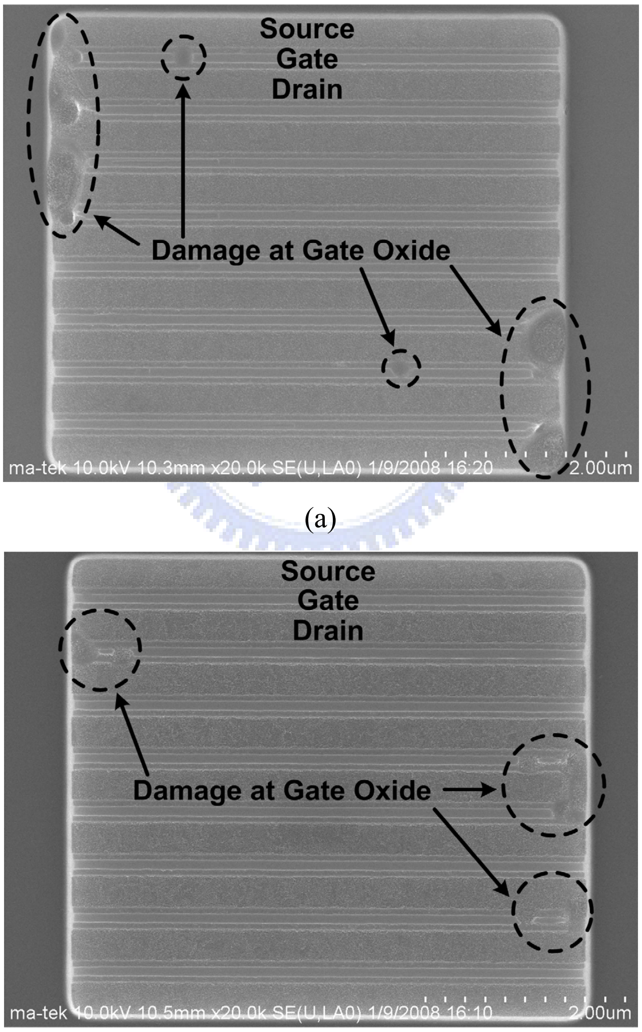
Comparison With Prior CMOS Differential LNAs

	Technology	f_0 (GHz)	VDD (V)	P_{DC} (mW)	NF (dB)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	HBM ESD Level (kV)	MM ESD Level (V)
LNA0	**0.13-μm CMOS**	**5**	**1.2**	**10.3**	**2.16**	**16.2**	**-27.2**	**-9.3**	**< 0.05**	**< 10**
LNA1	**0.13-μm CMOS**	**5**	**1.2**	**10.3**	**2.43**	**17.9**	**-18.7**	**-10.4**	**2.5**	**200**
LNA2	**0.13-μm CMOS**	**5**	**1.2**	**10.3**	**2.54**	**17.9**	**-24.8**	**-10.9**	**6.5**	**500**
LNA3	**0.13-μm CMOS**	**5**	**1.2**	**10.3**	**2.62**	**18**	**-25.4**	**-11.4**	**3**	**100**
LNA4	**0.13-μm CMOS**	**5**	**1.2**	**10.3**	**3.21**	**19.2**	**-22.4**	**-12.3**	**1.5**	**150**
LNA5	**0.13-μm CMOS**	**5**	**1.2**	**10.3**	**3.05**	**19.1**	**-25.2**	**-11.9**	**4**	**300**
Ref. [116]	**0.18-μm CMOS**	**5.75**	**1**	**16**	**0.9**	**14.2**	**N/A**	**-8**	**N/A**	**N/A**
Ref. [117]	**0.18-μm CMOS**	**5.8**	**1.8**	**14.4**	**3.7**	**12.5**	**-15**	**-9**	**N/A**	**N/A**
Ref. [118]	**0.18-μm CMOS**	**6**	**1.8**	**6.48**	**3**	**7.1**	**-10**	**-7.3**	**N/A**	**N/A**
Ref. [119]	**0.13-μm CMOS**	**3 - 5**	**1.5**	**45**	**4**	**25.8**	**-11**	**N/A**	**1.5**	**N/A**
Ref. [120]	**0.13-μm CMOS**	**2 - 4.6**	**1.5**	**16.5**	**3.5**	**9.5**	**-10**	**N/A**	**N/A**	**N/A**
Ref. [121]	**90-nm CMOS**	**0.1 - 8**	**1.4**	**16**	**3.4**	**17**	**-10**	**N/A**	**2.25**	**N/A**
Ref. [122]	**0.13-μm CMOS**	**18**	**1.5**	**36**	**4.1**	**22.4**	**-7**	**-17**	**2**	**N/A**

input NMOS which is connected to the input pad. The scanning electron microscope (SEM) pictures in Fig. 5.26(a) and (b) have confirmed the ESD failure location of the ESD-protected LNAs after ESD stresses. The failure locations of ESD damage in all of the fabricated differential LNAs during all ESD-test pin combinations are at the gate oxide of the input NMOS (M_1) whose gate is connected to the zapped pad. This failure mechanism indicates that even though the ESD protection device does not fail, the overshooting voltage across the gate oxide is so large to cause damage at the gate oxide. The ESD clamping voltage should be further lowered to prevent such internal ESD damages, because the gate-oxide breakdown voltage is decreasing as the CMOS technology is scaled down.

5.5. Discussions and Design Guidelines

In this chapter, several on-chip ESD protection designs for differential LNA have been proposed. Among these five ESD protection designs, the double-SCR ESD protection is the most recommended design for several reasons. First, the SCR has lower ESD clamp voltage as compared with the diode, so using the SCR can achieve higher ESD robustness than that of using the diode under the same parasitic capacitance. Second, the double-SCR ESD protection scheme provides two ESD current paths during the pin-to-pin ESD stresses, as shown in Fig. 5.25(b). Thus, the ESD robustness under pin-to-pin ESD test, which exhibits the lowest ESD level among all ESD-test pin combinations in the conventional double-diode ESD protection scheme, can be significantly improved. Moreover, the S-parameters of LNA2 with the double-SCR ESD protection scheme are not degraded as compared with LNA0 without ESD protection. The noise figure of LNA2 is only 0.38-dB higher than that of LNA0. With LNA and ESD protection co-design, the double-SCR ESD protection scheme could be the best ESD protection design for the differential LNA in nanoscale CMOS processes.



(a)

(b)

Fig. 5.26. SEM pictures at the failure points of (a) LNA1 with the double-diode ESD protection scheme after 3-kV HBM pin-to-pin ESD test, and (b) LNA2 with the double-SCR ESD protection scheme after 7-kV HBM PS-mode ESD test. The failure locations are all located at the gate oxide of input NMOS M_1.

5.6. Summary

In this chapter, five ESD protection schemes for a 5-GHz differential LNA have been presented and verified in a 130-nm CMOS process. All ESD protection schemes have the same parasitic capacitance of 300 fF at each input pad. With the LNA and ESD protection co-design, the RF performances of the ESD-protected LNAs have only little degradation as compared with the reference LNA without ESD protection. However, the ESD robustness of LNA is substantially improved by the proposed on-chip ESD protection circuit. Moreover, the pin-to-pin ESD robustness of gigahertz differential LNA is investigated in this work for the first time. The 5-GHz differential LNA (LNA1) with double-diode ESD protection scheme exhibits the power consumption of 10.3 mW, power gain of 17.9 dB, input matching of -18.7 dB, noise figure of 2.43 dB, as well as 2.5-kV HBM and 200-V MM ESD robustness The ESD robustness of the double-diode ESD-protected LNA is dominated by the most critical ESD-test combination, which is the pin-to-pin ESD test. With the same power consumption and power gain, the 5-GHz differential LNA (LNA2) with the proposed double-SCR ESD protection scheme features the input matching of -24.8 dB, noise figure of 2.54 dB, as well as 6.5-kV HBM and 500-V MM ESD robustness. Especially, the LNA with the proposed double-SCR ESD protection scheme can sustain the HBM and MM pin-to-pin ESD stress of over 8 kV and 550 V, respectively. With comparable RF performance, the differential LNA (LNA5) with the double diodes and the proposed cross-coupled SCR devices achieves 4-kV HBM and 300-V MM ESD robustness. The experimental results have demonstrated that the ESD protection schemes proposed in this chapter can be successfully co-designed with the LNA to achieve good RF performance and high ESD robustness simultaneously.

Chapter 6

ESD Protection Design for High-Speed I/O Interface Circuits in CMOS Technology

In this chapter, the electrostatic discharge (ESD) protection design for high-speed input/output (I/O) interfaces in a 130-nm CMOS process is presented. First, the ESD protection diodes were designed and fabricated to evaluate their ESD robustness and the parasitic effects in gigahertz frequency band. With the knowledge of the dependence of device dimensions on ESD robustness and the parasitic capacitance, the ESD protection circuit for high-speed I/O interface circuits was designed with slight degradation on high-speed circuit performance but satisfactory high ESD robustness. In this chapter, the dummy receiver NMOS and the dummy transmitter NMOS are designed with the whole-chip ESD protection scheme to investigate the ESD robustness of the general receiver and transmitter interface circuits. The ESD protection scheme presented in this chapter has been applied to an IC product with 2.5-Gb/s high-speed front-end interface [129], [130].

6.1. Background

With the advantage of low cost and high integration capability, more and more commercial integrated circuits (ICs) had been fabricated in CMOS processes, including the high-speed input/output (I/O) interface circuits. Electrostatic discharge (ESD), which has become one of the most important reliability issues for CMOS ICs, must be taken into consideration during the design phase. To achieve better high-speed circuit performance, high-speed I/O interface circuits are fabricated in nanoscale CMOS processes. However, nanoscale MOS transistors are very vulnerable to ESD because ESD was not scaled with CMOS processes. Recently, several ESD protection designs for high-speed I/O applications have been reported [131]–[135]. Diodes had been used to protect the dual-channel optical transceiver array [131]. To lower the overall capacitance at the I/O pad, the ESD protection scheme with the T-coil and negative impedance converter had been reported [132]. In SCR-based ESD protection scheme, an RC-based ESD detection circuit and an NMOS had been used to draw trigger current from the base terminal of the PNP BJT in the SCR [133]. Besides, a modified SCR with low trigger voltage had been used to protect the DDR3 DRAM interface circuit [134]. Another design using the darlington-based SCR structure had been proposed to reduce the breakdown voltage [135]. There are two major design considerations in ESD protection design for high-speed I/O interfaces. First, ESD protection circuits for high-speed I/O interfaces must sustain high enough ESD robustness to effectively protect the thin gate oxide in the internal circuits against ESD stress. Second, the degradation of high-speed circuit performance due to the parasitic effects of ESD protection devices needs to be minimized.

Traditional ESD protection devices, which have large parasitic capacitance, would significantly degrade high-speed circuit performance. Therefore, traditional ESD protection designs with large ESD protection devices are no longer suitable for high-speed I/O applications because of the intolerable large parasitic effects. With proper design, the double-diode ESD protection scheme in cooperation with active power-rail ESD clamp circuit can be used to realize the whole-chip ESD protection scheme for high-speed I/O applications with minimum degradation on circuit performance. In order to minimize the parasitic capacitance caused by the ESD protection devices and to achieve satisfactory ESD robustness, the high-frequency characteristics and the ESD levels of the ESD protection diodes in a 130-nm CMOS process were evaluated in this chapter to obtain the dependence of device size on ESD robustness and parasitic capacitance. After determining the dimensions of ESD protection diodes, whole-chip ESD protection scheme can be realized with the power-rail ESD clamp circuit [9].

In this chapter, experimental results on ESD robustness and parasitic capacitance of the fabricated ESD protection diodes in a 130-nm CMOS process are reported and discussed. The dummy receiver NMOS and dummy transmitter NMOS are fabricated in a 130-nm CMOS process. In the dummy receiver NMOS and dummy transmitter NMOS, the I/O pad is connected to the gate terminal and drain terminal of the NMOS transistor, respectively. After investigating the ESD robustness of the dummy receiver NMOS and dummy transmitter NMOS, the whole-chip ESD protection scheme is applied to a 2.5-Gb/s high-speed I/O interface circuit in a 130-nm CMOS process.

6.2. ESD Protection Diodes

The most popular ESD protection devices at the I/O pad are the shallow-trench-isolation

(STI) diodes. There are three diodes available in the 130-nm CMOS process, which are the P+/N-well diode, N+/P-well diode, and N-well/P-substrate diode. The P+/N-well diode, whose layout top view and cross-sectional view are shown in Fig. 6.1, is placed between the I/O pad and VDD, because the N-well is often connected to VDD. In a P+/N-well diode, the P+ diffusion is connected to the I/O pad, and the parasitic effects between the P+/N-well junction is contributed to the I/O pad. The size of the P+/N-well diode is referred to the size of the P+ diffusion.

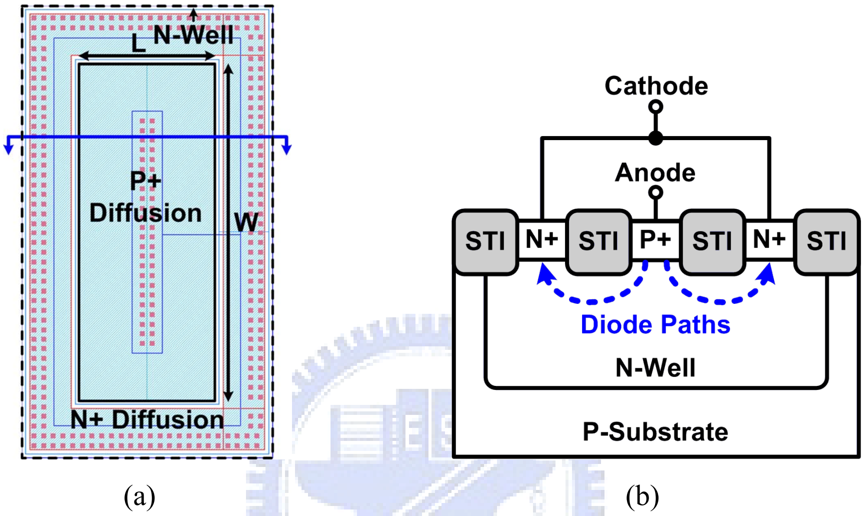
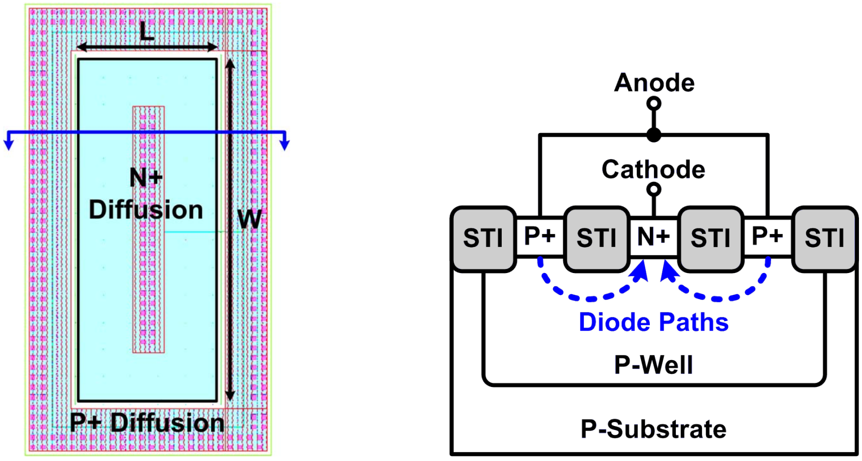


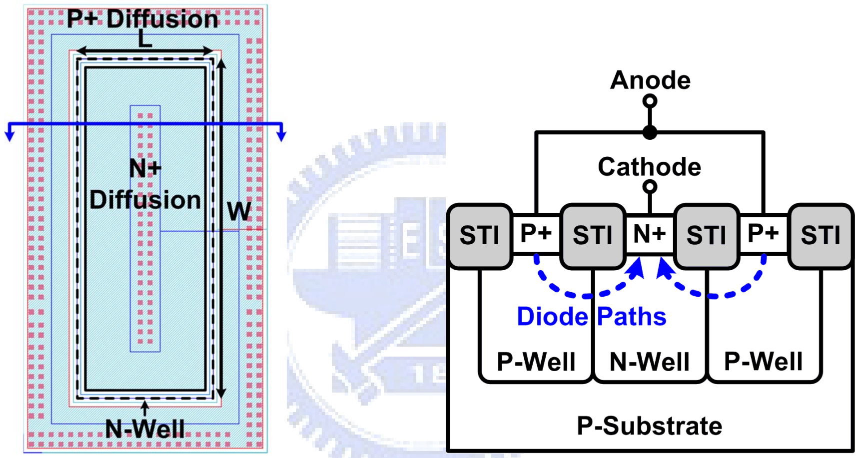
Fig. 6.1. (a) Layout top view and (b) cross-sectional view of P+/N-well diode.

Another ESD protection diode between the I/O pad and VSS is the N+/P-well diode, because the P-well must be connected to VSS. The layout top view and cross-sectional view of the N+/P-well diode are shown in Fig. 6.2(a) and (b), respectively. Since the N+ diffusion is connected to the I/O pad, the size of an N+/P-well diode is referred to the size of the N+ diffusion. Besides, the N-well/P-substrate diode can also be used between the I/O pad and VSS, and its layout top view and cross-sectional view are shown in Fig. 6.3(a) and (b), respectively. In the N-well/P-substrate diode, the N-well is connected to the I/O pad through the N+ diffusion. Thus, the size of the N-well region is the design parameter of the N-well/P-substrate diode. The dependence of ESD robustness on parasitic capacitance in a 130-nm CMOS process is investigated in this chapter to solve the trade-off between the ESD protection capability and the high-speed performance degradation. These three kinds of diodes with junction perimeters (PJ) of 20 μm, 40 μm, and 80 μm have been designed and fabricated in a 130-nm CMOS process [129].



(a) (b)

Fig. 6.2. (a) Layout top view and (b) cross-sectional view of N+/P-well diode.



(a) (b)

Fig. 6.3. (a) Layout top view and (b) cross-sectional view of N-well/P-substrate diode.

For high-speed I/O applications, the parasitic capacitance of the ESD protection diode is a key factor because it directly affects the high-speed circuit performance. To evaluate the parasitic capacitance of the ESD protection diodes, the two-port S-parameters of the fabricated ESD protection diodes were measured with the network analyzer. In the S-parameter measurement, port 1 and port 2 of the network analyzer were connected to the two terminals of the diode. Port 1 is connected to the terminal which is connected to the I/O pad when the ESD protection diode is applied to the high-speed I/O interface circuits. Port 2 is connected to the terminal which is connected to the AC ground node (VDD or VSS) when the ESD protection diode is applied to the high-speed I/O interface circuits. With the conversions between two-port S-parameters and Y-parameters shown in equation (3.5), the parasitic capacitance (C_{diode}) of the ESD protection diodes was extracted by

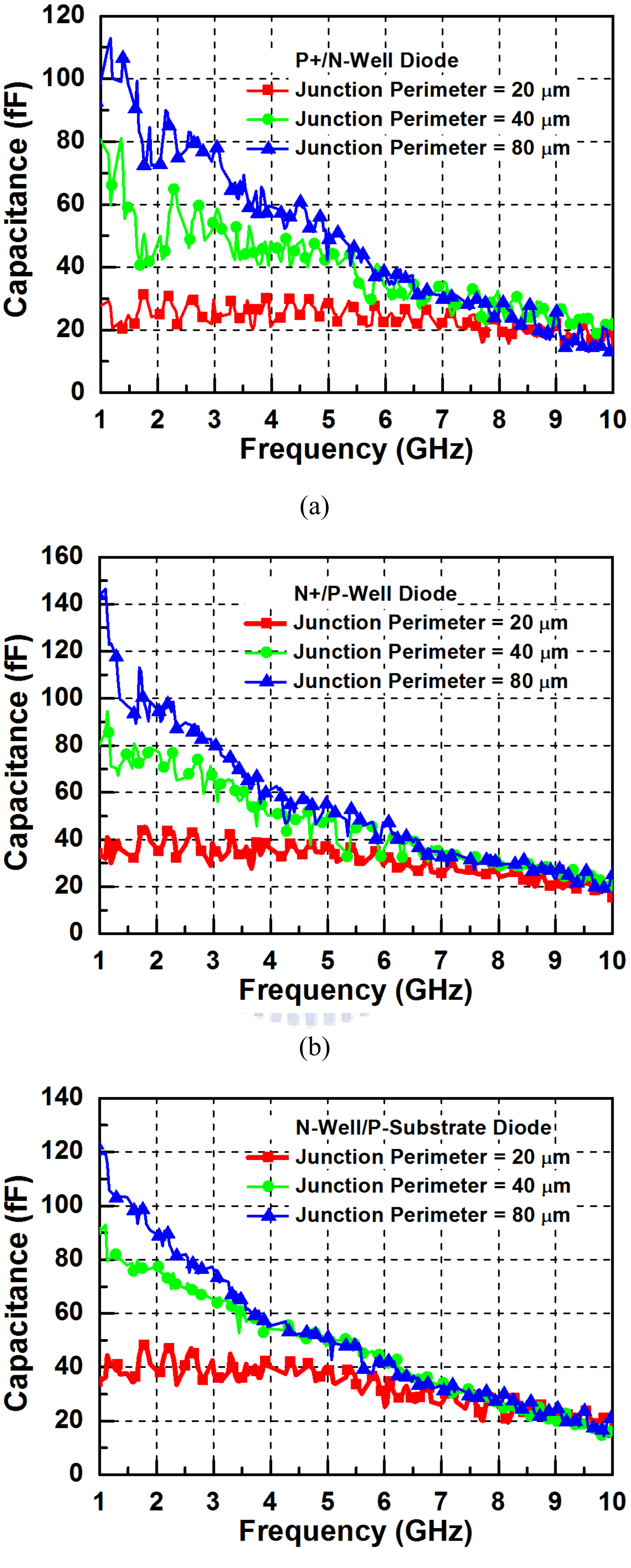
$$C_{diode} = \frac{\mathrm{Im}(Y_{11})}{\omega} = \frac{\mathrm{Im}(Y_{11})}{2\pi f} \tag{6.1}$$

where Y_{11}-parameter is the admittance seen from port 1 with port 2 grounded, and f denotes the frequency. Table 6.1 lists the device characteristics of the ESD protection diodes, including the parasitic capacitance and ESD robustness. Fig. 6.4 shows the extracted parasitic capacitances of the P+/N-well, N+/P-well, and N-well/P-substrate diodes with different device dimensions. At 2.5 GHz, the extracted parasitic capacitances of P+/N-well diode with 20-µm, 40-µm, and 80-µm junction perimeters are 27.9 fF, 51.1 fF, and 77.7 fF, respectively. For the N+/P-well diode (N-well/P-substrate) diode, the extracted parasitic capacitances at 2.5 GHz under 20-µm, 40-µm, and 80-µm junction perimeters are 37.9 fF (40.5 fF), 66.3 fF (69.3 fF), and 89.7 fF (81.9 fF), respectively. The parasitic capacitance of the ESD protection diode becomes larger when the diode size increases. Larger junction area and larger junction perimeter in the diode lead to larger junction capacitance. Besides, the DC junction capacitance can be calculated by using the SPICE model provided by the foundry. As listed in Table 6.1, the calculated DC junction capacitances of the P+/N-well diode with 20-µm, 40-µm, and 80-µm junction perimeters are 25.9 fF, 75.7 fF, and 151.4 fF, respectively. For the N+/P-well diode (N-well/P-substrate) diode, the calculated DC junction capacitances under 20-µm, 40-µm, and 80-µm junction perimeters are 20 fF (24.1 fF), 58.1 fF (52.1 fF), and 116.2 fF (104.2 fF), respectively. The difference between the extracted parasitic capacitance and the calculated junction capacitance is attributed to the parasitic series resistance in the well or substrate region, and the routing capacitance.

Table 6.1

Characteristics of ESD Protection Diodes in a 130-nm CMOS Process

	Junction Perimeter	C_{diode} at DC	C_{diode} at 2.5 GHz	It2	HBM ESD Level
P+/N-Well Diode	**20 µm**	**25.9 fF**	**27.9 fF**	**0.62 A**	**1 kV**
	40 µm	**75.7 fF**	**51.1 fF**	**1.47 A**	**3 kV**
	80 µm	**151.4 fF**	**77.7 fF**	**4.18 A**	**6 kV**
N+/P-Well Diode	**20 µm**	**20 fF**	**37.9 fF**	**0.55 A**	**1 kV**
	40 µm	**58.1 fF**	**66.3 fF**	**1.56 A**	**3 kV**
	80 µm	**116.2 fF**	**89.7 fF**	**3.75 A**	**6 kV**
N-Well/P-Sub Diode	**20 µm**	**24.1 fF**	**40.5 fF**	**0.61 A**	**1 kV**
	40 µm	**52.1 fF**	**69.3 fF**	**1.84 A**	**3 kV**
	80 µm	**104.2 fF**	**81.9 fF**	**3.9 A**	**6 kV**



(a)

(b)

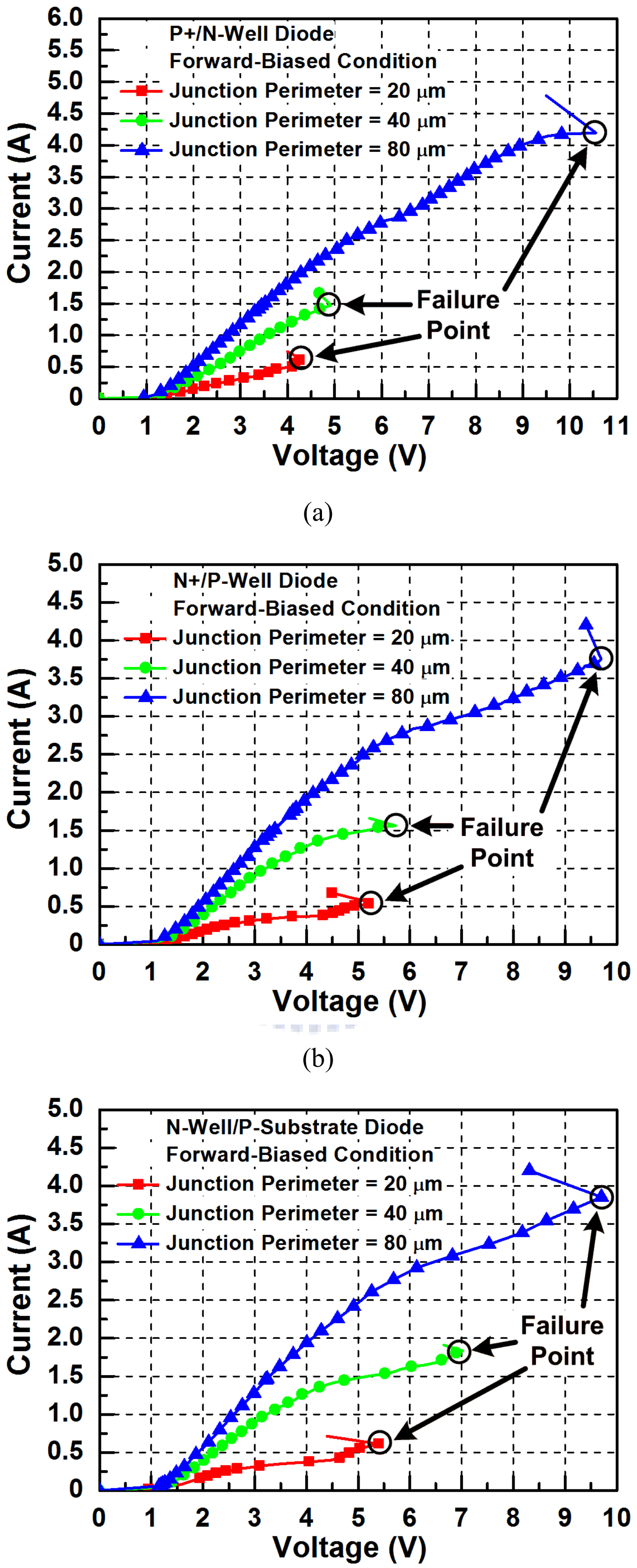
(c)

Fig. 6.4. Extracted parasitic capacitances of (a) P+/N-well diodes, (b) N+/P-well diodes, and (c) N-well/P-substrate diodes with different dimensions.

After investigating the parasitic capacitance, the ESD robustness of the ESD protection diode was characterized as well, which are also listed in Table 6.1. The characteristics of the fabricated ESD protection diodes in high-current regions were characterized by the transmission line pulsing (TLP) system with 10-ns rise time and 100-ns pulse width [136]. The secondary breakdown current (It2) can be obtained in the TLP measured I-V curve. It2 is the highest current that the device can handle under ESD stresses, which denotes the current at the failure point. The TLP-measured I-V curves of the stand-alone P+/N-well, N+/P-well, and N-well/P-substrate diodes with different dimensions under forward-biased condition are shown in Fig. 6.5. The It2 values of the P+/N-well diodes with 20-μm, 40-μm, and 80-μm junction perimeters are 0.62 A, 1.47 A, and 4.18 A, respectively. The It2 of the N+/P-well diodes with the junction perimeters of 20-μm, 40-μm, and 80-μm are 0.55 A, 1.56 A, and 3.75 A, respectively. As compared with the N+/P-well diodes, the N-well/P-substrate diodes have slightly higher It2 values. The It2 values of the N-well/P-substrate diodes with 20-μm, 40-μm, and 80-μm junction perimeters are 0.61 A, 1.84 A, and 3.9 A, respectively. Fig. 6.6 compares the It2 values of the ESD protection diodes with different device dimensions. The measured It2 values are well proportional to the device size, which demonstrates that good turn-on uniformity is achieved. As shown in Fig. 6.7, these three kinds of diodes exhibit identical human-body-model (HBM) ESD levels under the same device. The HBM ESD levels are 1 kV, 3 kV, and 6 kV with the junction perimeters of 20 μm, 40 μm, and 80 μm, respectively. Experimental results have shown that diodes with larger dimensions have higher ESD robustness, but larger diodes exhibit larger parasitic capacitance.

6.3. Whole-Chip ESD Protection Design

To investigate ESD robustness of the typical receiver and transmitter interface circuits with the ESD protection diodes and the power-rail ESD clamp circuit, the test circuits with the dummy receiver NMOS (RX_NMOS) and dummy transmitter NMOS (TX_NMOS) were implemented in a 130-nm CMOS process. In the RX_NMOS and TX_NMOS, the I/O pad is connected to the gate terminal and drain terminal of the NMOS transistor, respectively. In the RX_NMOS and TX_NMOS, the connections between the I/O pad and the NMOS transistor emulate the connections of the input NMOS and the output NMOS in general receiver and transmitter interface circuits. With such connections between the I/O pad and the MOS transistor, the ESD robustness of the ESD-protected receiver and transmitter interface circuits can be estimated by the ESD robustness of the RX_NMOS and TX_NMOS, respectively.



(a)

(b)

(c)

Fig. 6.5. TLP-measured I-V curves of (a) P+/N-well diodes, (b) N+/P-well diodes, and (c) N-well/P-substrate diodes with different dimensions.

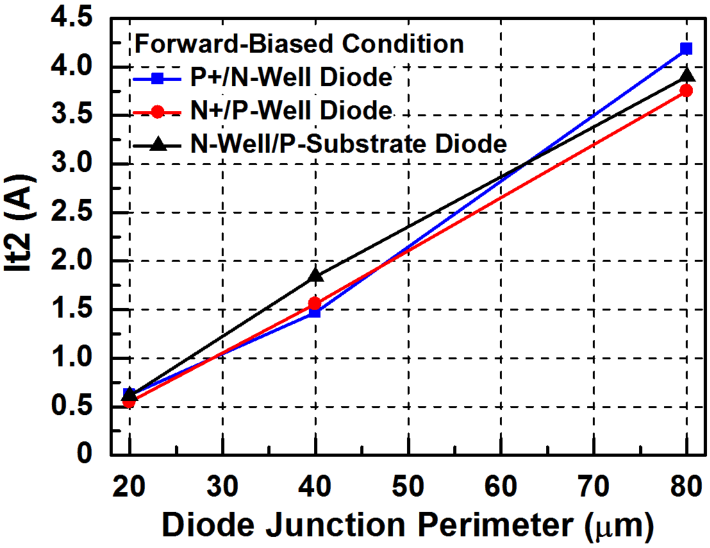


Fig. 6.6. TLP-measured It2 values of ESD protection diodes with different dimensions in a 130-nm CMOS process.

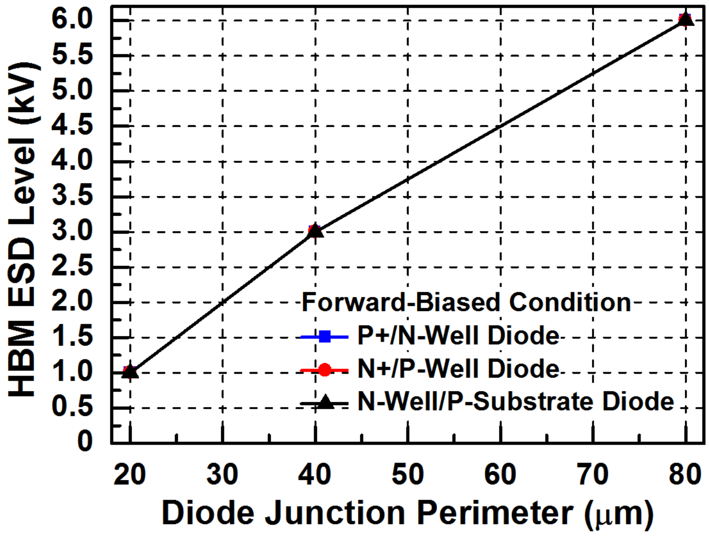


Fig. 6.7. HBM ESD levels of ESD protection diodes with different dimensions in a 130-nm CMOS process. The ESD protection diodes have identical HBM ESD robustness under the same size.

6.3.1. ESD Protection Design With Dummy Receiver NMOS

Fig. 6.8 shows the schematic of the dummy receiver NMOS (RX_NMOS). In the RX_NMOS, the gate terminal of the NMOS is connected to the I/O pad, whereas the drain, source, and bulk terminals are grounded. The ESD protection diode (D_P) between the I/O pad and VSS is realized by the P+/N-well diode, whereas the ESD protection diode (D_N) between the I/O pad and VSS is realized by the N-well/P-substrate diode. As reported in the last section, the stand-alone ESD protection diodes with more than 40-μm junction perimeter can provide over 2-kV HBM ESD level, which is the specification for general commercial IC products. To increase the margin of ESD robustness, the ESD protection diodes were realized with 45-µm and 55-µm junction perimeters to compare their ESD levels. In this whole-chip ESD protection scheme, the ESD clamp device of P-type substrate-triggered SCR (P-STSCR), which is presented in section 5.3.1, was implemented in the power-rail ESD clamp circuit with 59.6-µm width. When the I/O pad of RX_NMOS is zapped by ESD, the voltage across the I/O pad and VSS is across the gate oxide, which is the worst case for the gate oxide of NMOS during ESD stresses. Since the gate terminal of the MOS transistor is often connected to the input pad of the receiver, the ESD robustness of RX_NMOS can be used to estimate the ESD robustness of the practical receiver interface circuit with this ESD protection scheme.

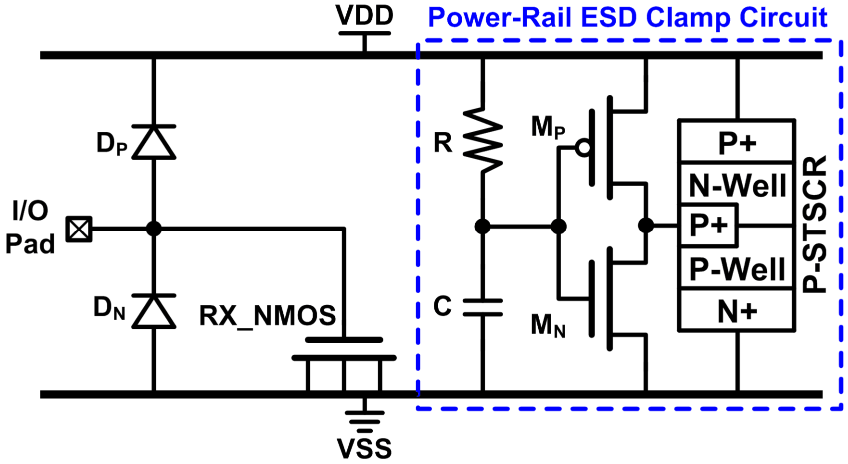


Fig. 6.8. Dummy receiver NMOS (RX_NMOS) used as a test circuit to verify the effectiveness of the proposed ESD protection scheme in a receiver (double diodes and active power-rail ESD clamp circuit).

6.3.2. ESD Protection Design With Dummy Transmitter NMOS

Fig. 6.9 shows the schematic of the dummy transmitter NMOS (TX_NMOS). In the TX_NMOS, the drain terminal of the NMOS is connected to the I/O pad, whereas the gate, source, and bulk terminals are grounded. Similarly, the ESD protection diode (D_P) between the I/O pad and VDD is realized by the P+/N-well diode, and the ESD protection diode (D_N) between the I/O pad and VSS is realized by N-well/P-substrate diode. D_P and D_N with 45-µm and 55-µm junction perimeters were used in the ESD protection scheme for the TX_NMOS. The P-STSCR with 59.6-µm width was implemented as the ESD clamp device in the power-rail ESD clamp circuit. When the I/O pad is zapped by ESD, the voltage between the

I/O pad and VSS is across the drain terminal and the other three terminals of the NMOS transistor, which is the worst case for the drain terminal of the NMOS transistor during ESD stresses. Since the drain terminal of the MOS transistor is often connected to the output pad of the transmitter, the ESD robustness of the TX_NMOS can be used to estimate the ESD robustness of the practical transmitter interface circuit protected by this ESD protection scheme.

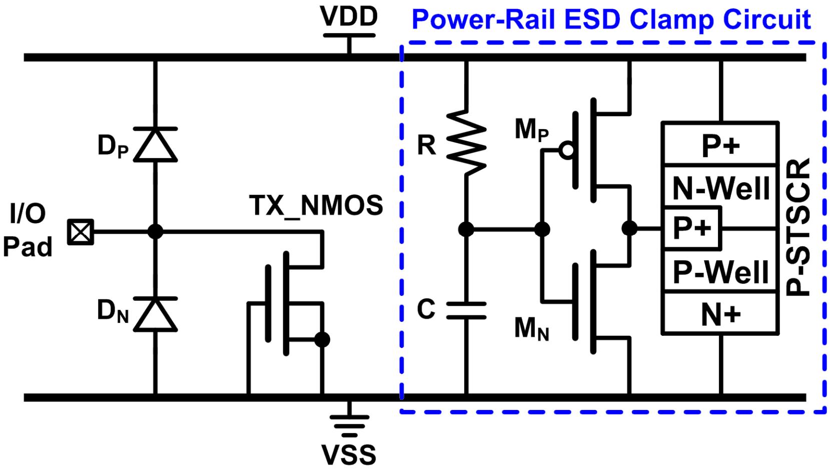


Fig. 6.9. Dummy transmitter NMOS (TX_NMOS) used as a test circuit to verify the effectiveness of the proposed ESD protection scheme in a transmitter (double diodes and active power-rail ESD clamp circuit).

6.3.3. ESD Levels of Dummy Receiver NMOS and Dummy Transmitter NMOS

The calculated DC junction capacitances of D_P with 45-µm and 55-µm junction perimeters are 88.1 fF and 118 fF, whereas the calculated DC junction capacitances of D_N with 45-µm and 55-µm junction perimeters are 59.1 fF and 73.1 fF. The HBM and machine-model (MM) ESD levels of the TX_NMOS and RX_NMOS with different diode junction perimeters are listed in Table 6.2. With the active power-rail ESD clamp circuit, the ESD protection diodes are assured to be operated in the forward-biased condition rather than the reverse-biased condition under all ESD-test pin combinatins. Therefore, high enough ESD robustness can be achieved in the RX_NMOS and TX_NMOS. The RX_NMOS with 45-µm diode junction perimeter has 2.5-kV HBM and 100-V MM ESD robustness. By using the ESD protection diodes with 55-µm junction perimeter, the HBM and MM ESD levels are improved to 3 kV and 150 V, respectively. In the TX_NMOS with 45-µm diode junction perimeter, the HBM and MM ESD levels are 3 kV and 300 V, respectively. With 55-µm diode junction perimeter, the HBM ESD level is improved to 3.5 kV with the MM ESD level unchanged. The TX_NMOS has higher NS- and ND-mode ESD levels as compared with those of the RX_NMOS, because the parasitic N+/P-well junction between the bulk and drain of the TX_NMOS discharges some ESD current. Moreover, it is found that the PS-mode ESD test is the most critical ESD-test pin combination for both RX_NMOS and TX_NMOS. In the following section, a modified design to improve the PS-mode ESD level is proposed.

Table 6.2

ESD Robustness of Dummy Receiver NMOS (RX_NMOS) and Dummy Transmitter NMOS (TX_NMOS) With Different Dimensions of ESD Protection Diodes

	Junction Perimeter		PS-Mode		NS-Mode		PD-Mode		ND-Mode	
	D_P	D_N	HBM	MM	HBM	MM	HBM	MM	HBM	MM
RX_NMOS	45 µm	45 µm	2.5 kV	100 V	3 kV	200 V	3 kV	150 V	3.5 kV	200 V
	55 µm	55 µm	3 kV	150 V	4 kV	200 V	4 kV	200 V	4 kV	250 V
TX_NMOS	45 µm	45 µm	3 kV	300 V	6 kV	450 V	3.5 kV	400 V	5 kV	300 V
	55 µm	55 µm	3.5 kV	300 V	6.5 kV	450 V	4.5 kV	450 V	5.5 kV	350 V

6.4. ESD-Protected 2.5-Gb/s High-Speed I/O Interface Circuit

After investigating the ESD robustness of RX_NMOS and TX_NMOS, this whole-chip ESD protection scheme is applied to a 2.5-Gb/s high-speed receiver interface circuit in a 130-nm CMOS process. Fig. 6.10 shows the schematic of the 2.5-Gb/s high-speed receiver interface circuit with the double-diode ESD protection scheme presented in the last section. The receiver interface circuit has the differential input stage. In the power-rail ESD clamp circuit, the ESD clamp device of P-STSCR is realized with 59.6-µm width. The diode junction perimeters of 35 µm and 55 µm were implemented in the ESD protection scheme shown in Fig. 6.10. As listed in Table 6.2, the RX_NMOS with the ESD protection diodes under 45-µm junction perimeter can sustain 2.5-kV HBM ESD robustness. In this high-speed receiver interface circuit, the ESD protection diodes with 35-µm junction perimeter were implemented to investigate its ESD robustness because lower parasitic capacitance from the ESD protection devices is preferred. Table 6.3 lists the dimensions of the ESD protection devices and the corresponding DC junction capacitance (by calculation) in each high-speed receiver interface circuit. In Receiver_1 (Receiver_2) with the diode junction perimeter of 35 µm (55 µm), the calculated capacitance from the ESD protection devices at the I/O pad is 108.3 fF (191 fF).

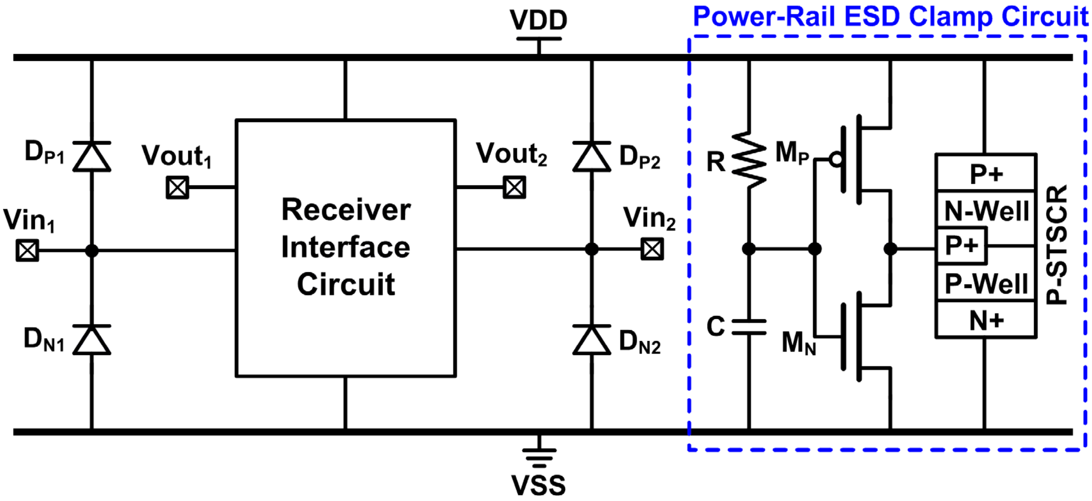


Fig. 6.10. 2.5-Gb/s high-speed receiver interface circuit with the first whole-chip ESD protection scheme (Receiver_1–Receiver_2).

Table 6.3
ESD Protection Design of Each High-Speed Receiver Interface Circuit

	ESD Protection Device Between I/O Pad and VDD		ESD Protection Device Between I/O Pad and VSS		Total C_{ESD}
	Device	C_{ESD}	Device	C_{ESD}	
Receiver_0	None	0 fF	None	0 fF	0 fF
Receiver_1	D_P (PJ = 35 μm)	63.2 fF	D_N (PJ = 35 μm)	45.1 fF	108.3 fF
Receiver_2	D_P (PJ = 55 μm)	117.9 fF	D_N (PJ = 55 μm)	73.1 fF	191 fF
Receiver_3	D_P (PJ = 35 μm)	63.2 fF	P-STSCR (W = 20 μm)	64.7 fF	127.9 fF
Receiver_4	D_P (PJ = 55 μm)	117.9 fF	P-STSCR (W = 20 μm)	64.7 fF	182.6 fF
Receiver_5	D_P (PJ = 35 μm)	63.2 fF	P-STSCR (W = 30 μm)	90.1 fF	153.3 fF
Receiver_6	D_P (PJ = 55 μm)	117.9 fF	P-STSCR (W = 30 μm)	90.1 fF	208 fF
Receiver_7	D_P (PJ = 35 μm)	63.2 fF	P-STSCR (W = 50 μm)	140.9 fF	204.1 fF
Receiver_8	D_P (PJ = 55 μm)	117.9 fF	P-STSCR (W = 50 μm)	140.9 fF	258.8 fF

It was mentioned that the PS-mode ESD test is the most critical ESD-test pin combination for the ESD protection scheme shown in Fig. 6.10. A modified design is proposed to improve the PS-mode ESD robustness, as shown in Fig. 6.11. In the proposed ESD protection scheme, the ESD protection diode between the I/O pad and VSS is replaced by the P-STSCR. The device dimensions in the power-rail ESD clamp circuit in Fig. 6.11 are identical to those in Fig. 6.10. Since the P-STSCR is already used in the power-rail ESD clamp circuit, the ESD detection circuit in the power-rail ESD clamp circuit can also be used to inject trigger current into the P-STSCRs at the I/O pads during ESD stresses. During

PS-mode ESD stresses, the ESD voltage is coupled from the I/O pad to VDD through D_P, and the P-STSCR devices can be turned on by the ESD detection circuit. When the P-STSCR at the I/O pad is turned on, it provides an ESD current path from the I/O pad to VSS. As a result, ESD current will flow through only the P-STSCR at the I/O pad instead of through D_P and the power-rail ESD clamp circuit. With fewer ESD protection devices along the ESD current path under PS-mode ESD tests, higher ESD robustness can be achieved. In the proposed design, the P-STSCR at the I/O pad was implemented with 20-µm, 30-µm, and 50-µm widths to investigate what ESD robustness can be achieved with different parasitic capacitances at the I/O pad. The dimensions of the ESD protection devices in the proposed ESD protection scheme and the corresponding junction capacitances (by calculation) are also listed in Table 6.3. In Receiver_3 (Receiver_4) with 20-µm wide P-STSCR between the I/O pad and VSS, the calculated parasitic capacitance at each I/O pad is 127.9 fF (182.6 fF) when D_P is realized with 35-µm (55-µm) junction perimeter. When the width of the P-STSCR between the I/O pad and VSS is increased to 30 µm, the calculated parasitic capacitances at each I/O pad is 153.3 fF (208 fF) in Receiver_5 (Receiver_6) with 35-µm (55-µm) D_P perimeter. With 50-µm wide P-STSCR between the I/O pad and VSS, Receiver_7 (Receiver_8) with 35-µm (55-µm) D_P perimeter has the parasitic capacitance of 204.1 fF (258.8 fF) at each I/O pad. To verify the effectiveness of the ESD protection schemes, the high-speed receiver interface circuit (Receiver_0) without ESD protection was also fabricated in the same process.

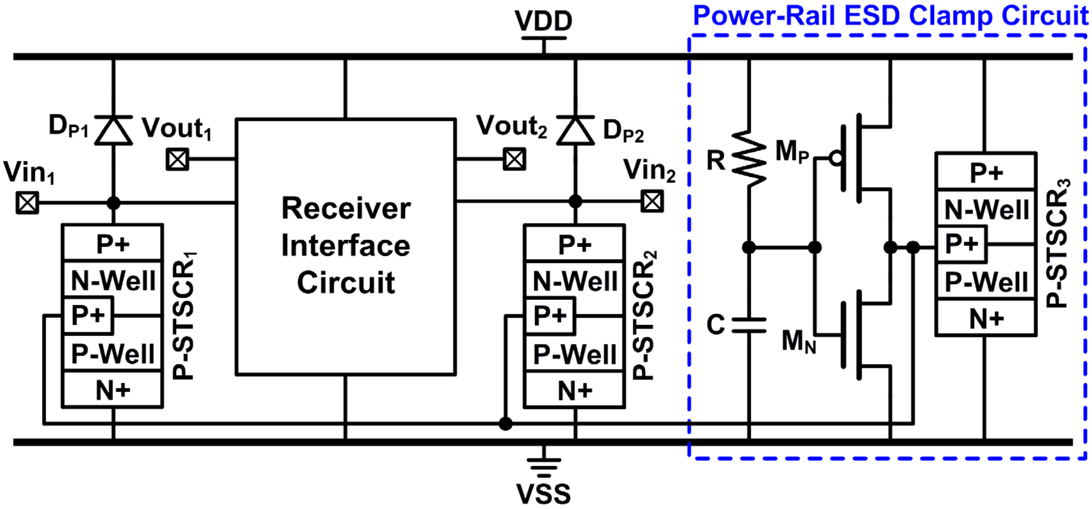


Fig. 6.11. 2.5-Gb/s high-speed receiver interface circuit with the second whole-chip ESD protection scheme (Receiver_3–Receiver_8).

To save the chip area of the ESD-protected high-speed receiver interface circuit, the

ESD protection devices at the input node, M_P, M_N, and the P-STSCR in the power-rail ESD clamp circuit were placed under the I/O pad. Fig. 6.12 shows the layout top view of the ESD protection devices under the bond pad in Receiver_1 and Receiver_2. The cross-sectional view of the ESD protection devices under the bond pad is shown in Fig. 6.13. By putting D_P and M_P together, only an N-well is needed. Similarly, only a P-well is needed because D_N and M_N are put together. The P-STSCR in the power-rail ESD clamp circuit is realized between the N-well and P-well regions. In Receiver_3 to Receiver_8, the P-STSCR between the I/O pad and VSS is also placed under the I/O pad. Besides saving the chip area, placing the ESD protection devices under the I/O pad reduces some parasitic capacitance at the I/O pad, because the bond-pad capacitance and the parasitic capacitance of the ESD protection devices are series connected between the I/O pad and the substrate.

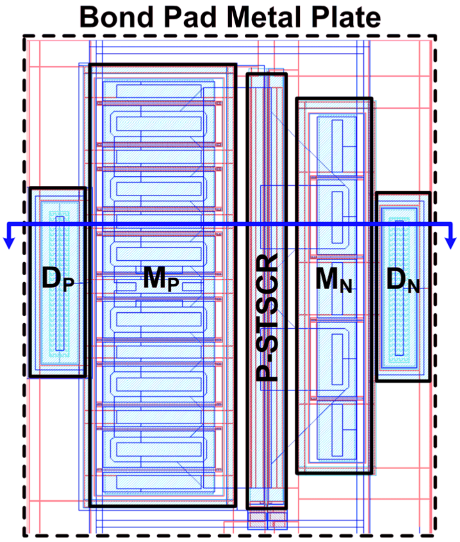


Fig. 6.12. Layout top view of the ESD protection devices under the bond pad.

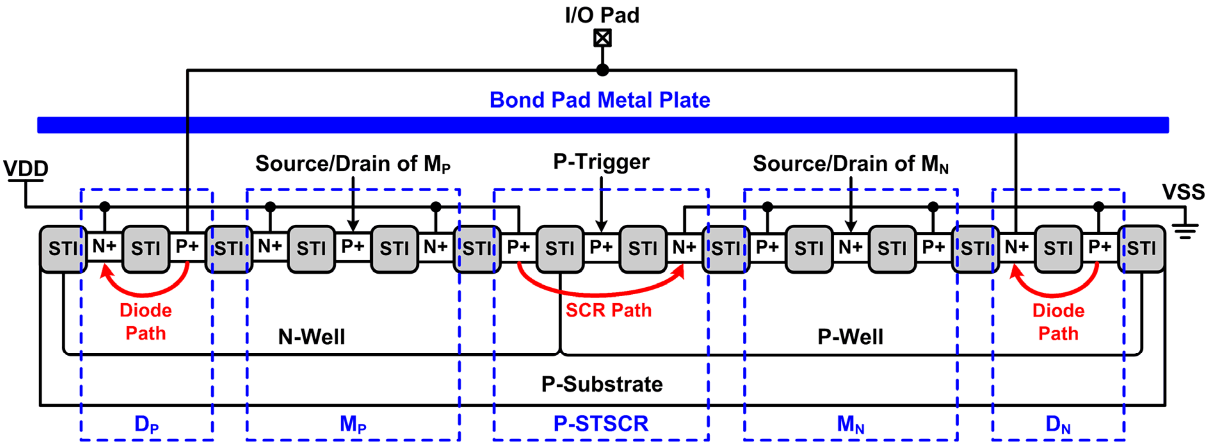


Fig. 6.13. Cross-sectional view of the ESD protection devices under the bond pad.

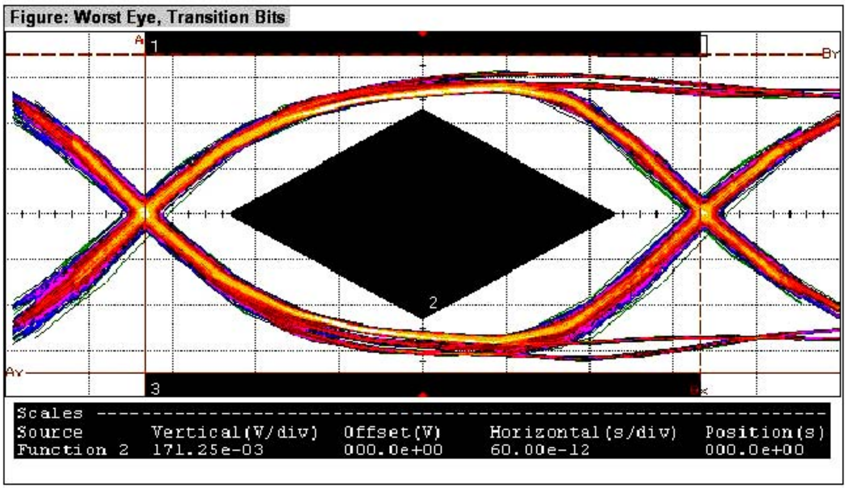
The nine high-speed receiver interface circuits were fabricated in a 130-nm CMOS process. Table 6.4 lists the HBM ESD levels of the nine fabricated high-speed receiver interface circuits under different ESD-test pin combinations. Without ESD protection, Reveiver_0 is very vulnerable to ESD, which fails at 0.5-kV HBM ESD test. With the double-diode ESD protection scheme, Receiver_1 and Receiver_2 have 2-kV and 3-kV HBM ESD levels, respectively. By using the P-STSCR between the I/O pad and VSS, the PS-mode ESD robustness can be improved. With 20-μm, 30-μm, and 50-μm wide P-STSCR between the I/O pad and VSS, the PS-mode HBM ESD level is improved to 4 kV, 5 kV, and 6.5 kV, respectively. Since the ESD protection device between the I/O pad and VDD is not changed in the proposed ESD protection scheme, the PD-mode ESD level does not have significant difference under the same D_P size.

Table 6.4

HBM ESD Robustness of the High-Speed Receiver Interface Circuits

	PS-Mode	**NS-Mode**	**PD-Mode**	**ND-Mode**
Receiver_0	**<0.5 kV**	**<0.5 kV**	**<0.5 kV**	**<0.5 kV**
Receiver_1	**2.5 kV**	**2 kV**	**2.5 kV**	**2.5 kV**
Receiver_2	**3 kV**	**3 kV**	**3.5 kV**	**3 kV**
Receiver_3	**2.5 kV**	**2.5 kV**	**2.5 kV**	**1.5 kV**
Receiver_4	**4 kV**	**2 kV**	**4.5 kV**	**2 kV**
Receiver_5	**4 kV**	**2.5 kV**	**2.5 kV**	**2.5 kV**
Receiver_6	**5 kV**	**3.5 kV**	**4.5 kV**	**2.5 kV**
Receiver_7	**6 kV**	**3.5 kV**	**2.5 kV**	**3 kV**
Receiver_8	**6.5 kV**	**3.5 kV**	**4.5 kV**	**3.5 kV**

The double-diode ESD protection scheme had been applied to an IC product with 2.5-Gb/s high-speed front-end interface fabricated in a 130-nm CMOS process. In this high-speed front-end chip, two P+/N-well diodes with 24.36-μm width and 2.74-μm length were used between the I/O pad and VDD, whereas two N+/P-well diodes with 26.46-μm width and 4.84-μm length were used between the I/O pad and VSS. The total calculated parasitic capacitance from the ESD protection diodes is 336 fF. The measured eye diagram of this 2.5-Gb/s high-speed front-end interface circuit is shown in Fig. 6.14. After the ESD protection devices are applied at the I/O pad, the measured eye diagram can be still satisfactory if the parasitic capacitance from the ESD protection devices is within the design budget.



```
Scales -------------------------------------------------------------
Source       Vertical(V/div)  Offset(V)    Horizontal(s/div)  Position(s)
Function 2   171.25e-03       000.0e+00    60.00e-12          000.0e+00
```

Fig. 6.14. Measured eye diagram of the 2.5-Gb/s high-speed I/O interface circuit in a 130-nm CMOS process.

6.5. Discussions and Design Guidelines

According the ESD test results, using larger ESD protection devices can achieve higher ESD robustness. By comparing the PS-mode ESD robustness, it has been verified that using the P-STSCR between the I/O pad and VSS can improve the PS-mode ESD robustness under the same parasitic capacitance. Besides P-STSCR between the I/O pad and VSS, applying the N-STSCR between VDD and the I/O pad is expected to improve the ND-mode ESD robustness. Therefore, applying the double-SCR ESD protection scheme (proposed in 5.3.4) for the high-speed I/O interface circuit is recommended. In the double-SCR ESD protection scheme, the N-well of the P-STSCR and the P-well of the N-STSCR are suggested to connect to VDD and VSS, respectively. With this configuration, the PD-mode ESD current path is provided by the parasitic P+/N-well diode in the P-STSCR, whereas the NS-mode ESD current path is provided by the parasitic N+/P-well diode in the N-STSCR. Thus, both the SCR path and the parasitic diode path in the substrate-triggered SCR need to be carefully designed to achieve efficient ESD current paths. With proper design of the P-STSCR and N-STSCR at the I/O pad, the double-SCR ESD protection scheme can be implemented with low parasitic capacitance to achieve high ESD robustness under all ESD-test pin combinations.

6.6. Summary

In this chapter, the ESD protection design for high-speed I/O interface circuits in a 130-nm CMOS process is presented in detail. The parasitic capacitances and the ESD levels of the stand-alone ESD protection diodes were investigated in the beginning. To estimate the ESD robustness of general receiver and transmitter interface circuits, the RX_NMOS and TX_NMOS with different ESD protection device dimensions were fabricated and their ESD levels were measured. Then, the double-diode ESD protection scheme was applied to a high-speed receiver interface circuit. To improve the ESD robustness under PS-mode ESD test, which is the most critical ESD-test pin combination for the double-diode ESD protection scheme, the ESD protection diode between the I/O pad and VSS was replaced by the P-STSCR in the proposed design. ESD test results have shown that the PS-mode ESD level is improved by using the proposed ESD protection scheme. With the ESD protection design methodology proposed in this chapter, the two most important requirements of ESD protection design for high-speed I/O interface circuits, which are high ESD robustness and low parasitic capacitance, can be met simultaneously.

Chapter 7

Investigation on Board-Level Charged-Device-Model ESD Issue in IC Products

In this chapter, the impacts caused by board-level charged-device-model (CDM) electrostatic discharge (ESD) events on integrated circuit (IC) products are investigated. The mechanism of board-level CDM ESD event is introduced first. Based on this mechanism, an experiment is performed to investigate the board-level CDM ESD current waveforms under different sizes of printed circuit boards (PCBs), different charged voltages, and different series resistances along the discharging path. Experimental results show that the discharging current peak strongly depends on the PCB size, charged voltage, and series resistance. Moreover, chip-level and board-level CDM ESD levels of several test devices and test circuits fabricated in CMOS processes are characterized and compared. The test results show that the board-level CDM ESD level of the test circuit is lower than the chip-level CDM ESD level of the test circuit, which demonstrates that the board-level CDM ESD event is more critical than the chip-level CDM ESD event. In addition, failure analysis reveals that the failure in the test circuit under board-level CDM ESD test is much severer than that under chip-level CDM ESD test. [137], [138].

7.1. Background

With the advance of CMOS processes, integrated circuits (ICs) have been fabricated with thinner gate oxides to achieve higher speed and lower power consumption. However, electrostatic discharge (ESD) was not scaled down with CMOS technology. Thus, ESD protection design in nanoscale CMOS processes becomes a challenging task. Among the three component-level (or called as chip-level) ESD test standards, which are human body model (HBM) [6], machine model (MM) [7], and charged device model (CDM) [16], [17], CDM becomes more and more critical because of the thinner gate oxide in nanoscale CMOS transistors and the larger die size for the application of system on chip (SoC). The thinner gate oxide causes a lower gate-oxide breakdown voltage, which makes the MOS transistor more vulnerable to ESD. An IC with larger die size stores more static charges, which leads to larger discharging current during CDM ESD events. CDM ESD current has the features of huge peak current and short duration. Furthermore, CDM ESD current flows from the chip substrate to the external ground, whereas HBM and MM ESD currents are injected from the external ESD source through the zapped pin into the IC. Thus, effective on-chip ESD protection design against CDM ESD stresses has become more challenging to be implemented.

Besides chip-level CDM ESD issue, board-level CDM ESD issue becomes more important recently, because it often causes the ICs to be damaged after the IC is installed to the circuit board of electronic system. For example, board-level CDM ESD events often occur during the module function test on the circuit board of electronic system. Even though the IC has been designed with good chip-level ESD robustness, it would still be very weak in board-level CDM ESD test. The reason is that the discharging current during the board-level CDM ESD event is significantly larger than that of the chip-level CDM ESD event. There are several papers addressing the phenomenon of the board-level CDM ESD events on real IC products [18], [19]. In these two previous works, the ICs which already passed the component-level ESD specifications were still returned by customers because of ESD failure. After performing the field-induced CDM ESD test on the ICs mounted on the printed circuit board (PCB), the failure is the same as that happened in the customer returned ICs. This indicates that the real-world charged-board-model (CBM) ESD damage can be duplicated by the board-level CDM ESD test. The previous works have demonstrated that the board-level CDM ESD events indeed exist, and they should be taken into consideration for all IC products.

In this chapter, the board-level CDM ESD issue for ICs is comprehensively addressed. The mechanisms of both chip-level and board-level CDM ESD events are developed and compared in section 7.2. The discharging current waveforms during board-level CDM ESD events under different measurement conditions are investigated in section 7.3. The chip-level and board-level CDM ESD tests are performed on some test devices and test circuits in section 7.4. Moreover, failure analysis is also performed to investigate the difference between the failure mechanisms under chip-level and board-level CDM ESD tests.

7.2. CDM ESD Events

7.2.1. Chip-Level CDM ESD Event

During the assembly of IC products, charges could be stored within the body of IC products due to induction or tribocharging. Once a certain pin of the IC is suddenly grounded, the static charges originally stored within the IC will be discharged through the grounded pin, which is called as the CDM ESD event and shown in Fig. 7.1. The CDM ESD event delivers a large amount of current in a very short time. There are many situations that the pins of an IC are grounded. For example, the pin may touch grounded metallic surfaces or the pin may be touched by grounded metallic tools. Different ICs have different die sizes, so their equivalent parasitic capacitances (C_D) are totally different from one another. Thus, different ICs have different peak currents and different CDM ESD levels. When a device under test (DUT) with the equivalent capacitance of 4 pF is under 1-kV CDM ESD test, the CDM ESD current rises to more than 15 A within several nanoseconds [139]. As compared with HBM and MM ESD events, the discharging current in CDM ESD event is not only larger, but also faster. Since the duration of CDM ESD event is much shorter than those of HBM and MM ESD events, the internal circuits may be damaged during CDM ESD events before the ESD protection circuit is turned on. When the signal frequency is increased, the capacitor becomes a low-impedance device. Thus, the CDM ESD current is most likely to flow through the capacitive structures in ICs. In CMOS ICs, the gate oxides of MOS transistors are capacitive structures, so the gate oxide is most likely to be damaged during CDM ESD events. In nanoscale CMOS processes, the gate-oxide thickness becomes thinner, which increases the equivalent capacitance (and thus reduces the impedance) per unit area. Consequently, the gate oxides of MOS transistors in nanoscale CMOS processes are more vulnerable to CDM ESD stresses. Moreover, more functions are integrated into a single chip in SoC applications, which increases the die size and thus increases the die capacitance. Under the same charged voltage, larger capacitance stores more static charges, so the CDM ESD current is larger with larger DUT capacitance. Since larger die size denotes larger equivalent capacitance, CDM ESD current is larger for ICs with larger die sizes. With larger die size and MOS transistors using thinner gate oxide, nanoscale CMOS ICs are very sensitive to ESD, especially CDM ESD events.

During the manufacturing of IC products, some of the steps had been reported to cause chip-level CDM ESD events, which leads to yield loss. There are several works addressing the cause of chip-level CDM ESD events during manufacturing of IC products [140]–[142]. In the packaging process of plastic-leaded-chip-carrier (PLCC) packages, the chips are induced to store static charges when they are carried by the carrier of the machine. When a certain pin of the charged chip is connected to external ground, a CDM ESD event may occur. To solve this problem, the balanced ionizer can be utilized in the manufacturing environment to neutralize the static charges stored in the chips and the machines [140].

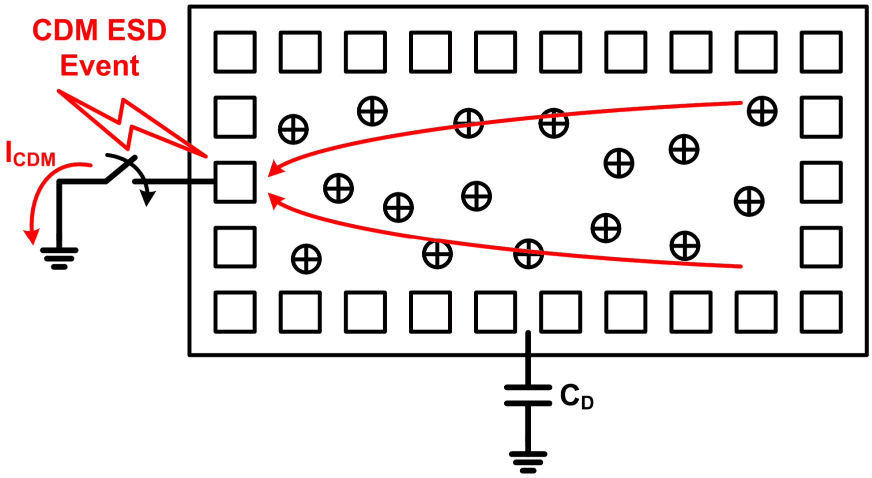


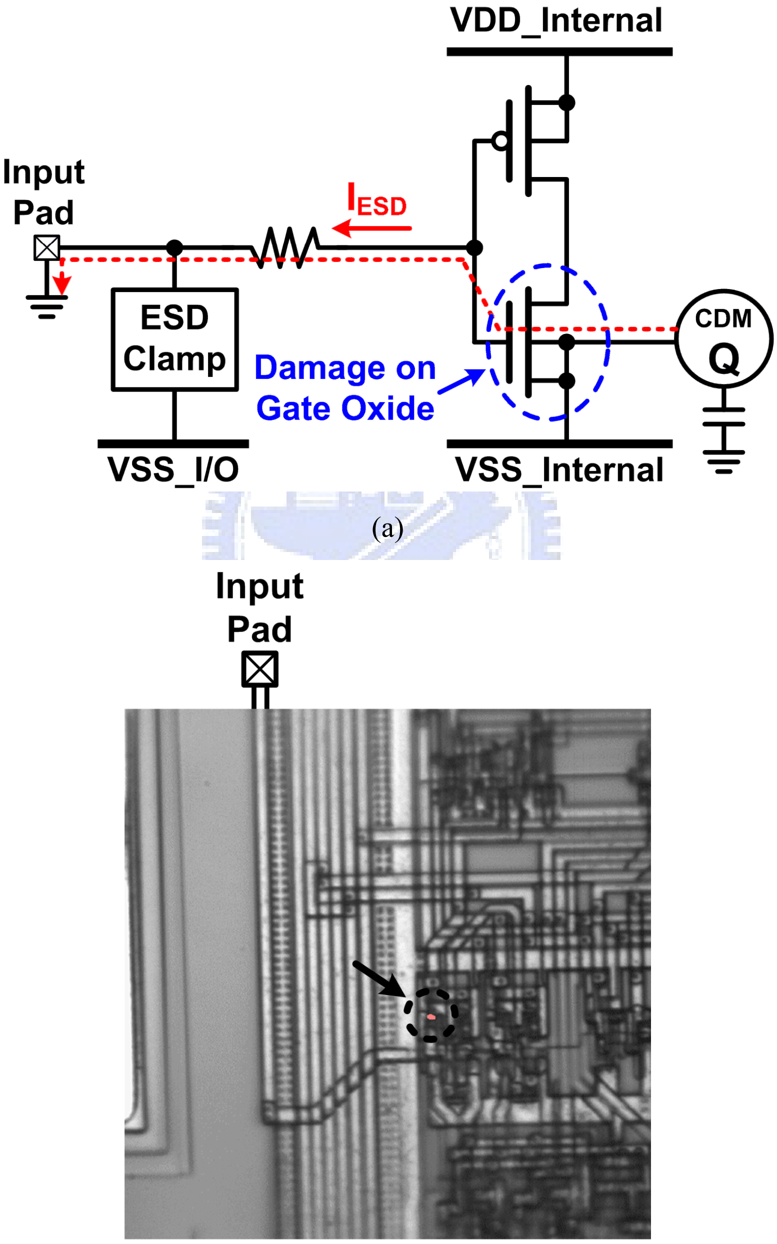
Fig. 7.1. CDM ESD event: When a certain pin is grounded, the stored charges in the integrated circuit (IC) will be quickly discharged through the grounded pin.

An IC fabricated in a 0.8-µm CMOS process had been found to have leakage current when it was normally biased, but it worked well during function test after fabrication. Failure analysis demonstrated that the gate oxide of the NMOS in the input buffer was damaged by CDM ESD event. After study, it was found that the socket of the IC tester was charged during function test, which induced the tested IC to store static charges. After finishing function test, the charged IC was placed on the grounded metallic table, and the CDM ESD event occurred to damage the IC which has passed function test [141].

During fabrication of ICs, separating the tape and die after cutting the die from wafer causes substantial charge accumulation in the die. Measured by the Faraday cup, it had been reported that the CDM ESD voltage could be more than 1000 V during the separation of the tape and die. Such a high CDM ESD voltage may damage the IC product [142].

7.2.2. Case Study on Chip-Level CDM ESD Damage

An input buffer fabricated in a 0.8-µm CMOS process is shown in Fig. 7.2(a). This chip passes 2-kV HBM and 200-V MM ESD tests. Although this chip is equipped with ESD protection circuit at its input pad, it is still damaged after 1000-V CDM ESD test. As shown in Fig. 7.2(b), the failure point after CDM ESD test is located at the gate oxide of the NMOS in the input buffer. Duo to consideration of noise isolation between I/O cells and internal circuits, the VSS of I/O cells (VSS_I/O) and the VSS of internal circuits (VSS_Internal) are separated in the chip layout. As a result, the ESD clamp device at the input pad can not efficiently protect the gate oxide during CDM ESD stresses, because there is no connection between VSS_I/O and VSS_Internal. The CDM ESD current which damages the gate oxide of NMOS is shown by the dash line in Fig. 7.2(a).



(a)

(b)

Fig. 7.2. (a) CDM ESD current path in an input buffer. (b) The failure point is located at the gate oxide of the input NMOS.

Fig. 7.3 is the failure picture of another IC after CDM ESD test. This IC was fabricated in a 0.5-μm CMOS process. The scanning-electron-microscope (SEM) picture had proven that the failure caused by the CDM ESD event is located at the poly gate of a MOS transistor in the internal circuit that is connected to some input pad. In these two cases, the charges stored in the body of chip still flow through the gate terminal of the input MOS transistor in the internal circuits to damage its gate oxide during CDM ESD stresses, even though ESD protection circuits have been applied to the input pad. According to the previous works, the pins near the corners in IC products are more prone to suffer CDM ESD events, because the corner pins are usually first touched by external ground during transportation or assembly [143]. In addition to HBM and MM ESD protection, the ESD protection strategy against CDM ESD stresses is another important consideration in component-level ESD protection design.

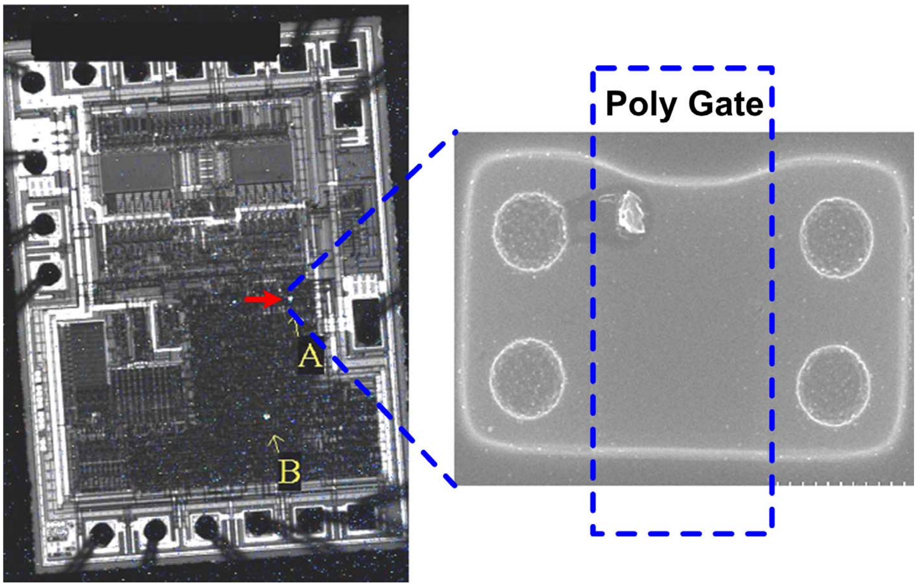

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Fig. 7.3. After chip-level CDM ESD test, the failure point is located at the gate oxide of an NMOS in the internal circuit.

7.2.3. Board-Level CDM ESD Event

In microelectronic systems, IC chips must be attached to the PCB. Before the attachment, static charges could be stored in the body of the chip or the metal traces on the dielectric layer in the PCB. During the attachment, the static charges originally stored in the IC chip and the PCB will be redistributed, as illustrated in Fig. 7.4. Fig. 7.5 illustrates the charge redistribution mechanism. C_1 and C_2 denote the parasitic capacitances of the IC chip and the PCB, respectively. Usually C_2 is much larger than C_1. The initial voltages across C_1 and C_2

are V_1 and V_2, respectively. C_1 and C_2 are not connected in the beginning. When the IC chip is attached to the PCB, C_1 and C_2 are shorted. Consequently, the voltages across C_1 and C_2 will become

$$V_{Final} = \frac{C_1 \times V_1 + C_2 \times V_2}{C_1 + C_2} \tag{7.1}$$

after they are connected together. The instantaneous current during the attachment of IC chip to PCB will be increased if the initial voltage difference between the IC chip and PCB is larger. The current peak during the charge redistribution may be larger than 10 A, which can easily damage the IC to cause a CDM-like failure. This is one of the examples of board-level CDM ESD events. Moreover, installing the modules to the system during the assembly of microelectronic products may also cause board-level CDM ESD events. To mitigate this impact, the balanced ionizer can be utilized in the manufacturing environment to neutralize the static charges stored in the chips and PCBs.

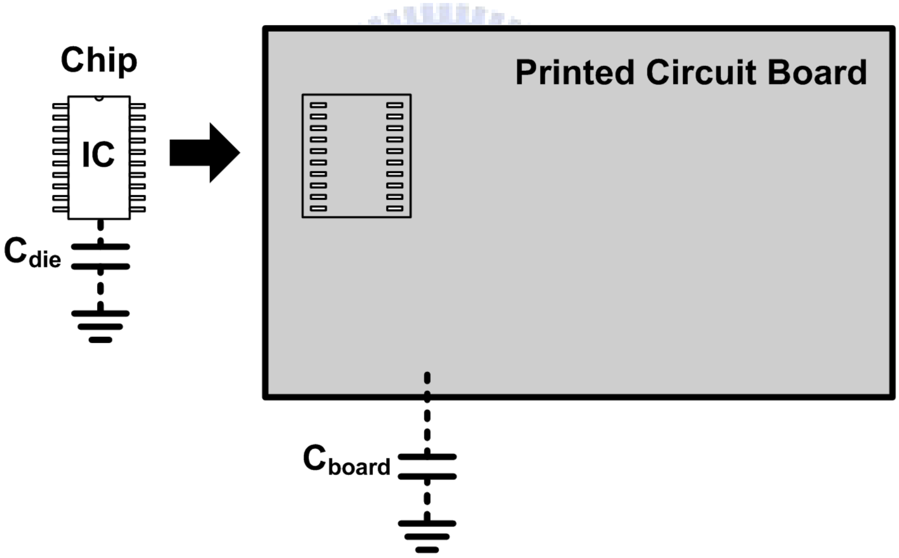


Fig. 7.4. The charges stored in the printed circuit board (PCB) and the chip will be redistributed when the chip is attached to the PCB.

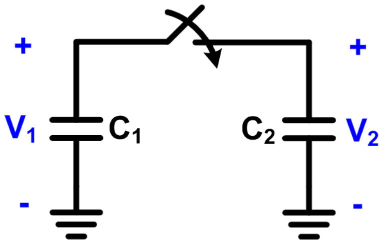


Fig. 7.5. When two capacitors with different voltages are shorted, charge redistribution will occur.

After the chips are attached to the PCB, certain pins in the PCB may be connected to low potential or accidentally grounded during module function test, as illustrated in Fig. 7.6. In this situation, the charges originally stored in the chips and the PCB will be quickly discharged through the grounded pin to damage the chips on the PCB. If the voltages across the equivalent capacitances of the chips and PCB are larger, more charges are stored, which leads to larger discharging current. To solve this problem, ESD dischargers consisting of large resistances (~ MΩ) can be used to ground the pins of PCB before module function test. Although there is still current flowing through the chips, the current peak is significantly reduced by the large series resistance. As a result, the chip can be protected from being damaged by the larger discharging current in board-level CDM ESD events during module function test.

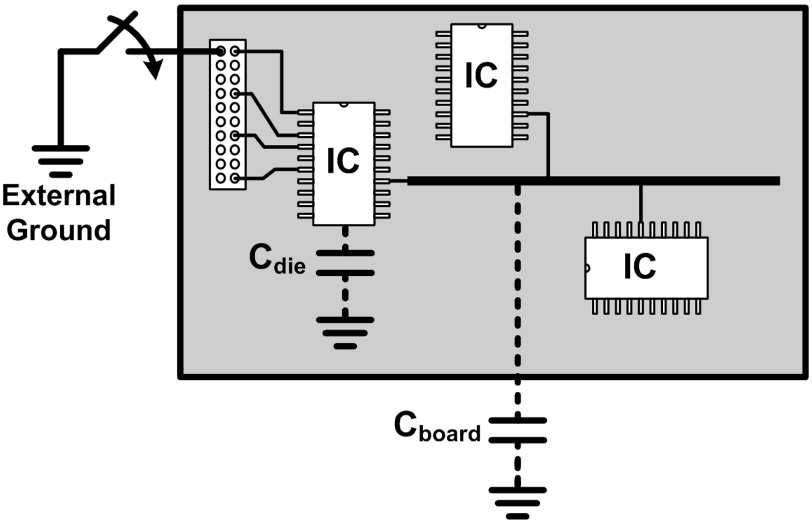


Fig. 7.6. When a certain pin of the PCB is grounded during function test, huge current will flow from the PCB through the IC.

In the assembly and testing of an LCD monitor, board-level CDM ESD events may often occur, too. As shown in Fig. 7.7, when the driver ICs are attached to the LCD panel, charge transfer occurs, which causes board-level CDM ESD current flowing between the driver ICs and LCD panel to damage them. Moreover, the driver IC can be also damaged by such board-level CDM ESD events when a certain pin of the driver IC on panel is accidentally grounded or connected to low potential during panel function test. The board-level CDM ESD current paths in such a situation are shown by the dash lines in Fig. 7.8. Since the on-glass thin-film transistors (TFTs) in LCD panel have higher operation voltage than that of the most digital ICs, the core circuits and I/O cells of LCD driver ICs have different operating

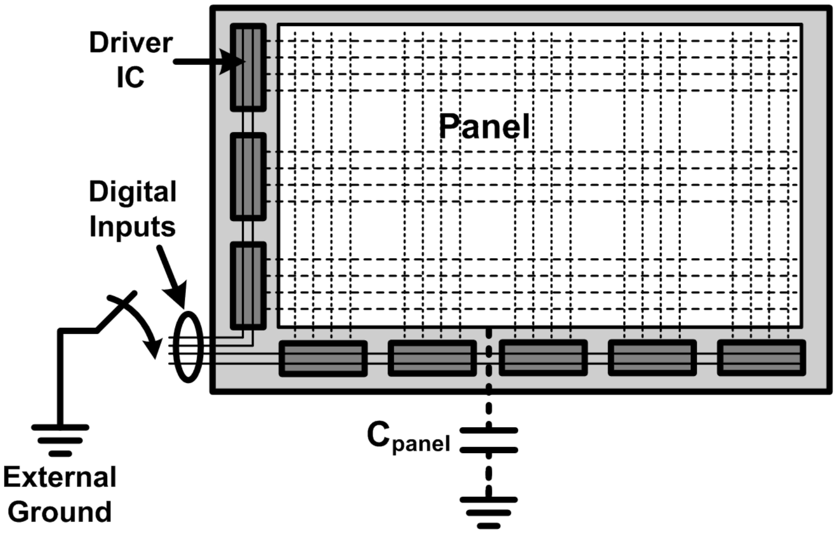


Fig. 7.7. When the driver IC is attached to the LCD panel during manufacturing, the charges originally stored in the LCD panel will be transferred to the driver IC, which causes board-level CDM ESD event. During panel function test, connecting the pins of the driver IC to ground will also induce the board-level CDM ESD event.

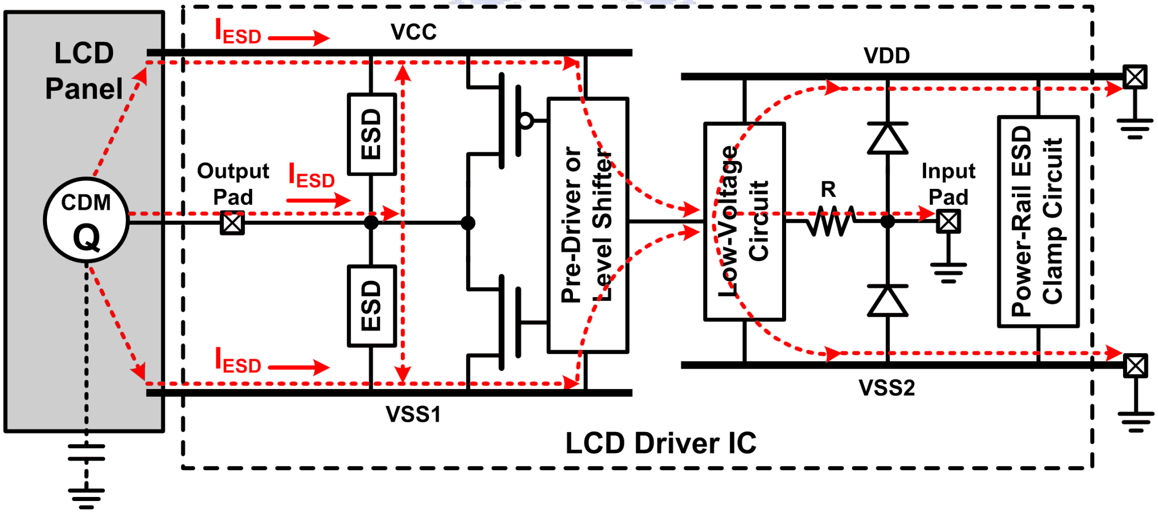


Fig. 7.8. When the pins of the driver IC are grounded, board-level CDM ESD current will flow from the LCD panel through the interface circuits within driver IC to the grounded pins.

voltages (VCC and VDD). Such ICs with multiple power domains have individual power pads and ground pads for each power domain. Once the aforementioned board-level CDM ESD events occur, ESD current will flow from the LCD panel through the output pad of the driver IC into the driver IC. Although ESD protection circuits have been applied to each output pad of the driver IC to bypass ESD current to the power pad (VCC) or ground pad (VSS1) within the power domain, the interface circuits between different power domains are often damaged during such board-level CDM ESD events due to the disconnection between the power pads or ground pads in different power domains. To solve this problem, ESD protection devices should be inserted between the power pads or ground pads in different power domains to provide ESD current paths between the separated power domains, as shown in Fig. 7.9 [144].

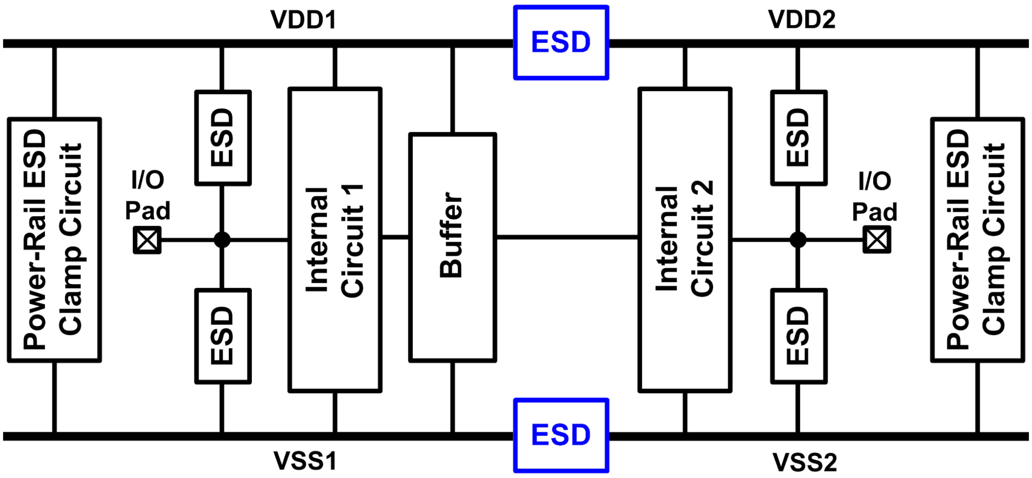


Fig. 7.9. ESD protection devices are inserted between different power domains to provide ESD current paths between the separated power domains.

7.3. Dependence of Current Waveforms on the Board Size in Board-Level CDM ESD Event

Recently, the simulation of CBM ESD event had been performed to evaluate the discharging current under different charged board dimensions [145]. Besides, the field induced charged board model (FICBM) ESD test has been performed on the microelectronic products [146]. In this section, different PCB sizes, different charged voltages, and different series resistances in discharging path are measured to explore their effects on board-level CDM ESD events.

7.3.1. Discharging Without Series Resistor

In the board-level CDM ESD event, ESD current is discharged from the charged PCB to the grounded pin of the chip on the PCB. To emulate the board-level CDM ESD event, the measurement setup with two-sided PCB shown in Fig. 7.10 was utilized in this study. The top side of the PCB was charged with some potential level, whereas the bottom side of PCB is relatively grounded. Four PCB sizes are used in the experiment, which are the A4 size (30 cm × 20 cm), 1/2 A4 size (20 cm × 15 cm), 1/4 A4 size (15 cm × 10 cm), and 1/8 A4 size (10 cm

× 7.5 cm). The charged voltage ranges from 20 V to 600 V. With the identical dielectric thickness, the capacitances of the PCBs are linearly proportional to the size of the PCB. The capacitances of the A4-sized, 1/2-A4-sized, 1/4-A4-sized, and 1/8-A4-sized PCBs in this work are 1.94 nF, 970 pF, 485 pF, and 242.5 pF, respectively. The top side of PCB was charged by the Tektronix 370B curve tracer through a 10-MΩ resistor, which was used to limit the charging current. The HP 34401A multimeter was used to monitor the charged voltage on the top side of PCB. After the top side of PCB was charged to some specified voltage level, it was grounded manually and the discharging current waveform was observed by the Tektronix 3054B oscilloscope with the Tektronix CT1 current probe.

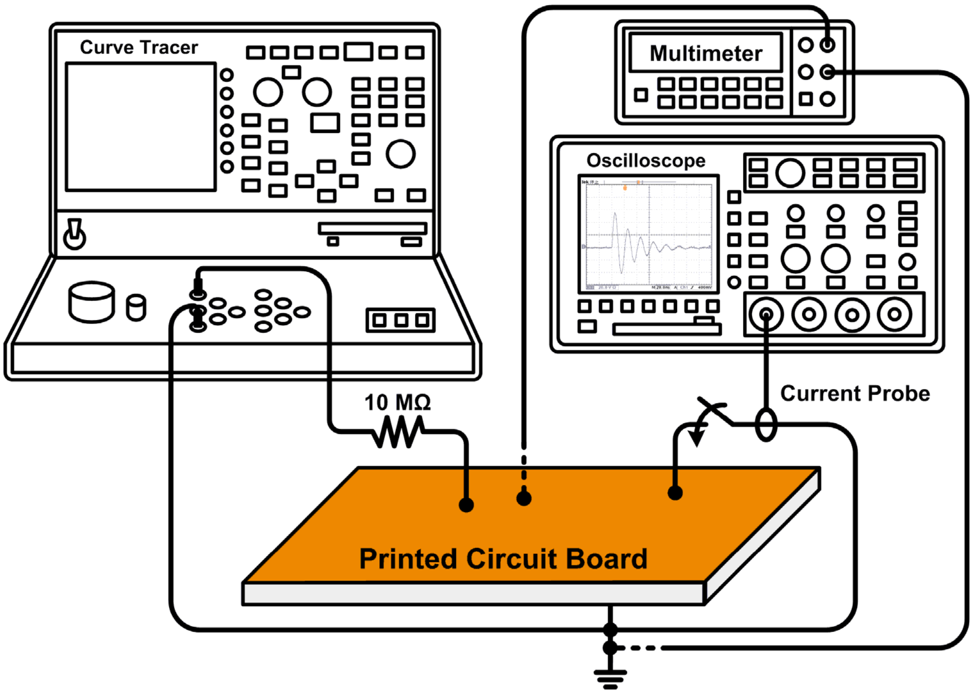
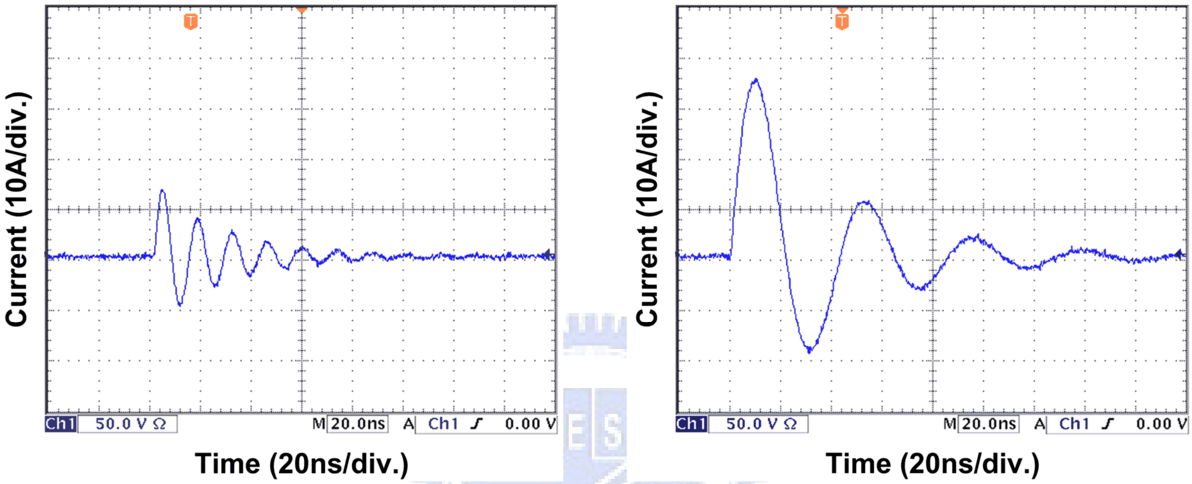


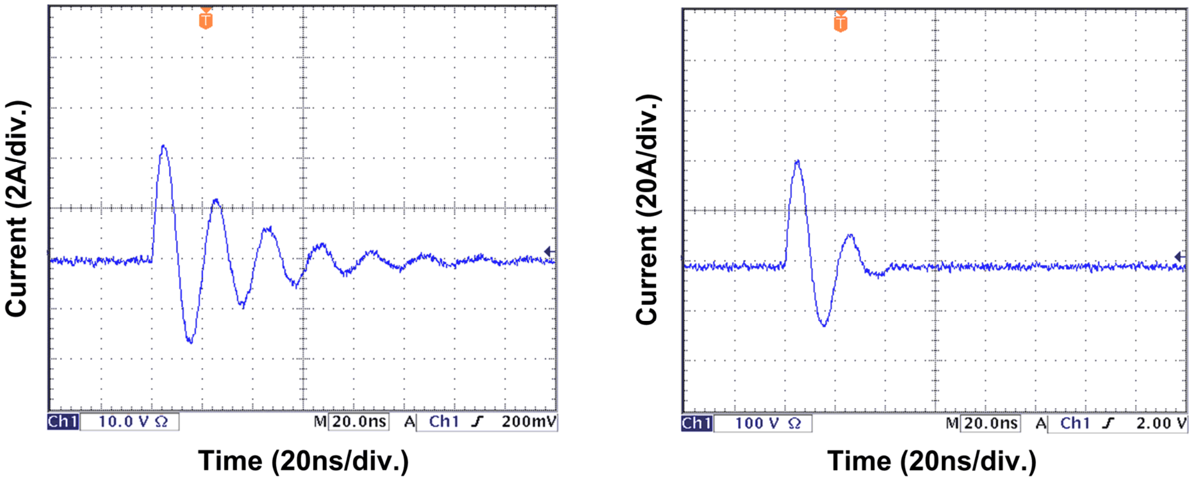
Fig. 7.10. Experimental setup to investigate the current waveforms under board-level CDM ESD events.

The measured discharging current waveforms from the 1/8-A4-sized and A4-sized PCB under the charged voltage of 100 V are shown in Fig. 7.11(a) and (b), respectively. Under the charged voltage of 100 V, the peak discharging currents of the 1/8-A4-sized and A4-sized PCBs are 14 A and 36 A, respectively. With the same PCB size of 1/4 A4, the measured discharging current waveforms under the charged voltages of 20 V and 200 V are shown in Fig. 7.12(a) and (b), respectively. The peak discharging current from the 1/4-A4-sized PCB is increased from 4.4 A (under the charged voltage of 20 V) to 42 A (under the charged voltage of 200 V). The peak discharging currents under different PCB sizes and different charged voltages are compared in Fig. 7.13. Under the same PCB size, higher charged voltage leads to higher peak discharging current. Larger PCB has larger capacitance, which can store more charges in the PCB. Thus, larger PCB provides higher peak discharging current under the same charged voltage. This experiment showed that the board-level CDM ESD event can generate huge current through the discharging path. Without the series resistor along the discharging path, the discharging current waveforms exhibit underdamped sinewave-like characteristics.



(a) (b)

Fig. 7.11. Measured board-level CDM ESD current waveforms from (a) 1/8-A4-sized PCB and (b) A4-sized PCB under 100-V charged voltage.



(a) (b)

Fig. 7.12. Measured board-level CDM ESD current waveforms from 1/4-A4-sized PCB under (a) 20-V and (b) 200-V charged voltage.

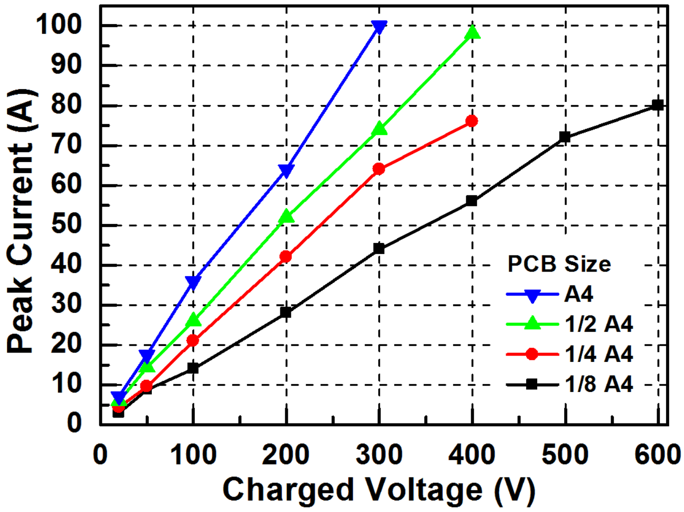


Fig. 7.13. Board-level CDM ESD peak currents under different charged voltages and different PCB sizes.

7.3.2. Discharging With Series Resistor

In the board-level CDM ESD experiment without the series resistor, the peak discharging currents are quite large. To reduce the peak discharging current, a series resistor was inserted along the discharging path to investigate the reduction of the discharging current, as illustrated in Fig. 7.14. The series resistances ranging from 10 Ω to 100 kΩ were used in this study. With this measurement setup, the dependence of the discharging current on series resistance can be investigated. Fig. 7.15(a) and (b) show the measured discharging current waveforms of the 1/2-A4-sized PCB with 100-Ω and 10-kΩ series resistances under 100-V charged voltage, respectively. As compared with the same PCB size and the same charged voltage without the series resistor, the peak discharging currents with the series resistances of 100 Ω and 10 kΩ were reduced from 26 A to 2.08 A and 20 mA, respectively. With the series resistor along the discharging path, the peak discharging current can be significantly reduced. Besides, no underdamped sinewave-like characteristics were observed when the series resistances were larger than 10 Ω. The peak discharging currents under different series resistances are compared in Fig. 7.16. The duration in which the discharging current is larger than 5% of its maximum value is defined as the discharging time. The discharging time becomes longer if a larger series resistance is used. The discharging times under different series resistances are compared in Fig. 7.17. Larger series resistance leads to longer discharging time due to the larger RC time constant. This experiment successfully demonstrates the effectiveness of the ESD discharger proposed in section 7.2.3, which consists of large series resistances to suppress the discharging current during board-level

CDM ESD events.

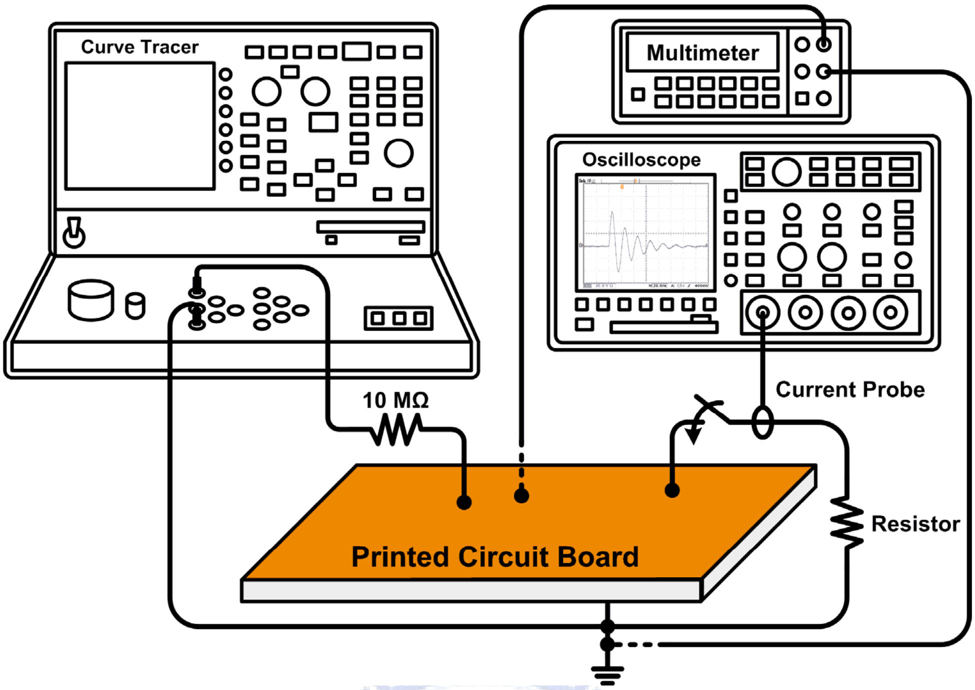
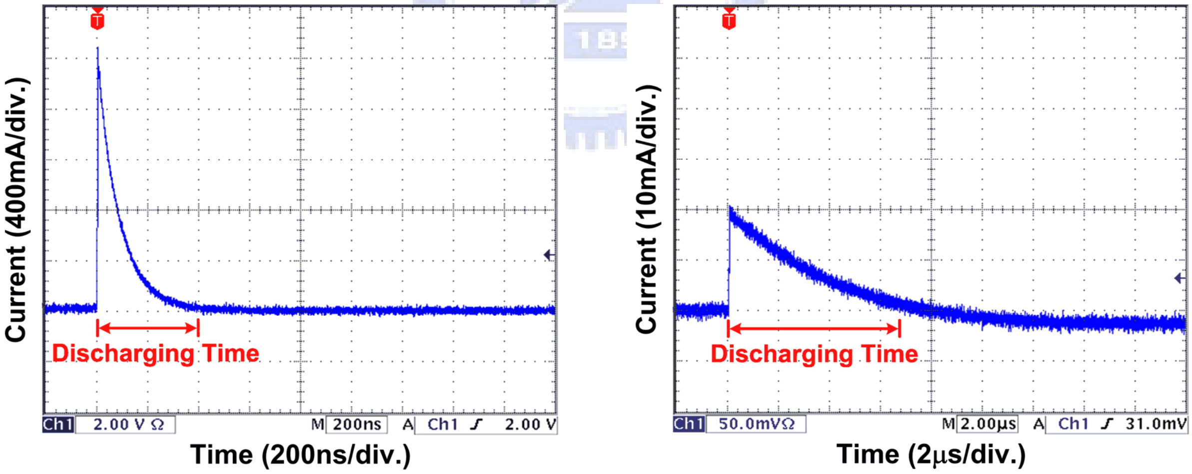


Fig. 7.14. Experimental setup to investigate the current waveforms under board-level CDM ESD events with a series resistor along the discharging current path.



(a) (b)

Fig. 7.15. Measured board-level CDM ESD current waveform of the 1/2-A4-sized PCB with (a) 100-Ω and (b) 10-kΩ series resistances along the discharging path under 100-V charged voltage.

7.4. Verifications With Test Devices and Test Circuits

After investigation on the board-level CDM ESD currents under different test conditions, the board-level CDM ESD test is performed to the CMOS ICs. There are three components to

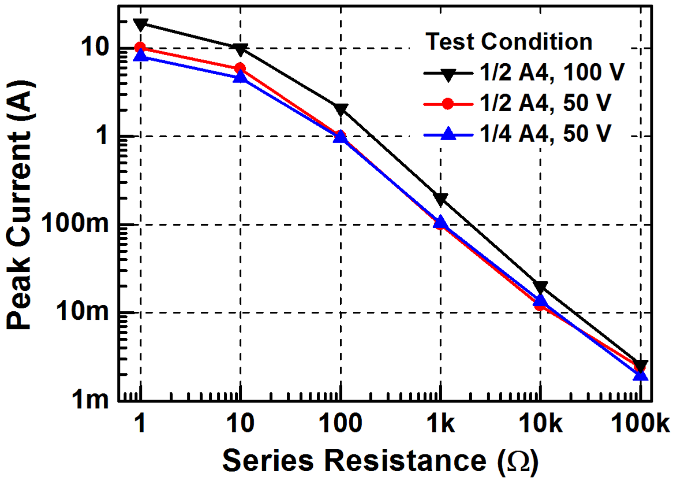


Fig. 7.16. Board-level CDM ESD peak currents under different series resistances.

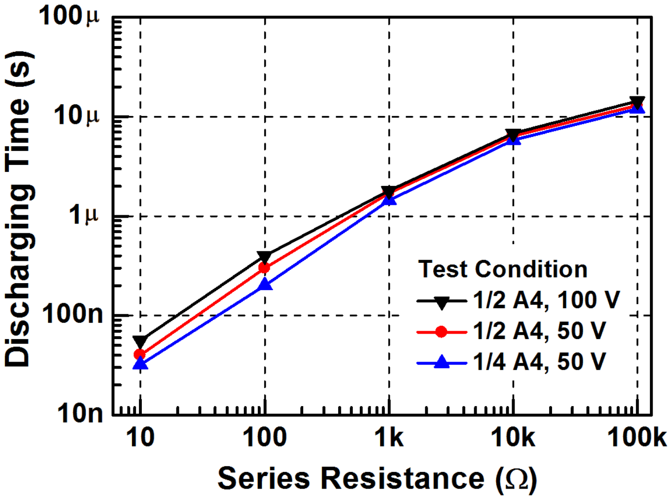


Fig. 7.17. Discharging times of board-level CDM ESD events under different series resistances.

be tested, which are the stand-alone gate-grounded NMOS (GGNMOS), dummy receiver NMOS (RX_NMOS), and 2.5-Gb/s high-speed receiver interface circuit. The packages used in all of the chip-level and board-level CDM ESD tests are the 40-pin dual-in-line (DIP) package. In the traditional chip-level CDM ESD test, only the IC chip (DUT) is put on the charging plate of the field-induced CDM ESD tester, as that shown in Fig. 7.18. However, the IC chip and the PCB on which the IC chip is mounted are both put on the charging plate of the field-induced CDM ESD tester to form the board-level CDM ESD test, as that shown in Fig. 7.19. The equivalent capacitance of the PCB in this board-level CDM ESD test setup is ~274 pF. The main difference between the board-level CDM and chip-level CDM ESD test is that the PCB is also charged in the board-level CDM ESD test. Since the equivalent capacitance of the PCB is significantly larger than that of the DUT, more charges are stored and discharged in board-level CDM ESD tests. Therefore, it is expected that the board-level CDM ESD test is more critical than the traditional chip-level CDM ESD test. The measured results on the chip-level and board-level CDM ESD levels with the different test components are compared. In addition, failure analysis is performed to characterize the failure mechanism.

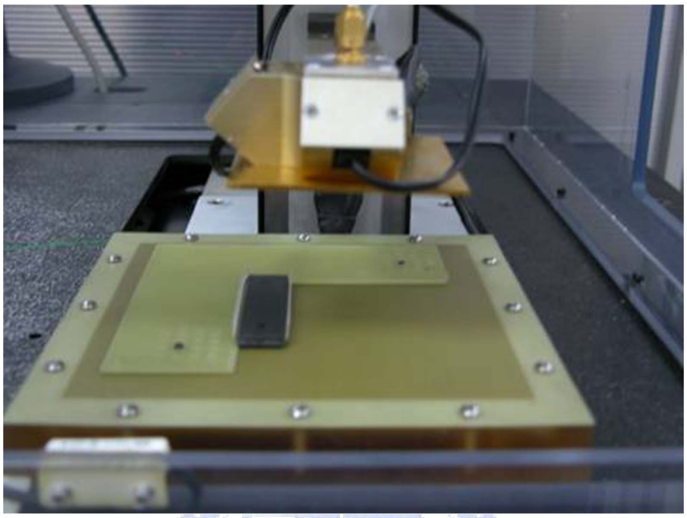


Fig. 7.18. Field-induced chip-level CDM ESD measurement setup.

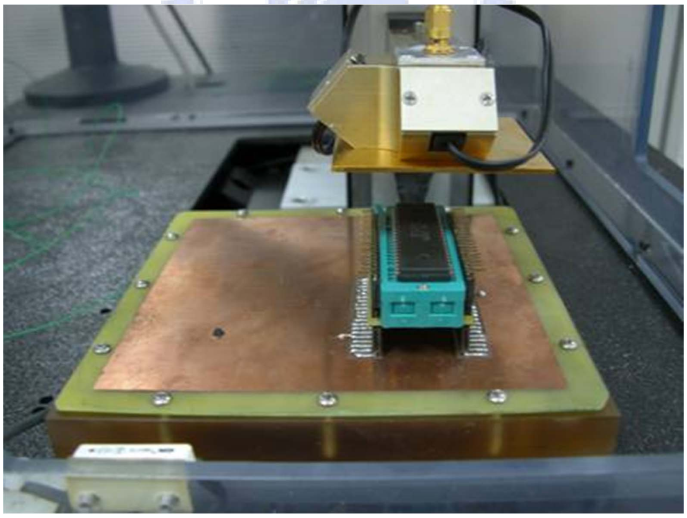
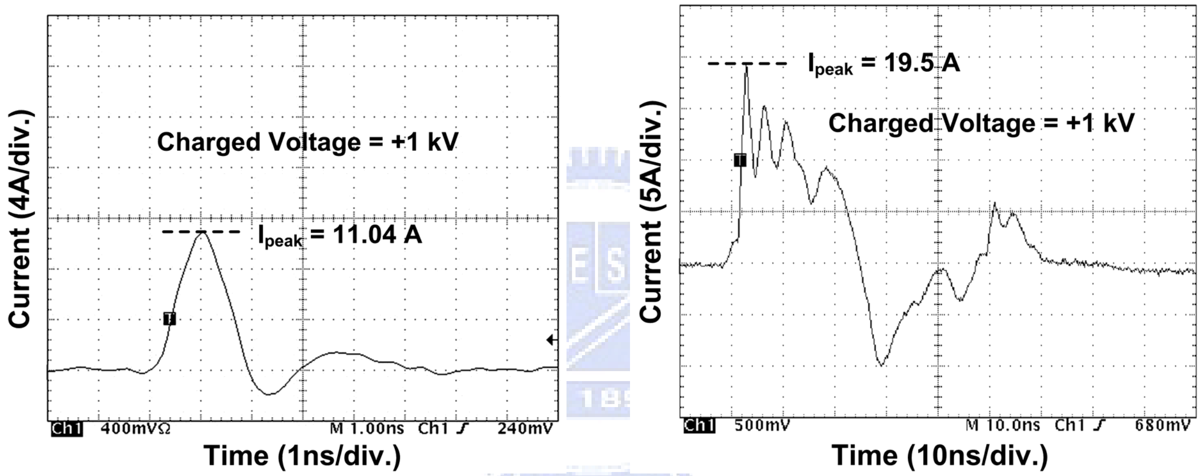


Fig. 7.19. Field-induced board-level CDM ESD measurement setup.

7.4.1. Test With Gate-Grounded NMOS

A gate-grounded NMOS (GGNMOS) fabricated in a 0.18-μm CMOS process was used as the DUT for the chip-level and board-level CDM ESD tests. The equivalent capacitance between the drain terminal and substrate of the GGNMOS in 40-pin DIP package is ~6.2 pF.

In the chip-level and board-level CDM ESD tests, the drain terminal of the GGNMOS is tested. Fig. 7.20(a) and (b) show the measured current waveforms under chip-level and board-level CDM ESD tests with the charged voltage of 1 kV, respectively. The peak currents under chip-level and board-level CDM ESD tests are 11.04 A and 19.5 A, respectively. Under the same charged voltage, the discharging current in the board-level CDM ESD test is significantly higher that in the chip-level CDM ESD test. Although the rise time of the board-level CDM ESD event is slower than that of the chip-level CDM ESD event, such a huge discharging current with a fast rise time during board-level CDM ESD events can easily damage the GGNMOS. Besides, the duration of the board-level CDM ESD event is longer than that of the chip-level CDM ESD event.



(a) (b)

Fig. 7.20. Measured current waveforms with gate-grounded NMOS (GGNMOS) under (a) +1-kV chip-level CDM ESD test, and (b) +1-kV board-level CDM ESD test.

7.4.2. Test With Dummy Receiver NMOS

In this section, the dummy receiver NMOS (RX_NMOS) with the on-chip ESD protection circuit fabricated in a 130-nm CMOS process was used as the test circuit. As shown in Fig. 7.21, the gate terminal of the RX_NMOS is connected to the input pad to emulate the connection of a typical input NMOS in a receiver. The drain, source, and bulk terminals of the RX_NMOS are connected to VSS. The On-chip ESD protection circuit is applied to the RX_NMOS. The typical double-diode ESD protection scheme is used at the input pad. The power-rail ESD clamp circuit consists of an RC timer, an inverter, and an ESD clamp NMOS. This RX_NMOS shown in Fig. 7.21 is the same that shown in Fig. 6.9 except that the ESD clamp device in the power-rail ESD clamp circuit is a 400-μm wide NMOS transistor in Fig. 7.21. The equivalent capacitance between the input pad and substrate of the RX_NMOS in 40-pin DIP package is ~6.8 pF. By performing board-level CDM ESD tests on input pad of the RX_NMOS, the board-level CDM ESD level of the typical receiver circuit can be evaluated. The peak currents and measured results of chip-level and board-level CDM ESD tests on the RX_NMOS with the on-chip ESD protection circuit are listed in Table 7.1. The RX_NMOS passes 200-V chip-level CDM ESD test, but fails at 200-V board-level CDM ESD test. This demonstrates that the board-level CDM ESD robustness is lower than the chip-level CDM ESD robustness, because the board-level CDM ESD event has larger discharging current than that in the chip-level CDM ESD event. For example, the peak current is 2.99 A in 200-V chip-level CDM ESD test, whereas the peak current in 200-V board-level CDM ESD test is 4.03 A.

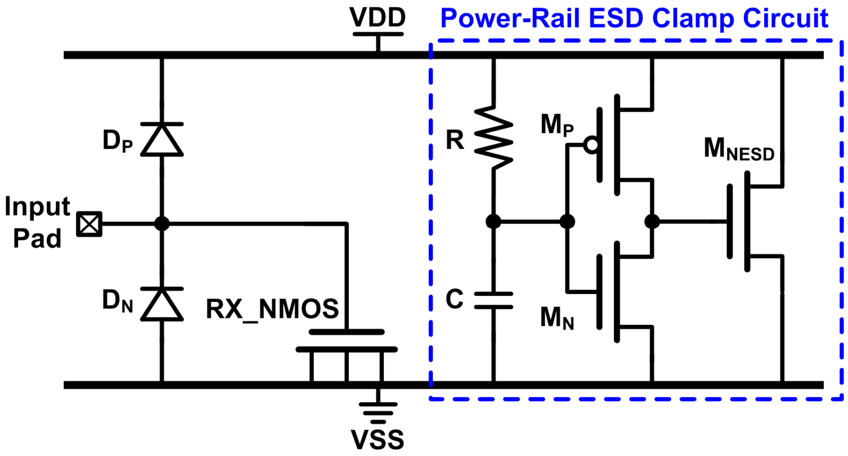


Fig. 7.21. Test circuit with dummy receiver NMOS (RX_NMOS) for chip-level and board-level CDM ESD tests.

Table 7.1

Measured Results on Chip-Level CDM and Board-Level CDM ESD Robustness of Dummy Receiver NMOS (RX_NMOS)

	Charged Voltage	Chip-Level CDM	Board-Level CDM
Peak Current	+100 V	N/A	1.72 A (Pass)
	+150 V	N/A	2.71 A (Pass)
	+200 V	2.99 A (Pass)	4.03 A (Fail)
	+400 V	8.43 A (Fail)	N/A

7.4.3. Test With 2.5-Gb/s High-Speed Receiver Interface Circuit

In this section, the 2.5-Gb/s differential high-speed receiver interface circuit, which is presented in section 6.4.1 and shown in Fig. 6.11, was verified with the chip-level and board-level CDM ESD tests. The high-speed receiver interface circuit was fabricated in a 130-nm CMOS process. Because of high-speed application, the dimensions of the ESD diodes at the I/O pads are limited to reduce the parasitic capacitance at the input pads. The equivalent capacitance between the Vin1 pad and substrate of the ESD-protected 2.5-GHz differential high-speed receiver interface circuit in 40-pin DIP package is ~5.4 pF. Besides, a reference high-speed receiver interface circuit without on-chip ESD protection circuit was also fabricated in the same process to compare the ESD robustness. The tested pin is the Vin_1 pad. The measured chip-level and board-level CDM ESD levels of the 2.5-Gb/s high-speed receiver circuits with and without on-chip ESD protection circuits are listed in Table 7.2 and 7.3, respectively. The chip-level and board-level CDM ESD levels of the reference high-speed receiver interface circuit are quite poor, which fail at ±100 V and ±50 V, respectively. With the on-chip ESD protection circuits, the failure voltages during chip-level and board-level CDM ESD tests are greatly improved to -1300 V and -900 V, respectively. Similarly, the board-level CDM ESD level is lower than the chip-level CDM ESD level. Failure analysis has been performed for the ESD-protected high-speed receiver interface circuits after -1300-V chip-level CDM ESD test and -900-V board-level CDM ESD test. The SEM failure pictures after chip-level CDM and board-level CDM ESD tests are shown in Fig. 7.22(a) and (b), respectively. The failure points are both located at the P+/N-well diode D_{P1} at the input pad. Although the ESD protection devices are successfully turned on during CDM ESD tests, huge current still damages the ESD protection devices. According to the SEM failure pictures, the failure is much worse after board-level CDM ESD test than that after chip-level CDM ESD test. This again demonstrates that board-level CDM ESD events are more critical than chip-level CDM ESD events.

7.5. Summary

In this chapter, the board-level CDM ESD issue is comprehensively addressed. The causes of both chip-level and board-level CDM ESD events are introduced first. Then, the discharging current waveforms during board-level CDM ESD events under different PCB sizes, different charged voltages, and different series resistances are investigated. Finally, the board-level CDM ESD test is performed to several test devices and test circuits fabricated in 0.18-μm and 130-nm CMOS processes. The measured results have shown that the board-level CDM ESD events are more critical than the chip-level CDM ESD events. Several

Table 7.2

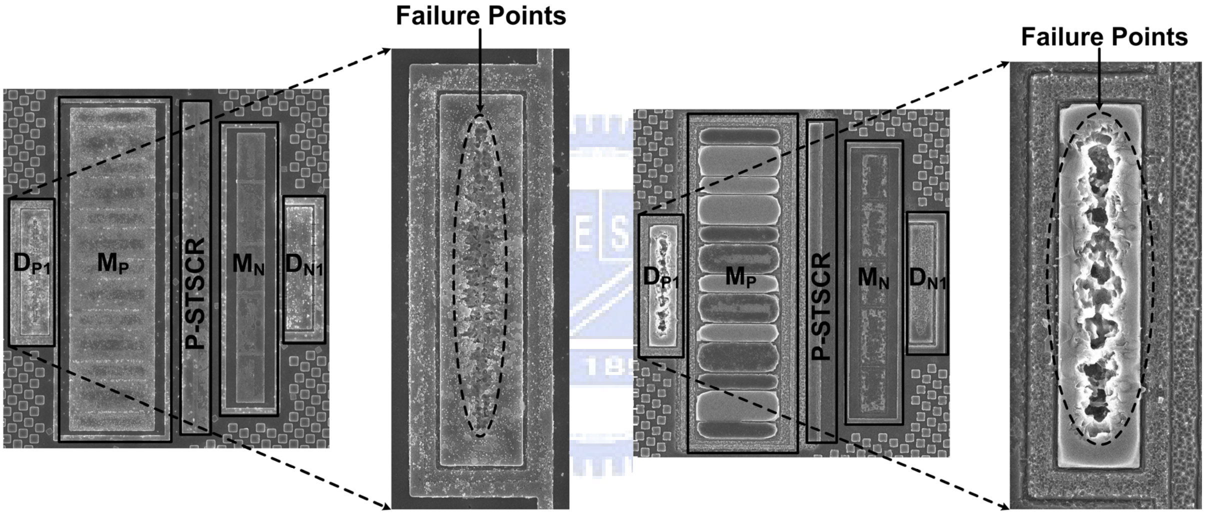
Measured Chip-Level CDM ESD Robustness of 2.5-Gb/s High-Speed Receiver Interface Circuit

	Without ESD Protection		With ESD Protection	
Polarity	**+**	**-**	**+**	**-**
Failure Voltage	**100 V**	**100 V**	**2000 V**	**1300 V**

Table 7.3

Measured Board-Level CDM ESD Robustness of 2.5-Gb/s High-Speed receiver Interface Circuit

	Without ESD Protection		With ESD Protection	
Polarity	**+**	**-**	**+**	**-**
Failure Voltage	**50 V**	**50 V**	**1300 V**	**900 V**



(a) (b)

Fig. 7.22. Scanning-electron-microscope (SEM) pictures of the failure points on the 2.5-Gb/s high-speed receiver interface circuit after (a) -1300-V chip-level CDM ESD test, and (b) -900-V board-level CDM ESD test.

designs had been reported for chip-level CDM ESD protection [147]–[153]. However, no design against board-level CDM ESD events is reported so far. In general, the board-level CDM ESD event is more critical in the I/O pins than in the power pins, because there are decoupling capacitors between the power pins and the ground plane, which can be used to clamp the voltage and discharge the ESD energy by the displacement current. In nanoscale CMOS processes, the gate oxide of MOS transistor becomes thinner, which degrades the CDM ESD robustness of CMOS ICs. In high-speed or radio-frequency (RF) applications, large ESD protection devices can not be applied to the I/O pad due to the limitation on parasitic capacitance, which further increases the difficulty of CDM ESD protection design. Moreover, the die size becomes larger in SoC applications, so more charges will be stored in the body of the chip. Consequently, CDM ESD issues, including chip-level and board-level CDM ESD events, will become more critical and should be taken into consideration in the ICs and microelectronic systems which are realized in nanoscale CMOS processes. In the board-level ESD protection design, applying the transient voltage suppressor (TVS) is a promising solution because the TVS can provide excellent ESD protection capability with small capacitive loading effect.

Chapter 8

Conclusions and Future Works

This chapter summarizes the main results and contributions of this dissertation. Suggestions for future research topics in the fields of on-chip ESD protection design for RF front-end circuits and high-speed I/O interface circuits are also provided in this chapter.

8.1. Main Results of This Dissertation

With the evaluation of CMOS technology, high-frequency characteristics of CMOS devices become better, which make CMOS processes suitable for implementing RF front-end circuits and high-speed I/O interface circuits operating in gigahertz frequency bands. To achieve good high-frequency performance, parasitic loading effects on the signal path must be minimized. Thus, the bond-pad capacitance needs to be minimized. In this dissertation, a novel ultra low-capacitance bond pad structure has been proposed and verified. Besides bond-pad capacitance, the parasitic capacitances of ESD protection devices at the I/O pads also need to be minimized while keeping satisfactory ESD robustness. Unfortunately, ESD is not scaled with CMOS technology, which makes nanoscale CMOS devices very vulnerable to ESD. Especially, the gate oxides of MOS transistors are easily to be damaged by ESD when the gate terminal is connected the input pad. Designing the ESD protection scheme with slight high-frequency circuit performance degradation and high ESD robustness becomes a tough task. In this dissertation, several novel on-chip ESD protection schemes for narrow band and wideband RF front-end circuits have been proposed and verified. With the proposed ESD protection schemes, good RF performance and high ESD robustness can be achieved simultaneously. Moreover, ESD protection design for high-speed I/O interface circuits has also been presented in this dissertation.

After finishing the ESD protection design for a single chip, board-level CDM ESD issues for microelectronic systems with multiple IC chips poses another design consideration. In the last part of this dissertation, the impacts caused by board-level CDM ESD events on IC products have been comprehensively investigated with experimental results. The contributions of each chapter in this dissertation are presented in the following.

Chapter 2 overviews the published ESD protection designs for high-frequency applications, including RF front-end circuits and high-speed I/O interface circuits. The designs are categorized with their individual advantages and disadvantages clearly analyzed. The published low-capacitance ESD protection designs are categorized into three groups, which are the circuit solution, layout solution, and process solution. Among the three groups, circuit solution is the most popular, because it can without modifying the manufacturing process. Finally, the design complexity, improved parasitic effect, ESD robustness, and area efficiency of all reported designs are compared in this chapter.

In Chapter 3, a new ultra low-capacitance bond pad structure is proposed and verified in a 130-nm CMOS process. The equivalent bond-pad capacitance has been verified to be reduced due to the parallel LC resonant network formed by the embedded inductor and the overlapped capacitance between the bond-pad metal plate and substrate. Three kinds of stacked inductors under the pad are used to realize different inductances in the parallel LC resonant network. By designing the inductance and capacitance in the proposed bond pad structure, the frequency band in which the bond-pad capacitance is reduced can be adjusted. Experimental results have shown that the extracted bond-pad capacitance is successfully reduced to almost 0 fF from 4.3 to 4.8 GHz. The new proposed bond pad structure is fully process-compatible to general CMOS processes without any extra process modification.

In Chapter 4, two distributed ESD protection schemes are proposed to protect the wideband distributed amplifier. Fabricated in a 0.25-μm CMOS process, the distributed amplifier with the equal-sized distributed ESD (ES-DESD) protection scheme, contributing an extra 300 fF parasitic capacitance at the signal path, sustains 5.5-kV HBM ESD level and 325-V MM ESD level, while exhibits the power gain of 4.7 ± 1 dB from1 to 10 GHz. With the same total parasitic capacitance, the distributed amplifier with the proposed decreasing-sized distributed ESD (DS-DESD) protection scheme achieves better ESD robustness, where the HBM ESD level is over 8 kV and the MM ESD level is 575 V. The power gain of 4.9 ± 1.1 dB over the 1 to 9.2-GHz band is achieved. With these two proposed distributed ESD protection schemes, good wideband RF performances and high ESD robustness of the distributed amplifier can be successfully achieved simultaneously.

In Chapter 5, several new RF ESD protection schemes for differential input stages are proposed and applied to a 5-GHz differential LNA in a 130-nm CMOS process. This is the first work which investigates the pin-to-pin ESD robustness of differential LNAs. The differential LNA with the conventional double-diode ESD protection scheme has also been designed and fabricated, and it has 2.5-kV HBM and 200-V ESD robustness. Experimental results have demonstrated that the pin-to-pin ESD test is the most critical ESD test mode for the differential LNA with the conventional ESD protection scheme. With the proposed double silicon-controlled rectifier (SCR) ESD protection scheme, the HBM and MM ESD levels are significantly improved to 6.5 kV and 500 V, respectively. Another proposed design with an ESD bus between the differential input pads achieves 3-kV HBM and 100-V ESD robustness. Besides, a novel design using cross-coupled SCR devices between the differential input pads has been proposed. By applying the cross-coupled SCR devices, not only ESD protection for a single input pad but also pin-to-pin ESD protection are achieved without adding any extra devices. Its HBM and MM ESD levels are 1.5 kV and 150 V, respectively. By using other diodes beside the cross-coupled SCR devices, the turn-on efficiency of ESD protection devices can be enhanced. With the double diodes and the cross-coupled SCR devices, the ESD-protected differential LNA achieves 4-kV HBM and 300-V MM ESD robustness. Both ESD robustness and RF performance of all fabricated LNAs with and without ESD protection have been measured and compared and in this chapter.

Chapter 6 presents the ESD protection design for high-speed I/O interface circuits. The ESD levels and parasitic capacitances of P+/N-well and N+/P-well ESD protection diodes with different dimensions are characterized in the beginning. Then the ESD protection diodes with appropriate dimensions are applied to the dummy receiver NMOS and the dummy transmitter NMOS. Since the connection of the dummy receiver NMOS (dummy transmitter NMOS) is similar to that of the NMOS transistor in a receiver (transmitter) interface circuit, the ESD robustness of the dummy receiver NMOS (dummy transmitter NMOS) can be used to predict the ESD robustness of the high-speed interface circuit with this ESD protection scheme. This whole-chip ESD protection scheme is also applied to a 2.5-Gb/s high-speed I/O interface circuit, and the ESD robustness is larger than 3 kV in HBM with the parasitic capacitance of less than 250 fF. By replacing the N+/P-well diode between the input pad and VSS with the SCR, the ESD robustness can be further improved. In the ESD protection schemes in Chapter 6, the ESD protection devices and part of the ESD detection circuit is placed under the I/O pad to reduce the chip area and the parasitic capacitance on the signal path.

The board-level CDM ESD issues in IC products are investigated in Chapter 7. The mechanism of board-level CDM ESD event is introduced first. Based on this mechanism, an experiment has been performed to investigate the board-level CDM ESD current waveforms under different sizes of PCBs, different charged voltages, and different series resistances in the discharging path. Experimental results have shown that the discharging current strongly depends on the PCB size, charged voltage, and series resistance. Moreover, chip-level and board-level CDM ESD levels of several test devices and test circuits fabricated in CMOS processes have been characterized and compared. Test results have shown that the board-level CDM ESD level of the test circuit is lower than the chip-level CDM ESD level, which indicates that the board-level CDM ESD event is more critical than the chip-level CDM ESD event. In addition, failure analysis reveals that the failure on the test circuit under board-level CDM ESD test is much severer than that under chip-level CDM ESD test. To provide board-level CDM ESD protection, the solution using the ESD discharger has been proposed. The ESD discharger, which consists of series resistances in the order of MΩ, can be used to slowly discharge the static charges in the module and to prevent the IC chips from being damaged by board-level CDM ESD events. Since the standard for the board-level CDM ESD test is not established so far, a draft of the test standard for board-level CDM ESD robustness of ICs is proposed in the appendix. In the proposed test standard, the test methodology and test conditions are clearly defined.

8.2. Future Works

Recently, the operating frequencies of RF front-end circuits are elevated to V band (50–75 GHz). Definitely, ESD protection is also needed for those RF front-end circuits. However, the limitation of parasitic capacitance from ESD protection devices becomes much stricter for circuits operating in such high frequency bands because the impedance of capacitive elements becomes lower as the frequency increased. Shunt ESD protection devices with lower impedance losses more signal under normal circuit operating conditions. As mentioned in Chapter 2, utilizing extra components to compensate the parasitic capacitance of ESD protection device is a feasible method. To achieve successful ESD protection design for V-band RF front-end circuits, precise modeling of ESD protection devices is necessary. Hence, modeling of ESD protection devices in higher frequency bands is need in the future.

Inductors are often used to compensate the parasitic capacitance of ESD protection devices. With the evolution of CMOS technology, the fabrication cost per unit chip area becomes more expensive. Reducing the number of inductors in the chip will be beneficial. Thus, developing active circuit blocks which can generate inductive impedance is promising in the future.

Designing ESD protection circuits for each individual circuit is demanding. It would be helpful if the ESD cells with different specifications are available in the foundry design kit. Establishing the ESD cells in nanoscale CMOS processes is highly necessary in the future. With the ESD cells, IC designers can take the parasitic effects of the ESD protection devices into consideration with the awareness of ESD robustness during the circuit design phase. Consequently, the time to market for the IC products can be reduced.

Appendix

Proposal of "Test Standard for Board-Level Charged-Device-Model Electrostatic Discharge Robustness of Integrated Circuits"

「積體電路之電路板層級元件充電模式靜電放電測試標準」提案

1. 適用範圍

本標準規定評估積體電路產品之電路板層級(Board-Level)元件充電模式(Charged-Device Model, CDM)靜電放電(Electrostatic Discharge, ESD)耐受度測試方法，並描述其測試評估程序。

本標準應用於所有已封裝之積體電路晶片，不論其積體電路製程與封裝型式為何。

2. 名詞釋義

下列各項定義應用於本標準。

2.1 靜電放電(ESD)：在不同靜電電位之物體間，靜電場以接觸或感應方式而產生之靜電荷之傳送。

2.2 元件充電模式靜電放電(CDM ESD)：積體電路先因磨擦或其他因素而在積體電路內部累積了靜電，但在靜電累積的過程中由於沒有放電路徑，故積體電路並未被損傷。此帶有靜電的積體電路在處理過程中，當有某一接腳碰觸到接地面時，儲存於積體電路內部的靜電荷便會自積體電路內部經由接地的接腳流出，造成元件充電模式靜電放電現象。

2.3 接地面：是一金屬片或金屬板，作為待測晶片與所有測試時所需之儀器設備的共同接地參考點。

3. 測試設備

此測試設備適用於本測試程序之所有部分，以下列出量測時所需要之儀器設備。

3.1 電源供應器：此電源供應器需有將載有待測晶片之電路板完全充電至 2000 V 之功能，以提供測試時的充電電源。

3.2 電阻：用來連接電源供應器輸出端與電路板。此電阻之電阻值為 10 MΩ，串聯大電阻的目的在於避免電源供應器對電路板充電之電流影響到量測之放電電流值。

3.3 電路板：需為雙層電路板，電路板之上下兩面之表面為導電之金屬(例如：銅、黃銅或鍍鋅鋼)，上下兩面中間為絕緣材料構成之介電層。電路板大小為 300 mm × 200 mm，電路板上下兩金屬表面間之寄生電容值在 1 MHz 時為 800 pF。

3.4 電容計：用以驗證電路板之寄生電容值。電容計需有小於 1 pF 之量測解析度，小於 3%之量測誤差，至少 1 MHz 之量測頻率。

3.5 晶片插座(Socket)：晶片插座需配合晶片封裝型式，不同封裝型式之晶片需搭配不同晶片插座進行測試。將晶片插座置於電路板上板，並把測試時要充電的接腳插座焊接至電路板之上板，保持其餘測試時不要充電的接腳插座浮接。針對測試時不同的充電接腳組合，需有不同的晶片插座與電路板之焊接方式。

3.6 電壓計：用來驗證測試時電路板的充電電壓是否達到預計之測試電壓。

3.7 絕緣物：應由乾燥的絕緣材料構成，此絕緣物的厚度應為 5 mm ± 1 mm，並超出接地面所有邊緣至少 50 mm。

3.8 接地面：一個具電傳導性的金屬片(例如：銅、黃銅或鍍鋅鋼板)，厚度至少為 1 mm，面積至少為 0.5 m^2 的區域，並確實超出電路板所有邊緣至少 100 mm。接地面需藉著長度小於 1 m，直徑至少為 1 mm 的接地金屬線連接至所有儀器設備的接地點。接地金屬線的電感必須小於 5 μH。

3.9 示波器：量測並顯示放電電流之量測裝置。示波器需擁有 50 Ω 之輸入阻抗，最小 500 MHz 以上的頻寬，最小 5 GS/s 以上的取樣率。

3.10 電流探棒：感測放電電流之裝置。電流探棒需要 500 MHz 以上之頻寬，並以 50 Ω 之阻抗連接示波器。

3.11 具有 50 Ω 阻抗的 20 dB 衰減器：若量測時產生之放電電流，經過電流探棒轉換為電壓後，大於示波器之量測範圍，可將此衰減器連接於電流探棒與示波器的輸入端之間，以衰減進入示波器之電壓訊號。衰減器需要 500 MHz 以上之頻寬。

4. 積體電路晶片之電路板層級元件充電模式靜電放電測試程序

4.1 在執行任何測試之前，先確認所有儀器設備之功能正常。

4.2 測試期間需維持周圍溫度在攝氏 23 ± 5 度和相對濕度 30%到 60%之間，其他的數值應經模組廠同意，且應應記錄於測試報告中。

4.3 測試的配置依照圖 1 所示。

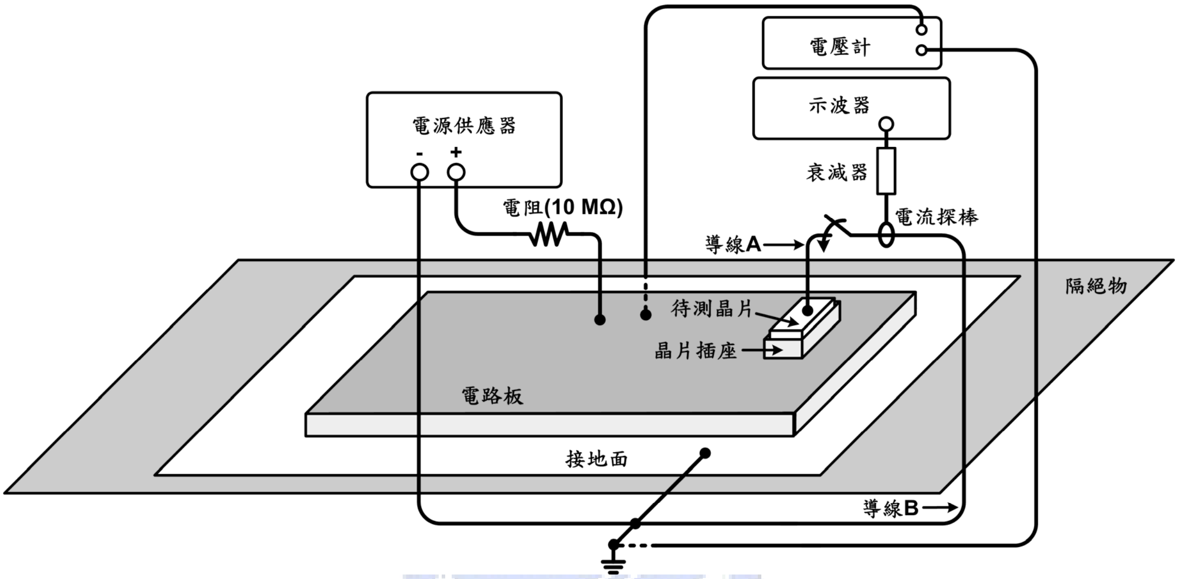


圖 1. 積體電路晶片之電路板層級元件充電模式靜電放電測試配置

4.4 以 3.8 節規定的接地金屬線，直接連接電源供應器、示波器、電壓計的接地端到接地面。

4.5 將待測晶片置於焊接在電路板上的晶片插座中，並將電路板置於接地面的中心位置，接地面置於隔絕物之中心位置。電路板下板碰觸接地面，使電路板下板接地。電源供應器的電壓輸出端透過一個 10 MΩ 的電阻接至電路板之上板，電源供應器透過該 10 MΩ 電阻對電路板上板充電。自待測晶片之放電接腳插座接出一條金屬導線(導線 A)，接地面接出另一條金屬導線(導線 B)(如圖 1 所示)。

4.6 調整電源供應器之輸出電壓，將電路板充電至測試電壓值。充電完成後使用電壓計量測電路板上板之電壓，確認電路板上板的確已充至測試電壓值，確認充電電壓值後，將電壓計的探針移離開電路板上板。

4.7 電路板上板充電完成後，將導線 A 與導線 B 短路，將已充電之電路板與待測晶片透過放電接腳放電。每個測試電壓值需進行至少三次測試，每次測試之時間間隔需大於 10 秒。每次放電均可透過電流探棒與示波器觀測放電電流波形。每個

測試電壓連續測試三次後，需驗證待測晶片是否已損壞。

4.8 起始測試電壓應為 100 V，之後每次遞增 100 V，建議最高測試電壓為 2000 V。測試時正負極性之測試電壓均需包括於測試範圍內。

4.9 測試接腳組合：待測晶片需進行以下所有充電接腳與放電接腳組合的測試。

4.9.1 對單一電源(VDD)與接地(VSS)接腳的晶片，測試接腳組合如下：

4.9.1.1 對 VSS 接腳充電，自 VDD 接腳放電。

4.9.1.2 對 VDD 接腳充電，自 VSS 接腳放電。

4.9.1.3 對一個輸入輸出(I/O)接腳充電，自另一 I/O 接腳放電，其他所有 I/O 接腳與所有 VDD、VSS 接腳皆浮接。所有 I/O 接腳均需經過充電接腳與放電接腳的測試。

4.9.2 對多重電源(VDD1、VDD2 等等)與接地(VSS1、VSS2 等等)接腳的晶片，測試接腳組合如下：

4.9.1.1 對 VSS1 接腳充電，自 VDD1 接腳放電。

4.9.1.2 對 VSS1 接腳充電，自 VDD2 接腳放電。

4.9.1.3 三組電源以上之晶片，任一 VSS 接腳均需擔任充電接腳，並搭配任一 VDD 接腳擔任放電接腳測試。

4.9.1.4 對 VDD1 接腳充電，自 VSS1 接腳放電。

4.9.1.5 對 VDD1 接腳充電，自 VSS2 接腳放電。

4.9.1.6 三組電源以上之晶片，任一 VDD 接腳均需擔任充電接腳，並搭配任一 VSS 接腳擔任放電接腳測試。

4.9.1.7 對一個輸入輸出(I/O)接腳充電，自另一 I/O 接腳放電，其他所有 I/O 接腳與所有 VDD、VSS 接腳皆浮接。所有 I/O 接腳均需經過充電接腳與放電接腳的測試。

5. 判讀電路板層級元件充電模式靜電放電耐受度標準

5.1 依照 4.7、4.8、4.9 節規範進行測試後，待測晶片所有測試腳位組合均能通過的最高測試電壓(測試後待測晶片仍未損壞)，為該待測晶片的電路板層級元件充電模式靜電放電耐受度。

5.2 測試後待測晶片是否損壞，可依下三種方式之一判斷：

5.2.1 經過測試後的放電接腳，在待測晶片正常偏壓下，若漏電大於 1μA，則判定

該待測晶片已經損壞。

5.2.2 經過測試後的放電接腳，進行直流掃瞄(DC Sweep)，將得到的電流-電壓曲線與測試前待測晶片該接腳的直流掃瞄之電流-電壓曲線比較，若經過測試後該放電接腳的電流-電壓曲線偏移超過 30%，則判定該待測晶片已經損壞。

5.2.3 對經過測試後的放電接腳進行功能測試，若測試後晶片功能失效，則判定該待測晶片已損壞。功能失效之認定需經模組廠同意。

5.3 電路板層級元件充電模式靜電放電耐受度等級分類如表 1 所示：

表 1. 積體電路之電路板層級元件充電模式靜電放電耐受度等級分類表

等級	耐受度
Level 1	**200 V以下**
Level 2	**200 V至500 V**
Level 3	**500 V至1000 V**
Level 4	**1000 V以上**
Level 5	**客戶定義**

6. 靜電放電電流波形特徵

6.1 每次進行測試前，需以不含晶片插座之電路板直接對接地面放電，以驗證靜電放電電流波形是否正確。

6.2 以 100 V 之測試電壓進行靜電放電電流波形驗證，正確之電流波形如圖 2 所示，電流波形之各項參數需符合表 2 所列之規格。

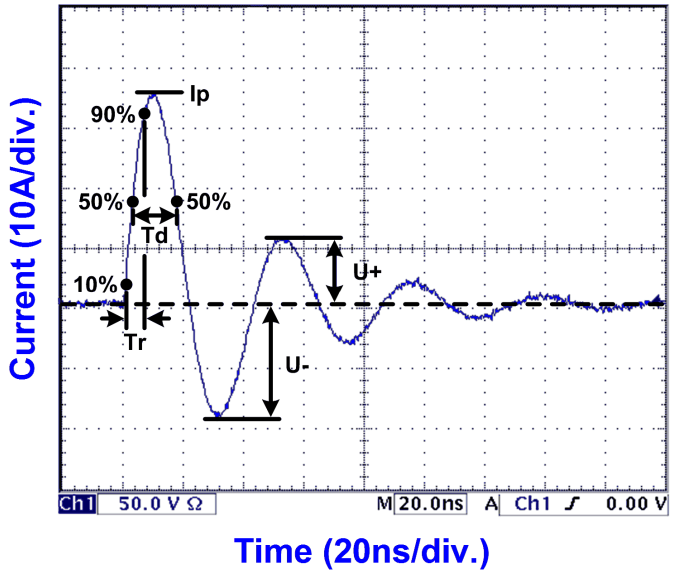


圖 2. 以 100 V 測試電壓，將不含晶片插座之電路板直接對接地面放電的電流波形

表 2. 電流波形之各項參數

測試電壓	100 V (± 5%)
電流峰值 (Ip)	36 A (± 15%)
上升時間 (Tr)	<8 ns
超過一半峰值電流的時間 (Td)	8 ns (± 2ns)
最大下衝(Undershoot)電流 (U-)	<50% Ip
最大過衝(Overshoot)電流 (U+)	<30% Ip

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On-Chip ESD Protection Designs for Radio-Frequency Integrated Circuits and High-Speed I/O Interface Circuits

Publication List

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