國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

高介電係數介電質與金屬閘極製程技術之研究與應用

The Investigation and Application of High-κ Dielectrics and Metal Gate Process Technologies

研 究 生 ：洪彬舫

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中華民國九十五年十二月

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研 究 生：洪彬舫　　Student: Bing-Fang Hung

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摘要

隨著互補式金氧半電晶體(CMOS)元件尺寸持續微縮，傳統的絕緣層-二氧化矽(SiO_2)將遭遇漏電流過大的物理限制。另外，傳統的多晶矽閘極也將遭遇諸多挑戰-多晶矽空乏、硼穿透及高電阻係數。因此，新的絕緣層及閘極材料將是往後幾年超大型積體電路(VLSI)發展極需解決的問題。近年來，高介電係數介電層與金屬閘極的技術發展，已成為半導體產業最重要的研究之一。在本論文中，吾人將探討數種高介電係數介電層與金屬閘極的研究與應用。

首先，我們將探討高介電係數氮氧化矽鉿(HfSiON)介電層，分別選用矽化鉿($HfSi_x$)與矽化銥(Ir_xSi)所形成的全金屬矽化閘極(FUSI)來當 n-型與 p-型金氧半場效電晶體的閘極。而氮氧化矽鉿雖然比氧化鉿有較低的介電係數，但卻有較佳的熱穩定性。另外，使用矽化鉿與矽化銥全金屬矽化閘極比純金屬閘極有更好的熱穩定性，且可有效降低費米栓(Fermi-level pinning)效應所造成的有效功函數偏移

現象。結果顯示，結合氧化矽鉿與矽化鉿與矽化鉍全金屬矽化閘極，是實現雙金屬閘極互補式金氧半電晶體很好的選擇之一。

其次，我們將探討另一種高介電係數介電層氮氧化鑭鉿(HfLaON)，結合金屬氮化物閘極氮化鉭(TaN)應用於 n-型金氧半場效電晶體。氮氧化鑭鉿與氮氧化矽鉿同樣具有良好的高溫熱穩定性，但氮氧化鑭鉿卻有比氮氧化矽鉿還要高的介電係數的優點。此外，氮化鉭閘極具有良好的高溫熱穩定性，且結合氮氧化鑭鉿介電層後，其有效功函數將可調變到適用於 n-型金氧半場效電晶體的應用。

最後，我們將高介電係數氧化鑭鋁($LaAlO_3$)應用於低溫複晶矽薄膜電晶體(Low Temperature poly-Si TFTs)並結合低功函數鐿(Yb)金屬閘極，可以有效降低有效氧化層厚度(EOT)來達成提升電流密度及降低臨界電壓，進而得到大的驅動電流元件特性。此良好的元件特性並無經過氫化及特殊再結晶製程，且將可應用於未來的面板系統(SOP)上。

The Investigation and Application of High-κ Dielectrics and Metal Gate Process Technologies

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Abstract

To continue down-scaling CMOS technology, traditional insulator layer - SiO_2 will face the physical limitation - large gate leakage current. In addition, traditional poly-Si gate encounters several inherent limitations, such as poly-Si depletion, boron penetration, and high resistivity. Therefore, new insulator and gate material technologies will become urgent for very large scale integration (VLSI) technology in the future years. Recently, metal-gate/high-κ process technologies become one of the most important researches in the semiconductor industry. In this dissertation, we will investigate the application of several high-κ dielectric and metal gate process technologies.

First of all, we will study the application of HfSiON dielectric with $HfSi_x$ and Ir_xSi full silicidation (FUSI) metal gates in n-MOSFETs and p-MOSFETs, respectively. Although HfSiON has smaller dielectric constant than HfO_2, it has better

thermal stability. Besides, using $HfSi_x$ and Ir_xSi FUSI metal gates can obtain better thermal stability than using pure metal gates, and also can reduce the effective work function shifts due to Fermi-level pinning effect. These results indicate that integrating HfSiON with $HfSi_x$ and Ir_xSi FUSI metal gates can achieve dual metal gates development in CMOS technology.

Next, we will study another high-κ dielectric HfLaON with metal nitride TaN gate in n-MOS application. HfLaON has good thermal stability as HfSiON, but it has the advantage of higher κ value. Moreover, TaN also has similarly good thermal stability. Integrating HfLaON with TaN gate will provide the appropriate effective work function in n-MOS application.

Finally, the application of high-κ $LaAlO_3$ dielectric into low-temperature poly-Si thin-film transistors (TFTs) combining with low work function Yb metal gates was investigated. Good TFT performance was achieved - such as a high drive current and low threshold voltage due to the down-scaling effective oxide thickness (EOT) provided by the high-κ dielectric. In addition, the good performance was achieved without hydrogen passivation or special crystallization steps. These results suggest that the Yb/$LaAlO_3$ TFTs can meet the device requirements for system-on-panel (SOP) applications.

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Contents

Table Captions

Chapter 5 Poly-Silicon Thin Film Transistors Using Ytterbium Metal Gate and $LaAlO_3$ Dielectric

Figure Captions

Chapter 1 Introduction

Chapter 2 High temperature stable Ir_xSi Gates with High Work Function on HfSiON p-MOSFETs

Chapter 3 HfSiON n-MOSFETs Using Low Work Function $HfSi_x$ Gates

Chapter 4 Novel High-κ HfLaON n-MOSFETs with Preserved Amorphous State to 1000°C

Chapter 1

Introduction

1.1 Overview of high-κ gate dielectrics

The gate leakage current through the gate oxide increases significantly because direct tunneling is the primary conduction mechanism in down-scaling CMOS technologies. To reduce the leakage current related higher power consumption in highly integrated circuit and overcome the physical thickness limitation of silicon dioxide, the conventional SiO_2 will be replaced with high dielectric constant (high-κ) materials as the gate dielectrics beyond the 65 nm technology mode [1]-[6]. Therefore, the engineering of high-κ gate dielectrics have attracted great attention and played an important role in VLSI technology. Although high-κ materials often exhibit smaller bandgap and higher defect density than conventional silicon dioxide, using the high-κ gate dielectric can increase efficiently the physical thickness in the same effective oxide thickness (EOT) that shows lower leakage characteristics than silicon dioxide by several orders without the reduction of capacitance density [2]-[5]. According to the ITRS (International Technology Roadmap for Semiconductor) [7], the suitable gate dielectrics must have κ value more than 8 for 50-70 nm technology nodes and that must be more than 15 when the technology dimension less than 50 nm. Fig. 1-1

shows the evolution of CMOS technology requirements.

Research on finding an appropriate substitute to the superior SiO_2 has been going on for almost a decade. Oxy-nitrides (SiO_xN_y) have been introduced to extend the use of SiO_2 in production but eventually it has to be replaced by a high-κ material, such as Ta_2O_5, TiO_2, HfO_2, ZrO_2, Al_2O_3, La_2O_3 or mixtures of them or metal-oxide-silicates of the mentioned compounds. However, most metal oxides will have the characteristics of crystallization at elevated temperature which cause devices generate non-uniform leakage distribution and give large statistical variation for nano-meter devices across the chip. Therefore, replacement gate strategies have been proposed to prevent crystallization and deleterious effects of mass and electrical transport along grain boundaries. Fig. 1-2 shows the summaries of the κ value and band offset for popular high-κ dielectric candidates.

1.2 Overview of metal gate electrodes

The gate electrode in CMOS devices is conventionally made of highly doped polycrystalline silicon (poly-Si). However, as the CMOS technology down-scaling, poly-Si gate will encounter several inherent limitations. One of them is depletion of the poly-Si electrode when the gate stack is biased in inversion [8]-[20]. The depleted region is added to the dielectric thickness, which results the increase of EOT and degradation of the transconductance. Increased resistance of the gate electrode fingers

is another issue due to the scaling geometry. Besides, diffusion of boron penetrates from the poly-Si gate will also degrade the performance of the transistors.

To overcome these problems, using metal gate electrodes will be a practical way to eliminate poly gate depletion and boron penetration [8]-[15]. In addition, metal gates also show the potential of reduced sheet resistance. However, metal-gate/high-κ CMOSFETs show undesired high threshold voltages (V_t), which is opposite to the VLSI scaling trend. This phenomenon is known as "Fermi-level pinning", although the background physics may be attributed to interface dipole and/or charged defects [8]. Moreover, thermal stability of the effective metal electrode and metal diffusion are also important considerations.

The work functions (Φ_m) of metal shown in Fig. 1-3 play an important role for metal-gate/high-κ CMOSFETs. The preferred work function of the metals are ~5.2 eV for p-MOSFETs and ~4.1 eV for n-MOSFETs. Recently, lots of metal or metal-nitride materials have been widely researched and successfully intergraded in advanced CMOSFETs, such as TiN, TaN, Pt, Mo and Ir [8]-[20]. However, it has been found that thermal annealing of the metal gates at temperatures above 900^{o}C results in mid-gap values for almost all metal gate candidates. Therefore, the Fermi-level pinning effect needs to be avoided by selecting suitable metal gate and high-κ materials for advanced CMOS technologies.

1.3 Innovation and Contribution

To compensate Fermi-level pinning effect, low and high work function metal electrodes are required to reduce the pinning effect for n- and p-MOSFETs, respectively. For p-MOSFETs, high work function metal electrodes larger than the 5.2 eV of p^+ poly-Si are needed. However, only Ir (5.27 eV) and Pt (5.65 eV) in the Periodic Table [21] can meet this requirement, which make the metal-gate/high-κ p-MOSFETs especially challenging [8]-[10]. Ir is more preferable than Pt due to a simpler etching process by reactive ion etching (RIE) [22]-[23]. Unfortunately, large metal diffusion through high-κ dielectrics was found in pure Ir gates after 1000^{o}C RTA which caused p-MOS device failures [24]-[25]. Another possibility is using low temperature full silicidation (FUSI) gates [9],[24]-[27]. However, the p-MOS devices incorporating high work function Pt_xSi or Ir_xSi still failed to integrate into the CMOS SALICIDE process due to the lack of required selective wet etching of Pt or Ir during SALICIDE. In this thesis, we have proposed and demonstrated a new high temperature stable Ir_xSi FUSI gate on high-κ HfSiON with a proper effective work function of 4.95 eV. HfSiON has good metal diffusion barrier property and the good compatibility with currently used SiON gate dielectric with added Hf for higher κ value.

For n-MOS application, we have used the similar method of Ir_xSi for p-MOS to

develop the low work function $HfSi_x$ gate for n-MOSFETs. This is because the Hf has very low work function of 3.5 eV in the Periodic Table. The $HfSi_x$ gate on HfSiON, formed by Hf deposition on thin amorphous Si, gives a low effective work function of 4.27 eV. In addition, the $HfSi_x$/HfSiON can sustain a high rapid thermal annealing (RTA) temperature of 1000◦C that is compatible with current VLSI process line. Since both process and mechanism of $HfSi_x$ and Ir_xSi, with respective low and high effective work function, are the same, these results indicate the high possibility to realize dual work function metal-gate/high-κ CMOS with large work function difference.

Besides, we also developed the novel HfLaON gate dielectric with simple TaN metal gate, good device integrity with a low effective work function of 4.24 eV has been obtained for n-MOSFETs. The preserved 1000^{o}C amorphous state is similar to currently used SiO_2 or SiON, with additional merit of full process compatibility with VLSI fabrication lines.

Finally, we have integrated low work function ytterbium (Yb) metal gate with high-κ $LaAlO_3$ dielectric into low-temperature poly-Si (LTPS) thin film transistors (TFTs). Good TFT performance was achieved - such as a high drive current, low threshold voltage and sub-threshold slope, as well as an excellent on/off current ratio and high gate-dielectric breakdown field. This was achieved without hydrogen

passivation or special crystallization steps. The good performance is related to the high gate capacitance density and small equivalent-oxide thickness provided by the high-κ dielectric.

1.4 Thesis Organization

This dissertation focused on the characterization of alternative metal gates and high-κ dielectric materials for the sub-45 nm technology node. In this chapter, the history of high-κ dielectrics and metal gate electrode evolution and the key materials have been reviewed. Chapter 2, 3, and 4 deeply study the $IrSi_x$ gate on HfSiON for p-MOS, Hf_xSi gate on HfSiON for n-MOS, TaN gate on HfLaON for n-MOS, respectively. Chapter 5 presents the study of Yb metal gate combining with a high-κ $LaAlO_3$ dielectric into low-temperature poly-Si TFTs. A summary and suggestion are presented in chapter 6.

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Year of Production	2005	2007	2010	2013	2016
MPU/ASIC Metal1 ½ Pitch (nm) (contacted)	90	68	45	32	22
Equivalent Oxide Thickness (EOT) Requirements					
Extended Planar Bulk (Å)	12	11	6.5		
UTB FD-SOI (Å)			7	5	
DG MOSFET (Å)				6	5
Gate Poly Depletion and Inversion-Layer Thickness Requirements					
Extended Planar Bulk (Å)	7.3	7.4	2.7		
UTB FD-SOI (Å)			4	4	
DG MOSFET (Å)				4	4
Saturation Threshold Voltage Requirements					
Extended Planar Bulk (mV)	195	165	151		
UTB FD-SOI (mV)			167	167	
DG MOSFET (mV)				185	195

Fig. 1-1 The evolution of CMOS technology requirements (ITRS 2005).

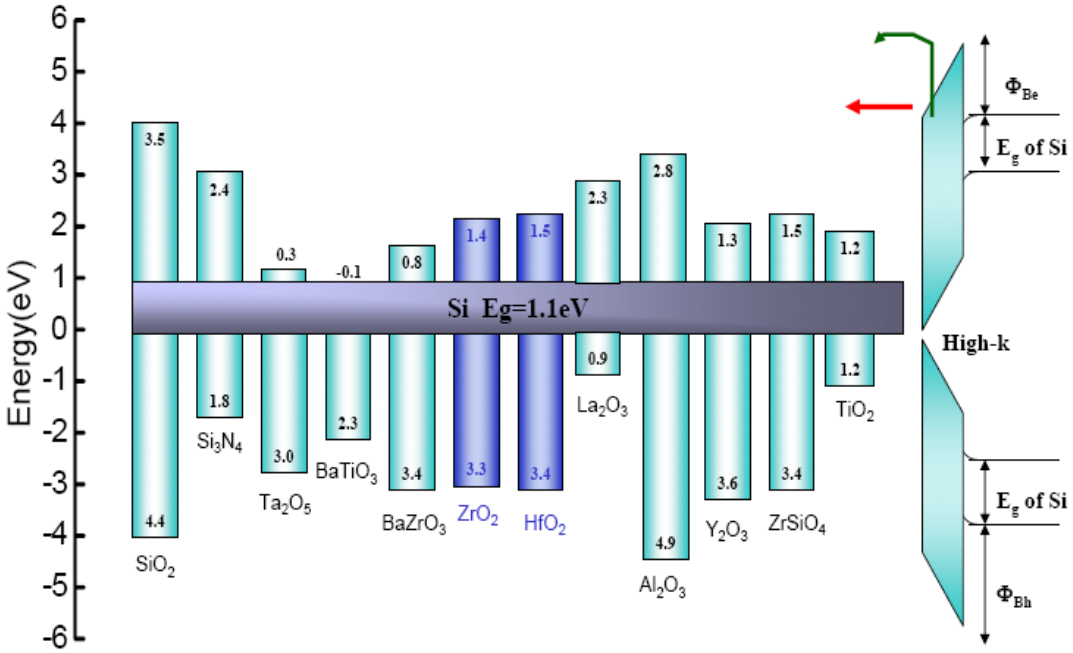

Fig. 1-2 The band offset of popular high-κ materials.

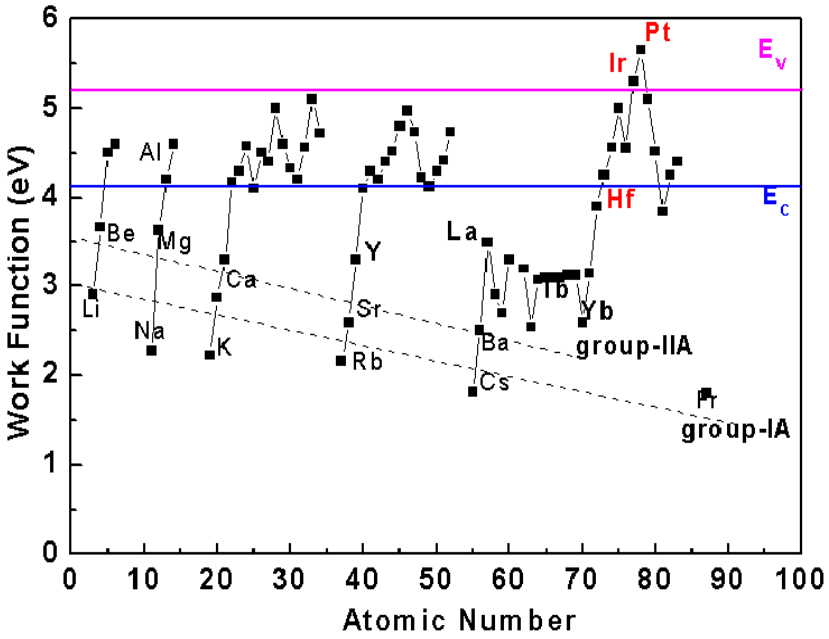

Fig. 1-3 The values of work function for different metal materials.

Chapter 2

High temperature stable Ir_xSi Gates with High Work Function on HfSiON p-MOSFETs

2.1 Introduction

To continue down-scaling VLSI technology and increase the integration density, high-κ gate dielectrics are needed for MOSFETs to reduce the large dc power consumption from gate leakage current [1]-[10]. In addition, metal gates are required to eliminate poly gate depletion. However, metal-gate/high-κ CMOSFETs show undesired high threshold voltages (V_t), which is opposite to the VLSI scaling trend. This phenomenon is known as "Fermi-level pinning" [1], although the background physics may be attributed to interface dipole and/or charged defects [1], [8]. To compensate this Fermi-level pinning effect, high work function metal electrodes larger than the 5.2 eV of p^+ poly-Si are needed. However, only Ir (5.27 eV) and Pt (5.65 eV) in the Periodic Table [11] can meet this requirement, which make the metal-gate/high-κ p-MOSFETs especially challenging [1]-[2]. Ir is more preferable than Pt due to a simpler etching process by reactive ion etching (RIE) [12]-[13]. Unfortunately, large metal diffusion through high-κ dielectrics was found in pure Ir gates after 1000°C RTA which caused p-MOS device failures [7]-[8]. Previous

attempts by using IrN to improve the thermal stability also failed due to weak Ir-N bonding strengths, where IrN decomposition and penetrating high-κ dielectrics were found after high temperature RTA [8]. Another possibility is using low temperature full silicidation (FUSI) gates [3]-[9]. However, the p-MOS devices incorporating high work function Pt_xSi or Ir_xSi still failed to integrate into the CMOS SALICIDE process due to the lack of required selective wet etching of Pt or Ir during SALICIDE.

To overcome this problem, we have proposed and demonstrated a new high temperature stable Ir_xSi FUSI gate on high-κ HfSiON. This is different from the low temperature FUSI process [3]-[6] since it is formed first before ion implantation and undergoes 1000°C RTA thermal cycle for implant activation. To achieve this high temperature stability goal, additional Si was inserted between Ir and high-κ HfSiON, where less Fermi-level pinning was obtained by forming Ir-rich Ir_xSi gates. High-κ HfSiON also has good metal diffusion barrier property [14]-[15], which is similar to our previous HfAlON [7]-[8] but it has the important advantage of better compatibility with currently used SiON gate dielectric with added Hf for higher κ value. After 1000°C RTA, Ir_xSi/HfSiON p-MOSFETs show good device integrity of a high effective work function ($\phi_{m\text{-}eff}$) of 4.95 eV, a small V_t of -0.15 V and a peak hole mobility of 84 cm^2/V-s. These results are compatible with and even better than the best reported metal-gate/high-κ p-MOSFETs [5]-[9].

2.2 Experimental procedure

The gate-first Ir_xSi/HfSiON p-MOSFETs were fabricated on 12-in N-type Si wafers with resistivity of 1~10 Ω-cm. After RCA cleaning, 4 nm HfSiO dielectric (Hf/(Hf+Si) = 50%) was deposited by atomic-layer deposition (ALD). HfSiON gate dielectric was formed by applying NH_3 plasma surface nitridation on HfSiO [16]. After post-deposition annealing (PDA), 5~30 nm amorphous Si and 20~30 nm Ir were deposited by PVD [7]. For Ir/Si/HfSiON capacitors, a 1000°C RTA was applied for 10 sec to form Ir_xSi gates. For MOSFETs, additional 400 nm Si was deposited on top of Ir/Si to avoid ion implantation penetrating through the thin Ir/Si. After gate definition, Boron was implanted at 25 KeV energy and 5×10^{15} cm^{-2} dose, and activated at 1000°C RTA for 10 sec. Meanwhile, Ir_xSi was also formed during RTA, where the x=3 was determined by x-ray diffraction measurements. Note that this process is different from the low temperature FUSI process [3]-[6], and such a simple self-aligned process is fully compatible to current VLSI lines. Secondary ion-mass spectroscopy (SIMS) was measured to study the Ir distribution profile. The fabricated p-MOSFETs were further characterized by *C-V* and *I-V* measurements. For comparison, Al and Ir gated MOS capacitors on HfSiON were also fabricated. To prevent the different oxide charge from causing error in $\phi_{m\text{-}eff}$ extraction, HfSiON was subjected to the same thermal cycle (1000°C RTA for 10 sec) before Al gate deposition.

2.3 Results and discussion

Fig. 2-1 shows the measured *C-V* characteristics of Ir_xSi, Ir and Al gates on HfSiON MOS devices. Low temperature Al gated HfSiON capacitors were used as a reference because pure metal deposited at low temperature has little interface reaction with high-κ dielectrics to cause Fermi-level pinning [10]. In addition, the flat band voltage (V_{fb}) is expressed as:

$$V_{fb} = \phi_{ms} - Q_f/C_{ox} = (\phi_m - \phi_s) - (Q_f/\varepsilon_o k_{ox})t_{ox} = (\phi_m - \phi_s) - (Q_f/\varepsilon_o k_{SiO2})EOT \quad (1)$$

where ϕ_m and ϕ_s are the work functions for metal gates and Si, respectively. Q_f, C_{ox}, t_{ox} and EOT are the oxide charge, capacitance, physical thickness and equivalent-oxide thickness for high-κ dielectrics, respectively. Since HfSiON has the same thermal cycle (1000°C RTA for 10 sec) before Al gate formation, the Q_f effect should be similar to FUSI gates. Therefore, the principal effect of V_{fb} shift might be due to the difference of effective ϕ_m. In comparing with the conventional $\phi_{m\text{-}eff}$ extraction from V_{fb}-t_{ox} or V_{fb}-EOT plot, this method uses a simple process without fabricating MOS devices with various t_{ox} and measuring the thickness carefully by transmission electron microscopy (TEM). Since the capacitance value or EOT of ~1.6 nm are the same for various gated HfSiON capacitors, the shifts of C-V curves with different gate electrodes are attributed to the different work functions. Ir/HfSiON after 900°C RTA has a large V_{fb} shift of 1.15 V to control low temperature Al gates (4.1 eV $\phi_{m\text{-}eff}$) that gives the required high $\phi_{m\text{-}eff}$ of 5.25 eV. This work function value is also

close to the reported 5.27 eV for Ir [11], indicating no pinning effect in pure metal Ir gates. This is due to weak bonding strengths of Ir-O or Ir-N that reduce the Fermi-level pinning related interface reaction [8]. However, Ir/HfSiON capacitors failed after 1000°C RTA. To improve thermal stability, additional amorphous Si of 5~30 nm was inserted between Ir and HfSiON. Good *C-V* characteristics were measured for Ir_xSi/HfSiON devices after the required 1000°C RTA for implant activation, although thermal stability was traded off at the Fermi-level pinning caused by the Si/HfSiON interface reaction. However, the continuously increasing V_{fb} toward the value of pure Ir gates was observed by decreasing the inserted amorphous Si layer, and a high $\phi_{m\text{-}eff}$ of 4.95 eV was obtained for Ir_xSi/HfSiON devices with the inserted 5 nm amorphous Si. This 4.95 eV $\phi_{m\text{-}eff}$ is significantly larger than Ni_3Si/HfSiON [6]. This result is also slightly better than previous Ir_xSi/HfAlON [7] due to thinner amorphous Si on high-κ dielectrics. Slow depletion for Ir_xSi/HfSiON devices with 30 nm amorphous Si may be due to non-uniform silicidation as examined by TEM, where locally un-reacted Si was found to cause voltage drop in gate electrodes. The formation of FUSI gates is evident from the same inversion and accumulation capacitances measured in MOSFETs.

Fig. 2-2 shows the *J-V* characteristics of Ir_xSi, Ir and Al gates on high-κ HfSiON devices. After 1000°C RTA, Ir/HfSiON devices failed due to large leakage current. In

sharp contrast, Ir_xSi gates on HfSiON showed successfully improved thermal stability to 1000°C RTA, which is evident from low leakage current comparable with P^+ poly-Si gates [17]. Here high temperature thermal cycle is required for dopant activation after ion implantation.

We have further used the X-Ray Diffraction (XRD) measurements to characterize the Ir_xSi. As shown in Fig. 2-3, the Ir-rich Ir_xSi with x=3 was found with distinct 2θ angle to residual Ir peak. The measured large V_{fb} shift of Ir_xSi is supported by SIMS profile as shown in Fig. 2-4. Here Ir segregation toward amorphous Si was measured to form Ir_xSi on HfSiON surface. Such FUSI formation directly on high-κ dielectrics is known to reduce Fermi-level pinning [6]-[8]. Therefore, good thermal stability of 1000°C RTA, a reasonable high $\phi_{m\text{-}eff}$ of 4.95 eV, and low gate dielectric leakage current can be simultaneously achieved in Ir_xSi/HfSiON MOS capacitors. To the best of our knowledge, this is the highest reported $\phi_{m\text{-}eff}$ in high-κ Hf-based oxide [5]-[8]. These are the few methods to achieve a high $\phi_{m\text{-}eff}$ in Hf-based oxide p-MOS devices. Although the V_{fb} tuning can be reached by impurity segregation in FUSI/SiON, this method becomes less useful in high-κ metal-oxide due to the stronger interface reaction. In the following we will study Ir_xSi/HfSiON devices with the thinnest 5 nm amorphous Si. This is because the V_{fb} of thicker Si layer is too low for p-MOSFETs application.

Fig. 2-5 shows the transistor I_d-V_d characteristics as a function of V_g-V_t for 1000°C RTA Ir_xSi/HfSiON p-MOSFETs. The well-behaved I_d-V_d curves of Ir_xSi/HfSiON transistors show little device performance degradation.

Fig. 2-6 shows the I_d-V_g characteristics of Ir_xSi gated p-MOSFETs with HfSiON as the gate dielectric. A small V_t as low as -0.15 V is obtained from the linear I_d-V_g plot, which is consistent with the large $\phi_{m\text{-}eff}$ of 4.95 eV from C-V curves and the Ir accumulation on HfSiON from SIMS.

Figs. 2-7 shows the extracted hole mobilities versus gate electric fields from the measured I_d-V_g data of Ir_xSi/HfSiON p-MOSFETs. High hole mobilities of 84 and 53 cm^2/V-s are obtained at peak value and 1 MV/cm effective field for Ir_xSi/HfSiON p-MOSFETs, respectively, which is compatible with the published data in the literature [5]-[8]. Good hole mobilities also indicate low Ir diffusion through HfSiON to inversion channel, even though excess Ir is necessary to prevent un-reacted amorphous Si from causing gate depletion or increased Fermi-level pinning. Therefore, a high $\phi_{m\text{-}eff}$, a small V_t and good hole mobilities are simultaneously achieved in Ir_xSi/HfSiON p-MOSFETs with additional merit of process compatible to current VLSI lines.

2.4 Conclusion

Good device performance of Ir_xSi/HfSiON p-MOSFETs is shown by a high

$\phi_{m\text{-}eff}$ of 4.95 eV, a small V_t of -0.15 V, a peak hole mobility of 84 cm^2/V-s and 1000^oC RTA thermal stability with the advantage of full process compatible to current VLSI lines.

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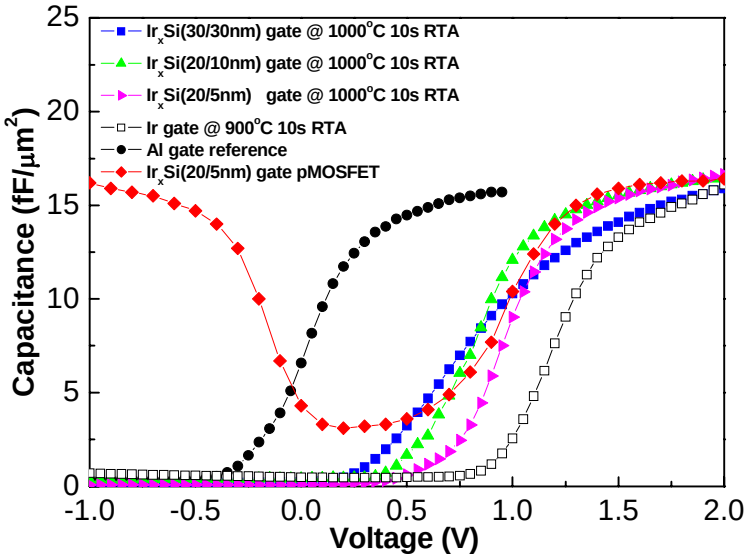

Fig. 2-1 *C-V* characteristics of HfSiON/n-Si with Ir_xSi, Ir and Al gates capacitors. The device areas are 100 μm × 100 μm.

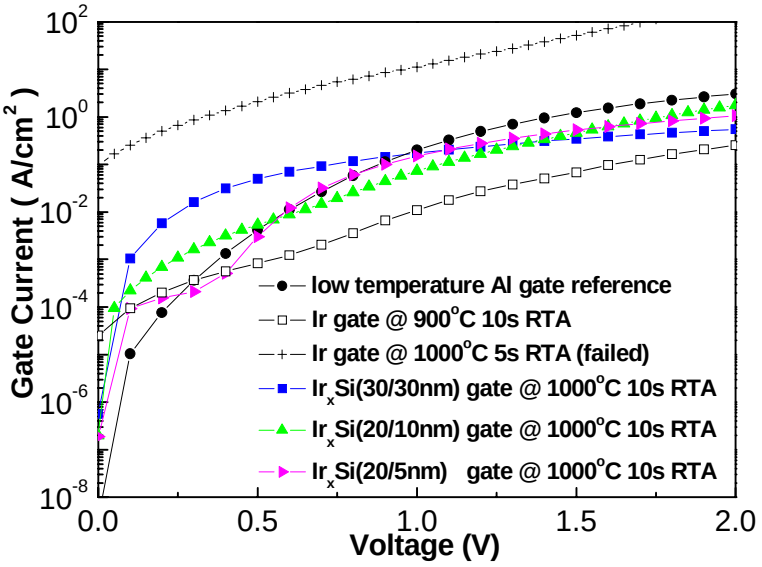

Fig. 2-2 *J-V* characteristics of HfSiON/n-Si with Ir_xSi, Ir and Al gates capacitors.

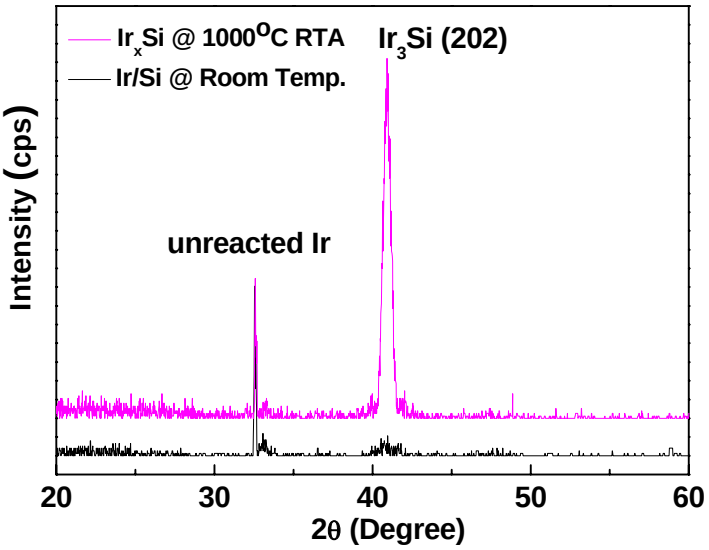

Fig. 2-3 XRD profiles of Ir_3Si/HfSiON structures.

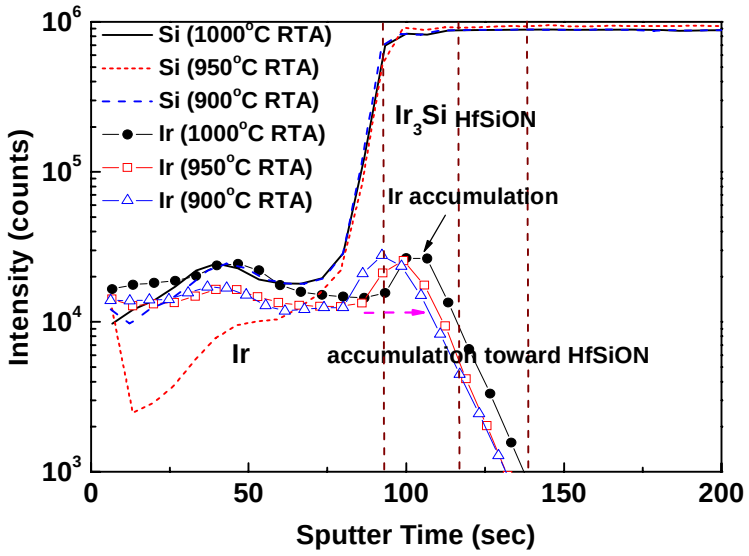

Fig. 2-4 SIMS profile of Ir_3Si gates on HfSiON at different RTA temperature. The Ir_3Si accumulated toward HfSiON interface is found to un-pin the Fermi-level.

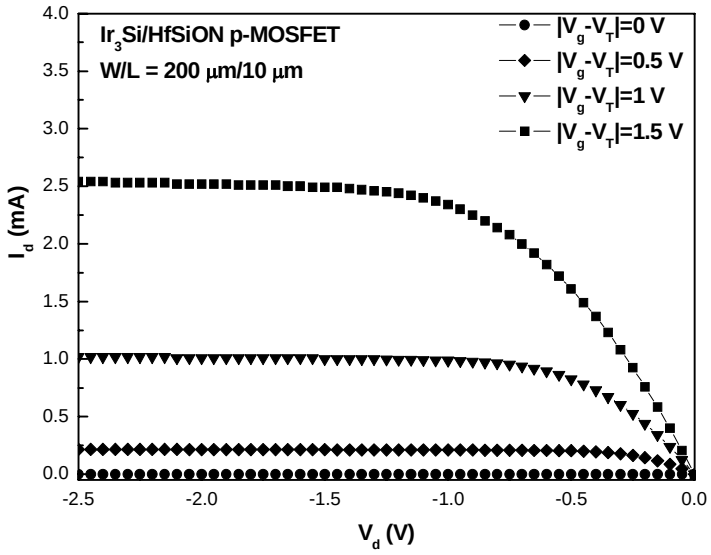

Fig. 2-5 The I_d-V_d characteristics of Ir_3Si/HfSiON p-MOSFETs.

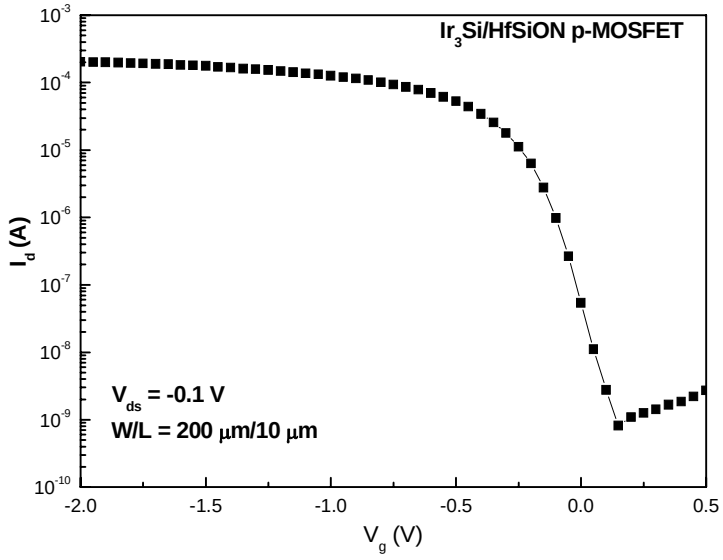

Fig. 2-6 The I_d-V_g characteristics of Ir_3Si/HfSiON p-MOSFETs.

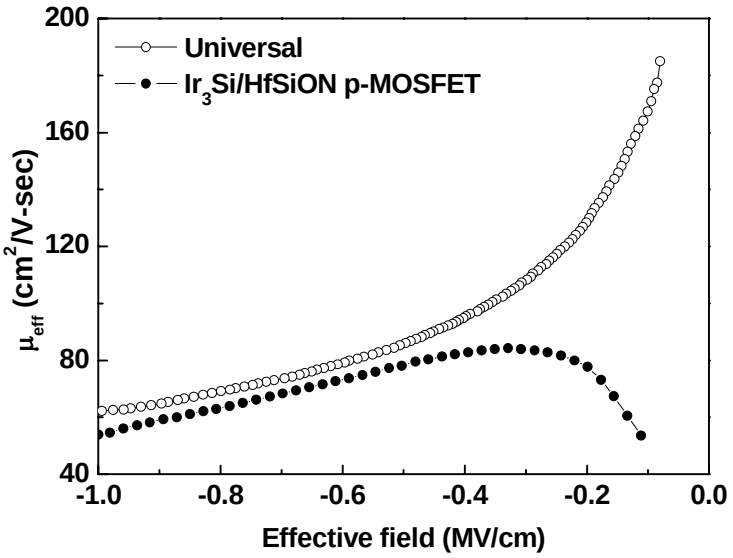

Fig. 2-7 The extracted hole mobilities from I_d-V_g characteristics of Ir_3Si/HfSiON p-MOSFETs.

Chapter 3

HfSiON n-MOSFETs Using Low Work Function $HfSi_x$ Gates

3.1 Introduction

To continue the VLSI scaling trend, the using metal gate and high-κ gate dielectric are needed to reduce the DC power consumption and gate depletion [1]-[12]. However, one of the difficult challenges for metal-gate/high-κ MOSFET is the large threshold voltage (V_t) by Fermi-level pinning that is opposite to scaling trend. To overcome this problem, low and high work-function metal-gates are required to reduce the pinning effect. Previously, we have reported the Ir_xSi gate on HfAlON has high effective work-function ($\phi_{m\text{-}eff}$) of 4.9 eV [12] and useful for p-MOS. For n-MOSFET, the novel TaC gate has shown low $\phi_{m\text{-}eff}$ [1]-[2]. However, the Full Silicidation (FUSI) gate [3]-[5], [8]-[13] for n-MOS is still needed to develop, which is due to the inherent advantage of the process compatibility with current poly-Si gate CMOS technology. In this chapter, we have used the similar method of previously reported Ir_xSi for p-MOS [12] to develop the low work-function $HfSi_x$ gate for n-MOSFET. This is because the Hf has very low work function of 3.5 eV in the Periodic Table. The Hf_xSi gate on HfSiON, formed by Hf deposition on thin

amorphous-Si, gives a low $\phi_{m\text{-}eff}$ of 4.27 eV and a good electron mobility of 216 cm^2/V-s. In addition, the $HfSi_x$/HfSiON can sustain a high RTA temperature annealing of 1000°C that is compatible with current VLSI process line. These results indicate the potential application for metal-gate/high-κ n-MOSFETs.

3.2 Experimental procedure

We have used the 12-inch p-type Si wafers in this study. After standard clean, the HfSiO was deposited by atomic-layer deposition (ALD) and the HfSiON was formed by applying direct nitrogen plasma to HfSiO surface. Then amorphous Si with various thickness of 50 to 5 nm was deposited on HfSiON as a silicide layer and metal barrier for subsequently deposited Hf by PVD. A Mo layer was also deposited to cover the Hf to prevent oxidation. The MOS capacitor was formed by patterning and RTA annealing at 1000°C for 10 sec. For n-MOSFET, additional 150 nm thick amorphous-Si was deposited on Hf/Si/HfSiON to prevent ion implantation penetration through gate, where the n^+ source-drain regions are formed by using a phosphorus ion implantation at 35 KeV. Then the 1000°C RTA was applied to activate the implanted dopant and the n-MOSFET was fabricated by this self-aligned gate first process. Note that the FUSI $HfSi_x$ gate is formed at high temperature RTA and similar to previous Ir_xSi gate [12], which are different from conventional low temperature salicide process. At such high 1000°C RTA temperature, the fast silicidation reaching

to the Si/HfSiON interface may also reduce the reaction of thin amorphous Si (5 nm) with high-κ dielectric to cause Fermi-level pinning. For comparison, Al gated devices on HfSiON were also formed. The fabricated devices were characterized by *C-V* and *I-V* measurements.

3.3 Results and discussion

Figs. 3-1 shows the *C-V* characteristics for $HfSi_x$/HfSiON and control Al/HfSiON capacitors, where the $HfSi_x$ gate was formed at 1000°C RTA. The Al-gated capacitor was used as a reference since it is known to have little Fermi-level pinning of low-temperature deposited pure metal gate on high-κ dielectric [7]. For thicker amorphous-Si of 50 and 10 nm on HfSiON, the capacitance density decreases with increasing the thickness of amorphous-Si indicating in $HfSi_x$ gate on HfSiON not fully silicided. This in tern gives a higher flat band voltage (V_{fb}) due to the Fermi-level pinning on high-κ dielectric. In contrast, the $HfSi_x$ formed by thin 5 nm amorphous-Si shows the same capacitance density with control Al gate suggesting the successful FUSI gate formation. From the *C-V* shift referenced to the control Al gate, an extracted $\phi_{m\text{-}eff}$ of 4.27 eV is obtained for $HfSi_x$/HfSiON that is suitable for n-MOS application. The low V_{fb} and $\phi_{m\text{-}eff}$ for $HfSi_x$ gate capacitors with 5 nm amorphous-Si may be due to the Hf diffusion toward the HfSiON surface through thin amorphous-Si that decreases the work function. Figs. 3-2 shows the *J-V* characteristics for

$HfSi_x$/HfSiON and control Al/HfSiON capacitors. Low leakage current of 1.9×10^{-5} A/cm at -1 V is measured at an equivalent oxide thickness (EOT) of ~1.6 nm, which suggests the good thermal stability of $HfSi_x$ gate on HfSiON dielectric even after 1000°C RTA. Therefore, improved Fermi-level pinning, reasonable low $\phi_{m\text{-}eff}$ of 4.27 eV and a low gate dielectric leakage current can be achieved in $HfSi_x$/HfSiON MOS capacitors at the same time.

Fig. 3-3 shows the transistor I_d-V_d characteristics as a function of V_g-V_t for the 1000°C RTA-annealed $HfSi_x$/HfSiON n-MOSFETs. The well-behaved I_d-V_d curves indicate the good device performance by using an $HfSi_x$ gate. Fig. 3-4 displays I_d-V_g characteristics of the $HfSi_x$/HfSiON n-MOSFETs. A low V_t of only 0.1 V was measured from the linear I_d-V_g plot, which is due to the low $\phi_{m\text{-}eff}$ of 4.27 eV from the C-V measurements.

Fig. 3-5 shows the electron mobility extracted from the measured I_d-V_g curves of the n-MOSFETs. A peak electron mobility of 216 cm^2/V-s was obtained for the $HfSi_x$/HfSiON n-MOSFETs, which is close to published data in literature [13]-[14].

3.4 Conclusion

Using the novel $HfSi_x$ gate formed by thin amorphous-Si on HfSiON, good device performance has been obtained for n-MOSFETs with low $\phi_{m\text{-}eff}$ and V_t values. This promising $HfSi_x$/HfSiON n-MOSFET has additional merit of full process

compatibility with current VLSI lines.

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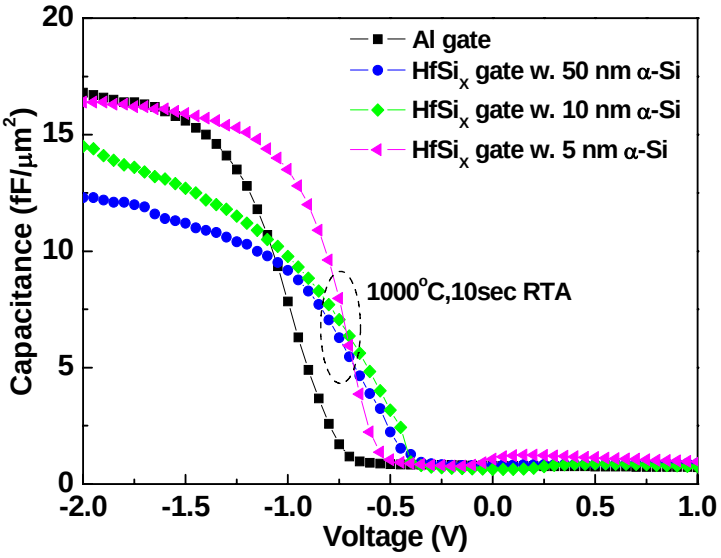

Fig. 3-1 *C-V* characteristics for high temperature RTA formed $HfSi_x$/HfSiON and low temperature Al/HfSiON capacitors. The device area was 100 μm×100 μm.

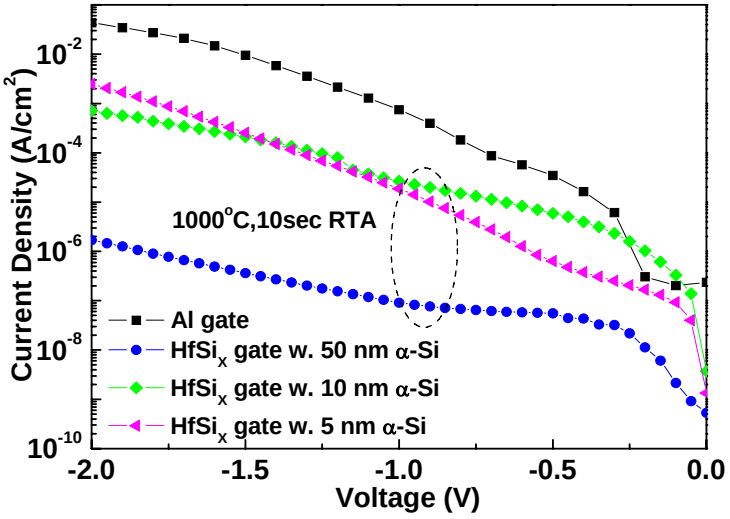

Fig. 3-2 *J-V* characteristics of $HfSi_x$/HfSiON and low temperature Al/HfSiON capacitors.

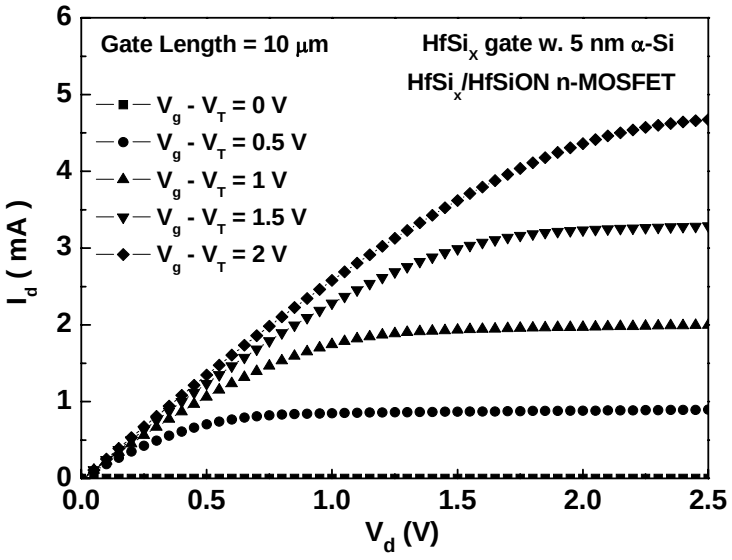

Fig. 3-3 The I_d-V_d characteristics of $HfSi_x$/HfSiON n-MOSFETs. The amorphous-Si on HfSiON was 5 nm and gate length was 10 μm.

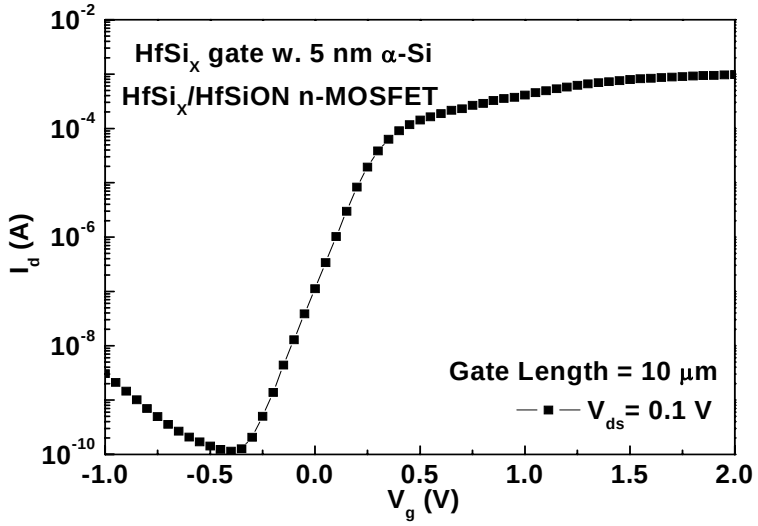

Fig. 3-4 The I_d-V_g characteristics $HfSi_x$/HfSiON n-MOSFETs. The amorphous-Si on HfSiON was 5 nm and gate length was 10 μm.

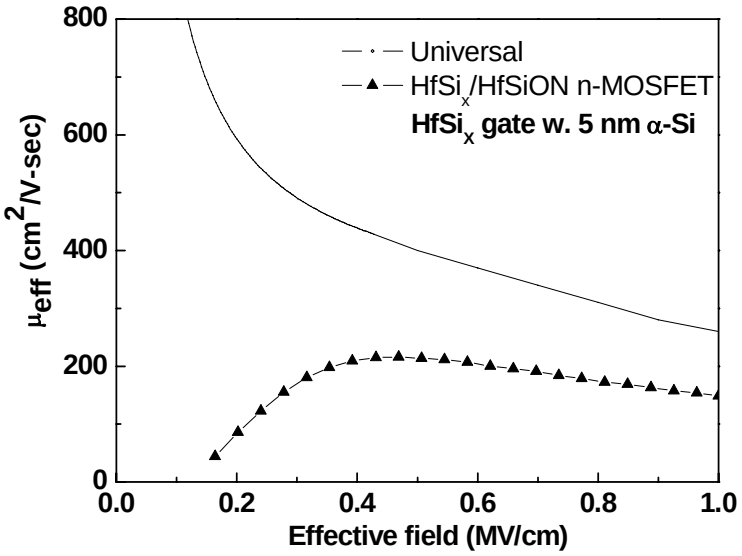

Fig. 3-5 The electron mobilities of $HfSi_x$/HfSiON n-MOSFETs.

Chapter 4

Novel High-κ HfLaON n-MOSFETs with Preserved Amorphous State to 1000°C

4.1 Introduction

The high-κ gate dielectric is needed for future generation MOSFET to reduce the dc power consumption [1]-[16]. The ideal high-κ MOSFET requires higher κ value for lower leakage current, less Fermi-level pinning for low threshold voltage (V_t), high mobility and 1000°C stability for ion implant doping activation. Unfortunately, the widely studied HfO_2 [1]-[2] is known to react with Si substrate at high temperature and causes κ value reduction. The other problem of HfO_2 is the unwanted crystallization at high temperature- this is different from the currently used amorphous SiO_2 or SiON and may cause charge trapping in poly-grain boundaries. To overcome these problems, the HfSiON [3]-[6] and HfAlON [7] are developed by adding high temperature stable SiO_2, Al_2O_3 and Nitrogen into HfO_2. However, again the κ value is reduced. An alternative way is to increase the dielectric entropy, which is realized by adding another high-κ such as Ta_2O_5 into HfO_2 [8]. Nevertheless, the small conduction band discontinuity of ~0.3 eV for Ta_2O_5/Si is the major concern. To address this issue, the HfLaO was proposed and shown good MOSFET characteristics

[9]-[11] with less Fermi-level pinning by added La_2O_3 [12]-[16]. However, the crystallization temperature of HfLaO is close to 900°C [9], [11] but still less than the required 1000°C RTA for source-drain implant activation. In this chapter, we have developed the novel HfLaON gate dielectric that remains amorphous at 1000°C with still high-κ value of 20. After a 1000°C RTA, the self-aligned TaN/HfLaON MOSFET showed low leakage current of 2.7×10^{-6} A/cm^2 at 1 V above flat-band voltage (V_{fb}), an effective work function ($\phi_{m\text{-}eff}$) of 4.24 eV and a peak electron mobility 217 cm^2/V-s at 1.6 nm equivalent-oxide thickness (EOT), with additional merit of full process compatible with current VLSI fabrication lines.

4.2 Experimental procedure

After standard clean, the 7 nm thick HfLaO with 1 to 1 Hf:La ratio was deposited by physical vapor deposition (PVD) and followed by post deposition anneal (PDA), although atomic layer deposition (ALD) of HfO_2 and La_2O_3 [15] were previously demonstrated. The HfLaON was formed by applying NH_3 plasma surface nitridation [6]-[7] on HfLaO. The gate-first TaN/HfLaON n-MOSFET was fabricated by depositing 150 nm TaN by PVD, device patterning, phosphorus ion implantation to source-drain at 25 KeV and 5×10^{15} cm^{-2} dose, and 1000°C RTA to activate the implanted dopant. This self-aligned process is fully compatible with currently used poly-Si/SiON MOSFETs for IC fabrication. The crystallization effect of HfLaON was

examined by grazing incident x-ray diffraction (XRD), X-ray Photoelectron Spectroscopy (XPS), Transmission Electron Microscope (TEM) and Secondary Ion Mass Spectrometry (SIMS) measurements and the fabricated n-MOSFETs were characterized by *C-V* and *I-V* measurements.

4.3 Results and discussion

Fig. 4-1 shows the XRD spectra of HfLaO under different RTA temperature. Although the HfLaO is amorphous at 800^{o}C RTA, strong unwanted crystallization is clearly measured at 1000^{o}C RTA for 10 sec. This result is consistent with previous study on HfLaO crystallization [9], [11]. The XRD spectra of HfLaON under different RTA temperature are shown in fig. 4-2. In sharp contrast, the HfLaON can remain the amorphous state even after the same 1000^{o}C for 10 sec RTA.

The existence of Hf, La, O and N in HfLaON is confirmed by XPS in Fig. 4-3. The dielectric physical interface was further examined by cross-sectional TEM in Fig. 4-4. The TEM photo shows good amorphous HfLaON even after 1000^{o}C RTA and smooth interface.

Fig. 4-5 & 4-6 show the *J-V* and *C-V* characteristics on various nitridation conditions for HfLaON: the thermal stability at 1000^{o}C RTA improves with increasing $NH3^{+}$ time but trading off the increasing pinning effect compared with previous HfLaO case [11].

Figs. 4-7 and 4-8 show the *C-V* and *J-V* characteristics for TaN/HfLaON MOS capacitors with various RTA temperatures, respectively. Low V_{fb} away from midgap is still measured even after 1000°C RTA. A $\phi_{m\text{-}eff}$ of 4.24 eV is obtained by the V_{fb} shift to control Al gate on 1000°C-annealed HfLaON. Such low temperature deposited metal gate is known to have little interface reaction caused Fermi-level pinning [3], [6]-[7] and the same 1000°C RTA thermal cycle ensures the close oxide charges. Although the $\phi_{m\text{-}eff}$ is relatively higher than the TaN/HfLaO [10]-[11] by surface nitridation in HfLaON, this is traded off the 1000°C amorphous state stability. In addition, low leakage current of 2.7×10^{-6} A/cm^2 was obtained at 1 V above V_{fb} with 1.6 nm EOT. From the careful thickness measurement from cross-sectional transmission electron microscopy, a κ value of 20 is still obtained even after 1000°C RTA that is in sharp contrast to the degraded κ in HfO_2 by interfacial silicate formation [9]. Therefore, low gate dielectric leakage current, low $\phi_{m\text{-}eff}$ and improved 1000°C amorphous state stability are simultaneously obtained in novel HfLaON MOS capacitors using simple TaN gate.

The TaN/HfLaON structures are further analyzed by SIMS. Fig. 4-9 shows the SIMS profile of TaN gate on HfLaON at different RTA temperature. No Ta penetration through HfLaON can be found. Such good device characteristics are due

to the nitridation on thick high-κ that prevents TaN metal from diffusing through the HfLaON gate dielectric.

Fig. 4-10 shows the comparison of gate leakage current density for MOS devices with SiO_2 and HfLaON gate dielectric. Much improved leakage current than SiO_2 is obtained at 1.6 nm EOT. The dielectric constant of HfLaON at different RTA temperature is shown in fig. 4-11. Significant higher κ value of 20 is still preserved even after 1000°C RTA and much better than HfO_2.

Fig. 4-12 shows the transistor I_d-V_d characteristics of the 1000°C RTA-annealed TaN/HfLaON n-MOSFETs. The well-behaved I_d-V_d curves indicate the good device performance by using a TaN gate. Furthermore, a low V_t of 0.18 V was measured from the linear I_d-V_g characteristics shown in fig. 4-13, which is due to the low $\phi_{m\text{-}eff}$ from the C-V measurements.

Fig. 4-14 shows the electron mobility extracted from the measured I_d-V_g characteristics of the n-MOSFETs. A peak electron mobility of 217 cm^2/V-s was obtained for the TaN/HfLaON n-MOSFETs, which is close to the published data of Hf-based oxides in literature [2]-[3], [5]-[8].

Further reliability study is from the BTI shown in fig. 4-15. The threshold voltage shifts (ΔV_t) < 20 mV are measured for TaN/HfLaON n-MOSFETs at 10 MV/cm stress and 85°C for 1 hr.

4.4 Conclusion

We have developed novel high-κ HfLaON gate dielectric that can preserve the amorphous state to 1000^{o}C RTA and similar with currently used SiO_2 or SiON. The gate-first and self-aligned TaN/HfLaON n-MOSFETs showed low leakage current of 2.7×10^{-6} A/cm^2 at 1 V above flat-band voltage, an effective work function of 4.24 eV and a peak electron mobility 217 cm^2/V-s at 1.6 nm equivalent-oxide thickness, with additional merit of full process compatible with current VLSI lines.

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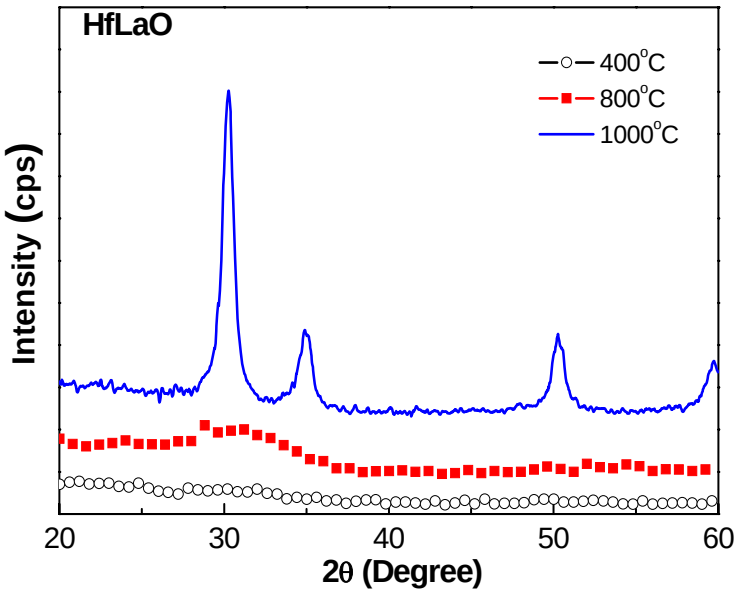

Fig. 4-1 Grazing incident XRD spectra of HfLaO after different RTA temperature.

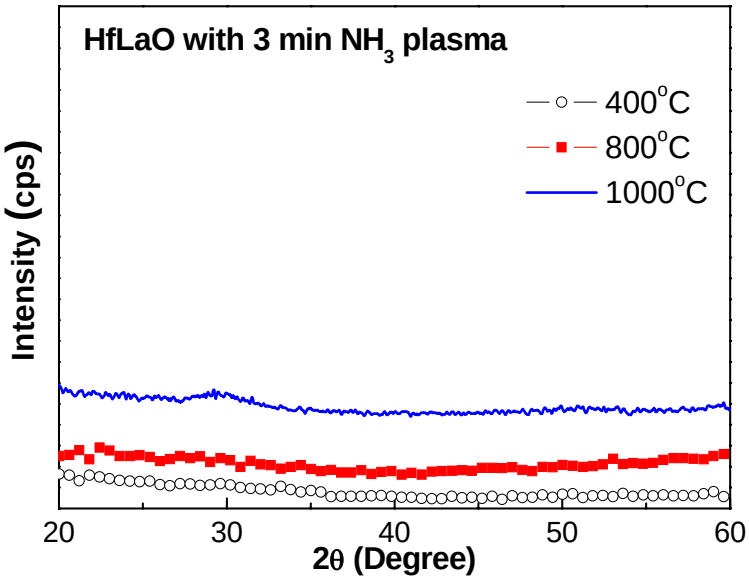

Fig. 4-2 Grazing incident XRD spectra of HfLaON with NH_3 plasma after different RTA temperature. In contrast to the HfLaO case, HfLaON stays amorphous state after 1000°C RTA.

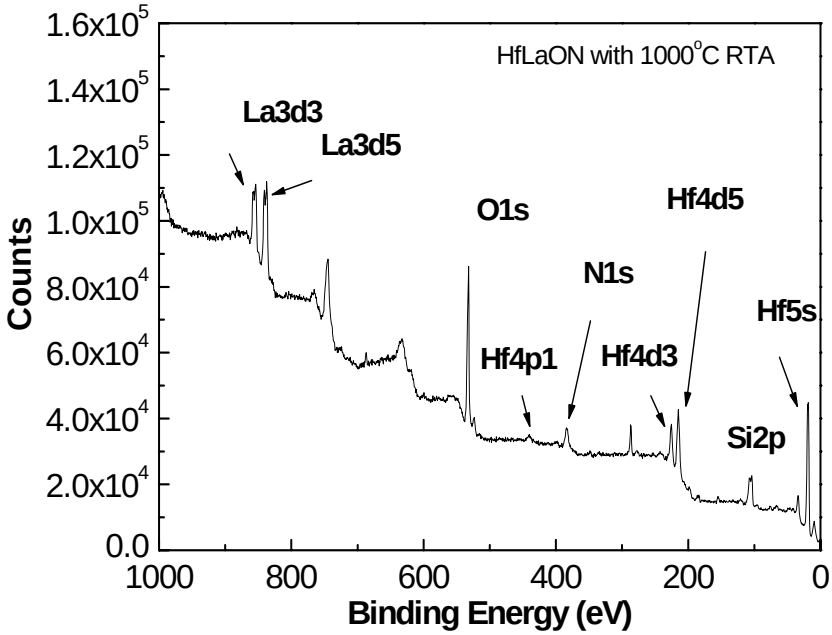

Fig. 4-3 XPS spectra of HfLaON after 1000°C RTA. The existence of Hf, La, O, and N is clearly seen.

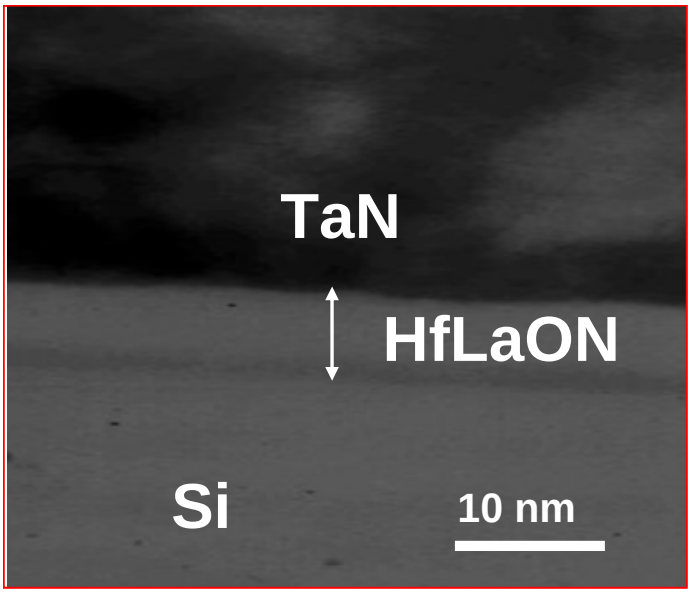

Fig. 4-4 TEM image of TaN/HfLaON/Si after 1000°C RTA. Good interface property is observed with very thin interfacial layer.

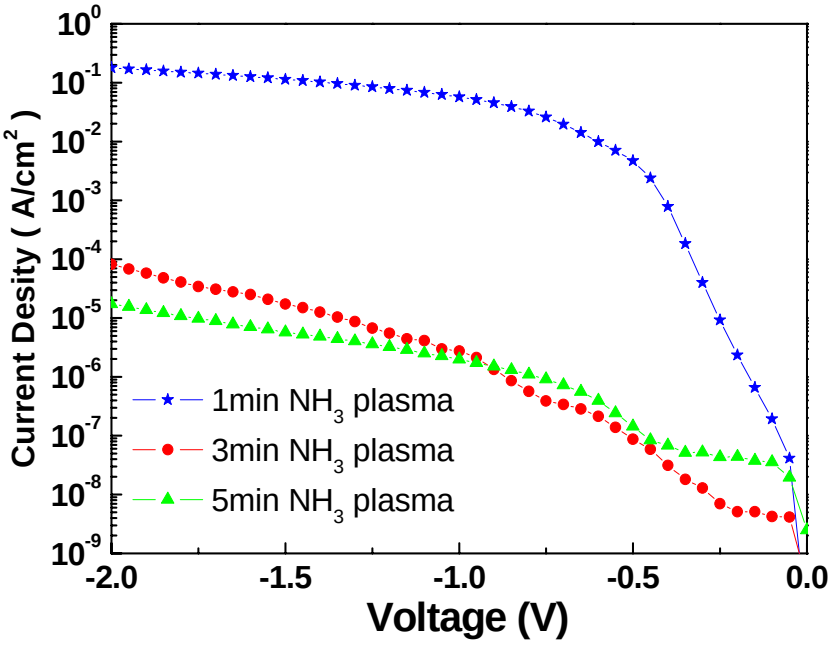

Fig. 4-5 *J-V* characteristics of 1000°C-annealed TaN/HfLaON n-MOS capacitors with various N^+ nitridation.

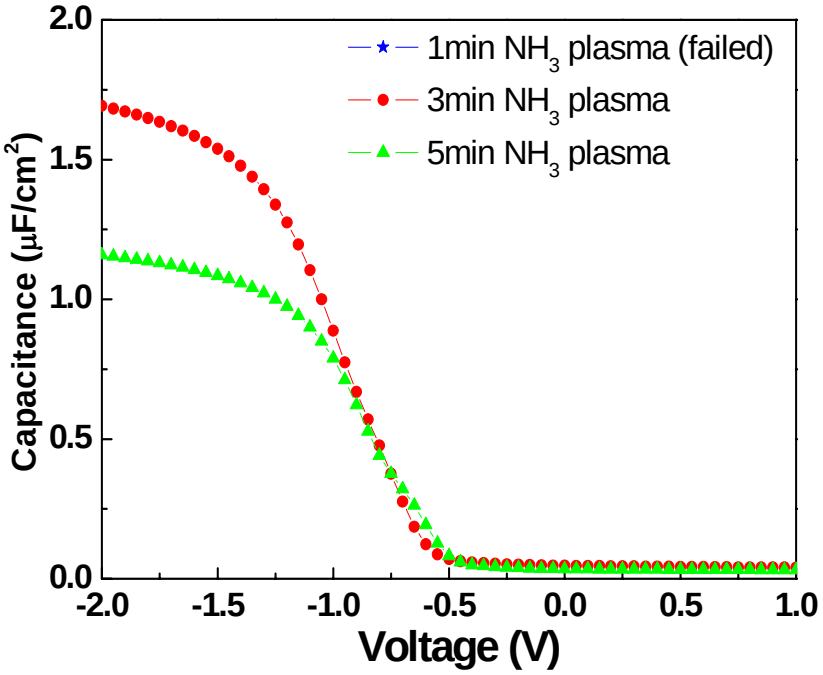

Fig. 4-6 *C-V* characteristics of 1000°C-annealed TaN/HfLaON n-MOS capacitors with various N^+ nitridation.

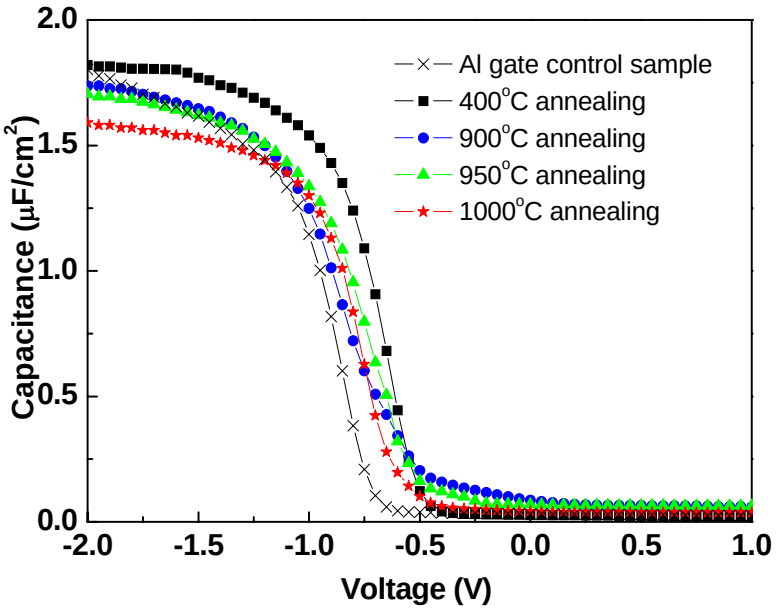

Fig. 4-7 *C-V* characteristics of TaN/HfLaON n-MOS capacitors after different temperature RTA. The device area was 100 μm×100 μm.

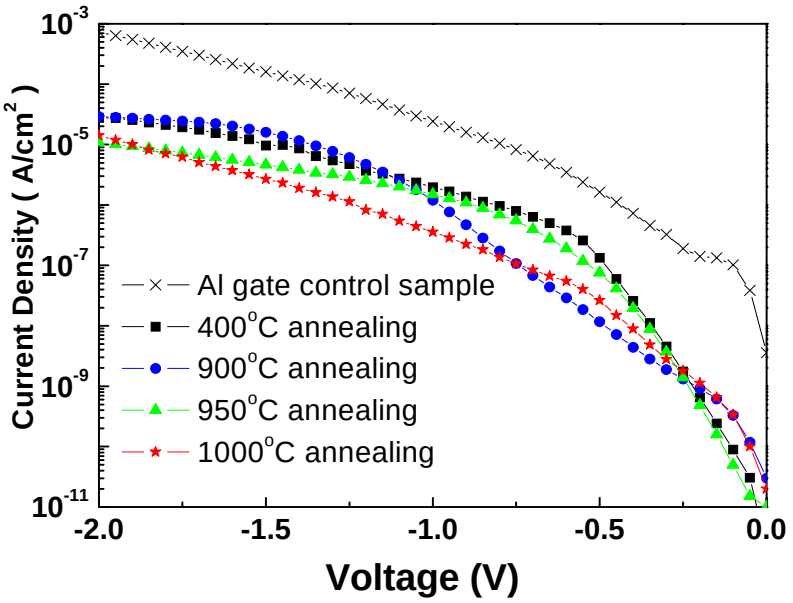

Fig. 4-8 *J-V* characteristics of TaN/HfLaON n-MOS capacitors after different temperature RTA.

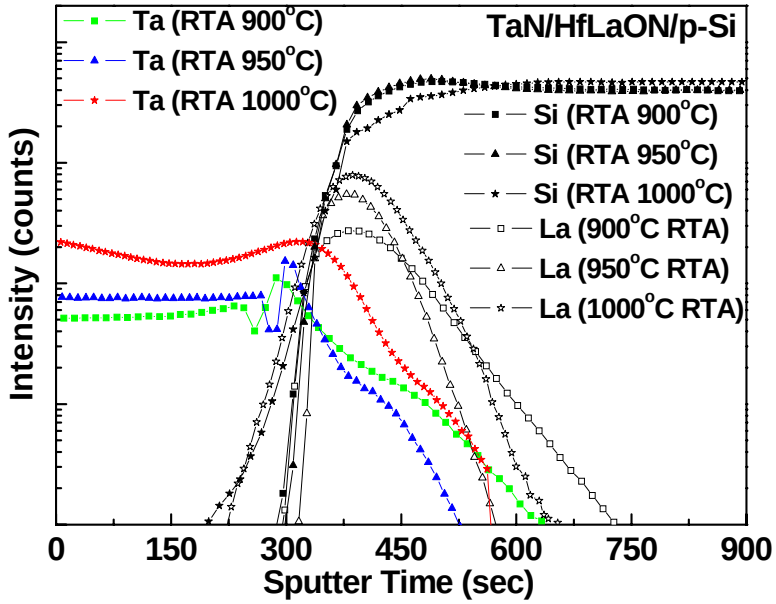

Fig. 4-9 SIMS profile of TaN gate on HfLaON at different temperature RTA. No Ta penetration through HfLaON can be found.

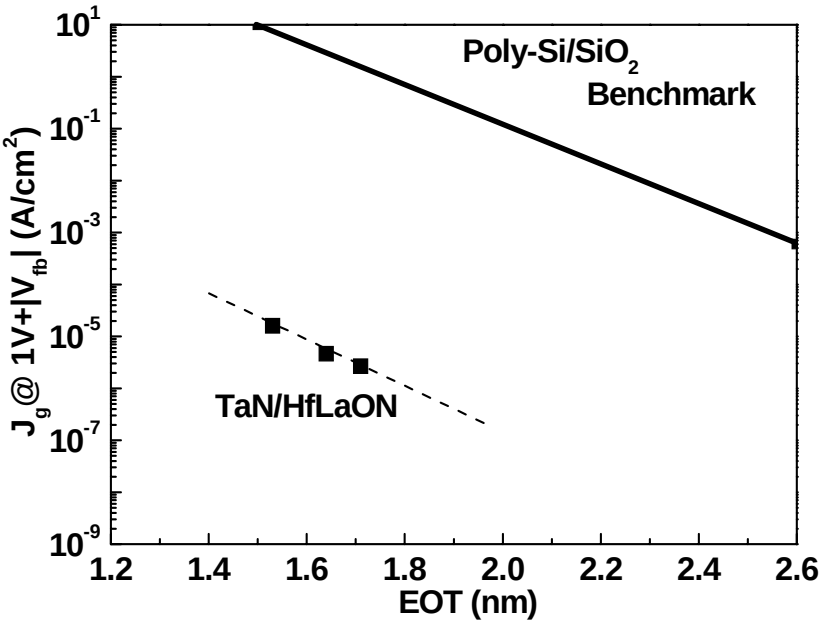

Fig. 4-10 The comparison of gate leakage current density for MOS devices with SiO_2 and HfLaON gate dielectrics.

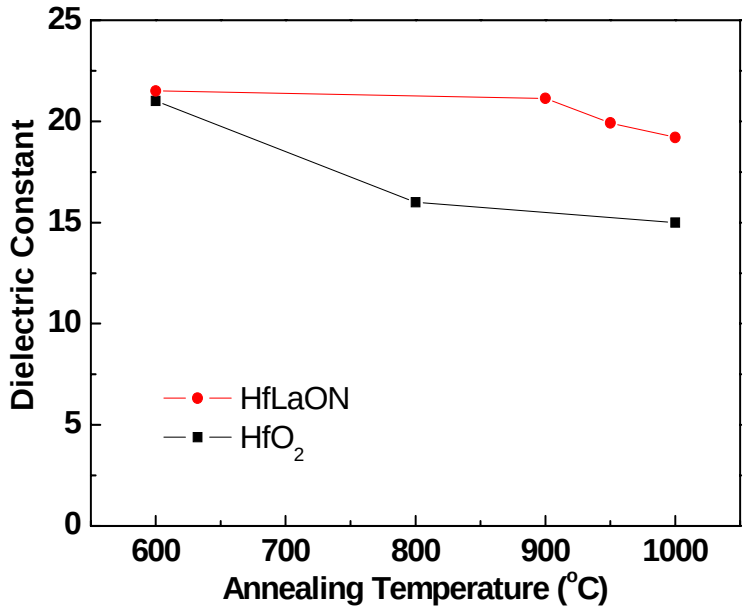

Fig. 4-11 The dielectric constant of HfLaON at different RTA temperature. Significant higher κ value at high RTA temperature is obtained than HfO_2.

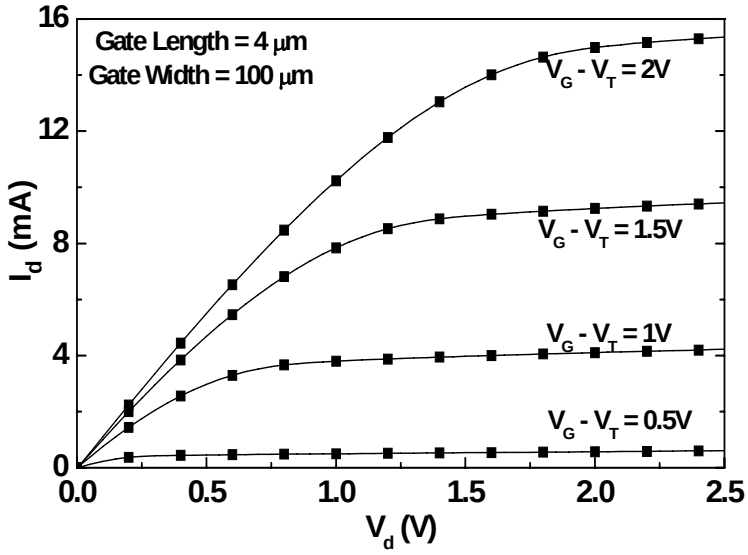

Fig. 4-12 The I_d-V_d characteristics of TaN/HfLaON n-MOSFETs fabricated at 1000°C RTA thermal cycle.

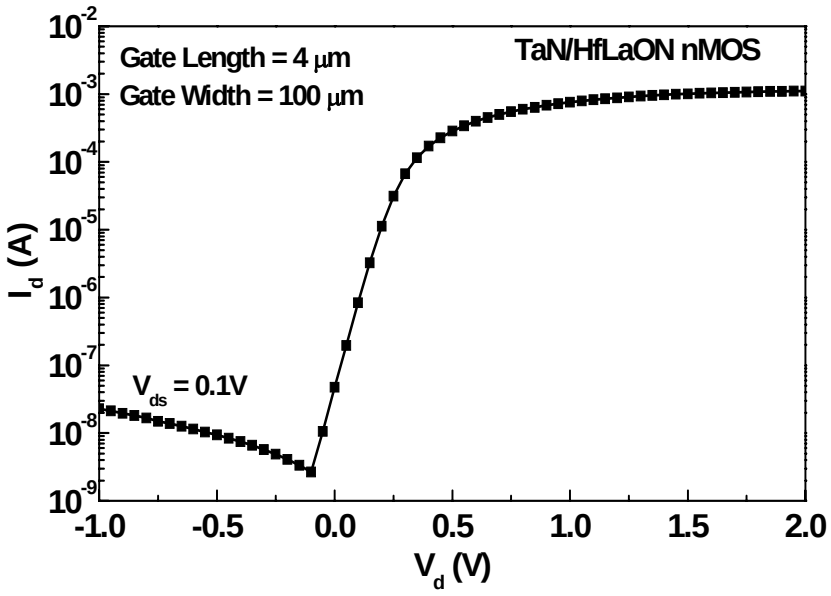

Fig. 4-13 The I_d-V_g characteristics of TaN/HfLaON n-MOSFETs fabricated at 1000°C RTA thermal cycle.

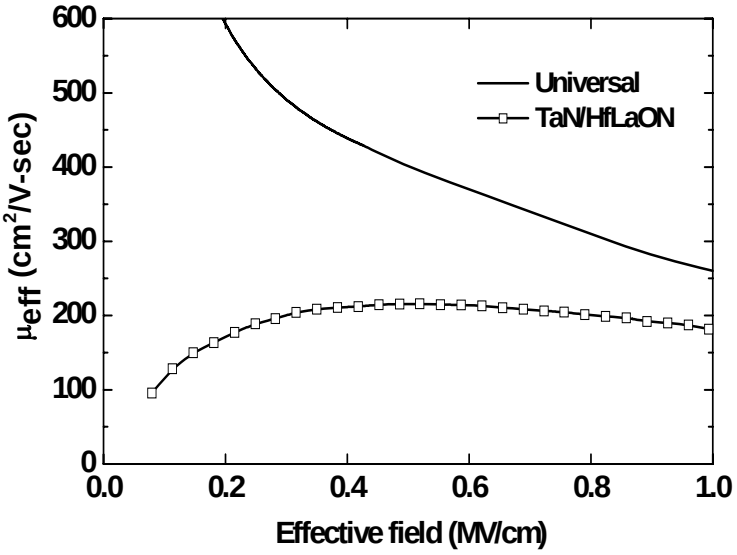

Fig. 4-14 The electron mobilities of TaN/HfLaON n-MOSFETs fabricated at 1000°C RTA thermal cycle.

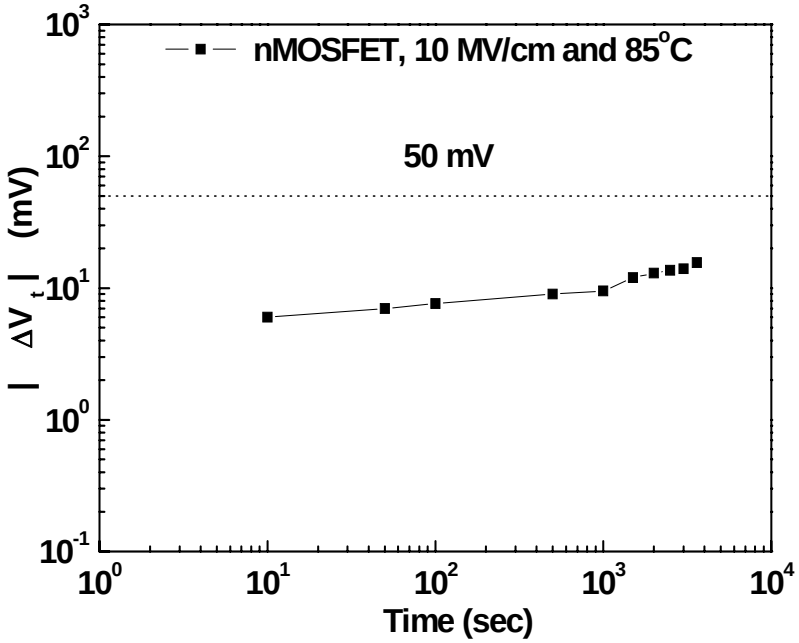

Fig. 4-15 The ΔV_t of TaN/HfLaON n-MOSFETs stressed at 85°C and 10 MV/cm for 1 hour.

Chapter 5

Poly-Silicon Thin Film Transistors Using Ytterbium Metal Gate and $LaAlO_3$ Dielectric

5.1 Introduction

One fundamental challenge for low-temperature poly-Si (LTPS) thin-film transistor (TFT) [1]-[8] is to develop high performance TFTs used for both pixel and display circuits [2]. Since the pixel TFTs need to drive the liquid crystal, the device requirements are high voltage operation and low gate leakage currents. For high speed display circuits, the TFT device requires low voltage operation and high drive currents. To meet above both requirements, we have previously demonstrated a TFT device having high breakdown voltage of 32 V and high drive current of 20 μA/μm at 5 V operations (4 μm gate length) [2]. This was achieved by using high-κ $LaAlO_3$ gate dielectric (κ=23) [9]-[11] instead of conventional TEOS oxide (κ=3.9): the high-κ gate dielectric can scale down the equivalent oxide thickness (EOT) to increase the drive current, where the thicker dielectric physical thickness increases the breakdown voltage significantly. In this chapter, we further reduce the V_{th} by integrating with low work-function Ytterbium (Yb) metal gate into LTPS TFTs, which has the lowest work function in Lanthanide [12]. The Yb/$LaAlO_3$ TFTs showed

good device integrity of low V_{th} of 0.85 V, a high gate-dielectric breakdown field of 6.25 MV/cm, high field-effect mobility of 31.4 cm^2/Vs, large on-off-state drive current ratio (I_{on}/I_{off}) of 1.63×10^6. The high breakdown voltage and high transistor drive current suggest that the Yb/$LaAlO_3$ TFTs can meet the device requirements for both pixel and display circuits. In addition, such low V_{th} device is especially important for future down-scaling trend of low power operation.

5.2 Experimental procedure

In this study, we first deposited the 100-nm amorphous Si on SiO_2/Si wafers using LPCVD at 550 ^oC. Then a 600^oC and 20 hour annealing in nitrogen ambient was used to crystallize the amorphous Si into poly-crystal. For device isolation and active area definition, a 500 nm thick oxide was deposited by PECVD followed by patterning and wet-chemical etching. The source-drain regions in active device region were implanted with phosphorus at 35 KeV and 5×10^{15} cm^{-2} dosage, followed by activation annealing at 600^oC for 12 hour annealing under nitrogen ambient. The 50-nm thick $LaAlO_3$ gate dielectric was then deposited on by sputtering from a ceramic source at condition of 150 W RF power and 30 sccm Ar flow rate, where the $LaAlO_3$ target is widely available and used as a superconductor substrate. To improve the gate oxide quality after sputter deposition, a 400^oC and 30 min furnace oxidation was applied using oxygen. Then the low work-function metal-gate was formed by

depositing 200 nm Yb by sputtering, gate patterning, electrode formation and 400^{o}C sintering for 30 min at nitrogen ambient.

5.3 Results and discussion

Fig. 5-1 shows the C-V hysteresis of 50 nm $LaAlO_3$ gate dielectric MOS capacitors. Small hysteresis less than 70 mV is observed after voltage sweeping between 5 V and -5 V, indicating the high-κ gate dielectric is high quality even processed at only 400^{o}C [13].

To further characterize the low temperature formed high-κ gate dielectric, fig. 5-2 shows the gate current density (J) as a function of electric field (E). A low leakage current of 1×10^{-5} A/cm^2 at 5 V and a high breakdown voltage of 31 V are obtained, which is high enough for high voltage operation to drive liquid crystal display. Such high breakdown voltage corresponds to an electric field of 6.2 MV/cm that is better than or comparable with LPCVD SiO_2 and PECVD TEOS oxide [4]-[5]. This is attributed to the higher bond enthalpy of high-κ $LaAlO_3$ than low temperature deposited SiO_2 or the plasma-free process with lower damage to high-κ gate dielectric.

The transistor I_d-V_g characteristics of Yb/$LaAlO_3$ TFTs are shown in Fig. 5-3. A low V_{th} of 0.85 V is obtained with a sub-threshold slope of 0.58 V/decade, which further gives a good electron field-effect mobility of 31.4 cm^2/Vs. The lower V_{th} is

due to both lower metal-work-function of Yb and large gate capacitance by using high–κ, from the relation of $V_{th}=\phi_m-\phi_s+Q_{total}/C_{dielectric}$. Such low V_{th} is very important to further improve the drive current and scale down the operation voltage for low power operation. In addition, large I_{on}/I_{off} ratio of 1.63×10^6 is measured for Yb/$LaAlO_3$ TFT even free from hydrogen passivation condition.

Fig. 5-4 shows the I_d-V_d characteristics of the Yb/$LaAlO_3$ TFT. A large drive current of 23 μA/μm is measured under 5 V that is the largest reported data for 4 μm gate length TFT using solid-phase furnace annealing crystallization. This large drive current is attractive for high-speed driver ICs, which is mainly due to the very high gate capacitance (3.9×10^{-7} F/cm^2 from C-V measurement) or alternatively small EOT of 8.7 nm [9]-[10]. The inherent merit of this high drive current high-κ TFT by using furnace crystallization is the good uniformity and large process window as compared with excimer-laser crystallization (ELC) [6]-[8]. The low work-function Yb metal gate also plays an important role to enhance the drive current- even a 9.2 μA/μm drive current is obtained at low 3 V operation using Yb gate.

The reliability of metal-gate/high-κ TFTs is an important issue. Fig. 5-5 shows the charge-trapping characteristics of the Yb/$LaAlO_3$ TFTs under constant-current stress from 0.1 to 10 mA/cm^2. The gate voltage shift is only 0.61 V even under 10 mA/cm^2 stress, which is significantly better than that in TEOS oxide TFTs (2.2 V shift)

under the same stress condition [14]. Therefore, the integration of Yb metal-gate on high-κ $LaAlO_3$ gate dielectric did not degrade the TFT device reliability.

We have summarized the important device parameters in Table 5.1. For comparison, the data from similar solid-phase crystallization but with different gate dielectric technologies or using poly-SiGe channel are also shown [4]-[5], [15] are also shown. The merits of this work are the higher drive current, lower V_{th}, good I_{on}/I_{off} and full process compatibility to current VLSI technology.

5.4 Conclusion

We have shown a high-performance Yb/$LaAlO_3$ LTPS TFT that provides good dielectric properties such as a high breakdown field, low leakage current and low charge trapping rate. These devices exhibit excellent electrical characteristics and high current drive, even without hydrogenation passivation or excimer laser crystallization process steps.

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Gate dielectric	$LaAlO_3$ 50 nm (8.7 nm EOT)	LPCVD SiO_2 80 nm [4]	PECVD TEOS oxide 60 nm [5]	Al_2O_3 50 nm [15]
Gate electrode	Yb	Poly-Si	Poly-Si	Poly-SiGe
V_{th} (V)	0.85	5.6	8.14	3
μ_{FE} (cm^2/Vs)	31.4	20	12.44	47
Sub-threshold slope (V/decade)	0.58	1.4	1.97	0.44
Drive current (μA/μm)	23 (W/L=100/4 @V_G=5V & V_D=5V)	1.4 (W/L=50/20 @V_G=20V & V_D=5V)	1.14 (W/L=50/10 @V_G=5V & V_D=5V)	6.2 (W/L=200/3 @V_G=5V & V_D=5V)
$I_D \times L_g/W_g$ (μA)	92 (@V_G=5V & V_D=5V)	28 (@V_G=20V & V_D=5V)	11.4 (@V_G=10V & V_D=5V)	18.6 (@V_G=5V & V_D=5V)
I_{on}/I_{off}	1.63×10^6	3.5×10^5	2.97×10^5	3×10^5

Table 5-1 Comparison of poly-Si TFTs formed by a furnace-crystallization with various gate dielectrics of $LaAlO_3$, Al_2O_3, LPCVD SiO_2, and PECVD TEOS oxides.

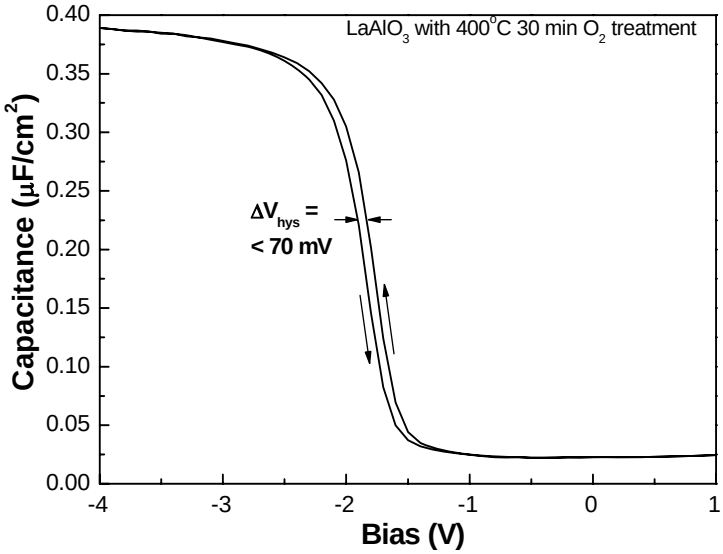

Fig. 5-1 *C-V* hysteresis of 50 nm $LaAlO_3$ gate dielectric with 400°C 30 min furnace O_2 treatment after sweeping between 5V and -5V. The ΔV_{hys} is smaller than 70 mV.

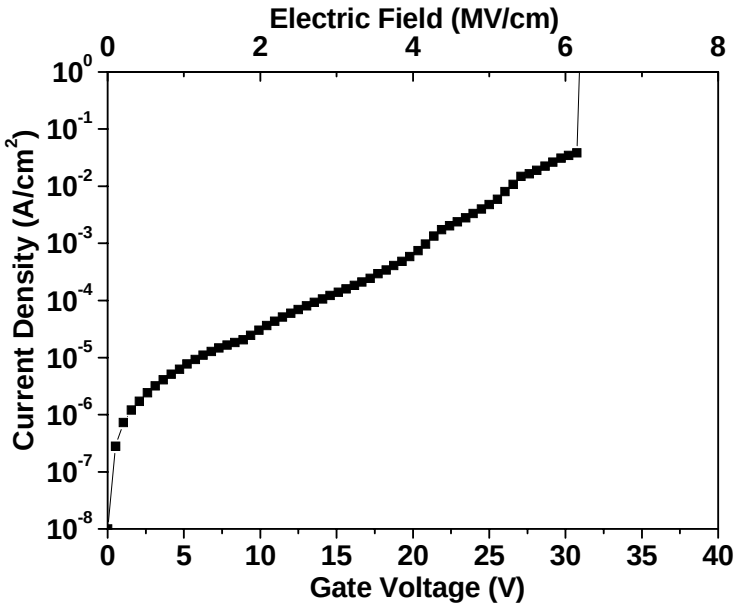

Fig. 5-2 The gate current density vs. electric field relation for $LaAlO_3$ gate dielectric poly-Si TFT.

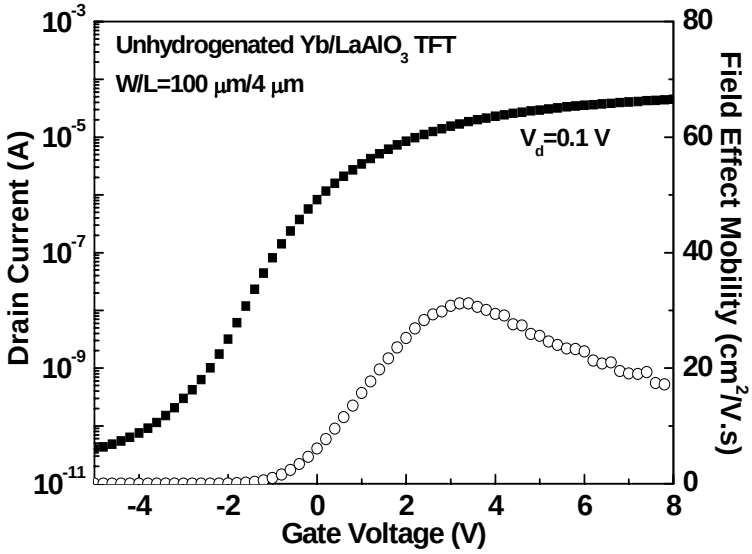

Fig. 5-3 The I_d-V_g characteristics of the Yb/$LaAlO_3$ poly-Si TFT measured at V_{ds} = 0.1 V.

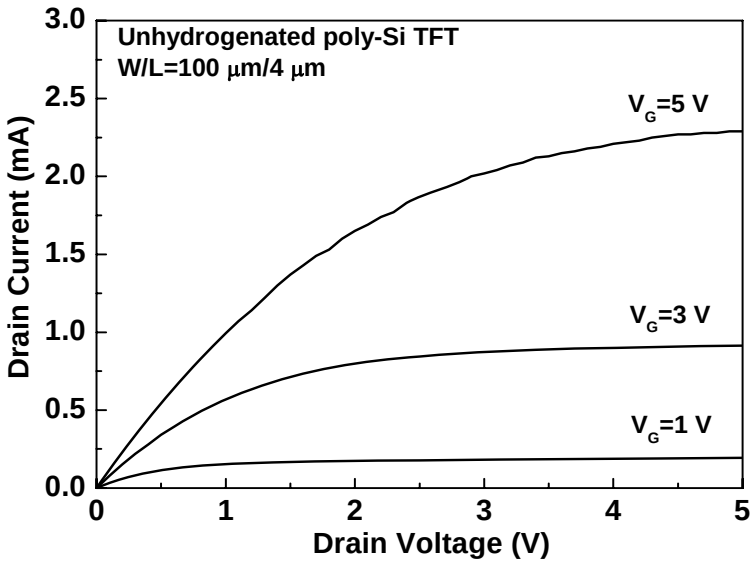

Fig. 5-4 The I_d-V_d characteristics of the Yb/$LaAlO_3$ poly-Si TFT.

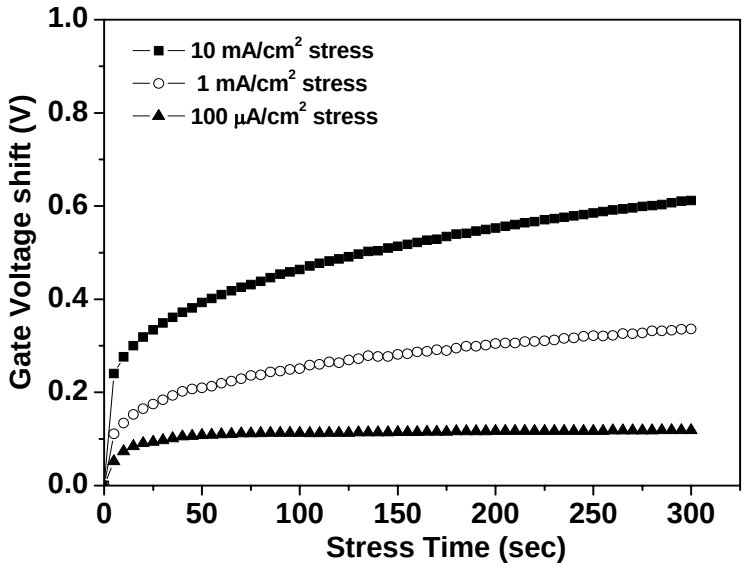

Fig. 5-5 The gate voltage shift of $Yb/LaAlO_3$ poly-Si TFT under constant-current stress of 100 μA/cm^2 to 10 mA/cm^2.

Chapter 6

Conclusions

In this dissertation, several high-κ dielectric materials and metal gate materials were studied for CMOSFETs applications. For p-MOSFETs, we have successfully demonstrated Ir_xSi/HfSiON transistors with good device characteristics. For n-MOSFETs, we have studied $HfSi_x$/HfSiON transistors and TaN/HfLaON transistors and also got excellent performance with additional merit of full process compatibility with VLSI fabrication lines. In addition, we have integrated a high-κ $LaAlO_3$ dielectric into low-temperature poly-Si TFTs and achieved good TFT performance. Finally, we have also achieved good RF performance for various passive devices on plastic substrates. Several important results are obtained and summarized as follows:

In chapter 2, a novel 1000°C-stable Ir_xSi gate on HfSiON is shown for the first time with full process compatibility to current VLSI fabrication lines and proper effective work function of 4.95 eV at 1.6 nm EOT. In addition, small threshold voltages and good hole mobilities are measured in Ir_xSi/HfSiON transistors. The 1000°C thermal stability above pure metal (900°C only) is due to the inserted 5nm amorphous Si, which also gives less Fermi-level pinning by the accumulated metallic full silicidation at the interface.

In chapter 3, we have developed a novel high temperature stable $HfSi_x$ gate for

high-κ HfSiON gate dielectric. After a 1000°C RTA, the $HfSi_x$/HfSiON devices showed an effective work function of 4.27 eV and a peak electron mobility of 216 cm^2/V-s at 1.6 nm EOT, with additional merit of a process compatible with current VLSI fabrication lines.

In chapter 4, we have studied the novel HfLaON gate dielectric with simple TaN metal gate, good device integrity of low gate leakage current, low $\phi_{m\text{-}eff}$ and high mobility has been obtained for n-MOSFETs. The preserved 1000°C amorphous state is similar to currently used SiO_2 or SiON, with additional merit of full process compatibility with VLSI fabrication lines.

In chapter 5, we have integrated low work function Yb metal gate combining with a high-κ $LaAlO_3$ dielectric into low-temperature poly-Si TFTs. Good TFT performance was achieved - such as a high drive current, low threshold voltage and sub-threshold slope, as well as an excellent on/off current ratio and high gate-dielectric breakdown field. This was achieved without hydrogen passivation or special crystallization steps. The good performance is related to the high gate capacitance density and small EOT provided by the high-κ dielectric.

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Publication lists:

(A) International Journal:

[1] C. H. Lai, **B. F. Hung**, A. Chin, W. J. Yoo, M. F. Li, C. Zhu, S. P. McAlister, and D. L. Kwong, "A Novel Program-erasable High-κ AlN Capacitor," *IEEE Electron Device Lett.* 26, no.3, pp. 148 - 150, 2005.

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(B) Conferences & Proceeding

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