國立交通大學

電子工程學系 電子研究所

博 士 論 文

先進材料應用於低溫複晶矽薄膜電晶體之研究

A Study of Low-Temperature Polycrystalline Silicon Thin Film Transistors Using Advanced Materials

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中華民國 九十七 年 十二 月

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摘要

在本論文中，我們利用了先進的高介電常數材料來製造高效能的低溫複晶矽薄膜電晶體。研究成果著重於探討利用新穎的分子氣相沉積(AVD)系統所成長出高介電薄膜的特性，並且利用此種新研發的薄膜來改善複晶矽薄膜電晶體的運作性能，最後並探討了這些高介電薄膜電晶體的可靠度。

首先，我們利用了一種新的分子氣相沉積系統來成長先進的高介電薄膜。在文章中，我們有系統地研究討論有關於各種參數對沉積薄膜的影響，其中包含了沉積溫度、腔體壓力、氧氣流量、注射頻率、以及薄膜成分調整等。而高溫的退火處理也被用來測試此高介電薄膜的熱穩定性。我們發現，要利用此種分子氣相沉積系統獲得高品質和化學當量比的高介電薄膜，較高的沉積溫度和充足的氧氣流量乃是必要的條件。在研究中，我們也發現擁有多晶結構的二氧化鉿(HfO_2)薄膜會導致較大的漏電流；相對地，矽酸鉿($HfSiO_x$)薄膜則表現出比較優異的熱穩定度，在高溫退火處理後仍維持其非晶狀態的結構。當然，較二氧化鉿薄膜低的介電常數，則為矽酸鉿薄膜的缺點。另外，具有較低介電常數的介面層自然形成於高介電薄膜和矽基板之間，將會導致等效氧化層厚度降低的問題。

接著，我們嘗試將此新開發的高介電薄膜應用在低溫複晶矽薄膜電晶體上。在這個部份，我們首先探討較厚高介電薄膜的結構和電性；接著，我們針對使用二氧化鉿和矽酸鉿薄膜當作閘極介電層的低溫 P 型通道複晶矽電晶體作一系列的研究和探討。我們發現因為高介電薄膜具有較大的閘極電容密度，因此以其作為閘極介電層的薄膜電晶體都展現出比使用傳統沉積氧化層的元件較佳的特性，例如較高的開關電流比、較低的次臨界擺幅、和較低的臨界電壓，除了稍高的關閉狀態的漏電流。其中，使用矽酸鉿薄膜當作閘極介電層的薄膜電晶體，其場效遷移率是使用沉積氧化層的電晶體的 1.76 倍；但是，使用二氧化鉿當作閘極介電層的元件卻表現出劣化的遷移率。最後，針對通道長度、通道寬度和元件特性的相關性也會在此被討論。

此外，我們更深入地研究有關二氧化鉿薄膜電晶體遷移率劣化的機制。我們討論了其他發生散射的原因，其中可能是存在於二氧化鉿薄膜中和二氧化鉿薄膜與多晶矽通道介面間的缺陷電荷、固定電荷、微弱聲子(soft Phonon)、和薄膜結晶化所造成的。我們也研討了有關使用高介電薄膜當作閘極介電層的複晶矽薄膜電晶體所引起的嚴重漏電流現象。我們認為高介電薄膜所產生的較高電場是引發嚴重的閘極誘發汲集漏電流(GIDL)的原因，而場發射電流為其主要的漏電流機制。緊接著，我們利用了變溫量測和負電壓溫度不穩定(NBTI)的應力量測方法來測試使用各種不同閘極介電層的薄膜電晶體的可靠度；很明顯地，高介電薄膜電晶體展現了相較於傳統使用沉積氧化矽的薄膜電晶體優異的溫度免疫能力。而在這些使用不同高介電薄膜的元件中，使用矽酸鉿薄膜的電晶體更展現出在負電壓溫度不穩定應力測試下較二氧化鉿薄膜電晶體優異的容忍度，其中包含了臨界電壓飄移、次臨界擺幅劣化、場效遷移率劣化、以及驅動電流衰退等測試項目。因此我們相信，相較於二氧化鉿薄膜，矽酸鉿薄膜將會是較佳的未來高性能複晶矽薄膜電晶體閘極介電層材料。

A Study of Low-Temperature Polycrystalline Silicon Thin Film Transistors Using Advanced Materials

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ABSTRACT

In this thesis, advanced high-κ materials were employed to fabricate high-performance low-temperature polycrystalline silicon thin film transistors (TFTs). Most of the efforts were focused on exploring the deposition of high-κ films by the new atomic-vapor deposition (AVD) system, improving the performance of the poly-Si TFTs with newly-developed high-κ films, and studying the reliability of these high-κ TFTs.

First of all, a new AVD system was employed for the deposition of the advanced high-κ materials. The impacts of deposition parameters, including the deposition temperature, chamber pressure, oxygen gas flow, injection frequency, and composition adjustment, were investigated systematically. The thermal stability of high-κ films was also tested by high temperature post-deposition annealing (PDA). It was found that higher deposition temperature and sufficient oxygen gas flow are essential to obtain the good quality and stoichiometric high-κ films by the AVD system. However, the large leakage current would be caused by the polycrystalline structure of HfO_2 films. In

contrast, $HfSiO_x$ films exhibit better thermal stability and retain the amorphous structure even after high temperature annealing. Certainly, the lower κ compared with HfO_2 film is the disadvantage of the $HfSiO_x$ films. Besides, the native interfacial layer with lower κ value always exists between the thin high-κ gate dielectric and Si substrate, which defeats the purpose of EOT lowering.

Next, we also tried to apply the newly-developed high-κ films to the low-temperature polycrystalline silicon (LTPS) TFTs. In this part, the structural and electrical properties of the thicker high-κ films were characterized first. Then, we performed a systematic study on the electrical properties of low-temperature-compatible p-channel poly-Si thin-film transistors (TFTs) using HfO_2 or $HfSiO_x$ high-κ gate dielectric. Because of their higher gate capacitance density, TFTs containing the high-κ gate dielectric exhibit superior device performance in terms of higher I_{on}/I_{off} current ratio, lower subthreshold swing (S.S.), and lower threshold voltage (V_{th}), relative to the conventional deposited-SiO_2 counterparts, albeit with slightly higher OFF-state current. TFTs incorporating $HfSiO_x$ as the gate dielectric has 1.76 times the field-effect mobility (μ_{FE}) relative to that of the deposited-SiO_2 TFTs. In contrast, the HfO_2-TFTs exhibit inferior mobility. The device performance dependence on the channel length and width of poly-Si TFTs was also discussed.

Furthermore, we also carefully investigated the mobility degradation mechanisms in these HfO_2-TFTs. We discussed possible origins of the additional scatterings, which might be attributed to the trapped charges, fixed charges, soft phonons, and crystallization in the HfO_2 films and HfO_2/poly-Si channel interface. Moreover, the higher leakage current of poly-Si TFTs using high-κ gate dielectrics was also studied. Aggravated gate-induced drain leakage (GIDL) current was thought to arise from the higher induced electric field by the introduction of high-κ films, and field-emission current would be the dominant leakage mechanism. In addition, the reliabilities of these

TFTs with different gate dielectrics were tested by the varying-temperature measurements and negative bias temperature instability (NBTI) stress. Obviously, the high-κ TFTs exhibit better temperature immunity over the conventional TFTs containing the deposited-SiO_2 film. In comparison with the devices using different high-κ gate dielectrics, the immunity of $HfSiO_x$-TFTs was better than that of HfO_2-TFTs—in terms of V_{th} shift, SS degradation, μ_{FE} degradation, and drive current deterioration—against NBTI stressing. Thus, we believe that $HfSiO_x$, rather than HfO_2, is a better candidate as the gate dielectric material for the future high-performance poly-Si TFTs.

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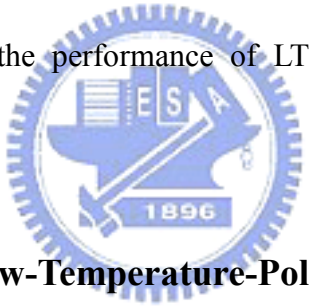
Chapter 1
Introduction

Low-temperature-polycrystalline-silicon (LTPS) thin-film-transistors (TFTs) have received much attention in recent years because of their increasing applications in active matrix displays (AMLCDs) [1.1]-[1.5], active matrix organic light emitting displays (AMOLEDs) [1.6]-[1.7], and memory devices [1.8]. Because of their better grain crystallinity, compared with the amorphous counterparts, higher carrier mobility and drive current can be achieved in poly-Si TFTs. The ability of fabricating high-performance LTPS TFTs enables their use in a wide range of new applications. Therefore, further improving the performance of LTPS TFTs is an interesting and important topic.



1-1 An Overview of Low-Temperature-Polycrystalline-Silicon (LTPS) Thin Film Transistors (TFTs)

The study of polycrystalline silicon (poly-Si) thin film transistors (TFTs) fabricated below a maximum temperature of 600°C commenced in the 1980s. The original motivation was to replace quartz substrate with low-cost glass for active matrix display applications. In the beginning, the a-Si:H (hydrogenated amorphous silicon) TFTs were applied as the pixel switching device in the first-generation active matrix liquid crystal displays (AMLCDs). The major advantages of a-Si:H TFT technology are low processing temperature compatible with large-area glass substrate and low leakage current due to the high off-state impedance. However, because of the lack of short range order, the low carrier field-effect mobility (typically below 1 $cm^2/(V\text{-}Sec)$) of a-Si:H TFTs limited their application to the switching elements only. Integration of driver

circuits with display panel on the same substrate is very desirable because of the cost reduction in the module and reliability improvement of the system. More recently, poly-Si TFTs are employed extensively in active-matrix liquid crystal displays because of their superior performance. The effective carrier mobility in poly-Si is significantly higher than that in a-Si, so the devices with reasonably high drive currents can be achieved in poly-Si TFTs [1.9]. The higher drive-current allows smaller TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance [1.10]. Previously, poly-Si TFT technology was primarily applied on small, high-definition LCD panels for projection display systems, however, the high processing temperature made it incompatible with commercial large-area glass substrates. With the rapid development of fabrication processes which are compatible with glass substrates in recent years, the manufacture of LTPS TFTs in AMLCDs on large-are substrates attracts more attentions. Modification of process procedure for enhancing TFT performance and reducing fabrication cost become an important issue in the fabrication of LTPS TFTs on large-area glass substrates.

Compared to the ultra-large scale integration (ULSI) process technology, the processes and device structures of LTPS TFTs are similar with metal-oxide-semiconductor field-effect-transistors (MOSFETs). The noticeable difference between LTPS TFTs and MOSFETs is that the former has to be performed at relatively low temperatures in order to be compatible with glass substrates. Due to this feature, only a-Si or poly-Si channels can be achieved on the glass substrate and the mobilities of a-Si and poly-Si are both much lower than that of c-Si (single-crystal silicon), which is widely used in conventional MOSFETs. Therefore, how to further increase the mobility of the low-temperature TFTs is one of the most important challenges. Among various process issues, the crystallization of a-Si thin films has been

considered to be the most important process for fabricating high-performance LTPS TFTs. The crystallized poly-Si thin films always serve as active layer (i.e., channel) in the poly-Si TFTs. As a result, the quality of crystallized poly-Si films profoundly affects the performance of the poly-Si TFTs. In polycrystalline materials, most of defects are present in the grain boundaries. Enlarging grain size by various crystallization methods, such as solid phase crystallization (SPC) [1.11], laser crystallization [1.12-1.13], and metal-induced crystallization (MILC) [1.14-1.16], can reduce the grain boundaries and effectively promote the quality of poly-Si. The performance of devices can be improved through the high-quality poly-Si formed by crystallization technologies.

Furthermore, other low-temperature process technologies of fabricating LTPS TFTs, such as gate dielectric formation, dopant activation, defect passivation, and device structures, are also essential for producing high-performance LTPS TFTs. Although many maturely developed fabrication processes in ULSI technology can be applied to LTPS TFTs technology, some high-temperature technologies, such as thermal oxidation and dopant activation, are not suitable for LTPS TFTs. Because of the thermal budget issue, the low-temperature oxide deposited by plasma-enhanced chemical vapor deposition (PECVD) system is widely applied in LTPS TFTs as the gate dielectric. The quality of the low-temperature deposited oxide is much worse than that of the thermal oxide used in MOSFETs. Therefore, a thicker low-temperature deposited-oxide is required to keep tight rein on the leakage current, which compromises the performance of LTPS TFTs. What kind of novel gate dielectric is appropriate for the next-generation LTPS TFTs is therefore a critical challenge.

1-2 Motivations for Improving Low-Temperature-Deposited Gate Dielectrics Used in LTPS TFTs

Although trap states in the poly-Si thin film serving as the device channel tend to

dominate electrical behavior of the poly-Si TFTs, the quality gate dielectric is also a critical issue for the performance and reliability of TFTs. Thin oxide films can be formed using physical vapor deposition (PVD) or chemical vapor deposition (CVD), and the latter is preferred due to its better step coverage and uniformity over large area substrate. Among various CVD methods, PECVD (plasma-enhanced chemical vapor deposition) has been the "de facto" choice for the gate oxide deposition in LTPS-TFT technology due to its low-temperature process and compatibility with large-area glass substrates. However, the low-temperature-deposited oxide used in LTPS TFTs always exhibits poorer physical and electrical quality, such as high interface trap density, high gate leakage and low breakdown field, compared with high-temperature thermal grown oxide used in VLSI MOSFETs. Consequently, thicker gate oxide has to be used to prevent the high gate leakage current.

Recently, the practicability of integrating the entire system on the panel (SOP) has been vigorously investigated [1.17]. In addition to cost reduction, integration of peripheral circuits can also reduce the weight of display module and increase panel reliability. This requires that the display driving circuits contain high-performance TFTs capable of operating at lower voltages while delivering higher drive currents. For the next-generation active-matrix displays with smaller size and higher resolution, scaling down of the gate oxide in poly-Si TFTs would be an essential issue to obtain the superior device performance. Although scaling down the gate oxide can increase the drive current of TFTs, it leads inevitably to a higher gate leakage current because of the decreased quality of the low-temperature-deposited gate dielectrics [1.18].

High-κ materials have attracted a lot of attentions in scaling MOSFETs technology in recent years. With the continuous scaling of CMOS technology for device performance improvement, the large gate leakage current due to the direct tunneling mechanism exceeds the specifications (i.e., 1 A/cm^2). To circumvent this critical

problem, high-κ materials such as hafnium-based, zirconium-based, and aluminum oxide have been introduced. The introduction of high-κ gate dielectrics can effectively reduce the tunneling leakage current due to its larger physical thickness under the same electrical thickness.

Other than the applications in MOSFETs, the high-κ materials also have been applied to LTPS TFTs. To maintain the physical dielectric thickness while increasing the gate capacitance, several new high-κ materials have been proposed, including Al_2O_3, Ta_2O_5, and HfO_2 [1.19–1.21]. Because Al_2O_3 films exhibit relatively low value of κ (around 7) and excess fixed charge, the TFT performance enhancement is only marginal [1.22]. The narrow band-gap of Ta_2O_5 means that a thicker film is necessary to reduce the gate leakage current of TFTs [1.23], which limits the increase in gate capacitance. Recently, hafnium dioxide (HfO_2) has been applied to TFTs because of its high value of κ (14–20) and sufficiently wide band-gap [1.24]. Although poly-Si TFTs incorporating HfO_2 as the gate dielectric exhibit superior performance in many respects, several issues remain problematic: e.g., the higher gate leakage current arising from poly-crystalline HfO_2 films and the degraded mobility arising from additional scattering. Therefore, the pursuit of an ideal high-κ material remains an important challenge for LTPS TFTs.

1-3 Organization of the Thesis

In this thesis, the advanced high-κ materials were employed to fabricate the high-performance low-temperature polycrystalline silicon thin film transistors.

In Chapter 2, a new AVD system, dedicated to the deposition of the advanced high-κ films, was introduced briefly. Afterwards, we focused on the study in which HfO_2 and $HfSiO_x$ films were deposited under different conditions using AVD system. Both structural and electrical characterizations of the high-κ films were presented. The effects of important deposition parameters, including the deposition temperature, the

chamber pressure, oxygen gas flow, deposition frequency, and the composition adjustment, on the physical properties of as-deposited thin films were examined. Then the thermal stability of the high-κ films was studied with the help of post-deposition annealing (PDA) at high temperature.

Due to the scaling limit of the thickness of the conventional low-temperature-deposited SiO_2 film, we tried to employ these newly-developed high-κ films to replace the conventional deposited-SiO_2 gate dielectric in the LTPS TFTs, as discussed in Chapter 3. Similar to the previous chapter, we presented both structural and electrical characterizations of the thick high-κ films prepared by AVD system, and employed HfO_2 and $HfSiO_x$ films as gate dielectrics to fabricate low-temperature-compatible p-channel poly-Si thin-film transistors. The systematic study of the electrical properties of these devices was then performed. Besides, the dependence of the electrical properties of high-κ TFTs on the channel length and width of the TFTs was also discussed.

Furthermore, the mechanisms of the mobility degradation, leakage current, and the reliability issues in these TFTs using different gate dielectrics were investigated in Chapter 4. The lower field-effect mobility caused by additional scatterings was found in the HfO_2-TFTs. In order to clarify the degradation mechanism of the poly-Si TFTs using HfO_2 gate dielectric, various possible origins of the mobility scatterings were analyzed and discussed in detail. Afterwards, the leakage current behaviors among the devices with different gate dielectrics were investigated. Although TFTs incorporating high-κ gate dielectrics exhibit better on-state electrical properties than conventional TFTs containing deposited-SiO_2, aggravated gate-induced drain leakage (GIDL) current was found clearly in TFTs using high-κ gate dielectrics. So, the leakage mechanism of poly-Si TFTs using high-κ gate dielectrics was addressed. Moreover, the reliability issues of these TFTs with different gate dielectrics were characterized by

varying-temperature tests and negative bias temperature instability (NBTI) stress. In the poly-Si TFTs, due to the poor thermal conductively of the glass substrate and high operation voltage, the NBTI effect was more important in the reliability issues. Due to the grain boundary in the channel regions and much severe gate induced drain leakage (GIDL) effect of poly-Si TFTs, the NBTI degradation mechanism in poly-Si TFTs could be different from that in MOSFETs. By measuring and analyzing the transfer characteristics before and after stressing for various stress times and temperatures, we determined the effects of NBTI on the poly-Si TFTs incorporating high-κ dielectrics.

Finally, conclusions as well as future prospects for further research were given in Chapter 5.

Chapter 2
Characterizations of High-κ Films Deposited by Atomic-Vapor deposition

2-1 Introduction

As the dimensions of complementary metal oxide semiconductor (CMOS) devices are scaled into the nanometer regime, the equivalent oxide thickness (EOT) of the gate dielectric decreases steadily to thinner than 1nm. Its leakage current under normal operation bias falls into the direct tunneling regime. For future generations of metal-oxide-semiconductor field-effect transistors (MOSFET), the current gate oxide layer (SiO_2 or SiO_xN_y) will need to be replaced with a new material possessing a higher dielectric constant (κ > 3.9). High-κ materials are employed to increase the physical thickness of the gate insulator while maintaining the same EOT and gate capacitance, thus reduces significantly the tunneling leakage current. Although many high-κ materials are proposed to replace silicon dioxide as gate insulator, HfO_2 is the most promising candidate for its excellent advantages, such as a suitable dielectric constant (~25) [2.1], high band-gap energy (~ 5.9eV), and suitable tunneling barrier height for both electron and hole (>1eV). However, HfO_2 is easily crystallized during deposition or following annealing processes, and crystallization increases the leakage current via grain boundaries. In order to improve the relatively low crystallization temperature of around 600°C of pure HfO_2 , alloying HfO_2 with Al_2O_3 and SiO_2 has been proposed[2.2]-[2.3]. Since their silicon or aluminum binary oxides, such as $HfSiO_x$ and $HfAlO_x$, retain an amorphous structure after high-temperature treatment, these binary oxides are now the most promising candidates to become the gate dielectric for

next-generation MOSFETs [2.4]-[2.8].

Recently, high-κ materials have been investigated using several deposition techniques including physical vapor deposition (PVD) [2.4], atomic layer deposition (ALD) [2.9], and pulsed laser deposition [2.10]. Although PVD is a simple technique for depositing new materials for evaluation in an academic organization, it may cause severe plasma damage to the electrical devices and is not preferred by industries because of poor step coverage and thickness uniformity. Chemical vapor deposition has the advantages of uniform thickness over large substrate areas and good conformal step coverage. In contrast to ALD, it is relatively easy to dope the HfO_2 using CVD, which may be necessary for future gate dielectrics.

In this chapter, we employed the new atomic-vapor deposition (AVD) system to deposit the high-κ films. The AVD system would be introduced briefly in section 2-2. Afterward, we focused on a study in which HfO_2 and $HfSiO_x$ films were deposited under different conditions using AVD system. We present both structural and electrical characterizations of the high-κ films. First of all, the deposition and evaluation of HfO_2 thin films have been performed in section 2-3. The effects of important deposition parameters, including the growth temperature, the chamber pressure and the gas flow of oxygen on the physical properties of as-deposited thin films have been examined. And then, the thermal stability of HfO_2 films would be tested by high temperature post-deposition annealing (PDA). In the second part, the Si incorporation into HfO_2 films was investigated and the results of $HfSiO_x$ films were discussed in section 2-4. The effects of the growth temperatures, the deposition frequencies and the composition adjustments on the physical and electrical properties of as-deposited thin films have been examined.

2-2 Overview of Atomic-Vapor Deposition (AVD) System

Figure 2-1 illustrates the schematic diagram of the AVD system. The main parts of the AVD system contain an AIXTRON horizontal reactor and a liquid-delivery TRIJET-TM vaporizer. Metal-organic precursors are used as the source of the high-κ film and kept at room temperature in liquid phase in a stainless tank. The precursor would be injected into the vaporizer via high-speed electro-mechanical valves and the injector plays the important role to control the injection amounts of the precursors. The injected amounts of the precursors can be controlled exactly by adjusting the injection numbers and opening time of individual injectors. In our experiment, the opening times of the injectors were all fixed at 0.8 msec. The injection periods and pulses can be adjusted to control the thickness and composition of the deposited films. The liquid precursor was injected to the vertical vaporizer and transferred from liquid type to gas type immediately. The temperature of vaporizer (160^{o}C and 170^{o}C in our experiment) could be adjusted according to the kind of precursors. Argon gas would be used as carrier gas to carry the vaporized precursor into the reactor through the showerhead. The process gas, oxygen in our experiment, would be heated first in gas-box and then mixed with vaporized precursors in the showerhead. Finally, the mixed gases flowed to the process reactor and film deposition would take place on the hot substrate. The deposition parameters, including deposition temperature, chamber pressure, oxygen gas flow, injection frequency and pulse numbers, could be fine-tuned to obtain the adaptable films in different device applications. Among all process parameters, the substrate temperature is the key issue to affect the quality of the as-deposited films.

2-3 Structural and Electrical Characterizations of HfO_2 Films

2-3.1 Experimental

HfO_2 films were deposited by liquid-injection atomic-vapor deposition (AVD) system and the liquid precursor was tetrakis(diethylamido)hafnium, $Hf[N(C_2H_5)_2]$,

which was dissolved in octane to make a 0.05 M solution. The evaporation temperature of vaporizer was 170^{o}C. Argon was used as the carrier gas, with a flow rate of 200 sccm, and oxygen as the oxidant, with a flow rate of 100 to 500 sccm. Substrate temperatures were in the range from 340^{o}C to 500^{o}C, and the chamber pressures were varied from 1.5 to 5mbar. Prior to the deposition, the 6-inch silicon substrates were treated with standard RCA clean. After the cleaning process, the HF-treatment was to immerse wafers into a 100:1 diluted HF solution and then spun dry without rinse in DI water. Subsequently, wafers were put immediately into AVD system for HfO_2 deposition to prevent the native oxide formation. The thickness of HfO_2 was controlled by the injection pulse numbers. The deposition rate was extracted by measuring the thickness of thick HfO_2 films with N&K analyzer. Because the system was designed for 200 mm wafers, the 150 mm wafers would be placed on a quartz adaptor and transferred to the process reactor. After film deposition, post-deposition annealing (PDA) was performed on all samples to investigate its impact on material properties and electrical characteristics of HfO_2 films. The fundamental physical properties of these films were analyzed by many techniques, such as grazing incidence x-ray diffraction spectrum (GI-XRD), x-ray photoelectron spectrum (XPS), transmission electron microscopy (TEM) and conductive atomic force microscopy (C-AFM). In addition, the electrical characteristics of the HfO_2 films were extracted from the capacitors and MOSFET devices. For electrical analysis, a precision impedance meter (Agilent 4284) was used for C-V measurements and a semiconductor parameter analyzer (Agilent 4156C) was used for I-V measurements.

2-3.2 Thickness Dependence of HfO_2 Films on Deposition Temperature

As mentioned above, the substrate temperature is the most important process parameter of as-deposited films by AVD system. The thickness of as-deposited HfO_2

films versus substrate temperature is shown in Figure 2-2. It can be seen clearly that the film thickness decreases monotonously as the substrate temperature increases. For conventional CVD systems, the deposition mechanisms could be divided into two regimes: Reaction-rate-limited regime at low temperature and mass-transport-limited regime at high temperature (Figure 2-3). The CVD mechanism, in which the growth rate decreases as the deposition temperature increases, is contrary to our experimental data. Possible reasons are described as follow: Firstly, although the liquid precursor was evaporated at the vaporizer, the vaporized precursor still contained a lot of organic elements. When the substrate temperature was higher, the precursor would be decomposed more quickly and completely during film deposition step. And then, the large amount of decomposed organic elements could not be pumped out immediately and retarded subsequent precursors to go to the surface. So the thinner films obtained at higher deposition temperature could be attributed to the reduced surface chemical reaction. Secondly, the supply of the precursor was discrete and limited in AVD system. The desorption and flow rate would increase at higher temperature due to the higher thermal energy. For this reason, the surface reaction time became shorter and the thinner deposited film would be obtained.

2-3.3 Structural Characterizations of HfO_2 Thin Films by XRD Analysis

Figure 2-4 shows the GI-XRD spectra of the HfO_2 films, which were deposited at various temperatures ranging from 340°C to 500°C. The chamber pressure and oxygen flow were fixed to 1.5 mbar and 500 sccm, respectively. For the samples deposited below 400°C, the intensities of the signals are extremely low. However, a bump at the position of around 57° has been clearly observed. We speculate that thin films deposited at the temperature below 400°C consist of diverse-oriented small granules, and the

bump is the convolution of these discrete signals of the granules. As a result, it is unlikely to exactly identify the structure of HfO_2 thin films with this broad and weak x-ray signal peak. The only thing can be confirmed is that films deposited at such low temperature range have poor crystallinity. This trend may imply that lower temperature will lead to the formation of amorphous structure. Concomitant with increasing temperature, more sharp peaks, which are identified to come from monoclinic crystal structure, become more visible. It means that thin film will undergo structural phase change and start to form monoclinic polycrystalline structures as the deposition temperature is higher than 460°C. The corresponding orientations in monoclinic structure are identified and shown by the labeled indices.

The effect of chamber pressure on the structure of thin films is demonstrated in Fig. 2-5. It is found that the crystallinity of the deposited film also strongly depends on the pressure conditions. Obviously, lower pressure results in better crystallinity for the samples grown at the same temperature. This is related to longer mean free path of reactive species in lower pressure ambient.

Figure 2-6 shows the XRD spectra of HfO_2 thin films deposited at 340^{o}C with various post-annealing conditions. The initial aim of depositing thin film at such low temperature of 340°C is to see if HfO_2 can retain its amorphous phase even after subjecting to higher thermal cycles in subsequent processes, for example, during annealing for activation of dopant impurities in S/D region. The advantages of amorphous thin films in the device applications are the lower leakage current, superior heterogeneous interface quality, blocking capability against impurity diffusion from poly-electrode. Rapid thermal annealing in N_2 ambient for 30s was employed to test the thermal stability of the deposited HfO_2 films. However, the HfO_2 film is not a good diffusion barrier for O atoms, HfO_2 film starts to crystallize as annealing temperature is above 650°C and the crystallinity of deposited films is enhanced by increasing RTA

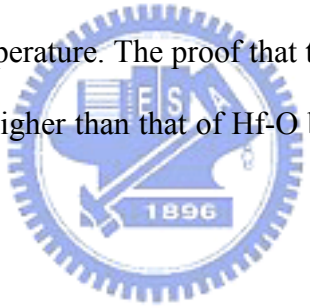
temperature, as shown by increasing signal intensity. These results show that the HfO_2 film will depict polycrystalline structure above 600°C, no matter at film deposition or subsequent high-temperature annealing.

2-3.4 Chemical Bonding and Composition of HfO_2 Thin Films by XPS Analysis

Chemical characterizations of HfO_2 films were accomplished by x-ray photoelectron spectroscopy (XPS) utilizing monochromatic and standard Al x-ray source. The results are shown in figure 2-7. Detected elements in thin films are hafnium (Hf), oxygen (O), and carbon (C). In order to avoid the undesirable carbon contamination on the sample surfaces, XPS analyses were also performed with ion milling. The low energy ion sputtering time is 15 sec, 3 min, and 8 min, respectively. Negligible damage by low energy ions during depth profiling could be assumed since no significant shift of the binding energies is observed. The relative contents of Hf, C, and O elements, which were determined by the spectra of the non-sputtering and 8min sputtering samples, are summarized in Table 2-1. It is found that the relative intensity of C_{1s} signals decreases drastically after sputtering. This result is reasonable due to the fact that all air-exposed materials will have a thin film deposition, composed primarily of hydroxide (i.e., alcohol-type, C-OH units). After removing this thin layer, the signals originating from purer HfO_2 can be obtained. Estimating from the data of 8-min sputtered samples, the content of C elements incorporated in the bulk of HfO_2 thin films during deposition process is only at the level of approximately 2.56%. This result strongly suggests that the decomposition of the employed Hf-precursor is very effective at 400°C. Therefore, the carbon atoms contained in the ligand can easily be evacuated. As a consequence, the concern of high level C incorporation using other Hf-precursors, such as alkoxdes and β-diketonates, doesn't apply to the use of the

tetrakis(diethylamido)-hafnium precursor. With such low C concentration level, thin films are be expected to have lower defect density, resulting in more robust thin films from the viewpoint of reliability.

Figure 2-8 shows Hf_{4f} and O_{1S} XPS spectra as a function of deposition temperature. The binding energy of Hf-O bond is nearly the same among all samples deposited at different temperatures. This result also means that the Hf precursor, $Hf[N(C_2H_5)_2]$, is easily decomposed above 360°C to form the HfO_2 films. Nevertheless, it can be seen clearly that the separation of the two peaks of Hf spectra, Hf $4f_{7/2}$ and Hf $4f_{5/2}$, becomes more apparent at higher deposition temperature. This phenomenon shows that the composition of HfO_2 becomes more stoichiometric at higher deposition temperature; in contrast, the impurities of the organic precursor are more easily incorporated into HfO_2 system at lower deposition temperature. The proof that the binding energy of Hf-O bond in a silicate film is about 1eV higher than that of Hf-O bond in a pure HfO_2 system will be given in section 2-4.



2-3.5 Structural Images of HfO_2 Thin Films by TEM Analysis

Figure 2-9 shows the images of plane-view TEM for (a) the HfO_2 sample deposited at 400°C and the samples with subsequent (b) 600°C, (c) 800°C, (d) 1000°C post-deposition annealing for 30sec in N_2 ambient, respectively. There are obviously two contrast regions in all the samples: dark and bright regions; with the dark areas embedded in the bright regions. At first glance, the spherical-shaped dark regions would be easily recognized as polycrystalline grains. However, only a few of them in as-deposited sample show crystalline diffraction patterns. This poor crystallinity has been evidenced by broad x-ray peaks, which become sharper concomitant with enhancing growth temperature. The contrast is supposed to be caused by the different compositions. Dark region is more likely to be produced by Hf-rich composition while

bright zone is more close to stoichiometric composition, which are identified by TEM energy-dispersive spectroscopy (EDS). Table 2-2 lists the element ratios of O and Hf in dark and bright regions separately. The preciseness depends on the beam size. However, this table reveals important information of the composition of HfO_2 thin films. This compositional inhomogeneity is hypothesized to be caused by the insufficient Hf atom surface migration due to its large mass and insufficient oxygen gas flow during the film depositions.

With 600°C annealing, it is observed that many grains start to crystallize while the change of the film structure in bright regions can hardly be detected. Noteworthy, there is dramatic structural alternation taking place around the grain boundary. High temperature annealing produces significant structural modification along the grain boundaries. The presence of the seam between the grains and adjacent regions is supposed to be the primary cause of tremendous leakage current increase, compared with as-deposited samples. After annealing at 800°C, the situation is very different from that in 600°C. The crack along the original grain boundary disappears. Instead, the crystalline patterns with diverse orientations could be seen almost everywhere in both dark and bright regions. As annealing temperature goes up to 1000°C, it is found that the grain starts to merge with each other and the size of a single grain substantially increases as a result of high temperature annealing. This structural re-arrangement reduces the number of the grain and grain boundary.

Figure 2-10 shows the images of cross-sectional TEM for (a) the HfO_2 sample deposited at 400°C and the samples with subsequent (b) 600°C, (c) 800°C, and (d) 1000°C post-deposition annealing for 30sec in N_2 ambient, respectively. The contrast is not only observed in plane-view TEM but also in cross-sectional TEM pictures. The lighter contrast is near the Si/film interface. This interfacial layer is thought to be a Si-rich Hf silicate according to many previous reports, even though this speculation can

be hardly identified by any compositional analysis method. The total physical thickness, the individual thickness of HfO_2 films and interfacial layer are plotted in Fig. 2-11. After 600°C annealing, total physical thickness of thin film is increased by 10 Å. Interestingly, most of the thickness increase, approximately 8.5 Å, occurs on the upper layer. Meanwhile, the increase in thickness for interfacial layer is only slightly larger than 1 Å. This result obviously contradicts with the previous report, which stated high temperature annealing would lead to significant increase in thickness of interfacial layer. It is hypothesized that the as-deposited thin films content more Hf than expected. In other words, it is Hf-rich as revealed by the huge dark area portion in plane-view TEM picture. In rapid thermal annealing process, there exists residual moisture, which would react with the excess Hf violently and contributes to the growth of additional upper layer. Once the excess Hf atoms are consumed, the oxygen would diffuse through metal oxide and interfacial layer and react with underlying silicon substrate. It can be confirmed by the fact the thickness of upper layer doesn't change with further enhanced annealing temperature. Meanwhile, the interfacial layer experiences nearly 10 Å increase after 1000^{o}C PDA treatment. With the combination effects of reduced grain-boundaries (shown in plane-view TEM images) and increased thickness of interfacial layer, a lot of leakage paths are eliminated and leakage current is also decreased significantly, which are supported by following results of conductive-AFM images. Nevertheless, the EOT of high-κ films also increases unexpectedly which is related to the interfacial layer with lower κ value. In fact, the κ values still increase as the PDA temperature increases (the κ value of interfacial layer is assumed to be 5) and close to the idea HfO_2 dielectric value (~25) due to the improved film quality. The characterizations of the as-deposited HfO_2 film and the samples after PDA treatments are summarized in Table 2-3.

2-3.6 Structure Changes of HfO_2 Thin Films by Conductive AFM Analysis

Figure 2-12 shows the images of conductive AFM(C-AFM) for (a) the HfO_2 sample deposited at 400°C and with subsequent (b) 600°C (c) 800°C (d) 1000°C post-deposition annealing for 30sec in N_2 ambient, respectively. The contrast represents the relative magnitude of the leakage current; the brighter the region, the larger the leakage current. The darkest region denotes zero current flow, which means the leakage current is too small to be detected by C-AFM system. The scanning area is approximately 800×800 nm^2. The parameters are summarized in Table 2-4. In general, the as-deposited thin film exhibits the lowest average leakage current. However, there are still many bright spots in its C-AFM image, shown in Fig. 2-12(a). The presences of bright dots strongly indicate the leakage current is a localized behavior. From the results of AFM, this characteristic doesn't correlate with the surface condition of the thin film since only minor difference of roughness exists among all samples. Among the annealed samples, the 600°C-annealed sample shows the largest average leakage current. The mean leakage current decreases with increasing annealing temperature up to 1000°C. The trend is consistent with the previous TEM results. Crystallization of HfO_2 films would take place after high-temperature annealing and result in larger leakage, but the increased interfacial layer would suppress the leakage current.

2-3.7 Electrical Properties of HfO_2 Thin Films

The capacitors were fabricated on p-type (100)-oriented silicon wafers with 8~10 Ω-cm nominal resistivity. After RCA clean, the HF-treatment was to immerse wafers into a 100:1 diluted HF solution and then spun dry without rinse in DI water. Subsequently, wafers were put immediately into AVD system for HfO_2 depositions and the thickness of the deposited HfO_2 films was set to around 6 nm. After film deposition,

post-deposition annealing (PDA) was performed on all samples to investigate its impact on electrical characteristics of HfO_2 films. Next, the top gate electrode was formed in an e-beam evaporating system through a shadow mask. After top gate electrode deposition, another 500nm-thick Al metal was deposited at wafer backside as backside-electrode to ensure good conductive contact to measurement system. Finally, the post-metal annealing (PMA) by furnace at 400°C for 30 min in N_2 ambient was executed to complete the fabrication.

Figures 2-13(a) & (b) exhibit Capacitance-Voltage (C-V) and leakage current density-voltage (J-V) curves of HfO_2 thin films deposited at different substrate temperatures. It can be seen clearly that the C-V curve of the sample deposited at 345°C depicts the hump behavior and flat-band voltage (V_{FB}) shift. As mentioned before, the organic elements are difficult to be decomposed completely at these low deposition temperature and insufficient oxygen gas flow. So we believe that the worse C-V result is caused by the residual impurity inside the low-temperature deposited films. By increasing the deposition temperature to 400°C, the C-V curve exhibits the normal behavior. This hypothesis is also supported by the characteristic of J-V curve, as shown in Fig. 2-13(b). From the XRD analysis, the HfO_2 films deposited at 345°C exhibits the amorphous structure and should have a smaller leakage current than the partial-crystallized HfO_2 films deposited at 400°C. However, the sample deposited at lower temperature depicts worse J-V characteristics than the sample deposited at 400°C. Therefore, we speculate that the quality of the lower-temperature-deposited HfO_2 films is poor due to the residual impurity.

Figure 2-14 exhibits C-V curves of HfO_2 thin films deposited at 500°C with different oxygen gas flow. The data show that the C-V curve of the sample with lower oxygen gas flow is distorted due to higher leakage current (1.03E-5 A/cm^2 at -1V, as shown in Fig. 2-15(b)). From the above results, the higher leakage current in HfO_2 films

deposited at lower substrate temperature may originate from the residual organic impurity. Nevertheless, for samples deposited at higher deposition temperature, the origin of the higher leakage current may be caused by the Hf-rich composition and worse interface on HF-last base related to the insufficient oxygen gas flow. We try to deposit HfO_2 thin films with stoichiometric composition by increasing the oxygen gas flow. We also flow the oxygen gas and Hf precursor at the same time to passivate the interface. From Figure 2-14, normal C-V behavior for the sample with higher oxygen gas flow can be seen clearly and this result is also consistent with the lower leakage current (6.23E-8 A/cm^2 at -1V, as shown in Fig. 2-15(b)).

Next, the effects of PDA treatments are shown in Figure 2-15. Obviously, the sample with higher oxygen gas flow exhibits two orders of magnitude lower in leakage current, compared with the sample with 300 sccm oxygen gas flow, however, both samples depict a similar trend, i.e., the leakage current increases slightly as the PDA temperature increases and then decreases dramatically after 1000^{o}C annealing. This phenomenon has been discussed previously, and is believed to be due to the crystallization of HfO_2 films that takes place after high-temperature annealing, resulting in larger leakage, despite the simultaneous increase of the interfacial layer that tends to suppress the leakage current. The thicker interfacial layer also increases the EOT due to its lower κ value.

2-3.8 Characteristics of MOSFETs Using HfO_2 Gate Dielectrics

For the test run, PMOSFETs with ultra-thin HfO_2 gate dielectric were fabricated firstly. After LOCOS isolation and active area definition, HfO_2 gate dielectrics with calculated thickness of around 6nm were deposited by AVD system after standard RCA clean. The deposition temperature, chamber pressure, and oxygen flow of the HfO_2 thin film was 400°C, 1.5 mbar, O_2=300 sccm, respectively. Then, a 200nm thick undoped

poly-Si film was deposited, and BF_2 was implanted by an energy of 10keV, followed by source/drain junction formation. All samples were then annealed at 1050°C to active the dopant using rapid thermal annealing (RTA) in N_2 ambient for 10 sec. After passivation layer deposition, contact hole formation, Al metallization and patterning, the forming gas annealing at 400°C was finally performed for 30 min. In addition, another NMOSFETs device run with 4nm HfO_2 gate dielectrics using different precursor, $Hf[OC(CH_3)_3]_2(mmp)_2$, was fabricated later for comparisons. This precursor was pre-tested already by AIXTRON Company and recommended for its fewer amount of residual impurity. Similar with our previous discussions, the higher substrate temperature (500°C) and larger oxygen gas flow (1700 sccm) are also essential for this precursor to form high quality deposited thin films.

Typical transfer characteristics of the devices from both runs are shown in Figure 2-16(a) and (b), respectively. For the first test run, the high-κ MOSFET was successfully fabricated, but the device performance was inferior to the conventional device with 2.5nm SiO_2 gate dielectric, as shown in Fig. 2-16(a). This result could be explained by the following reasons: Firstly, the non-optimum process parameters for high-κ thin film deposition, including lower deposition temperature (400°C) and insufficient oxygen gas flows (300sccm), could be the major factor for poor device performance. Secondly, the interfacial layer between high-κ/Si substrate interface would become thicker after high temperature dopant activation and degrade the device performance. As the quality of the high-κ thin film is improved, better device performance is clearly seen in Fig. 2-16(b). However, the performance of high-κ devices is still degraded by the increasing interfacial layer after high temperature annealing. Therefore, the parameters of high-κ thin films deposition has to be optimized and the surface treatment, such as chemical oxide or NH_3 passivation, has to be applied to obtain the optimum device performance in the nano-scale devices.

2-3.9 Summaries of Characteristics of HfO_2 Films

We had discussed the effect of various process parameters and analyzed the deposited HfO_2 films through the material analysis and electrical measurements. In conclusion, firstly, a high deposition temperature and sufficient process gas flow are very important for the deposition of high quality HfO_2 films. Nevertheless, the polycrystalline structure of the HfO_2 films will be formed naturally at higher deposition temperature or after high temperature annealing. Secondly, the surface treatments are essential to improve the high-κ/Si substrate interface and decrease the interfacial layer formation to obtain the lower EOT in MOSFET applications.

2-4 Structural and Electrical Characterizations of $HfSiO_x$ Films

2-4.1 Experimental

Now we focus on the deposition and evaluation of $HfSiO_x$ thin films using $Hf[OC(CH_3)_3]_2(mmp)_2$ and $Si[OC(CH_3)_3]_2(mmp)_2$ precursors. In this section, we replace the original Hf-precursor ($Hf[N(C_2H_5)_2]$) with $Hf[OC(CH_3)_3]_2(mmp)_2$, because this commended precursor decomposes more effective and the as-deposited films contain fewer amounts of the residual impurity. First of all, the effects of growth temperature, deposition frequency and composition adjustment on the physical properties of as-deposited $HfSiO_x$ films were examined. $HfSiO_x$ films were deposited by liquid-injection atomic vapor deposition (AVD) and the liquid precursors were $Hf[OC(CH_3)_3]_2(mmp)_2$ and $Si[OC(CH_3)_3]_2(mmp)_2$ respectively; both are dissolved in octane to make a 0.05M solution. Form the reference process parameters for HfO_2 thin films deposition (deposition temperature= 500^oC, chamber pressure= 9 mbar, O_2 gas flow= 1700 sccm, injection frequency= 0.2 Hz), pre-tested by AIXTRON company, the set of parameters for $HfSiO_x$ film deposition in our experiment was determined as:

deposition temperature= 550°C, chamber pressure= 9 mbar, oxygen gas flow= 2000 sccm, and the deposition frequency= 0.1 Hz. We fixed the injected number to 100 pulses in this experiment. It is well known that the Si precursor usually needs higher processing temperature for the film deposition. Therefore, the higher substrate temperature, larger oxygen gas flow, and fewer amounts of injected precursors are beneficial in producing high quality $HfSiO_x$ films because the precursors can decompose and react more completely. In order to have a more detailed surveillance over the influence of stoichiometric ratio on the properties of thin films, deposition temperature series (range from 550 to 350°C), injection frequency series (range from 0.1 to 3Hz), and the composition series (Hf/Si ratio= 1/1, 2/1, 1/2, 2/0) were executed separately.

After film deposition, post-deposition annealing (PDA) was also performed on all samples to investigate its impact on material properties and electrical characteristics of $HfSiO_x$ films. The fundamental physical properties of thin films were analyzed by many techniques, such as x-ray photoelectron spectrum (XPS), Auger electron spectroscopy (AES), grazing incidence x-ray diffraction spectrum (GI-XRD), and transmission electron microscopy (TEM). Furthermore, the electrical properties of $HfSiO_x$ thin films were also extracted from the capacitors with MIS structure. For electrical analysis, a precision impedance meter of model Agilent 4284 was used for C-V measurements and a semiconductor parameter analyzer of model Agilent 4156C was used for I-V measurements.

2-4.2 Thickness Dependence of Different Parameters (Deposition Temperature, Injection Frequency, Film Composition) on $HfSiO_x$ Films

Figures 2-17(a)-(c) show the thickness and deviation variations of the deposited

$HfSiO_x$ films for deposition temperature series, injection frequency series, and composition series, respectively. In Figure 2-17(a), it is found that the deposition rate of $HfSiO_x$ films is nearly constant with the condition of deposition rate 1.2 Å/pulse and temperature above 450°C, but decreases abruptly as the temperature is below 450°C. As mentioned above, the Si precursor needs higher deposition temperature to complete chemical reaction. Therefore, the reason that the deposited film becomes thinner as the substrate temperature goes down can be attributed to the fact that the deposition temperature is too low to complete chemical reaction. Most of Si precursor is un-reacted and pumped away. Next, the relationships between thickness and deviation variations versus injection frequency are shown in Fig. 2-17(b). The deposition rate is around 1.1~1.3 Å/pulse for all testing frequencies but the standard deviation becomes larger as the injection frequency goes up to 3 Hz. This result may be caused by incomplete decomposition arsing from too much precursors within one time unit and the uniformity of deposition thickness is degraded. Finally, the composition series of $HfSiO_x$ film was executed. For the composition adjustments, we kept the maximum deposition time (0.1 Hz * 100 pulses= 1000 sec) constant, and set different injection frequency of individual precursor to change the composition of the as-deposited $HfSiO_x$ films. The results are shown in Fig. 2-17(c). The highest deposition rate, 1.3 Å/pulse, is obtained by the $HfSiO_x$ film with Hf/Si ratio equal to 1:1. When the Hf/Si ratio is changed to 2:1 or 1:2, the deposition rate decreases to around 0.8 Å/pulse. The pure hafnium oxide exhibits the lowest deposition rate of 0.6 Å/pulse, due to the lowest amount of the injected precursor.

2-4.3 Chemical Bonding and Composition of $HfSiO_x$ Thin Films by XPS Analysis

Chemical characterizations of $HfSiO_x$ films were accomplished by x-ray

photoelectron spectroscopy (XPS) utilizing monochromatic and standard Al x-ray source. Figures 2-18 to 2-20 show the spectra of Hf_{4f}, Si_{2p}, and O_{1s} as a function of Hf/Si composition ratios. From Figure 2-18 of Hf_{4f}, we found that pure hafnium oxide shows two clearly separated peaks and becomes broader as the concentration of Si increases. These broad peaks are caused by additional created-peaks when the concentration of Si increases. The binding energy of Hf-O bond monotonically increases with increasing concentration of Si. It means that more and more Si-O bonds are formed as the Si ratio increases, so the peak shifts to the higher binding energy. The same trends have been seen in the binding energy spectra of Si_{2p} and O_{1s} states, shown in Figures 2-19 and 2-20. Typical values of the binding energy of Si_{2p} and O_{1s} states are around 103.2 eV and 532.8 eV for silicon dioxides, respectively. As the amount of Si increases, the peaks of Si_{2p} shift from 101.9 eV to 102.7 eV and the peaks of O1s shift from 530.3 eV to 532.2 eV. These shifts mean that oxygen prefers to bind with Si than Hf, so more and more Si-O bonds are formed. One strong peak and one weak peak located at 98.2 eV are found in pure HfO_2 and $HfSiO_x$ (Hf/Si=1/2) films. These are Si peaks coming from Si substrate in XPS measurements due to the thinner films of these two samples.

Figures 2-21 to 2-23 show the spectra of Hf_{4f}, Si_{2p}, and O_{1s} of $HfSiO_x$ films with Hf/Si ratio (1/1) deposited at 500°C and subjected to different PDA treatments. In comparison with the HfO_2 films, the $HfSiO_x$ films exhibit better thermal stability even after 900°C PDA treatments for 30 seconds in N_2 ambient. The spectra of Hf_{4f}, Si_{2p}, and O_{1s} of $HfSiO_x$ films are nearly the same for these as-deposited, 800°C-PDA and 900°C-PDA samples. But the small shift and two separate peaks of Hf_{4f} are found in the sample after 1000°C PDA treatment. The peak of Si_{2p} also shifts from 102.5eV to 103.2eV, closer to the peak of SiO_2. Fig. 2-23 shows the broaden peak of O_{1s} of the $HfSiO_x$ film after 1000°C PDA treatment, which means that additional peaks are formed

after this high temperature annealing. From these results, we believe that the $HfSiO_x$ films with Hf/Si ratio (1/1) deposited at 500°C would segregate to Hf-rich $HfSiO_x$ films and SiO_x films after 1000°C PDA treatment for 30 seconds in N_2 ambient.

The quantitative analysis by XPS measurement of composition series and PDA series of $HfSiO_x$ films can be seen in Figures 2-24 and 2-25, respectively. As the injected pulses of Si increase, the amount of Si in $HfSiO_x$ films also increases. But the resultant atomic percentage of Hf and Si seems not to be determined solely by the injected pulses, as shown in Fig. 2-24. The results show that Si atoms are more active to incorporate into the $HfSiO_x$ films than Hf atoms, and Si-rich $HfSiO_x$ films are more easily formed. Figure 2-25 displays the composition variation versus PDA temperature, the total amounts of Si and Hf is kept nearly constant for the as-deposited $HfSiO_x$ films with Hf/Si ratio (1/1) after PDA treatments. After 1000°C PDA treatment, the amount of Si increases slightly and this phenomenon is caused by Si out-diffusion from Si substrate at this high annealing temperature. This result is also consistent with our XPS spectra described above. Nevertheless, the $HfSiO_x$ films retain amorphous structure and exhibit better thermal stability than HfO_2 films after high temperature annealing, which is beneficial for device applications.

2-4.4 Depth Profiles of $HfSiO_x$ Films by AES Analysis

The depth profiles analyzed by AES analysis of as-deposited $HfSiO_x$ film with Hf/Si ratio (1/1) deposited at 500°C and subjecting to different PDA treatments are shown in Figures 2-26(a)-(d). First of all, the profiles look similar among all analyzed samples: Hf atoms decrease rapidly in $HfSiO_x$/Si interface, however, more Si atoms pile up at the interface. The distributions of Hf and Si do not seem to be uniform across the films. Secondly, the total sputtering time increases as the PDA temperatures rise up but the total physical thickness of these films measured by n&k analyzer is nearly the same.

We believe these results are probably due to the densification of $HfSiO_x$ films after high-temperature PDA treatments. Although some difference in profile is found in XPS analysis for samples with 1000°C annealing, no clear difference could be seen in AES analysis between as-deposited and annealing samples.

2-4.5 Structural Characterizations of $HfSiO_x$ Thin Films by XRD Analysis

Figure 2-27 shows GI-XRD spectra of $HfSiO_x$ thin films with Hf/Si ratio (1/1) deposited at 500°C and subjecting to different PDA treatments. A strong signal at the position of around 33° is clearly observed. We speculate this peak corresponds to the Si double diffraction from Si substrate. For the spectra of these measured samples, we didn't find any signal besides substrate signal. We believe that the $HfSiO_x$ films deposited with these parameters exhibit amorphous structures even after 1000°C PDA treatments, which is preferred from the viewpoint of suppressing leakage current and better thermal stability during device fabrications, compared with HfO_2 films.

2-4.6 Structural Images of $HfSiO_x$ Thin Films by TEM Analysis

Figure 2-28 shows the images of cross-sectional TEM for the as-deposited $HfSiO_x$ film with Hf/Si ratio (1/1) deposited at 500°C on Si substrate with native oxide. This sample was deposited for thickness correction with the data measured by n&k analyzer without any clean step, so the thicker interfacial layer is related to the native oxide. The uniform film and amorphous structure can be seen in this figure, which are consistent with the XRD results. The TEM-EDX data confirm that the as-deposited thin film is in fact composed by Hf, Si and O elements, as shown in Figure 2-29.

2-4.7 Electrical Properties of $HfSiO_x$ Thin Films

To evaluate the electrical properties of $HfSiO_x$ thin films, a simple capacitor structure with the configuration of Pt/5nm $HfSiO_x$/Si-substrate/Al was fabricated. The top Pt electrode was formed by E-Gun system onto the as-deposited and annealed $HfSiO_x$ films through shadow-mask process to produce the circle diode with an area of $3.5x10^{-4}$ cm^2. Figure 2-30(a) exhibits the high frequency (100K Hz) C-V characteristics of 5nm $HfSiO_x$ thin films with Hf/Si ratio (1/1) deposited at 500°C and 1050°C PDA treatment for 10 seconds in N_2 ambient. The as-deposited film shows larger capacitance density (C/A) than PDA samples. But the larger hystersis values (~50mV), large flat-band voltage (V_{FB}) shift and worse interface characteristics of as-deposited film also can be found in Fig. 2-30(a). The quality of films could be improved after PDA treatments with the elimination of hystersis and sharp C-V curve. However, the capacitance density also reduces after the high-temperature treatment. We believe that the lower C/A value is related to the thicker interfacial layer formed after high temperature annealing, as mentioned in the behavior of HfO_2 films. The lower leakage current density of the sample after 1050°C PDA treatment is apparently related to the thicker interfacial layer, which can be seen in Fig. 2-30(b).

The high frequency (100K Hz) C-V and I-V characteristics of 5nm $HfSiO_x$ thin films with Hf/Si ratio (1/1) deposited at different temperatures are shown in Figures 2-31(a) and (b). Higher deposition temperature of as-grown films results in higher C/A value and lower leakage current density, except for the sample deposited at 400°C. We believe this is because the films deposited at higher temperature exhibit better chemical combination of Hf, Si and O atoms and fewer amount of residue carbon. The denser films deposited at higher temperature result in higher κ value and lower leakage current density. The film deposited at 400°C shows different trend with the other samples, with the highest C/A value and the worst leakage current density. This phenomenon, also mentioned in the thickness dependence and XPS results, is because the process

temperature of 400°C is too low to form $HfSiO_x$ films, so pure HfO_2 films is formed at 400°C, which has higher dielectric permittivity but inferior leakage current behavior. In Figure 2-32, the split deposited at 450°C exhibits large positive V_{FB} shift, compared with the split deposited at 400°C, and then V_{FB} shifts back to the lower value for the splits deposited at higher temperatures. The large V_{FB} difference between the films deposited at 400°C and 450°C is attributed to the different deposited films, HfO_2 (400°C) and $HfSiO_x$ (450°C). As the deposition temperature is above 450°C, $HfSiO_x$ films can be formed by AVD system and the quality of the deposited films becomes better as the deposition temperature increases, so V_{FB} shifts back due to the reduced fixed charges. Figure 2-33 exhibits the relationship between EOT and leakage current density at -3V. Consistent with the above results, HfO_2 films (400°C) has lower EOT related to higher dielectric constant but inferior leakage current related to the poly-crystalline structure. As the deposition temperature rises, $HfSiO_x$ films are formed and the quality of as-deposited films becomes better at higher deposition temperature. Consequently, the EOT and leakage current density both decreases as the deposition temperature increases.

High frequency (100K Hz) C-V and I-V characteristics of 5nm $HfSiO_x$ thin films deposited at 500°C with different Hf/Si ratio are shown in Figures 2-34(a) and (b). Higher capacitance density and hump behavior are found in the sample with Hf/Si ratio of 2/1. Although more Hf element in the $HfSiO_x$ film results in higher dielectric constant, higher trap density is also introduced into the deposited films simultaneously. As the amount of Si increases, the C/A value drops due to reduced dielectric constant. However, the hump behavior is also eliminated in the sample with Hf/Si ratio of 1/1. In Figure 2-34(b), the sample with Hf/Si ratio of 2/1 shows higher leakage current density as expected due to the higher trap density, compared with the sample with Hf/Si ratio of 1/1.

2-4.8 Summaries of Characteristics of $HfSiO_x$ Films

In this section, we have discussed the effect of various process parameters and analyzed the deposited $HfSiO_x$ films through the material analysis and electrical measurements. In conclusion, $HfSiO_x$ films with amorphous structure were deposited successfully by AVD system and the composition of $HfSiO_x$ films could be adjusted by controlling the injected pulses of Hf and Si precursors. Higher deposition temperature, compared with the HfO_2 films, is necessary in order to achieve good quality of the $HfSiO_x$ films. Although the Si-rich $HfSiO_x$ films exhibit lower dielectric constant than HfO_2 film, better thermal stability and lower leakage current density is achieved.

2-5 Summary

In this chapter, the advanced high-κ films, including HfO_2 and $HfSiO_x$ materials, were deposited successfully by the new AVD system. The effects of process parameters, such as deposition temperature, chamber pressure, oxygen gas flow, injection frequency, and composition adjustment were discussed in detail. The structural characterizations and electrical properties of these high-κ films were extracted by various material analyses and electrical measurements. In summary, higher deposition temperature and sufficient oxygen gas flows are essential to obtain the high quality high-κ films by AVD system. However, large leakage current inherent in the polycrystalline structure is observed in HfO_2 films. In contrast, the $HfSiO_x$ films exhibit better thermal stability and still retain the amorphous structure even after high temperature annealing. Certainly, the lower κ compared to the HfO_2 film was the disadvantage of the $HfSiO_x$ films. Besides, the unexpected interfacial layer with lower κ value always exists between the thin high-κ gate dielectric and Si substrate. For advanced MOSFET applications, surface treatments have to be done to suppress the interfacial layer growth, and lower EOT value could be achieved by using these high-κ films.

Table 2-1

Relative contents of Hf, C and O elements of as-deposited HfO_2 films. The deposition temperature, chamber pressure and oxygen flow are 400°C, 1.5 mbar, and 300sccm, respectively.

	Hf	**O**	**C**
Non-sputtering	23.88%	45.66%	30.46%
Sputtering 8min.	28.55%	68.89%	2.56%

Table 2-2

Compositions of HfO_2 films inside and outside the grain region

Condition (element)	**O**	**Si**	**Hf**	**Hf/O**
As-deposited (inside grain)	11. 9%	74.1%	14.0%	1.18
As-deposited (outside grain)	14.0%	75.3%	10.7%	0.77

Table 2-3

Summary of thickness, dielectric constant, EOT for the sample deposited at 400°C with and without post annealing.

	Physical thickness (Å) (TEM)	***Thickness of HfO_2/interfacial layer (Å)***	***EOT (Å)***	***Dielectric Constant (κ) (HfO_2/ interfacial layer)***
As-deposited	51.1	32.5/18.6	31.3	7.5/5.0
600°C annealing	61.7	41.7/20	29.4	11.8/5.0
800°C annealing	64.8	42.9/21.9	29.4	13.6/5.0
1000°C annealing	72.7	41.8/30.9	33.7	17.0/5.0

Table 2-4

Parameters of topographic AFM and conductive AFM for as-deposited HfO_2 film and those subjected to post-deposition annealing at 600°C -1000°C in N_2 ambient for 30sec. The deposition temperature, chamber pressure and oxygen flow are 400°C, 1.5mbar, and 300sccm, respectively.

Condition	**As-deposited**	**600°C**	**800°C**	**1000°C**
Surface roughness (nm)	0.16	0.13	0.14	0.13
$\mathbf{I_{peak\text{-}to\text{-}peak}}$	13.3 pA	52.6 pA	18.7 pA	0.4 pA
Mean value of $\mathbf{I_{leak}}$	0 pA	0.33 pA	0.25 pA	0.22 pA

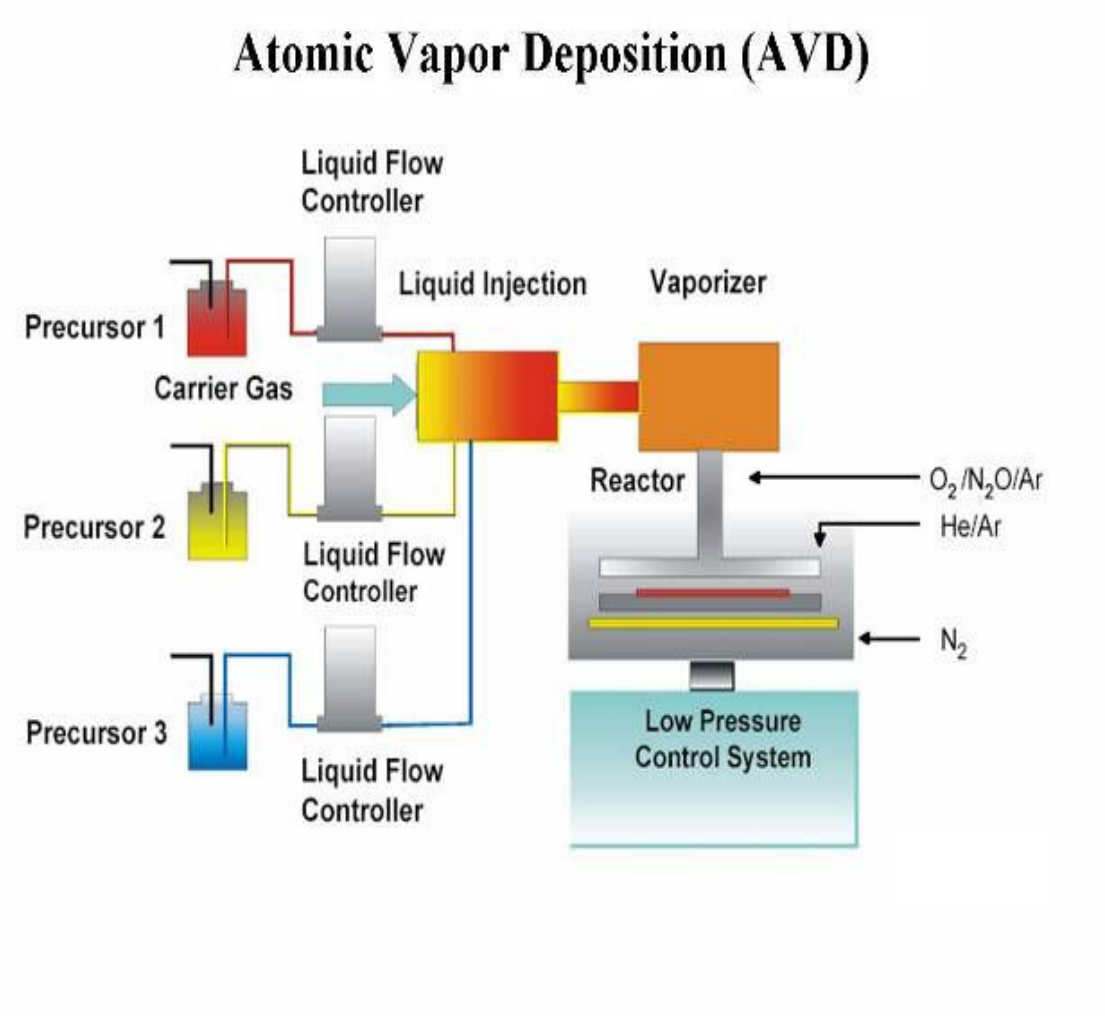


Figure 2-1 Schematic diagram of atomic-vapor deposition (AVD) system.

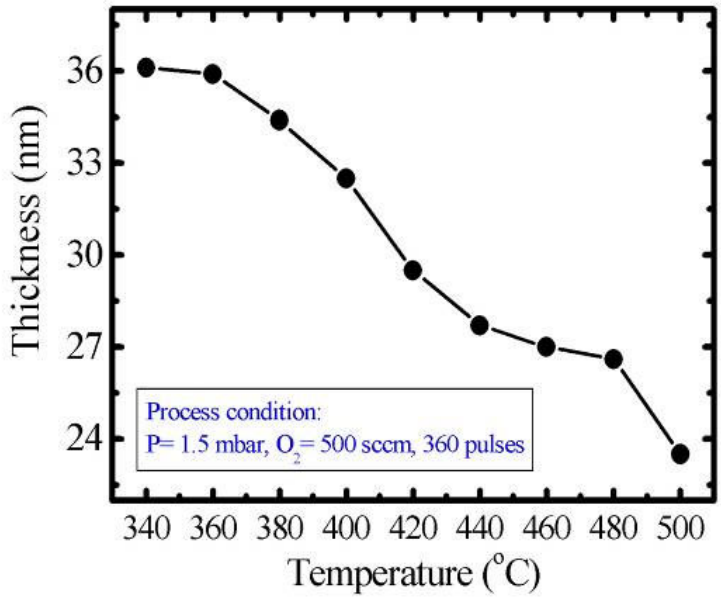


Figure 2-2 Temperature dependence of the thickness of HfO_2 films.

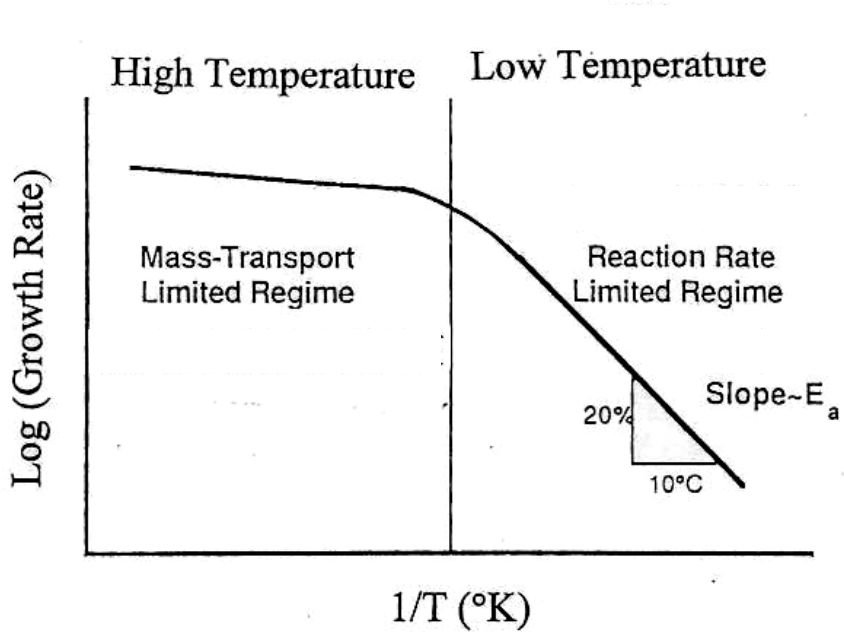


Figure 2-3 Temperature dependence of the growth rate of the CVD films.

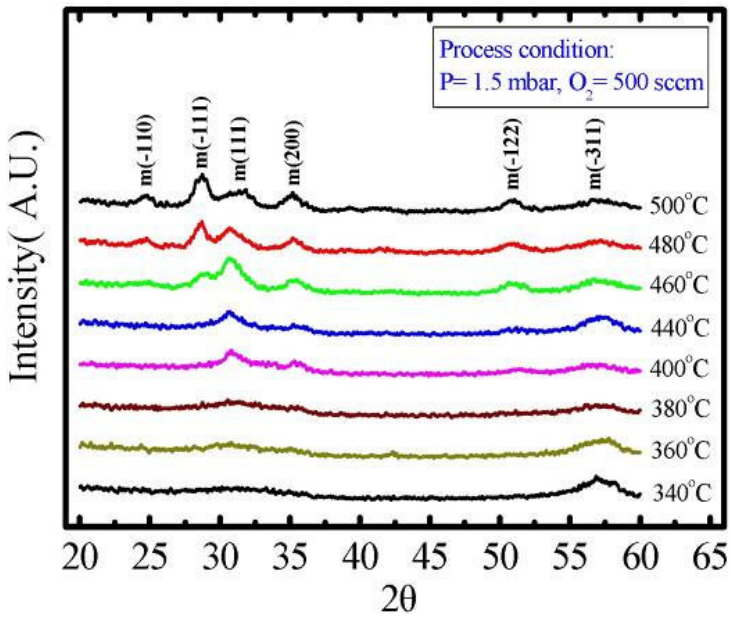


Figure 2-4 XRD spectra of as-deposited HfO_2 films at various process temperatures. The chamber pressure is 1.5mbar and oxygen flow is 500sccm.

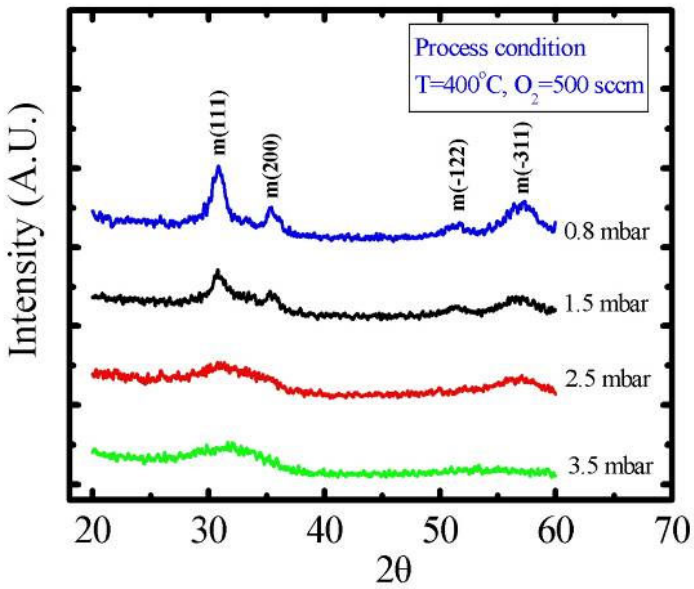


Figure 2-5 XRD spectra of as-deposited HfO_2 films at various chamber pressures. The temperature is 400°C and oxygen flow is 500sccm.

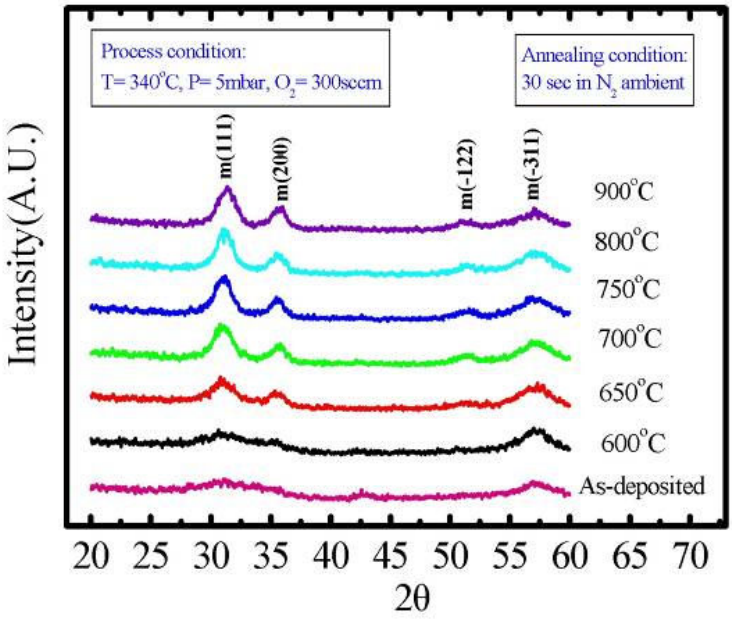


Figure 2-6 XRD spectra of HfO_2 films deposited at 340°C with different post-annealing temperatures, in N_2 ambient, 30seconds.The chamber pressure is 5mbar and oxygen flow is 300sccm.

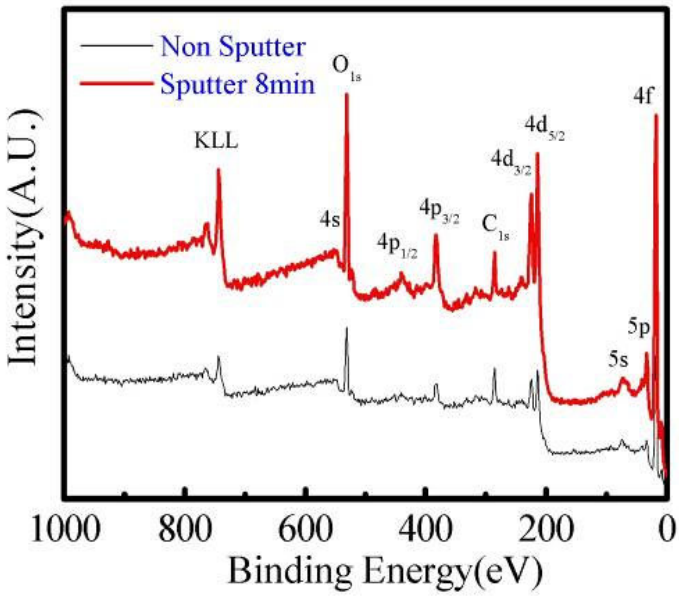
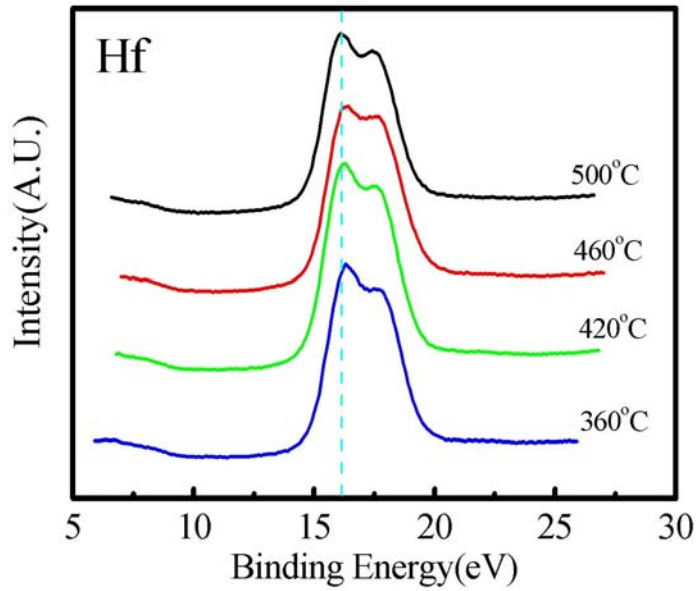
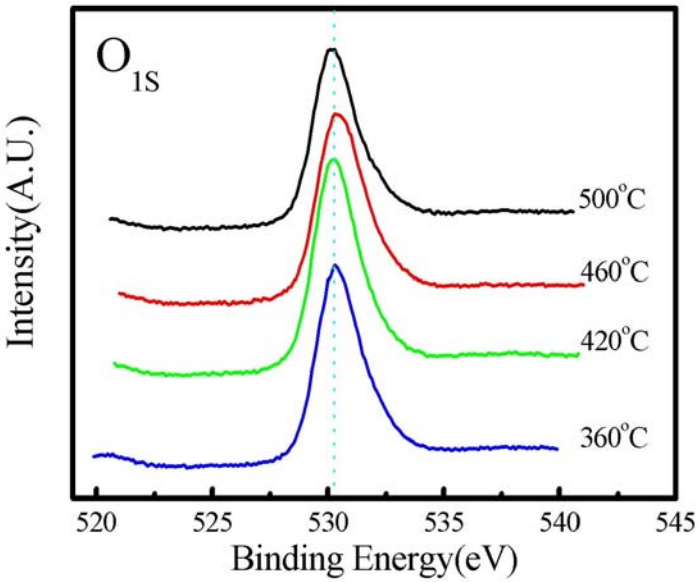


Figure 2-7 XPS spectra of as-deposited HfO_2 thin films. The deposition temperature, chamber pressure and oxygen flow are 400°C, 1.5mbar, and 500sccm, respectively.



(a)



(b)

Figure 2-8 XPS data of (a) Hf $_{4f}$ spectra, and (b) O_{1s} spectra for HfO_2 films deposited at various temperatures. The thickness is around 30nm.

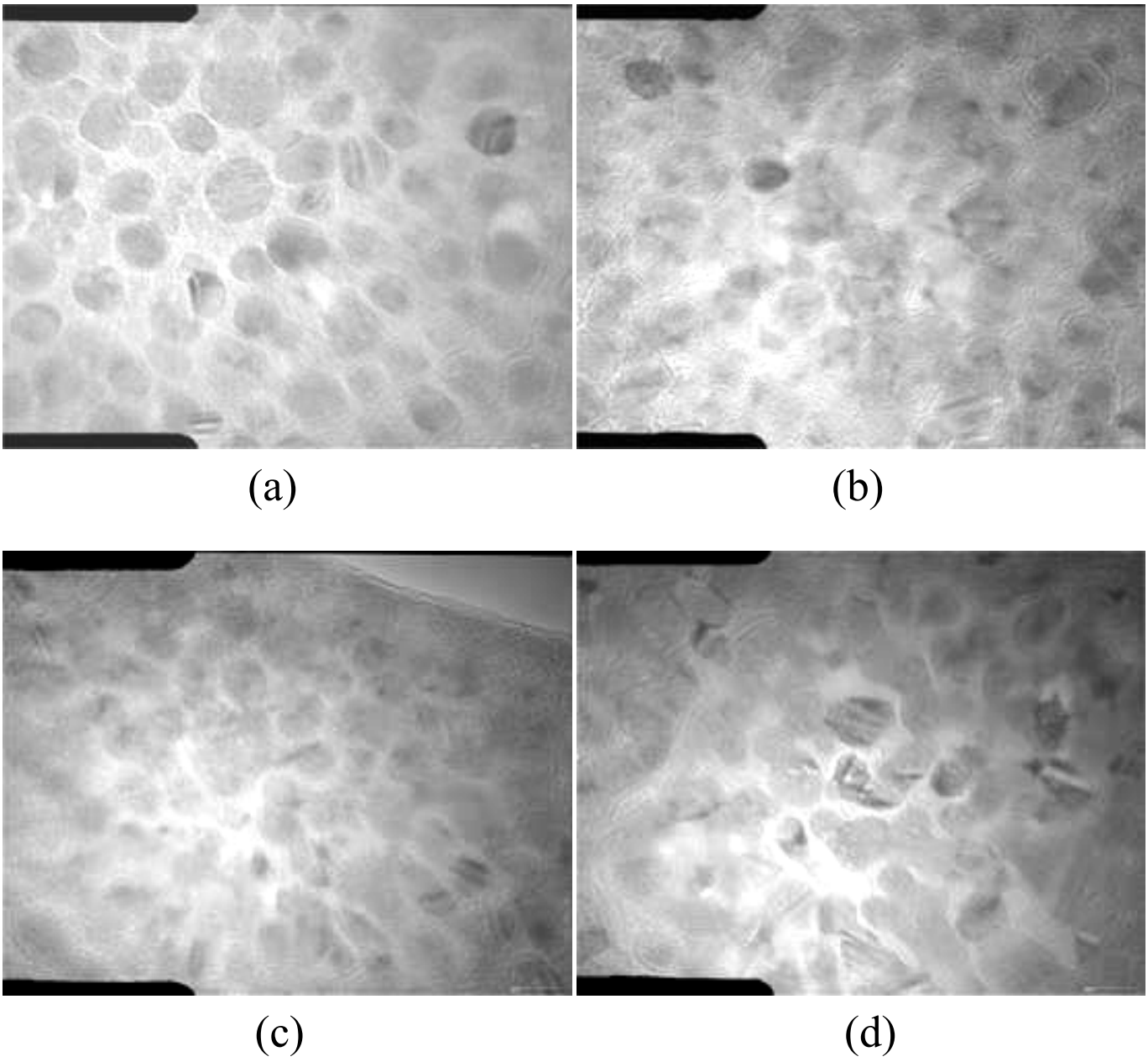


Figure 2-9 Plane-view TEM images of (a) as-deposited thin film and those subjected to (b) 600°C, (c) 800°C, (d) 1000°C post-deposition annealing in N_2 ambient for 30sec. The deposition temperature, chamber pressure and oxygen flow are 400°C, 1.5mbar, and 300sccm, respectively.

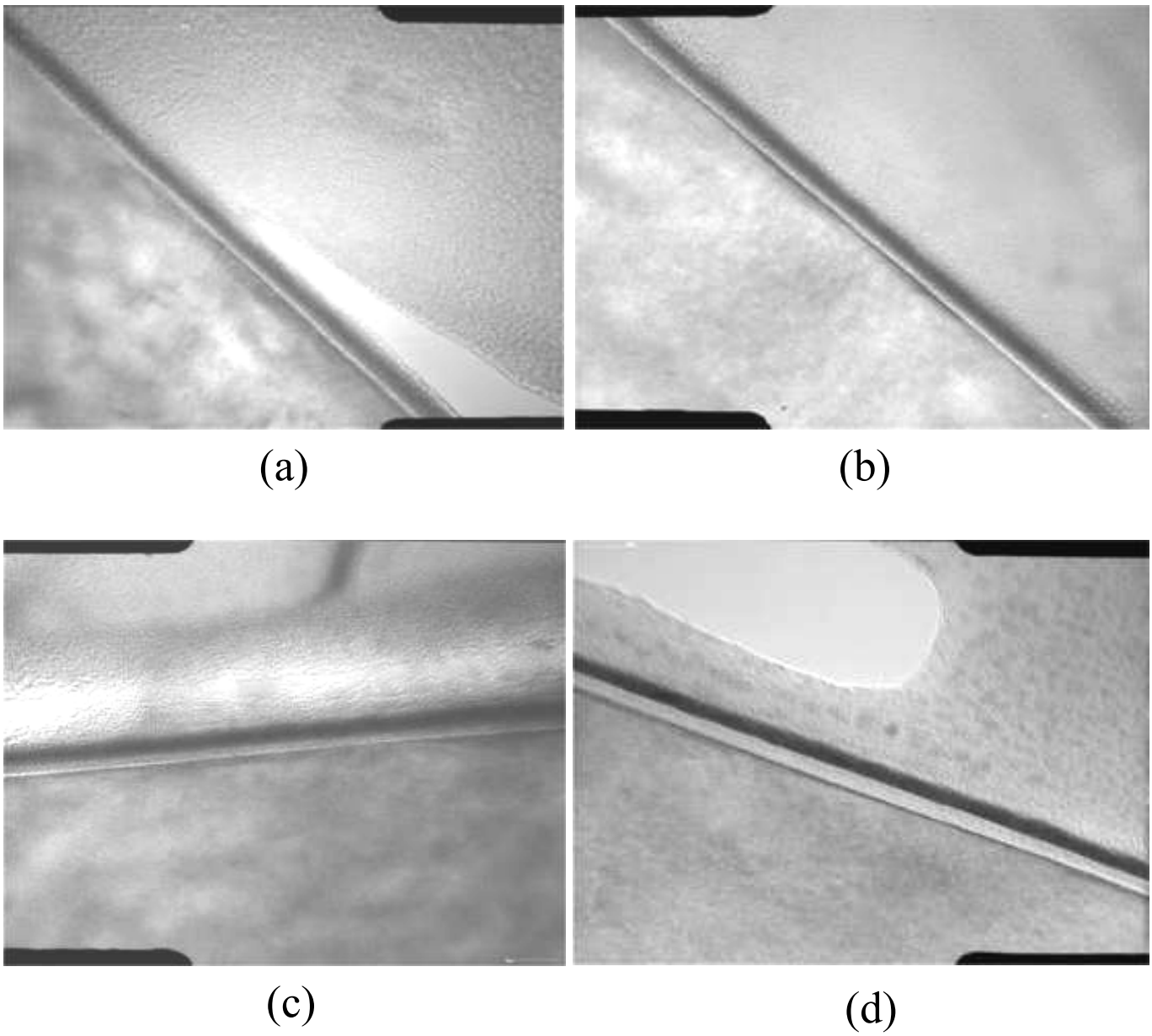


Figure 2-10 Cross-sectional TEM images of (a) as-deposited thin film and those subjected to (b) 600°C, (c) 800°C, (d) 1000°C post-deposition annealing in N_2 ambient for 30sec. The deposition temperature, chamber pressure and oxygen flow are 400°C, 1.5mbar, and 300sccm, respectively.

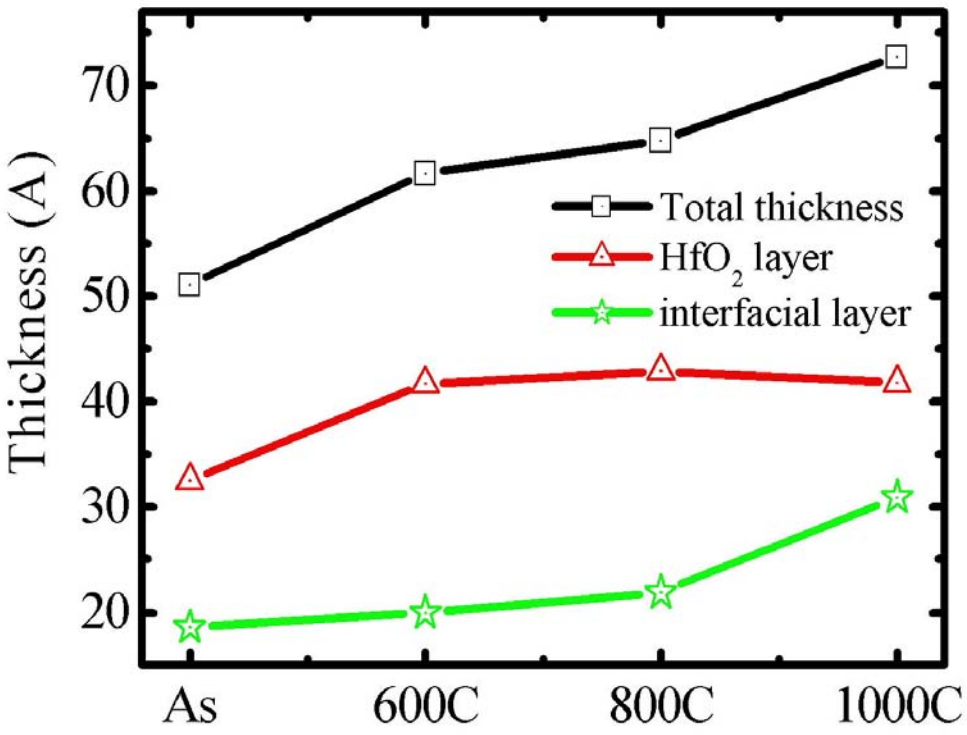


Figure 2-11 Thickness versus PDA temperature of individual layers.

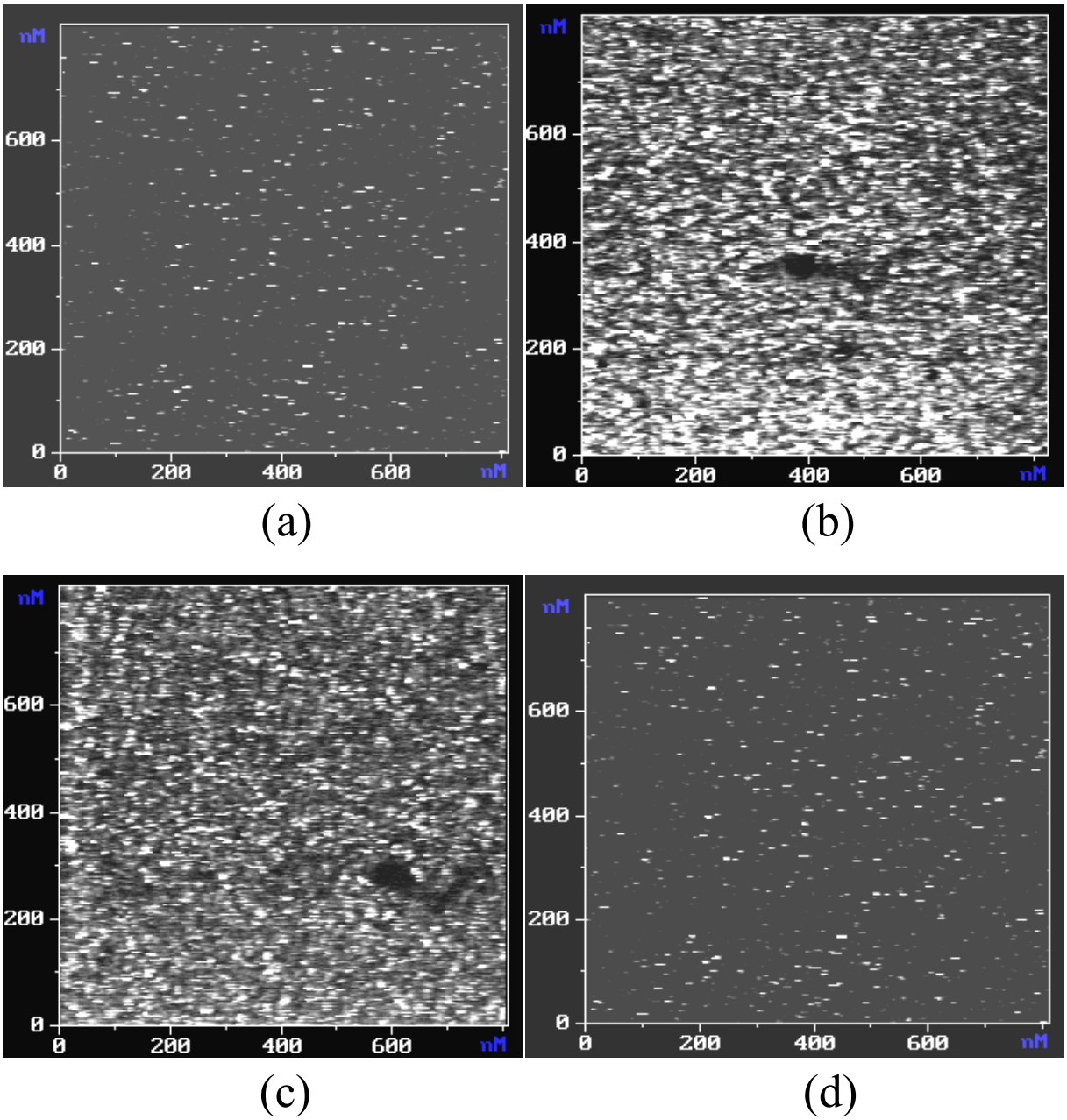


Figure 2-12 The images of conductive-AFM of (a) as-deposited thin film and those subjected to (b) 600°C, (c) 800°C, (d) 1000°C post-deposition annealing in N_2 ambient for 30sec. The deposition temperature, chamber pressure and oxygen flow are 400°C, 1.5mbar, and 300sccm, respectively.

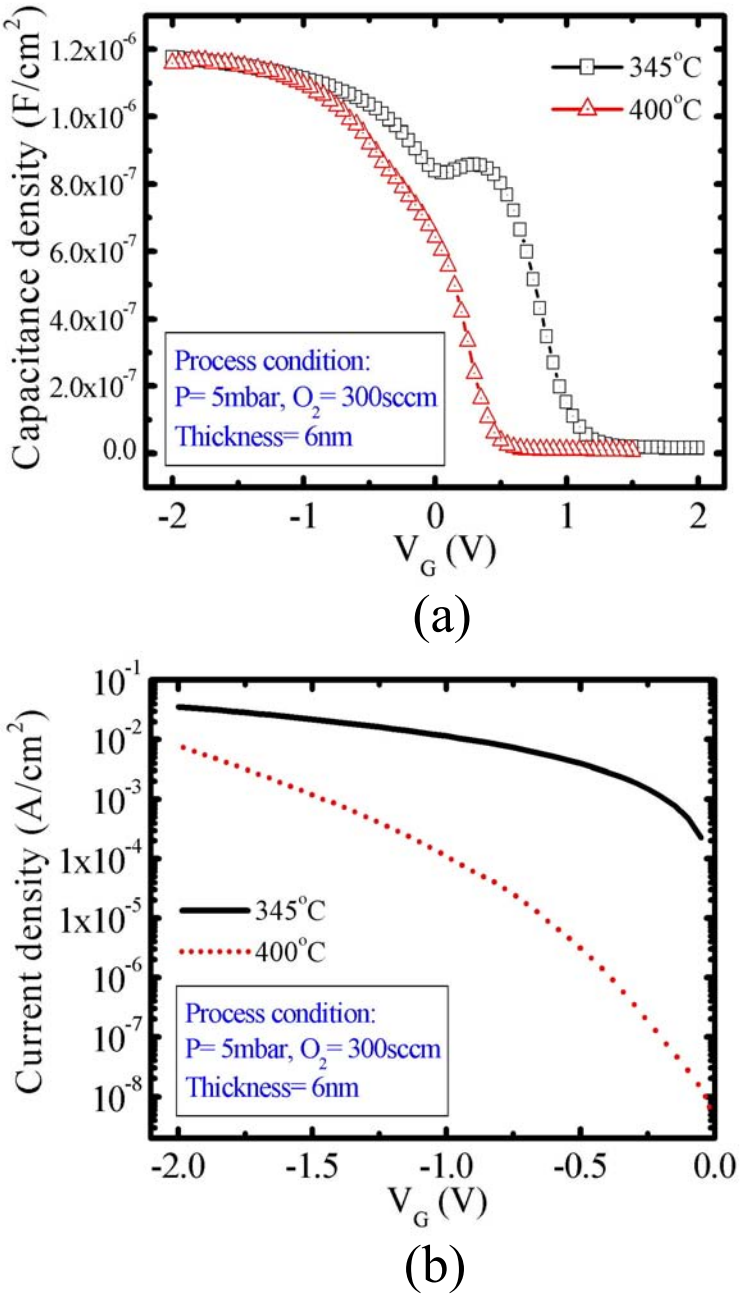


Figure 2-13 (a) C-V and (b) J-V characteristics of the HfO_2 films deposited at different substrate temperature on HF-treated wafers. The chamber pressure is 5mbar and the oxygen flow is 300sccm. The thickness is around 6nm.

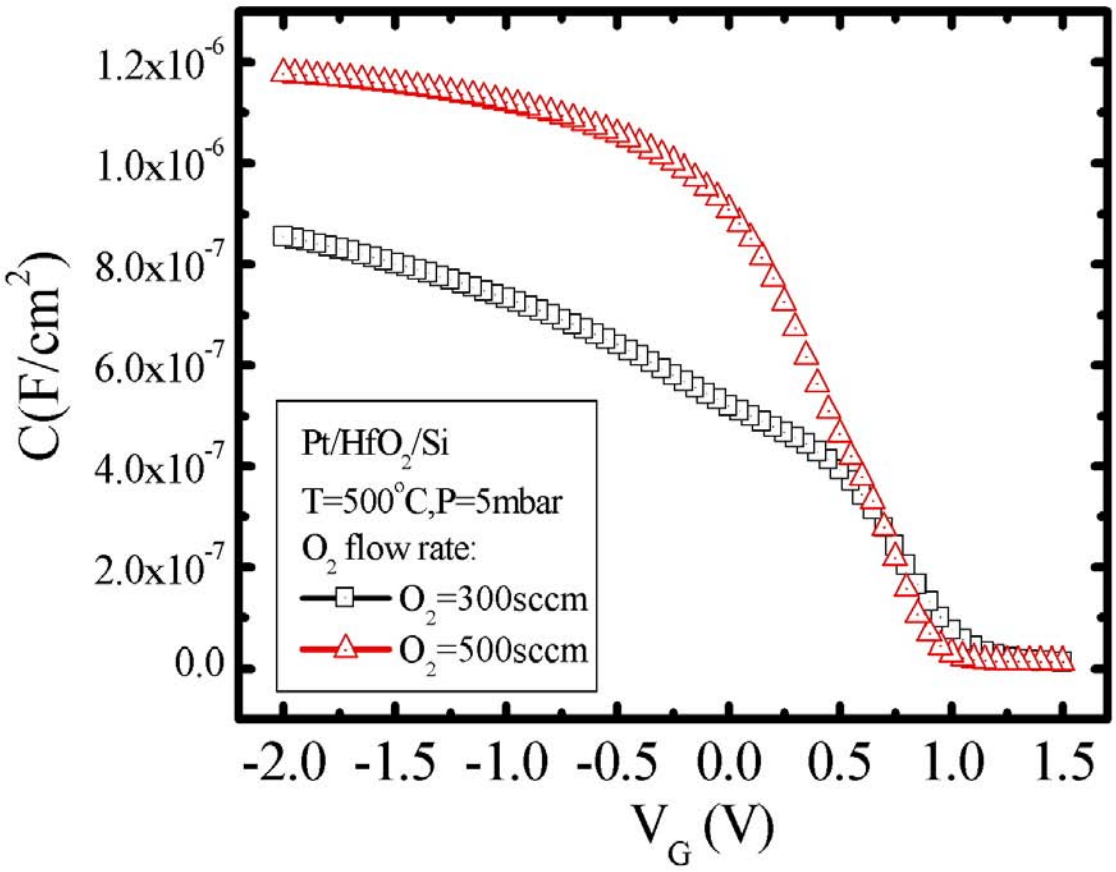
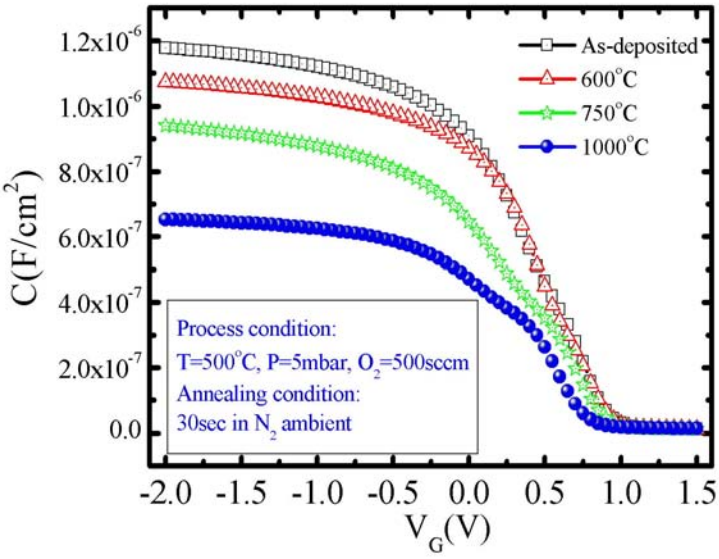
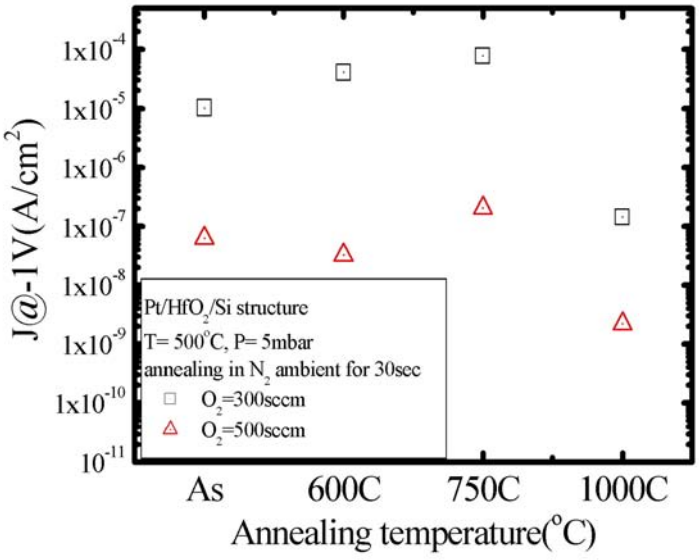


Figure 2-14 C-V characteristics of the HfO_2 films deposited with different oxygen gas flows on HF-treated wafers. The substrate temperature is 500°C and the chamber pressure is 5mbar. The thickness is around 6nm.

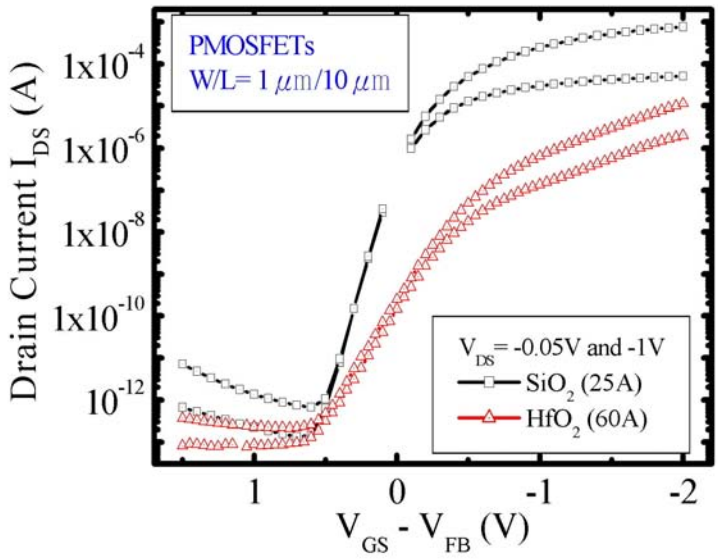


(a)

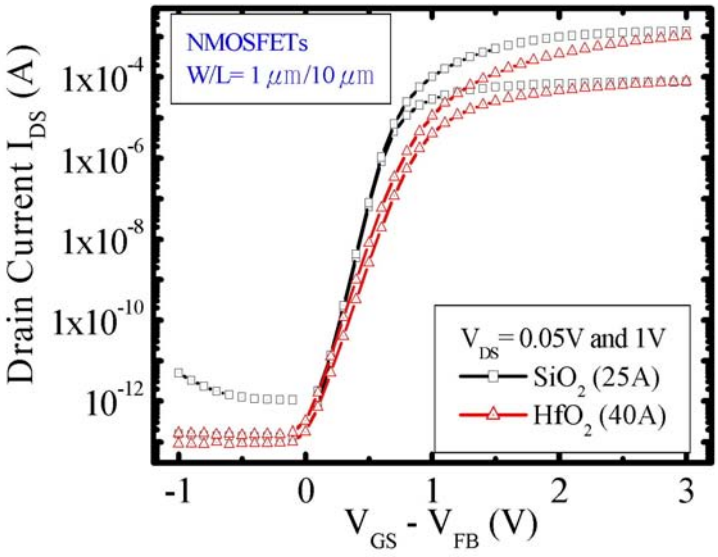


(b)

Figure 2-15 (a) C-V characteristics and (b) leakage current density at -1V versus PDA temperature of the HfO_2 films deposited at 500℃ with different O_2 gas flow on HF-treated wafers.

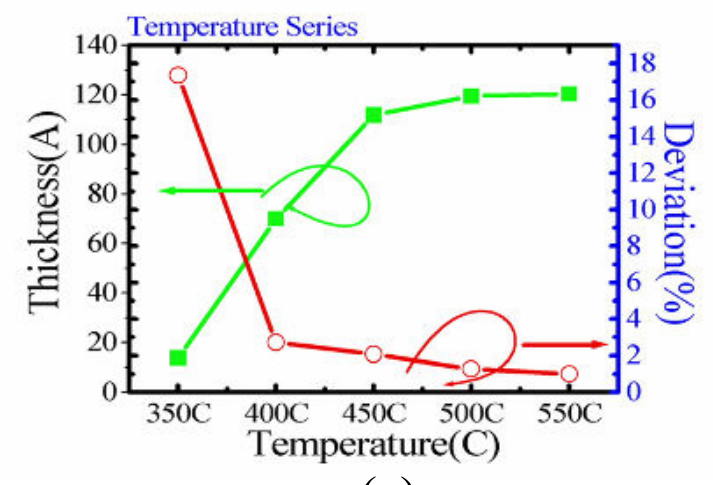


(a)

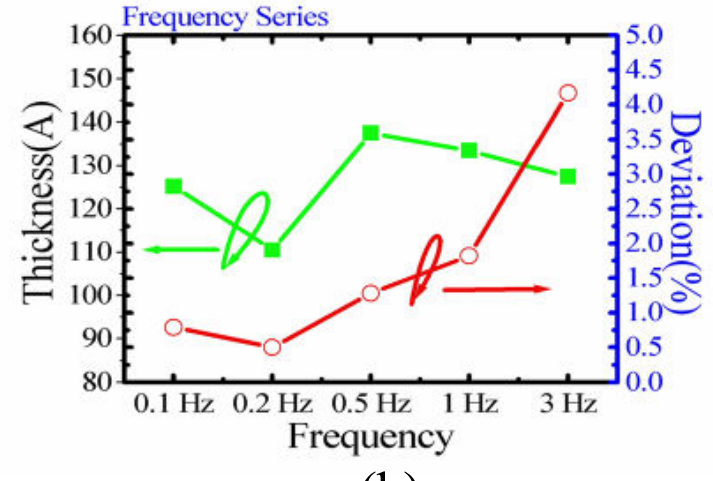


(b)

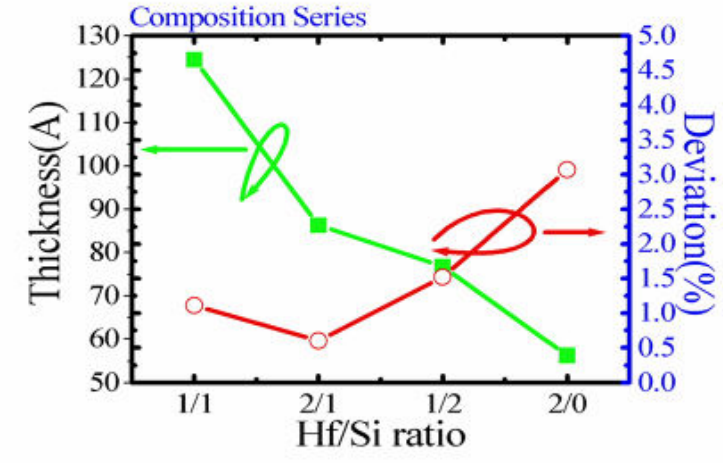
Figure 2-16 Transfer characteristics of (a) PMOSFETs, and (b) NMOSFETs with HfO_2 gate dielectrics. The deposition temperature and oxygen flow of the HfO_2 film are 400°C, 300sccm for PMOSFETs and 500°C, 1700sccm for NMOSFETs, respectively.



(a)



(b)



(c)

Figure 2-17 Thickness and Deviation variations of (a) Temperature series, (b) Frequency series, and (c) Composition series.

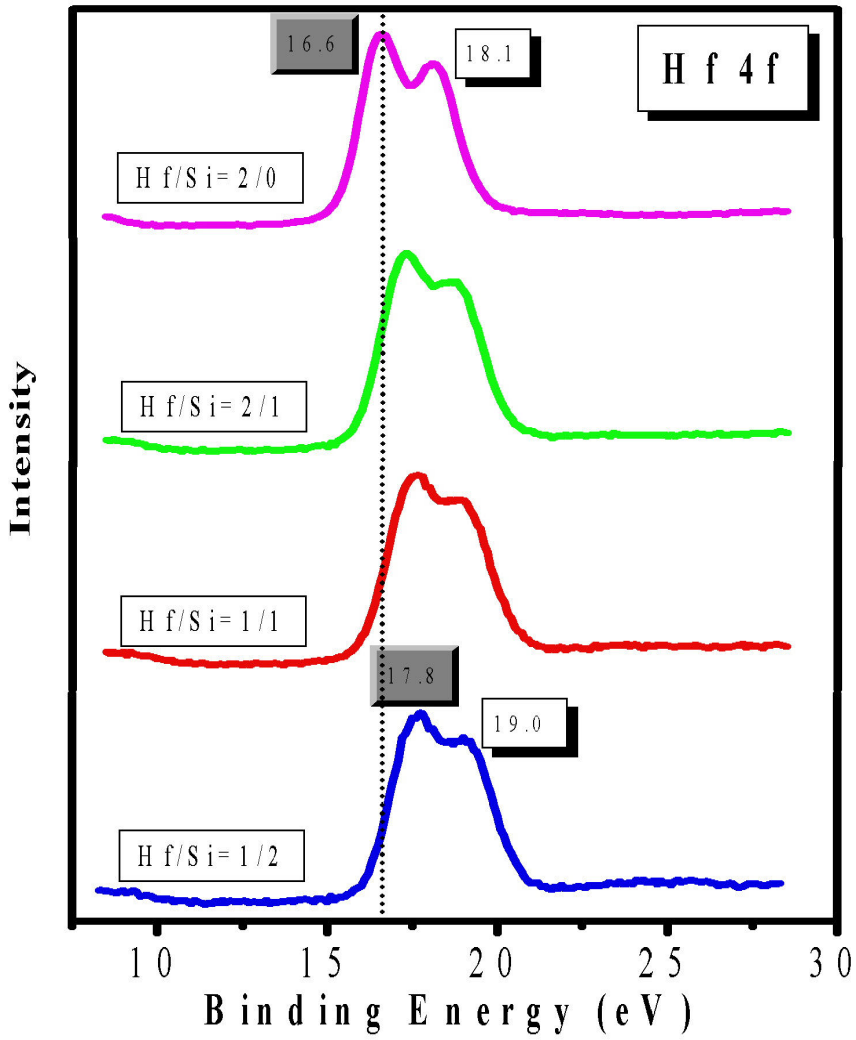


Figure 2-18 XPS Spectra of Hf_{4f} for $HfSiO_x$ films deposited by AVD at various Hf/Si composition ratios on Si (100).

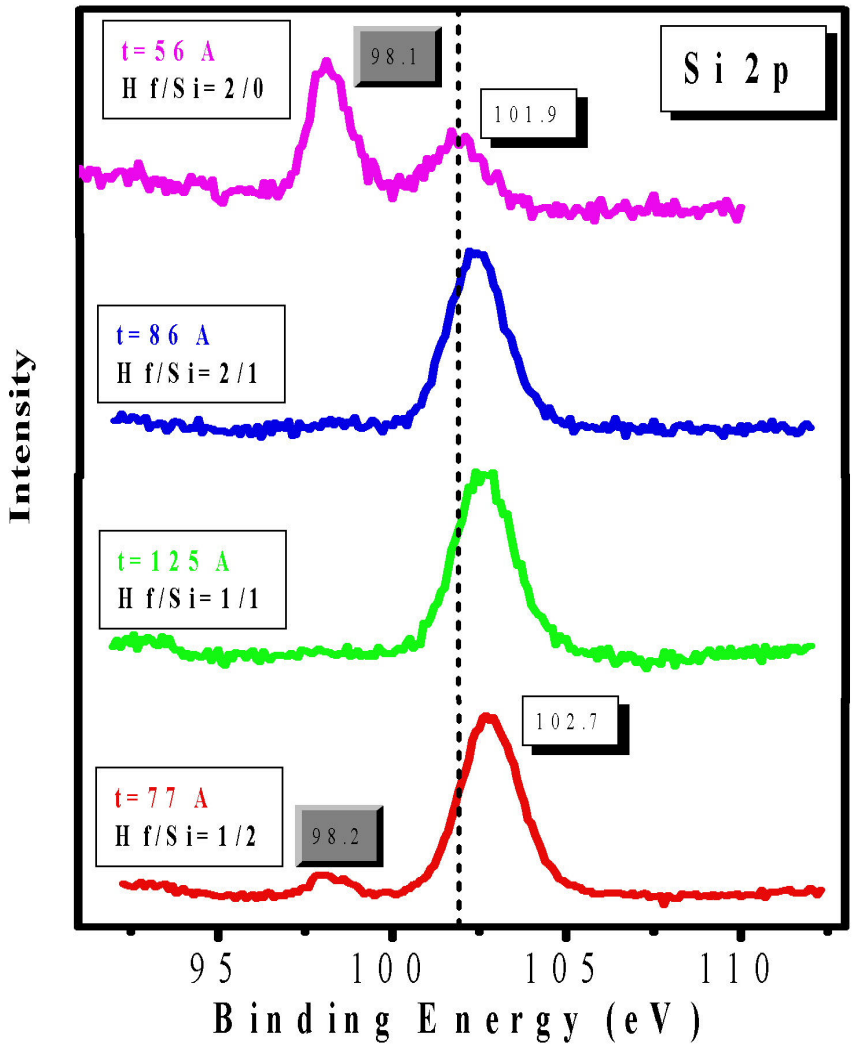


Figure 2-19 XPS Spectra of Si_{2p} for $HfSiO_x$ films deposited by AVD at various Hf/Si composition ratios on Si (100).

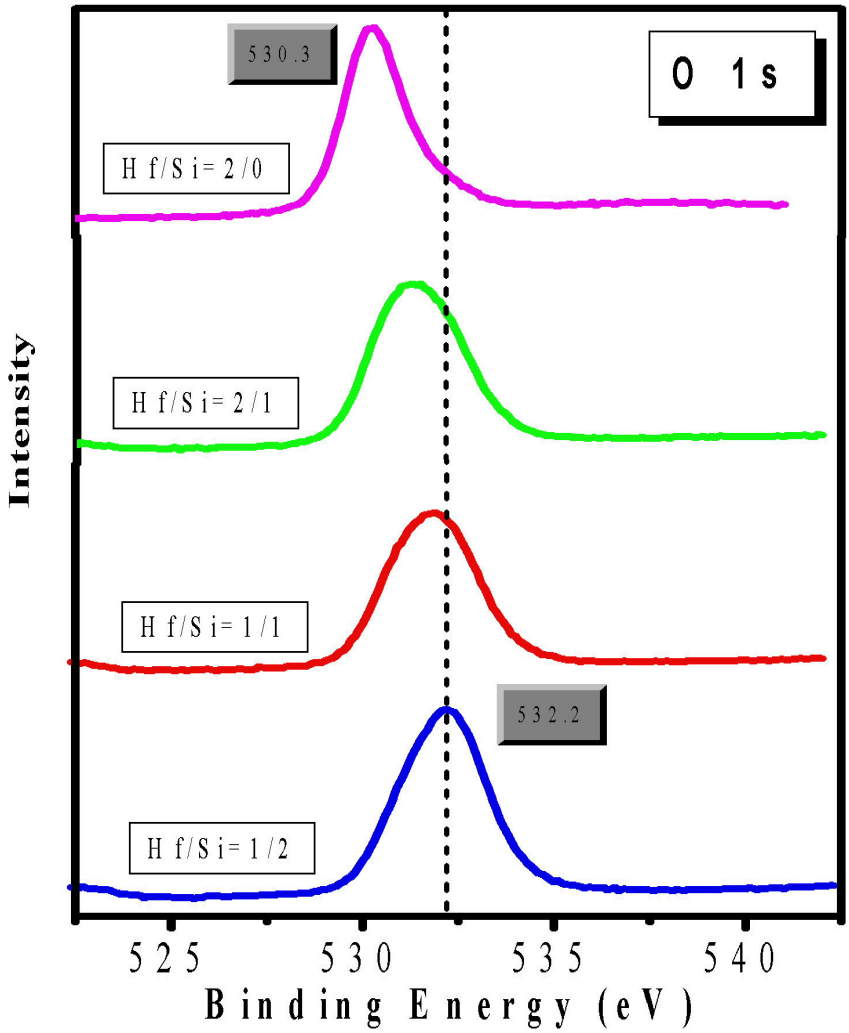


Fig. 2-20 XPS Spectra of O_{1s} for $HfSiO_x$ films deposited by AVD at various Hf/Si composition ratios on Si (100).

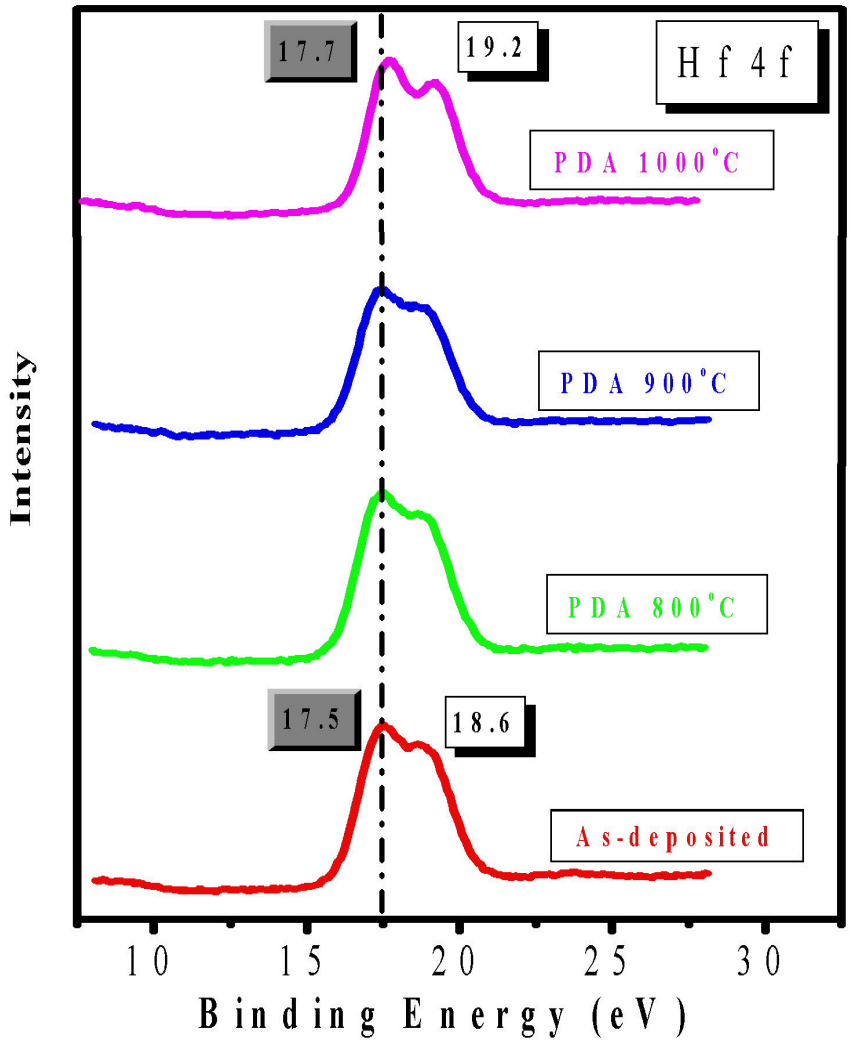


Figure 2-21 XPS Spectra of Hf_{4f} for $HfSiO_x$ films with Hf/Si ratio of 1/1 deposited by AVD on Si (100) after different PDA treatments. The thickness is around 26nm.

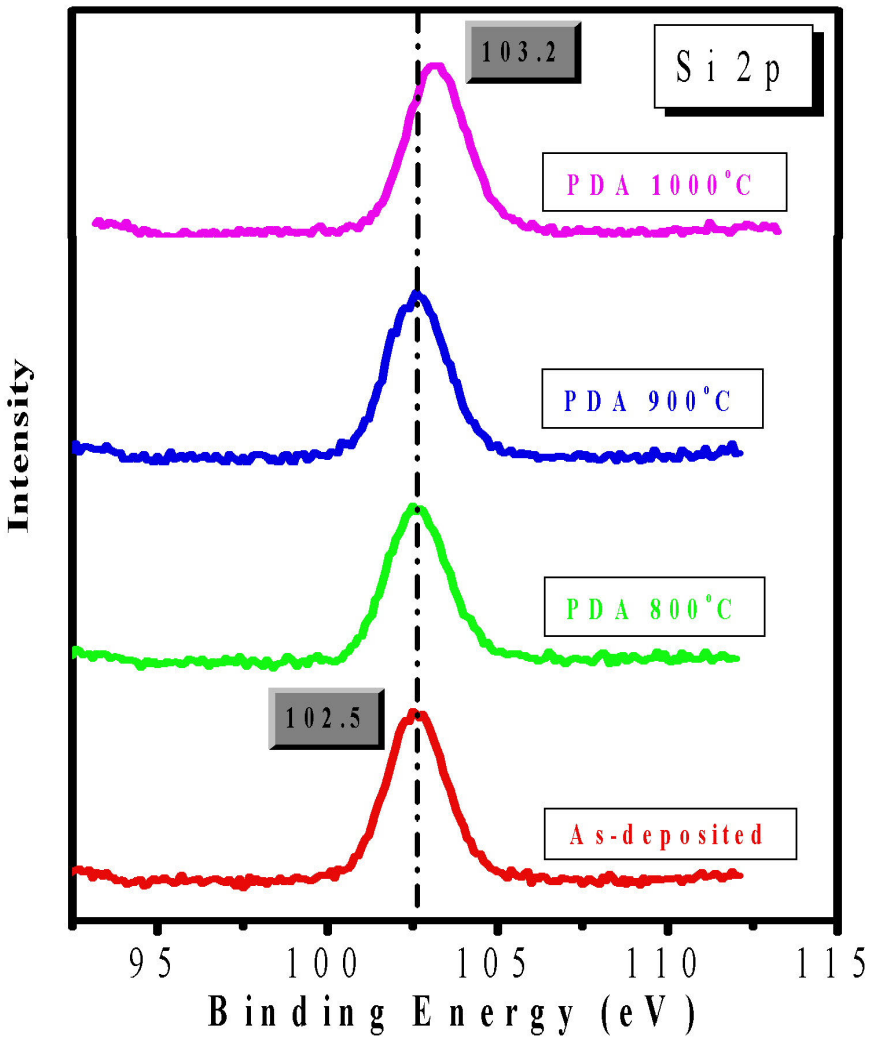


Figure 2-22 XPS Spectra of Si_{2p} for $HfSiO_x$ films with Hf/Si ratio of 1/1 deposited by AVD on Si (100) after different PDA treatments. The thickness is around 26nm.

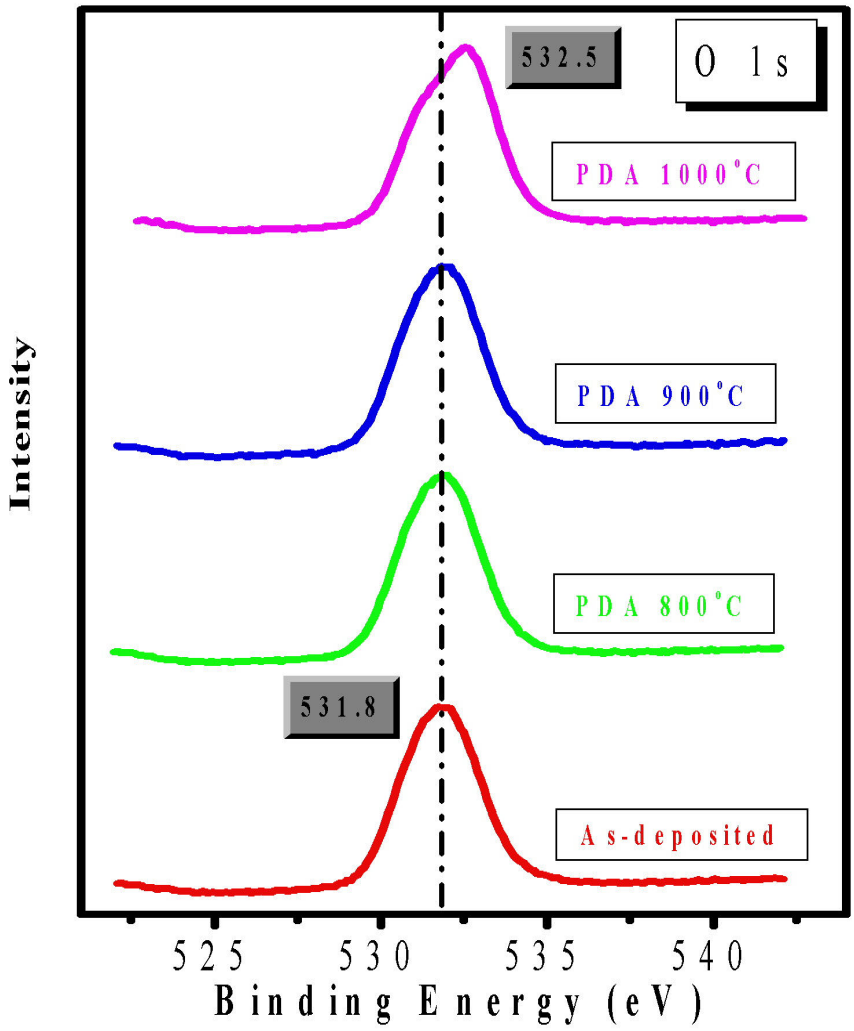


Figure 2-23 XPS Spectra of O1s for HfSiOx films with Hf/Si ratio of 1/1 deposited by AVD on Si (100) after different PDA treatments. The thickness is around 26nm.

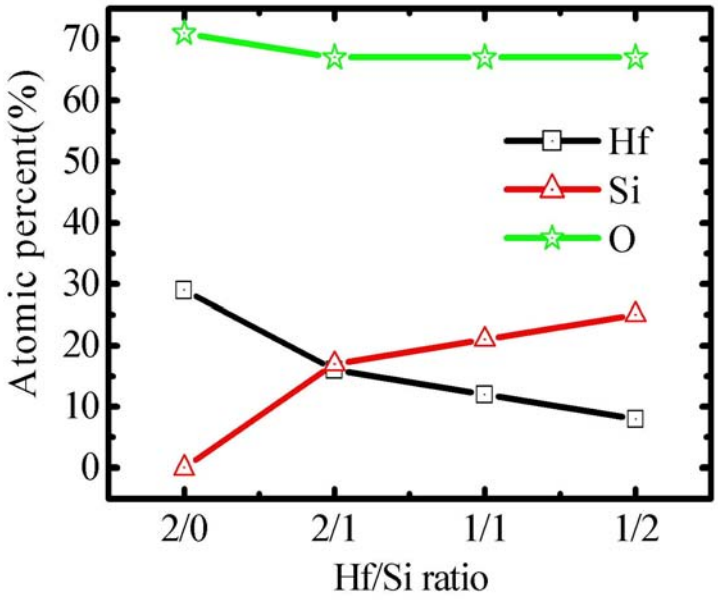


Figure 2-24 Variations of different atomic percent for HfSiOx films deposited by AVD at various Hf/Si composition ratios on Si (100).

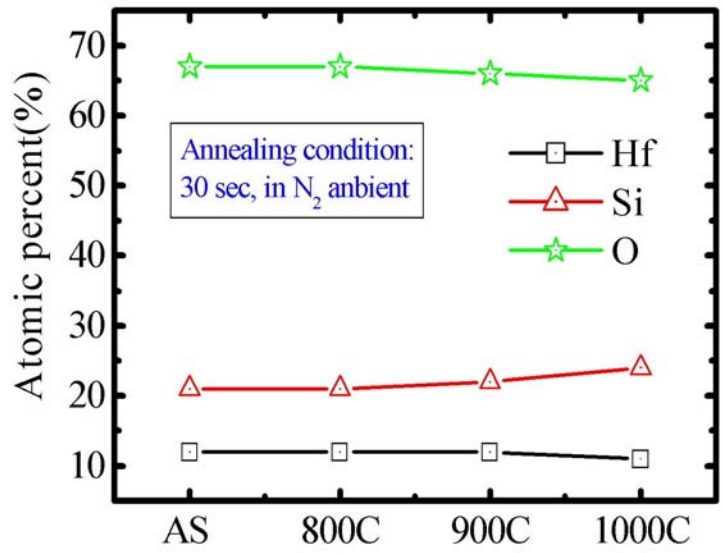
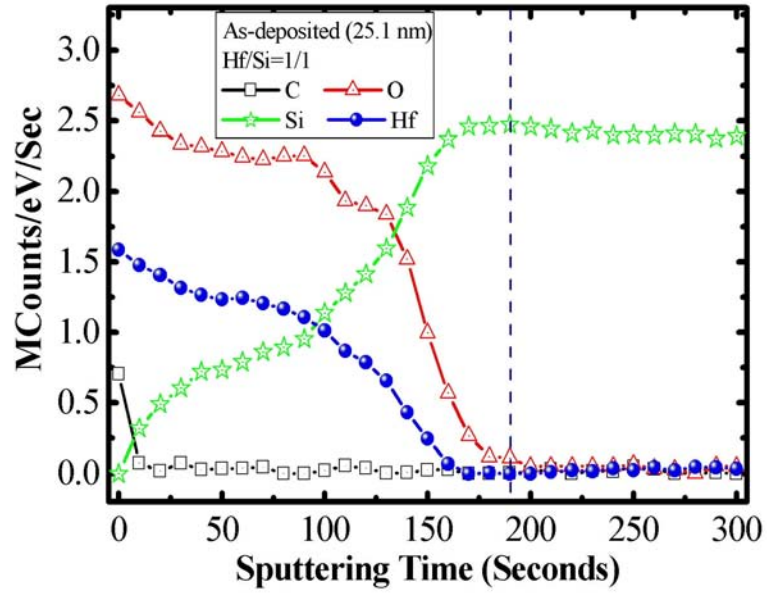
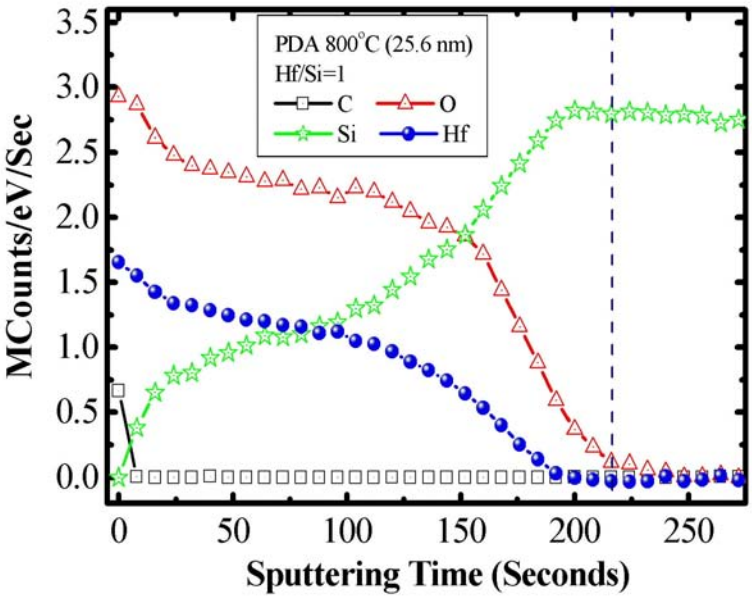


Figure 2-25 Variations of different atomic percent for $HfSiO_x$ films with Hf/Si ratio of 1/1 deposited by AVD on Si (100) after different PDA treatments. The thickness is around 26nm.

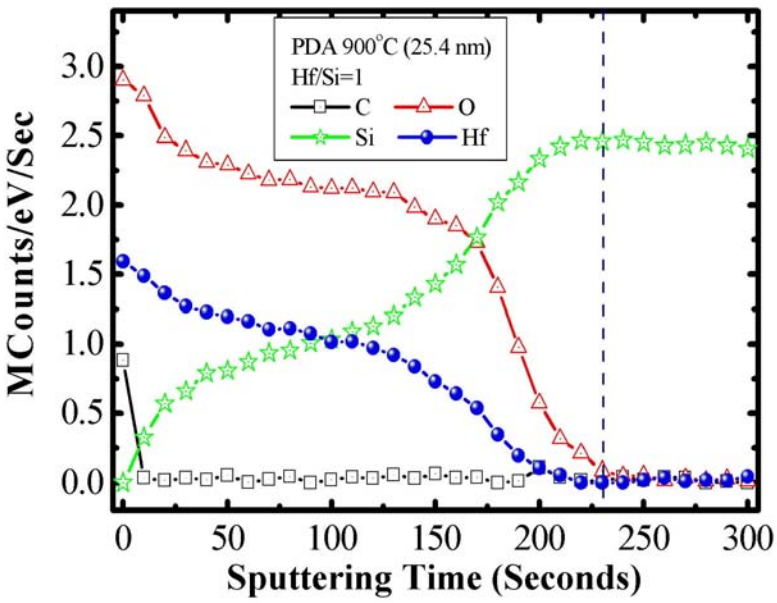


(a)

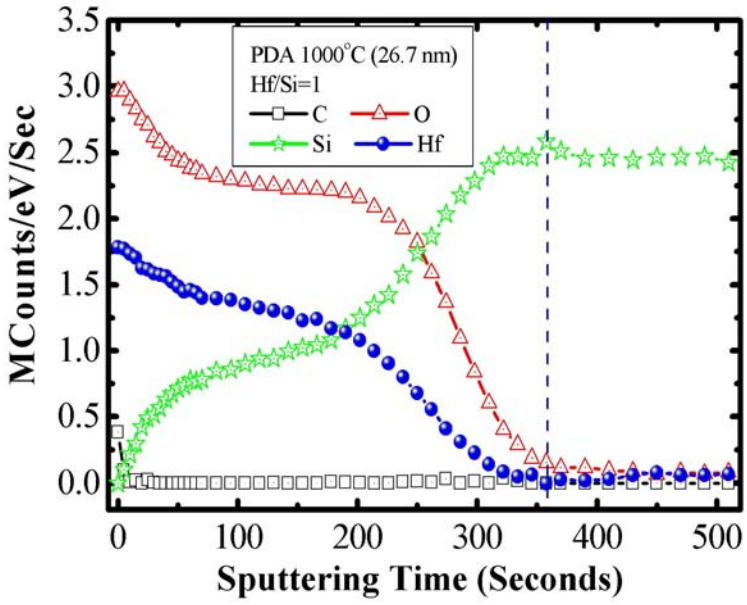


(b)

Figure 2-26 AES depth profiles of (a) the as-deposited $HfSiO_x$ film with Hf/Si ratio of 1/1 deposited at 500°C by AVD on Si (100) and the samples with (b) 800°C PDA treatments.



(c)



(d)

Figure 2-26 AES depth profiles of as-deposited $HfSiO_x$ film with Hf/Si ratio of 1/1 deposited at 500°C by AVD on Si (100) with (c) 900°C, (d) 1000°C PDA treatments.

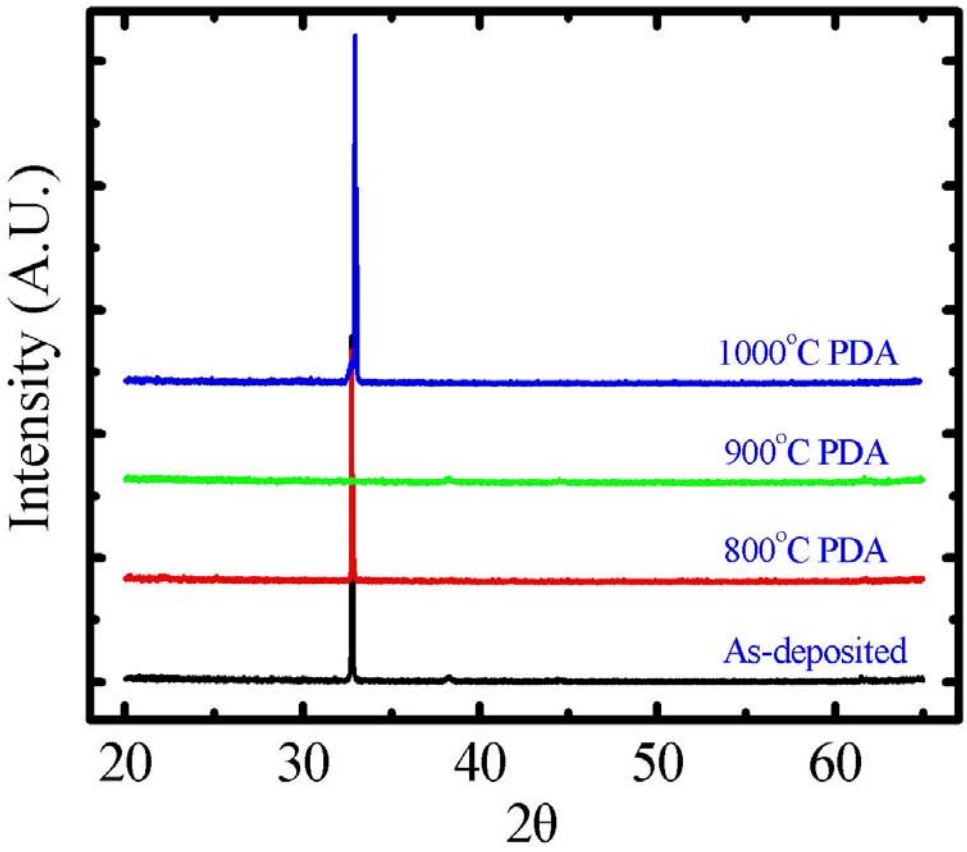


Figure 2-27 XRD Spectra of $HfSiO_x$ film with Hf/Si ratio of 1/1 deposited at 500°C by AVD on Si (100) with various PDA temperature, T= 800°C ~ 1000°C. The thicknesses is around 25nm.

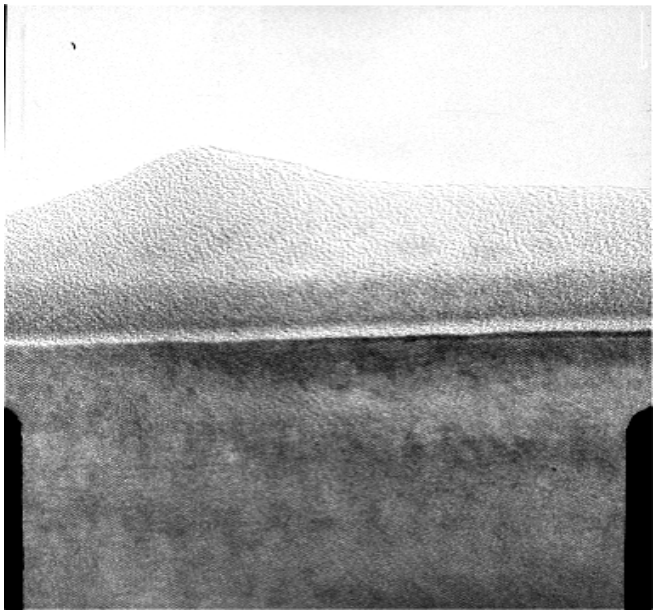


Figure 2-28 Images of cross-sectional TEM for as-deposited $HfSiO_x$ film with Hf/Si ratio of 1/1 deposited at 500°C by AVD on native-oxide-based Si-substrate. The thicknesses of $HfSiO_x$ thin film is around 11nm.

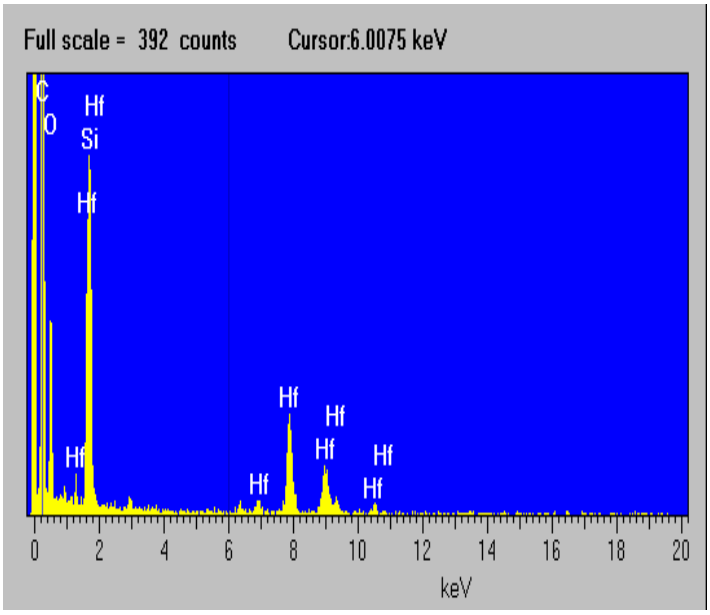
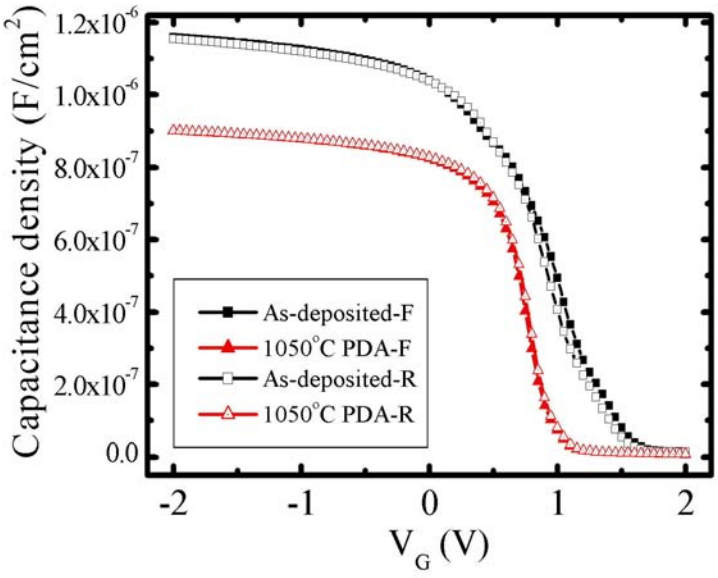
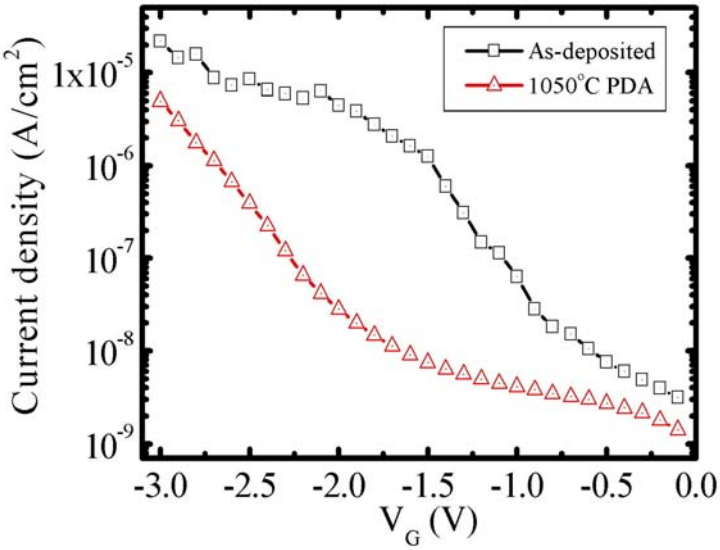


Figure 2-29 TEM-EDX for as-deposited $HfSiO_x$ film with Hf/Si ratio of 1/1 deposited at 500°C by AVD on native-oxide-based Si-substrate. The thickness is around 11nm.

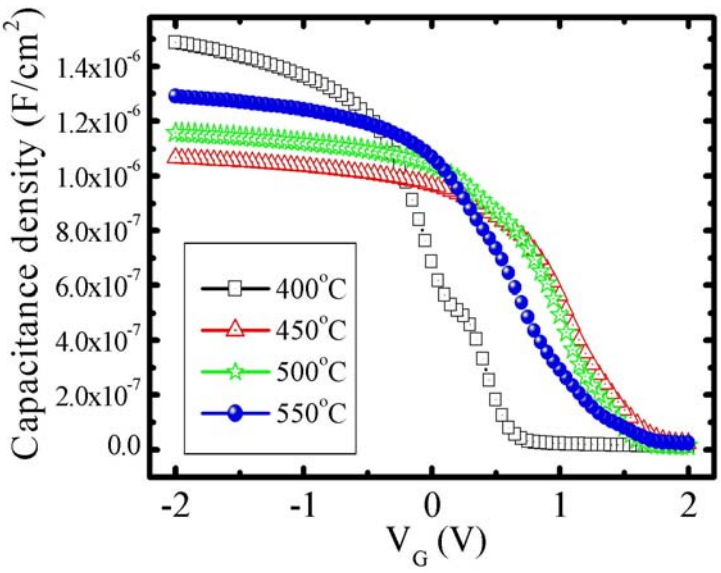


(a)

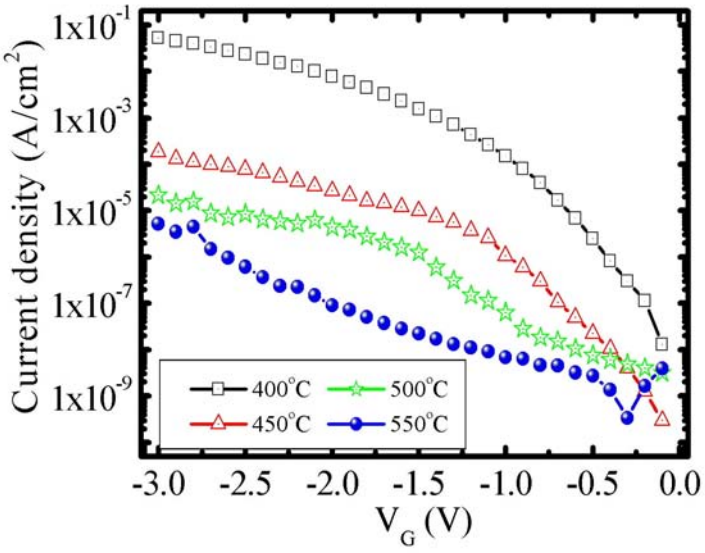


(b)

Figure 2-30 (a) C-V and (b) J-V characteristics of $HfSiO_x$ films deposited at 500°C and 1050°C PDA treatment for 10sec in N_2 ambient. The oxygen gas flow is 1700sccm and the thickness is around 5nm.



(a)



(b)

Figure 2-31 (a) C-V and (b) J-V characteristics of $HfSiO_x$ films deposited at different substrate temperatures. The oxygen gas flow is 1700sccm and the thickness is around 5nm.

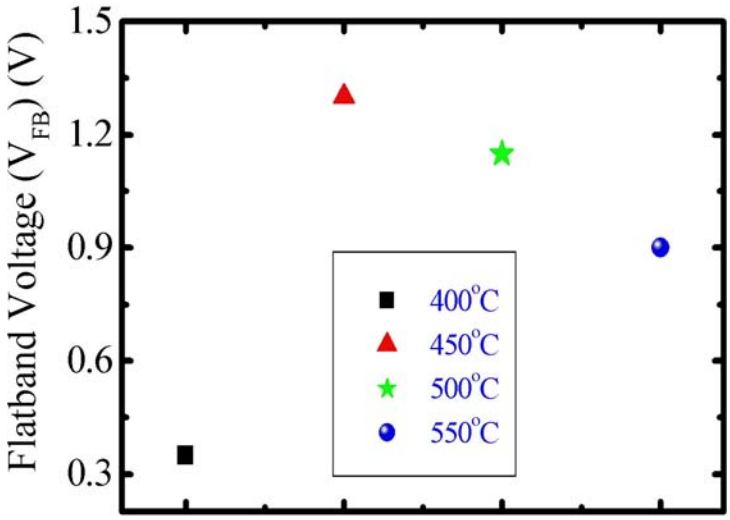


Figure 2-32 Flatband voltage of $HfSiO_x$ films deposited at different substrate temperatures. The oxygen gas flow is 1700sccm and the thickness is around 5nm.

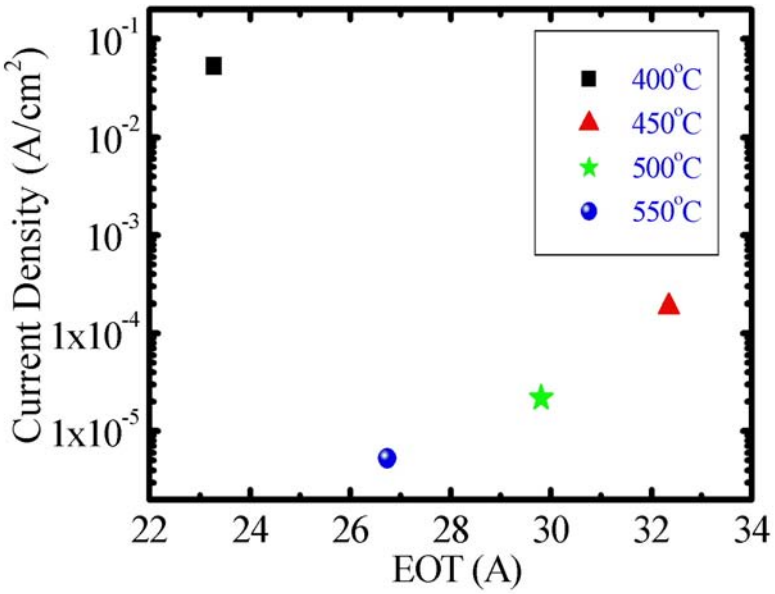
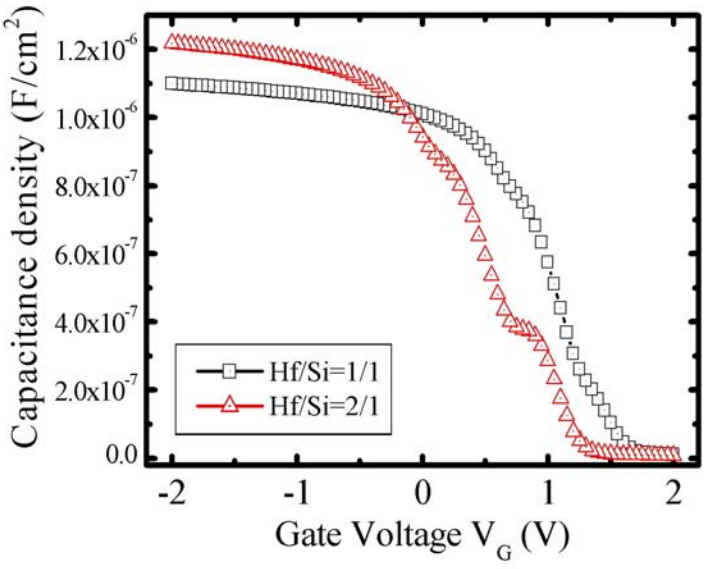
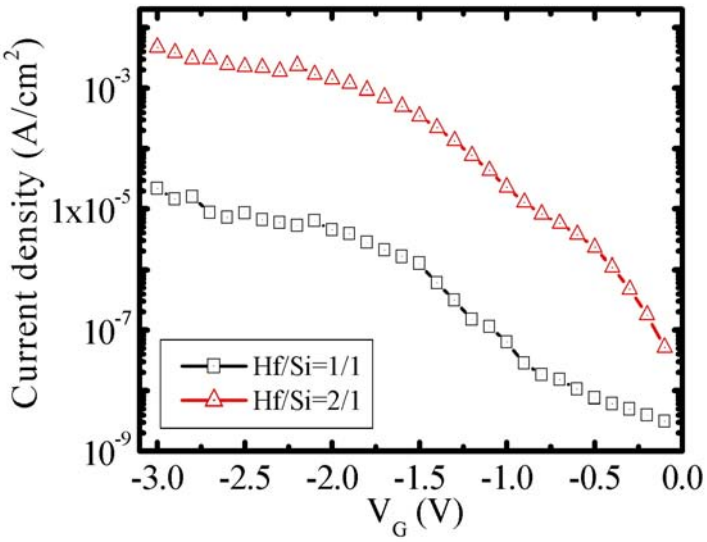


Figure 2-33 Leakage current density versus EOT of the $HfSiO_x$ films deposited at different substrate temperatures. The oxygen gas flow is 1700sccm and the thickness is around 5nm.



(a)



(b)

Figure 2-34 (a) C-V and (b) J-V characteristics of $HfSiO_x$ films deposited at 500°C with different Hf/Si ratios. The oxygen gas flow is 1700sccm and the thickness is around 5nm.

Chapter 3
High-Performance and Low-Temperature-Compatible P-Channel Polycrystalline-Silicon TFTs Using Hafnium Silicate Gate Dielectric

3-1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are employed extensively in active-matrix liquid crystal displays because of their superior performance [3.1]. Recently, the practicability of integrating the entire system on the panel (SOP) has been investigated vigorously [3.2]. This goal requires that the display driving circuits contain high-performance TFTs capable of operating at lower voltages while delivering higher drive currents. Although scaling down the gate oxide can increase the drive current of a TFT, it leads inevitably to a higher gate leakage current because of the decreased quality of the low-temperature-deposited gate dielectrics [3.3]. To maintain the physical dielectric thickness while increasing the gate capacitance, several new high-κ materials have been proposed, including Al_2O_3, Ta_2O_5, and HfO_2 [3.4]–[3.6]. Because Al_2O_3 films exhibit relatively low values of κ (roughly 7) and excess fixed charge, the TFT performance is not improved sufficiently for application [3.7]. The narrow band-gap of Ta_2O_5 implies that a thicker film is necessary to reduce the gate leakage current of TFTs [3.8], which limits the increase in gate capacitance. Recently, hafnium dioxide (HfO_2) has been applied to TFTs because of its high value of κ (14–20) and sufficiently wide band-gap [3.6]. Although poly-Si TFTs incorporating HfO_2 as the gate dielectric exhibit superior performance in many respects, several issues remain problematic: e.g., the

higher gate leakage current arising from poly-crystalline HfO_2 films and the degraded mobility arising from additional scattering.

In this chapter, we focus on the depositions of thicker high-κ films (~60nm) and present both structural and electrical characterization of these high-κ films. And then, we describe a systematic study of the electrical properties of low-temperature-compatible p-channel poly-Si thin-film transistors (TFTs) using HfO_2 and $HfSiO_x$ high-κ gate dielectrics. We found that the transistors containing $HfSiO_x$ gate dielectric exhibit higher values of I_{on}/I_{off} and μ_{FE} and smaller values of subthreshold swing (S.S.) and V_{th}, relative to transistors containing the conventional deposited-SiO_2 dielectric.

3-2 High-κ Film Depositions and Device Fabrications

Firstly, the thicker high-κ films (~60nm) were deposited through atomic vapor deposition (AVD) system. From the experience of thin high-κ film deposition, we set the substrate temperature as 500°C and oxygen gas flow as 1700sccm. The $Hf[OC(CH_3)_3]_2(mmp)_2$ precursor, $Si[OC(CH_3)_3]_2(mmp)_2$ precursor and oxygen gas were employed as Hf, Si, and O sources, respectively. The structural characterizations of these films would be analyzed by various measurements, such as atomic force microscopy (AFM), scan electron microscopy (SEM), x-ray diffraction (XRD), and high-resolution transmission electron microscopy (HRTEM). And then, self-aligned top-gated p-channel poly-Si TFTs were fabricated and the procedure flow was illustrated in Figure 3-1. First of all, a 550nm-thick thermal oxide was grown on Si wafers in a furnace to simulate the glass substrate. Next, a 100nm-thick amorphous silicon layer was deposited through the dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550°C. Subsequently, solid phase crystallization (SPC) was performed at 600°C for 24 hour in N_2 ambient to induce the

crystallization of amorphous silicon. Individual active regions were then patterned by lithography and defined by dry etching. After RCA cleaning, various gate dielectrics (with thickness of 60nm) were deposited. Specifically, HfO_2 and $HfSiO_x$ films were deposited through atomic vapor deposition (AVD) using an AIXTRON Tricent system at a substrate temperature of 500°C. The as-deposited oxide, which served as the control sample, was prepared through LPCVD at 700°C using tetraethyloxysilane (TEOS) as the precursor. All of the wafers were then subjected to deposition of a 300nm-thick amorphous silicon layer, which served as the gate electrode, through LPCVD at 550°C. The gate electrodes were patterned and the source, drain, and gate regions were doped through self-aligned boron ion implantation (dosage: 5×10^{15} ions/cm^2; energy: 15 keV). After formation of the source and drain, the dopant was activated at 600°C for 24 hour in N_2 ambient. Following that, 500nm SiO_2 was deposited by PECVD as the interlayer dielectric. Finally, contact holes were opened and 550nm AiSiCu alloy was deposited and defined. Wafers were then sintered at 400°C for 30 min in forming gas to complete the fabrication. No plasma treatment was executed for all device samples. Capacitors containing high-κ dielectrics were fabricated simultaneously through the use of a shadow mask to allow measurement of dielectric constants and leakage current densities (the process flow is illustrated in Figure 3-2). Device measurements were performed using a Keithley 4200 semiconductor characterization system, a HP 4156A precision semiconductor parameter analyzer, and an Agilent 4284A precision LCR meter. The field effect mobility, which was extracted from the maximum transconductance (G_m), and the S.S. were measured at V_{DS} of -0.1 V. The value of S.S. was extracted from the maximum slope of I_D-V_{GS} characteristics. Threshold voltage (V_{th}) was defined as the gate voltage at which the drain current reached a normalized drain current (I_D) equal to $(W/L) \times 10^{-8}$ A at V_{DS} of -0.1 V, where W was the drawn channel width and L was the drawn channel length.

3-3 Structural Characterization of High-κ Films

Figures 3-3(a)-(c) display AFM images of HfO_2, $HfSiO_x$ and deposited-SiO_2 films, respectively. The mean surface roughness of $HfSiO_x$ and deposited-SiO_2 films were 0.42 and 0.60 nm, respectively—much smaller than that of the HfO_2 film (i.e., 1.98 nm). Obviously, HfO_2 film exhibits apparent grain structure (as seen clearly in Fig. 3-4) related to its polycrystalline structure and shows a rough surface. Instead, $HfSiO_x$ and deposited-SiO_2 films depict small surface roughness related to their amorphous structures. For further analysis, we used XRD measurements to investigate the crystallinity of HfO_2 and $HfSiO_x$ films (Fig. 3-5). After annealing at 600°C and 24 hour in a N_2 ambient, HfO_2 films clearly exhibit polycrystalline monoclinic structure, whereas $HfSiO_x$ films remain in amorphous form. This behavior suggests that the $HfSiO_x$ film has better thermal stability than the HfO_2 film. Figures 3-6 to 3-8 display cross-sectional transmission electron microscopy (TEM) images at different magnifications of the HfO_2, $HfSiO_x$, and deposited-SiO_2 films, with physical thicknesses of 57, 53, and 61 nm, respectively. These TEM samples of poly-TFT devices were fabricated by focus ion beam (FIB) method and the test structures (poly-Si gate-electrode/gate-dielectric/poly-Si channel) are included in all samples. Samples with $HfSiO_x$ and deposited-SiO_2 films possess amorphous structures, which are conducive to forming smoother surfaces at both the top and bottom interfaces, whereas the device with HfO_2 gate dielectric depicts polycrystalline structure and displays rough top interface, consistent with the above AFM results. In addition, as discussed in Chapter 2, the interfacial layer between high-κ/poly-Si interface is generated during the film deposition and becomes thicker (~3nm) after 600^{o}C and 24 hour annealing, as shown at Figure 3-9.

3-4 Electrical Properties of High-κ Thick Films

Figures 3-10(a) and (b) provide plots of the capacitance density versus gate voltage and leakage current density versus the electric field, respectively, for the high-κ dielectrics. The extracted value of κ for the HfO_2 film is around 14.2, which is significantly lower than that of bulk HfO_2 (κ= 25~30), possibly because of (a) the thicker interfacial layer with lower κ value (Fig. 3-9), or (b) the presence of excess oxygen atoms in the HfO_2 film [3.9], and (c) the fact that effective charges associated with the softest modes are relatively weak when the HfO_2 film possesses its most-stable monoclinic structure [3.10]-[3.11]. On the other hand, the value of κ for the $HfSiO_x$ film is around 8.11, which is also lower than expected. The Hf/Si composition ratio calculated from this value of κ (around 1:1.44) is close to that measured using electron spectroscopy for chemical analysis (ESCA, 1:1.38~1:1.75). This result indicates that Si atoms are more reactive toward oxygen atoms than are Hf atoms under our process conditions, which is consistent with the results in Chapter 2. The lower dielectric constant of the $HfSiO_x$ films is therefore due to their being Si-rich. In terms of the current–voltage characteristics, the $HfSiO_x$ films exhibit superior performance—smaller leakage current (4.70×10^{-9} A/cm^2 at V_{GS} = -10 V) and larger breakdown field (-7 MV/cm), compared with the HfO_2 films (7.60×10^{-8} A/cm^2 and -4 MV/cm, respectively), presumably because of the amorphous nature of $HfSiO_x$ after processing. Furthermore, the $HfSiO_x$ films also exhibit smaller frequency dispersion (~6%) than the HfO_2 films (~13%) on the C-V curves measured at 100K and 1M Hz, as shown in Figure 3-11. We believe this is due to the better film quality and less trap density in the $HfSiO_x$ films.

3-5 Characteristics of Low-Temperature-Polycrystalline-Silicon (LTPS) TFTs Using High-κ Gate Dielectrics

Figure 3-12(a) provides comparisons of transfer characteristics between TFTs containing $HfSiO_x$ and deposited-SiO_2, while Fig. 3-12(b) provides comparisons between TFTs containing $HfSiO_x$ and HfO_2, measured at V_{DS} of -0.1 and -2 V. It can be seen that TFTs containing high-κ dielectrics display considerably better performance than the TFT containing conventional deposited-SiO_2, with the exception of the OFF-state leakage current. From the output characteristics shown in Figure 3-13, it can be seen more clearly that the TFT with $HfSiO_x$ gate dielectric exhibits larger drive-current than those devices using deposited-SiO_2 and HfO_2 gate dielectrics. Table 3-1 summarizes these measured data and the extracted device parameters among all samples. In addition to the superior quality of the gate dielectric–poly-Si interface [3.5], we believe that the thinner equivalent oxide thicknesses (EOTs) of the high-κ dielectrics at the same physical thickness accounts for the lower value of V_{th} and the significantly improved S.S. [3.12]-[3.13]. Moreover, some authors have reported previously that the values of V_{th} and S.S. are sensitive to the density of deep states near the mid-gap; i.e., as the density of states decreases, the values of V_{th} and S.S. decrease [3.14]. This behavior is supported by the plots of the density-of-state versus ΔE (where $\Delta E = E - E_{fb}$) for the poly-Si TFTs incorporating various gate dielectrics (Fig. 3-14). The values of density-of-state were extracted from the transfer characteristics measured at 25, 50, 75, 100, and 125°C [3.15]. We found that the high-κ dielectrics deposited by AVD system at 500°C did possess lower densities-of-state than the lower-temperature deposited-SiO_2 film. On the other hand, the effective interface-trap-state density (N_{it}) near the poly-Si–gate dielectric interface can also be evaluated from the value of S.S. [3.16]:

$$N_{it} = \left[\left(\frac{S}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{gate\ dielectric}}{q}\right). \quad (3.1)$$

The calculated values of N_{it} for the HfO_2, $HfSiO_x$, and deposited-SiO_2 TFTs were 5.60 × 10^{12}, 4.44 × 10^{12}, and 7.86 × 10^{12}/cm^2, respectively. Thus, this approach also reveals

that the high-κ dielectrics possess lower densities-of-states relative to that of the deposited-SiO_2.

Although the values of the S.S. and I_{on}/I_{off} current ratio of TFTs containing $HfSiO_x$ are slightly worse than those of the TFTs incorporating HfO_2, we believe that $HfSiO_x$ is a better choice for use as the gate dielectric in future poly-Si TFTs for the following reasons: First, TFTs containing $HfSiO_x$ films exhibit smaller leakage current and larger breakdown field strength than TFTs containing HfO_2 because of the amorphous nature of the $HfSiO_x$ film after processing. Second, the hole mobility of TFTs containing $HfSiO_x$ is 76% better than that of the conventional TFTs incorporating the deposited-SiO_2 dielectric, whereas it is worse for the TFTs containing the HfO_2 gate dielectric. According to previous reports [3.17]–[3.19], we speculate that the degraded mobility of the TFTs containing the HfO_2 dielectric is due to additional Coulomb scattering caused by the charges in the HfO_2 dielectric. In MOSFETs application, additional Coulomb scattering is closely related to the polycrystalline structure of the HfO_2 films, which in turn leads to severe mobility degradation in devices possessing physically thicker HfO_2 films [3.18]. In contrast, $HfSiO_x$ films prevent this additional scattering and exhibit improved mobility because of their higher thermal stability. Possible mechanisms of mobility degradation will be discussed in detail in next chapter. Third, the removal of $HfSiO_x$ through etching is much easier than that of HfO_2. This feature is rather important for device fabrication. We employed a buffer-oxide-etch (BOE) solution and an induced-coupling-plasma (ICP) etcher to perform wet and dry etching, respectively. Table 3-2 summarizes the etching rates for the various dielectrics when using the two etching methods and various gases. The HfO_2 film could not be etched away; its thickness remained nearly constant after wet etching for 1 min. For dry etching, we found that the etching rate for HfO_2 film with CF_4/CHF_3 mixing gas (0.4 nm/s) was much lower than that for the deposited-SiO_2 (6.5 nm/s). Even though the

etching rate could be increased to 1.3 nm/s when using Cl_2 gas, the poly-Si channel was more vulnerable to etching damage because of its relatively high etching rate(3 nm/s). In contrast, $HfSiO_x$ films could be removed by the BOE solution at a rate of 0.65 nm/s, and the dry etching rates were also faster than those of the HfO_2 films. As a result, less etching damage occurred at the $HfSiO_x$ film–poly-Si interface of contact regions when using a sequence of dry etching followed by wet etching near the end of the etching process.

3-6 Dependence of Electrical Characteristics on Channel Length and Channel Width

Figures 3-15 to 3-19 exhibit various dependence of electrical properties on the channel length and width of LTPS TFTs, including threshold voltage (V_{th}), subthreshold swing (S.S.), off-state current (I_{off}), drive current (I_{on}), and field-effect mobility (μ_{FE}). For the channel length dependence measurements, we fixed the channel width at 10μm and varied the channel length from 10μm to 1μm. By the same token, we fixed the channel length at 10μm and varied the channel widths from 50μm to 1μm in the channel width dependence measurements. As shown in Figure 3-15, it can be found clearly that TFTs using high-κ gate dielectrics exhibit lower V_{th} and smaller S.S. than their counterparts with deposited-SiO_2, and are nearly independent of the channel length. However, poly-Si TFTs with deposited-SiO_2 exhibit a drop of V_{th} and S.S. in short channel regimes. For poly-Si TFTs, V_{th} and S.S. would be affected by the number of grain boundary [3.20]-[3.21]. The trap states at grain boundaries have to be filled first before the device can be turned on, and the interface trap density also influences the subthreshold swing. For large-dimension devices, the large number of grain boundaries in the channel would result in higher threshold voltage and inferior subthreshold swing. As the device scales down, the number of grain boundaries decreases and V_{th} and S.S.

would reduce accordingly, which could be seen in the deposited-SiO_2 sample. However, the high-κ TFTs with thin EOT and large gate capacitance density can speedily fill the trap states at grain boundaries and turn on the devices fast; therefore, the grain-boundary effect can be relieved by using the advanced high-κ materials. In comparison with the short-channel-length regime of TFTs with deposited-SiO_2 gate dielectric, apparent decrease of V_{th} and S.S. of can be found in the narrow-channel-width regime, as shown in Fig. 3-16. Besides the grain-boundary effect, the higher electric field caused by the corner would turn on the devices early and induce steeper S.S. in the narrow channel width regime [3.20], [3.22]. Poly-Si TFTs with high-κ gate dielectrics also show slight decrease of V_{th} and S.S. as the channel width is below 2μm related to the narrow width effect. Figures 3-17(a) & (b) show the off-state current as a function of channel length and width of poly-Si TFTs, respectively. As is well known, the off-state current of poly-Si TFTs is caused by the field-emission current in the gate-drain overlap region. As the channel length decreases, the off-state current becomes larger owing to the increased gate-drain overlap ratio in the short channel regime, as can be seen in Fig. 3-17(a). As shown in Fig. 3-17(b), the off-state current decreases monotonously as the channel width scales down for all samples. Figures 3-18(a) & (b) display the dependence of normalized field-effect mobility and drive current on the channel length and width, respectively. Obviously, the drive current is proportional to the field-effect mobility, so the variations of μ_{FE} and I_{on} show similar treads. The field-effect mobility of poly-Si TFTs using deposited-SiO_2 and $HfSiO_x$ gate dielectrics increases slightly as the channel length or width scales down due to the reduced grain-boundary scattering. However, poly-Si TFTs with HfO_2 gate dielectric exhibit the opposite trend as the channel length and the channel width scales down. The mechanism is unclear now and further analysis has to be executed to clarify this phenomenon.

3-7 Summary

In this chapter, high performance p-channel poly-Si TFTs using hafnium silicate gate dielectric is demonstrated using low-temperature processing. Higher I_{on}/I_{off} current ratio, smaller subthreshold swing, lower threshold voltage and higher mobility than those with conventional deposited-SiO_2 gate dielectric are achieved at lower operation voltages. Our results suggest that $HfSiO_x$ is a potential candidate for the gate-dielectric material of future high-performance poly-Si TFTs.

Table 3-1

Device parameters of Low-Temperature P-Channel Poly-silicon TFTs (W/L= 5μm/10μm) incorporating various gate dielectrics at V_{DS} of -0.1V.

W/L= 5μm/10μm Gate dielectric	I_{on}/I_{off} ratio (@V_{DS}= -2V)	S. S. (V/Dec)	V_{th} (V)	μ_{FE} (cm^2/V-sec)	EOT (nm)
HfO_2 ($T_{physical}$ = 57nm)	5.78E6 (V_{GS}= -8V)	0.31	0.19	15.73	15.7
$HfSiO_x$ ($T_{physical}$ = 53nm)	4.09E6 (V_{GS}= -10V)	0.40	-1.24	31.89	25.5
Deposited-SiO_2 ($T_{physical}$ = 61nm)	3.91E6 (V_{GS}= -16V)	0.98	-6.78	18.09	46.5

Table 3-2

Etching rates of various gate dielectrics.

Gate dielectric	**BOE etching**	**ICP dry etcher**	
		CF_4/CHF_3	**Cl_2**
HfO_2	0 nm/sec	0.4 nm/sec	1.3 nm/sec
$HfSiO_x$	0.65 nm/sec	1.1 nm/sec	2.6 nm/sec
Deposited-SiO_2	10 nm/sec	6.5 nm/sec	3.5 nm/sec

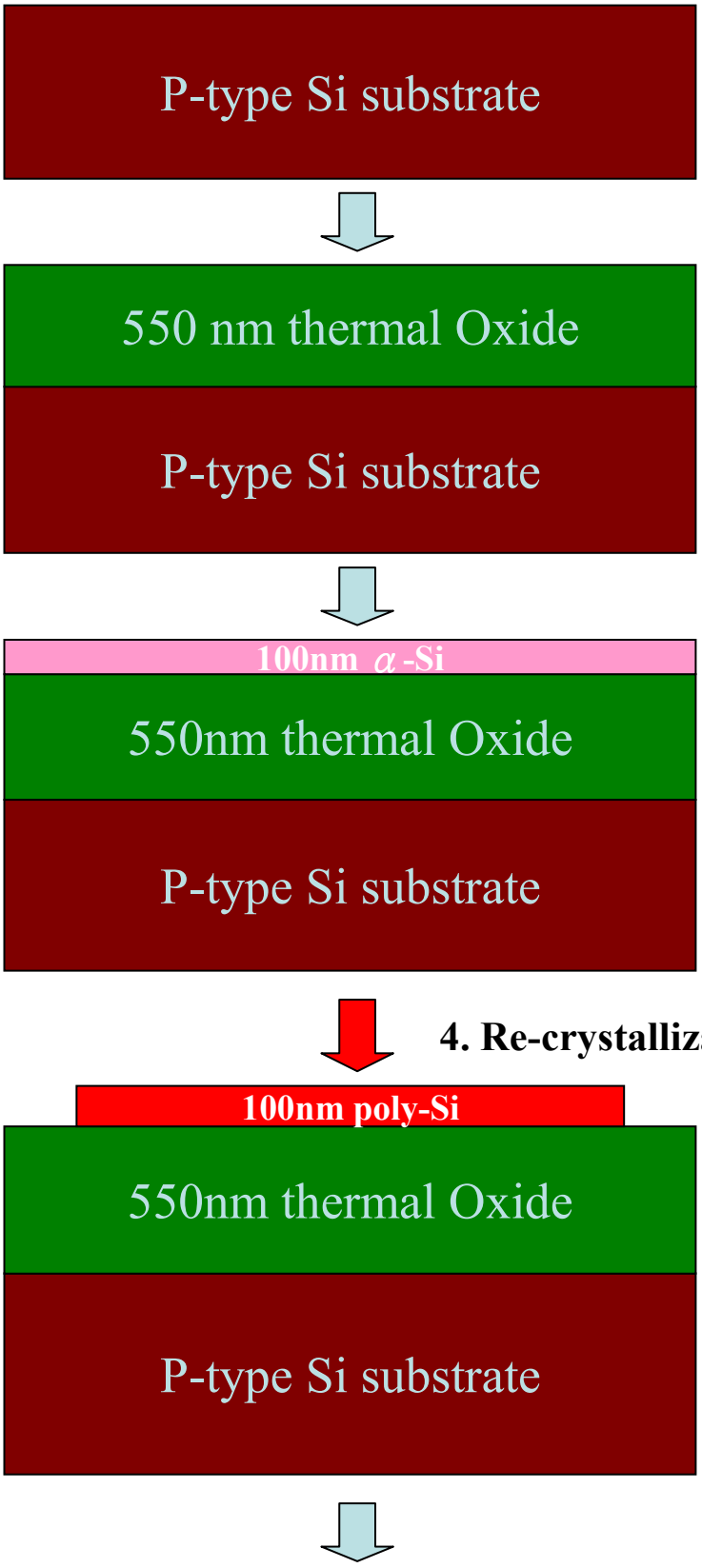
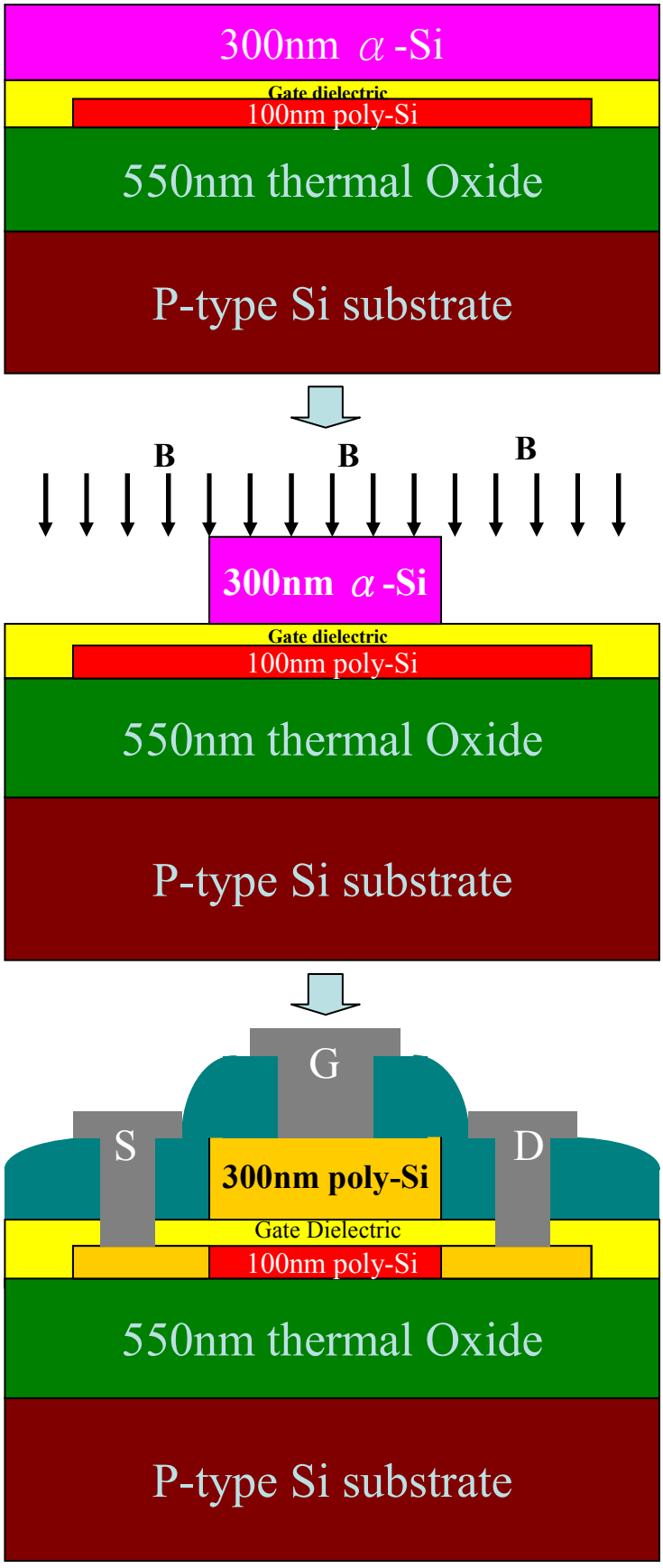


Figure 3-1 Schematic flow charts for the fabrication of poly-Si TFTs.

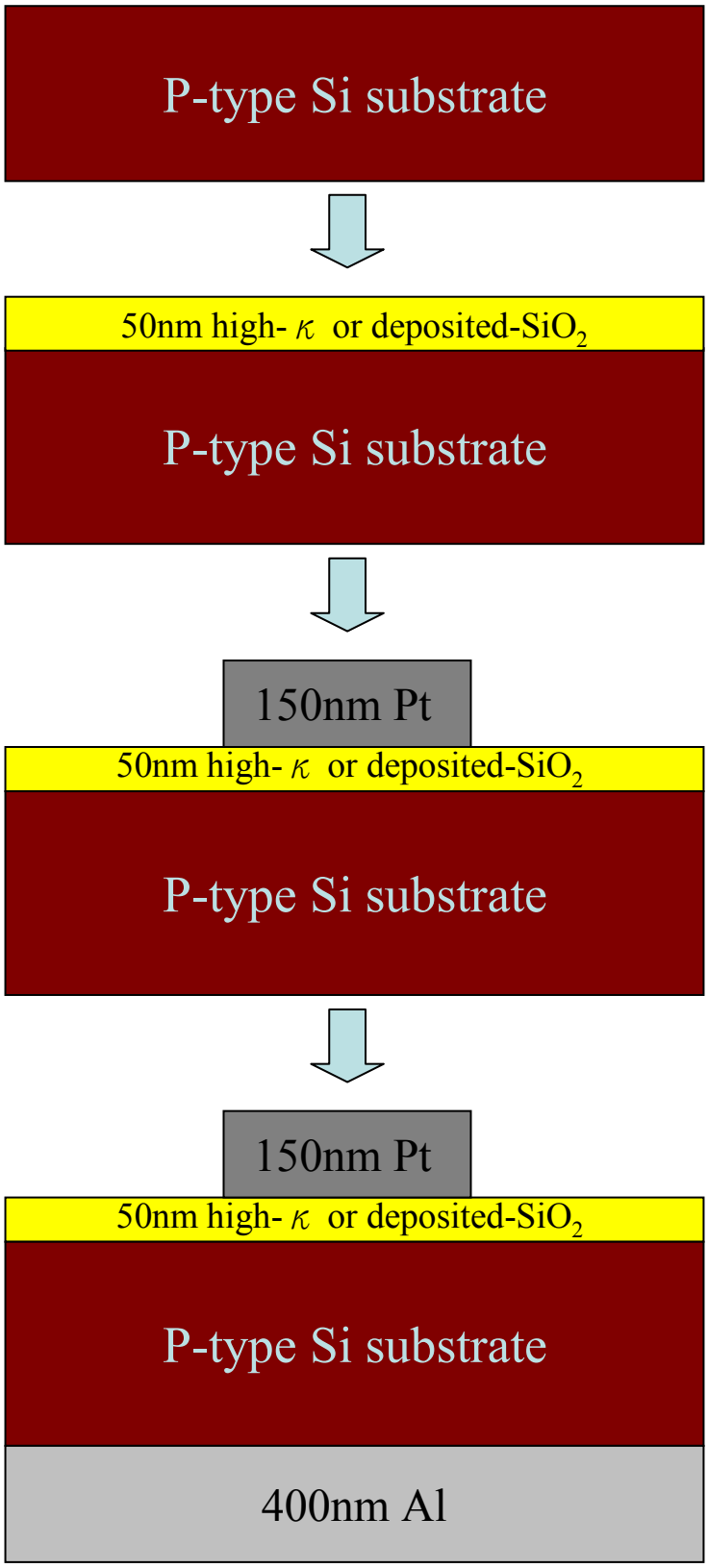


6. 50nm Gate dielectrics deposition by AVD or LPCVD systems.
7. 300nm amorphous-Si date deposition by LPCVD system.

8. Amorphous-Si gate definition (Mask 2).
9. Ion implantation to gate and channel.

10. Amorphous-Si gate re-crystallization and dopant activation (600°C, N_2, 24 hr)
11. Passivation layer deposition by PECVD system and contact hole definiyion (Mask 3).
12. 500nm Al-Si-Cu deposition by PVD system and netal-pad definition (Mask 4).
13. Forming gas sintering, 400°C, 30 min.

Figure 3-1 Schematic flow charts for the fabrication of poly-Si TFTs.



1. Si substrate

2. 50nm gate dielectrics deposition by AVD or LPCVD systems.
3. Annealing by LPCVD system at 600°C, 24hr, in N_2 ambient.

4. Top Pt (150nm) electrode deposition by sputter system through shadow mask.

5. Backside Al (400nm) electrode deposition by thermal coater system.
6. Annealing by furnace system at 400°C, 30 min., in N_2 ambient.

Figure 3-2 Schematic flow charts for the fabrication of capacitors.

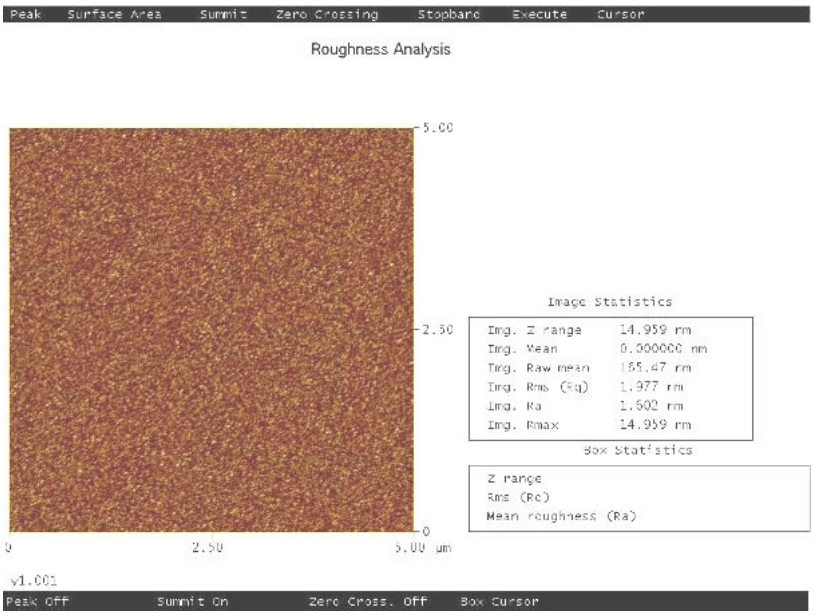


Figure 3-3(a) Atomic force microscope (AFM) image of the HfO_2 film. The samples was annealed in furnace at 600°C in N_2 ambient for 24 hr. The thickness is around 50nm.

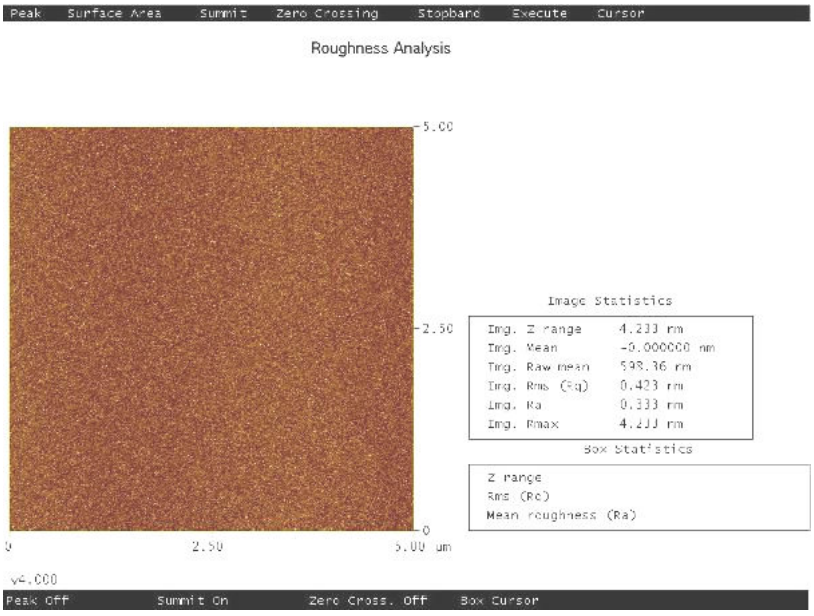


Figure 3-3(b) Atomic force microscope (AFM) image of the $HfSiO_x$ film. The sample was annealed in furnace at 600°C in N_2 ambient for 24 hr. The thickness is around 50nm.

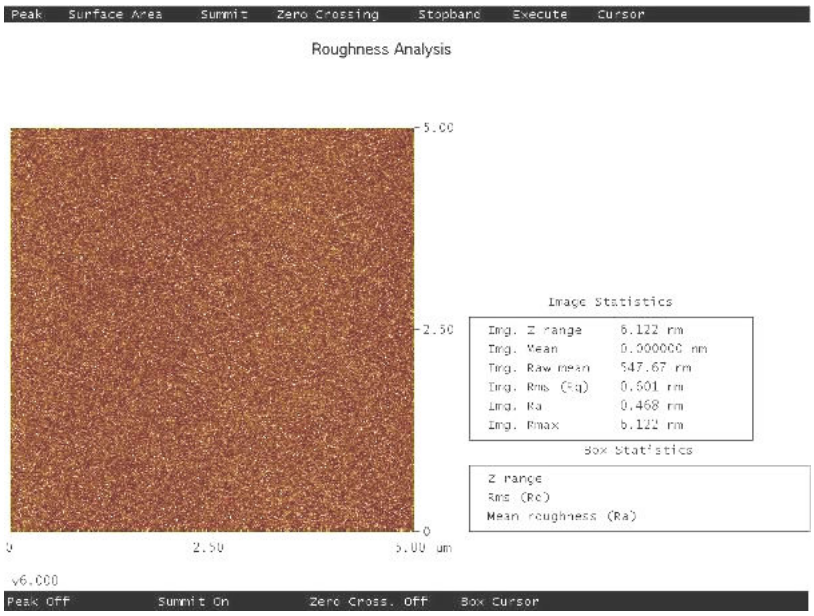


Figure 3-3(c) Atomic force microscope (AFM) image of the deposited-SiO_2 film. The sample was annealed in furnace at 600°C in N_2 ambient for 24 hr. The thickness is around 50nm.

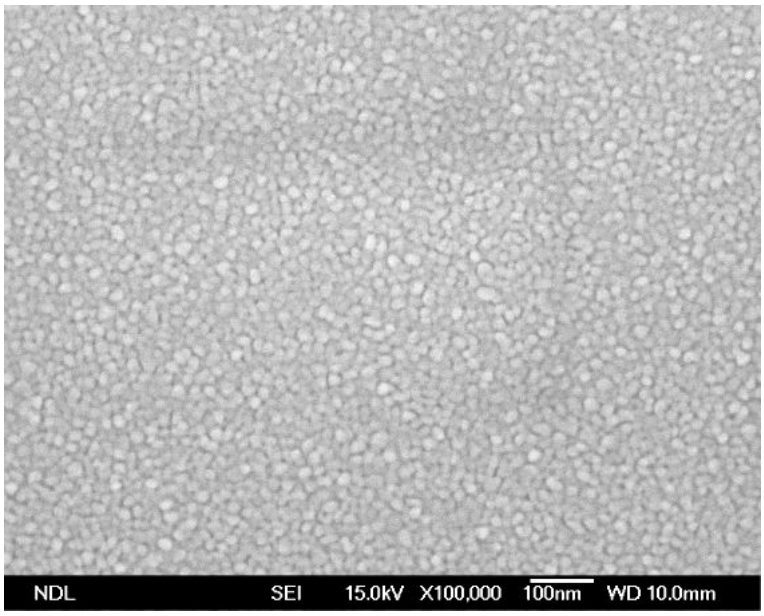


Figure 3-4 Scan Electron Microscope (SEM) image of the HfO_2 film after annealing for 24 h at 600 ˚C in a N_2 ambient. The thickness is around 50nm.

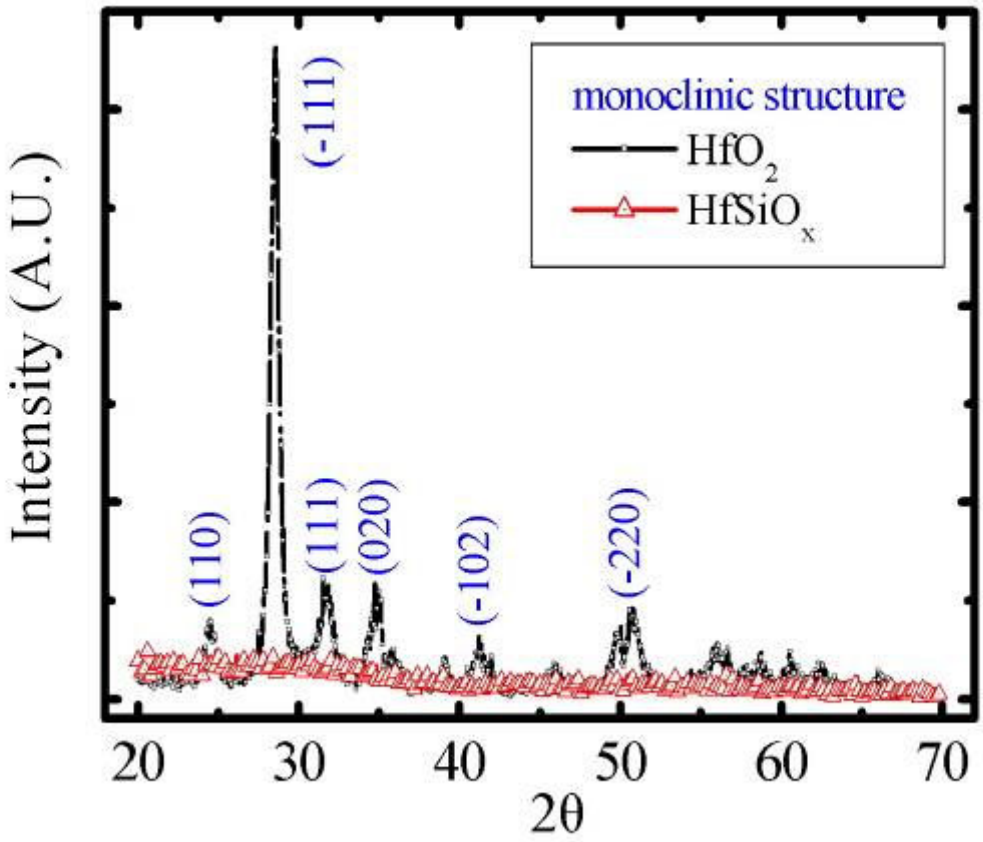
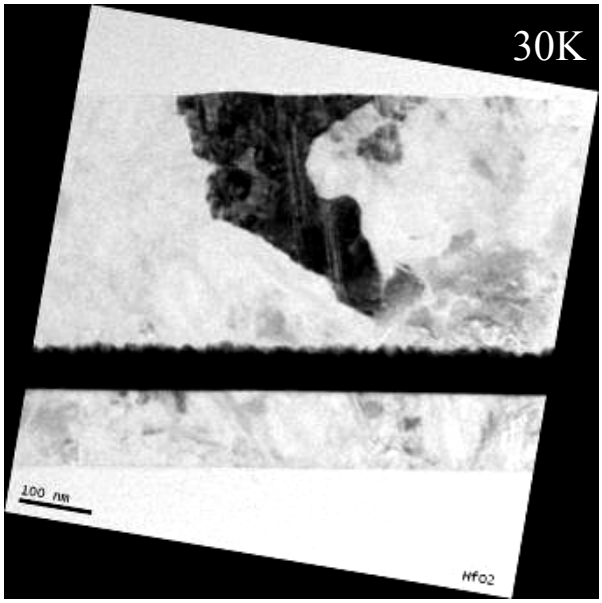
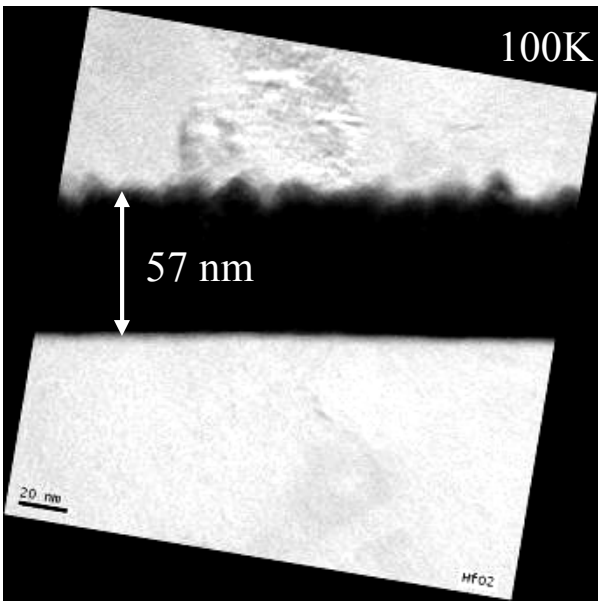


Figure 3-5 X-ray diffraction patterns of HfO_2 and $HfSiO_x$ films after annealing for 24 h at 600 ˚C in a N_2 ambient. The thicknesses of all samples are around 50nm.

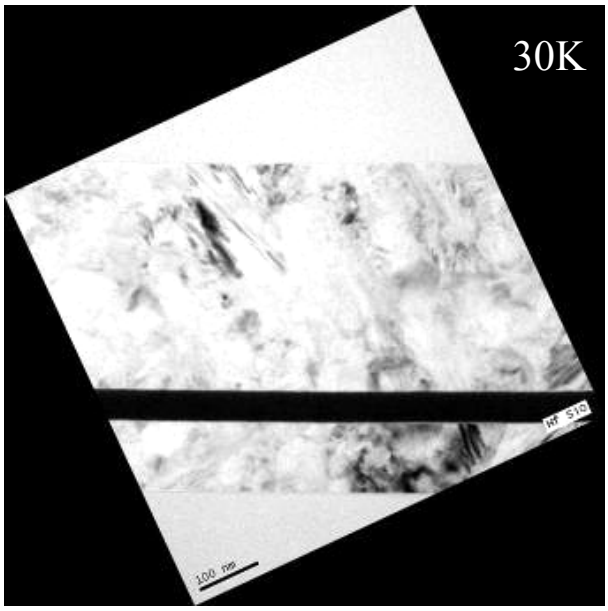


(a)

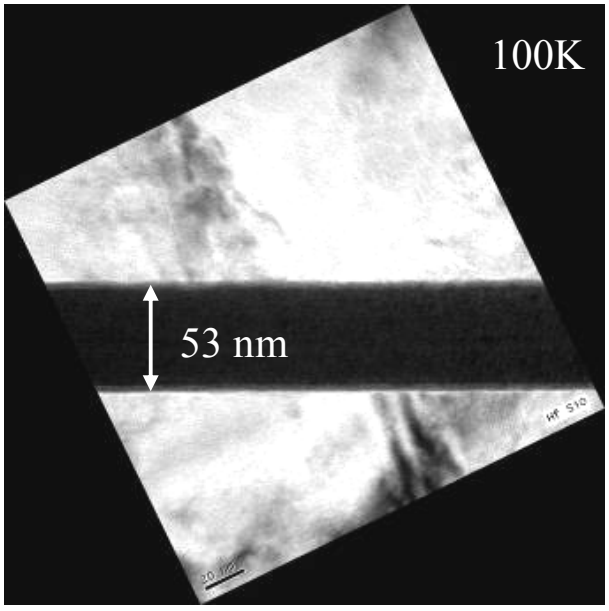


(b)

Figure 3-6 Cross-sectional TEM images of TFTs incorporating HfO_2 gate dielectrics. The magnifications of TEM images are (a) 30k and (b) 100k, respectively.

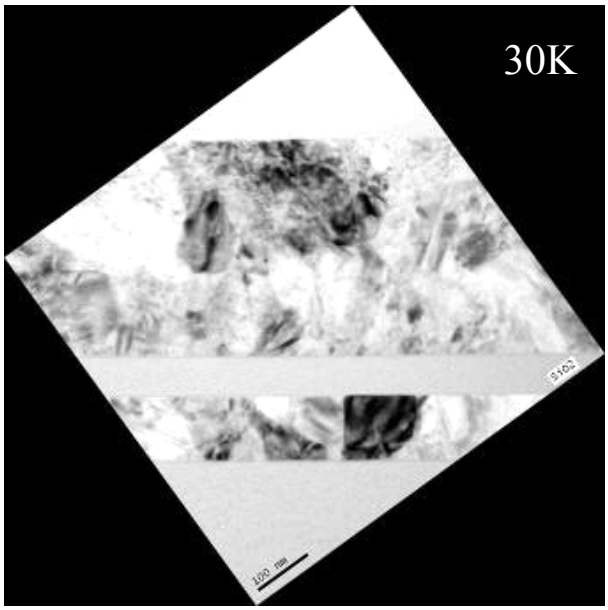


(a)

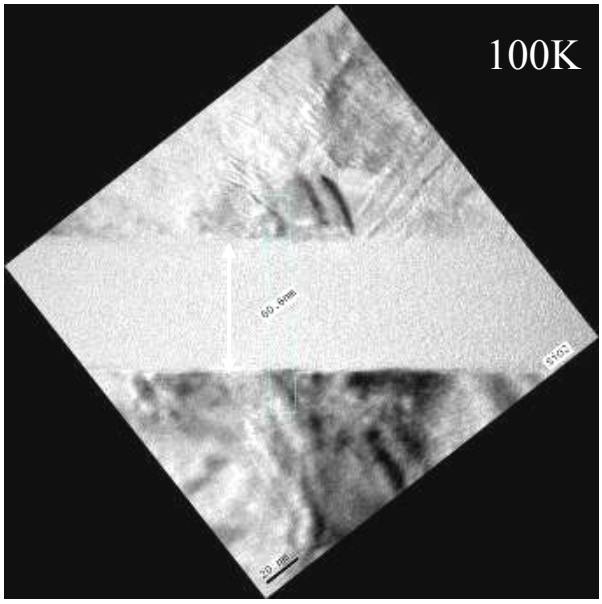


(b)

Figure 3-7 Cross-sectional TEM images of TFTs incorporating $HfSiO_x$ gate dielectrics. The magnifications of TEM images are (a) 30k and (b) 100k, respectively.



(a)



(b)

Figure 3-8 Cross-sectional TEM images of TFTs incorporating deposited-SiO_2 gate dielectrics. The magnifications of TEM images are (a) 30k and (b) 100k, respectively.

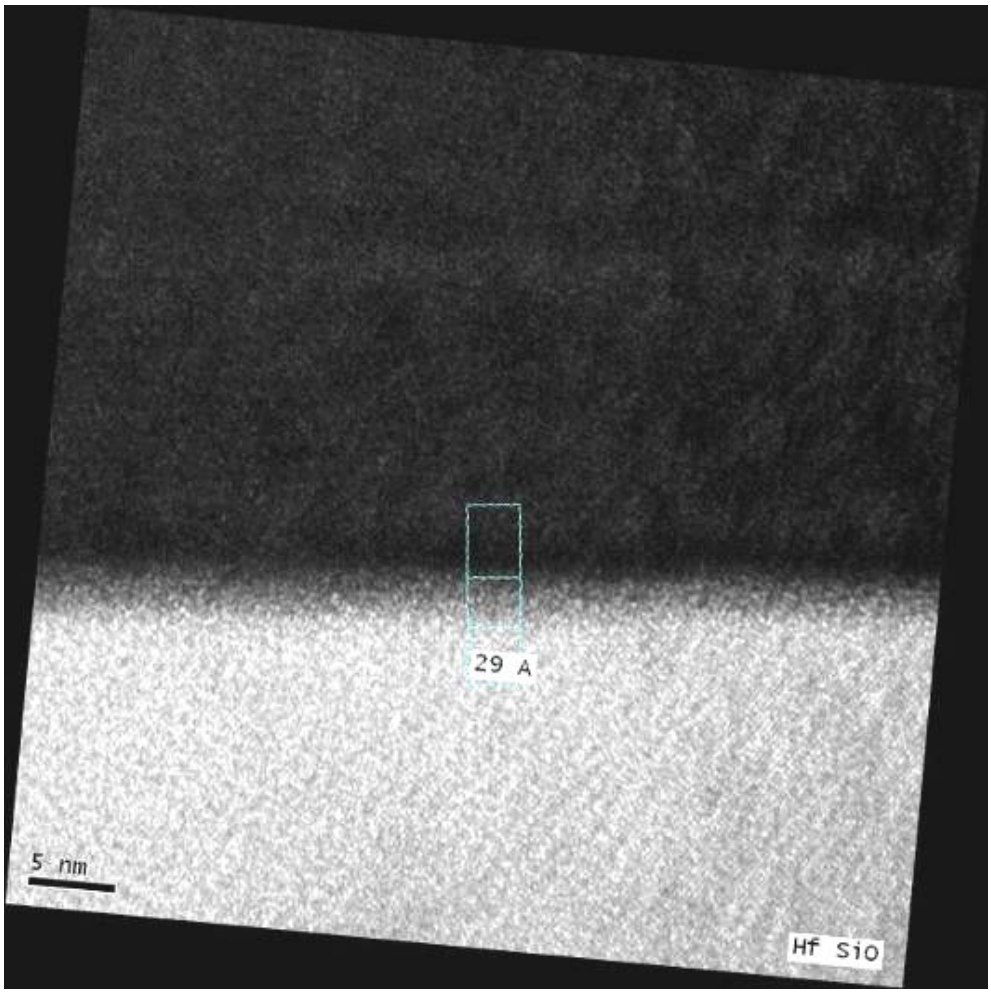


Figure 3-9 Cross-sectional TEM image of the interfacial layer between the $HfSiO_x$ gate dielectric and poly-Si channel.

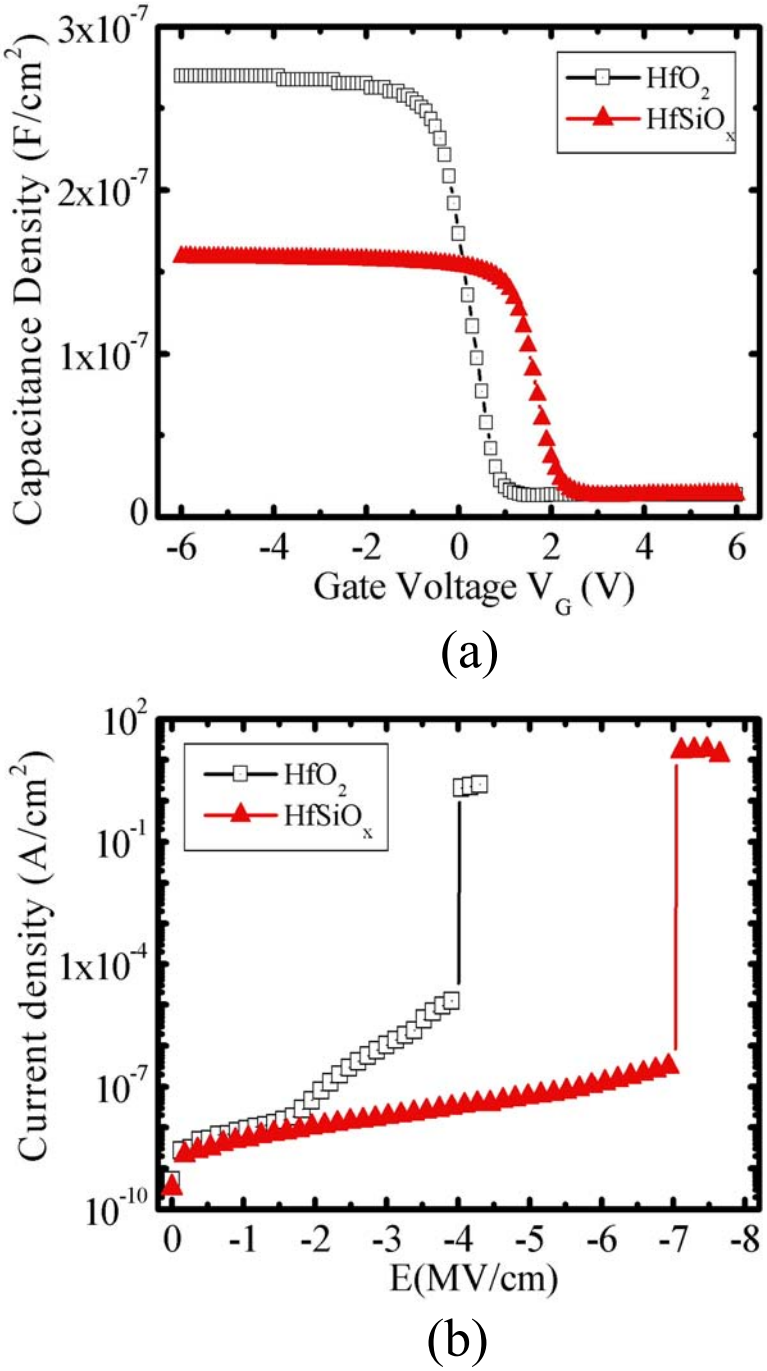
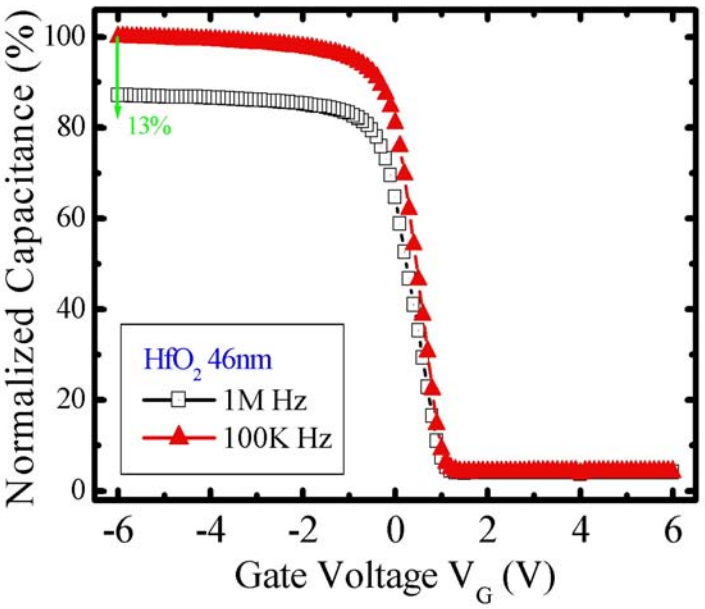
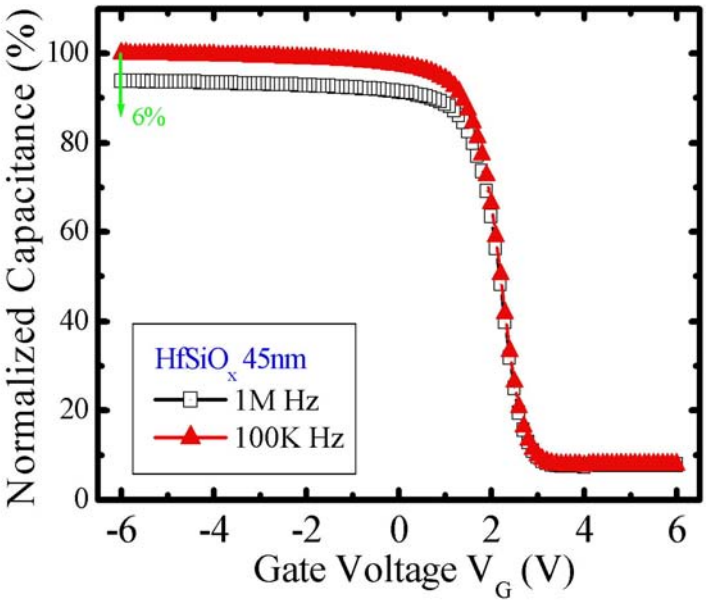


Figure 3-10 Plots of (a) capacitance density versus gate voltage and (b) leakage current density versus electrical field for the HfO_2 and $HfSiO_x$ films obtained after annealing for 24h at 600 ˚C in N_2 ambient.

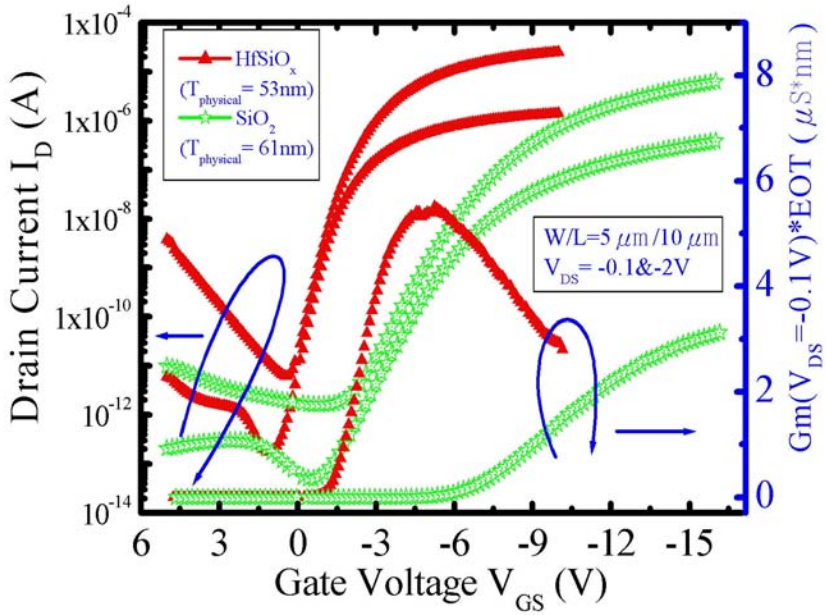


(a)

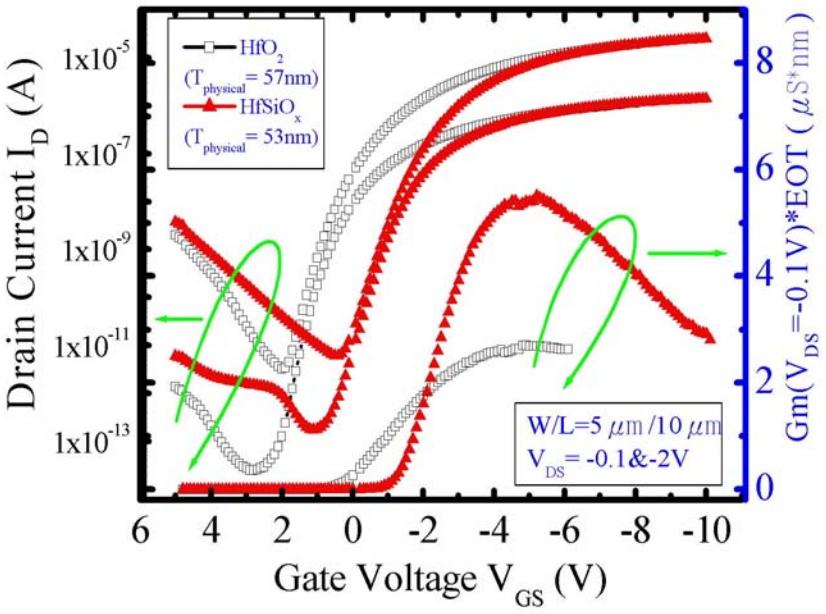


(b)

Figure 3-11 Frequency dispersions of normalized capacitance versus gate voltage for (a) HfO_2 and (b) $HfSiO_x$ films obtained after annealing for 24h at 600 ˚C in N_2 ambient.

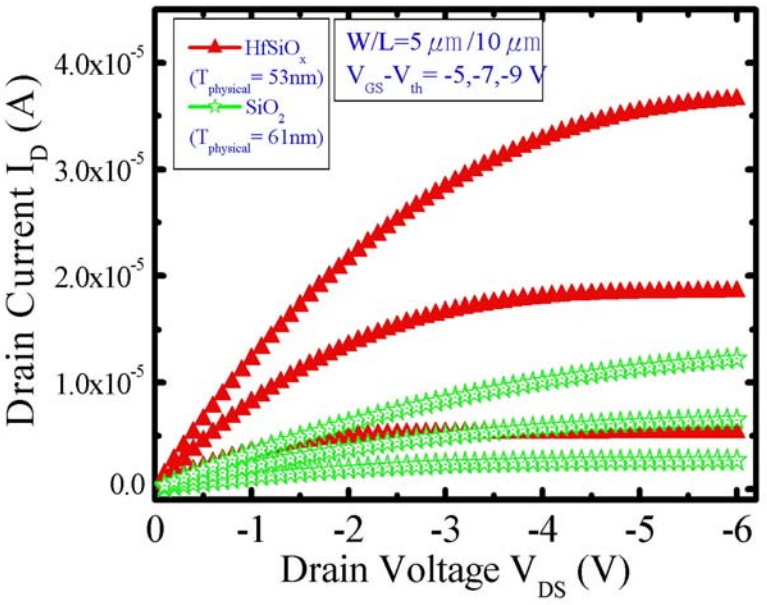


(a)

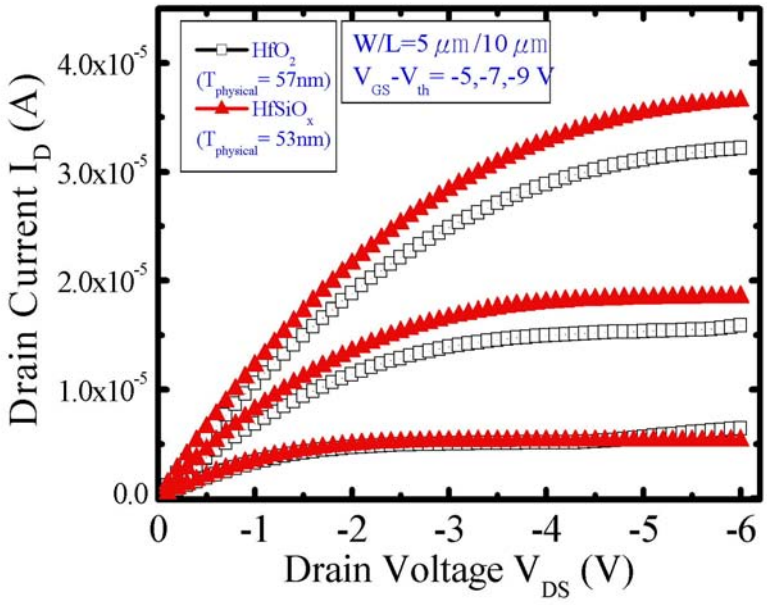


(b)

Figure 3-12 Comparisons of transfer characteristics at V_{DS} of -0.1 and -2 V between TFTs containing (a) $HfSiO_x$ and deposited-SiO_2 and (b) $HfSiO_x$ and HfO_2 as gate dielectrics.



(a)



(b)

Figure 3-13 Comparisons of output characteristics at V_{DS} of -0.1 and -2 V between TFTs containing (a) $HfSiO_x$ and deposited-SiO_2 and (b) $HfSiO_x$ and HfO_2 as gate dielectrics.

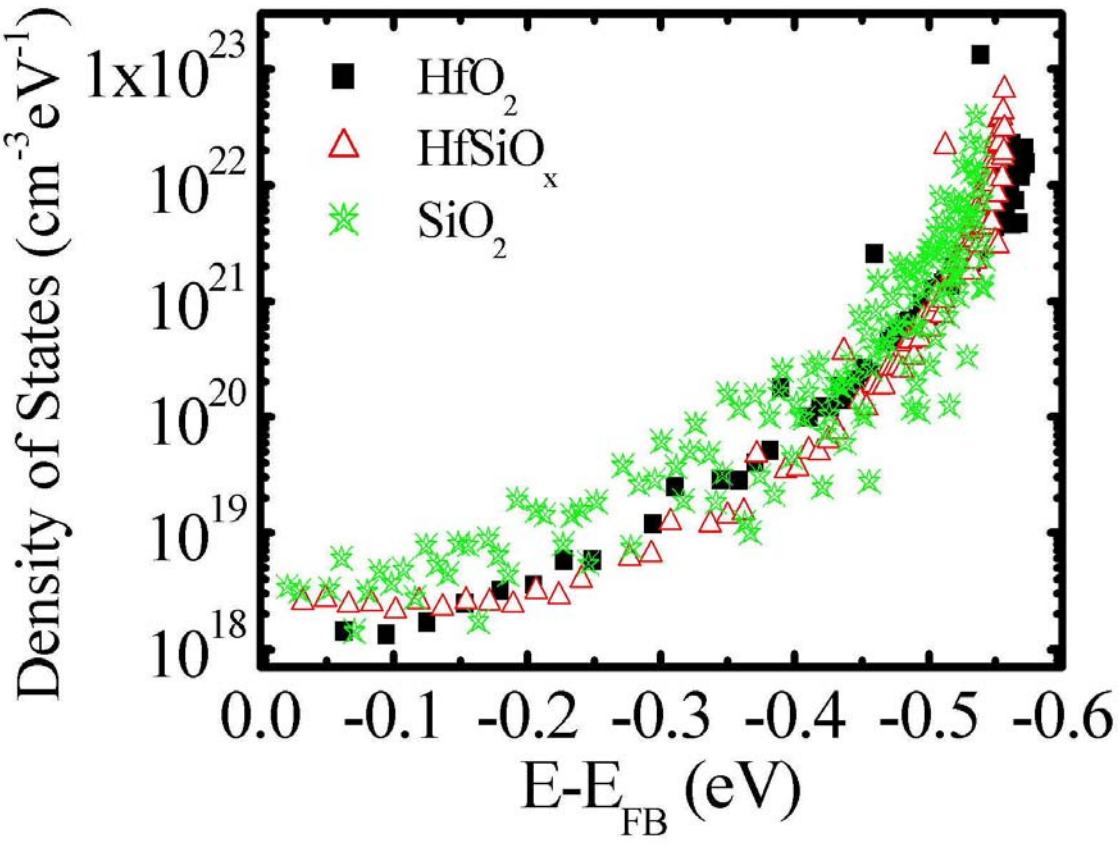
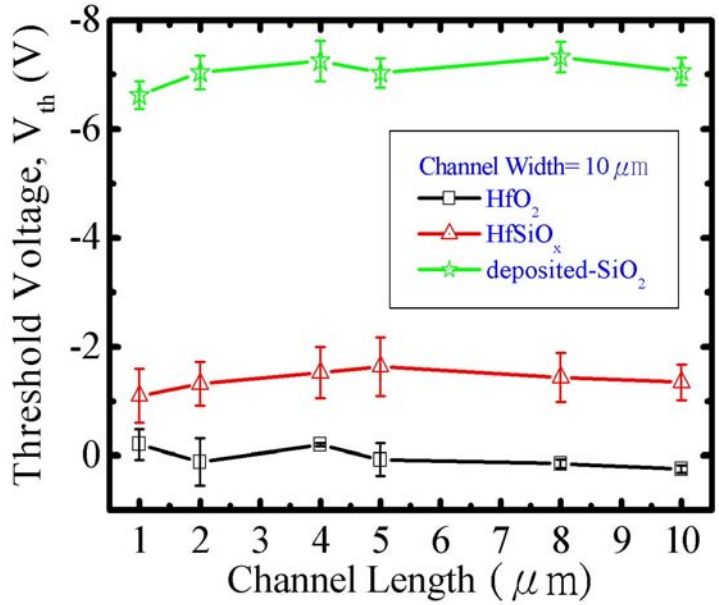
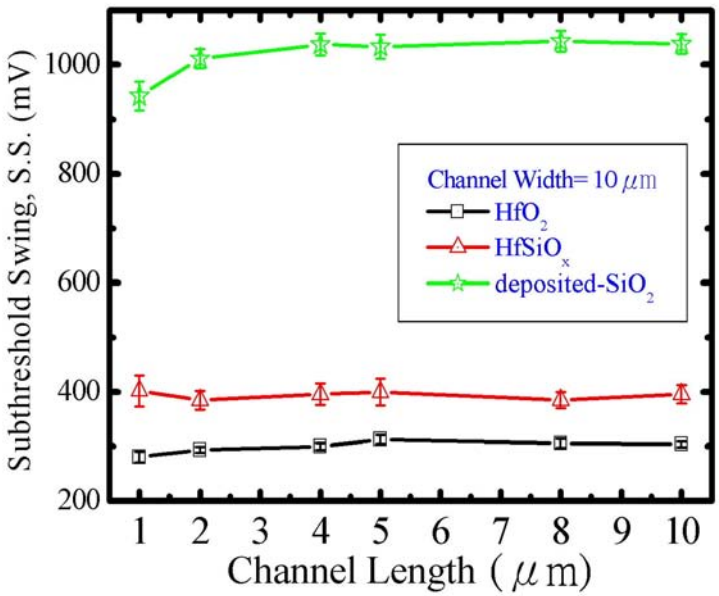


Figure 3-14 Densities of states extracted from transfer characteristics (V_{DS} = -0.1 V) of poly-Si TFTs incorporating various gate dielectrics.

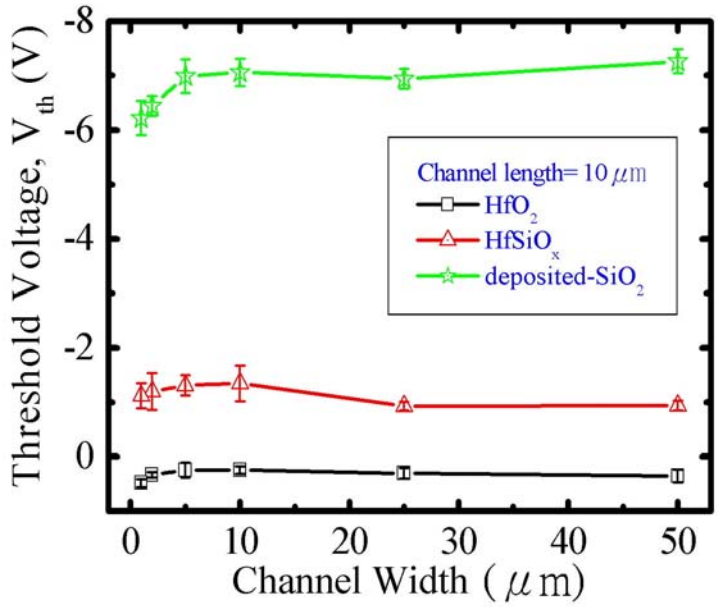


(a)

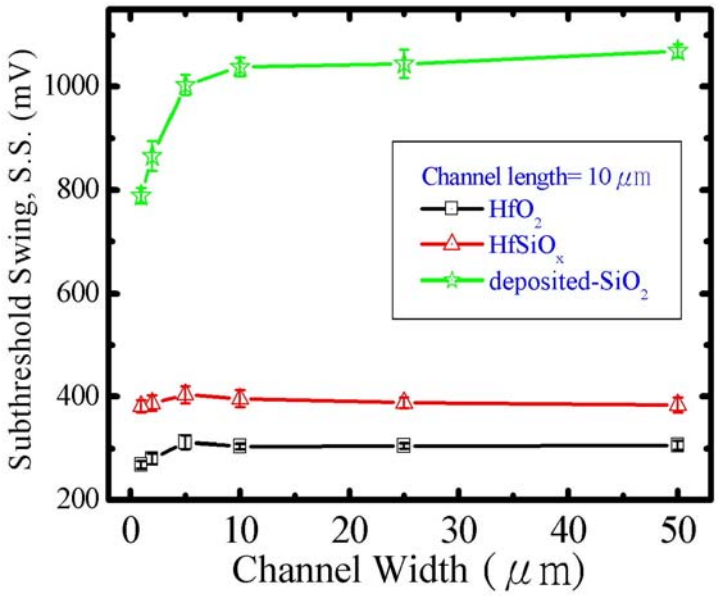


(b)

Figure 3-15 (a) Threshold voltage and (b) subthreshold swing versus channel length for devices with different gate dielectrics.

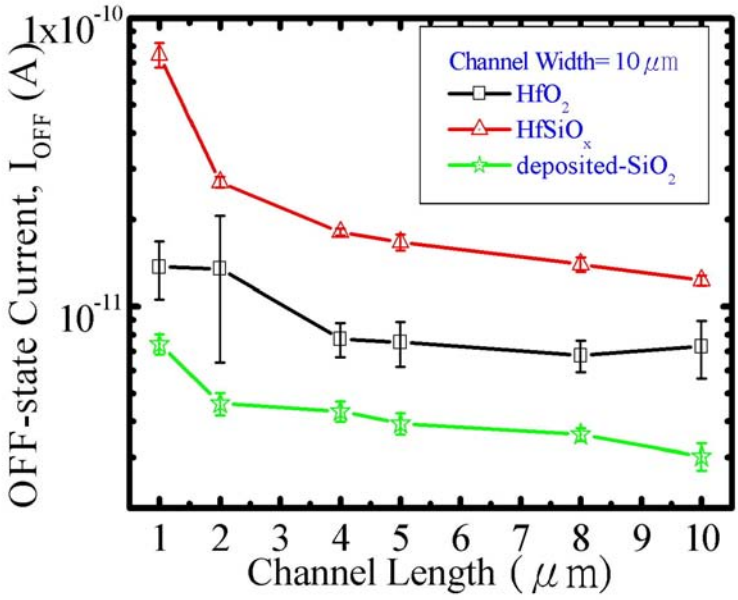


(a)

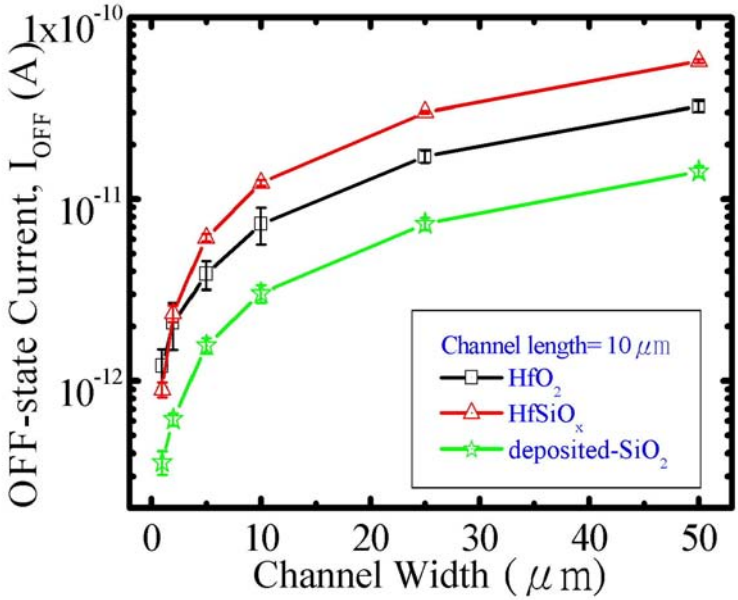


(b)

Figure 3-16 (a) Threshold voltage and (b) subthreshold swing versus channel width for devices with different gate dielectrics.

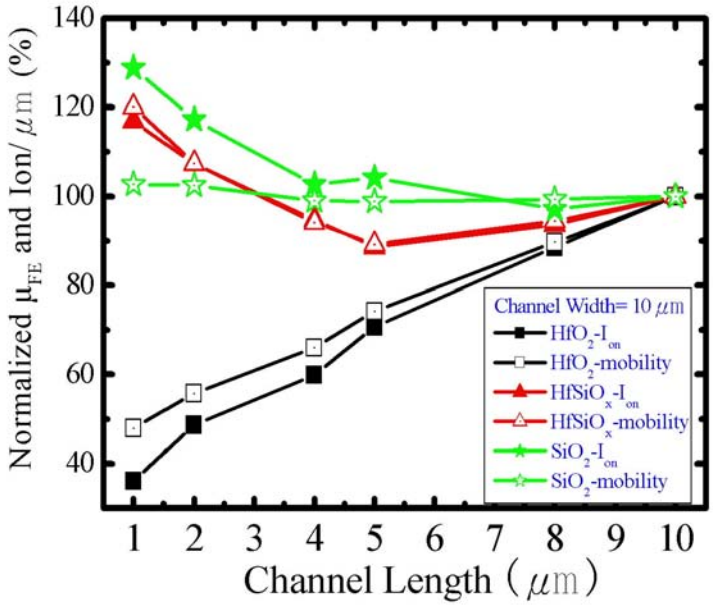


(a)

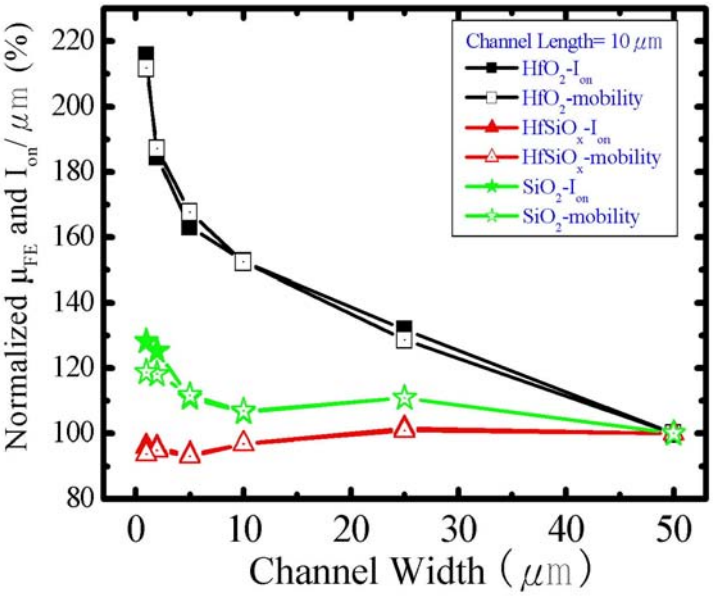


(b)

Figure 3-17 Off-state current versus (a) channel length and (b) channel width for devices with different gate dielectrics.



(a)



(b)

Figure 3-18 Normalized field-effect mobility and drive current versus (a) channel length and (b) channel width for devices with different gate dielectrics.

Chapter 4
Mobility, Off-State Current, and Reliability Study of the Newly-Developed TFTs

4-1 Introduction

To achieve the goal that the display driving circuits contain high-performance TFTs capable of operating at lower voltages while delivering higher drive currents, advanced high-κ materials have been proposed as the new choice of gate dielectric for poly-TFTs. In the previous chapter, low-temperature-compatible p-channel polycrystalline-silicon thin-film transistors (poly-Si TFTs) using high-κ gate dielectrics are fabricated successfully and exhibit excellent device performance. In this chapter, we focus on the electrical characteristics and reliability of these poly-Si TFTs.

First of all, possible mobility degradation mechanisms of TFTs using HfO_2 gate dielectric will be discussed. The reduced mobility in MISFETs is one of the main issues that prevent the use of high-κ gate stacks in conventional silicon process. Several scattering sources have been identified as being responsible for the reduced mobility including Coulomb scattering [4.1]-[4.3], remote-Coulomb scattering [4.4]-[4.5], soft-phonon scattering [4.6]-[4.9], remote-phonons scattering [4.10]-[4.11], fixed charge scattering [4.12]-[4.13], remote-surface roughness scattering [4.14], and crystallization scattering [4.15]. However, the exact origin of the mobility degradation is still unclear. In section 4-2, we employ these possible sources of scattering to analyze our measured data and try to clarify the mobility degradation mechanism of poly-Si TFTs using HfO_2 gate dielectric.

Secondly, the leakage current behaviors for devices with different gate dielectrics

are investigated. Although TFTs incorporating high-κ gate dielectrics exhibit better on-state electrical characteristics than conventional TFTs containing deposited-SiO_2, much severe effects of gate-induced drain leakage (GIDL) are clearly evident in the transfer characteristics of high-κ TFTs. Poly-Si TFTs using high-κ gate dielectrics show deteriorated off-state current and the leakage current mechanism will be discussed in detail.

Finally, we have also studied the instability of these TFTs under negative bias temperature instability (NBTI) stress. The NBTI effect, which is mainly attributed to the generation of interface trap states and fixed oxide charges, has been found to be an important reliability concern in p-channel MOSFETs and widely investigated [4.16]-[4.20]. In poly-Si TFTs, due to the poor thermal conductively of the glass substrate and high operation voltage, the NBTI effect is even more important in the reliability issues. Due to the grain boundary in the channel regions and much severe gate induced drain leakage (GIDL) effect of poly-Si TFTs, the NBTI degradation mechanism in poly-Si TFTs may be different from that in conventional MOSFETs. By measuring and analyzing the transfer characteristics before and after stressing for various stress times and temperatures, we characterize the effects of NBTI on poly-Si TFTs incorporating high-κ dielectrics.

4-2 Device Fabrications

Self-aligned top-gated p-channel poly-Si TFTs were fabricated and the detail process flow was already illustrated in previous chapter. First, a 550nm-thick thermal oxide was grown on Si wafers in a furnace to simulate the glass substrate. Next, a 100nm-thick amorphous silicon layer was deposited through the dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550°C. Subsequently, solid phase crystallization (SPC) was performed at 600°C for 24 h in N_2 ambient to induce

the crystallization of amorphous silicon. Individual active regions were then patterned by lithography and defined by dry etching. After cleaning, various gate dielectrics (each 60nm thick) were deposited. Specifically, HfO_2 and $HfSiO_x$ films were deposited through atomic vapor deposition (AVD) using an AIXTRON Tricent system at a substrate temperature of 500°C. The $Hf[OC(CH_3)_3]_2(mmp)_2$ precursor, $Si[OC(CH_3)_3]_2(mmp)_2$ precursor and oxygen gas were employed as Hf, Si, and O sources, respectively. The as-deposited oxide, which served as the control sample, was prepared through LPCVD at 700°C using tetraethyloxysilane (TEOS) as the precursor. All wafers were then subjected to the deposition of a 300nm-thick amorphous silicon layer, which served as the gate electrode, through LPCVD at 550°C. Gate electrodes were then patterned and the source, drain, and gate regions were doped through self-aligned boron ion implantation (dosage: 5×10^{15} ions/cm^2; energy: 15 keV). After formation of the source and drain, the dopant was activated at 600°C for 24 h in N_2 ambient. Following that, 500nm SiO_2 was deposited by PECVD as the interlayer dielectric. Finally, contact holes were opened and 550nm AiSiCu alloy was deposited and defined. Wafers were then sintered at 400^{o}C for 30 min in forming gas to complete the fabrication. Device measurements were performed using a Keithley 4200 semiconductor characterization system and a HP 4156A precision semiconductor parameter analyzer. The field effect mobility, which was extracted from the maximum transconductance (G_m), and the S.S. were measured at V_{DS} of -0.1 V. The value of the SS was extracted from the maximum slope of the I_D-V_{GS} characteristics. The threshold voltage was defined as the gate voltage at which the drain current reached a normalized drain current (I_D) equals to (W/L) $\times 10^{-8}$ A at V_{DS} of -0.1 V, where W is the drawn channel width and L is the drawn channel length. To clarify the mechanisms of the mobility degradation and leakage current, devices were measured at various temperatures (ranging from -175 to 125^{o}C). During NBTI stressing, the substrate was

heated to the stress temperature (ranging from 25 to 100°C) and then the stress bias of 2 MV/cm was applied to the gate with the source and drain grounded. The stress was removed periodically to measure the basic device characteristics and to characterize the NBTI effect; all measurements were performed at the stress temperature.

4-3 Possible Mobility Degradation Mechanisms of High-κ TFTs

According to Matthiessen' rule, the field-effect mobility of poly-Si TFTs can be described by the following equation:

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_{GB}} + \frac{1}{\mu_{ADD}} \qquad (4.1)$$

where C= Coulomb scattering, PH= phonon scattering, SR= surface roughness scattering, GB= grain-boundary scattering ,and ADD= additional scattering. The mobility is limited by different mechanisms at different electric fields and temperatures, as shown in Figure 4-1. At low fields, the mobility is limited by Coulomb scattering by trapped charges in the gate-dielectric/channel or gate-dielectric/gate-electrode interface; at moderate field, the mobility is limited by phonon scattering and at high field by surface roughness scattering. For temperature dependences, phonon scattering would be enhanced apparently as the temperature is raised because the phonon numbers increase with temperature. While scattering of the grain-boundary decreases as the temperature increases because carrier transportation across the potential barrier of the grain boundary belongs to the thermal activated process. Besides the well-known scattering mechanism, the additional scatterings had been already found for the devices using high-κ gate dielectrics and the other possible origins is illustrated in Figure 4-2 [4.21]. Figure 4-3 displays the relationship between the field-effect mobility (μ_{FE}) and the gate voltage of poly-Si TFTs with different gate dielectrics. Obviously, $HfSiO_x$-TFT depicts much higher μ_{FE} than both HfO_2-TFT and deposited-SiO_2 TFT. The device with

deposited-SiO_2 gate dielectric depicts slowly rising mobility and lower peak of μ_{FE} related to the thicker equivalent oxide thickness (EOT) and inferior deposited-oxide quality. Grain-boundary scattering and Coulomb charge scattering would be main mobility degradation mechanisms for this conventional device. For poly-Si TFTs using high-κ gate dielectrics, the mobility should be improved due to the thinner EOT and superior film quality, such as in the case of $HfSiO_x$-TFTs. However, the HfO_2 TFT depicts the worst mobility among three samples. The poly-Si channels were prepared and crystallized by LPCVD system at the same time, so we thought the grain boundary scattering should be nearly the same among all samples. We believe that the degraded mobility of HfO_2-TFT arises from the additional Coulomb scattering. Several possible mobility degradation mechanisms of HfO_2-TFTs are discussed as follow:

(1) **Remote surface roughness scattering:** From TEM images, as shown in Figure 4-4, all threes devices display smooth bottom-interface (gate-dielectric/poly-Si channel, as shown in the lower part of each picture), but only HfO_2 TFT displays much rougher top-interface (poly-Si gate-electrode/the HfO_2 film, as shown in the upper part of each picture). For first glance, we consider that lower μ_{FE} could be caused by the rougher top-surface. However, a previous literature has reported that the remote interface roughness scattering could be ignored when the oxide thickness is above 10nm [4.22]. Consequently, the degraded mobility of HfO_2-TFTs is not contributed by this scattering.

(2) **Phonon scattering:** From the above description, phonon scattering would dominate in the intermediate transverse field and would be enhanced at higher temperature related to increasing phonons. To clarify this mechanism, all devices were measured at low temperature (ranging from 300^oK to 150^oK). Figure 4-5 displays the relationship between the transcondance (G_m) at various temperatures and the gate voltage of poly-Si TFTs with different high-κ gate dielectrics. Obviously, the

mobility of $HfSiO_x$-TFTs depicts a strong temperature dependence, while HfO_2-TFTs exhibit only weak temperature dependence. Therefore, the phonon scattering would also not be the predominant mobility degradation mechanism of our devices using HfO_2 gate dielectric. Nevertheless, the other extra phonon scattering mechanism has been found to exhibit relatively weak temperature dependence, and is attributed to the soft optical phonons associated with highly polarizable bonds in the HfO_2 layer [4.6], [4.10], [4.23]. These polar modes have a strong coupling to scatter carriers in the Si channel. But the soft phonon scattering is smaller in $HfSiO_4$ film which is covalently bonded without the soft modes. Therefore, the device with Hf-silicate gate insulator shows a higher mobility than the one using HfO_2 gate insulator, which is consistent with our results.

(3) **Coulomb charge scattering:** In comparison with the thermal oxide, the high-κ materials possess high density of traps and fixed charges contained in the bulk or at the high-κ/Si interface. Fixed charges and charged traps give rise to Coulomb scattering and induce the lower mobility in high-κ transistors [4.1]-[4.5], [4.12]-[4.13]. Yamaguchi et al. [4.3] had reported that electron mobility in the MISFETs with Zr-silicate was degraded with increasing Zr concentration, especially at the low electric field region. The result indicated the influence of Coulomb scattering by the high level of bulk charges in Zr-rich films. The other report also mentioned that Coulomb scattering was much severe in the physically thicker HfO_2 films [4.24]. Figure 4-6 displays I_D-V_{GS} characteristics of devices having HfO_2 and $HfSiO_x$ gate dielectrics. The larger V_{FB} shift of the HfO_2 TFTs from zero voltage indicates that larger amount of fixed charges or traps exist in the HfO_2 films or HfO_2 gate-dielectric/poy-Si channel interface. The slow rising of μ_{FE} in HfO_2 TFTs at low electric field is attributed to the severe Coulomb charge scattering, and is shown in

Figure 4-3. Furthermore, the observation that Gm of HfO_2 TFT increases at low electric field as the temperature increases also proves the mobility dependence on Coulomb charge scattering, as shown in Figure 4-7(a). In contrast, $HfSiO_x$ TFT that contains less trapped charges depicts less Coulomb charge scattering and thus shows temperature-independent Gm in the low electric field, as shown in Figure 4-7(b). Therefore, the high-level of trapped charges and fixed charges in HfO_2 films would introduce severe Coulomb charge scattering and might be the predominant mobility degradation mechanism in our devices.

(4) **Crystallization induced scattering:** In our experiments, the device with $HfSiO_x$ gate dielectric exhibits higher carrier mobility than the one with HfO_2 film which suffered from the additional mobility scatterings. Except for the possible scattering mechanisms discussed above, the apparent difference between these two devices is the crystallinity of the HfO_2 and $HfSiO_x$ films. As mentioned in Chapter 3, the HfO_2 film clearly exhibits polycrystalline monoclinic structure after annealing at 600°C for 24 hour in N_2 ambient, whereas the $HfSiO_x$ film still retains its amorphous form. Yamaguchi et al. [4.15] had reported that partially crystallized-HfO_2 portions in the Hf-silicate would be formed after high temperature annealing. Furthermore, the carrier mobility is strongly influenced by the additional Coulomb scattering caused by the partial crystallization in the Hf-silicate, as schematically shown in Figure 4-8. According to this report, we speculate that the additional Coulomb charge scattering would also incur in the polycrystalline HfO_2 films, resulting in the lower mobility of HfO_2 TFTs in our experiments. In contrast, $HfSiO_x$ films could prevent this additional scattering and exhibit better mobility because of the higher thermal stability.

In summary, the additional mobility degradation mobility of poly-Si TFTs using high-κ gate dielectrics in our experiments could be attributed to the trapped charge

scattering, the soft phonon scattering, and the crystallization induced scattering. However, the predominant mobility degradation mechanism is not invariable and could be different from process to process and the type of high-κ materials.

4-4 Origins of Off-State Current among Poly-Si TFTs with Different Gate Dielectrics

Although TFTs incorporating high-κ gate dielectrics exhibit better on-state characteristics than the conventional TFT containing deposited-SiO_2, much severe effects of gate-induced drain leakage (GIDL) are clearly evident in the plots of transfer characteristics of high-κ TFTs, as shown in Figure 4-9. To further clarify the mechanism of the larger off-state current, the activation energies of different gate dielectrics were calculated from I_D-V_{GS} curves obtained at 25, 50, 75, 100, and 125°C. Figures 4-10(a) and (b) present plots of the dependence of activation energy (E_a) on V_{GS} measured at V_{DS} of -0.1 and -2 V, respectively. At the lower value of V_{DS}, the TFT containing HfO_2 depicts the highest activation energy accounting for the observed lowest minimum leakage current. Upon increasing $|V_{GS}|$ in the off-state regime, the activation energy of the TFT incorporating HfO_2 decreases drastically, whereas those containing $HfSiO_x$ and deposited-SiO_2 exhibit smoother decrease in their activation energies. When the value of V_{DS} is -2 V, all TFTs exhibit rapidly decreasing values of E_a upon increasing $|V_{GS}|$. To explain these results, we must consider the leakage mechanisms of poly-Si TFTs in the off-state [4.25]-[4.29]. Typically, the off-state current in poly-Si TFTs can be divided into three parts: (i) in the region of very low $|V_{GS}|$, the increasing off-state current as $|V_{GS}|$ increases is related to the resistive current, which is assumed to be an ohmic current flowing through the polysilicon layer; (ii) in the almost-flat region, the off-state current that does not change with increasing $|V_{GS}|$ is related to the thermal generation current, which was reported to be nearly independent

of $|V_{GS}|$ [4.25]; (iii) in the high-$|V_{GS}|$ region, the increasing off-state current as $|V_{GS}|$ increases is linked to the thermionic field or Frenkel–Poole emission current, which is due to field-enhanced thermal excitation.

Figures 4-11 to 4-13 display the relations between the temperatures and I_D-V_{GS} characteristics of the devices with different gate dielectrics at V_{DS} of -0.1 and -2 V, respectively. In Figure 4-11, we observe clearly that the off-state current is dominated by the resistive current and thermal generation current for the TFT containing deposited-SiO_2 gate dielectric at V_{DS} of -0.1 V. The leakage current related to thermal generation increases monotonously with increasing temperature and is almost V_{GS}-independent. When V_{DS} increases to -2 V, the thermal generation current prevails in the low-$|V_{GS}|$ regime and the Frenkel–Poole emission current preponderates in the high-$|V_{GS}|$ regime. As the measured temperature increases, the thermal generation leakage current dominates again. On the other hand, we found that the off-state current in the $HfSiO_x$ TFT at V_{DS} of -0.1 V is resistive, thermal generation, and Frenkel–Poole emission currents in the low-, intermediate-, and high-$|V_{GS}|$ ranges, respectively; in contrast, only the Frenkel–Poole emission current is present when V_{DS} is -2 V for all $|V_{GS}|$ ranges, as shown in Fig. 4-12. Similarly, the portion of the leakage current related to thermal generation mechanism increases as the measurement temperature goes up. The HfO_2 TFT exhibits similar behavior, although the Frenkel–Poole emission current prevails over the other two currents, even when V_{DS} is -0.1 V, as shown in Fig. 4-13. At high drain voltage, the field emission current of HfO_2 TFT becomes much stronger and is the dominant leakage current even at higher measurement temperatures. We speculate that these results are closely related to the higher values of κ possessed by the high-κ dielectrics. According to Frenkel–Poole emission mechanism, the off-state current is highly dependent on the peak electric field (E_{pk}) at the drain junction, and is dominated by the vertical electric field at the interface; thus

$$I_{FE} \propto \exp\left(\sqrt{E_{pk}}\right) ; \qquad (4.2)$$

$$E_{pk} = \frac{(V_{GS} - V_{DS} - V_{FB})\varepsilon_{\text{gate dielectric}}}{(T_{\text{gate dielectric}}\varepsilon_{Si})},$$

where ε_{Si} and $\varepsilon_{\text{gate dielectric}}$ are the permittivities of Si and the gate dielectric, respectively, V_{FB} is the flat-band voltage defined as minimum I_{DS}, and $T_{\text{gate dielectric}}$ is the physical thickness of the gate dielectric. Poly-Si TFTs incorporating high-κ gate dielectrics definitely exhibit their higher peak electric fields as a result of their higher values of κ (because the physical thicknesses of all the dielectrics are similar), which then cause the rapidly increasing Frenkel–Poole emission current. These results can also be explained by considering the plots of the activation energy. At a low drain-to-gate bias $|V_{DG}|$, the thermal generation current is the dominant leakage current mechanism and the corresponding value of E_a is higher. As $|V_{DG}|$ increases, the Frenkel–Poole emission current gradually becomes the predominant leakage mechanism and the value of E_a, which is most significant for the thermal generation current, decreases rapidly.

As a result, we suggest two approaches to solve the severe leakage problem. One way is to improve the quality of the poly-Si channel. Lower defect density in poly-Si channel could reduce the gate-induced-drain-leakage current. The other way is to employ lightly doped drain (LDD), multi-gate, and offset structures, which can reduce the electric field between the drain and the channel of the TFT, thus suppressing the off-state current when high-κ dielectrics are employed as gate dielectrics.

4-5 Temperature Instability of Poly-Si TFTs with Different Gate Dielectrics

For reliability testing, all devices were measured at various temperatures, ranging from 150°K to 400°K. Figures 4-14(a)-(e) display the electrical characteristics (i.e., V_{th},

S.S., I_{off}, μ_{FE}, and I_{on}, respectively) as a function of measurement temperature for poly-Si TFTs having different gate dielectrics. As shown in Fig. 4-14(a), the devices using high-κ gate dielectrics depict smaller V_{th} shift than the deposited-SiO_2 sample and V_{th} decreases slightly as the temperature increases. This result can be attributed to the increasing carrier numbers at higher temperature, so the device will turn on early. But, a larger V_{th} increase is found in the device with deposited-SiO_2 film at higher temperature. We believe that the degradation is caused by the defect creation related to the inferior quality of the deposited-SiO_2 film. The assumption can be validated by the S.S. measurement, as shown in Fig. 4-14(b). The severe S.S. degradation of the deposited-SiO_2 device indeed indicates that large amounts of interface defects are created at high temperature. In contrast, devices using better quality high-κ films show just slight increase of subthreshold swing. The off-state current as a function of measurement temperatures for various splits are shown in Figure 4-14(c). It can be seen that devices with $HfSiO_x$ and deposited-SiO_2 films exhibit stronger temperature dependence of I_{off} than the one with HfO_2 film. According to the discussion in previous section, the device using HfO_2 films with higher κ value would depict higher portion of field-emission current and weaker temperature dependence of off-state current. In figure 4-14(d), the $HfSiO_x$-TFT depicts apparent mobility increase at lower temperature due to reduced phonon scattering. Compared with the deposited-SiO_2 sample, devices using high-κ gate dielectrics exhibit less mobility degradations at high temperature. The variation of the drive current, as shown in Figure 4-14(e), also follows similar trend. Finally, the temperature instability was also tested in the devices with different dimensions. The tendencies of the variations of electrical characteristics, including V_{th}, S.S., and I_{off}, are similar and nearly independent of the device dimensions, as shown in Figures 4-15 to 4-17. Nevertheless, the variations of field-effect mobility and drive current exhibit distinct trends among varied dimensions for devices with different gate

dielectrics. In Figure 4-15(d), it can be found that μ_{FE} of HfO_2-TFTs was nearly constant in larger dimension (W/L= 50/10μm), which was different with other two dimensions. The behavior could be explained by that reduced grain-boundary scattering at high temperature would become more apparent related to the plenty numbers of poly-grains in larger dimension. So, the mobility degradation of HfO_2-TFTs caused by Coulomb scattering would be eliminated by the reduced grain-boundary scattering, and the drive current increased slightly as the temperature went high. In contrast, deposited-SiO_2 TFTs depicted severe drive current degradation as the device dimension became larger, as shown in figure 4-17(e). As mention above, the defect creation related to the inferior quality of the deposited-SiO_2 film would be enhanced at higher temperature. In addition, the density of state in the grain-boundary would also increase in the device with larger dimension. As a result, the degradation of drive current would be deteriorated by larger amount of created defects at higher temperature and larger dimension. Briefly, we believe that poly-Si TFTs incorporating high-κ gate dielectrics exhibit better temperature immunity than the conventional TFT containing deposited-SiO_2 film.

4-6 Negative-Bias-Temperature-Instability (NBTI) of Poly-Si TFTs with Different Gate Dielectrics

We have also studied the instability of low-temperature p-channel poly-Si TFTs with various gate dielectrics under NBTI stress. Figures 4-18 (a)-(d) show V_{th}, S.S., μ_{FE}, and the drive current, respectively, as functions of the NBTI stress time. Initially, the deposited-SiO_2 TFT displays smaller shift in V_{th} and the drive current degradation than the other two splits. In contrast, TFTs incorporating high-κ dielectrics exhibit less degradation than the deposited-SiO_2 TFT for all measured parameters when the stress period prolongs; specifically, the $HfSiO_x$ TFT exhibits the strongest immunity against NBTI stress. We believe that these results are closely related to the fact that the trapped

charge accumulates in the high-κ dielectric via filling, rather than through generation, which occurs in the deposited-SiO_2 [4.30]-[4.31]. According to previous reports [4.16]-[4.20], the degradation of both S.S. and μ_{FE} is attributed mainly to interface-trap-state generation. The NBTI stress, which causes bonds to break at the gate-dielectric/poly-Si channel interface and generates more dangling bonds, results in the increased number of interface trap states. Our results confirm that the $HfSiO_x$ film possesses superior interface quality; i.e., fewer traps would be created during the application of stress. Based on formula (3.1), we estimated the N_{it} increment to be only 6.43% for the $HfSiO_x$ TFT after stressing. This value was much lower than those for the TFTs containing the HfO_2 and deposited-SiO_2 films (both are around 19%). In addition, V_{th} shift in poly-Si TFTs caused by the NBTI stress is also governed by the generation of grain-boundary traps in the channel [4.20]. To investigate the effects of grain-boundary traps during NBTI stress, we applied the Levinson–Proano method to estimate the grain-boundary trap densities (N_{trap}) for all samples [4.32]-[4.33]. Figures 4-19 (a)-(c) present the plots of $\ln[I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ at V_{DS} of -0.1 V and at high V_{GS}, where the flat-band voltage (V_{FB}) is defined as the gate voltage that yields the minimum drain current from the transfer characteristics. We found that the $HfSiO_x$ TFT not only provides the lowest initial value of N_{trap} but also the highest immunity against N_{trap} creation during stressing, although the detailed mechanism is not clear at present. As a consequence, we expect less degradation of the drive current for $HfSiO_x$ TFTs because the drive current degradation is mainly attributed to the V_{th} shift and the decrease in μ_{FE}. Figures 4-20 (a)-(d) display V_{th}, SS, μ_{FE}, and the drive current, respectively, as a function of the NBTI stress time at 100°C. Although the tendencies are similar to those revealed at room temperature, we note that TFTs containing high-κ dielectrics are relatively insensitive to high temperature, whereas the deterioration of the deposited-SiO_2 TFT is dramatic. This feature seems very favorable for TFTs for display

applications because glass substrates have very poor thermal conductivity. As a result, using high-κ gate dielectrics can not only enhance the performance of poly-Si TFTs but also improve their reliability over those incorporating conventional deposited-SiO_2. In addition, $HfSiO_x$ appears to have better potential over HfO_2 for use as a future gate dielectric in low-temperature-compatible poly-Si TFTs.

4-7 Summary

In this chapter, the mechanisms of mobility degradation and leakage current of poly-Si TFTs incorporating high-κ gate dielectrics are investigated. The lower mobility of HfO_2-TFTs is attributed to the additional (trapped charges, soft phonons, and crystallization) scatterings. In contrast, $HfSiO_x$ films can prevent this additional scattering and exhibit the improved mobility because of the higher thermal stability. Nevertheless, the higher electric field caused by high-κ devices would induce severe GIDL current. Hence, the LDD or offset structures are suggested to suppress the leakage current. The temperature instability and NBTI were also studied for the reliability testing. Our results show that using high-κ gate dielectrics can not only enhance the performance of poly-Si TFTs but also improve their reliability over those incorporating conventional deposited-SiO_2.

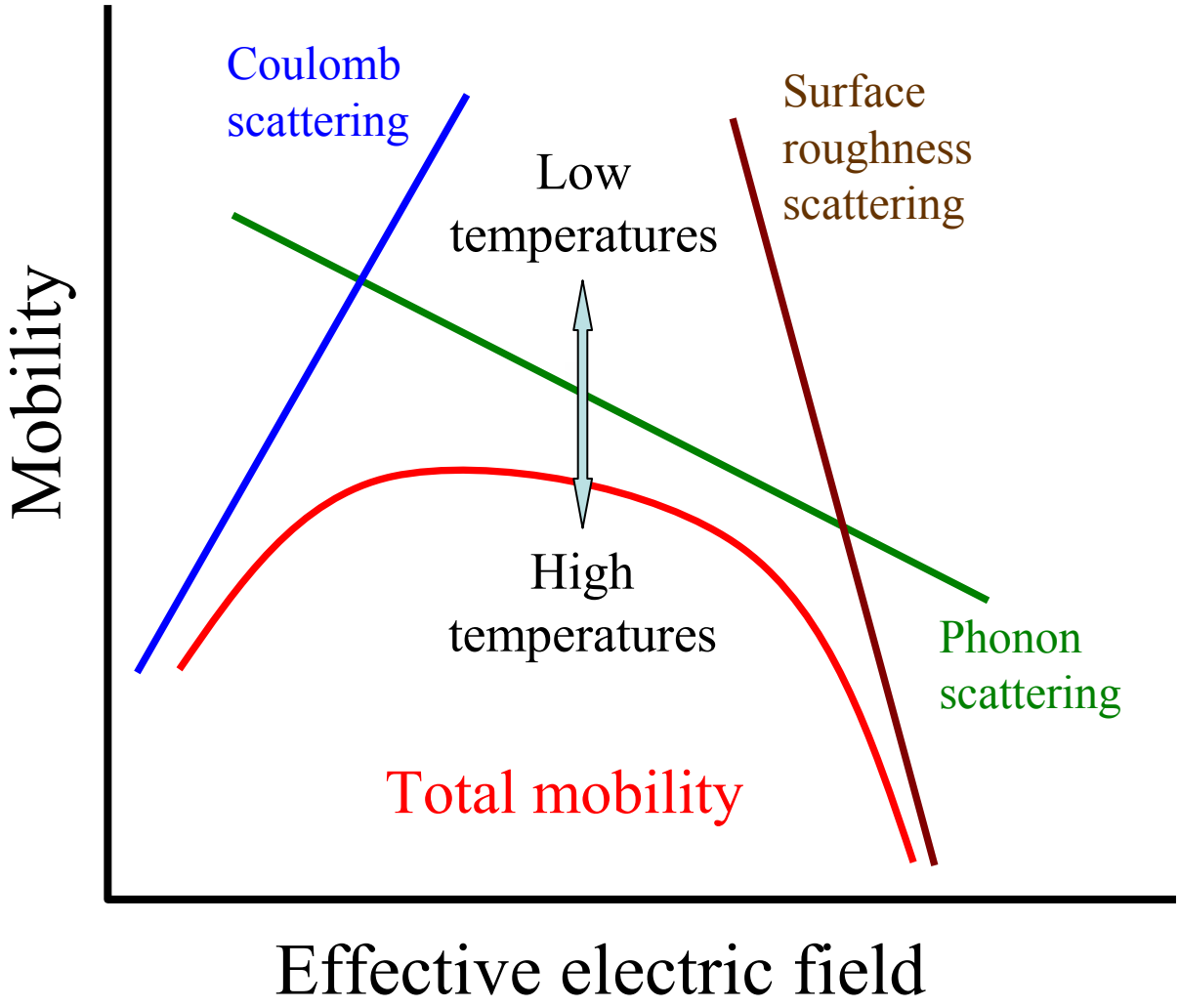


Figure 4-1 Schematic for carrier mobility as a function of vertical electric field for MOSFETs in the universal mobility model.

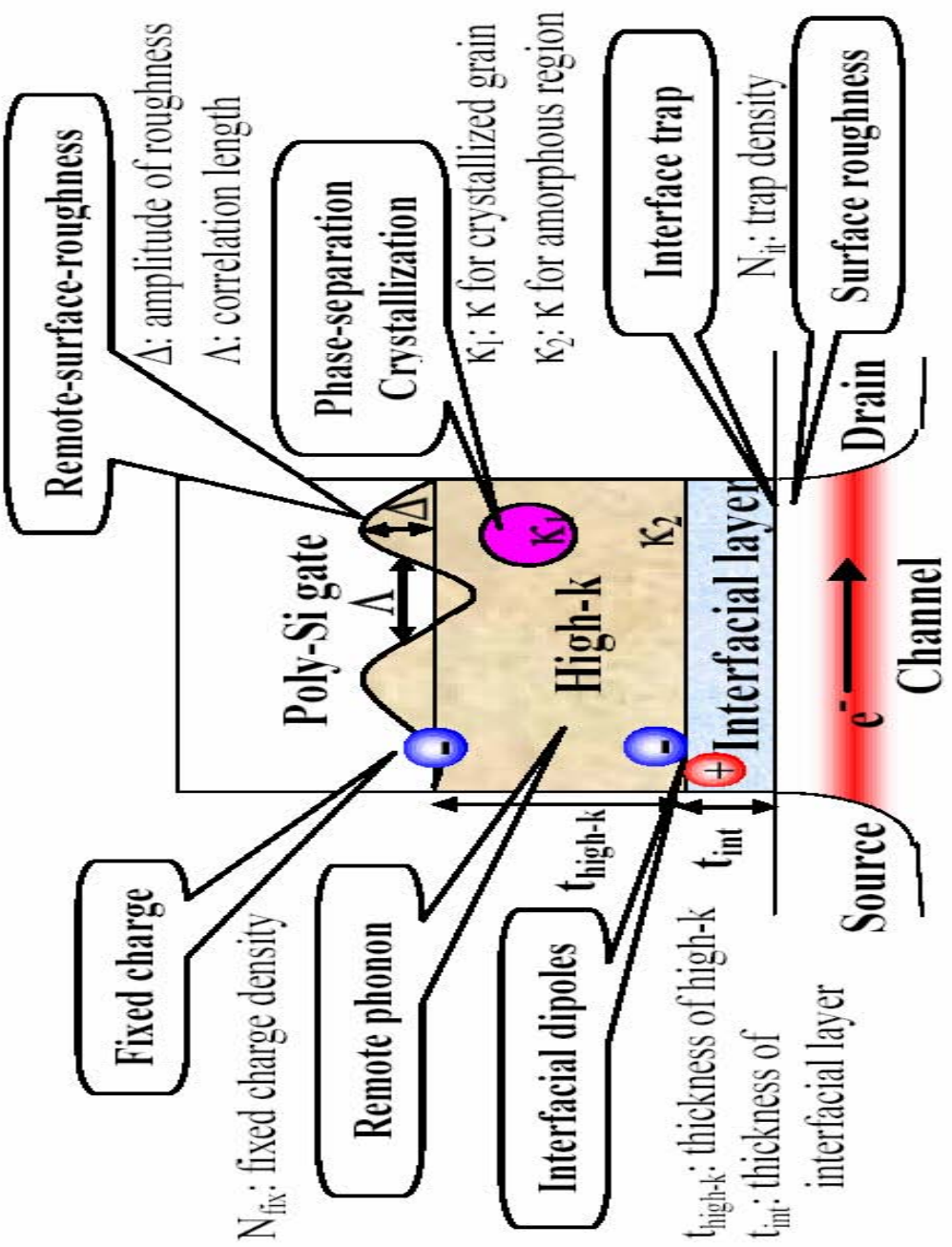


Figure 4-2 Possible sources for reduced mobility in high-κ gate stacks. *(Ref. [4.21] S. Saito, D. Hisamoto, S. Kimura, and M. Hiratani, "Unified Mobility Model for High-κ Gate Stacks", IEDM Technical Digest, 33.3.1-4, 2003.)*

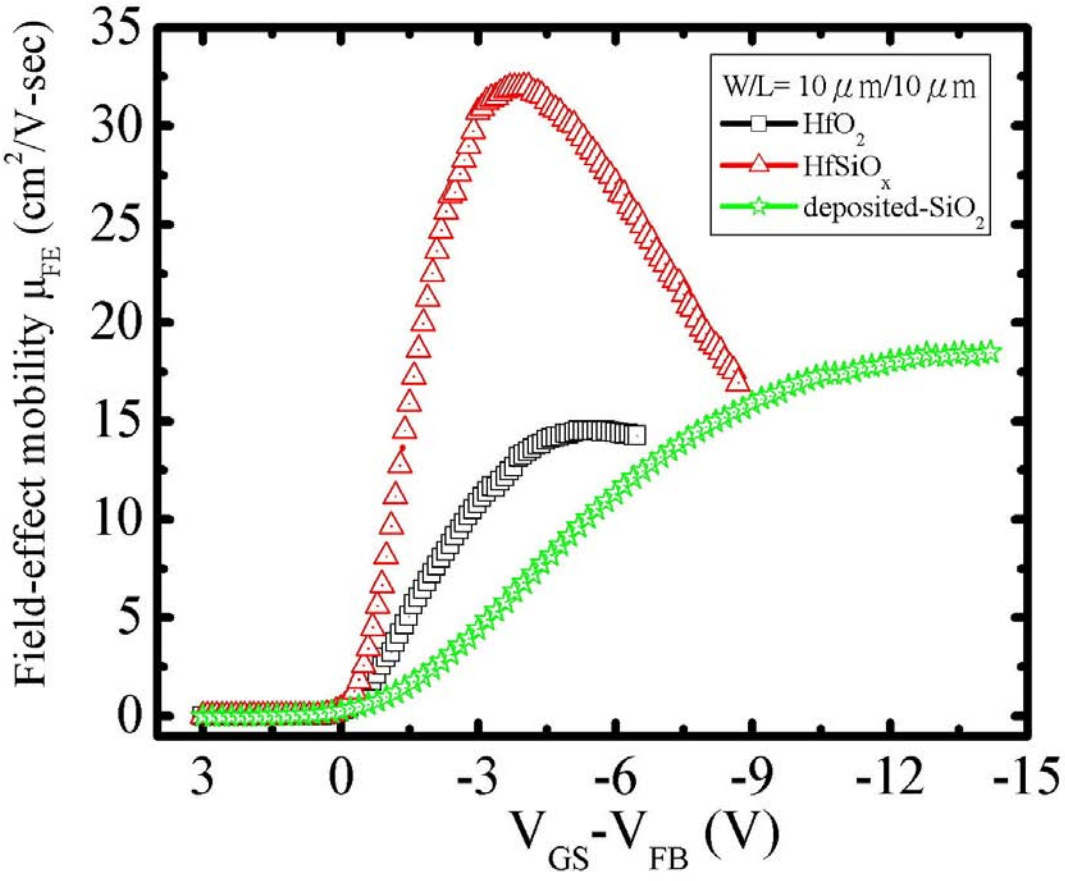
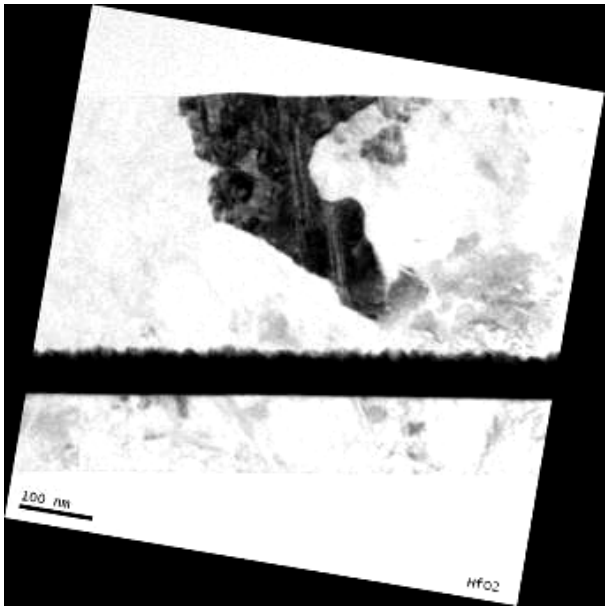
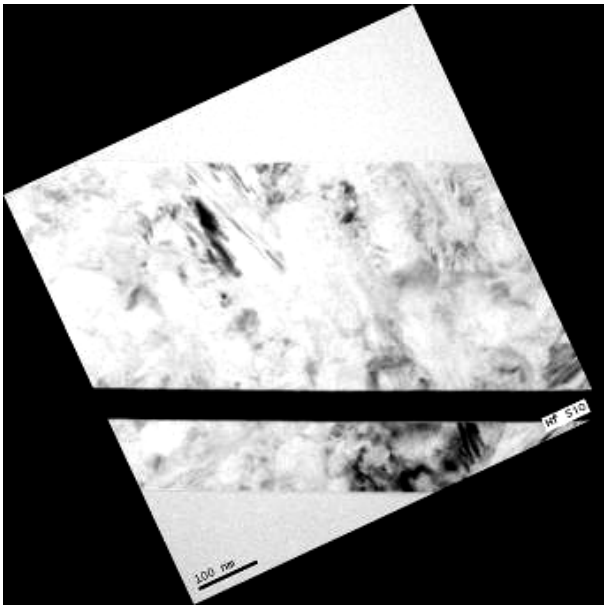
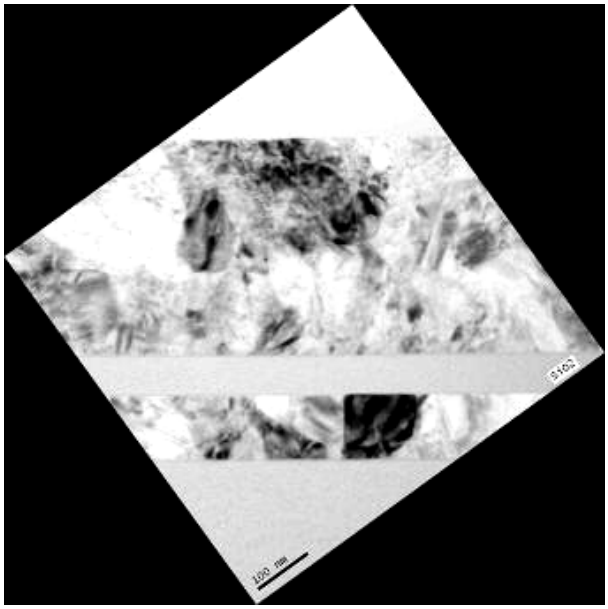


Figure 4-3 Comparisons of the field-effect mobility versus gate voltage between TFTs containing different gate dielectrics.



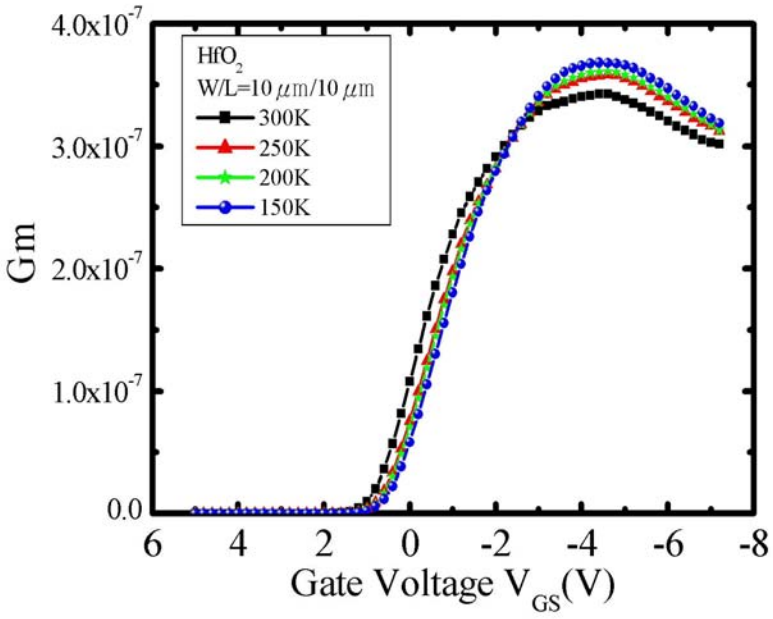
(a)



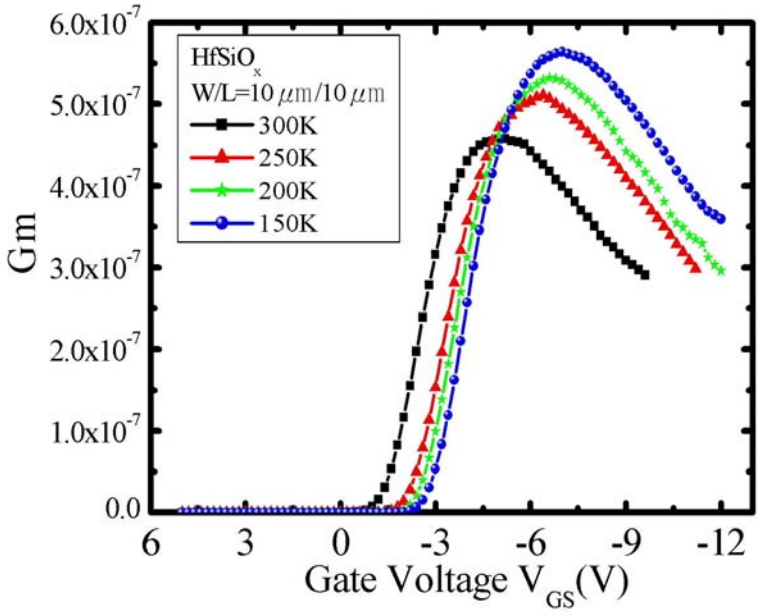


(b) (c)

Figure 4-4 Cross-sectional TEM images of TFTs incorporating (a) HfO_2, (b) $HfSiO_x$, and (c) deposited-SiO_2 gate dielectrics.



(a)



(b)

Figure 4-5 Transconductance (Gm) versus gate voltage at different measured temperatures (150^{o}K to 300^{o}K) for devices using (a) HfO_2 and (b) $HfSiO_x$ as gate dielectrics.

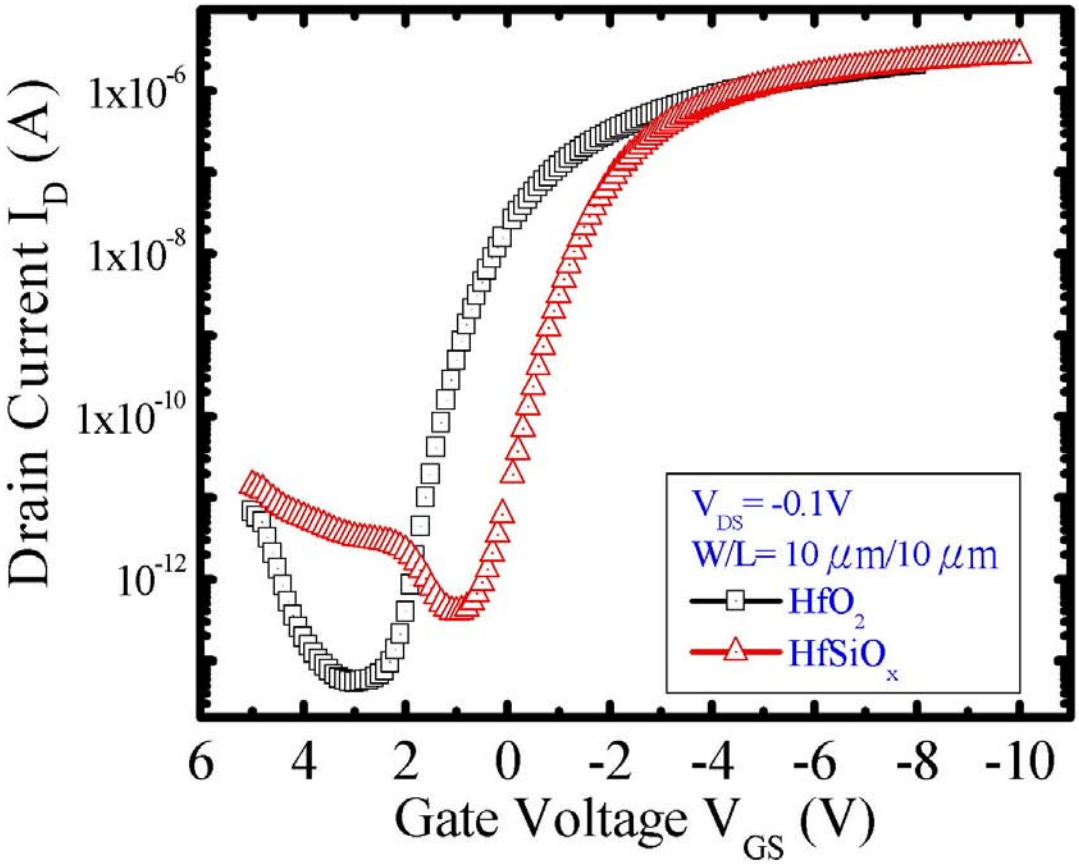
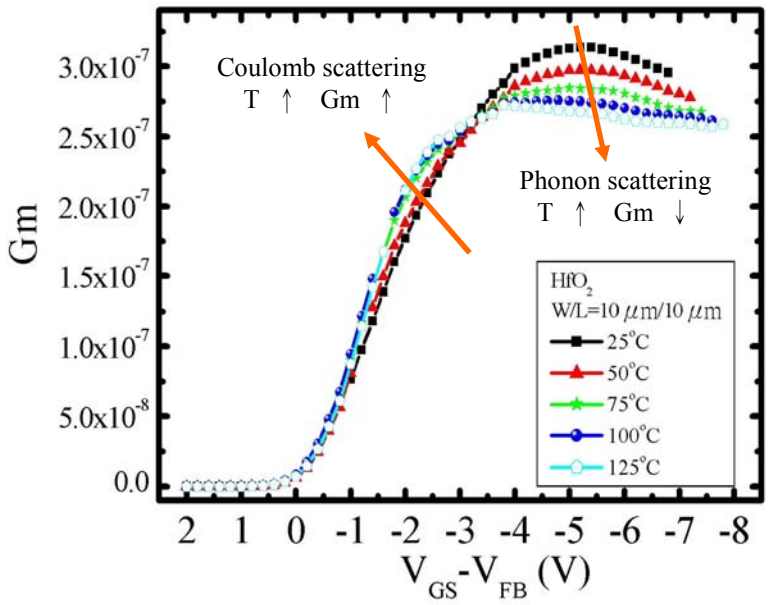
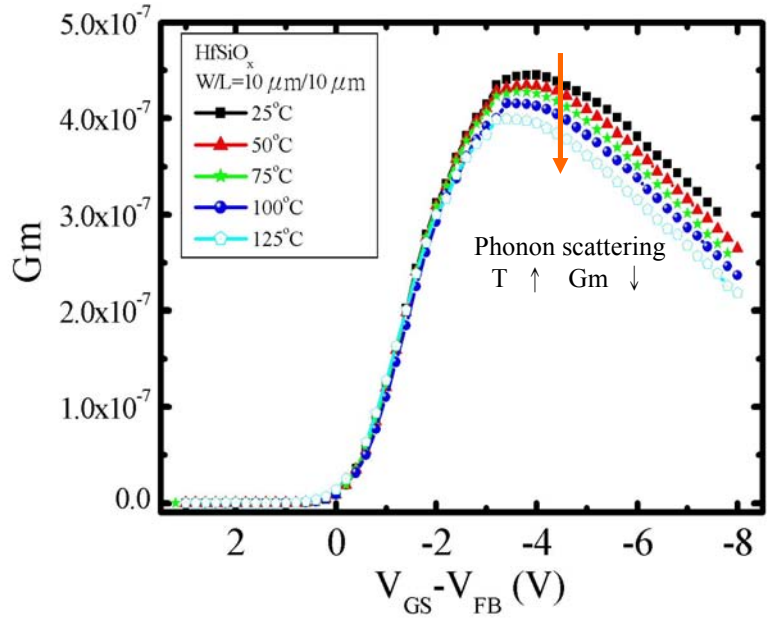


Figure 4-6 Comparisons of transfer characteristics at V_{DS} of -0.1 V between TFTs containing HfO_2 and $HfSiO_x$ as gate dielectrics.



(a)



(b)

Figure 4-7 Transconductance (Gm) versus gate voltage at different measured temperatures (25°C to 125°C) for devices using (a) HfO_2 and (b) $HfSiO_x$ as gate dielectrics.

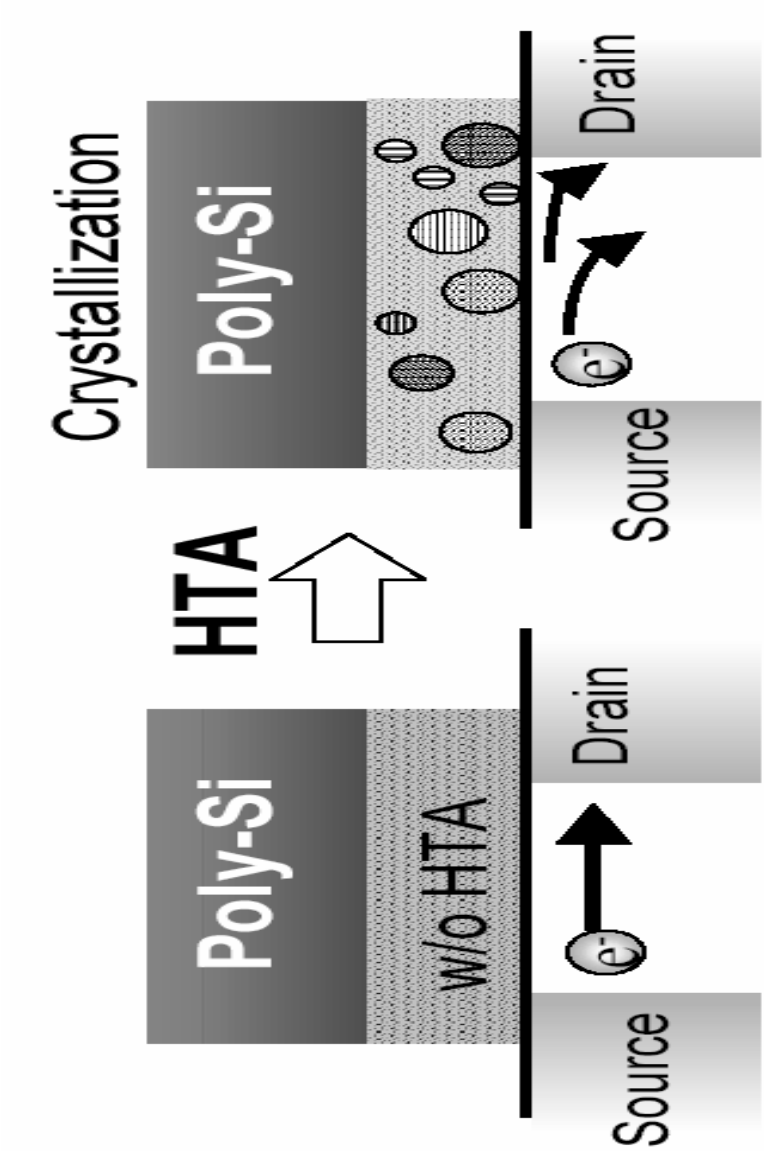
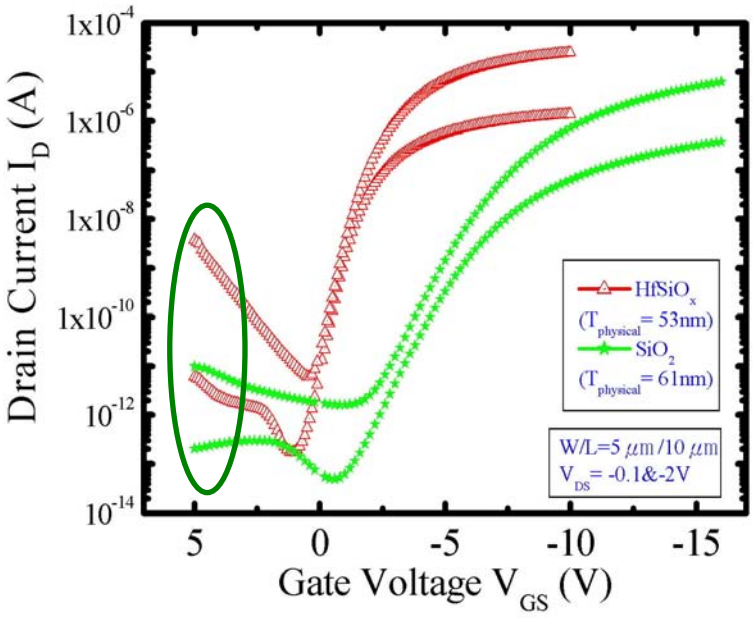
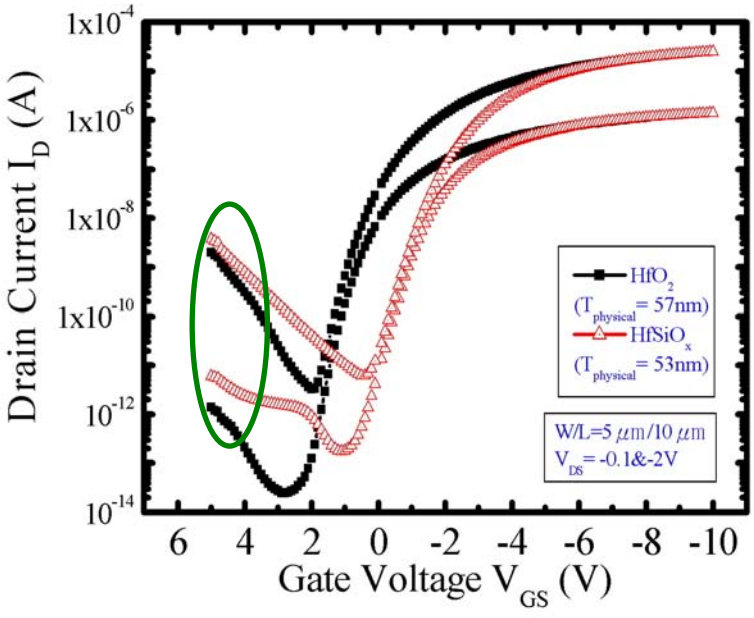


Figure 4-8 Schematic illustrations of electron mobility degradation observed in MISFET with partially crystallized Hf-silicate. *(Ref. [4.15] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, and H. Satake, "Additional Scattering Effects for Mobility Degradation in Hf-silicate Gate MISFETs", IEDM Technical Digest, 26.3.1-4, 2002.)*

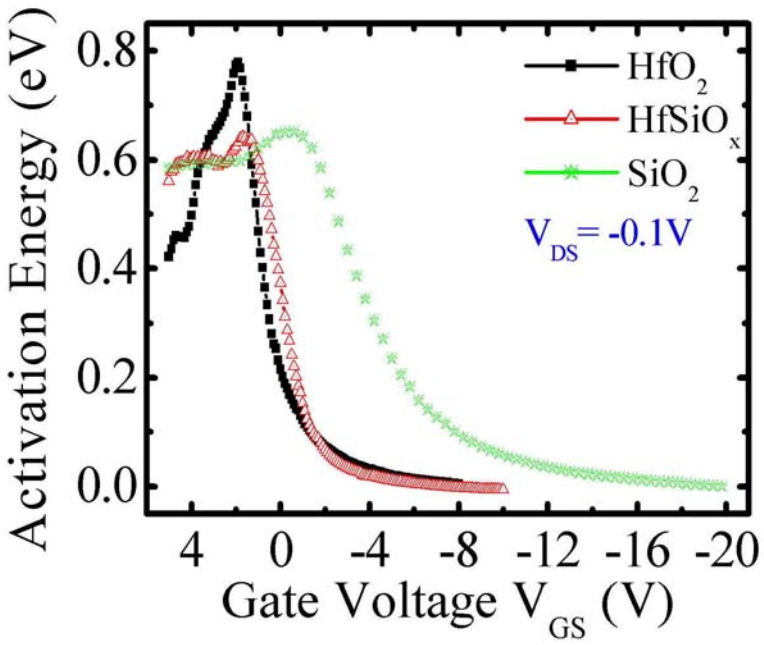


(a)

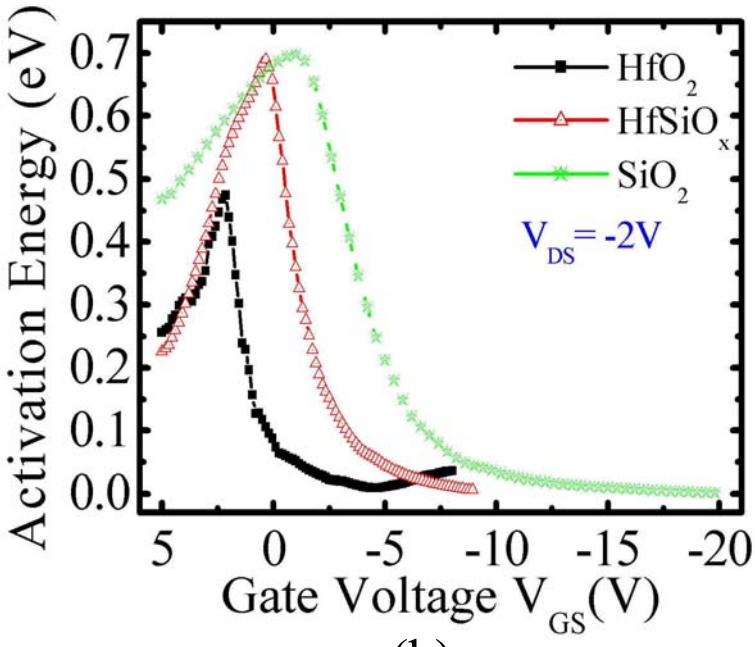


(b)

Figure 4-9 Comparisons of transfer characteristics at V_{DS} of -0.1 and -2 V between TFTs containing (a) $HfSiO_x$ and deposited-SiO_2 and (b) $HfSiO_x$ and HfO_2 as gate dielectrics.

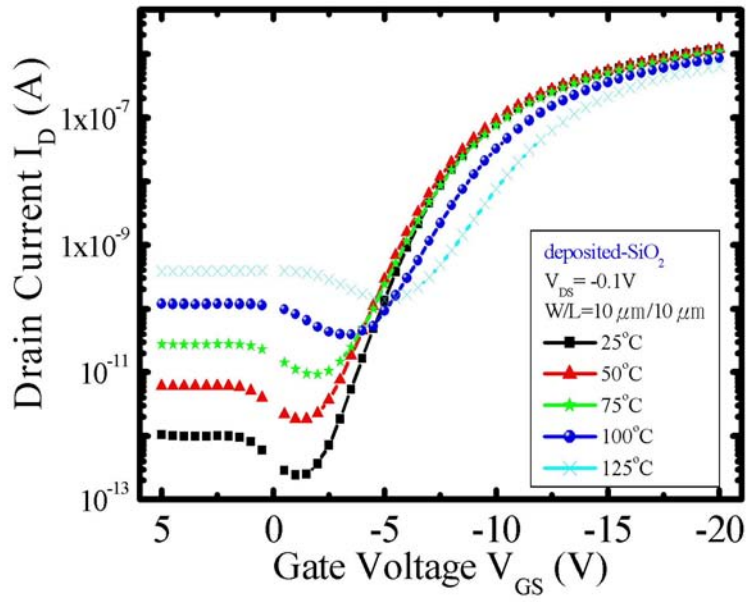


(a)

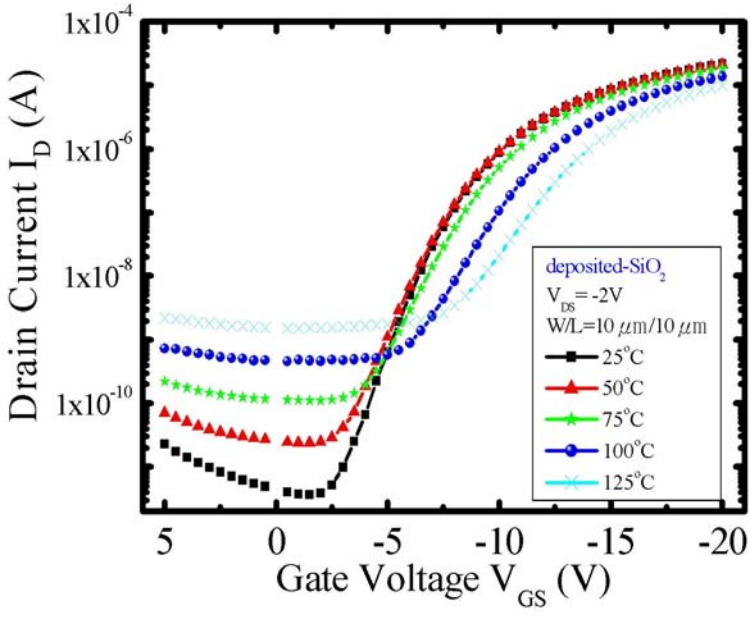


(b)

Figure 4-10 Channel activation energies obtained from the temperature dependence of transfer characteristics of poly-Si TFTs incorporating various gate dielectrics at V_{DS} of (a) –0.1 and (b) –2 V.

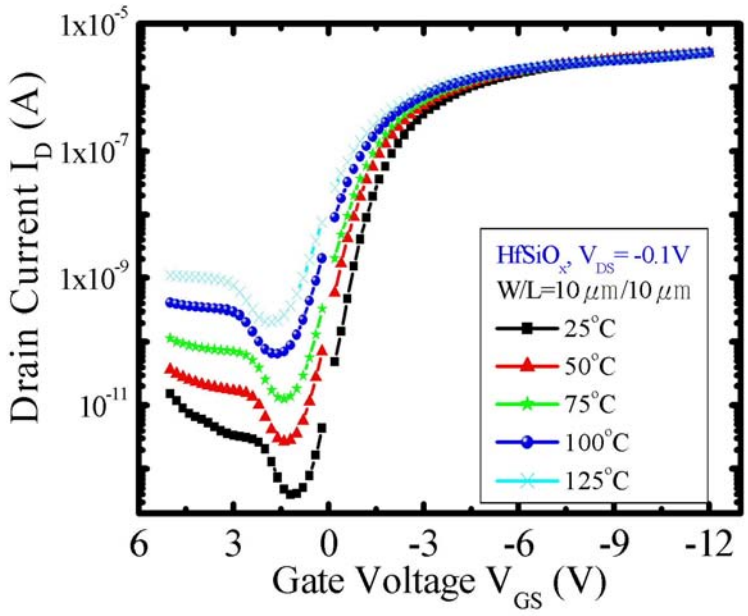


(a)

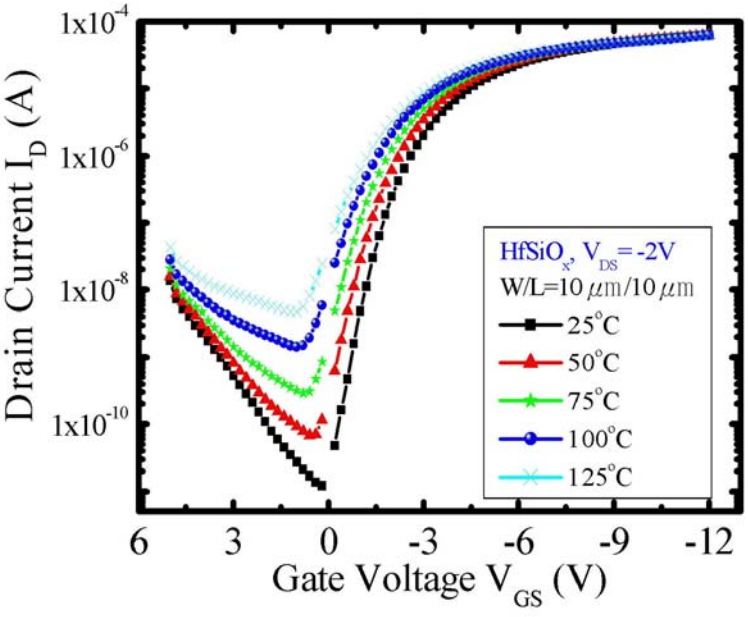


(b)

Figure 4-11 Comparisons of transfer characteristics at V_{DS} of (a) -0.1 and (b) -2 V at different measured temperatures for the TFT containing deposited-SiO_2 gate dielectric.

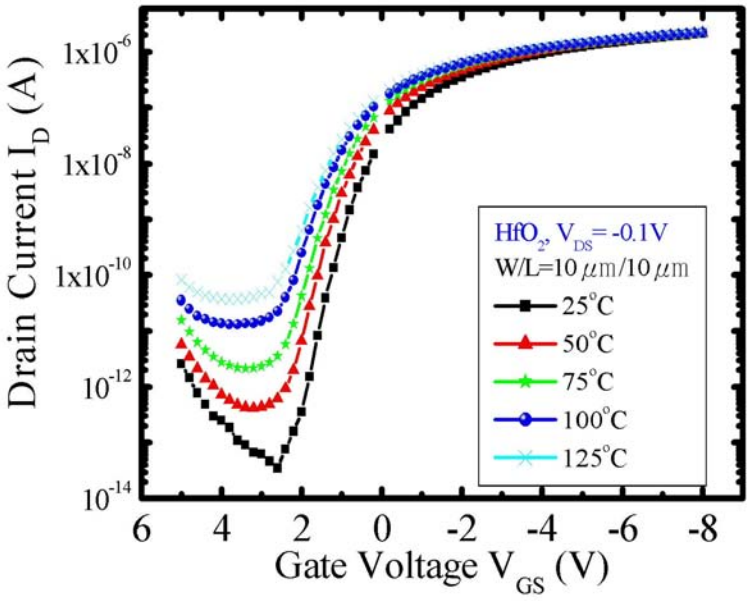


(a)

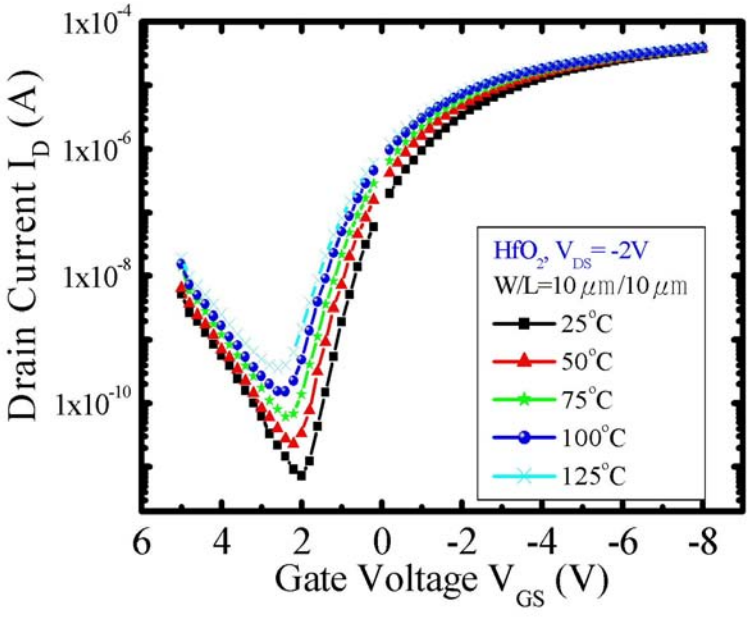


(b)

Figure 4-12 Comparisons of transfer characteristics at V_{DS} of (a) -0.1 and (b) -2 V at different measured temperatures for the TFT containing $HfSiO_x$ gate dielectric.



(a)



(b)

Figure 4-13 Comparisons of transfer characteristics at V_{DS} of (a) -0.1 and (b) -2 V at different measured temperatures for the TFT containing HfO_2 gate dielectric.

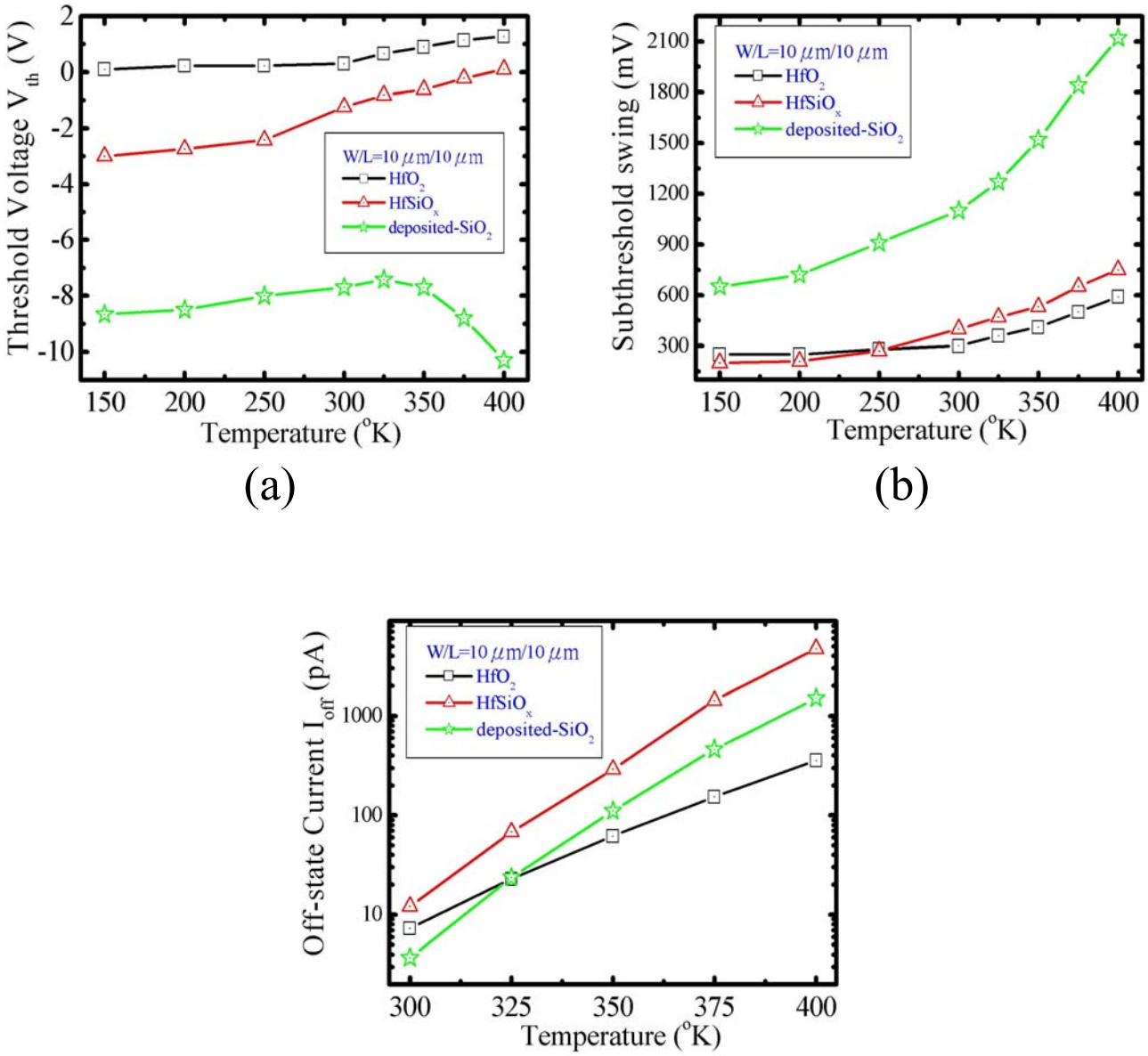
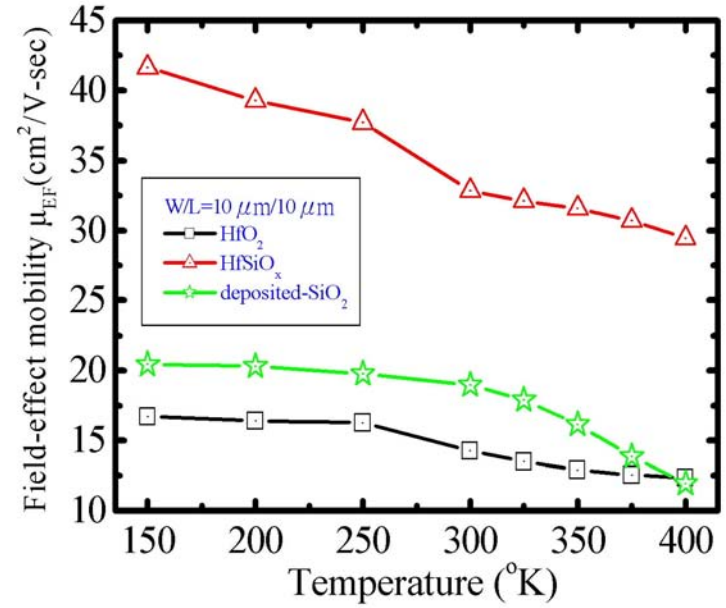
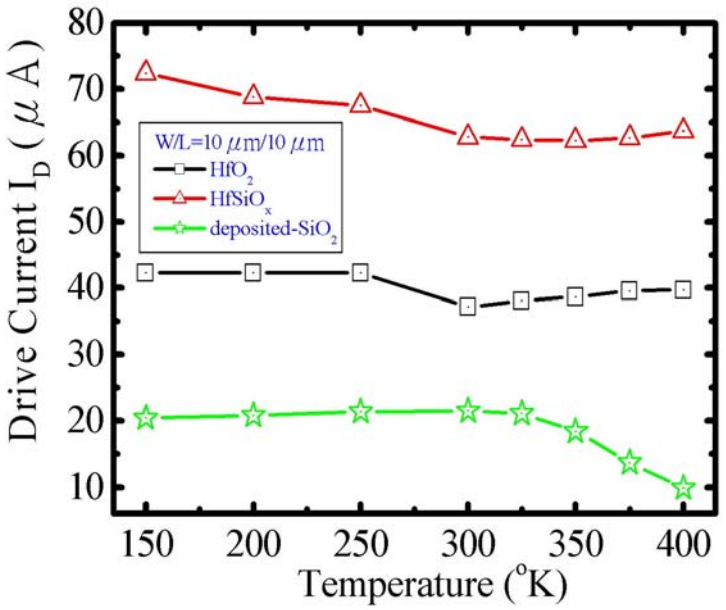


Figure 4-14 Comparisons of (a) threshold voltage,(b) subthreshold swing, and (c) off-state current versus measured temperatures among TFTs using different gate dielectrics.



(d)



(e)

Figure 4-14 Comparisons of (d) field-effect mobility and (e) drive current versus measured temperatures for TFTs using different gate dielectrics.

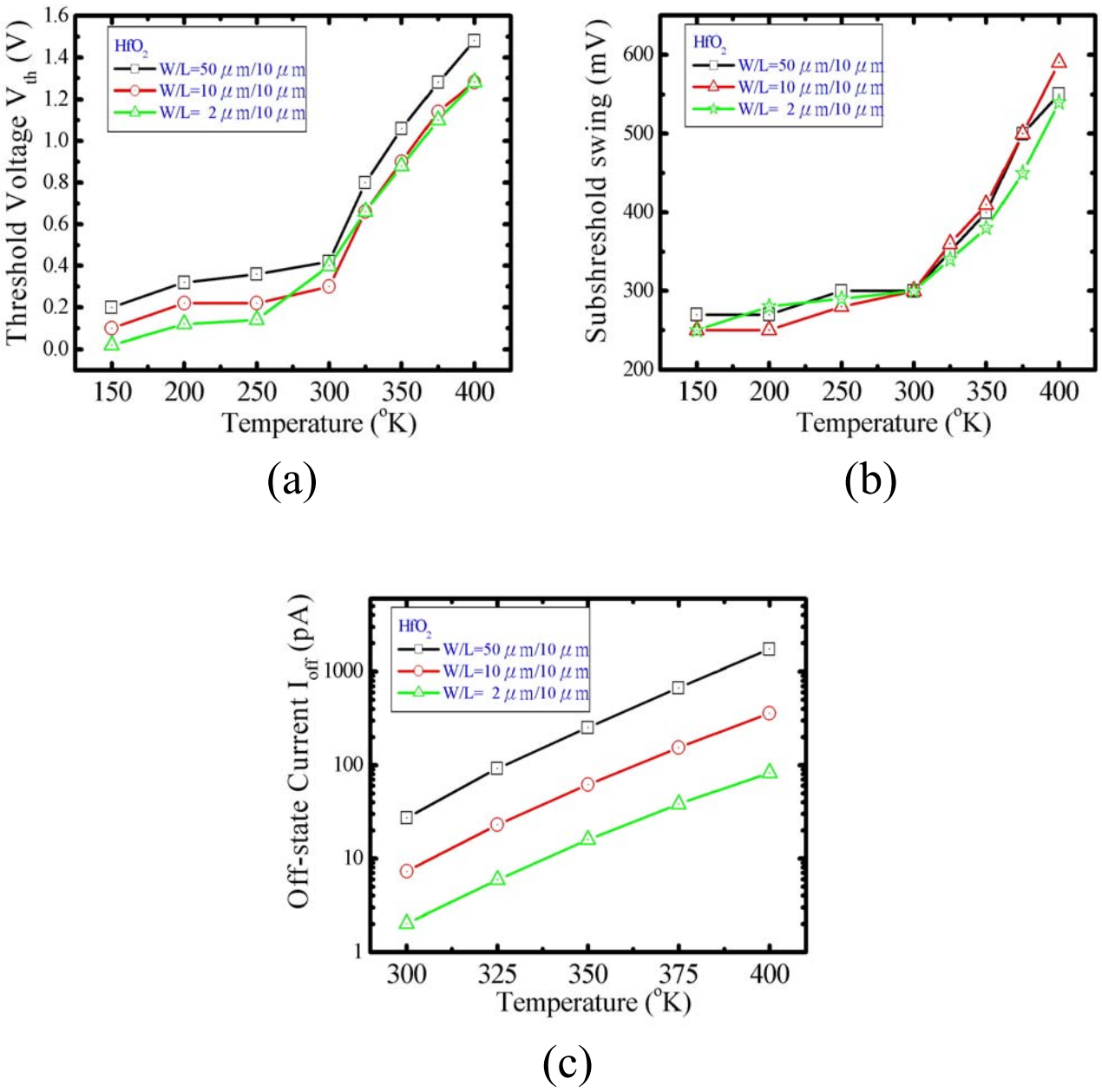
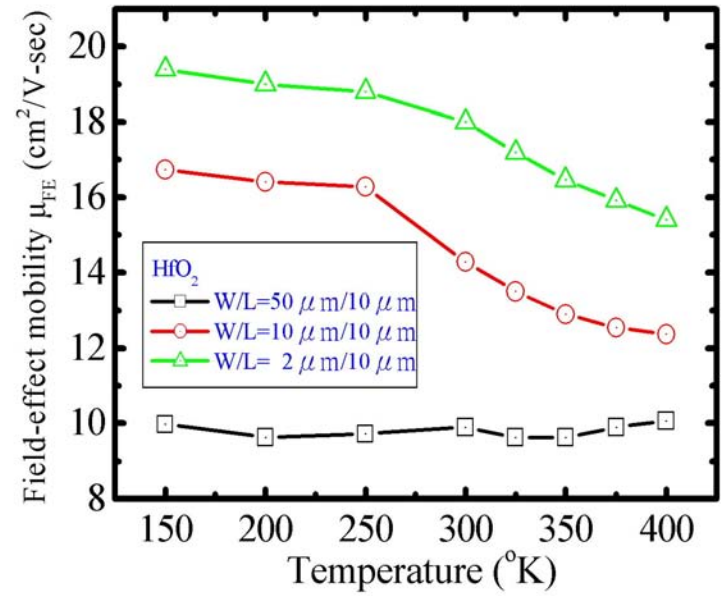
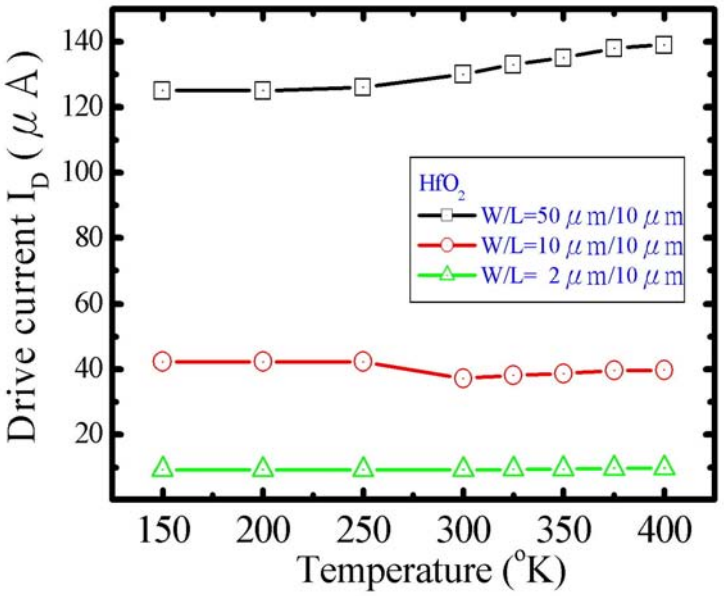


Figure 4-15 Comparisons of (a) threshold voltage, (b) subthreshold swing, and (c) off-state current versus measured temperatures among HfO_2-TFTs with different device dimensions.



(d)



(e)

Figure 4-15 Comparisons of (d) field-effect mobility and (e) drive current versus measured temperatures for HfO_2-TFTs with different device dimensions.

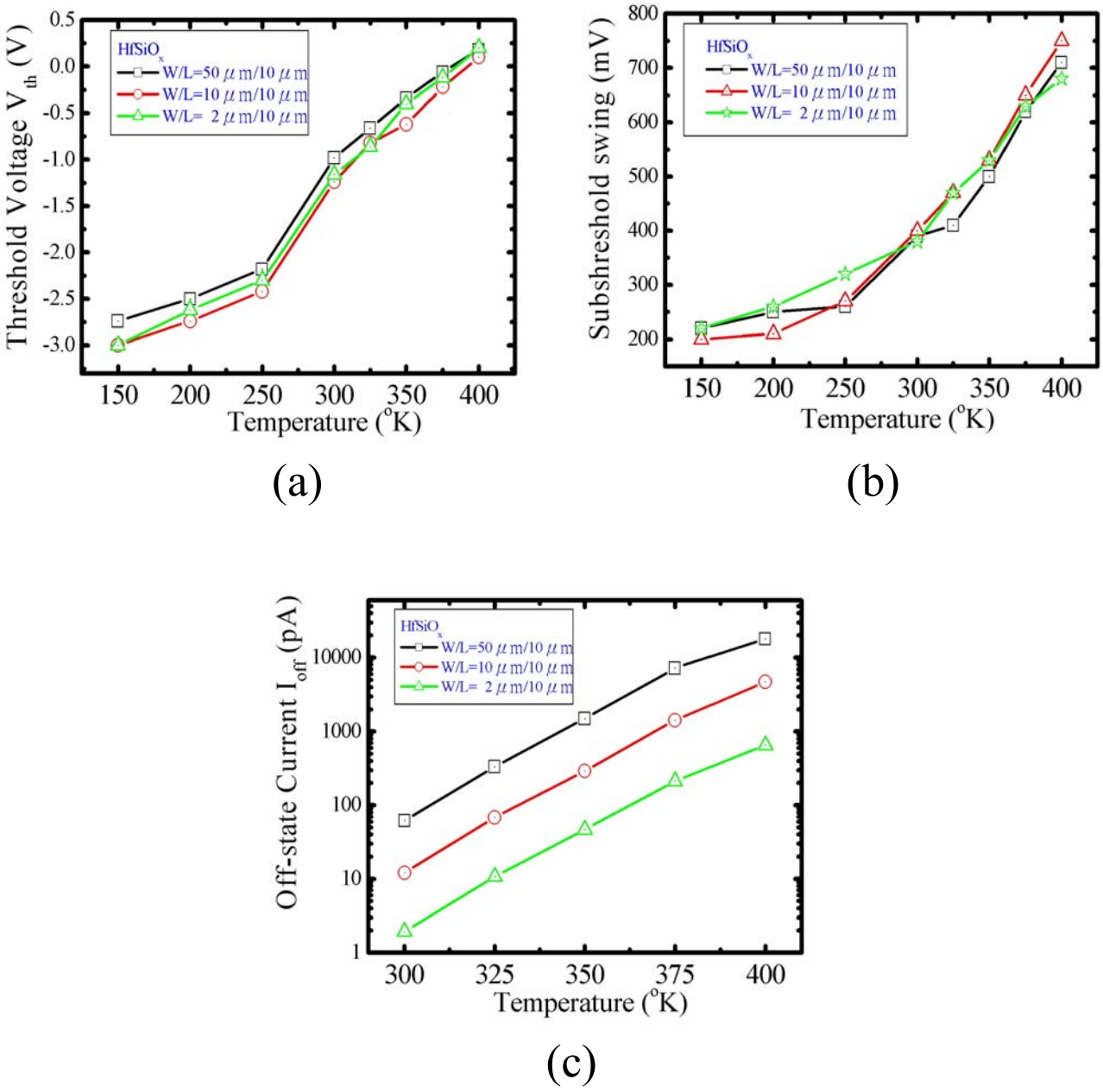
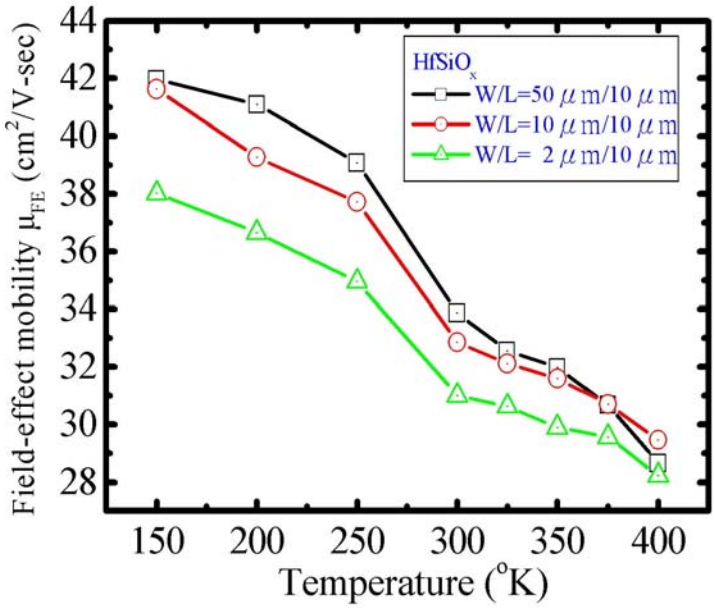
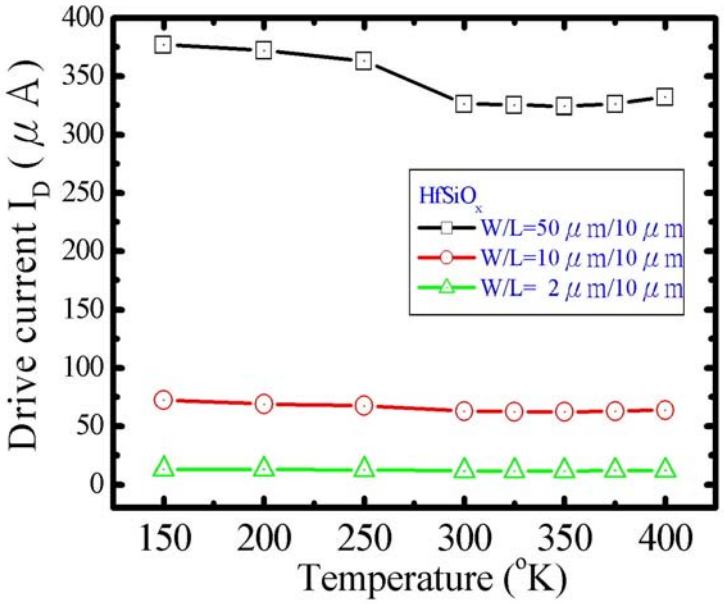


Figure 4-16 Comparisons of (a) threshold voltage, (b) subthreshold swing, and (c) off-state current versus measured temperature for $HfSiO_x$-TFTs with different device dimensions.



(d)



(e)

Figure 4-16 Comparisons of (d) field-effect mobility and (e) drive current versus measured temperatures for $HfSiO_x$-TFTs with different device dimensions.

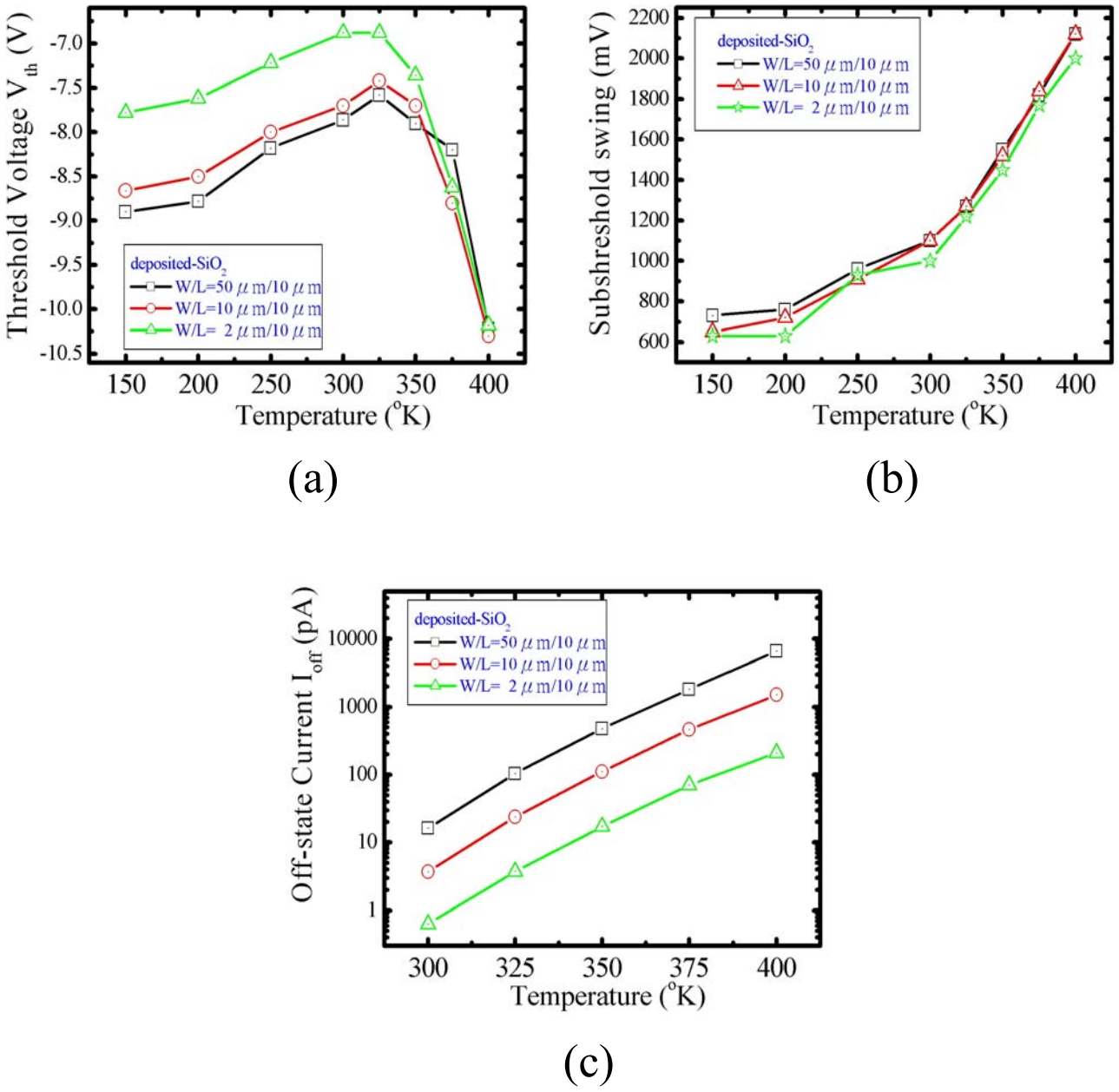
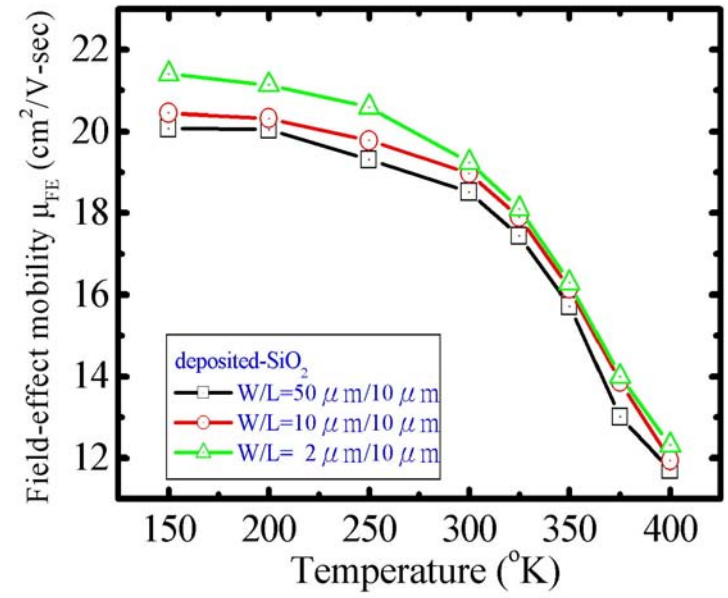
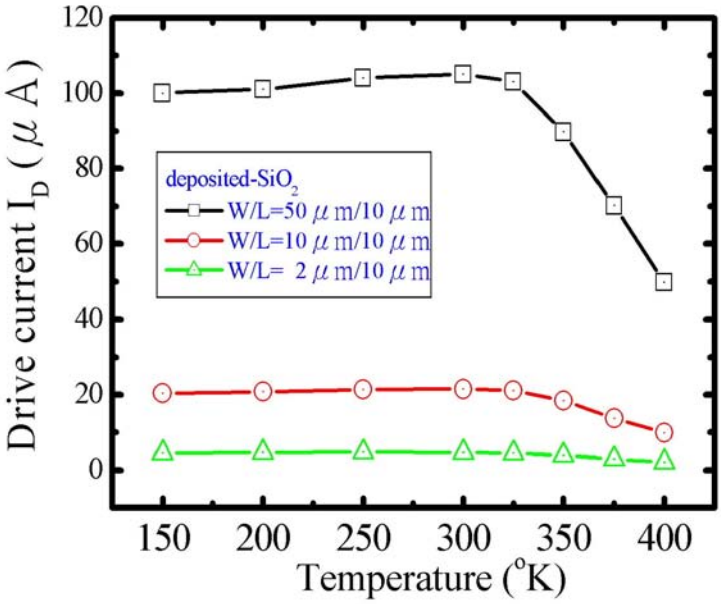


Figure 4-17 Comparisons (a) threshold voltage, (b) subthreshold swing, and (c) off-state current versus measured temperatures for deposited-SiO_2 TFTs with different device dimensions.



(d)



(e)

Figure 4-17 Comparisons of (d) field-effect mobility and (e) drive current versus measured temperatures for deposited-SiO_2 TFTs with different device dimensions.

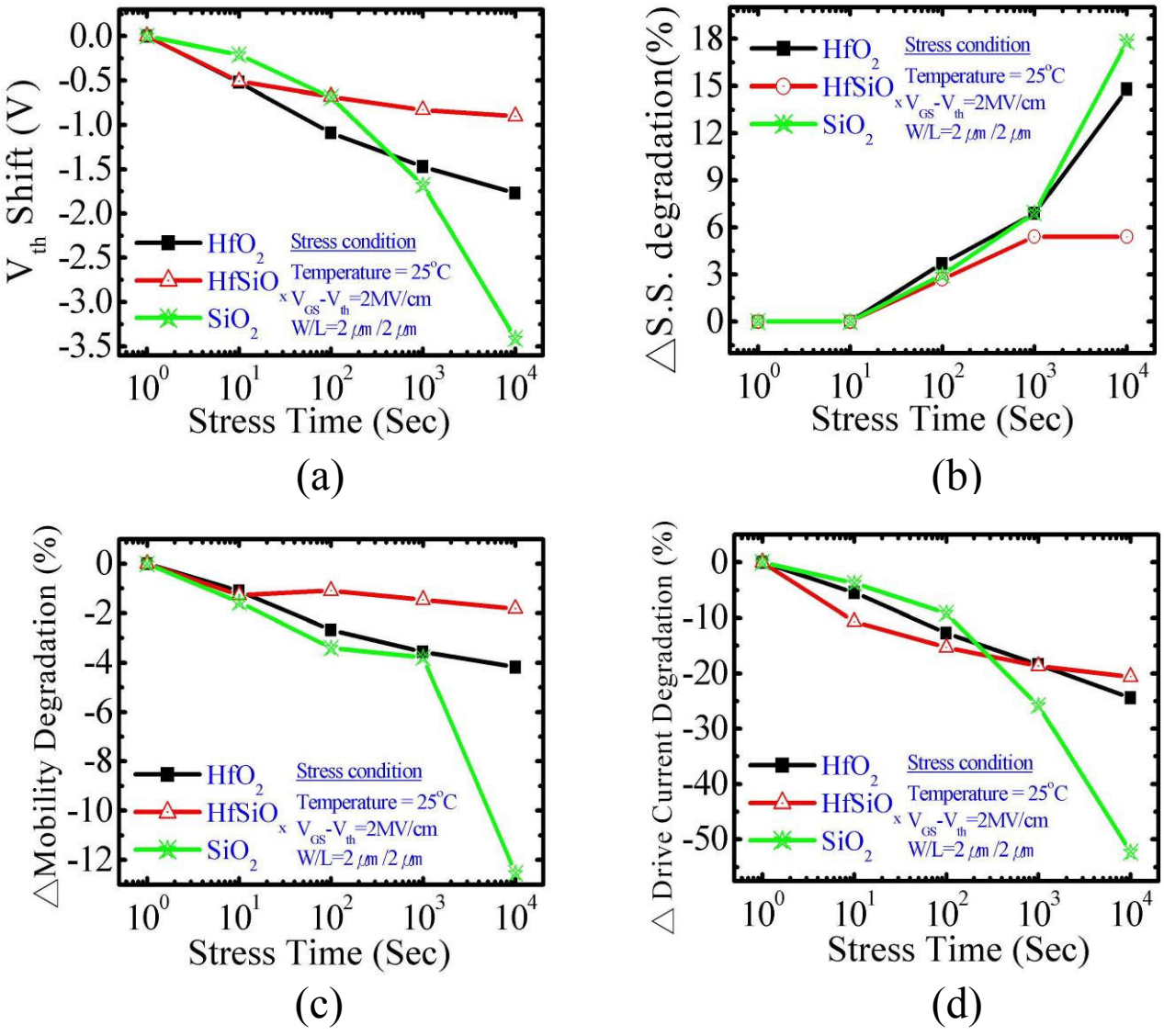


Figure 4-18 (a) V_{th}, (b) SS, (c) μ_{FE}, and (d) drive current as a function of stress time at 25°C for poly-Si TFTs incorporating various gate dielectrics.

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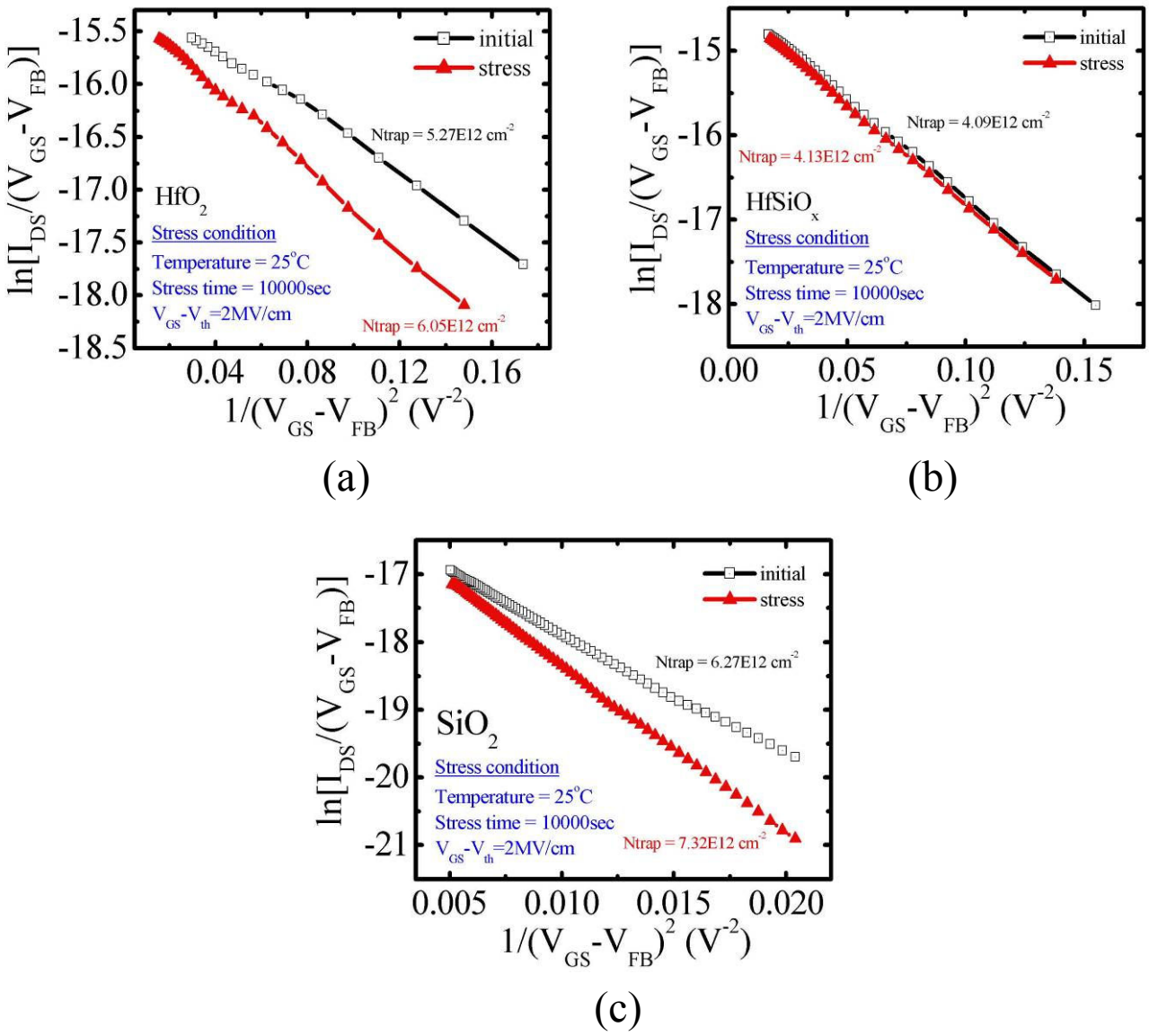


Figure 4-19 Grain-boundary trap-state density extraction of poly-Si TFTs incorporating (a) HfO_2, (b) $HfSiO_x$, and (c) deposited-SiO_2 gate dielectrics before and after NBTI stressing for 10,000 s at 25 ˚C; stress bias: $V_{GS} - V_{th} = 2$ MV/cm.

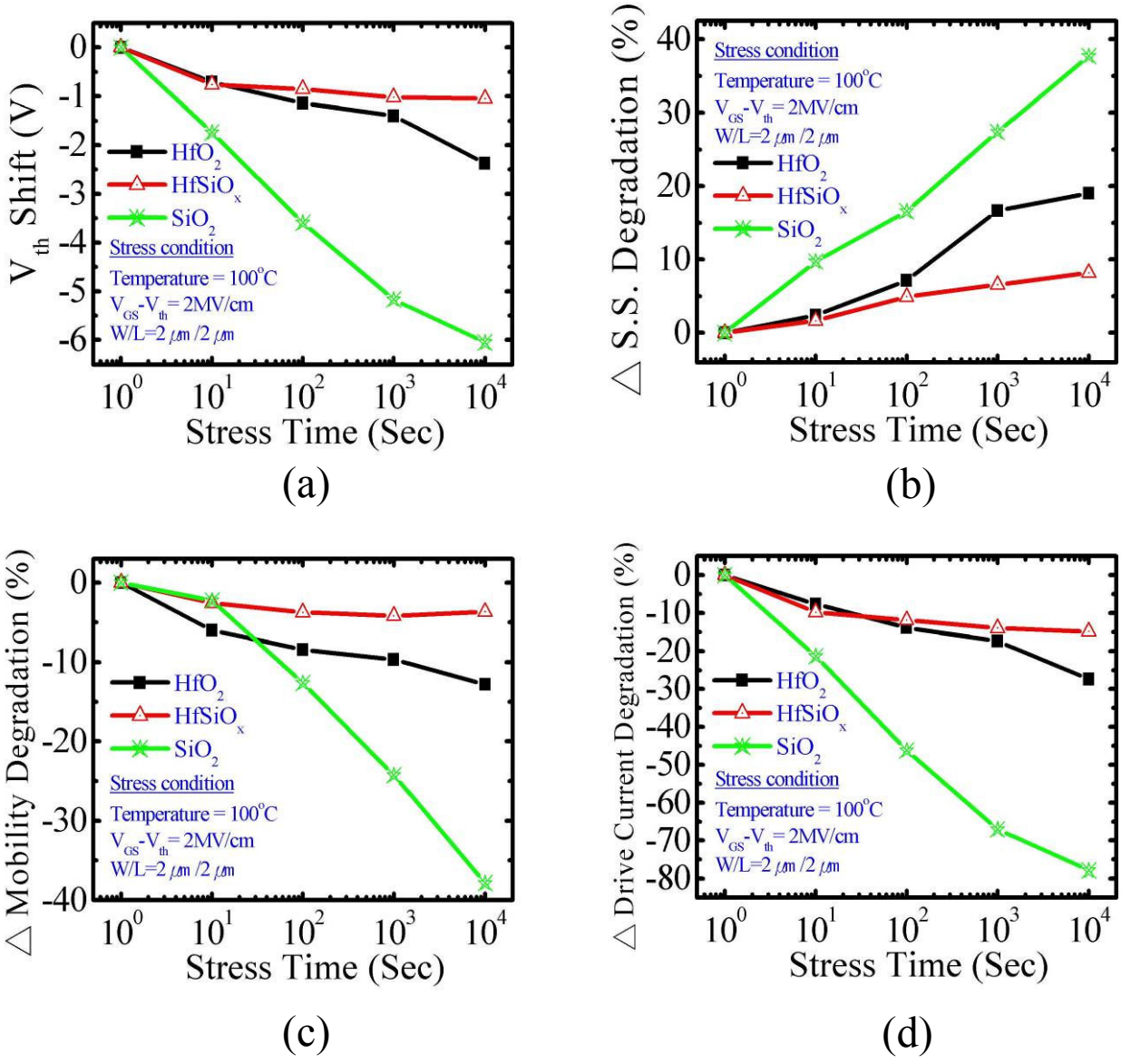


Figure 4-20 (a) V_{th}, (b) SS, (c) μ_{FE}, and (d) drive current as a function of stress time at 100°C for poly-Si TFTs incorporating various gate dielectrics.

Chapter 5
Conclusions and Future Prospects

5-1 Conclusions

In this dissertation, we have employed advanced high-κ materials to replace conventional low-temperature deposited oxide as the gate dielectric and fabricated high-performance low-temperature thin film transistors.

Firstly, the deposition parameters of the newly-developed high-κ materials prepared by atomic-vapor deposition (AVD) system were investigated in chapter 2. It was found that higher deposition temperature and sufficient oxygen gas flow are essential to obtain the high quality high-κ films by AVD system. However, the large leakage current would be caused by the polycrystalline structure of HfO_2 films. In contrast, the $HfSiO_x$ films exhibit better thermal stability and still keep the amorphous structure after high temperature annealing. Moreover, the presence of unwanted interfacial layer with lower κ value always exists between the thin high-κ gate dielectric and Si substrate. For the advanced MOSFETs application, deliberate surface treatments have to be done to suppress the interfacial layer growth in an effort to achieve lower EOT value by using these high-κ films.

Furthermore, we applied these high-κ materials to replace the conventional SiO_2 gate dielectric of LTPS TFTs and studied their impacts on the performance in chapter 3. We found that higher performance p-channel poly-Si TFTs using hafnium-silicate gate dielectric was obtained with low-temperature-compatible processing. Higher I_{on}/I_{off} current ratio, smaller subthreshold swing, lower threshold voltage and higher mobility than those with conventional deposited-SiO_2 gate dielectric were achieved at lower operation voltages. Our results suggest that $HfSiO_x$ is a potential candidate for the

gate-dielectric material of future high-performance poly-Si TFTs.

Finally, the mechanisms of mobility degradation and leakage current of poly-Si TFTs incorporating high-κ gate dielectrics were investigated in chapter 4. The lower mobility of HfO_2 TFTs was attributed to the additional scatterings, such as trapped charges, fixed charges, soft phonons, and crystallization, etc. However, using $HfSiO_x$ films can significantly eliminate these additional scatterings and achieve better mobility because of the higher thermal stability and better inherent properties. Nevertheless, high-κ gate dielectrics would lead higher electric field and induce severe GIDL current of poly-Si TFTs. The temperature instability and NBTI tests were also executed for the reliability characterization. We found that using high-κ gate dielectrics can not only enhance the performance of poly-Si TFTs but also improve their reliability over those incorporating conventional deposited-SiO_2.

5-2 Future Prospects

Although many aspects and topics have been covered in our study, there are still several interesting works that could be organized and executed.

(1) **The optimization of LTPS TFTs using high-κ gate dielectrics:** The high-κ TFTs were fabricated successfully in our study and exhibited better performance than the sample with deposited-SiO_2 gate dielectric. However, the characteristics of high-κ TFTs can be optimized by using more advanced methods and new structures. For example, better quality of poly-Si channel could be achieved by excimer laser annealing, which has been widely used in mass-production. As expected, enhancing the quality of deposited poly-Si films by laser annealing can bring about superior performance of high-κ TFTs. Also, as mentioned in the literature, high-κ gate dielectrics would lead higher electric field and induce severe GIDL current of poly-Si TFTs. The adoption of lightly doped drain (LDD), multi-gate, and offset

structures, which can reduce the electrical field between the drain and the channel of the TFT, can be applied to suppress the deterioration of the off-state current when high-κ dielectrics are employed as gate dielectrics. Furthermore, high-κ materials with thermally-stable amorphous structure and higher κ value or the high-κ stack films also could be utilized to decrease the EOT and enhance the device performance. Finally, to accomplish the entire processing of the poly-Si TFTs in low-temperature, the metal gate and low-temperature activation methods have to be employed to achieve the goal.

(2) **The fabrication of low-temperature poly-Ge TFTs:** First successful deposition of pure poly-Ge film was deposited successfully onto SiO_2-covered Si substrates using ICP-CVD techniques in appendix. However, the fabrication of TFTs using poly-Ge films as the channel has not been accomplished yet. Several key issues have to be overcome in the process of poly-Ge TFTs in future. Firstly, the crystallinity of poly-Ge could be modified by other methods, such as laser crystallization and metal-induced lateral crystallization, which have been already employed in the preparation of poly-Si films. And then, more attentions have to be paid to the behaviors of dopant activation at the contact and junction regions. Furthermore, high-κ gate dielectrics also could be utilized to enhance the device performance.

References

Chapter 1

[1.1] Y. Matsueda, T. Ozawa, M. Kimura, T. Itoh, K. Kitwada, T. Nakazawa, H. Ohsima, "A 6-bit-color VGA low-temperature poly-Si TFT-LCD with integrated digital data drivers," in *SID Tech. Dig.*, pp. 879-882, 1998.

[1.2] Y. Aoki, T. Lizuka, S. Sagi, M. Karube, T. Tsunashima, S. Ishizawa, K. Ando, H. Sakurai, T. Ejiri, T. Nakazono, M. Kobayashi, H. Sato, N. Ibaraki, M. Sasaki, and N. Harada, "A10.4-in. XGA low-temperature poly-Si TFT-LCD for mobile PC applications," in *SID Tech. Dig.*, pp. 176-179, 1999.

[1.3] J. G. Blake, J. D. III Stevens, and R. Young, "Impact of low temperature polysilicon on the AMLCD market," *Solid States Tech.*, vol. 41, pp. 56-62, 1998.

[1.4] Yasuhisa Oana, "Current and future technology of low-temperature poly-Si TFT-LCDs," *Journal of the SID*, Vol. 9, pp. 169-172, 2001.

[1.5] Jun Hanari, "Development of a 10.4-in. UXGA display using loe-temperature poly-Si technology," *Journal of the SID*, Vol. 10, pp. 53-56, 2002.

[1.6] Mark Stewart, Robert S. Howell, Leo Pires, and Miltiadis K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," *IEEE Trans. Electron Devices*, Vol. 48, pp. 845-851, 2001.

[1.7] Zhiguo Meng and Man Wong, "Active-matrix organic light-emitting diode displays realized using metal-induced unilaterally crystallized polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, Vol. 49, pp. 991-996, 2002.

[1.8] N. D. Young, G. Harkin, R. M. Bunn, D. J. McCulloch, and I. D. French, "The fabrication and characterization of EEPROM arrays on glass using a low-temperature poly-Si TFT process," *IEEE Trans. Electron Devices*, Vol. 43, pp.

1930-1936, 1996.

[1.9] W. G. Hawkins, “Polycrystalline-silicon device technology for large-area electronics,” *IEEE Trans. Electron Devices*, Vol. 33, pp. 477-481, 1986.

[1.10] I-W. Wu, “Cell design considerations for high-aperture-ratio direct-view and projection polysilicon TFT-LCDs,” in *SID Tech. Dig.*, pp. 19-22, 1995.

[1.11] A. Mimura, N. Konishi, K. Ono, J. Ohwada, Y. Hosokawa, Y. Ono, T. Suzuki, K. Miyata, and H. Kawakami, “High performance lo-temperature poly-Si n-channel TFTs for LCD,” *IEEE Trans. Electron Devices*, Vol. 36, pp. 351-359, 1989.

[1.12] P. M. Smith, P. G. Carey, and T. W. Sigmon, “ Excimer laser crystallization and doping of silicon films on plastic substrates,” *Appl. Phys. Lett.*, Vol. 70, pp. 342-344, 1997.

[1.13] S. D. Brotherton, D. J. McCulloch, J. P. Gowers, J. R. Ayres, C. A. Fisher, and F. W. Rohlfing, “Excimer laser crystallization of poly-Si TFTs for AMLCDs,” *Mat. Res. Soc. Symp. Proc.*, Vol. 621, Q7.1.1-Q7.1.12, 2000.

[1.14] Seok-Woon Lee, Tae-Hyung Ihn, and Seung-Ki Joo, “Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization,” *IEEE Electron Device Lett.*, Vol. 17, pp. 160-162, 1996.

[1.15] Seok-Woon Lee, Tae-Hyung Ihn, and Seung-Ki Joo, “Fabrication of high-mobility p-channel poly-Si thin-film transistor by self-aligned metal-induced lateral crystallization,” *IEEE Electron Device Lett.*, Vol. 17, pp. 407-409, 1996.

[1.16] Zhonghe Jin, Hoi S. Kwok, and Man Wong, “Performance of thin-film transistors with ultrathin Ni-MILC polycrystalline silicon channel layers,” *IEEE Electron Device Lett.*, Vol. 20, pp. 167-169, 1999.

[1.17] K. Werner, “The flowering of flat displays”, *IEEE Spectrum*, Vol. 34, pp. 40–49, 1997.

[1.18] A. Takami, A. Ishida, J. Tsutsumi, T. Nishibe, and N. Ibaraki, “Threshold voltage

shift under the gate bias stress in low-temperature poly-silicon TFT with the thin gate oxide film", in *Proc. Int. Workshop AM-LCD 2000*, pp. 45–48.

[1.19] M. Y. Um, S.-K. Lee, and H. J. Kim, "Characterization of thin film transistor using Ta_2O_5 gate dielectric", in *Proc. Int. Workshop AM-LCD 1998*, pp. 45–46.

[1.20] Z. Jin, H. S. Kwok, and M. Wong, "High-performance polycrystalline SiGe thin-film transistors using Al_2O_3 gate insulators", *IEEE Electron Device Lett.*, Vol. 19, no. 12, pp. 502–504, Dec. 1998.

[1.21] C.-P. Lin, B.-Y. Tsui, M.-J. Yang, R.-H. Huang, and C.-H. Chien, "High-Performance Poly-Silicon TFTs Using HfO_2 Gate Dielectric", *IEEE Electron Device Lett.*, Vol. 27, no. 5, pp. 360–363, May 2006.

[1.22] B. W. Busch, O. Pluchery, Y. J. Chabal, D. A. Muller, R. L. Opila, J. R. Kwo, and E. Garfunkel, "Materials characterization of alternative gate dielectrics", *MRS Bull.*, Vol. 27, no. 3, pp. 206–211, Mar. 2002.

[1.23] H. S. P. Wong, "Beyond the conventional transistor", *IBM J. Res. Develop.*, Vol. 46, no. 2/3, pp. 133–168, May 2002.

[1.24] C.-P. Lin, B.-Y. Tsui, M.-J. Yang, R.-H. Huang, and C.-H. Chien, "High-Performance Poly-Silicon TFTs Using HfO_2 Gate Dielectric", *IEEE Electron Device Lett.*, Vol. 27, no. 5, pp. 360–363, May 2006.

[1.25] H. Jorke and H. J. Herzog, "Mobility Enhancement in modulation-Doped Si-$Si_{1-x}Ge_x$ Superlattice Grown by Molecular Beam Epitaxy," *J. Electrochem. Soc.*, Vol. 133, pp. 998–1001, 1986.

[1.26] H. Shinoda, M. Kosaka, J. Kojima, H. Ikeda, S. Zaima and Y. Yasuda, "Electrical properties of metal/$Si_{1-x}Ge_x$/Si(100) heterojunctions," *Appl. Surf. Sci.*, Vol. 100/101, 526–529, 1996.

[1.27] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "Germanium MOS capacitors incorporating ultrathin high-k gate dielectric ,"

IEEE Electron Device Lett., Vol. 23, no. 8, pp. 473–475, 2002.

[1.28] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS characteristics with CVD HfO/sub 2/ gate dielectrics and TaN gate electrode," *Symposium on VLSI Technology*, Digest of Technical Papers, p. 121-122 , 2003.

[1.29] H. Shang, H. Okorn-Schimdt, J. Ott, P. Kozlowski, S. Steen, E. C. Jones, H.-S. P. Wong, and W. Hanesch," Electrical characterization of germanium p-channel MOSFETs," *IEEE Electron Device Lett*., Vol. 24, no. 4, pp. 242–244, 2003.

[1.30] H. Hibino, N. Shimizu and Y. Shinoda, "Mesh pattern of Ge islands grown using solid phase epitaxy," *J. Vac. Sci. Technol*., A11, pp. 2458–2462, 1993.

[1.31] C. H. Huang, M. Y. Yang, A. Chin,W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, "Very low defects and high performance Ge-on-insulator p-MOSFETs with Al_2O_3 gate dielectrics," *Symposium on VLSI Technology*, Digest of Technical Papers, pp. 119-120, 2003.

[1.32] S.-I. Takagi, "Re-examination of subband structure engineering in ultra-short channel MOSFETs under ballistic carrier transport," *Symposium on VLSI Technology*, Digest of Technical Papers, pp. 115-116, 2003.

[1.33] T. Sadoh, H. Kamizuru, A. Kenjo, and M. Miyao, "Low-temperature formation (<500 °C) of poly-Ge thin-film transistor with NiGe Schottky source/drain", *Appl. Phys. Lett.*, Vol. 89, (192114) 2006.

[1.34] D. Dentel, J. L. Bischoff, T. Angot, and L. Kubler, " The influence of hydrogen during the growth of Ge films on Si(001) by solid source molecular beam epitaxy", *Surf. Sci.*, Vol. 402–404, pp. 211–214, 1998.

[1.35] M. Okada, A. Muto, I. Suzumura, H. Ikeda, S. Zaima, and Y. Yasuda, "Hydrogen Effects on Heteroepitaxial Growth of Ge Films on Si(111) Surfaces by Solid Phase Epitaxy", *Jpn. J. Appl. Phys.*, part 1, No. 12B, Vol. 37, pp. 6970–6973,

1998.

[1.36] Q. Li, S. M. Han, S. R. J. Brueck, S. Hersee, Y. B. Jiang, and H. Xu, "Selective growth of Ge on Si(100) through vias of SiO_2 nanotemplate using solid source molecular beam epitaxy", *Appl. Phys. Lett.*, Vol. 83, No.24, pp. 5032–5034, 2003.

[1.37] S. Kobayashi, M. Sakuraba, T. Matsuura, J. Murota, and N. Mikoshiba, "Initial growth characteristics of germanium on silicon in LPCVD using germane gas:, *J. Cryst. Growth*, Vol. 174, pp. 686–690, 1997.

[1.38] M. Racanelli and D. W. Greve, "Low-temperature selective epitaxy by ultrahigh-vacuum chemical vapor deposition from SiH_4 and GeH_4/H_2", *Appl. Phys. Lett.*, Vol. 58 (19), pp. 2096-2098, 1991.

[1.39] T. Baron, B. Pelissier and et al., "Chemical vapor deposition of Ge nanocrystals on SiO_2", *Appl. Phys. Lett.*, Vol. 83(07), pp. 1444-1446, 2003.

[1.40] Y. Liu, M. D. Deal, and J. D. Plummer, "High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates", *Appl. Phys. Lett.*, Vol. 84 (14), pp. 2563-2565, 2004.

Chapter 2

[2.1] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations", *J. Appl. Phys.,* Vol. 89, pp. 5243-5275, 2001.

[2.2] D. A. Neumayer and E. Cartier, "Materials characterization of ZrO_2–SiO_2 and HfO_2–SiO_2 binary oxides deposited by chemical solution deposition", *J. Appl. Phys.*, Vol. 90, pp. 1801-1808, 2001.

[2.3] W. Zhu, T. P. Ma, T. Tamagawa, Y. Di, J. Kim, R. Carruthers, M. Gibson, and T.

Furakawa, "HfO_2 and HfAlO for CMOS: thermal stability and current transport ", *IEDM Technical Digest* 2001, 20.4.1-20.4.4.

[2.4] A. Callegari, E. Cartier, M. Gribelyuk, H. F. Okorn-Schmidt, and T. Zabel, "Physical and electrical characterization of Hafnium oxide and Hafnium silicate sputtered films", *J. Appl. Phys.*, Vol. 90, pp. 6466-6475, 2001.

[2.5] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "Hafnium and zirconium silicates for advanced gate dielectrics", *J. Appl. Phys.*, Vol. 87, pp. 484-492, 2000.

[2.6] H. Y. Yu, N. Wu, M. F. Li, C. Zhu, B. J. Cho, D.-L. Kwong, C. H. Tung, J. S. Pan, J. W. Chai, W. D. Wang, D. Z. Chi, C. H. Ang, J. Z. Zheng, and S. Ramanathan, "Thermal stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ on Si", *Appl. Phys. Lett.*, Vol. 81, pp. 3618, 2002.

[2.7] M. A. Quevedo-Lopez et al., "Boron penetration studies from p^+ polycrystalline Si through $HfSi_xO_y$", *Appl. Phys. Lett.*, Vol. 81, pp. 1074-1076, 2002.

[2.8] T. Kawahara, K. Torii, R. Mitsuhashi, A. Muto, A. Horiuchi, H. Ito, and H. Kitajima, "Effect of Hf Sources, Oxidizing Agents, and NH_3/Ar Plasma on the Properties of $HfAlO_x$ Films Prepared by Atomic Layer Deposition", *Jpn. J. Appl. Phys.*, Vol. 43, 4129-4134, 2004.

[2.9] J. Aarik, A. Aidla, H. Mandar, T. Uustare, K. Kukli, and M. Schuisky, "Phase transformations in hafnium dioxide thin films grown by atomic layer deposition at high temperatures", *Applied Surface Science,* Vol. 173, pp. 15-21, 2001.

[2.10] H. Ikeda, S. Goto, K. Honda, M. Sakashita, A. Sakai, S. Zaima, and Y. Yasuda, "Structural and Electrical Characteristics of HfO_2 Films Fabricated by Pulsed Laser Deposition", *Jpn. J. Appl. Phys.,* Vol. 41, 2476-2479, 2002.

Chapter 3

[3.1] H. Oshima and S. Morozumi, "Future trends for TFT integrated circuits on glass substrates", *IEDM Technical Digest*, pp. 157–160, 1989.

[3.2] K. Werner, "The flowering of flat displays", *IEEE Spectrum*, Vol. 34, pp. 40–49, May 1997.

[3.3] A. Takami, A. Ishida, J. Tsutsumi, T. Nishibe, and N. Ibaraki, "Threshold voltage shift under the gate bias stress in low-temperature poly-silicon TFT with the thin gate oxide film", in *Proc. Int. Workshop AM-LCD*, Tokyo, Japan, Jul. 2000, pp. 45–48.

[3.4] M. Y. Um, S.-K. Lee, and H. J. Kim, "Characterization of thin film transistor using Ta_2O_5 gate dielectric", in *Proc. Int. Workshop AM-LCD*, Tokyo, Japan, Jul. 1998, pp. 45–46.

[3.5] Z. Jin, H. S. Kwok, and M. Wong, "High-performance polycrystalline SiGe thin-film transistors using Al_2O_3 gate insulators", *IEEE Electron Device Lett.*, Vol. 19, no. 12, pp. 502–504, Dec. 1998.

[3.6] C.-P. Lin, B.-Y. Tsui, M.-J. Yang, R.-H. Huang, and C.-H. Chien, "High-Performance Poly-Silicon TFTs Using HfO_2 Gate Dielectric", *IEEE Electron Device Lett.*, Vol. 27, no. 5, pp. 360–363, May 2006.

[3.7] B. W. Busch, O. Pluchery, Y. J. Chabal, D. A. Muller, R. L. Opila, J. R. Kwo, and E. Garfunkel, "Materials characterization of alternative gate dielectrics", *MRS Bull.*, Vol. 27, no. 3, pp. 206–211, Mar. 2002.

[3.8] H. S. P. Wong, "Beyond the conventional transistor", *IBM J. Res. Develop.*, Vol. 46, no. 2/3, pp. 133–168, Mar./May 2002.

[3.9] J. F. Conley, Jr., Y. Ono, D. J. Tweet, and W. Zhuang, "Atomic layer deposition of thin hafnium oxide films using a carbon free precursor", *J. Appl. Phys.*, Vol. 93,

no. 1, pp. 712–718, Jan. 2003.

[3.10] X. Zhao and D. Vanderbilt, “First-principles study of structural, vibrational, and lattice dielectric properties of hafnium oxide”, *Phys. Rev. B*, Vol. 65, p. 233106, 2002.

[3.11] T. S. Boscke, S. Govindarajan, C. Fachmann, J. Heitmann, A. Avellan, U. Schroder, S. Kudelka, P. D. Kirsch, C. Krug, P. Y. Hung, S. C. Song, B. S. Ju, J. Price, G. Pant, B. E. Gnade, W. Krautschneider, B.-H. Lee, and R. Jammy, “Tetragonal Phase Stabilization by Doping as an Enabler of Thermally Stable HfO_2 based MIM and MIS Capacitors for sub 50nm Deep Trench DRAM”, *IEDM Technical Digest*, (341011) 2006.

[3.12] B. F. Hung, K. C. Chiang, C. C. Huang, A. Chin, and S. P. McAlister, “High-Performance Poly-Silicon TFTs Incorporating $LaAlO_3$ as the Gate Dielectric”, *IEEE Electron Device Lett.*, Vol. 26, no. 6, pp. 384–386, Jun. 2005.

[3.13] K. H. Lee, J. K. Park, and Jin Jang, “A High-Performance Polycrystalline Silicon Thin Film Transistor with Silicon Nitride Gate Insulator”, *IEEE Trans. Electron Devices*, Vol. 45, no. 12, pp. 2548–2551, Dec. 1998.

[3.14] I.-W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis, and A. Chiang, “Passivation Kinetics of Two Types of Defects in Polysilicon TFT by Plasma Hydrogenation”, *IEEE Electron Device Lett.*, Vol. 12, no. 4, pp. 181–183, Apr. 1991.

[3.15] H.-C. Lin, K.-L. Yeh, M.-H. Lee, Y.-C. Su, T.-Y. Huang, S.-W. Shen, and H.-Y. Lin, “A Novel Methodology for Extracting Effective Density-of-States in Poly-Si Thin-Film Transistors”, *IEDM Technical Digest*, pp. 781–784, 2004.

[3.16] C. A. Dimitriadis, P. A. Coxon, L. Dozsa, L. Papadimitriou, and N. Economou, “Performance of thin-film transistors on polysilicon films grown by low-pressure chemical vapor deposition at various pressures,” *IEEE Trans.*

Electron Devices, Vol. 39, no. 3, pp. 598–606, Mar. 1992.

[3.17] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, and N. Fukushima, "Additional Scattering Effects for Mobility Degradation in Hf-silicate Gate MISFETs", *IEDM Technical Digest*, pp. 621–624, 2002.

[3.18] P. D. Kirsch, M. A. Quevedo-Lopez, H.-J. Li, Y. Senzaki, J. J. Peterson, S. C. Song, S. A. Krishnan, N. Moumen, J. Barnett, G. Bersuker, P. Y. Hung, and B. H. Lee, "Nucleation and growth study of atomic layer deposited HfO_2 gate dielectrics resulting in improved scalling and electron mobility", *J. Appl. Phys*., Vol. 99, no. 2, Jan. 2006.

[3.19] A. Morioka, H. Watanabe, T. Mogami, and et al., "High mobility MISFET with low trapped charge in HfSiO films", *VLSI Tech. Digest 2003*, p. 165.

[3.20] N. Yamauchi, J-J. J. Hajjar, R. Reif, K. Nakazawa, and K. Tanaka, "Characteristics of Narrow-Channel Polysilicon Thin-Film Transistors", *IEEE Trans. Electron Devices*, Vol. 38, no. 8, pp. 1967–1968, Aug. 1991.

[3.21] D. N. Yaung, Y. K. Fang, K. C. Hwang, K. Y. Lee, K. H. Wu, J. J. Ho, C. Y. Chen, Y. J. Wang, M. S. Liang, J. Y. Lee, and S. G. Wuu, "Narrow Width Effects of Bottom-Gate Polysilicon Thin Film ?Transistors", *IEEE Electron Device Lett.*, Vol. 19, no. 11, pp. 429–431, Nov. 1998.

[3.22] H. C. Lin, M. H. Lee, C. J. Su, and S. W. Shen, "Fabrication and Characterization of Nanowire Transistors With Solid-Phase Crystallized Poly-Si Channels", *IEEE Trans. Electron Devices*, Vol. 53, no. 10, pp. 2471–2477, Oct. 2006.

Chapter 4

[4.1] J. F. Yang, Z. L. Xia, G. Du, X. Y. Liu, R. Q. Han, and J.F. Kang, "Coulomb Scattering induced mobility degradation in ultrathin-body SOI MOSFETs with

high-k gate stack", *Solid-State and Integrated Circuit Technology 2006*, pp1315-1317.

[4.2] G. S. Lujan, S. Kubicek, S. De Gendt, M. Heyns, W. Magnus and K. De Meyer, "Mobility Degradation in High-K Transistors: The role of the Charge scattering", *European Solid-State Device Research 2003*, pp. 399-402.

[4.3] T. Yamaguchi, H. Satake, and N. Fukushima, "Degradation of Current Drivability by the Increase of Zr Concentrations in Zr-silicate MISFET", *IEDM Technical Digest*, pp. 663–666, 2001.

[4.4] S. Saito, K. Torii, M. Hiratani, and T. Onai, "Quantitative Understanding of Mobility Degradation due to Remote Charge Scattering", *IWGI 2001*, pp. 116-118.

[4.5] D. Esseni, and A. Abramo, "Modeling of Electron Mobility Degradation by Remote Coulomb Scattering in Ultrathin Oxide MOSFETs", *IEEE Trans. Electron Devices*, Vol. 50, no. 7, pp. 1665–1674, July 2003.

[4.6] Z. Ren, M. V. Fischetti, E. P. Gusev, E. A.Cartier, and M. Chudzik, " Inversion channel mobility in high-κ high performance MOSFETs", *IEDM Technical Digest*, pp. 793–796, 2003.

[4.7] H. –H. Tseng, J. M. Grant, C. Hobbs, P. J. Tobin, Z. Luo, T. P. Ma, L. Hebert, M. Ramon, S. Kalpat, F. Wang, D. Triyoso, D. C. Gilmer, B. E. White, P. Abramowitz, and M. Moosa, "Mechanism of Gm Degradation and Comparison of Vt Instability and Reliability of HfO2, HfSiOx, and HfAlOx Gate Dielectrics with 80 nm Poly-Si Gate CMOS", *IEEE VLSI-TSA International Symposium 2005*, pp 132-133.

[4.8] H. Tanimoto, M. Kondo, T. Enda, N. Aoki, R. Iijima, T. Watanabe, M. Takayanagi, and H. Ishiuchi, "Modeling of Electron Mobility Degradation for HfSiON MISFETs", SISPAD 2006, pp. 47-50.

[4.9] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-κ/Metal-Gate Stake and Its MOSFET Characteristics", *IEEE Electron Device Lett.*, Vol. 25, no. 6, pp. 408–410, June 2004.

[4.10] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high-κ insulator: The role of remote phonon scattering", *J. Appl. Phys.*, Vol. 90(9), 4587 (2001).

[4.11] H. Ota, A. Hirano, Y. Watanabe, N. Yasuda, K. Iwamoto, K. Akiyama, K. Okada, S. Migita, T. Nabatame, and A. Toriumi, "Intrinsic Origin of Electron Mobility Reduction in High-κ MOSFETs – From Remote Phonon to Bottom Interface Dipole scattering-", *IEDM Technical Digest*, pp. 65–68, 2007.

[4.12] K. Torii, Y. Shimamoto, S. Saito, O. Tonomura, M. Hiratani, Y. Manabe, M. Caymax, and J. W. Maes, "The mechanism of mobility degradation in MISFETs with Al2O3 gate dielectric", *2002 Symposium On VLSI Technology Digest of Technical Paper*, (19.2).

[4.13] J. H. Lee, K. Koh, N. I. Lee, M. H. Cho, Y. K. Kim, J. S. Jeon, K. H. Cho, H. S. Shin, M. H. Kim, K. Fujihara, H. K. Kang, and J. T. Moon, "Effect of Polysilicon Gate on the Flatband Voltage Shift and Mobility Degradation for ALD-Al2O3 Gate Dielectric", *IEDM Technical Digest*, 28.3.1-4, 2000.

[4.14] J. Li, and T. P. Ma, "Scattering of silicon inversion layer electrons by metal/oxide interface roughness", *J. Appl. Phys.*, Vol. 62(10), 4212 (1987).

[4.15] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, and H. Satake, "Additional Scattering Effects for Mobility Degradation in Hf-silicate Gate MISFETs", *IEDM Technical Digest*, 26.3.1-4, 2002.

[4.16] C. E. Blat, E. H. Nicollian, and E. H. Poindexter, "Mechanism of negative bias-temperature instability," *J. Appl. Phys.*, Vol. 69, no. 3, pp. 1712–1720, Feb.

1991.

[4.17] S. Ogawa and N. Shiono, “Generalized diffusion-reaction model for the low-field charge-buildup instability at the Si−SiO2 interface,” *Phys. Rev. B, Condens. Matter*, Vol. 51, no. 7, pp. 4218–4230, Feb. 1995.

[4.18] N. Kimizuka, K. Yamaguchi, K. Imai, T. Iizuka, C. T. Liu, R. C. Keller, and T. Horiuchi, “NBTI enhancement by nitrogen incorporation into ultrathin gate oxide for 0.1-μm gate CMOS generation,” in *VLSI Symp. Tech. Dig.*, 2000, pp. 92–93.

[4.19] D. K. Schroder and J. A. Babcock, “Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing,” *J. Appl. Phys.*, Vol. 94, no. 1, pp. 1–18, Jul. 2003.

[4.20] C.-Y. Chen, J.-W. Lee, S.-D. Wang, M.-S. Shieh, P.-H. Lee, W.-C. Chen, H.-Y. Lin, K.-L. Yeh, and T.-F. Lei, “Negative Bias Temperature Instability in Low-Temperature Polycrystalline Silicon Thin-Film Transistors”, *IEEE Trans. Electron Devices*, Vol. 53, no. 12, pp. 2993–3000, Dec. 2006.

[4.21] S. Saito, D. Hisamoto, S. Kimura, and M. Hiratani, “Unified Mobility Model for High-κ Gate Stacks”, *IEDM Technical Digest*, 33.3.1-4, 2003.

[4.22] F. Gamiz, A. Godoy, F. J. Molinos, P. C. Cassinello, and J. B. Roldan, “Remote surface roughness scattering in ultrathin-oxide MOSFETs”, *European Solid-State Device Research 2003*, pp. 403-406.

[4.23] W. J. Zhu, and T. P. Ma, “Temperature Dependence of Channel Mobility in HfO_2-Gated NMOSFETs”, *IEEE Electron Device Lett.*, Vol. 25, no. 2, pp. 89–91, Feb. 2004.

[4.24] P. D. Kirsch, M. A. Quevedo-Lopez, H.-J. Li, Y. Senzaki, J. J. Peterson, S. C. Song, S. A. Krishnan, N. Moumen, J. Barnett, G. Bersuker, P. Y. Hung, and B. H. Lee, “Nucleation and growth study of atomic layer deposited HfO_2 gate

dielectrics resulting in improved scalling and electron mobility", *J. Appl. Phys*., Vol. 99, no. 2, Jan. 2006.

[4.25] C. F. Yeh, S. S. Lin, T. Z. Yang, C. L. Chen, and Y. C. Yang, "Performance and Off-State Current Mechanisms of Low-Temperature Processed Polysilicon Thin-Film Transistors with Liquid Phase Deposited SiO_2 Gate Insulator", *IEEE Trans. Electron Devices*, Vol. 41, no. 2, pp. 173–179, Feb. 1994.

[4.26] C. T. Angelis, C. A. Dimitriadis, I. Samaras, J. Brini and G. Kamarinos, V. K. Gueorguiev, and Tz. E. Ivanov, "Study of leakage current in n-channel and p–channel polycrystalline silicon thin-film transistors by conduction and low frequency noise measurements", *J. Appl. Phys.*, Vol. 82, no. 8, Oct. 1997.

[4.27] M. Hack, I.-W. Wu, T. J. King, and A. G. Lewis, "Analysis of Leakage Currents in Poly-Silicon Thin Film Transistors", *IEDM Technical Digest*, pp. 385–388, 1993.

[4.28] M. Yazaki, S. Takenaka, and H. Ohshima, "Conduction Mechanism of Leakage Current Observed in Metal-Oxide-Semiconductor Transistors and Poly-Si Thin-Film Transistors", *Jpn. J. Appl. Phys.*, Vol. 31, no. 2A, pp. 206–209, Feb. 1992.

[4.29] C. H. Kim, K.-S. Sohn, and J. Jang, "Temperature dependent leakage currents in polycrystalline silicon thin film transistors", *J. Appl. Phys.*, Vol. 81, no. 12, Jun. 1997.

[4.30] S. Zafar, A. Callegari, E. Gusev, and M. V. Fischetti, "Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks", *J. Appl. Phys.*, Vol. 93, no. 11, pp. 9298–9303, Jun. 2003.

[4.31] W.-T. Lu, P.-C. Lin, C.-H. Chien, M.-J. Yang, I.-J. Huang, P. Lehnen, and T.-Y. Huang, "The characteristics of hole trapping in HfO2/SiO2 gate dielectrics with TiN gate electrode", *Appl. Phys. Lett.*, Vol. 85, no. 16, pp. 3525–3527, Oct.

2004.

[4.32] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, “Conductivity behavior in polycrystalline semiconductor thin film transistors,” *J. Appl. Phys.*, Vol. 53, no. 2, pp. 1193–1202, Feb. 1982.

[4.33] R. E. Proano, R. S. Misage, and D. G. Ast, “Development and electrical properties of undoped polycrystalline silicon thin-film transistor,” *IEEE Trans. Electron Devices*, Vol. 36, no. 9, pp. 1915–1922, Sep. 1989.

Appendix

Physical and Electrical Properties of Ge Films Grown by Inductively Coupled Plasma Chemical Vapor Deposition at Low Temperature on SiO_2 Substrates

A-1 Introduction

Germanium is increasingly attracting attention because of its wide applications in ULSI and nanotechnology. Ge/Si and SiGe/Si heterostructures have been used in high-performance devices because of their higher electron and hole mobilities relative to those of Si [A.1]-[A.5]. Three-dimensional Ge islands formed on Si surfaces through solid phase epitaxy have great potential for use in fabricating nanostructures [A.6]. In addition, Ge on insulators (GOIs) are especially desirable for the preparation of extremely high performance metal oxide silicon field-effect transistors (MOSFETs) exhibiting sufficiently low leakage currents [A.7]-[A.8]. For thin film transistor (TFT) applications, poly-Ge deposited using molecular beam epitaxy (MBE) has been applied to replace the poly-Si channel because poly-Ge exhibits higher field effect mobility [A.9]. Successful Ge thin film deposition directly on SiO_2 substrates using chemical vapor deposition (CVD) techniques has not been demonstrated previously, however, because an extremely long incubation time is required [A.10]-[A.16]. Nevertheless, CVD has the advantage of uniformity control, which is highly critical in large

dimension substrates and mass production, compared with such techniques as sputtering [A.17] and e-gun deposition [A.18]-[A.19].

In this chapter, firstly, we demonstrate the deposition of polycrystalline Ge films directly on top of fully-SiO_2-covered Si substrates with nearly no incubation time by using inductively coupled plasma chemical vapor deposition (ICP-CVD) technique at 400°C. X-ray photoelectron spectroscopy (XPS) and Auger electron spectroscopy (AES) analyses show that the deposition of very pure Ge thin films can be achieved without significantly detectable O and C incorporations. X-ray diffraction (XRD) patterns clearly illustrate that the deposited Ge films are of cubic structure with primarily (111), (220), and (311) orientations, and are mainly composed of small grains with sizes around 14nm calculated from full width at half maximum (FWHM). Moreover, the results of high-resolution transmission electron microscopy (HRTEM) analysis firmly show that only very short incubation time is needed for the deposition.

However, such a high deposition temperature causes overheating of the plasma windows (the top plate for plasma generation) and leads to the formation of abundant particles, which is detrimental to the quality of Ge films. Increasing the cooling interval from run to run could relieve the overheating of the plasma window, but it would decrease the throughput. Therefore, we tried to lower the deposition temperature to 300°C to prevent overheating of the plasma window and examined the properties of the resultant thin films. In addition, we found that the mechanism of deposition was related to a hydrogen etching effect from the plasma, rather than a gas phase reaction or carbon contamination. To enhance the grain size and quality of the as-deposited Ge films at lower temperature, we performed a re-crystallization process using SiN_x capping layer. Finally, we investigated the electrical characteristics of n- and p-doped polycrystalline Ge thin films.

A-2 Characterizations of Polycrystalline Ge Films on SiO_2 Substrate by ICP-CVD at 400°C

A-2.1 Experimental

After standard cleaning, a 550nm-thick SiO_2 layer was grown thermally on p-type 150mm Si(100) wafers. Before starting the Ge film deposition, the reaction chamber was cleaned by CF_4/O_2 mixtures at 400°C. Next, the Ge films were deposited with different deposition times, from 10s to 720s at 400°C, by ICP-CVD system. The base pressure of the reaction chamber was 10 mtorr and the gas species were GeH_4 (3 sccm) and H_2 (150 sccm). The plasma generation RF power from an ICP generator (13.56 MHz) was 500W with no additional bottom RF power supply. XPS and AES systems were used to detect the composition and contamination of the deposited Ge films. Atomic force microscopy (AFM) was used to determine the film roughness. The crystalline properties and thicknesses of the Ge films were evaluated by XRD and TEM measurements.

A-2.2 Structural Characterization of Deposited-Ge Films by XPS, AES, XRD, and TEM Analysis

Figure A-1 shows the XPS spectrum of an as-grown Ge film. A very sharp Ge peak located at the binding energy of 29.5 eV with a small shoulder at higher binding energy can clearly be seen. The origin of the shoulder is attributed to the presence of GeO_2, which is believed to be formed by surface oxidation when the sample is exposed to air rather than the incorporation in the bulk. This assumption can be further identified by the AES profile, shown in Figure A-2. Obviously, both O and C signals only appear significantly near the surface region supplying the evidence that very pure Ge films can be successfully deposited directly on top of fully-SiO_2-covered substrates.

Figure A-3 displays the resultant XRD spectrum of the deposited Ge film. Three

main peaks corresponding to cubic (111), (220), and (311) orientations, respectively, can be unequivocally found. Hence, the deposited Ge film is polycrystalline. The grain sizes, roughly calculated by Scherrer's formula (**$D= 0.9\lambda / B \cos\Theta$),** for the (111), (220), and (311) orientations are 11.4, 17.1, and 12.4 nm, respectively. The mean grain size around 14nm leads to a rather smooth surface of approximately 1nm in the root-mean-square (RMS) examined by AFM image, as shown in Figure A-4, which seems very suitable for the TFT applications.

Figures A-5 (a)-(d) show the images of TEM and diffraction patterns of the deposited Ge thin films for various deposition times (30sec, 60sec, 180sec and 600sec). Better crystallinity toward top surface of the film can be obtained as the deposition time increases. Figure A-6 shows the film thickness versus deposition time. At the initial stage, the growth kinetic is strongly surface-dependent, and, thus, slower deposition rates are observed. Once the thin film has fully covered the SiO_2 substrate, the reaction becomes faster on the resultant Ge surface and the grains begin to grow [A.20]. In strong contrast to previous reports with other CVD systems [A.12]-[A.14], [A.21]-[A.22], our results certainly suggest that ICP-CVD can achieve the Ge deposition on the SiO_2 substrates with nearly no incubation time. This might be owing to the fact that the high density of H ions will slightly etch the SiO_2 surface and partially reduce SiO_2 into Si or SiO_x [A.23]. Those exposed Si bonds on the surface can then enhance the adsorption probability of Ge atoms and act as the nucleation sites for the subsequent Ge deposition [A.11], [A.15]. This mechanism would be discussed in detail in next section.

The relationship between the growth rate and the crystallinity of the layers can be explained by the following growth mechanism. The pair correlation function g(r)=density(r)/density(0) describes the radial distribution function of the atoms in the crystal on an atomic scale with density(0) as the mean density of the system and density

(r) the probability density to find an atom at the distance r. Therefore, different crystalline structures lead to different characteristic atoms distribution patterns and amorphous structures do not show an ordered distribution [A.24]. The correlation length is the thermodynamic parameter of the system which defines the critical size of the ordered phase which is needed to stabilize the phase: g(r) ~exp (A/correlation length), with A as a scaling factor. If the region is below this critical size it is still amorphous even though it might have local ordering. Typically a few lattice cells are needed to establish a stable crystalline phase. In order to obtain a three-dimensional crystalline phase, the layer thickness needs to overcome the correlation length. But, defects and lattice-mismatch-induced strains in the nucleation layer are breaking the correlation between the atoms in the crystalline phase. The claimed Si bonds might support both, defects at the interface and a lattice mismatch. In addition, induced stresses due to the two-dimensionality of thin layers lead to an anisotropic distribution of the correlation length regarding the in-plane and out-of-plane components. Depending on the total layer thickness and the number of defects this leads to a clustering of the layer in the amorphous phase and grains in the crystalline phase, respectively. Very high amounts of defects can even keep the layer amorphous by reducing the crystalline correlation below the correlation length. Therefore, the more defects and strains are in the layer the less pronounced is the crystalline phase in the thin films leading to smaller average grain sizes [A.25]. Thick Ge layers are relaxed and, hence, show a higher amount of crystallinity compared with the thin layers. Low growth rates can also support the crystallinity by giving the Ge atoms more time to diffuse on the growing surface and moving defects to the grain boundaries, like carbon contaminations for example. Since the growth rate of crystallites is typically higher than that of amorphous materials, it explains that the observed growth rate increase due to the established crystalline phase at a certain Ge layer thickness.

However, such a high deposition temperature causes overheating of the plasma windows and leads to the formation of an abundance of particles, which is obviously detrimental to the quality of Ge films. Therefore, we tried to lower the deposition temperature to 300°C to prevent overheating of the plasma window and determined the properties of the resultant thin films as described in the next section.

A-3 Physical and Electrical Properties of Ge Films Deposited at 300°C by ICP-CVD System

A-3.1 Experimental

After standard cleaning, 550nm-thick SiO_2 layers were grown thermally on p-type Si(100) wafers in a furnace. Subsequently, the oxidized wafers were transferred to a process chamber of ICP-CVD system. Prior to depositing the first Ge film, the reaction chamber was cleaned using a CF_4/O_2 mixture at 350°C. And then, Ge films were deposited using the ICP-CVD system at a deposition temperature of either 300 or 400°C. The process pressure of the reaction chamber was 50 mtorr; the gas species were GeH_4 (3 sccm), H_2 (150 sccm), and Ar (30 sccm). The plasma generation RF power from an ICP generator (13.56 MHz) was 500 W; no additional bottom RF power supply was used. Simultaneously, the other experiment about plasma treatment using only hydrogen plasma was also performed on the oxidized wafer to observe the H_2 etching effect. A SiN_x layer, deposited using a SiH_4/NH_3 mixture at 375°C, was also deposited using the ICP-CVD system to cap the Ge films prior to their re-crystallization to reduce the extent of any reactions with residual oxygen. After deposition, the Ge films were re-crystallized in the furnace and in a rapid thermal annealing (RTA) system to enhance the crystalline properties of the low temperature-grown Ge films. Dopant activation of the Ge films, which was conducted in the RTA system at various temperatures under an N_2 atmosphere, was followed by the implantation of boron and phosphorus using a

dosage of 5×10^{15} cm^{-2} at 50 and 130 keV, respectively. Scanning electron microscopy (SEM) was used to identify the physical thickness of the Ge films and, hence, to calculate the rate of deposition. X-ray photoelectron spectroscopy (XPS) and Auger electron spectroscopy (AES) were employed to detect the composition and contamination of the deposited Ge films. The crystalline properties of the Ge films were evaluated through X-ray diffraction (XRD) measurements. Atomic force microscopy (AFM) was used to determine the film roughness. The sheet resistance of the activated Ge films was measured using a four-point probe system.

A-3.2 Structural Characterization of Lower-Temperature Deposited-Ge Films

Plasma-enhanced CVD and high-density plasma CVD systems were designed for applications requiring low temperatures. Although high substrate temperatures can enhance the quality of the as-deposited film, they should not be too high so that they have a negative effect on processing. During deposition, the top plate for plasma generation is hot; a substrate at higher temperature will lead to a hotter plasma window. In addition, the coated films on the top plate might become cracked as a result of overheating and might create many particles on the deposited Ge films. Although increasing the cooling interval can prevent these phenomena from occurring, the throughput would decrease accordingly, which would not be favorable for mass production. To reduce the overheating of the plasma window, we sought to lower the deposition temperature to 300°C. Figure A-7 displays XPS spectra of the as-grown Ge films deposited at 300 and 400°C. Consistent with our previous findings, a very sharp Ge peak is clearly evident for each sample at a binding energy of 29.2 eV, with a small shoulder at higher binding energy, which we attribute to the formation of surface GeO_2 through oxidation when the sample is exposed to air. The AES profile of the Ge film

deposited at 300°C (Fig. A-8) confirms that the oxygen atoms are present on the surface and not incorporated into the bulk: signals for O and C atoms both appear near the surface, but their intensity decreases abruptly thereafter. We obtained a similar result in our previous study of a Ge film deposited at 400°C. According to these XPS and AES data, we believe that very pure Ge films can be deposited directly onto SiO_2-covered substrates at 300°C. The major drawback of performing deposition at such a low temperature is that the intensity of the GeO_2 peak is slightly stronger. We suspect that this phenomenon may be related to the formation of a thick surface-oxidized GeO_2 layer, which is formed over the surface because of the poor crystallinity of the low temperature-grown Ge film.

Figure A-9 provides a comparison of the film thickness obtained at various deposition time and temperature. A faster deposition rate (24 nm/per min) occurs for the sample deposited at 300°C, presumably because of a lower migration rate and a lower desorption rate of the Ge radicals on the surface at lower temperature. From XRD analyses (Fig. 5-10), we found that the sample deposited at 300°C possesses the same cubic structure, but with a smaller grain size (around 13.9nm), as that deposited at 400°C (around 16.7nm). Nevertheless, the faster deposition rate results in poorer crystallinity of Ge films, but re-crystallization process could be used to enhance the crystallinity of the deposited Ge film (see A-3.4).

A-3.3 The Deposition Mechanism of Ge Films by ICP-CVD

No previous reports have described the successful deposition of Ge thin films on SiO_2 substrates using CVD techniques because of the extremely long incubation time required [A.12]-[A.14], [A.21]-[A.22]. In our experiments, we noted that the deposition of Ge onto SiO_2 substrates in an ICP-CVD system can be achieved with nearly no incubation time. We speculate that this result is due to the fact that the high density of H

radicals will slightly etch the SiO_2 surface and partially reduce SiO_2 groups into Si or SiO_x units. Those exposed Si dangling bonds on the surface or newly-formed Si-H interface could act as nucleation sites enhancing the probability of adsorption of Ge atoms. Our hypothesis is based on two factors: (i) A previous paper reported that feeding SiH_4 gas into the chamber prior to deposition helps to form the nucleation sites on the SiO_2 surface, which reduces considerably the incubation time for the following Ge deposition [A.15]. (ii) Hydrogen etching effects have been observed previously in other plasma systems [A.23], [A.26], with the hydrogen radicals' etching of the SiO_2 surface resulting in the presence of the additional Si peak in XPS spectrum. Unlike other CVD systems, radicals of high energy can be generated during high-density plasma CVD, such as in ICP and ECR CVD systems. The sheath layer would accelerate these radicals, such that slight etching of the sample surface would occur even in the absence of a bottom RF bias. To prove our hypothesis, we performed an etching test using H_2 plasma in our ICP-CVD system. The oxidized wafer was transferred to the process chamber and treated with H_2 plasma at 300°C for 30s under an RF power of 500W; no additional bottom RF power was applied. Because hydrogen atoms are so small, it is not easy to generate a stable plasma at low pressure; thus, we increased the process pressure from 10 to 50 mtorr and fed Ar gas into the chamber during the processing to overcome this problem. Figure A-11 displays XPS spectra of the samples prepared with and without H_2 etching. From figure A-11(a), we observe a clear Si^{4+} peak for both samples, but an additional Si peak appears in the spectrum of the sample obtained after H_2 plasma etching, which is consistent with previous findings [A.26]. In addition, the signal for the O atoms (i.e., for SiO_2 and SiO_x units) is broadened for the sample subjected to H_2 plasma etching, as shown in Fig. A-11(b), suggesting that the additional Si and SiO_x bonds that were created after H_2 plasma etching acted as nucleation sites for subsequent deposition of Ge atoms, which is consistent with our hypothesis.

A-3.4 Characterizations of the Re-Crystallization Ge Films

Although the Ge films could be deposited successfully at 300°C, they exhibited poor crystallinity. To enhance the qualities of the as-deposited Ge films, we utilized furnace and RTA methods to re-crystallize them. Figure A-12 displays XRD spectra of the as-deposited Ge film and the resultant samples after re-crystallization at 400°C for various times in the furnace system under a N_2 ambient. We observe three main peaks corresponding to cubic (111), (220), and (311) orientations, respectively. As the annealing time increases, the mean grain size of re-crystallized Ge films increases, suggesting that the quality of Ge films has improved. After re-crystallization for 4 h, the grain sizes for the (111), (220), and (311) orientations, calculated roughly using Scherrer's formula ($D = 0.9\lambda/B \cos\Theta$), are 10.3, 19.1, and 13.9 nm, respectively. The mean grain size (around 14.4 nm) is slightly larger than that in the as-deposited Ge film. Accordingly, we have determined that pure Ge films can be deposited at a lower substrate temperature of 300°C and the quality of the as-deposited film can be enhanced through re-crystallization. We noted, however, that an additional peak near (111), which we assign to GeO_x species, emerged in the XRD spectra when samples were subjected to anneal of longer than 4 h. This phenomenon might be caused by the residual oxygen in furnace, which would react with the Ge film to form GeO_x during longer annealing processes. When we increased the annealing temperature to 500°C, parts of the Ge film peeled off as a result of the decomposition of GeO_x after 1 h of annealing. To eliminate the formation of GeO_x during re-crystallization, we capped a SiN_x layer of around 50 nm in thickness over the Ge film to prevent it from reacting directly with residual oxygen. This SiN_x layer suppresses the intensity of the GeO_x peak dramatically after long-duration, higher-temperature re-crystallization (Fig. A-13). The average grain size of the re-crystallized Ge films featuring a SiN_x capping layer increases to around 16.7

nm, significantly larger than those for the uncapped samples. We also employed the RTA system in an attempt to enhance the crystallinity of the Ge films with a shorter time. Figure A-14 displays XRD spectra of the Ge films that we re-crystallized in the RTA system at various re-crystallization temperatures and times. We observed that the polycrystalline cubic structure was retained after RTA treatments and that the grain size increased upon increasing the annealing time or temperature. Moreover, the weak GeO_x peak was nearly eliminated completely after annealing at higher temperatures. We suspected that the density of the Ge film would be improved after higher-temperature annealing and that the degree of surface oxidation would be reduced because of the higher density of the re-crystallized Ge film. Figure A-15(a) and (b) display the images of TEM and diffraction patterns of the deposited Ge films at 300°C and the sample after RTA treatment (700°C, 30sec, N_2 ambient). Obviously, better crystallinity of the Ge film could be found after RTA treatment, which is consistent with our XRD results. Table A-1 summarizes the grain sizes, calculated using Scherrer's formula, of the Ge films treated with the various different re-crystallization methods. Figure A-16 displays the variation in surface roughness of the re-crystallized Ge films as a function of the RTA temperature. The capping SiN_x layer would be removed by buffer-oxide-etch (BOE) solution and then sent to AFM measurements. The surface roughness of re-crystallized Ge films initially decreased after annealing at 600°C because of the smaller grains, but then increased after annealing at temperatures greater than 700ºC as the grains grew. Nevertheless, the RMS values of the surface roughness remained small for all samples. Figure A-17 displays AFM images of the as-deposited Ge film and the samples with RTA treatments. Although larger grains could be obtained after annealing at 800°C (Fig. A-16(c)), some voids are also formed as a result of the decomposition of GeO_x units. In summary, the use of a capping SiN_x layer suppresses GeO_x formation during the densification and the use of RTA methods enhance the crystallinity and grain size of the

deposited Ge films more efficiently.

A-3.5 Electrical Characteristics of Doped Ge Films

Figures A-18(a) and (b) provide plots of the sheet resistance as a function of RTA temperature for polycrystalline Ge (poly-Ge) and Si (poly-Si) films implanted with phosphorus and boron dopants, respectively. Prior to implantation, the poly-Ge films underwent RTA re-crystallization (700°C, 60 s) in a N_2 ambient; the poly-Si films were subjected to furnace re-crystallization (600°C, 24 h) in a N_2 ambient, i.e., under conditions used for poly-Si channel TFT devices. The RTA activation time for each sample after implantation was maintained constant at 60 sec. For the n-type-doped films, the sheet resistance of the implanted poly-Si films decreases as the RTA temperature increases, and the dopant becomes activated at temperatures greater than 600°C. In contrast, the sheet resistance of the implanted poly-Ge films increases initially but then decreases abruptly at temperatures greater than 500°C. The minimum sheet resistance of the poly-Ge films (231 Ω/square) is obtained at an annealing temperature of 550°C; the sheet resistance increases upon increasing the RTA temperature above 600°C. The activation behavior of phosphor and boron implants in Ge has been investigated extensively [A.27]-[A.31]. The activation efficiency of phosphorus dopants is poor: only a small fraction of the implanted dosage can be activated after RTA treatment. Furthermore, the dopant exhibits rapid diffusion, which, in turn, leads to a significant loss of dopant in the Ge case. As a result, we suspect that the increase in sheet resistance of the n-type dopants as the RTA temperature increases to above 600°C is due to the decreased dose of activated dopant and the increased dose loss at higher annealing temperatures. In contrast to the behavior of phosphorus, a high proportion of boron is electrically active immediately after implantation and it undergoes negligible diffusion in Ge after annealing. As a result, the sheet resistance for the p-type-doped poly-Ge and

poly-Si films exhibits similar trends. The implanted poly-Ge films are activated at 500°C and reach the minimum sheet resistance (105 Ω/square) at 550°C. There is only a slight increase in the sheet resistance when the annealing temperature is increased up to 750°C; this behavior may also be related to loss of the dopant when the annealing temperature is high. These results indicate that a low thermal budget is required for activation of the dopant, which seems to be very suitable for the fabrication of TFT devices on glass substrates.

A-4 Unfinished Low-Temperature Poly-Ge TFTs

Through the optimization of the Ge films deposited by ICP-CVD and the analysis of electrical properties, the final objective is to fabricate the low temperature poly-Ge TFTs successfully. However, the easily oxidized Ge films and water-soluble GeO_2 would be the major problems for the device fabrication. The severe oxidation between the deposited-SiO_2 gate-dielectrics and poly-Ge channel interface could be seen clearly through the TEM image, as shown in Figure A-19. To solve this problem, we tried to use the deposited-SiN_x film to replace the conventional gate dielectric. Obviously, the much better interface and the complete device structure could be found in Figure A-20. Nevertheless, the device still failed again and could not be turn on normally in the electrical measurements. We consider that further improvements of the Ge film quality and process optimization have to be executed to accomplish the successful fabrication of low-temperature poly-Ge TFTs.

A-5 Summary

We have investigated the physical and electrical properties of Ge films deposited directly using ICP-CVD techniques onto SiO_2-covered Si substrates. The deposition of very pure Ge thin films could be achieved at low temperatures (300°C and 400°C)

without significant incorporation of O and C atoms. The mechanism of deposition is consistent with hydrogen etching effect. Re-crystallization in an RTA system rapidly improves the quality and smoothness of the Ge films. As a result, the adaptable sheet resistance of the poly-Ge films could be achieved at lower activation temperatures, making them more suitable for use in low-temperature TFT device fabrication processes.

A-6 References

[A.1] H. Jorke and H. J. Herzog, "Mobility Enhancement in Modulation-Doped Si-$Si_{1-x}Ge_x$ Superlattice Grown by Molecular Beam Epitaxy", *J. Electrochem. Soc.*, Vol. 133, pp. 998–1001, 1986.

[A.2] H. Shinoda, M. Kosaka, J. Kojima, H. Ikeda, S. Zaima and Y. Yasuda, "Electrical properties of metal/$Si_{1-x}Ge_x$/Si(100) heterojunctions", *Appl. Surf. Sci.*, Vol. 100-101, pp. 526–529, 1996.

[A.3] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "Germanium MOS capacitors incorporating ultrathin high-κ gate dielectric", *IEEE Electron Device Lett.*, Vol. 23, pp. 473–475, 2002.

[A.4] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS characteristics with CVD HfO_2 gate dielectrics and TaN gate electrode", *2003 Symposium on VLSI Technology*, Digest of Technical Papers, p. 121-122.

[A.5] H. Shang, H. Okorn-Schimdt, J. Ott, P. Kozlowski, S. Steen, E. C. Jones, H.-S. P. Wong, and W. Hanesch, "Electrical characterization of germanium p-channel MOSFETs", *IEEE Electron Device Lett.*, Vol. 24, pp. 242–244, 2003.

[A.6] H. Hibino, N. Shimizu and Y. Shinoda, "Mesh pattern of Ge islands grown using solid phase epitaxy", *J. Vac. Sci. Technol*. A, Vol. 11, pp. 2458–2462, 1993.

[A.7] C. H. Huang, M. Y. Yang, A. Chin,W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, "Very low defects and high performance Ge-on-insulator p-MOSFETs with Al_2O_3 gate dielectrics", *2003 Symposium on VLSI Technology*, Digest of Technical Papers, p. 119-120.

[A.8] S.-I. Takagi, "Re-examination of subband structure engineering in ultra-short channel MOSFETs under ballistic carrier transport", *2003 Symposium on VLSI Technology*, Digest of Technical Papers, p. 115-116.

[A.9] T. Sadoh, H. Kamizuru, A. Kenjo, and M. Miyao, “Low-temperature formation (<500 °C) of poly-Ge thin-film transistor with NiGe Schottky source/drain”, *Appl. Phys. Lett.*, Vol. 89, (192114), 2006.

[A.10] D. Dentel, J. L. Bischoff, T. Angot, and L. Kubler, “ The influence of hydrogen during the growth of Ge films on Si(001) by solid source molecular beam epitaxy”, *Surf. Sci.*, Vol. 402–404, pp. 211–214, 1998.

[A.11] M. Okada, A. Muto, I. Suzumura, H. Ikeda, S. Zaima, and Y. Yasuda, “Hydrogen Effects on Heteroepitaxial Growth of Ge Films on Si(111) Surfaces by Solid Phase Epitaxy”, *Jpn. J. Appl. Phys.*, part 1, No. 12B, Vol. 37, pp. 6970–6973, 1998.

[A.12] Q. Li, S. M. Han, S. R. J. Brueck, S. Hersee, Y. B. Jiang, and H. Xu, “Selective growth of Ge on Si(100) through vias of SiO_2 nanotemplate using solid source molecular beam epitaxy”, *Appl. Phys. Lett.*, Vol. 83, No.24, pp. 5032–5034, 2003.

[A.13] S. Kobayashi, M. Sakuraba, T. Matsuura, J. Murota, and N. Mikoshiba, “Initial growth characteristics of germanium on silicon in LPCVD using germane gas”, *J. Cryst. Growth*, Vol. 174, pp. 686–690, 1997.

[A.14] M. Racanelli and D. W. Greve, “Low-temperature selective epitaxy by ultrahigh-vacuum chemical vapor deposition from SiH_4 and GeH_4/H_2”, *Appl. Phys. Lett.*, Vol. 58 (19), pp. 2096-2098, 1991.

[A.15] T. Baron, B. Pelissier and et al., “Chemical vapor deposition of Ge nanocrystals on SiO_2”, *Appl. Phys. Lett.*, Vol. 83(07), pp. 1444-1446, 2003.

[A.16] Y. Liu, M. D. Deal, and J. D. Plummer, “High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates”, *Appl. Phys. Lett.*, Vol. 84 (14), pp. 2563-2565, 2004.

[A.17] K. Egami and A. Ogura, “Germanium film on SiO_2 with a <100> texture

deposited by the rf sputtering technique", *Appl. Phys. Lett*., Vol. 47, pp. 1059–1061, 1985.

[A.18] D. Shahrjerdi, B. Hekmatshoar, S. Mohajerzadeh, and S. Darbari, " *ICM 2003*, pp. 361–364.

[A.19] J. L. Xu, J. L. Chen, and J. Y. Feng, "Growth of Ge films by cluster beam deposition", *Nucl. Instrum. Methods Phys. Res., Sect B*, Vol. 194, pp. 297–301, 2002.

[A.20] Y. Kajikawa, T. Tsuchiya, S. Noda and H. Komiyama, "Incubation Time During the CVD of Si onto SiO_2 from Silane", *Chem. Vap. Deposition*, Vol. 10, No. 3, pp. 128-133, 2004.

[A.21] H. Ishii, Y. Takahashi, and J. Murota, "Selective Ge deposition on Si using thermal decomposition of GeH_4", *Appl. Phys. Lett.*, Vol. 47, no. 8, pp. 863-864, 1985.

[A.22] J. Hanna, and K. Shimizu, "Low-temperature growth of polycrystalline Si and Ge films by redox reactions of Si_2H_6 and GeF_4", *J. Organomet. Chem.*, Vol. 611, pp. 531–536, 2000.

[A.23] B.-T. Lee, T. R. Hayes, P. M. Thomas, R. Pawelek, and P. F. Sciortino, Jr., "SiO_2 mask erosion and sidewall composition during CH_4/H_2 reactive ion etching of InGaAsP/lnP", *Appl. Phys. Lett*., Vol. 63, no. 23, pp. 3170-3172, 1993.

[A.24] R. Haberland, S. Fritzsche, G. Peinel and K. Heinzinger, *Molekulardynamik*, Vieweg, Braunschweig 1995.

[A.25] Y. Z. Hu, C. Y. Zhao, C. Basa, W. X. Gao, and E. A. Irene, "Effects of hydrogen surface pretreatment of silicon dioxide on the nucleation and surface roughness of polycrystalline silicon films prepared by rapid thermal chemical vapor deposition", *Appl. Phys. Lett.*, Vol. 69**,** no**.** 4, pp. 485-487, 1996.

[A.26] T. Matsuura, T. Ohmi, J. Murota, and S. Ono, "Inversion from selective

homoepitaxy of Si to selective Si film deposition on SiO_2 using ;in ultraclean electron cyclotron resonance plasma", *Appl. Phys. Lett.*, Vol. 61, no. 24, pp. 2908-2910, 1992.

[A.27] C. H. Poon, L. S. Tan, B. J. Cho, and A. Y. Du, "Dopant Loss Mechanism in n+/p Germanium Junctions during Rapid Thermal Annealing", *J. Electrochem. Soc.*, Vol. 152, G895–G899, 2005.

[A.28] A. Satta, E. Simoen, R. Duffy, T. Janssens, T. Clarysse, A. Benedetti, M. Meuris, and W. Vandervorst, "Diffusion, activation, and regrowth behavior of high dose P implants in Ge", *Appl. Phys. Lett.*, Vol. 88, (162118), 2006.

[A.29] B. J. Pawlak, R. Surdeanu, B. Colombeau, A. J. Smith, N. E. B. Cowern, R. Lindsay, W. Vandervorst, B. Brijs, O. Richard, and F. Cristiano, "Evidence on the mechanism of boron deactivation in Ge-preamorphized ultrashallow junctions", *Appl. Phys. Lett.*, Vol. 84, no. 12, pp. 2055–2057, 2004.

[A.30] Y. S. Suh, M. S. Carroll, R. A. Levy, G. Bisognin, D. De Salvador, M. A. Sahiner, and C. A. King, "Implantation and Activation of High Concentrations of Boron in Germanium", *IEEE Trans. Electron Devices*, Vol. 52, no. 11, pp. 2416–2421, 2005.

[A.31] Q. Zhang, J. Huang, N. Wu, G. Chen, M. Hong, L. K. Bera, and C. Zhu, "Drive-Current Enhancement in Ge n-Channel MOSFET Using Laser Annealing for Source/Drain Activation", *IEEE Electron Device Lett.*, Vol. 27, no. 9, pp. 728–730, 2006.

Table A-1

The grain size of the as-deposited Ge film capped with SiN_x layer and after re-crystallization with various re-crystallization methods, annealing temperatures, and durations.
The thicknesses of Ge films are around 160nm.

Furnace / Orientation	300°C deposited	400°C 4h	400°C 8h	400°C 12h	500°C 8h	600°C 8h
(111)	9.3 nm	15.1 nm	12.6 nm	13.2 nm	14.6 nm	12.2nm
(220)	18.7 nm	19.1 nm	19.6 nm	20.5 nm	20.0 nm	20.0 nm
(311)	13.7 nm	15.9 nm	15.6 nm	16.8 nm	15.4 nm	15.9 nm
RTA / Orientation	**300°C deposited**	**600°C 60sec**	**600°C 180sec**	**700°C 60sec**	**800°C 30sec**	**800°C 60sec**
(111)	9.3 nm	8.8 nm	11.2 nm	18.2 nm	19.5 nm	20.4 nm
(220)	18.7 nm	16.9 nm	17.9 nm	22.7 nm	23.9 nm	23.9 nm
(311)	13.7 nm	13.3 nm	13.9 nm	21.2 nm	21.7 nm	22.8 nm

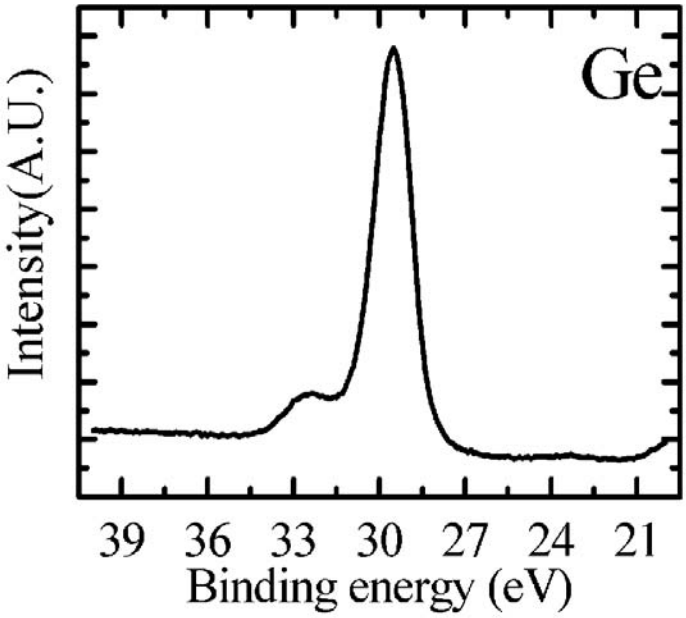


Figure A-1 The spectrum of Ge 3d level by XPS measurement, which revealed the surface conditions of the as-grown Ge films deposited onto SiO_2 substrate at 400°C.

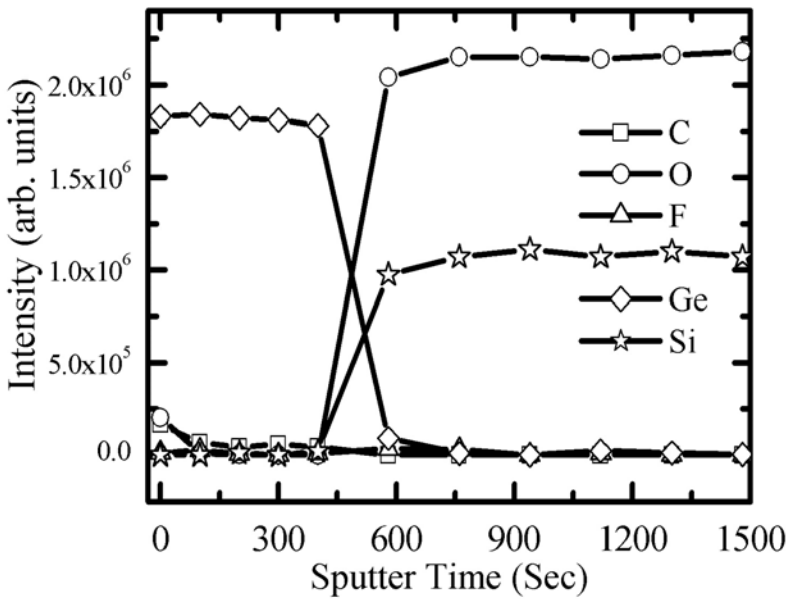


Figure A-2 AES depth profiles of Ge film deposited onto SiO_2 substrate at 400°C.

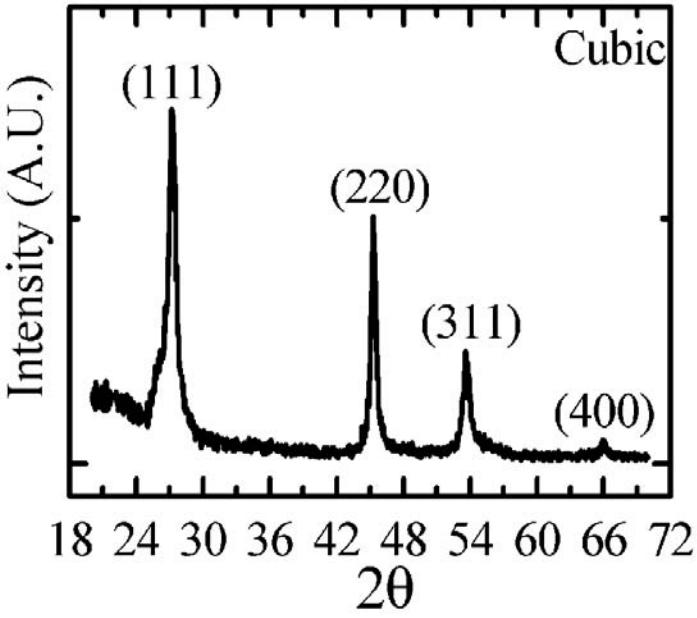


Figure A-3 X-ray diffraction patterns of Ge film deposited at 400°C on SiO_2 substrate. The thickness of the Ge film is around 100nm.

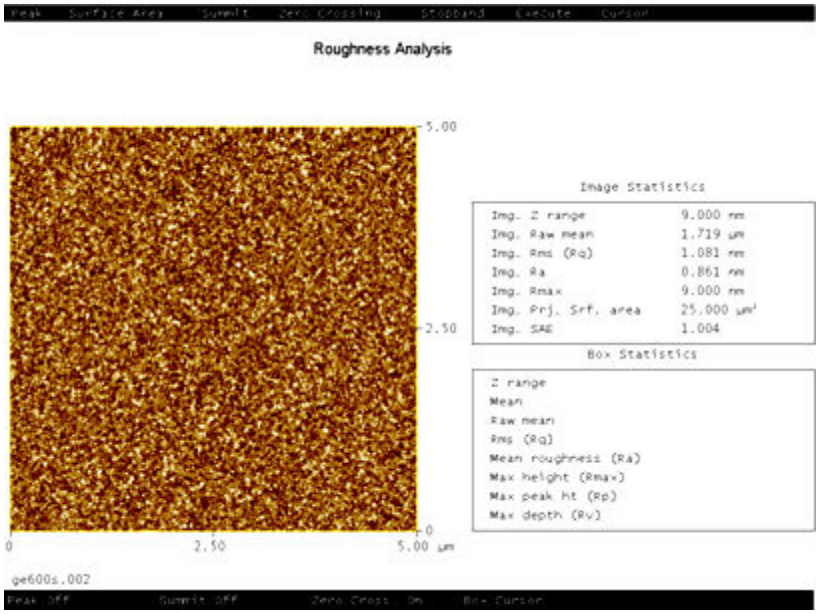


Figure A-4 Atomic force microscope (AFM) image of Ge film deposited at 400°C. The thicknesses of the sample is around 100nm.

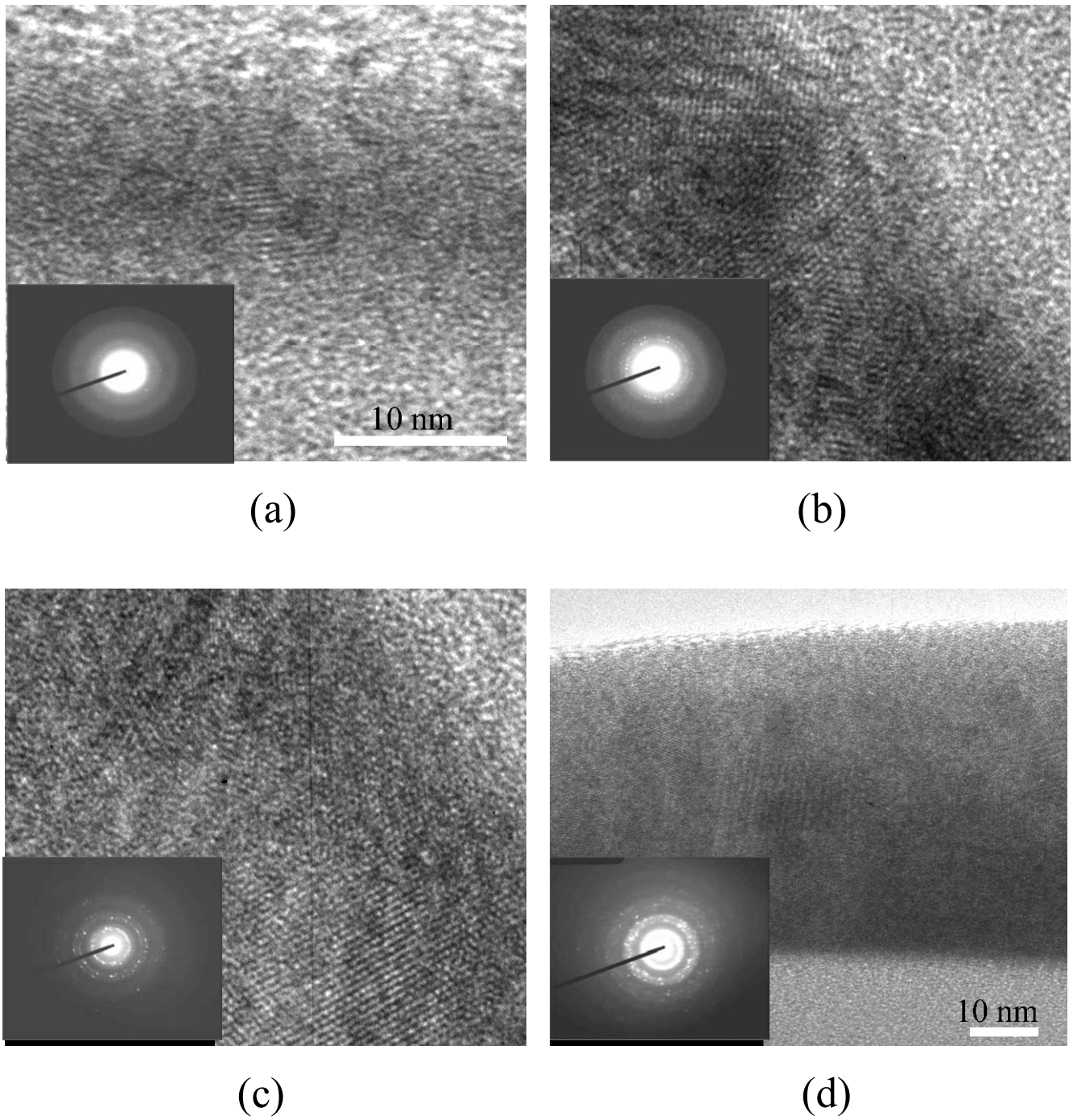


Figure A-5 TEM images and diffraction patterns (insets) of the deposited Ge thin films for (a) 30s, (b) 60s, (c) 180s, and (d) 600s deposition time, respectively.

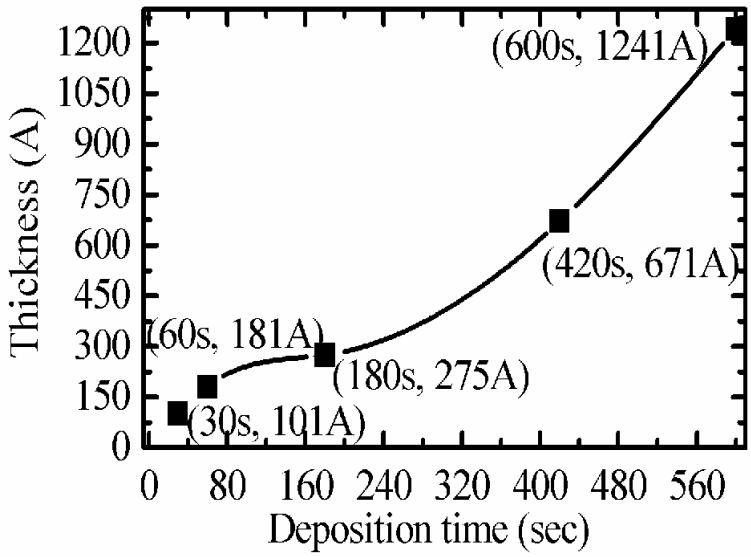


Figure A-6 Ge film thicknesses (by SEM and TEM measurements) plotted as a function of the deposition time at 400°C.

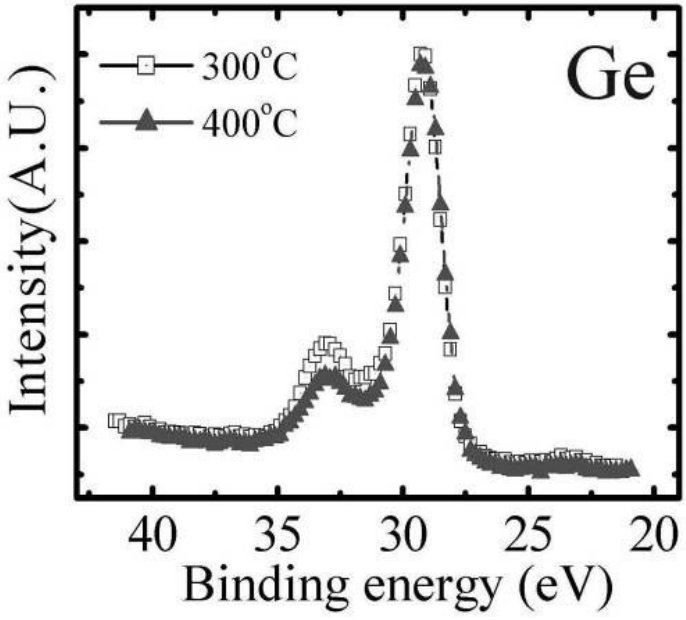


Figure A-7 The spectrum of Ge 3d level by XPS measurement, which revealed the surface conditions of the as-grown Ge films deposited onto SiO_2 substrate at 300 and 400°C.

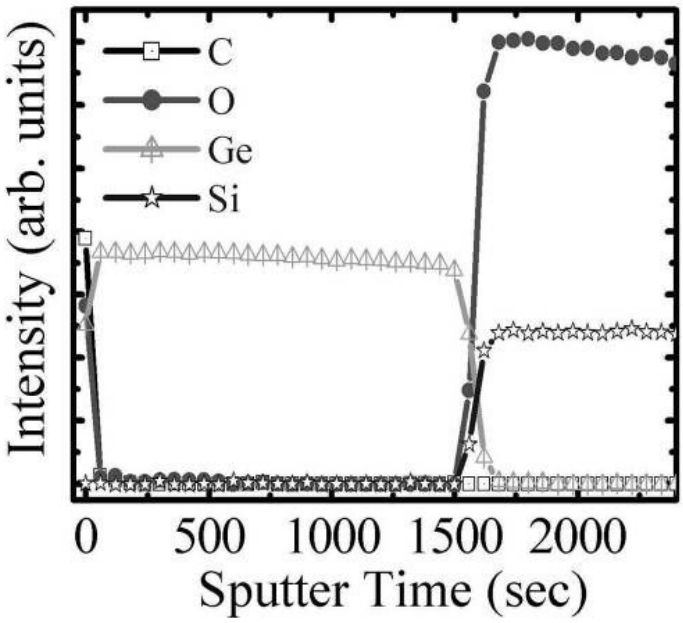


Figure A-8 AES depth profiles of Ge film deposited onto SiO_2 substrate at 300˚C.

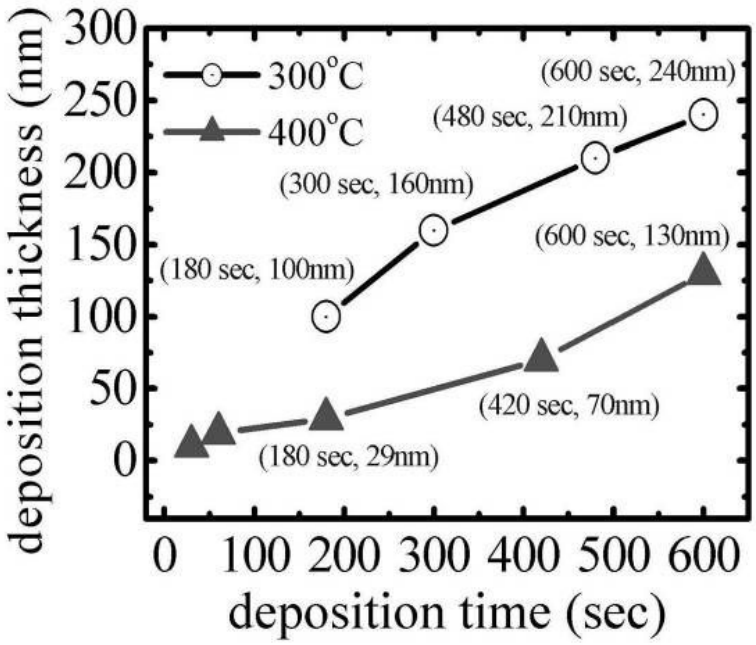


Figure A-9 Ge film thicknesses (by SEM and TEM measurements) plotted as a function of the deposition time at 300 and 400°C.

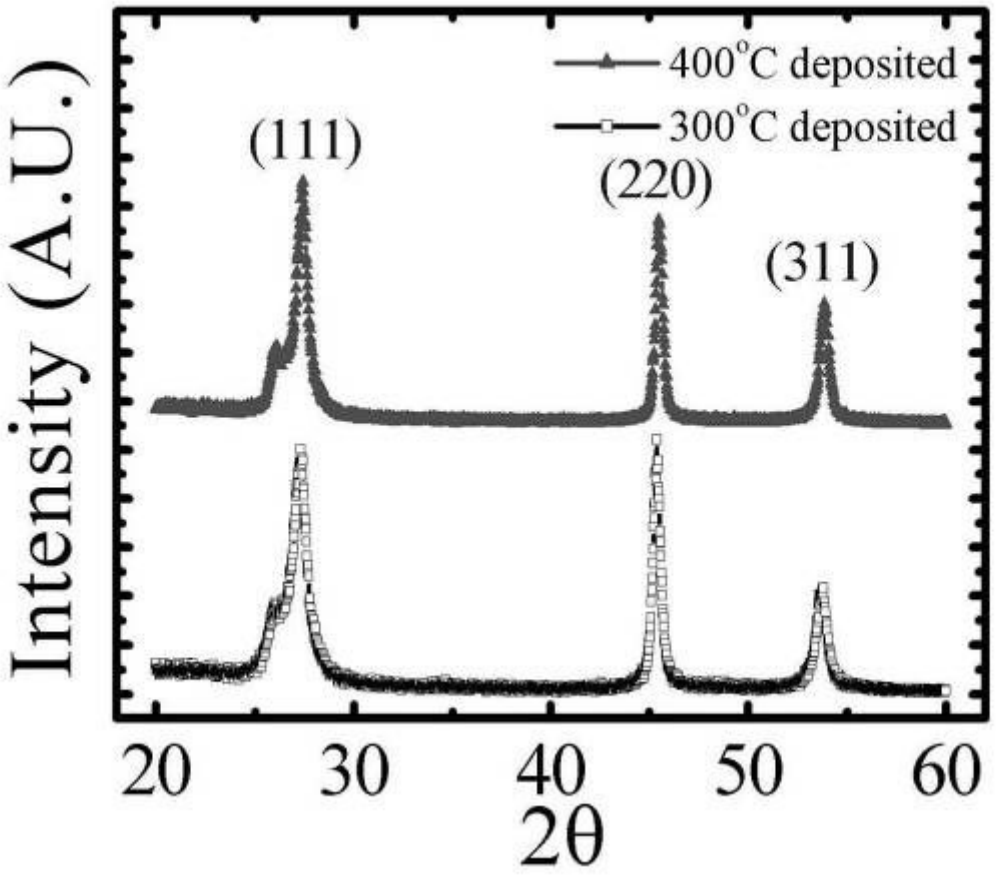
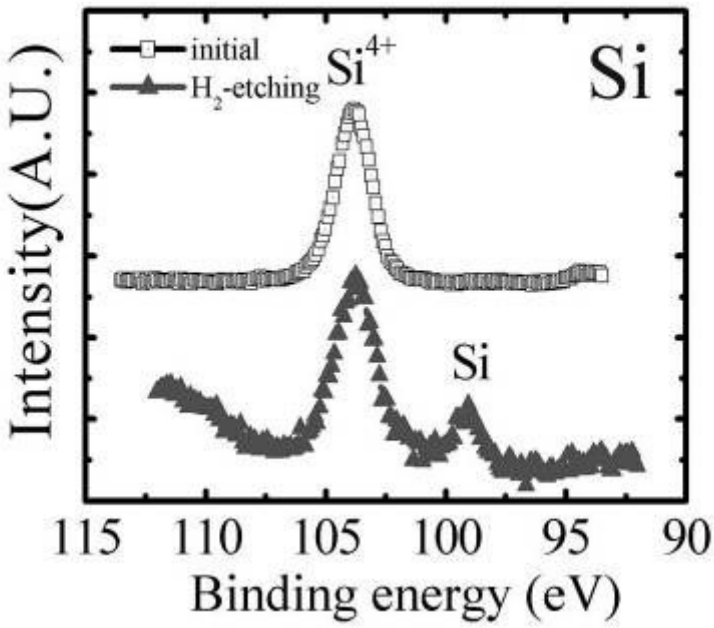
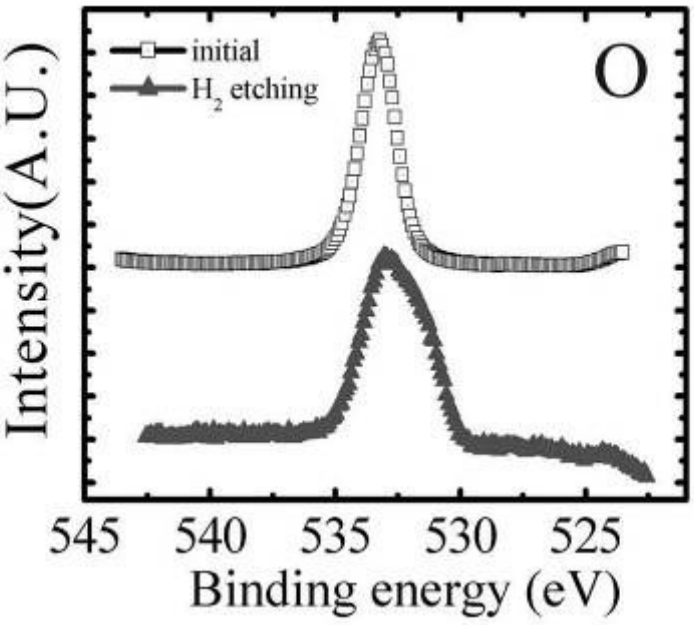


Figure A-10 X-ray diffraction patterns of the as-grown Ge films of about 150nm in thickness, deposited onto SiO_2 substrates at 300 and 400°C.



(a)



(b)

Figure A-11 XPS spectra revealing the status of (a) Si and (b) O atoms of an oxidized wafer before and after etching with H_2 plasma.

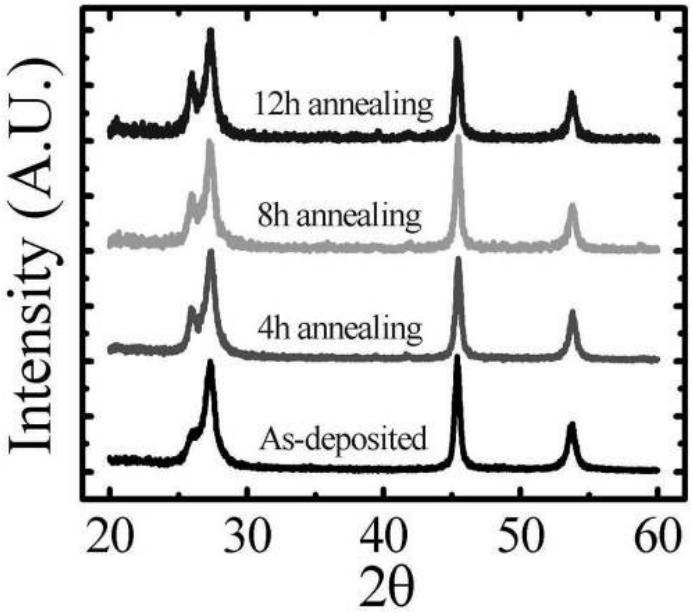


Figure A-12 X-ray diffraction patterns of the as-deposited Ge film without capping SiN_x layer and after re-crystallization in a furnace at 400°C for various duration. The thickness of Ge films is around 160nm.

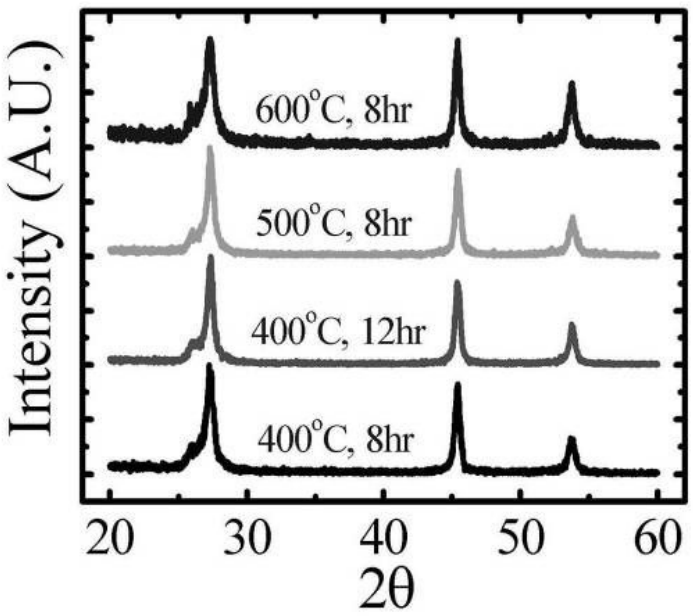


Figure A-13 X-ray diffraction patterns of the as-deposited Ge film capped with a SiN_x layer and after re-crystallization in a furnace for various duration. The thickness of Ge films is around 160nm.

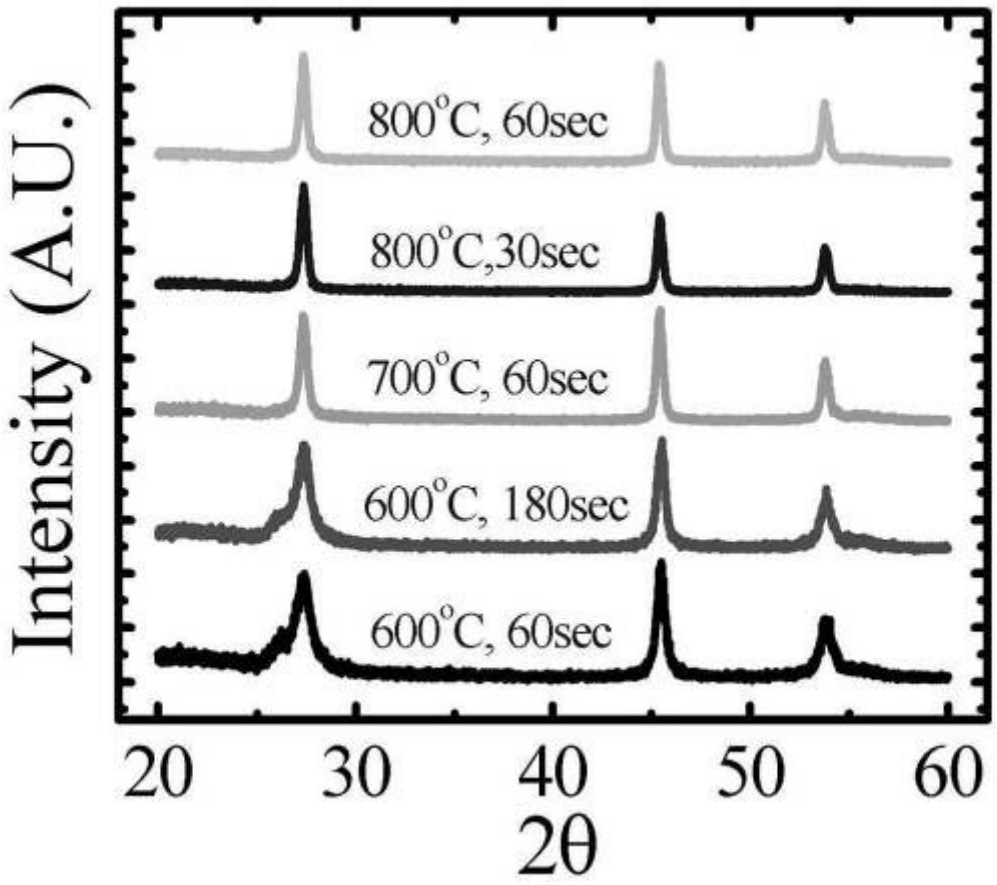
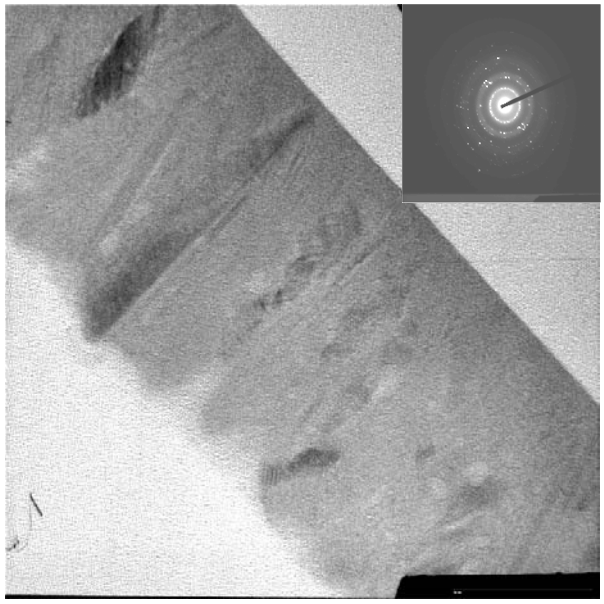
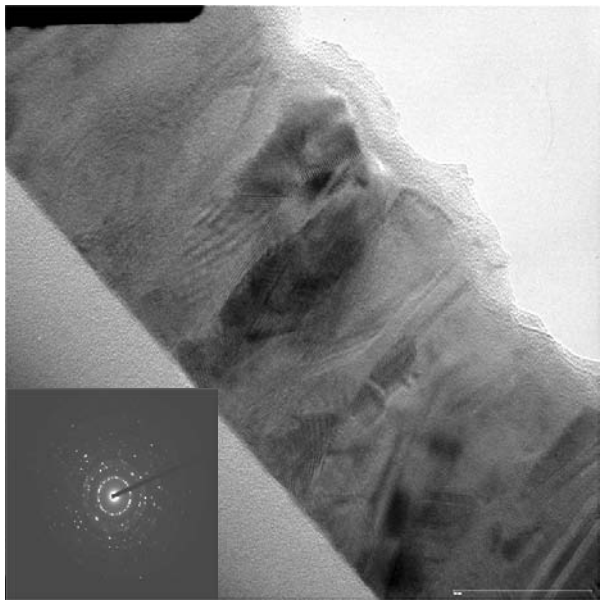


Figure A-14 X-ray diffraction patterns of the as-deposited Ge film capped with a SiN_x layer and after re-crystallization in a RTA system for various duration. The thickness of Ge films is around 160nm.



(a)



(b)

Figure A-15 TEM images and diffraction patterns (insets) of (a) the Ge film deposited at 300^{o}C and (b) the sample after 700^{o}C, 60s, RTA treatment.

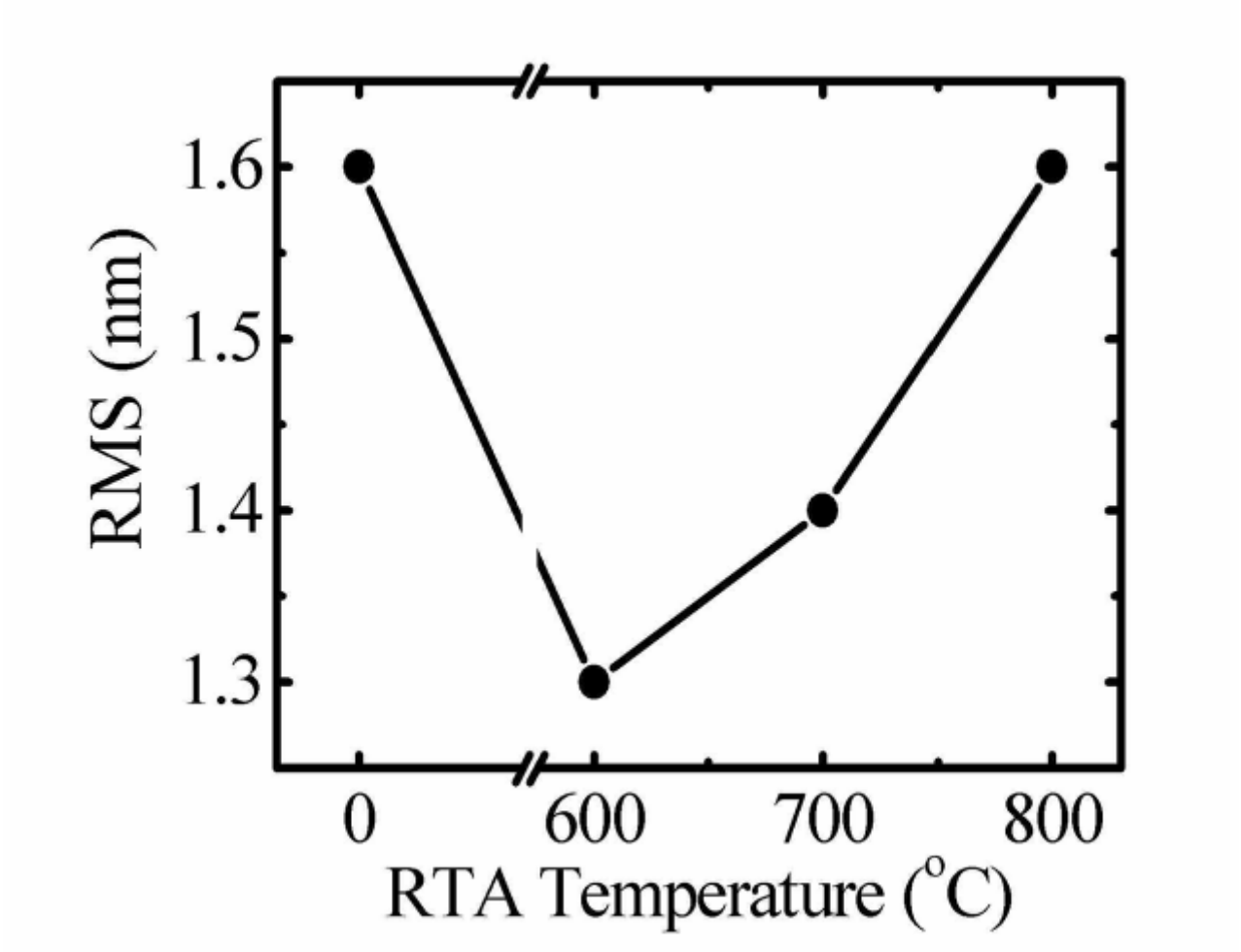


Figure A-16 Surface roughness of re-crystallized Ge films, all with thickness of about 160nm, as a function of RTA temperature. The RTA process time is 60 seconds.

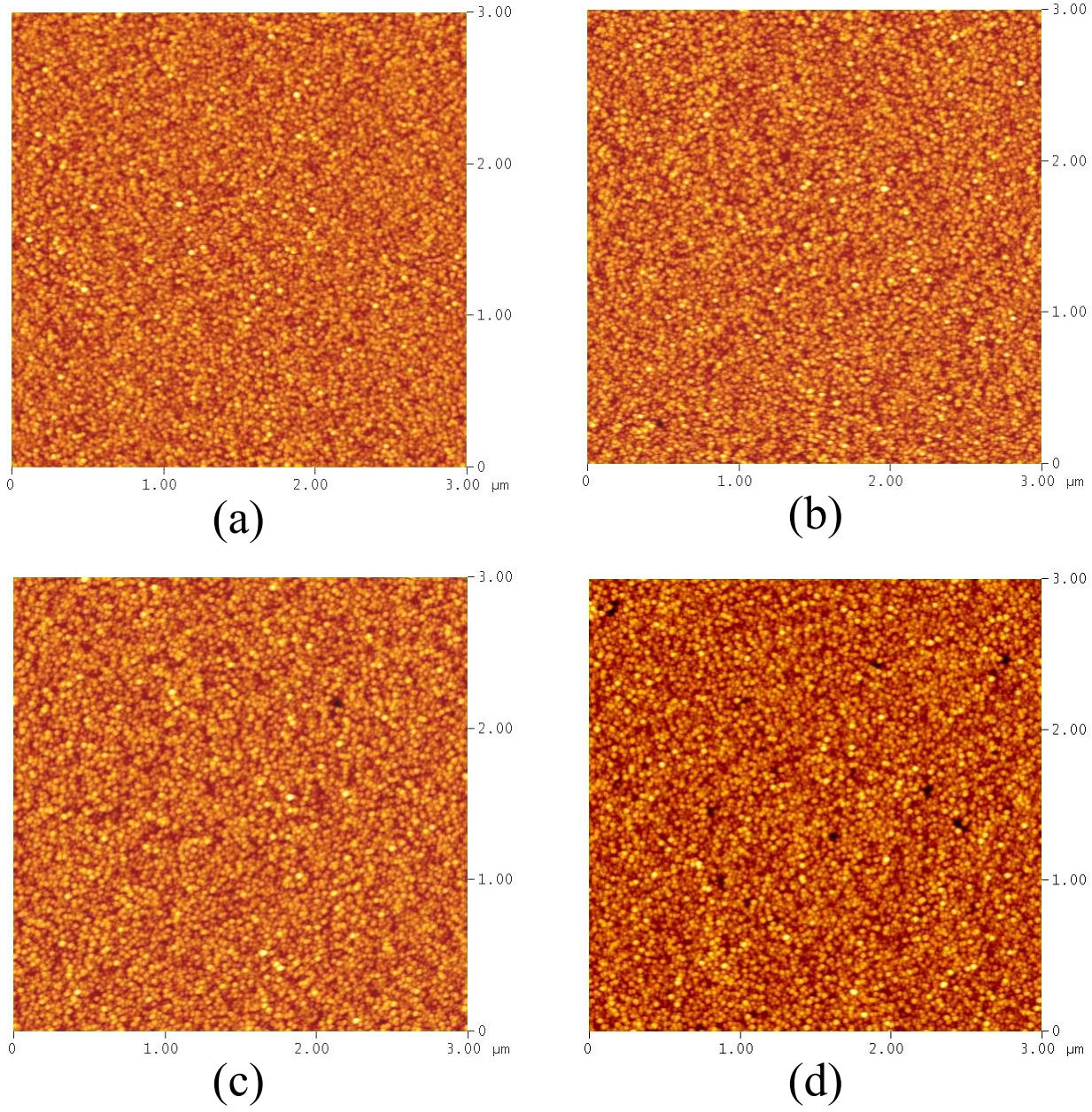
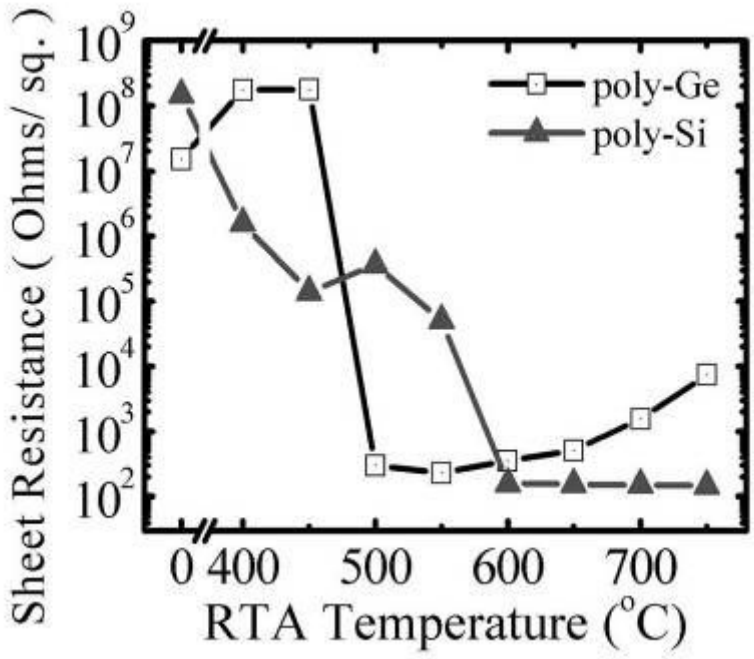
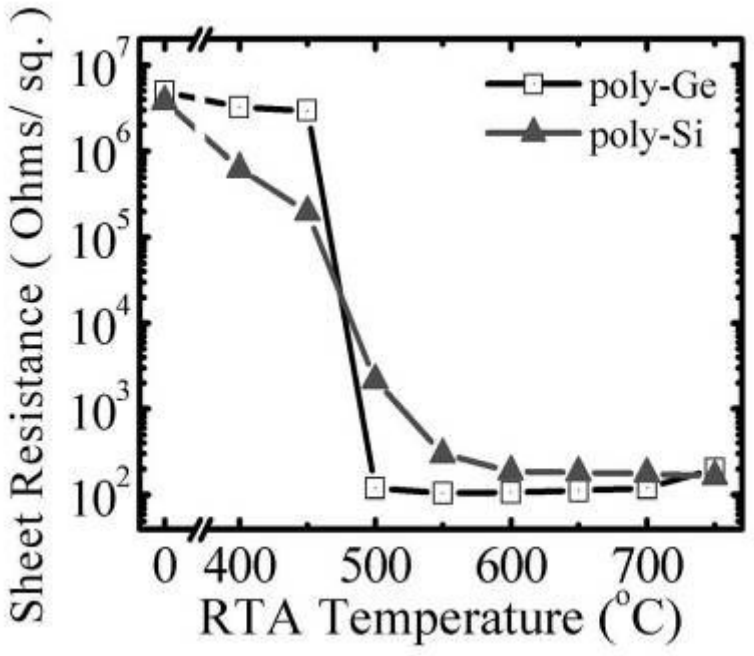


Figure A-17 AFM images of Ge films obtained after RTA treatment: (a) 600 ˚C, 60 s; (b) 700 ˚C, 60 s; (c) 800 ˚C, 30 s; (d) 800 ˚C, 60 s.



(a)



(b)

Figure A-18 Sheet resistance as a function of the RTA temperature for implanted poly-Ge and poly-Si films incorporating (a) phosphorus and (b) boron dopants.

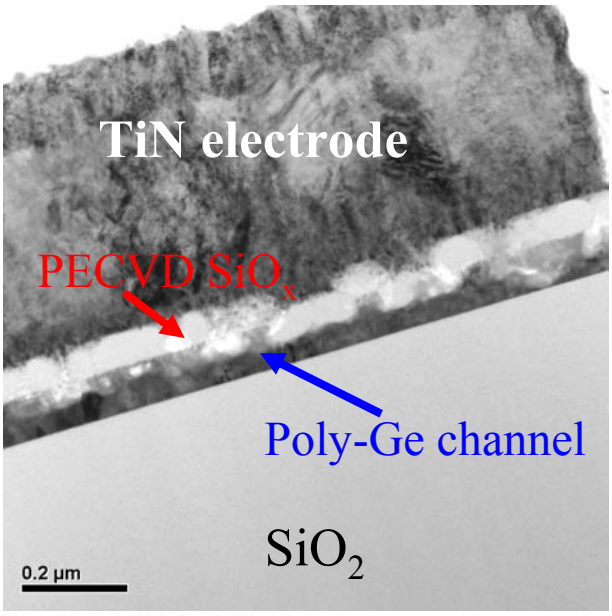


Figure A-19 Cross-sectional TEM images of poly-Ge TFTs. The device structure is TiN electrode/PECVD SiO_2/poly-Ge channel/thick SiO_2 layer/Si Substrate.

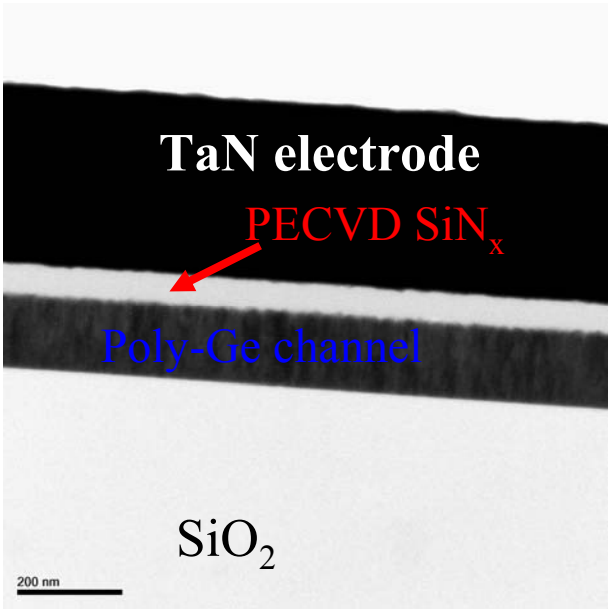


Figure A-20 Cross-sectional TEM images of poly-Ge TFTs. The device structure is TaN electrode/PECVD SiN_x/poly-Ge channel/thick SiO_2 layer/Si Substrate.

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論文題目：先進材料應用於低溫複晶矽薄膜電晶體之研究

A Study of Low-Temperature Polycrystalline Silicon Thin Film Transistors Using Advanced Materials

Publication Lists

A. International Journal:

1. Ching-Chich Leu, Hung-Tao Lin, Chen-Ti Hu, Chao-Hsin Chien, **Ming-Jui Yang**, Ming-Che Yang, and Tiao-Yuan Huang, "Effects of titanium and tantalum adhesion layers on the properties of sol-gel derived $SrBi_2Ta_2O_9$ thin films", ***Journal of Applied Physics***, Vol. 92, No. 3, pp. 1511-1517, Aug. 2002.
2. Ching-Wei Chen, Chao-Hsin Chien, Tsu-Hsiu Preng, **Ming-Jui Yang**, Jann-Shyang Liang, Peer Lehnen, Bing-Yue Tsui and Chun-Yen Chang, "Electrical Characteristics of Thin HfO_2 Gate Dielectrics Prepared Using Different Pre-Deposition Surface Treatments", ***Japanese Journal of Applied Physics***, Vol. 44, No. 1A, pp. 87-93, Jan. 2005.
3. Wen-Tai Lu, Chao-Hsin Chien, Ing-Jye Huang, **Ming-Jui Yang**, Peer Lehnen, and Tiao-Yuan Huang, "Effects of Low-temperature NH_3 Treatment on the Characteristics of HfO_2/SiO_2 Gate Stack", ***Journal of The Electrochemical Society***, Vol. 152, No. 11, pp. G799-G803, Sep. 2005.
4. Wen-Tai Lu, Chao-Hsin Chien, Wen-Ting Lan, Tsung-Chieh Lee, **Ming-Jui Yang**, Shih-Wen Shen, Peer Lehnen and Tiao-Yuan Huang, "Improvements on Electrical Characteristics of p-Channel Metal–Oxide–Semiconductor Field Effect Transistors with HfO_2 Gate Stacks by Post Deposition N_2O Plasma Treatment", ***Japanese Journal of Applied Physics***, Vol. 44, No. 11, pp. 7869-7875, Nov. 2005.
5. **Ming-Jui Yang**, Chao-Hsin Chien, Yi-Hsien Lu, Chih-Yen Shen, and Tiao-Yuan Huang, "Electrical Properties of Low-Temperature-Compatible

P-Channel Polycrystalline-Silicon TFTs Using High-κ Gate Dielectrics", ***IEEE Transactions on Electron Devices***, Vol. 55, No. 4, pp. 1027-1034, April 2008.

6. **Ming-Jui Yang**, Chao-Hsin Chien, Chih-Yen Shen, and Tiao-Yuan Huang, "Properties of Ge Films Grown Through Inductively Coupled Plasma Chemical Vapor Deposition on SiO_2 Substrates", ***Journal of The Electrochemical Society***, Vol. 155, No. 6, pp. H363-H368, April 2008.
7. Ching-Chich Leu, Chen-Han Lin, Chao-Hsin Chien, and **Ming-Jui Yang**, "Effect of HfO_2 buffer layer thickness on the Properties of $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ structure", ***Journal of Materials Research***, Vol. 23, No.7, pp. 2023-2032, July 2008.

B. International Letter:

1. Ching-Chich Leu, Ming-Che Yang, Chen-Ti Hu, Chao-Hsin Chien, **Ming-Jui Yang**, and Tiao-Yuan Huang, "Effects of tantalum adhesion layer on the properties of $SrBi_2Ta_2O_9$ ferroelectric thin films", ***Applied Physical Letters***, Vol. 79, No. 23, pp. 3833-3835, Dec. 2001.
2. **Ming-Jui Yang**, Chao-Hsin Chien, Ching-Chich Leu, Ren-Jian Zhang, Shich-Chuan Wu, Tiao-Yuan Huang and Tseung-Yuen Tseng, "The Effects of Low-Pressure Rapid Thermal Post-Annealing on the Properties of (Ba, Sr)TiO_3 Thin Films Deposited by Liquid Source Misted Chemical Deposition", ***Japanese Journal of Applied Physics***, Vol. 40, No. 12A, pp. L1333-L1335, Dec. 2001.
3. Ching-Chich Leu, Chao-Hsin Chien, **Ming-Jui Yang**, Ming-Che Yang, Tiao-Yuan Huang, Hung-Tao Lin and Chen-Ti Hu, "Effects of ultrathin tantalum seeding layers on sol-gel-derived $SrBi_2Ta_2O_9$ thin films", ***Applied Physical Letters***, Vol. 80, No. 24, pp. 4600-4602, June 2002.
4. Chao-Hsin Chien, Ding-Yeong Wang, **Ming-Jui Yang**, Peer Lehnen,

Ching-Chich Leu, Shiow-Huey Chuang, Tiao-Yuan Huang, and C. Y. Chang, "High-Performance Pt/$SrBi_2Ta_2O_9$/HfO_2/Si Structure for Nondestructive Readout Memory", ***IEEE Electron Device Letters***, Vol. 24, No. 9, pp. 553-555, Sep. 2003.

5. Wen-Tai Lu, Po-Ching Lin, and Tiao-Yuan Huang, Chao-Hsin Chien, **Ming-Jui Yang**, and Ing-Jyi Huang, Peer Lehnen, "The characteristics of hole trapping in HfO_2/SiO_2 gate dielectrics with TiN gate electrode", ***Applied Physical Letters***, Vol. 85, No. 16, pp. 3525-3527, Oct. 2004.
6. Tsu-Hsiu Perng, Chao-Hsin Chien, Ching-Wei Chen, **Ming-Jui Yang**, Peer Lehnen, Chu-Yen Chang, and Tiao-Tuan Huang, "HfO_2 MIS Capacitor with Copper Gate Electrode", ***IEEE Electron Device Letters***, Vol. 25, No. 12, pp. 784-786, Dec. 2004.
7. **Ming-Jui Yang**, Jiann Shieh, Shih-Lu Hsu, Ing-Jye Huang, Ching-Chich Leu, Shih-Wen Shen, Tiao-Tuan Huang, Peer Lehnen, and Chao-Hsin Chien, "Low-Temperature Growth of Polycrystalline Ge Films on SiO_2 Substrate by HDPCVD", ***Electrochemical and Solid-State Letters***, Vol. 8, No. 5, pp. C74-C76, March 2005.
8. Shih-Lu Hsu, Chao-Hsin Chien, **Ming-Jui Yang**, Rui-Hao Huang, Ching-Chich Leu, Shih-Wen Shen, and Tsung-Hsi Yang, "Study of thermal stability of nickel monogermanide on single- and polycrystalline germanium substrates", ***Applied Physical Letters***, Vol. 86, pp. 1-3 (251906), Oct. 2005.
9. Chia-Pin Lin, Bing-Yue Tsui, **Ming-Jui Yang**, Ruei-Hao Huang, and Chao-Hsin Chien, "High-Performance Poly-Silicon TFTs Using HfO_2 Gate Dielectric", ***IEEE Electron Device Letters***, Vol. 27, No. 5, pp. 360-363, May 2006.
10. M. N. Chang, C. Y. Chen, **M. J. Yang**, and C. H. Chien, "Photovoltaic effect

on the conductive atomic force microscopic characterization of thin dielectric films", ***Applied Physical Letters***, Vol. 89, pp. 1-3 (133109), Sep. 2006.

11. Ching-Chich Leu, Chia-Feng Leu, Chao-Hsin Chien, **Ming-Jui Yang**, Rui-Hao Huang, Chen-Han Lin, and Fan-Yi Hsu, "Properties of $Pt/SrBi_2Ta_2O_9/BL/Si$ MFIS Structures Containing HfO_2, SiO_2, and Si_3N_4 Buffer Layers", ***Electrochemical and Solid-State Letters***, Vol. 10, No. 5, pp. G25-G28, Feb. 2007.
12. Sheng-Chih Lai, Hang-Ting Lue, Jong-Yu Hsieh, **Ming-Jui Yang**, Yan-Kai Chiou, Chia-Wei Wu, Tai-Bor Wu, Guang-Li Luo, Chao-Hsin Chien, Erh-Kun Lai, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu, "Study of the Erase Mechanism of MANOS ($Metal/Al_2O_3/SiN/SiO_2/Si$) Device", ***IEEE Electron Device Letters***, Vol. 28, No. 7, pp. 643-645, July 2007.
13. **Ming-Jui Yang**, Chao-Hsin Chien, Yi-Hsien Lu, Guang-Li Luo, Su-Ching Chiu, Chun-Che Lou, and Tiao-Yuan Huang, "High-Performance and Low-Temperature-Compatible P-Channel Polycrystalline-Silicon TFTs Using Hafnium-Silicate Gate Dielectric", ***IEEE Electron Device Letters***, Vol. 28, No. 10, pp. 902-904, Oct. 2007.

C. International Conference

1. C. W. Lin, **M. Z. Yang**, C. C. Yeh, L. J. Cheng, T. Y. Huang, H. C. Cheng, H. C. Lin, T. S. Chao, and C. Y. Change, "Effects of Plasma Treatments, Substrate Types, and Crystallization Methods on Performance and Reliability of Low Temperature Polysilicon TFTs", in ***IEDM Technical Digest***, pp. 305-308, December 5-8, 1999, Washington, D.C., America.
2. **Ming-Jui Yang**, Guang-Li Luo, Tiao-Yuan Huang, and Chao-Hsin Chien, "The characteristics of re-crystallized low-temperature- grown Ge films on SiO_2 substrate", in ***17th International Vacuum Congress and 13th***

International Conference on Surface Science International Conference on Nano Science and Technology, July 2-6, 2007, Stockholm, Sweden.

3. Sheng-Chih Lai, Hang-Ting Lue, Chien-Wei Liao, Yu-Fong Huang, **Ming-Jui Yang**, Yi-Hsien Lue, Tai-Bor Wu, Jung-Yu Hsieh, Szu-Yu Wang, Shih-Ping Hong, Fang-Hao Hsu, Chih-Yen Shen, Guang-Li Luo, Chao-Hsin Chien, Kuang-Yeu Hsieh, Rich Liu and Chih-Yuan Lu, "An Oxide-Buffered BE-MANOS Charge-Trapping Device and the Role of Al_2O_3", in ***the 2008 Non Volatile Semiconductor Memory Workshop (NVSMW 2008)***, May 18th -22nd, 2008, Opio, France.

D. Local Conference

1. Sheng-Chih Lai, Hang-Ting Lue, Jung-Yu Hsieh, **Ming-Jui Yang**, Yan-Kai Chiou, Chia-Wei Wu, Tai-Bor Wu, Guang-Li Luo, Chao-Hsin Chien, Erh-Kun Lai, Kuang-Yeu Hsieh, Rich Liu and Chih-Yuan Lu, "A Study on the Erase and Retention Mechanisms for MONOS, MANOS, and BE-SONOS Non-Volatile Memory Devices", in ***The 2007 International Symposium on VLSI Technology, Systems, and Applications (2007 VLSI-TSA)***, April 23-25, 2007, Hsinchu, Taiwan.
2. Sheng-Chih Lai, Hang-Ting Lue, Chien-Wei Liao, Tai-Bor Wu, **Ming-Jui Yang,** Yi-Hsien Lue, Jung-Yu Hsieh, Szu-Yu Wang, Guang-Li Luo, Chao-Hsin Chien, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu, "Highly Reliable MA BE-SONOS (Metal-Al_2O_3 Bandgap Engineered SONOS) Using a SiO_2 Buffer Layer", in ***The 2008 International Symposium on VLSI Technology, Systems, and Applications (2008 VLSI-TSA)***, April 21-25, 2008, Hsinchu, Taiwan.