射頻金氧半場效電晶體之電性效應與元件模型

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摘要

由於矽射頻金氧半場效電晶體在雜訊以及高頻功率效能上已逐漸被改善，因此目前被廣泛的使用在無線通訊上。但是，在矽射頻積體電路與三五族射頻積體電路的比較之中，其在主動元件中的射頻效能仍然較低，而在被動元件中效能的大量損失和較大的雜訊，都還是矽射頻積體電路技術的主要挑戰，此外，由於射頻積體電路在阻抗匹配、低射頻雜訊以及高功率上的要求，要比數位及類比電路還要嚴苛，因此，另一個矽射頻元件的問題，是牽涉於隨後而來在電性操作造成元件射頻效能退化的真實判斷。然而，矽射頻金氧半場效電晶體的量測是相當複雜，主要是因為所量測的射頻特性有絕大部分來自於基板的寄生效應，解決此寄生效應，將可準確的判斷矽射頻金氧半場效電晶體的特性。

本論文中，我們首先採用一種新奇的微代線電路佈局方式，來得到一個真實的最小雜訊指數量測方式而無需任何的扣除嵌進過程，此種方式有效的解決了基板的寄生效應。基於此電路佈局方式，我們可以直接量測真實的最小雜訊指數，因此可以建立直流電流電壓、散射參數和最小雜訊指數的模型，同時可以預測元件在隨後的電性操作上射頻效能的退化。更進一步的，我們將射頻積體電路整合於高絕緣的塑膠基板上，此種塑膠基板的絕緣方式將有效改善被動元件中大

量的射頻效能損失且有較低的成本。除此之外，由於塑膠基版是可彎曲的，因此可以將伸展的應力應用於其上，此種應力將可以改善矽射頻金氧半場效電晶體的直流及射頻效能，同時我們也利用模擬軟體的方式來驗證之。如此極好效能的射頻電晶體以及元件模型的預測，將非常適合於低雜訊超寬頻的電路應用。

Electrical Stress Effects and Device Modeling of RF MOSFETs

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Abstract

Silicon RF MOSFETs are now widely-used for wireless communications, due to improvements of their RF noise and high frequency gain performance as the technology has evolved. The major technology challenges for Si RF ICs compared with their III-V counterparts are the lower performance of the active RF transistors, and large loss and noise from the passive devices. Furthermore, the RF ICs is especially important for the tight requirements regarding impedance matching, low RF noise and high gain compared with their digital and analog counterparts. Therefore, another key issue involves accurate determination of the RF performance degradation of the Si MOSFETs under continuous operation. Besides, the RF noise is difficult to measure in Si MOSFETs due to the large noise generated from the parasitic substrate loss. To overcome the parasitic effect, the performance of the Si RF MOSFETs can be accurate determinated.

In this thesis, we used a novel microstrip transmission line layout to make accurate measurements of the minimum noise figure (NF_{min}) without any de-embedding. Due to the accurate *as-measured* NF_{min}, a self-consistent DC *I-V*, S-parameters and NF_{min} model was developed and also predicted the RF performance degradation under continuous operation. Moreover, we integrated the Si RF ICs on highly-insulating plastic. This provides lower RF loss than the poorly isolating VLSI-standard Si substrates, and at a lower cost. In the meanwhile, plastic substrates are also flexible and can apply tensile strain. The DC-RF performances for the RF MOSFETs with microstrip line layout were improved by applying tensile strain on plastic and also confirmed by T-Supreme and Medici simulations (TMA). The excellent performance of RF transistors and device model are suitable for low-noise ultra-wide band (UWB) (3.1-10.6 GHz) applications.

ACKNOWLEDGMENTS

I would first like to thank my adviser Prof. Albert Chin for his illuminative suggestions and discussions during the period of my working toward PhD degree. His inspiration benefits me a lot on the creative ideas, effective schedule control and the integrity to the processing tasks.

I appreciate the financial and equipment supports from National Science Council (NSC 94-2215-E-009-062**)**, National Nano Device Lab. and Semiconductor Center of NCTU. I am also grateful to those who ever assisted this work: the crew of ED633 Lab. (especially to, C. C. Liao, C. H. Wu, C. C. Chen, B. F. Hung, C. H. Lai, Z. M. Lai, C. F. Lee, and Y. Y. Tseng).

Finally, much gratitude must be expressed to Dept. of Electronics Eng., NCTU, for the 3-year training, to my dear friends especially S. J. Luo for the encouragement and to my father 高明道, my mother 高汪美美 and my brother 高泉合 who always support me and give me all their love. This work can’t be finished without them.

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Chapter 1

Introduction

1.1 Motivation

Si radio frequency (RF) MOSFETs [1.1.1]-[1.1.12] are widely used for wireless communications, due to the continuous improvements in their RF noise and high frequency gain, associated with the down-scaling of the technology. As the gate length scales into submicron regime, the unit gain cut-off frequency f_T and maximum oscillation frequency f_{max} can be improved up to 100 GHz range and better noise figure. Although Si RF MOSFET technology can give such impressive performance, it still lacks accurate model to predict the RF performance and following electrical operation. This is especially important for RF ICs compared with their digital and analog counterparts due to the tight requirements regarding impedance matching, low RF noise and high gain. Therefore, the primary challenge is develop an accurate model to determinate the RF performance and the degradation of the Si MOSFETs under continuous operation. Besides, Si substrates have a much lower resistivity of 10 Ω-cm [1.1.13]-[1.1.15] and result in large RF substrate loss due to the large parasitic effects. Another important issue is that the large parasitic effect from the high RF loss Si substrates substantially degrades the performance of passive components and affects minimum noise figure (NF_{min}) measurement [1.1.8]-[1.1.12]. The accurate measurement method of RF MOSFETs is important for the device modeling.

The performance of RF passive devices on Si can be improved by integration on high-resistivity Si substrates [1.1.16], using MEMS [1.1.17]-[1.1.19] or ion-implant translated semi-insulating (10^6 Ω-cm) Si technology [1.1.14]-[1.1.15], [1.1.20]-[1.1.23]. This improvement is traded-off by the increased cost of added mask and process steps, or package costs. One solution is to integrate the Si RF ICs on highly-insulating plastic [1.1.24], since high performance RF passive devices can be realized on the low-cost plastic substrate. In the meanwhile, thin-body Si ICs on plastic can be used for Flexible Electronics, RF ID, wireless Displays and System-on-Plastic [1.1.8], [1.1.24]-[1.1.25], since no practical flexible polymer or organic transistors have been demonstrated for the RF regime. However, a challenge for integrating RF ICs on plastic is that high performance transistors are required and need to be transferred from their Si substrates, and mounted on plastic with little performance degradation. Integration with high performance RF passive devices on the plastic substrate demands that the Si substrate of the RF transistors be thinned. Therefore, thinned-down the Si substrate and also keep high performance transistors is one of the issues for the RF ICs on plastic. Additionally, the plastic substrate is flexible and can be apply strain. The strain effect of DC and RF performance for RF MOSFETs is also worthy to study.

1.2 Si RF MOSFETs Technology and Modeling

The silicon-based technology has also been developed for more than 30 years. As the technology continues to scale down and concept of silicon on a chip (SOC) emerges, the Si RF MOSFET becomes possible to be introduced into RF front end design. Multi-fingered layout has been used in RF MOSFET to overcome the gate resistance, because the gate resistance is the most important concern that would influence operation frequency (f_T and f_{max}) and minimum noise figure (NF_{min}) [1.1.8]-[1.1.10]. However, another important problem has been observed in Si RF technology, which is the substrate problem. The important active and passive components such as MOSFET, inductor and transmission line will be severely degraded as the substrate effect has been taken into consideration [1.1.8]-[1.1.15]. The high substrate loss and cross-talk, due to the low resistivity of Si (~10 Ω-cm), have become the main technology challenge to realize high performance Si monolithic millimeter wave integrated circuits (MMICs). Recently, a novel microstip transmission line layout has been proposed in our researches, which can help us to screen out the dominant thermal noise arising from the substrate resistances of the RF probing pads and the CPW line [1.1.10]-[1.1.11]. The excellent isolation can be achieved by this method, which makes the Si RF technology more applicable in the future.

An accurate device model from DC to RF frequency range is necessary to confirm required specification of designed circuit, and to shorten design cycle. The noise performance is a principal requirement for RF circuit design, for example: low noise amplifier (LNA) design. The design of LNA amplifier not only needs precise DC and S-parameters model but even more needs accurate noise model to valuate the noise performance of the circuit. It is needed a physical, scalable MOSFET model in a specific frequency range capable of simulation of DC to RF characteristics in all bias condition. BSIM3 model is a good candidate for DC modeling and it allows users to accurately model upon parameter extraction on existing technology or predict MOSFET behavior based on the default or an extracted technology. However, when BSIM3 model is applied to simulated S-parameter and noise performance of MOSFET at high frequency, it must require some modification for fitting both characteristics of the device. In this thesis, we provided a model to predict device DC I-V, S-parameters, and NF_{min} due to the accurate model can be directly measured using microstrip transmission line layout. The precise RF model is also important for the implementation of MOSFETs and other device in RF front-end circuit.

1.3 Innovation and Contribution

In this thesis, we first developed a novel microstrip line layout that can directly measure the minimum noise figure (NF_{min}) accurately instead of the complicated de-embedding procedure. Very low 0.46 dB NF_{min} and high 16.6 dB associate gain at 10 GHz on 90 nm node MOSFETs with a 65 nm gate length was obtained. This record low NF_{min} is among the best published data [1.3.1]-[1.3.2], [1.1.6]. Based on the accurate NF_{min} measurement, we have developed the self-consistent DC, S-parameters and NF_{min} model to predict device characteristics after the continuous stress with good accuracy. This approach can be used in circuit design as a tool for predicting the RF performance degradation under continuous operation. Furthermore, the RF performance of thin-body (30~40 μm) Si MOSFETs can be improved by applying mechanical strain. The DC-RF performances were enhanced by applying tensile strain and confirmed the strain effect by T-Supreme and Medici simulations (TMA) software. We also report the current $I_{d,sat}$ was 14.3% higher, and f_T increased from 103 to 118 GHz with NF_{min} decreasing from 0.89 to 0.75 dB at 10 GHz of 0.13 μm RF MOSFETs. These improvements are comparable with those for SiN-capped 90 nm strained-Si nMOS and consistent with device simulations. The high performance RF transistors are suitable for low-noise ultra-wide band (UWB) (3.1-10.6 GHz) applications.

Chapter 2

A Novel Microstrip Transmission Line Layout

2.1 Introduction

One difficult challenge for RF MOSFETs is the large parasitic effect from the low resistivity Si substrate - this lowers the RF gain and increases the noise [2.1.1]-[2.1.2]. This becomes worse during RF noise measurements, where the thermal noise from RF probing pads and coplanar waveguide (CPW) transmission lines dominates the *as-measured* minimum noise figure (NF_{min}) rather than the *intrinsic* MOSFET noise. The accurate NF_{min} values over wide frequencies are also important in deriving a self-consistent DC to RF device model needed for IC design. Therefore, de-embedding procedure is required to give the much smaller *intrinsic* NF_{min} [2.1.2]-[2.1.4]. However, the procedures for de-embedding open RF pads and through transmission lines, which occupy additional layout area, are complicated and can produce errors. To overcome these problems, we developed a method to measure the RF noise directly [2.1.5]-[2.1.6]. We used multi-gate-finger structure and microstrip transmission line layout. This helps screen out the dominant thermal noise arising from the substrate resistances of the RF probing pads and the CPW line [2.1.3]-[2.1.4]. With this approach we have been able to measure NF_{min} of intrinsic MOSFET directly and accurately to avoid difficulties with the de-embedding procedures for the RF pads and the “through” CPW lines. The success of this approach is evident from the very low *as-measured* NF_{min} for our RF MOSFETs.

2.2 Microstrip Transmission Line Layout

As mentioned above the RF noise is difficult to measure in Si MOSFETs due to the large noise generated from the parasitic substrate loss [2.2.1]-[.2.3], [2.1.1]-[2.1.4]. Figure 2.2.1(a) shows the layout of conventional CPW and microstrip lines. In the conventional CPW layout, the Electro-Magnetic (EM) waves can penetrate deeply into low resistivity Si substrate (shown in Fig. 2.2.1(b)) to cause the loss and increasing NF_{min}. Figure 2.2.2(a) shows the equivalent circuit model for RF MOSFETs using a conventional CPW transmission line layout, where accurate modeling of the *as-measured* NF_{min} was previously obtained by considering the thermal noise generated from the pad (R_{pad}) and transmission lines (R_{sub}) [2.1.2]. The RF noise from R_{pad} and R_{sub} dominate the *as-measured* NF_{min} rather than from the *intrinsic* noise of a MOSFET. Therefore, de-embedding is required to give the smaller *intrinsic* NF_{min} [2.1.2]. However, the procedures for de-embedding open RF pads and through transmission lines, which occupy additional layout area, are complicated and can produce errors. To overcome these problems we propose a microstrip line layout was shown in Fig. 2.2.1(a) and the equivalent circuit model is shown in Fig. 2.2.2(b). The 3-dimentional schematic view of microstrip transmission line layout was shown in Fig. 2.2.3. The M1 is underneath both RF probing pads and transmission line except device-under-test (DUT), which is connected to RF/DC ground by via. In sharp contrast, the microstrip layout can confine the EM waves within the low loss backend dielectric [2.2.4], as also shown in Fig. 2.2.1(b). Thus, the M1 is used as a shield to prevent EM waves penetrating to high loss and noisy Si substrate. Because the Metal-1 (M1) is used as the ground plane of the microstrip transmission line, above the lossy Si substrate, the R_{pad}- and R_{sub}-generated noise can be screened out, and thus do not contribute to the *as-measured* NF_{min}. This is the strong merit using the new microstrip layout without complicated NF_{min} de-embedding procedure used in conventional CPW layout.

2.3 Device Characteristic of RF MOSFETs

2.3.1 Device Characteristic of 0.18 μm RF MOSFETs

We first measured the DC I_d-V_g and I_d-V_d characteristics. Fig. 2.3.1 shows the I_d-V_g and I_d-V_d characteristic of 16 gate fingers 0.18 μm nMOSFETs with standard CPW layout and microstrip line layout. The almost identical I_d-V_g and I_d-V_d characteristics are shown in Fig. 2.3.1. It indicated that the microstrip line layout could not effect the DC characteristics of RF MOSFETs.

To demonstrate this approach, in Figs. 2.3.2(a) and 2.3.2(b) we show the *as-measured* NF_{min} for the 16 and 32 finger 0.18 μm RF MOSFETs respectively, where both the data from standard CPW and microstrip transmission line layouts are shown for comparison. A large NF_{min} reduction of 0.5 to 2.5 dB was obtained using the microstrip transmission line design, as the frequency was increased from 1 to 18 GHz, even without de-embedding. At 10 GHz, the *as-measured* NF_{min} was reduced to 1.05 dB and 1.12 dB for the 16 and 32 finger 0.18μm MOSFETs, respectively. This *as-measured* low NF_{min} is close to the de-embedded value of standard CPW layout [2.1.2] (also show in Fig. 2.3.2), which indicates that the microstrip transmission line design can successfully shield the thermal noise from the lossy R_{pad} and R_{sub} and yield accurate NF_{min} values. This indicates the good accuracy of directly measured NF_{min} by using microstrip line layout without de-embedding or possible causing errors, which also confirmed the successful shielding EM waves from lossy Si substrate shown in Fig. 2.3.2. This is lowest reported NF_{min} for a 0.18 μm MOSFET and is comparable with the data for 0.13 μm devices (L_g=80nm) [2.1.2]-[2.1.4]. The low NF_{min} of 1.05 dB at 10 GHz is sufficient for UWB (3.1-10.6 GHz) applications.

2.3.2 Device Characteristic of 90nm node RF MOSFETs

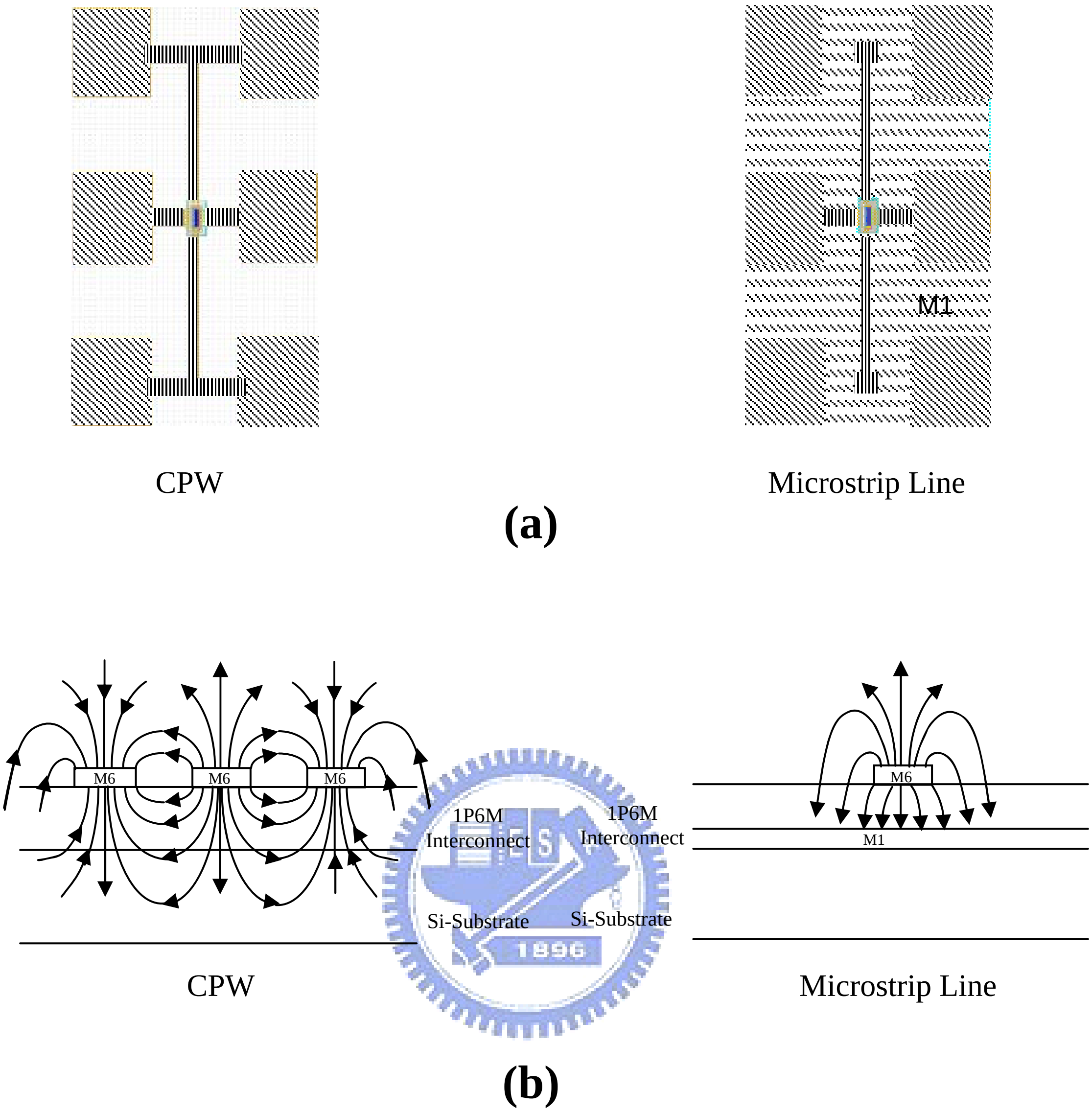
Figure 2.3.3 shows measured I_d-V_g and I_d-V_d for 8 gate-finger 90 nm node RF MOSFET with microstrip transmission line layout structure. For comparison, data for similar devices with standard CPW layout are also displayed. The almost identical I_d-V_g and I_d-V_d characteristics in Fig. 2.3.3, suggest that the grounded shielding has no effect on device DC characteristics.

In Fig. 2.3.4 we show the *as-measured* NF_{min} and associated gain of 8-finger 90 nm node RF MOSFETs. The NF_{min} in the CPW layout is as high as 6.72 dB at 18 GHz. In contrast, a low NF_{min} of only 0.83 dB is measured directly at 18 GHz using the microstrip line layout. Although the NF_{min} in the CPW case is lowered after de-embedding, the measured *intrinsic* NF_{min} from the microstrip line layout shows that it only contributes a small (-5.89 dB or 26%) fraction of the total noise. This indicates that it is hard to de-embed the *intrinsic* NF_{min} in the CPW case accurately. The large *as-measured* NF_{min} in the CPW layout arises mainly from thermal noise generated by the parasitic resistances of the probing pad and transmission line [2.1.2].

This is shielded by the ground plane in the microstrip layout. The substrate shielding also gives much higher gain of 11.2 dB (13.2 times) at 18 GHz than for the CPW case. A record low 0.46 dB NF_{min} at 10 GHz was achieved with a high 16.6 dB gain [2.3.1]-[2.3.3]. This confirms the merit of microstrip line layout in shielding the substrate-noise. This record low NF_{min} is among the best published data [2.3.1]-[2.3.3]. The low noise and high gain to 18 GHz are important for RF ICs at higher frequency bands.

2.4 Conclusions

The novel microstrip transmission line layout was developed. The measurement DC characteristics were identical with standard CPW layout and the measured NF_{min} was accurately without the need for complicated de-embedding. The microstrip transmission line layout can help us to develop the RF active device model accurately.



CPW Microstrip Line

(a)

CPW Microstrip Line

(b)

Fig. 2.2.1 (a) Layout for conventional CPW and novel microstrip lines of low noise 0.18 μm MOSFETs. For the microstrip line design, M1 and M6 are used to form the transmission line and the R_{pad}- and R_{sub}-generated noises are screened by M1. (b) Cross-sectional view of different CPW and novel microstrip lines.

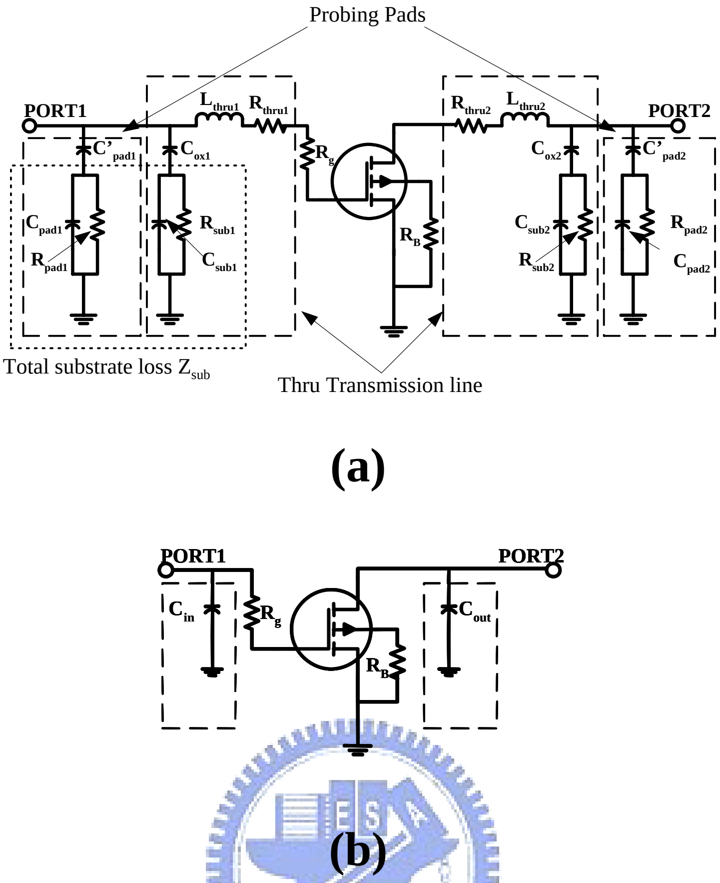


Fig. 2.2.2 Equivalent circuit model for RF MOSFETs using (a) CPW transmission lines and (b) microstrip transmission lines layout.

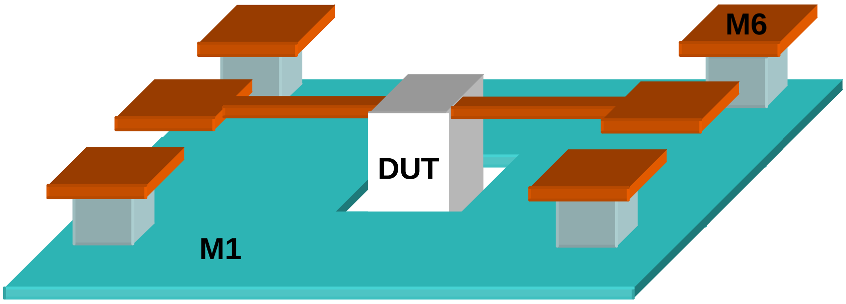
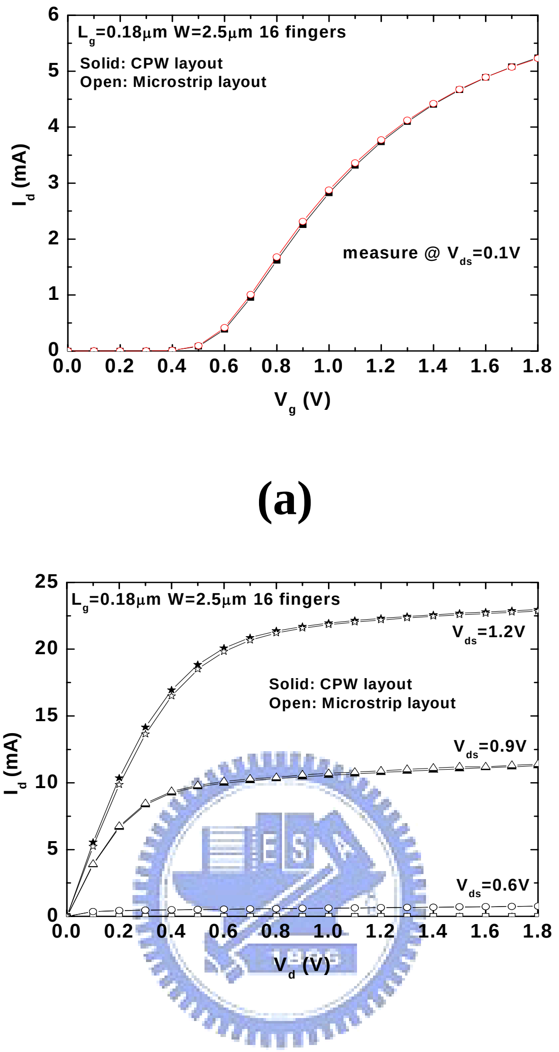


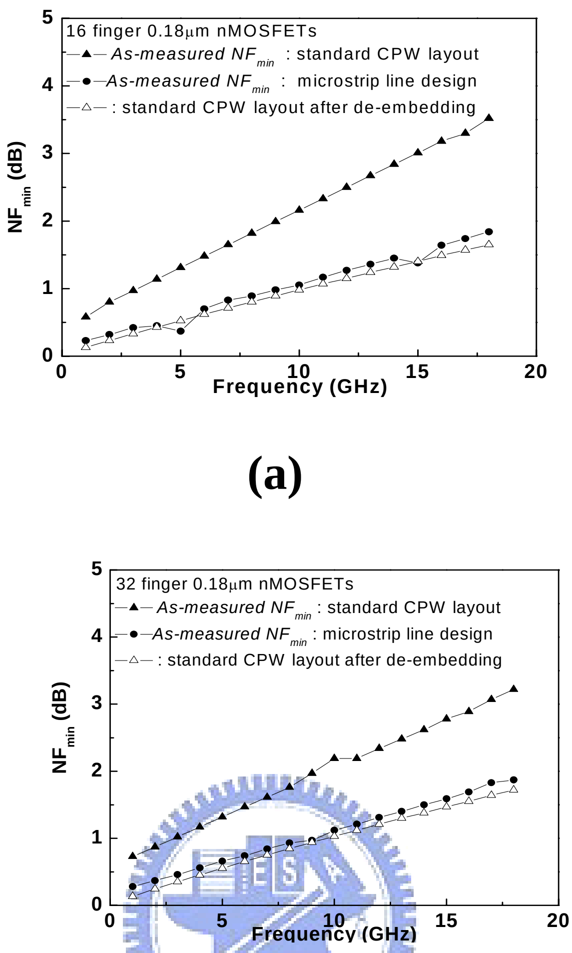
Fig. 2.2.3 Three-dimensional schematic view of microstrip transmission line layout used for low noise 90 nm MOSFETs. The M1 is connected to ground pad by via.



(a)

(b)

Fig. 2.3.1 Measured (a) I_d-V_g (b) I_d-V_d curves of 16 finger 0.18 μm RF MOSFETs with CPW line layout and with microstrip transmission line layout.



(a)

(b)

Fig. 2.3.2 Comparison of the *as-measured* NF_{min} data of a standard CPW layout and a microstrip transmission line design for (a) 16- and (b) 32-finger 0.18 μm RF MOSFETs.

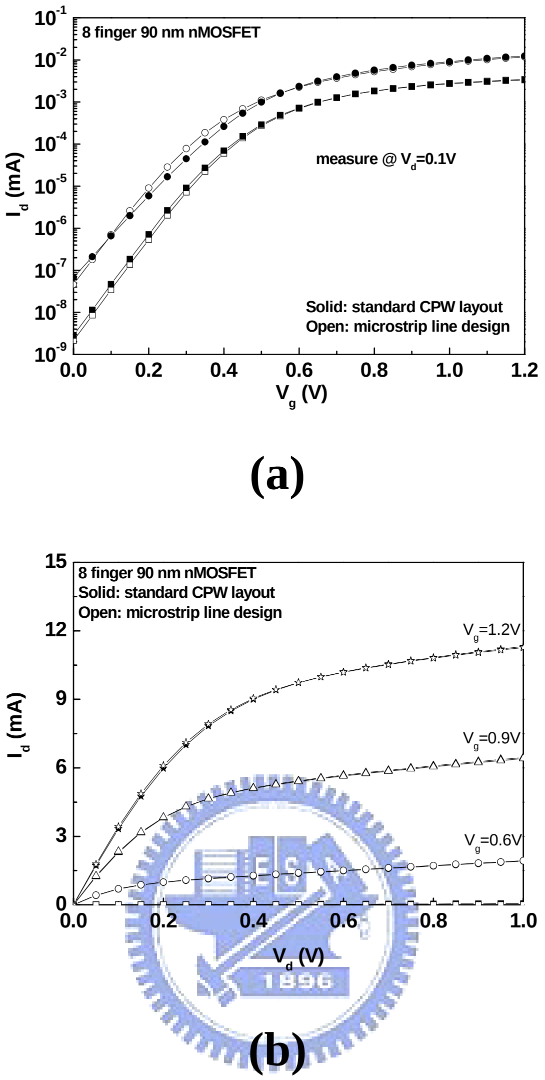


Fig. 2.3.3 Measured (a) I_d-V_g (b) I_d-V_d curves of 90 nm node MOSFETs (L_G=65 nm) with CPW line layout and with microstrip transmission line layout.

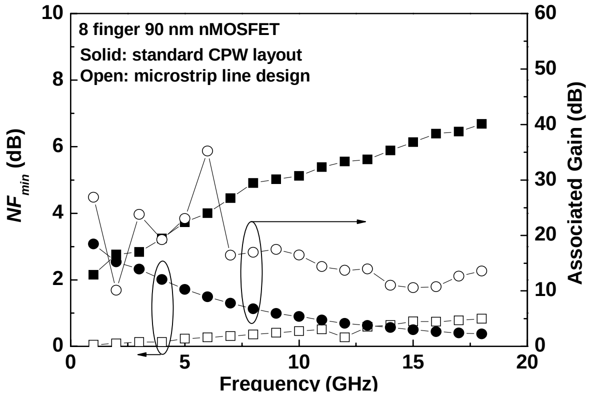


Fig. 2.3.4 Measured NF_{min} and Associated Gain versus frequency of 8-gate-finger 90 nm node MOSFETS with CPW line layout and with microstrip transmission line layout.

Chapter 3

Electrical Stress Effects and Device Modeling

3.1 Introduction

As silicon technology has evolved, the device performance has improved to the point where Si RF MOSFETs [3.1.1]-[3.1.9] are now widely used in wireless communication ICs. RF transistors, compared with their digital and low frequency analog counterparts, require more accurate device models and supporting measurements. This arises from the tight specifications for impedance matching, low RF noise and high gain. As IC operation frequencies increase so too does the minimum noise figure (NF_{min}), and the RF gain also degrades. The higher operational frequencies are required in emerging Ultra-Wide Band (UWB) (3.1-10.6 GHz) wireless communication technology beyond the Wireless-LAN. Thus a sound understanding of the RF performance degradation of MOSFETs is desirable [3.1.10]-[3.1.12].

To accurately model the stress effect on NF_{min}, we used microstrip line layout which is reported in chapter 2 can directly measure the NF_{min} with good accuracy. For the 0.18 μm MOSFETs, very low *as-measured* NF_{min} of 1.05 dB is measured at 10 GHz in 16 gate fingers without any de-embedding. Such low NF_{min} is comparable with de-embedded 0.13 μm node MOSFETs (80 nm gate length) [3.1.6]-[3.1.7]. The devices were further stressed to give a ~20% reduction in current drive, which is equivalent to 12.5 years continuous operation at 1.8 V or 1.9 V overdrive with 2.7 years lifetime. Significant RF performance degradation was measured: at 10 GHz the NF_{min} increases by 0.4-0.5 dB and $|H_{21}|^2$ and G_{max} reduce by 2.1-2.2 dB.

Using the derived analytical equation of NF_{min} and self-consistent DC I-V, S-parameters and NF_{min} model [3.1.8]-[3.1.9], we have successfully simulated the performance degradation of MOSFETs after stress for the 0.18 μm RF MOSFETs. This approach can be used in circuit design as a tool for predicting the RF performance before and during continuous operation.

3.2 Experiment Procedure

In this study we have used 8, 16 and 32 fingers 0.18 μm node nMOSFETs to reduce the gate-resistance generated RF noise [3.1.5]-[3.1.6]. To help in the measurement and modeling of the RF noise we used a novel microstrip transmission line layout, as describe in chapter 2. This permits accurate measurement of the degradation of the noise with electrical stress. The fabricated devices were first characterized by DC I-V, S-parameters and NF_{min} measurements using an HP4155C, HP8510C network analyzer and ATN-NP5B noise parameter system, respectively. The 0.18 μm RF MOSFETs were then stressed electrically at V_{ds}=3V and V_{gs}=1/2V_{ds}=1.5V for 5,000 sec. A self-consistent DC to RF model was developed which had a BSIM core and had parasitic RC elements to the gate, drain and body - to simulate the device characteristics before and after stress.

3.3 Device Characteristic of 0.18 μm RF MOSFETs before and after stress

The DC characteristics (I_d -V_d and I_d -V_g) for 16 and 32 finger 0.18 μm RF MOSFETs are compared in Figs. 3.3.1(a) and 1(b), before and after hot-carrier stress. The I_d degrades monotonically with increasing stress time as does the threshold voltage (V_t) and sub-threshold slope (SS). The saturation drain current ($I_{d,sat}$) decreases with stress time to a 20% degradation. The I_d degradation is also evident in the I_d-V_g curves, where additional threshold voltage (V_t) and sub-threshold slope (SS) degradations occur with stress. After hot-carrier stress V_t increases from 0.475 to 0.675 V and the SS shifts from 85 to 110 mV/decade. These degradations are due to electron trapping and oxide-Si interface state generation on the drain side of the devices, which result in the higher V_t and lower electron mobility in the channel, respectively [3.3.1]-[3.3.3]. In addition, the output resistance r_o ($=1/\partial I_d/\partial V_{ds}$), shown in Fig. 3.3.1(c), also decreases after stress that is important for the RF gain and matching in a circuit. A similar degradation of the DC characteristics occurred for the 32-gate-finger devices.

Figure 3.3.2(a) illustrates the time dependence of the $\Delta I_{d,sat}/I_{d,sat}$ degradation for 0.18 μm RF MOSFETs, under the worst hot-carrier stress conditions of V_{gs}=1/2V_{ds}=1.5V. The $I_{d,sat}$ degrades monotonically with increasing stress time, which is typical for hot-carrier stress. Figure 3.3.2(b) displays the lifetime for a 20 % $I_{d,sat}$ reduction in the devices, under different stress voltage conditions. The extrapolated lifetime follows an exponential dependence on $1/V_d$ [3.3.2], and thus our stress conditions mimic continuous operation at 1.8V for 12.5 years, or at 1.9V overdrive for 2.7 years. Fig. 3.3.2(c) shows the channel length modulation coefficient λ as a function of stress time. This was obtained from the r_o and I_d using $\lambda=1/r_oI_d$. The linear variation of λ with the stress time is important for modeling the I_d-V_d after stress.

Figures 3.3.3(a) and (b) show the measured S-parameters of the 16 and 32 finger 0.18 μm RF MOSFETs, respectively, for both fresh and stressed devices. The hot-carrier stress has little effect on S_{11} and S_{12} which is due to the unchanged input capacitance (C_{gs}) and only slightly altered feedback capacitance (C_{gd}) after stress. In contrast significant change occurred for S_{21} and S_{22} for both multi-fingered devices. The degraded S_{21} after stress is due to the reduced forward gain and is related to the lower trans-conductance (g_m). The degraded S_{22}, as shown in the horizontal left shift in the Smith chart, comes from a decrease of r_o as shown in the DC I_d-V_d characteristics of Fig. 3.3.1(b). This will result in poor output impedance matching in a circuit.

The effects of stress on the frequency dependence of the RF current gain $|H_{21}|^2$ and the G_{max} at maximum stable gain (MSG) region, for a 16 finger device, are shown in Fig. 3.3.4(a). The $|H_{21}|^2$ follows the typical -20 dB/decade slope and G_{max} at MSG follows a -10 dB/decade slope [3.3.4]. The G_{max} is used here since the unilateral gain (U) gives unrealistic higher gain than G_{max} [3.3.4]. The stress lowers the cut-off frequency (f_t) from 48.3 to 38.7 GHz. This amounts to a 19.8% degradation of f_t, similar to the DC drive current reduction. Figure 3.3.4(b) displays the f_t-V_g and g_m-V_g dependences for the 16 finger 0.18 μm RF MOSFETs, before and after stress. Note that the f_t curve follows the g_m curve with respect to V_g, and the stress not only lowers the f_t and g_m but also shifts both curves by the amount of ΔV_t. Although in an RF circuit it is desirable to use a low V_g bias to reduce the DC power dissipation, the shift of the f_t curve after stress should be considered and the MOSFETs should rather be biased in the saturation region with a larger V_t. For 0.18 μm RF MOSFETs, a higher V_g bias of 1.2V is suggested, rather than 1.0V, when one considers the stress effects.

Figures 3.3.5(a) and (b) show the measured NF_{min} of the 16 and 32 finger devices employing the microstrip transmission line design. At 10 GHz, the NF_{min} was 1.05 dB and 1.12 dB for the 16 and 32 finger devices, respectively. The NF_{min} after hot-carrier stress increased over the whole measured frequency range. At 10 GHz NF_{min} increased from 1.05 to 1.37 dB for the 16 finger devices and from 1.12 to 1.46 dB for 32 finger devices. Such NF_{min} increase should also be considered in RF circuit design.

3.4 Device Calibration of 0.18 μm RF MOSFETs before and after stress

Since the hot-carrier stress has significant effects on both DC and RF performance, accurate modeling of the device performance after stress is needed. We first established the device model for unstressed devices. The circuit model is shown in chapter 2 (Fig. 2.2.2(b)), where a BSIM core (Level 3.2) is used with only added parasitic gate resistance (R_g), substrate resistance (R_b), input (C_{in}) and output (C_{out}) shunt capacitances. Note that the BSIM model can simulate the DC characteristics of CMOS devices well, but it is still challenging to model the RF performance especially the NF_{min}. This is because of the large parasitic effects from high RF loss Si substrate. Although using open pad and through transmission line layout followed by complicated de-embedding procedure can develop the self-consistent transistor model of DC, S-parameters and NF_{min} [3.1.5], it is highly desirable to develop a simple method to directly measure the RF performance such as NF_{min} without additional layout and de-embedding. This device model shown in Fig. 2.2.2(b) is simpler than the one used for the CPW case shown in Fig. 2.2.2(a), since the substrate RF loss from the pads and transmission lines are successfully shielded.

The simulated DC I_d-V_g, I_d-V_d and r_o-V_d curves are included in Figs. 3.3.1(a), (b) and (c), respectively. The modeled RF S-parameters, $|H_{21}|^2$, G_{max} and f_t-V_g are shown in Figs. 3.3.3 and 3.3.4, respectively. Good agreement between the measured and modeled DC I-V, RF S-parameters, $|H_{21}|^2$, G_{max} and f_t were all obtained self-consistently using the simple equivalent circuit model incorporating the microstrip line design.

To get an accurate model for NF_{min}, we have used an analytical equation previously derived from the equivalent noise circuit of MOSFETs [3.1.5], [3.1.8]:

$$NF_{min} = 1+2\gamma(1+ \mathrm{g_m} R_g/\gamma)^{1/2} f/f_t \qquad (1)$$

Here γ is the drain current noise correlation factor, which has an ideal value of 2/3 [3.4.1]-[3.4.2]. Close agreement between measured and simulated NF_{min} is shown in Fig. 3.3.5, in addition to the good agreement for the DC I-V, S-parameters, and RF gain, as shown above. The device parameters for the NF_{min} simulation, for both unstressed devices, are summarized in Table 1, where the γ values used in the simulation were 0.67 and 0.7 for the 16 and 32 finger devices respectively. These values are close to the ideal value of 2/3.

After achieving good agreement for the DC and RF characteristics of fresh 0.18μm MOSFETs we have simulated the device characteristics after stress. Using the criteria of 20% $I_{d,sat}$ degradation, as shown in Fig. 3.3.2 after continuous operation, we first obtained good agreement of the simulated DC I_d-V_d, I_d-V_g and r_o-V_d with measurements shown in Fig. 3.3.1. Without changing the values of the parasitic R_g, R_b,

C_{in} and C_{out} in the equivalent circuit model, good agreement was obtained between the simulated RF S-parameters, $|H_{21}|^2$, G_{max} and NF_{min} and the measured data (see Figs. 3.3.3, 3.3.4 and 3.3.5). The drain current noise correlation factor γ was kept constant before or after hot-carrier stress for the same multi-finger devices. The $g_m\mathrm{R_g}$ term in eq. (1) plays only a minor role for NF_{min}, since by using parallel fingers, the $\mathrm{R_g}$ and $g_m\mathrm{R_g}/\gamma$ are reduced. Therefore, the NF_{min} degradation appears to be dominated by the cut-off frequency f_t.

3.5 Scaling Trend of Device Characteristic

3.5.1 Finger numbers dependence

The dependence on the number of gate fingers for 90 nm node RF MOSFETs is shown for NF_{min} and the associated gain at 10 GHz, in Fig. 3.5.1. This small 8 finger device can also largely reduce the DC power consumption than previous large fingered MOSFET [3.1.4]-[3.1.5]. The NF_{min} independence on number of gate-fingers can be explained by the g_m*R_g and f_T in eq. (1) which are weakly dependent on the number of fingers (Fig. 3.5.2). Good agreement between the measured and modeled g_m, R_g, f_T and f_{max} were obtained using the self-consistent equivalent circuit model.

3.5.2 Length dependence

The dependence of g_m, R_g, f_T, f_{max} and NF_{min} on the down-scaled L_G [3.1.5] is shown by the following equations.

$$I_{ds} = \frac{\mu_{eff} C_{ox} (W/L_G)\left[(V_g - V_t)V_{ds} - (m/2)V_{ds}{}^2\right]}{1 + (\mu_{eff} V_{ds} / v_{sat} L_G)} \tag{2}$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{3}$$

$$R_g = R_s \frac{W}{L} \propto \frac{1}{L_G} \tag{4}$$

$$f_T \sim \frac{g_m}{(C_{gs} + C_{gd})} \propto g_m \tag{5}$$

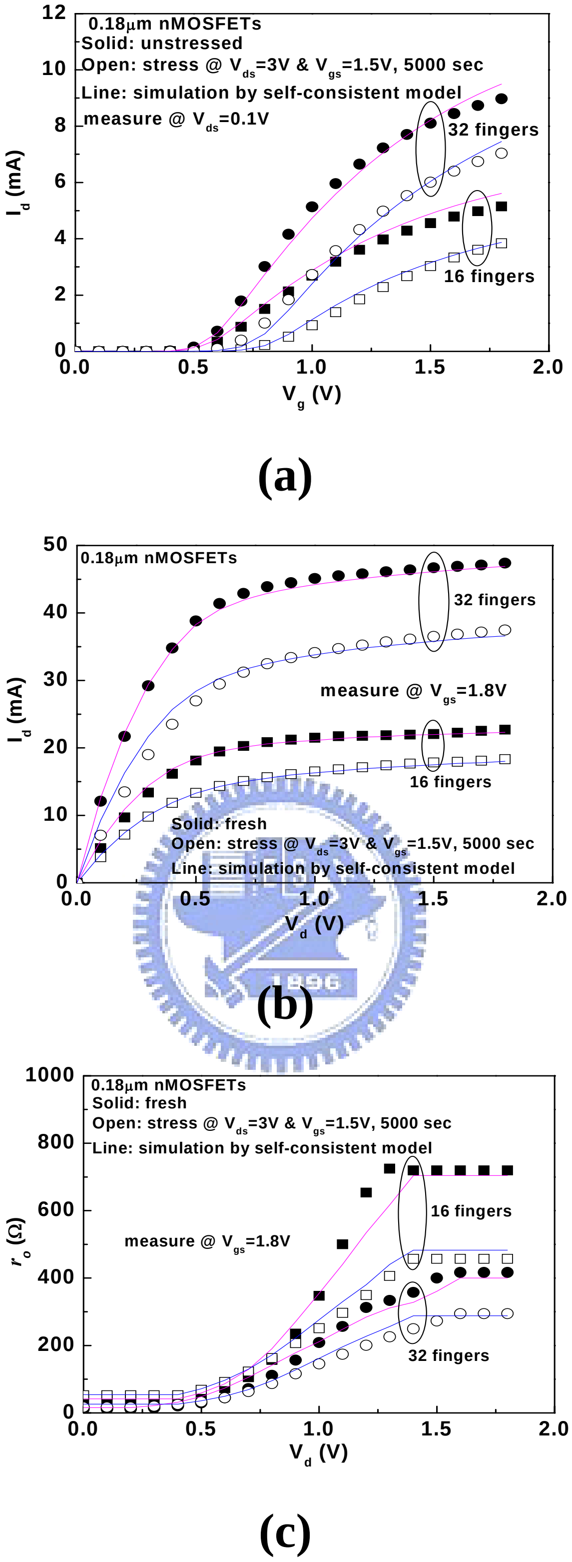
$$f_{max} = \frac{1}{2} f_T \sqrt{\frac{R_{ds}}{R_g + R_i}} \propto \frac{g_m}{\sqrt{L_G}} \tag{6}$$

$$NF_{min} = 10log(1 + 2\gamma\sqrt{1 + g_m R_g / \gamma}\,\frac{f}{f_T}) \propto log(1 + C_1\sqrt{1 + \frac{C_2}{L_G}}) \tag{7}$$

Owing to the good agreement between the measured and modeled data, we can predict the RF characteristic beyond 65nm MOSFETs. Figs. 3.5.3-3.5.4 show the down-scaling trend of the measured and modeled RF characteristics from L_G of 0.18 μm-90 nm [3.1.5]-[3.1.9], and 65 nm MOSFETs to 15 nm gate-length devices. Because the difficult technology barrier to scale down the gate dielectric and C_{gs} even using high-κ dielectric [3.5.1], the g_m can no longer be improved continuously. In addition, the f_T also degrades slightly due to the unavoidable increasing reverse feedback C_{gd} in highly scaled MOSFET. The combined degradation of f_T and R_g largely limits the further improvement of f_{max} and NF_{min} as $L_G < 45$ nm. Further improving the RF performance for $L_G < 45$ nm can only be achieved by using strained Si or III-V MOSFETs proposed recently.

3.6 Conclusion

We have successfully developed a model to predict device DC I-V, S-parameters, and NF_{min} by using a microstrip transmission line layout design. Close agreement was obtained for the accurate NF_{min} measurements and the analytical NF_{min} simulation. This approach is important as a tool in predicting the RF performance degradation of MOSFETs in a circuit where the devices are under continuous bias operation and the NF_{min} scaling trend, beyond 65 nm devices to 15 nm, has been predicted.

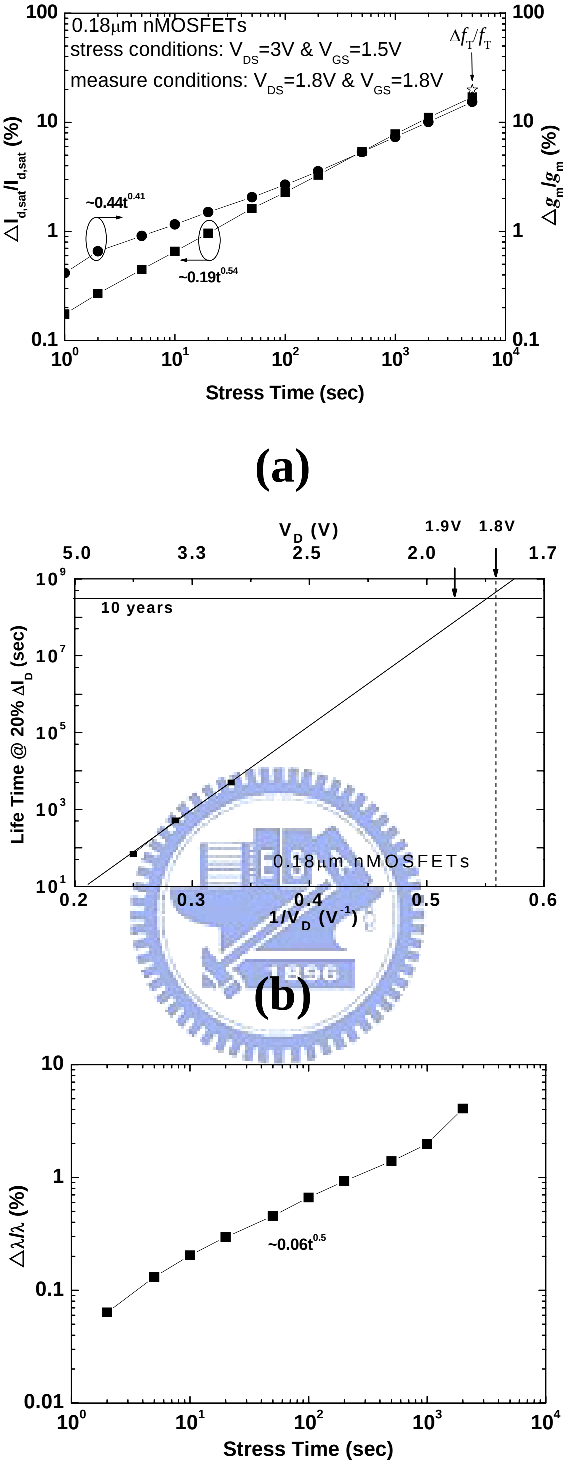


(a)

(b)

(c)

Fig. 3.3.1 Measured and modeled DC (a) I_d -V_d and (b) I_d -V_g and (c) r_o-V_d characteristics of 16 finger and 32 finger 0.18 μm RF MOSFETs before (solid symbols) and after (open symbols) hot-carrier stress. The line represents the simulation using a self-consistent device model.



(a)

(b)

(c)

Fig. 3.3.2 (a) Time dependence of $I_{d,sat}$ and g_m degradation for 0.18 μm RF MOSFETs. (b) The lifetime at 20% $\Delta I_{d,sat}/I_{d,sat}$ for 0.18 μm RF MOSFETs. The stress conditions were equivalent to 12.5 years of continuous operation at 1.8V or a 2.7 year lifetime at 1.9V overdrive. (c) Time dependent degradation of the drain current noise correlation factor, λ.

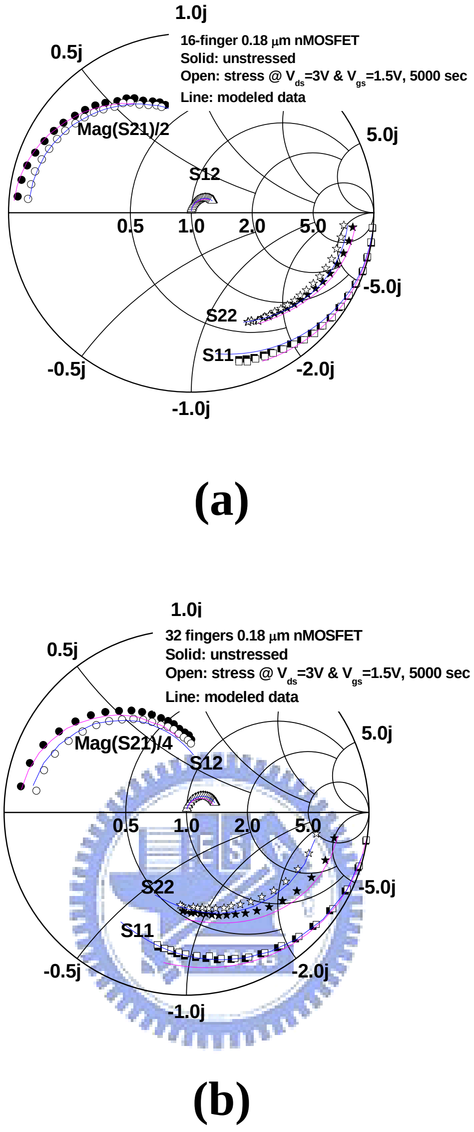


Fig. 3.3.3 Measured and modeled S-parameters for (a) 16 and (b) 32 finger 0.18 μm RF MOSFETs before (solid symbols) and after (open symbols) hot-carrier stress. The lines represent the simulated data.

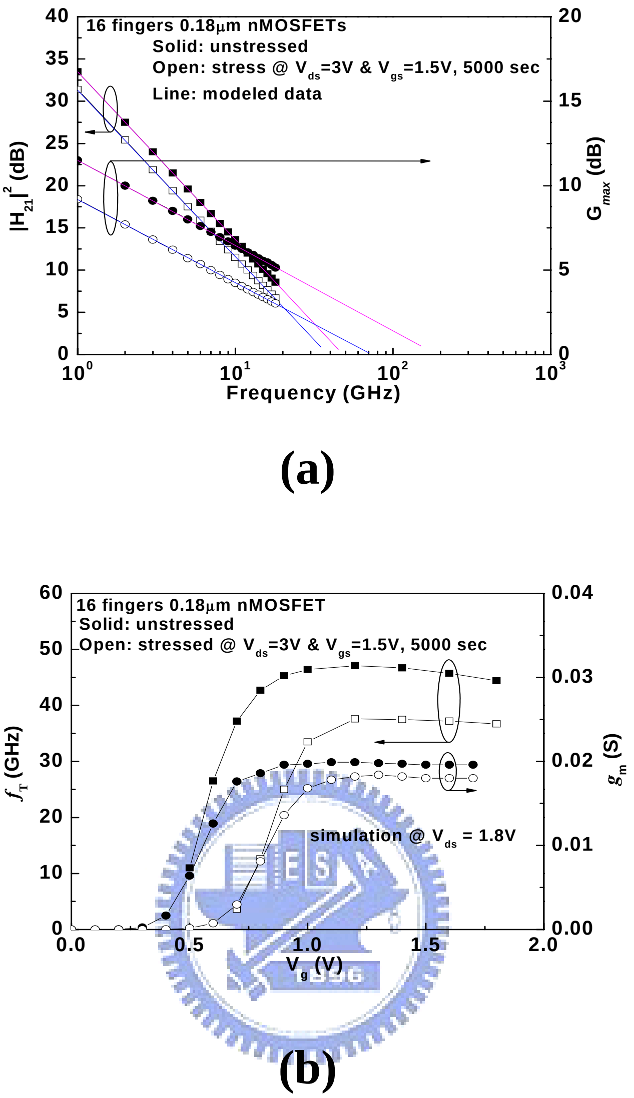
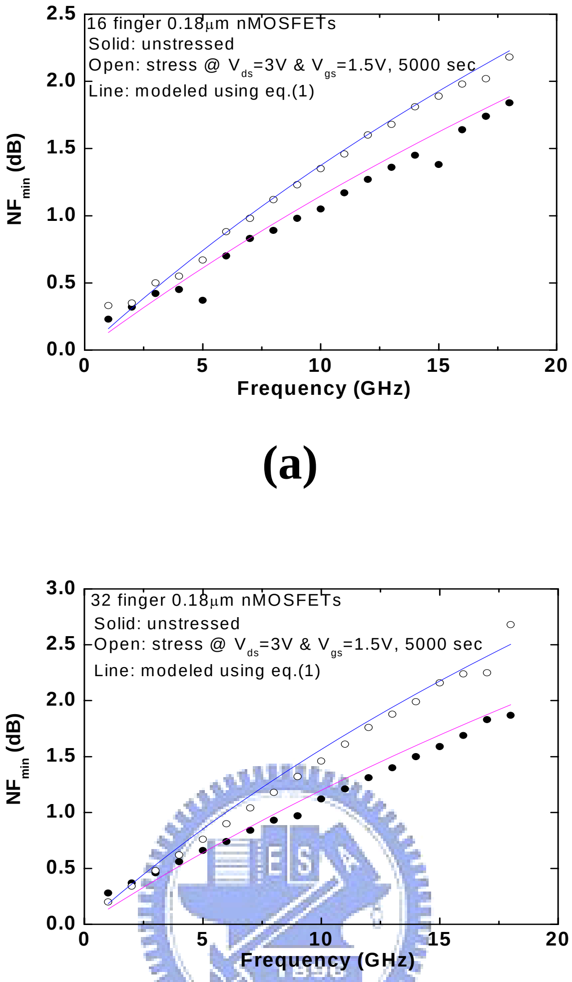


Fig. 3.3.4 (a) Measured and simulated $|H_{21}|^2$ and G_{max} vs. frequency. (b) The f_t vs. V_g for 16 finger 0.18 μm RF MOSFETs, before (solid symbols) and after (open symbols) hot-carrier stress.



(a)

(b)

Fig. 3.3.5 Measured and modeled NF_{min} of (a) 16- and (b) 32-finger 0.18 μm MOSFETs before and after hot-carrier stress.

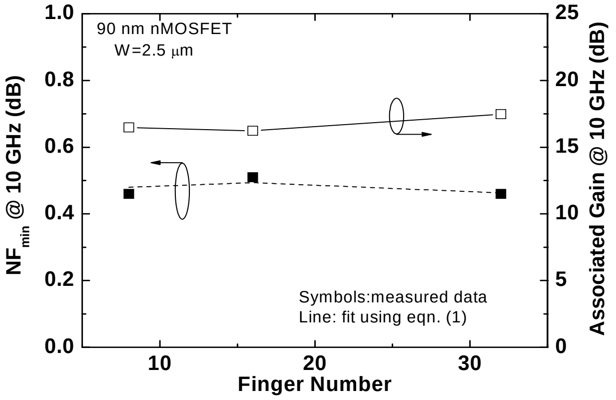


Fig. 3.5.1 NF_{min} and Associated Gain vs. number of gate fingers for 90 nm node RF MOSFETs, at 10 GHz

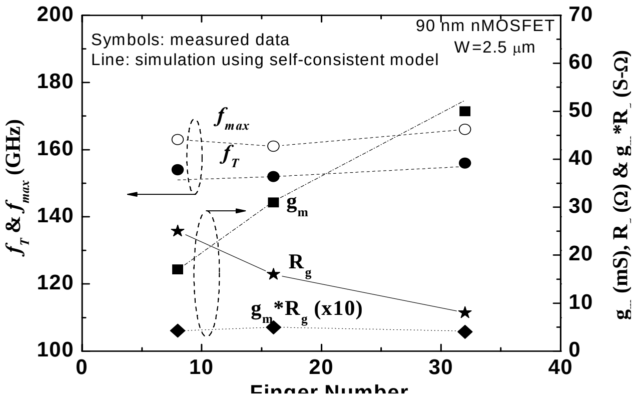


Fig. 3.5.2 Measured f_T, f_{max}, g_m, R_g and g_m*R_g vs. number of gate finger for 90 nm node RF MOSFETs

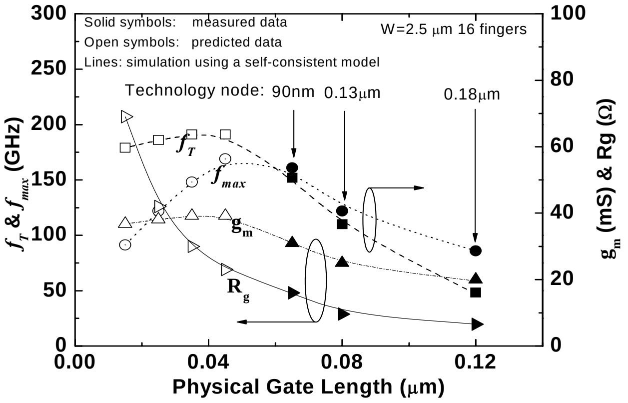


Fig. 3.5.3 Measured f_T, f_{max}, g_m, and R_g of down-scaled RF MOSFETs.

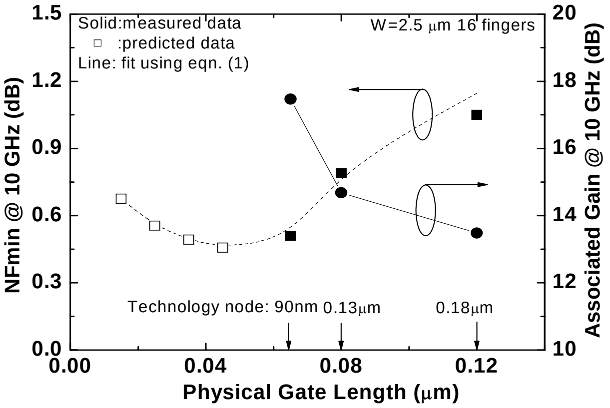


Fig. 3.5.4 NF_{min} and Associated Gain for down-scaled RF MOSFETs. The line is simulation data

Table 3.2.1 Device parameters used in the NF_{min} simulation for 16 finger and 32 finger 0.18 μm MOSFETs, before and after hot-carrier stress.

Device	**before stress**		**after 5,000 sec stress**	
parameters	**16 finger**	**32 finger**	**16 finger**	**32 finger**
f_T **(GHz)**	48.3	48.0	38.7	37.2
γ	0.67	0.7	0.67	0.7
g_m **(S)**	0.02	0.039	0.017	0.034
R_g **(Ω)**	6.55	3.45	6.55	3.45
$g_m * R_g/\gamma$	0.196	0.192	0.167	0.168

Chapter 4

RF MOSFETs on Plastic Substrate

4.1 Introduction

The integration of RF ICs on plastic substrates is a useful technology for RF ID [4.1.1]-[4.1.2] and wireless display applications. Plastic substrates are not very lossy and are highly insulating (resistivity ~10^8-10^9 Ω–cm) - this is ideal for RF IC integration. In contrast, VLSI-standard Si substrates have a much lower resistivity of 10 Ω-cm; this results in large RF substrate loss and poor Q-factors [4.1.3]-[4.1.12]. The performance of RF passive devices on Si can be improved by integration on high-resistivity Si substrates [4.1.9], using MEMS [4.1.10]-[4.1.12] or ion-implant translated semi-insulating (10^6 Ω-cm) Si technology [4.1.3]-[4.1.8]. This improvement is traded-off by the increased cost of added mask and process steps, or package costs. A challenge for integrating RF ICs on plastic is that high performance transistors are required and need to be transferred from their Si substrates, and mounted on plastic with little performance degradation. Integration with high performance RF passive devices on the plastic substrate demands that the Si substrate of the RF transistors be thinned.

Plastic substrates are also flexible. Thin-body Si ICs on plastic can be used for Flexible Electronics, RF ID, wireless Displays and System-on-Plastic [4.1.2], [4.1.13]-[4.1.14] , since no practical flexible polymer or organic transistors have been demonstrated for the RF regime. Additionally, the RF performance on thin-body (30~50 μm) Si MOSFETs can be improved by applying mechanical strain, which narrows the performance gap between them and III-V transistors [4.1.13]-[4.1.14]. We could apply tensile strain to improve the RF performance of Si MOSFETs. This was done by thinning the Si substrate to 40 μm and mounting it on plastic, which could be flexed to create strain.

In this chapter, we report the DC to RF performance of 0.13 μm thin-body (40 μm) Si MOSFETs on plastic, aiming to improve the RF performance. Using a microstrip line layout, to shield the RF noise from the low resistivity Si substrate [4.1.13]-[4.1.15], good performance, in terms of the minimum noise figure (NF_{min}), associated gain and cut-off frequency (f_T) was measured for the 0.13 μm MOSFETs mounted on plastic. The data were close to those for control devices, indicating little process-related degradation. The DC-RF performances were enhanced by applying 0.7% tensile strain. The improvements arise from the thin body thickness (t_b) and high flexibility, since the surface strain increases with $1/t_b^2$ [4.1.16]. The RF noise improvement fits an analytical NF_{min} equation well [4.1.17]-[4.1.19], and it is due to the increase in g_m and the RF gain under strain.

4.2 Experiment Procedure

Multiple-gate-finger (8, 16, and 32) 0.13 μm MOSFETs [4.1.17]-[4.1.19] with a novel microstrip line layout [4.1.17]-[4.1.19] were used in this study. The multiple-gate-finger structure was used to reduce the gate-resistance-generated thermal noise and the microstrip line layouts were designed using Metal-1 as the ground plane to reduce the RF noise from the lossy Si substrate. To achieve integration onto plastic, we first thinned down the Si substrate from 500 μm to 40 μm by using a Chemical Mechanical Polish (CMP) procedure. The thinned die was then glued onto a 180 μm thick light-transparent polyethylene terephthalate (PET) plastic as shown in Fig. 4.2.1(a). The plastic had a resistivity of 10^9 Ω-cm. Figure 4.2.1(b) shows the 40 μm Si substrate under a large surface strain. Thus, it is possible to apply a large mechanical strain to the flexible Si substrate devices on plastic and not crack the Si substrate. We have calculated the surface strain by using ANSYS 8.0 simulation software and the device characteristics, under various applied tensile strains, using TMA process-device simulation software.

The device characteristics were measured using an HP4155C for DC, HP8510C network analyzer for S-parameter and ATN-NP5B for noise measurements.

4.3 Device Characteristic of 0.13 μm RF MOSFETs on Plastic Substrate

Figure 4.3.1 shows a comparison of DC I_d -V_g and I_d–V_d characteristics for the 16-gate-finger n-MOSFET on a VLSI-standard substrate and on plastic with the 40 μm Si. The measured I_d -V_g and I_d –V_d of the 0.13 μm devices, before and after thinning and mounting on plastic, is almost identical. Thus there is little degradation resulting from the thinning-down process and mounting on plastic. Similarly, little change appeared in the measured S-parameters and $|H_{21}|^2$ RF gain for the 0.13 μm MOSFETs, before and after thinning down and mounting, as depicted in Fig. 4.3.2. It is indicated that the thinned-down process did not damage the devices. Good device performance is indicated by a f_T of 103 GHz for the 0.13 μm RF MOSFETs.

In additional, Figs. 4.3.1 and 4.3.2 also shows the modeling data using TMA process-device simulations software. Good agreement between measured and simulation I_d–V_d, S-parameters and $|H_{21}|^2$ RF gain were obtained using the accurate TMA process-device simulations on VLSI-standard Si substrate.

RF noise in front-end MOSFETs is normally the dominant noise source for the whole of an RF system. Figure 4.3.3 shows the measured NF_{min} and associated gain of 16- gate-finger 0.13 μm MOSFETs on plastic substrates. For comparison NF_{min} of the reference devices on VLSI-standard Si substrates are also plotted. For the devices on plastic substrates, NF_{min} is 0.87 dB and a high associated gain of 14.1 dB was measured at 10 GHz for 16-finger device. The process of substrate thinning and mounting on plastic increases NF_{min} by only 0.06 dB at 10 GHz, suggesting the excellent RF device performance on plastic. Only slightly better RF performance, 0.06 dB lower NF_{min} and 0.6 dB higher associated gain, were obtained for the control 0.13 μm MOSFETs at 10 GHz. These very small NF_{min} and associated gain differences, for the devices on plastic and on control Si substrates, are consistent with the nearly identical S-parameters shown in Fig. 4.3.2.

4.4 Strain Enhanced Device Characteristic of 0.13 μm RF MOSFETs on Flexible Plastic Substrate

By exploiting the flexibility of the thin substrate, we have applied a tensile stress to the MOSFETs die on plastic. The schematic of mechanical stress measurement is shown in Fig. 4.4.1. The large surface strain ($\varepsilon = 3aF/bt_b^{2}E$) [4.4.1] results from the applied force (F) associated with the bending distance (a) and width (b). Figure 4.4.2 shows the thin Si substrate under an applied longitudinal tensile strain, as calculated using ANSYS 8.0 simulation software. The bending distance was 0.17 cm when using 0.8 GPa stress on 40 μm thick Si substrate. This condition gives a tensile strain of 0.7% (= 0.8GPa /115GPa), assuming that the Young's Modulus of Si is 115GPa.

Under the same conditions, the experimental data of the effect of strain on the DC characteristics are also shown in Fig. 4.4.3. After applying a ~0.7% tensile strain, the thin-Si body MOSFETs on plastic showed a 0.045V lower threshold voltage (V_{th}) and a 14.3% higher $I_{d,sat}$.

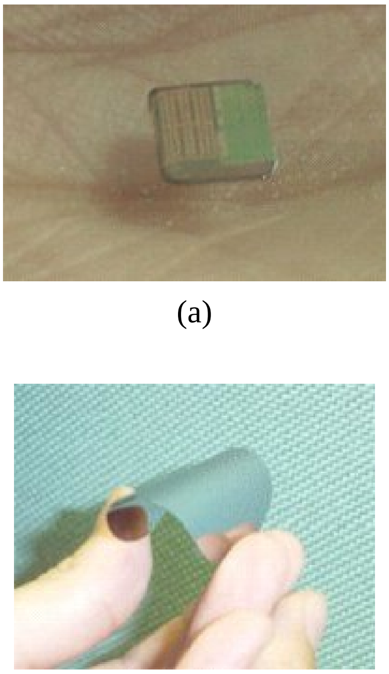
To understand the improvements, we have used TMA process-device simulation software to simulate the effect of strain on the 0.13 μm MOSFETs. The simulated stress distribution is shown in Fig. 4.4.4. A good match between the measured and simulated I_d-V_g and I_d–V_d results were first achieved for the unstrained case to show the accuracy of the TMA simulation and they are included in Figs. 4.4.3(a) and (b), respectively. Then effect of strain on 0.13 μm transistors themselves was simulated. Figure 4.4.4 (b) summarizes the measured and simulated $I_{d,sat}$ improvement as a function of strain. The strain lowers V_{th} ($=\phi_{MS}-Q_{ox}/C_{ox}+2\phi_F+Q_{dpl}/C_{ox}$) because it reduces the energy band-gap (E_G) and thus ϕ_F and Q_{dpl}. A significant $I_{d,sat}$ improvement (14.3%) was seen compared with SiN-capped 90 nm strained-Si nMOS, where the increase was 11% [4.4.1]. The effect arises from the $1/t_b^2$ dependence of the strain for thin-body Si. This shows that both the lower RF loss for the passive devices and a higher transistor drive current can be obtained simultaneously using the mechanical strain made possible by using highly-insulating plastic substrates.

Fig. 4.4.5 includes the dependence of the RF current gain $|H_{21}|^2$ with frequency, for a 16-gate-finger 0.13 μm device with tensile strain, was $|H_{21}|^2$ follows the typical -20 dB/decade slope with increasing frequency. After applying a 0.7% tensile strain to the 40 μm thinned-body Si of the 0.13μm RF MOSFETs, f_T increased from 103 GHz to 118 GHz. These improvements were consistent with the simulations, which are included in Fig. 4.4.5.

We also investigated how strain affects the RF noise. Figure 4.4.6 shows NF_{min} and the associated gain of the 0.13μm transistors under tensile strain. For the unstrained case, a good NF_{min} of 0.87 dB and associated gain of 14.1 dB at 10 GHz was observed. Under the applied 0.7% tensile strain, better RF characteristics were achieved, such as a lower 0.75 dB NF_{min} and a higher 15.3 dB associated gain at 10 GHz. This is related to the larger g_m, smaller V_{th} and higher $I_{d,sat}$ arising from the strain, as shown in Fig. 4.3.1 and Fig. 4.4.3. The lower NF_{min} arises by eq.(1) and that the strain improved the f_T. The close agreement between the measured and simulated NF_{min} also appears in Fig. 4.4.6. The improved NF_{min} and associated gain values are comparable with those for 90 nm node SiN-capped strained-Si nMOS [4.4.2], and also depicted in Fig. 4.4.6. The large DC-RF improvements with tensile strain are the main advantages of thin-Si-body flexible electronics on plastic, in addition to the improved RF passive device performance.

4.5 Conclusion

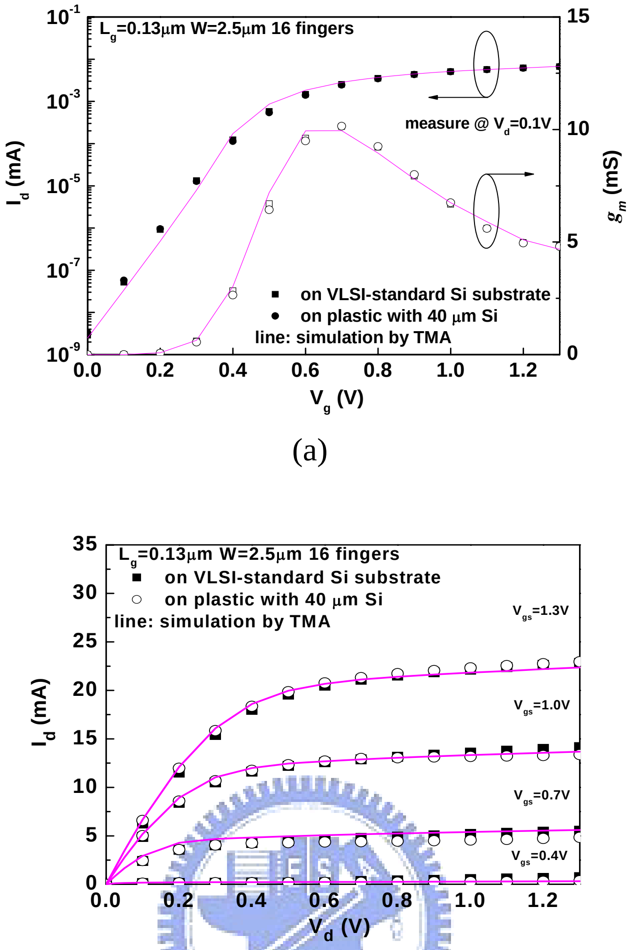
We have successfully demonstrated high DC and RF performance for 0.13 μm RF MOSFETs on 40 μm Si substrates mounted on a flexible plastic base. These devices showed excellent DC and RF performance after applying tensile strain to the thinned-down substrate. The high performance RF transistors are suitable for low-noise ultra-wide band (UWB) (3.1-10.6 GHz) applications.



(a)

(b)

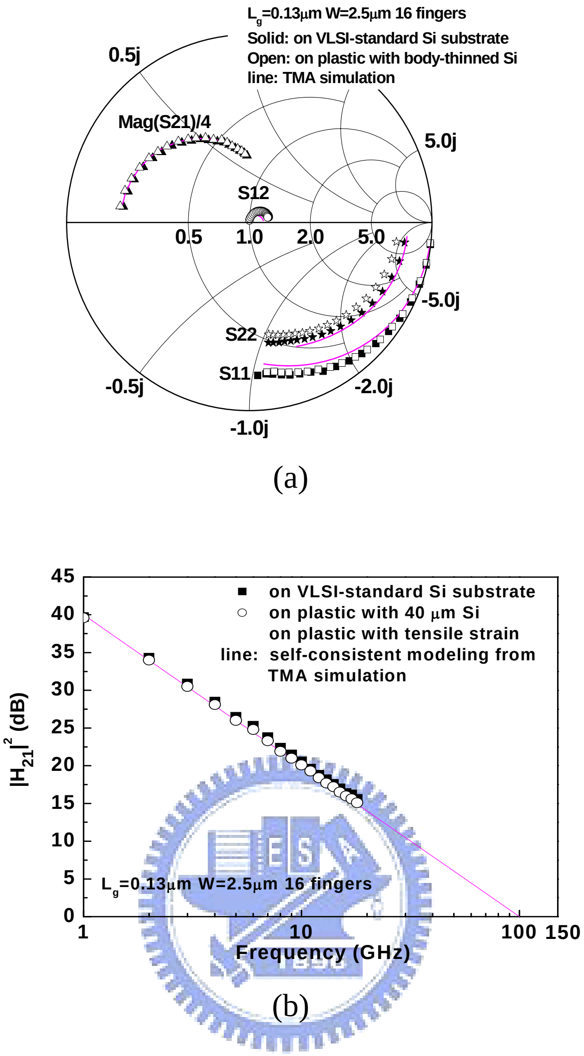
Fig. 4.2.1 (a) Image of a die with multiple-gate-finger 0.13 μm RF MOSFETs on transparent plastic (hand-held). (b) Image showing the flexibility of the ~40 μm-thick Si substrate (t_b) under mechanical strain (which is proportional to $1/t_b^2$).



(a)

(b)

Fig. 4.3.1 (a) Measured and simulated I_d-V_g characteristics and (b) I_d-V_d for 16-gate-finger 0.13 μm RF MOSFETs on a VLSI-standard substrate and on plastic with 40 μm Si. The solid lines are the TMA-simulated data for a VLSI-standard Si substrate.



(a)

(b)

Fig. 4.3.2 Measured and simulated (a) S-parameters and (b) $|H_{21}|^2$ as a function of frequency for 16-gate-finger 0.13 μm RF MOSFETs on a VLSI-standard substrate and on plastic with 40 μm Si. The line is the modeled data. The devices were DC biased at V_g =1.0V and V_d =1.3V.

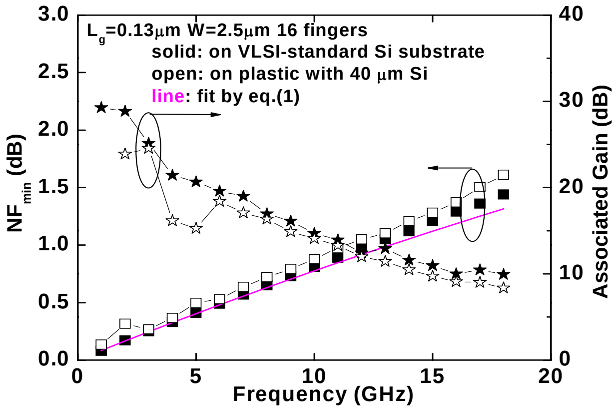


Fig. 4.3.3 Measured and modeled NF_{min} and associated gain of 16-gate-finger 0.13 μm RF MOSFETs on VLSI-standard Si substrate and on plastic. The line is the TMA-modeled data and derived from the NF_{min} equation.

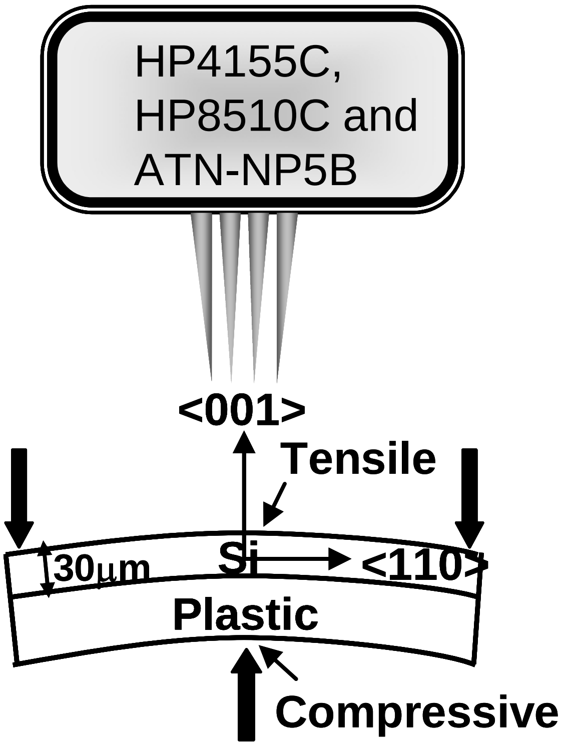


Fig. 4.4.1 The schematic of the mechanical stress measurement.

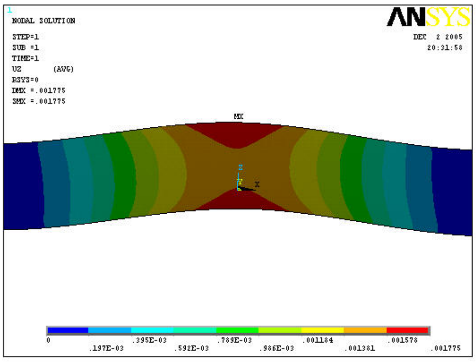
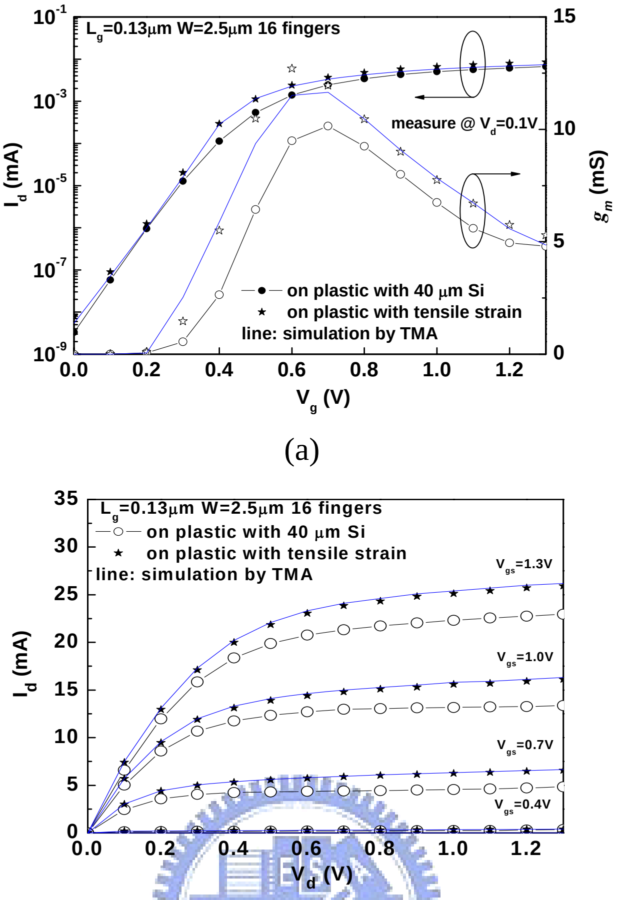


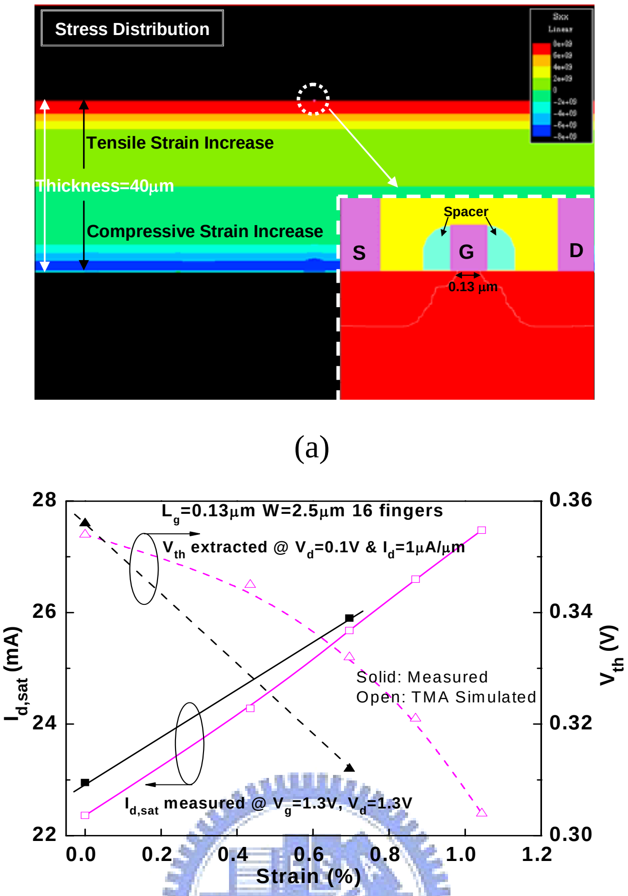
Fig. 4.4.2 The mechanical stress calculated by using ANSYS 8.0 simulation software.



(a)

(b)

Fig. 4.4.3 Measured and simulated (a) I_d-V_g and (b) I_d-V_d characteristics for 16-gate-finger 0.13 μm RF MOSFETs on plastic with 40 μm Si, with or without tensile strain. The solid lines are the TMA-simulated data for 0.13 μm RF MOSFETs on plastic under ~0.7% tensile strain.



(a)

(b)

Fig. 4.4.4 (a) TMA device simulation of a 40 μm Si-body 0.13 μm RF MOSFETs under applied mechanical strain. (b) Simulated (shown open) and measured (shown solid) $I_{d,sat}$ and V_{th} versus strain. The strain increases $I_{d,sat}$ but decreases V_{th}.

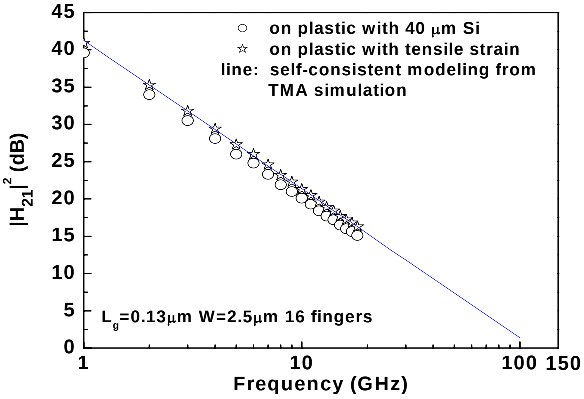


Fig. 4.4.5 Measured and simulated $|H_{21}|^2$ as a function of frequency for 16-gate-finger 0.13 μm RF MOSFETs on on plastic with 40 μm Si with or without tensile strain. The solid lines are the TMA-simulated data for 0.13 μm RF MOSFETs on plastic under ~0.7% tensile strain.

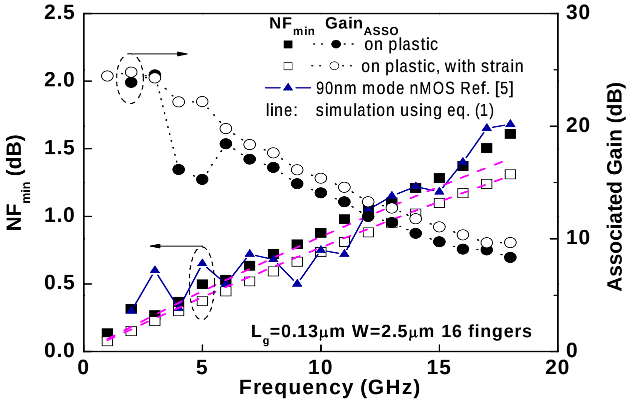


Fig. 4.4.6 Measured and modeled NF_{min} and associated gain of 16-gate-finger 0.13 μm RF MOSFETs on plastic with 40 μm Si, with or without tensile strain. The line is the TMA-modeled data and derived from the NF_{min} equation.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

We have successfully developed a model to predict device DC I-V, S-parameters, and NF_{min} by using a microstrip transmission line layout design. The novel microstrip transmission line layout can help us to develop the RF active device model accurately. Close agreement was obtained for the accurate NF_{min} measurements and the analytical NF_{min} simulation. This approach is important as a tool in predicting the RF performance degradation of MOSFETs in a circuit where the devices are under continuous bias operation.

In the meanwhile, we have successfully demonstrated high DC and RF performance for 0.13 μm RF MOSFETs on 40 μm Si substrates mounted on a plastic. These devices showed excellent DC and RF performance after applying tensile strain to the thinned-down substrate. The high performance RF transistors are suitable for low-noise ultra-wide band (UWB) (3.1-10.6 GHz) applications.

5.2 Future Works

Since the great improvements in the RF MOSFETs had been demonstrated for ultra-wide band (UWB) (3.1-10.6 GHz) applications. More works is to further integrate RF MOSFETs with novel microstrip layout on circuit level application. It can help us to realize the high performance CMOS RF/microwave circuit or system.

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論文題目：

射頻金氧半場效電晶體之電性效應與元件模型

(Electrical Stress Effects and Device Modeling of RF MOSFETs)

PUBLICATION LISTS

(A) International Journal:

[1]. **H. L. Kao**, Albert Chin, C. C. Liao, C. C. Chen, S. P. McAlister and C. C. Chi, "Electrical Stress Effects and Device Modeling of 0.18 μm RF MOSFETs," in *IEEE Transactions on Electron Devices*, Vol. 53, Issue 4, pp. 636-642, April, 2006.

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