國立交通大學

電子工程學系 電子研究所

博士論文

高敏感度之矽鍺奈米生醫感測之研究與應用

The Investigation and Application of High Sensitivity SiGe Nanowire for Bio-sensor

研 究 生：郭俊銘

指導教授：張國明　教授

中華民國九十七年七月

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研究生：郭俊銘　　Student：Jiun-Ming Kuo

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博士論文

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中華民國九十七年七月

高敏感度之矽鍺奈米生醫感測之研究與應用

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中文摘要

在這篇論文中我們探討矽鍺奈米線的感測能力之優缺點，並針對氧化過後之矽鍺薄膜做研究，緊接著將此結果應用於矽鍺奈米線並作感測能力之探論。

首先，先探討著矽鍺奈米線與傳統的多晶矽奈米線差異，矽鍺奈米線擁有優於傳統多晶矽奈米線較高的導通電流，但也擁有著較高的接觸電阻。

接著，我們利用傳統的薄膜電晶體元件做為我們測試結構，探討著不統的氧化條件下所造成的電流增益情況。越高的溫度及越長的時間氧化，都會造成其電流增益。此外，我們嘗試著在不同的氧化溫度與時間的條件已達到相同的氧化厚度，其電流增益也相同，此結果為相同的氧化厚度所導致的鍺析出也是一樣的。

其次，我們探討著不同的矽鍺濃度的奈米線的蛋白質感測。越高的鍺濃度擁有較高的感測能力，但是太高的鍺濃度其感測能力卻下降，我們推測是因為表面擁有過多的缺陷所導致。

再者，我們探討著矽鍺奈米線氧化厚的感測能力，在低濃度時，其感測能力隨著氧化溫度升高而提高，但是隨著濃度的提高其感測能力可能會因為過高的氧化溫度而下降，其原因可能為氧化溫度或時間過久使的鍺濃度超過一定值時會造表面缺陷上升。

最後，除了從材料或表面處理外，我們提出了一個新穎的結構來提升其奈米線的敏感度，利用雙層的高導通與低導通電特性，來有效的決定電流的路徑，

如此在相同的電場變化下可擁有著較高的影響力，已得到較高的感測能力。

The Investigation and Application of High Sensitivity SiGe Nanowire for Bio-sensor

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Abstract

In this thesis, we concentrate our efforts on the advantage and disadvantage of SiGe nanowire and Poly-Si nanowire for bio-sensor. The behavior of oxidation for SiGe film was studied in the follows. The application of the SiGe oxidation was used to enhance the sensitivity in the end of thesis.

First, we demonstrated the electric properties of SiGe and Poly-Si nanowires. The higher drive current is obtained for SiGe nanowire, but the disadvantage of the higher contact resistance appeared for SiGe nanowire.

Secondly, the thin-film-transistor (TFT) was used to understand the increase of drive current after different oxidation conditions. The higher drive current obtained for the higher temperature, oxidation time and oxygen flow. Besides, the same oxide thicknesses were achieved by controlling the different oxidation time and temperature.

The same drive current improves for the same oxide thickness. The reason come form the same Ge condensed after oxidation.

Third, we studied the sensitivity of SiGe nanowire with different Ge concentration. The higher sensitivity was observed for the SiGe nanowire with high Ge concentration. However, the sensitivity decreased for the over-high Ge concentration. The reason may be that the higher defect appears on the surface.

Finally, we used the Ge condensation technique on the SiGe nanowire for bio-sensor. The sensitivity improved for the SiGe nanowire with low Ge concentration after high temperature oxidation. However, the sensitivity decreased for SiGe nanowire with higher Ge concentration. It may be that the higher defect appears on the surface.

In the end of the thesis, we introduce a novel structure to improvement the sensitivity. A double layer with high/low drive current is combined to achieve this point. The sensitivity improves under the same electric filed change by controlling the current through.

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本論文的完成首先要感謝我的指導老師張國明教授，張教授在研究上的指導確切詳盡，在生活上的關心無微不至，讓我這五年的博士生活中受益良多，其幫忙與建議，讓我的論文發表更順利。

在完成論文的建立過程中，還要特別感謝實驗室的學長學弟們的幫助：游凱翔學長、楊文誌學長、王敬業學長、朱俊宜學長、趙高毅學長、吳資麟學弟、曾文賢學弟、吳恆信學弟、梁家榮學弟、趙文全學弟、滕聚翔學弟、王育彬學弟、鄭文魁學弟在實驗上的建議與幫忙；林建宏學弟、陳伯寧學弟和黃士軒學弟等在我心情低落時陪我放鬆心情;感謝交通大學奈米中心（NCTU-NFC）林素珠小姐、徐秀鑾小姐、何惟美小姐在實驗上的幫忙。

最後謹以此論文現給我的父母親郭春坤先生與陳寶春女士，感謝他們在我求學階段的鼓勵與支持，感謝我的哥哥和妹妹們的鼓勵，因為你們的存在，我才能順利完成我的博士論文，謝謝你們。

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Chapter 1

Introduction of Nanowires

1.1 The Application of Nanowires

Nanowires (NWs) have been attracting considerable attention in recent years. In fact, the downscaling of material dimension does not only imply an increase in device packing density but also a decrease in power consumption. Semiconductor nanowires (NWs) are nowadays intensively studied due to their great potential for electronic and photonic devices[1-2], Poly-Si TFT channel[3], high performance Logic transistor[4] and highly sensitivity Bio-Sensor[5-9] have recently been demonstrated. Since the development of nano-technology, more and more people combine the one-dimension nano-structure with bio-molecular. Due to the large surface-to-volume ratio and quasi-1D characteristics, the Silicon nanowire (NW) sensor provides a high sensitivity in chemical detection such as pH buffer solution, protein, ions, and DNA[5-9] etc. Silicon nanowires (SiNWs) are particularly appealing for sensing applications since the silicon dioxide can effectively passivate surface dangling bonds, and at the same time can be chemically modified through the well known silanol chemistry to provide surface functionalization and, therefore, selectivity for particular analytes. Liber[5] is the first person to use the SiNWs as bio-sensor. First, we discuss the mechanism of bio-detecting which diagram is shown is figure 1.1(a). The P-type SiNWs (Boron doping) with two metal pads served as Source and Drain were deposited on the Silicon wafer with 2000 Å thermal silicon dioxide growth and 5000 Å aluminum served as bottom gate was deposited on the back side. As the negative voltage applied on the bottom gate, more holes will accumulate in the Silicon nanowire thus increase the conductance. However, if the positive voltage applied on the bottom gate, the holes will deplete in the SiNW thus decrease the conductance. Figure 1.1 (b) shows the conductance of SiNW with positive or negative gate voltage applied. We can consider the conductance as a function of extra-voltage applied.

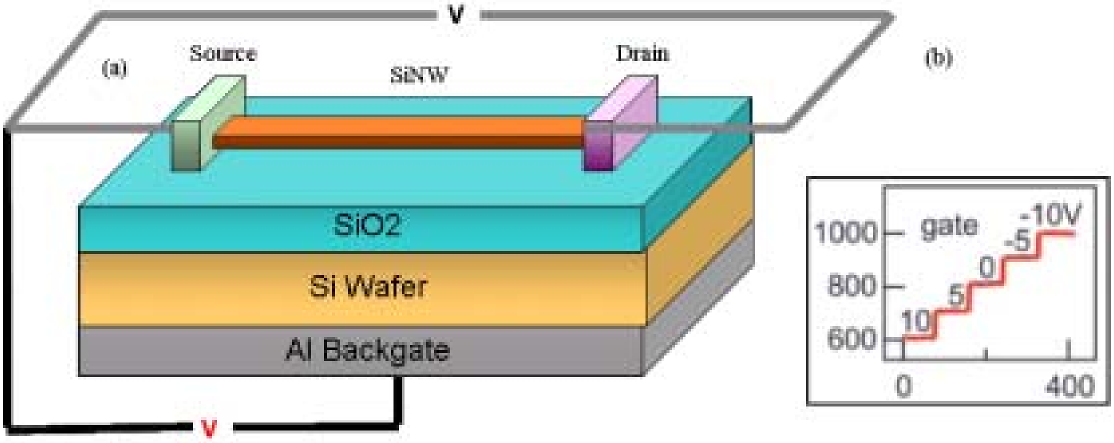

Figure 1.1 (a) The diagram of silicon nanowire. (b) The conductance changed with back side gate voltage changed. (Ref. 5)

Second, Liber considered silicon nanowire solid state FET whose conductance is modulated by an applied gate. The 3-amino-propyl- triethoxy-silane (APTES) that composition shown in figure 1.2 (a) was used to modify the surface, which can detect the charge with different pH solutions. The H$^+$ will absorb on the APTES as the lower pH buffer solution add. The H will be taken away as the high pH buffer solution add. The conductance of silicon nanowire will decrease by the additional H$^+$ which takes as a positive gate voltage. However, the conductance will increase by the additional O$^-$ which is treated as a negative gate voltage. Figure 1.2(b) shows the conductance of silicon nanowire with various pH buffer solutions. The conductance increases as the pH decreases. Thus the silicon nanowire with the APTES modified could serve as pH detection.

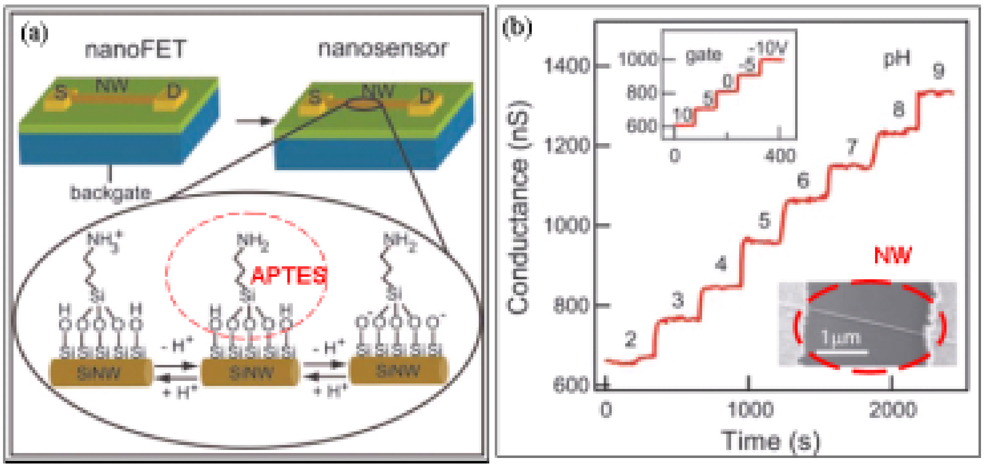

Figure 1.2 (a) The mechanism of pH solution detection. (b) The conductance changed with different pH buffer solutions. (Ref. 5)

Not only the pH solution but also other materials were measured by SiNWs. Figure 1.3 (a) shows the diagram after the bio-linker modified and the biotin-streptavidin connected with the bio-linker. Measurements show that the conductance of biotin-modified SiNWs increases rapidly to a constant value upon addition of a 250 nM streptavidin solution and that this conductance value is maintained after the addition of pure buffer solution (Figure 1.3(b)). The increase in conductance upon addition of streptavidin is consistent with binding of a negatively charged species to the p-type SiNW surface and the fact that streptavidin is negatively charged at the pH of our measurements. In addition, several control experiments were carried out to confirm that the observed conductance changes are due to the specific binding of streptavidin to the biotin ligand. First, addition of a streptavidin solution to an unmodified SiNW did not produce a change in conductance (figure (c)). Unlike the pHs detection, the biotin-streptavidin can not restore.

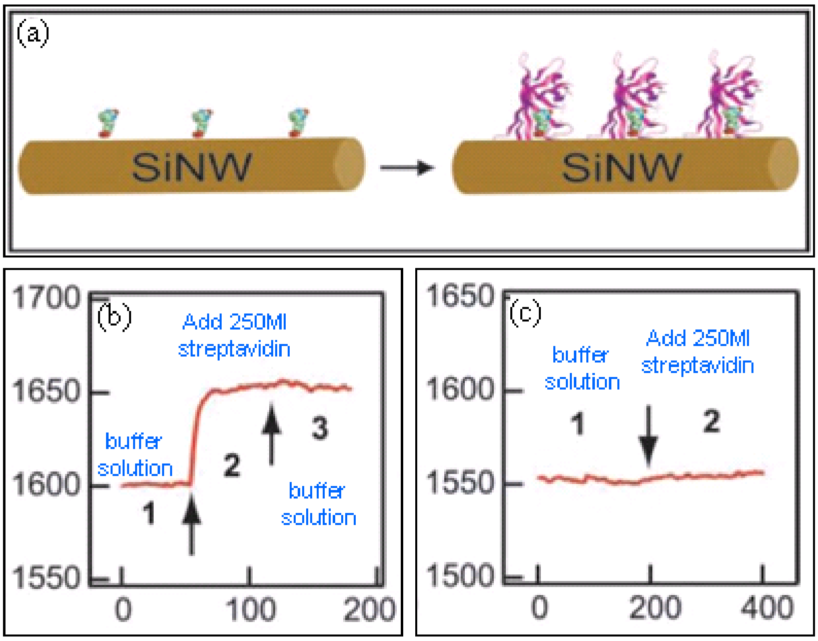

Figure 1.3 (a) Schematic illustrating a biotin-modified SiNW (left) and subsequent binding of streptavidin to the SiNW surface (right). (b) The conductance increases by positive biotin adsorption. However, the chemical link is irreversible. (c) The unchanged-conductance is found because of unmodified. (Ref. 5)

The Sequence-Specific DNA also can be detected by SiNWs. The 3-mercaptopropyltrimethoxysilane (MPTMS) by gas-phase reaction in Ar for 4 h was utilized to modify the surface. The CCT-AAT-AAC-AAT DNA linked on it. The conductance remained the same as the un-match DNA connected (Figure 1.4(a)). However, the conductance increases as the GGA-TTA-TTG-TTA DNA connect. The sequence DNA is confirmed on the SiNWs by the SPV technique (not shown here).

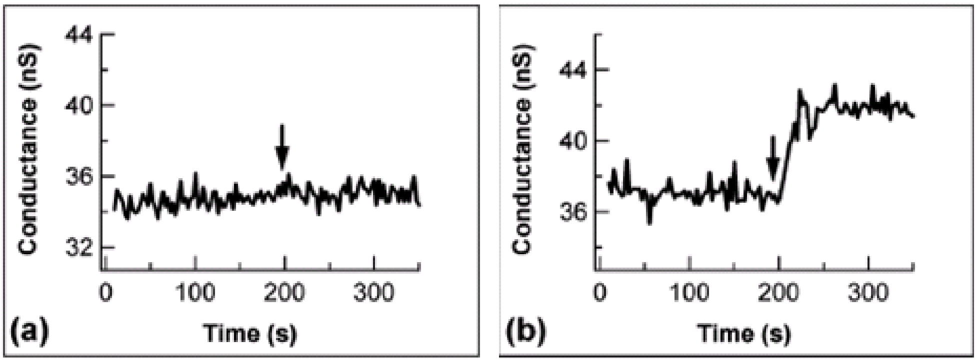

Figure 1.4 (a) The conductance does not change by un-match DNA (b) The conductance enhanced after matched-DNA modified. (Ref. 6)

1.2 The Materials of Nanowires Sensor

The main application for the nanowire is used to be a nano-sensor. Nanowire sensors were fabricated by various materials, such as silicon nanowire sensors[5-9], metal oxide semiconductor nanowire sensor[10-14], polymer nanowire sensesors[15-16], and metal nanowire sensors[17-18].

The fundamental sensing mechanism of metal oxide base gas sensors relies on a change in electrical conductivity due to the interaction process between the surface complexes and the gas molecules to be detected. Metal oxide nanowires were synthesized by thermal evaporation of oxide powders under controlled conditions without the presence of a catalyst. Ultralong nanowires have been successfully synthesized for ZnO, SnO_2, In_2O_3, CdO, Ga_2O_3, WO_3 and PbO_2 by simply evaporating the desired commercial metal oxide powders at high temperature[10-14].

For example, Gas sensors have been fabricated using the SnO_2 nanowires[11]. The responses of the sensors have been characterized for gaseous polluting species like CO and NO_2 for environmental applications, as well as for ethanol for breath analyzers and food control applications. The response of the current flowing through the SnO_2 nanowires when two square concentration pulses of CO (250 and 500 ppm) are fed into the test chamber, at a working temperature of 400 °C and 30% RH. The electric current increased for about 60% and 100% with the introduction of 250 and 500 ppm CO, respectively which is shown in figure 1.5.

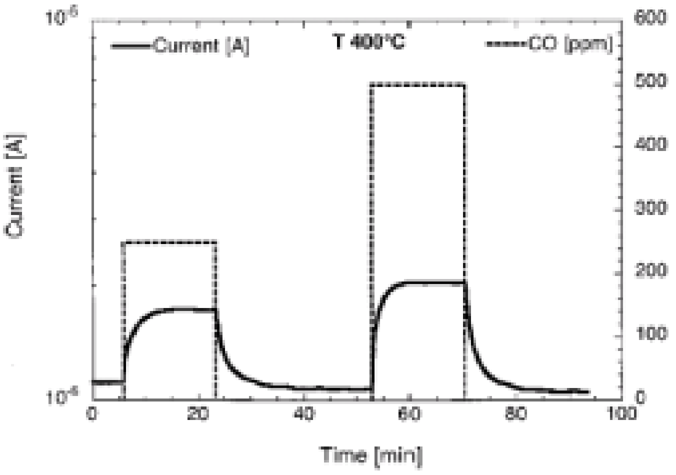

Figure 1.5 Response of the SnO_2 nanobelts to CO at a working temperature of 400 °C and 30% RH. (Ref. 11)

Conducting polymers have attractive features such as mechanical flexibility, ease of processing, and modifiable electrical conductivity. Polyaniline/poly-(ethylene oxide) (PANI/PEO) nanowire sensors that can detect NH_3 gas at concentrations as low as 0.5 ppm with rapid response and recovery time[15]. The measured current versus time curves, which reflect the gas-concentration dependence of the temporal conductance behavior, as shown in figure 1.6. The higher current changed as the higher NH_3 gas flowed.

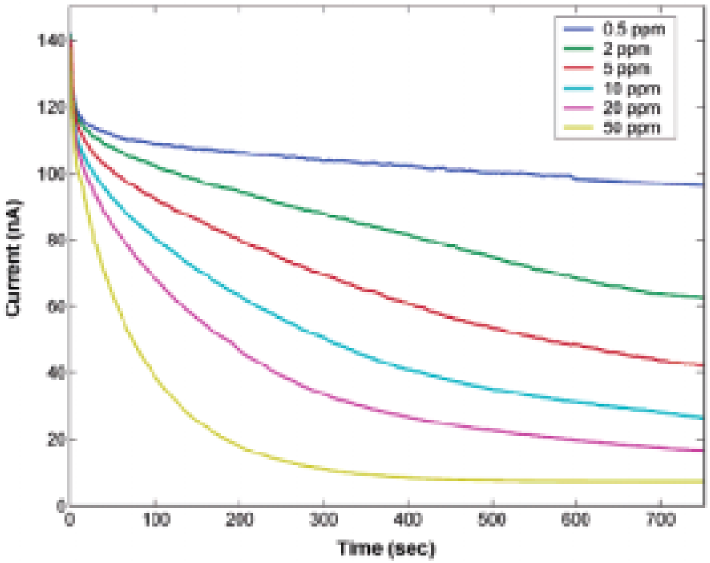

Figure 1.6 Measured time-dependent current through an individual CPNW sensor upon exposure to NH_3 gas. The nanowire device being tested was about 335 nm in diameter. (Ref. 15)

Pd nanowires have been studied to detect hydrogen gas due to safety reasons [17]. The sensor based on resistance change of Pd nanowires upon hydrogen incorporation. The measured electrical resistance versus time curves exhibited sharp decreases upon hydrogen injections. The electrical resistance change is dependent on hydrogen concentration, as shown in Figure 1.7. The higher current changed as the higher H_2 concentration.

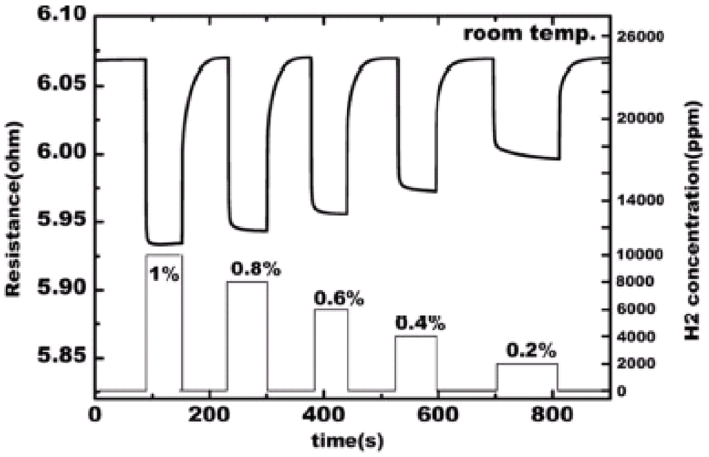

Figure 1.7 Sensor resistance responses for hydrogen concentration varied in a range from 0.2 to 1% by pulses. (Ref. 17)

All applications of nanowire sensor are listed in the following table 1-1.

Material of nanowire sensor	Application
Silicon	pH sensor, bio-sensor, DNA sensor and virus sensor
Metal oxide	gas sensor
Polymer	gas sensor and bio-sensor
Metal	gas sensor

Table 1-1 The applications of various materials of nanowire sensor.

1.3 Motivation

The more applications were observed for the silicon nanowire form table 1-1 since the silicon dioxide can effectively passivate surface dangling bonds, and at the same time can be chemically modified through the well known silanol chemistry to provide surface functionalization and, therefore, selectivity for particular analytes. The high surface-to-volume ratio of nanowires results in a strong dependence of carrier concentration on charge transfer from the surface and changes in nanowire conductance. For the study of SiGe field effect transistor[19], we could found that the higher current change as the same gate voltage applied (shown in figure 1.8). However, the mechanism for the silicon nanowire sensor is detecting the surface charge as the molecular stays on it. This result point out SiGe nanowires maybe have higher change in electrical property at the same chemical species bonding to surface of nanowires. Therefore, if we used the SiGe nanowire instead of Si nanowire, we would get higher current change at the same bio-molecular bound on the surface. It means we would have higher sensitivity for SiGe nanowire instead of Si nanowire.

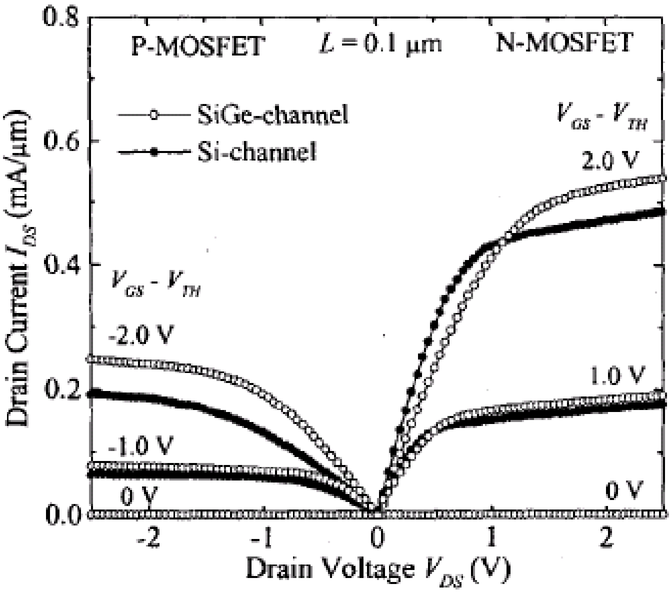

Figure 1.8 Drain current of N- and P-MOSFETs are improved with Si/SiGe-channel. (Ref. 19)

Chapter 2

Fabrication of Nanowires

2.1 Introduction

Various approaches for growing nanowires, including (1) lithography with photons in UV, DUV, EUV and X-ray spectrum[20] (2) machining using AFM, STM, NSOM[21] (3) nanoimprint lithography[22] (4) spacer formation[23] (5) vapor state synthesis[24] (6) vapor-liquid-solid growth(VLS) approach[25] (7) electrochemical deposition[26] (8) Laser Ablation[27].

2.1.1 Lithography with Photons

In photon and particle-based lithography, by using nonlinear resists, near-field phase shifting or topographically directed technology, it has been possible to achieve sub-50nm feature. For example, EBL has demonstrated the ability to achieve 20nm width nanowires with 60nm height. Height is often limited by the lift-off process. Extreme ultraviolet light (EUV) lithography has generated 38nm patterns[20].

2.1.2 Machining Using AFM, STM, NSOM

In 1990, J. A . Dagata *et al.* proposed the tip-induced anodic surface oxidation by using scanning probe lithography (SPL) to define nano- patterns on the semiconductor surface, as shown in Figure 2.1. AFM, STM and NSOM and the like are called SPM. The operation mechanism is in an environment humidity control when approximately 50% and the sample surface attaches a water thin film when the probe contacts this water thin film. Take the probe as negative electrode and take the sample surface as the positive electrode then the water molecule can start to ionization and produces the partial region oxide compound with the probe under- earth sample surface. The probe produces the electric field can along with the distance of sample surface to attenuation, the oxidation stops immediately when the electric-field intensity is smaller than 10^9 V/m[21]. The oxide compound growth speed gives the probe bias to have the enormous relations. In the process by way of program configure, but fine holds controls scans the probe the displacement, carries on oxide compound of the specific line to grow, then achieves the micro region design forming the goal, this is scanning probe lithography technique to apply to the lithography at the beginning of shape.

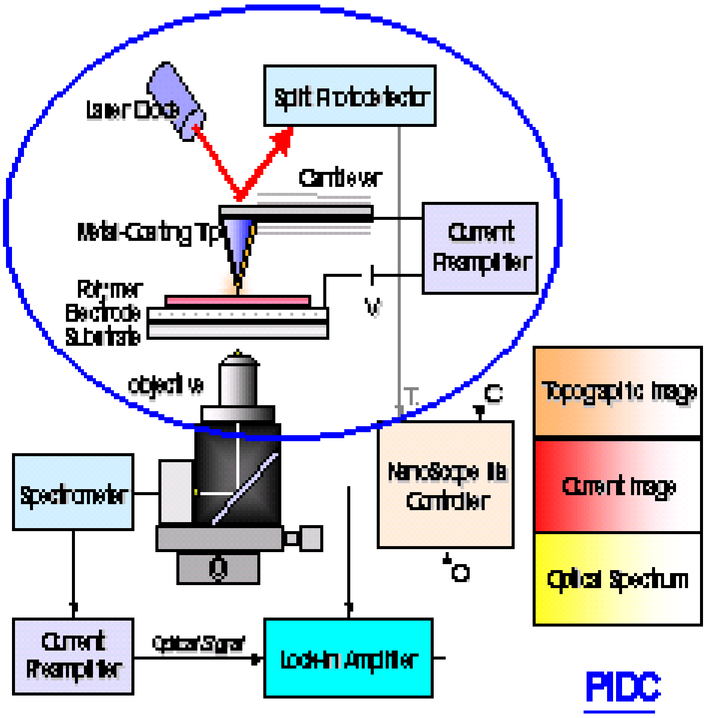

Figure 2.1 Schema of Scanning Probe Lithography (SPL).

2.1.3 Nanoimprint Lithography (NIL)

Nanoimprint lithography is a novel method of fabrication nanometer scale patterns. In previous report[22], the single crystalline Si nanowire structures are fabricated as a mold for producing high surface area Pt wire. PMMA are spun on substrate and are used as imprint resist. The process flow for nanoimprint patterning is shown in Figure 2.2.

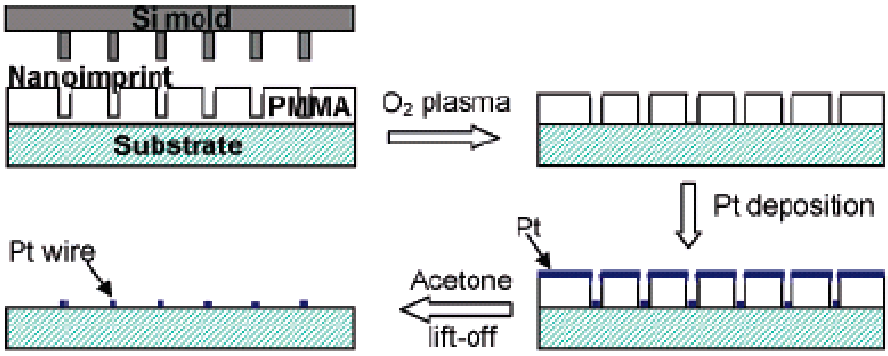

Figure 2.2 Schema of imprint process. (Ref. 22)

2.1.4 Spacer Formation

Controlled deposition and size reduction, which involves deposition on cleaved edges, or oxidation, followed by anisotropic etching forming spacers This process provides a density increase as well as size reduction. It can be used to pattern silicon fins for double-gate MOSFETs shown in Figure 2.3.

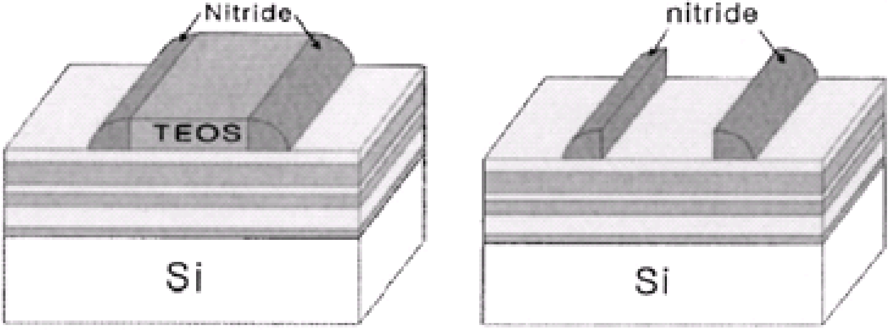

Figure 2.3 Schema of spacer process. (Ref. 23)

2.1.5 Vapor State Synthesis

Vapor state synthesis of single-crystalline freestanding Ag nanowire has been reported by Kim's group[24]. Their synthetic method is unique in that it uses only a single reactant, Ag_2O, without using any templates or catalysts. In a typical synthesis,

Ag_2O powder was placed in an alumina boat in the middle of horizontal quartz tube furnace. The NWs were grown at a few centimeters downstream from the precursor on a Si substrate. At high temperature (T = 900°C-1000°C), the precursor vapor was carried downstream by the flow of Ar to a lower temperature zone (T = 500°C), where Ag NWs were grown.

2.1.6 Vapor-Liquid-Solid (VLS) Growth Approach

Vapor state synthesis grown nanowires lack a diameter-control mechanism. Diameter of nanowires can be controlled by the catalyst nanoparticle size. Zhou's group reported an efficient route for the synthesis of single-crystalline In_2O_3 nanowires via the VLS mechanism, where the in vapor was generated by laser ablation of an indium-containing target. Excellent diameter control was achieved by using monodispersed gold clusters as the catalyst[25].

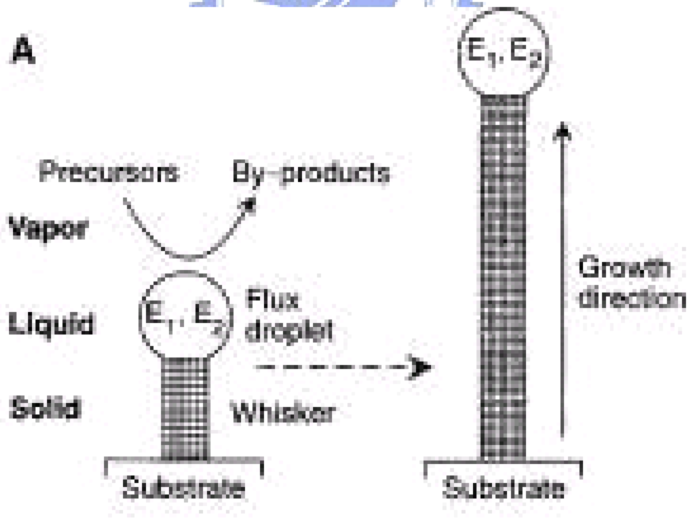

Figure 2.4 Mechanism of spacer process. (Ref. 25)

2.1.7 Electrochemical Deposition

Anodized aluminum oxide (AAO) film is a kind of poriferous material. In previous report, the free-standing Pd nanowires were prepared by electrodeposition into the nanopores of anodized aluminum oxide (AAO) films. The free-standing Pd nanowires were formed after removing the AAO template.

2.1.8 Laser Ablation

A method combining laser ablation cluster formation and VLS growth was developed for the synthesis of semiconductor nanowires[27]. In this process, laser ablation was used to prepare nanometer diameter catalyst clusters that define the size of wires produced by VLS growth. This approach was used to prepare bulk quantities of uniform single-crystal Si and Ge nanowires with diameters of 6 to 20 and 3 to 9 nm, respectively, and lengths ranging from 1 to 30 micrometers. The schematics are shown in Figure 2.5. In the Laser ablation technique, (1) Laser ablation with photons of energy hν of the SiFe target creates a dense, hot vapor of Si and Fe species. (2) The hot vapor condenses into small clusters as the Si and Fe species cool through collisions with the buffer gas. The furnace temperature is controlled to maintain the Si-Fe nanocluster in a liquid state. (3) Nanowire growth begins after the liquid becomes supersaturated in Si and continues as long as the Si-Fe nanoclusters remain in a liquid state and Si reactant is available. (d) Growth terminates when the nanowire passes out of the hot reaction zone onto the cold finger and the Si-Fe nanoclusters solidify.

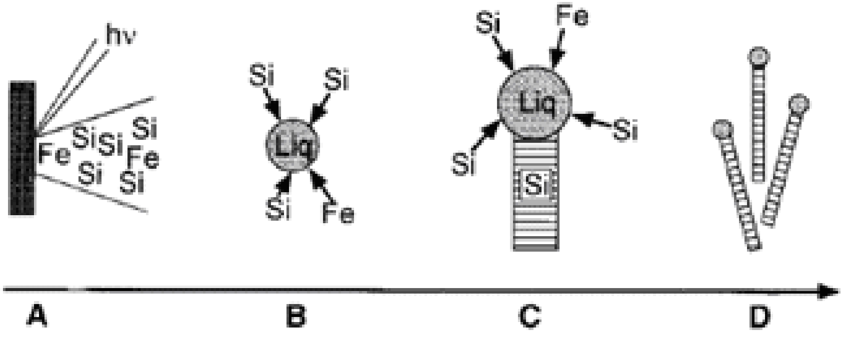

Fig 2.5 The mechanisms of the laser ablation formation technique. (Ref. 27)

The side-wall spacer technique is the cheapest and easier controlled technique to fabricate the nanowires. In the following, we would use the cheapest technique side-wall spacer to fabricate the Poly-Si/SiGe nanowire and discuss the drive current and sensitivity enhancement of Poly/SiGe nanowire with different Ge concentrations.

2.2 Experiment

The side-wall spacer formation is an easy process for nanowire fabrication with the advantages of high-yield and low-cost. The method only using the combination of the conventional lithography and processes technology was demonstrated without complex processes such as EBL, SPL and VLS etc. In the beginning, a p-type (100)-oriented bare silicon wafer with 1-10Ω-cm resistivity was prepared.

1. After standard RCA cleaning, 980℃ Wet Oxidation was performed for 1 hours to grow the bottom oxide as an insulator oxide by ASM/LB45 Furnace system. The thickness of the oxide is 3000Å which was shown in Figure 2.6.
2. Mask #1: Define the active area. We etched the oxide 1000 - 1500 Å by dry oxide etcher (TEL 5000) after Mask I defined. Then, a 1500 - 2000 Å oxide step was formed shown in Figure 2.7.
3. Following standard RCA clean, we deposited 150Å amorphous Si film on bottom oxide in the condition of 650℃ and 160 mTorr. The process increased adhesion between SiGe film and SiO2 layer shown in Figure 2.8.
4. Then, 500-1000 Å SiGe films with different Ge concentrations were deposited with the ultra-high-vacuum chemical vapor deposition (ANELAVA SiGe UHV-CVD) at 650℃. Also, the 800 Å poly-Si film was deposited, too. The structure is shown in Figure 2.9.
5. We defined the S/D contact regions with Mask II, and etched the whole height of the SiGe film (20% over etched) and the poly-Si film (20% over etched) by TCP

poly etcher in the follows. Only the S/D and SiGe/poly-Si deposited in the sidewall spacer were stayed. The residual SiGe film is what we want – SiGe nanowire. The structure is shown in Figure 2.10.

6. Next, we etched each pair of the parallel SiGe NW by TCP poly etcher after Mask III was defined. Thus, the poly-Si/SiGe nanowires were isolated. The structure is shown in Figure 2.11.
7. Finally, the aluminum was then deposited with a thickness of 5000 Å by thermal coater. Mask IV was used to reserve the S/D region, and then 400°C sintering 30 min was done shown in Figure 2.12.
8. Al sintering at 430°C in N_2 ambient for 25 minutes.

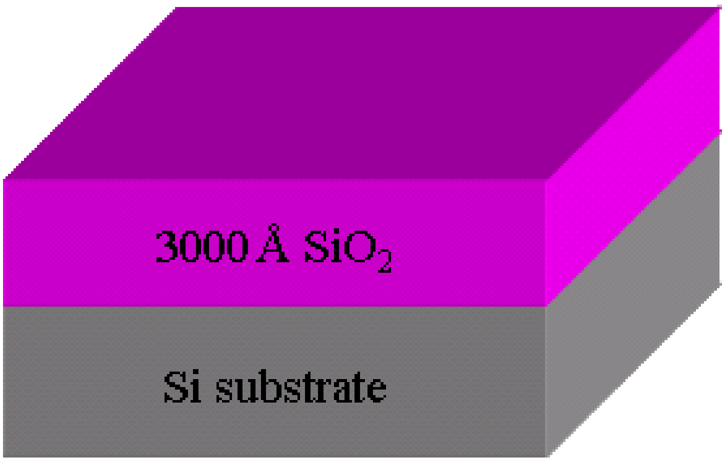

Figure 2.6 3000Å SiO_2 layer was grown on Si substrate.

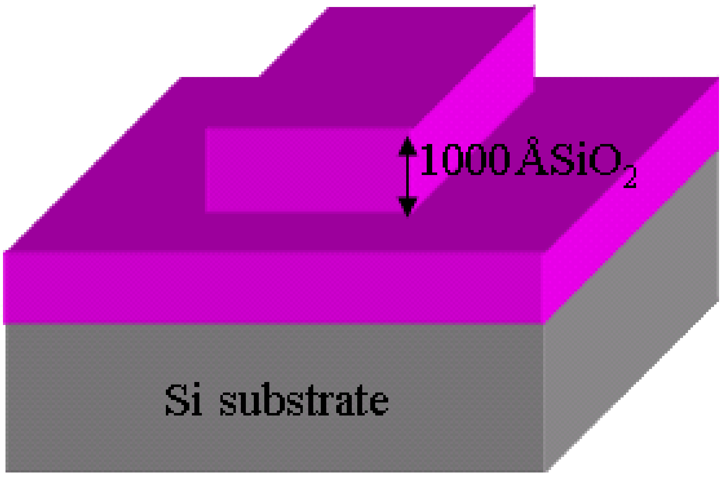

Figure 2.7 Definition of the active area. The height of oxide step is 1000Å

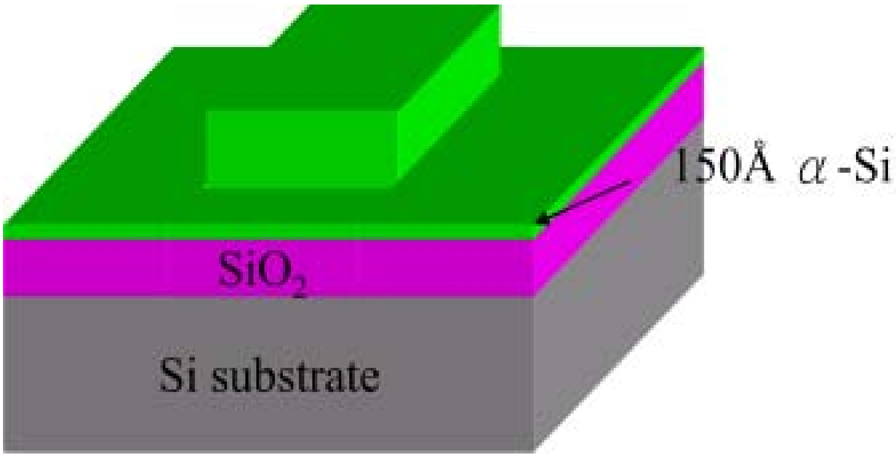

Figure 2.8 150Å Amorphous Si layer is deposited on SiO_2 layer.

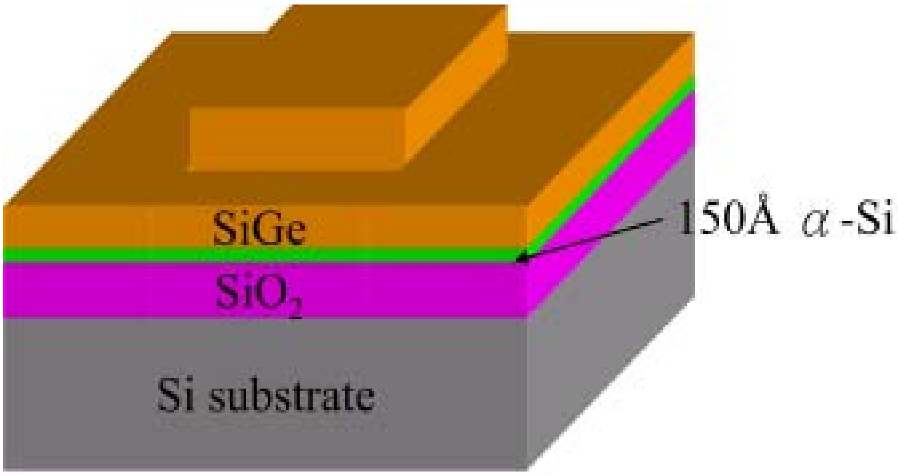

Figure 2.9 SiGe films with different Ge concentration were deposited on α-Si layer.

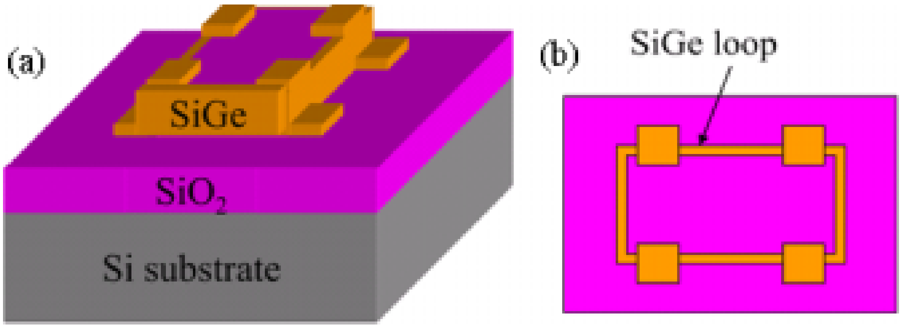

Figure 2.10 The definition of the S/D region and nanowire. (a) The 3-D view (b) The top view

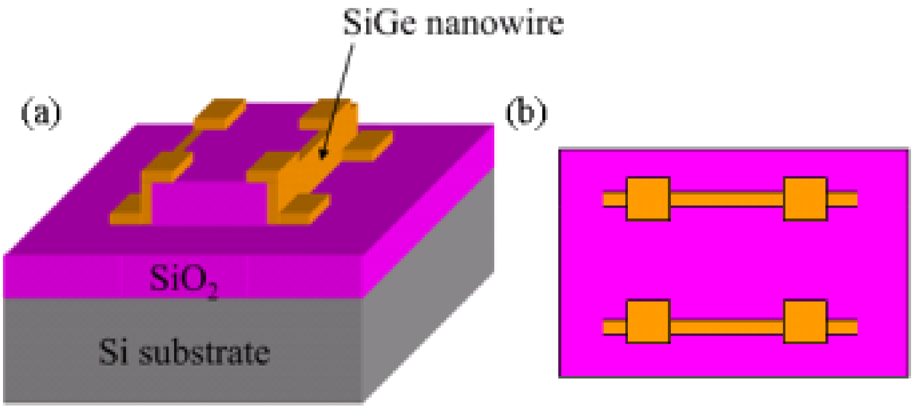

Figure 2.11 Remove one side of the parallel SiGe spacer to cut off the leakage current (a) The 3-D view (b) The top view.

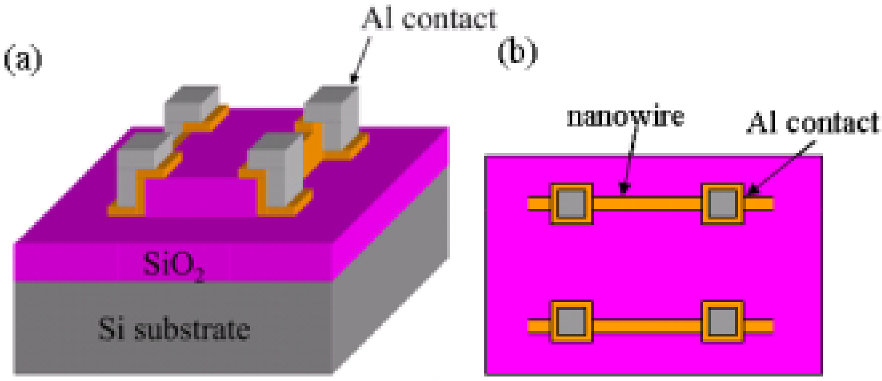

Figure 2.12 Defined Al contact pad. (a) The 3-D view (b) The top view.

2.3 The Dimension of Nanowires

The dimension of nanowire was controlled by the deposition for the width and the step of oxide for the height. In order to etch the poly-Si or SiGe film clearly, we added the 20% over-etching at the step of dry etching. The dimensions of poly-Si nanowires and SiGe nanowires with different Ge concentrations were observed by Scanning Electron Microscope (SEM) after dry etching, which is shown in Figure 2.13 (a) and (b) show the poly-Si nanowire with 174 nm in height and 76.9 nm in width, (c) shows the poly-Si$_{0.93}$Ge$_{0.07}$ nanowire with 280 nm in height and 108 nm in width, and (d) shows the poly-$Si_{0.89}Ge_{0.11}$ nanowire with 86 nm in height and 44 nm in width respectively.

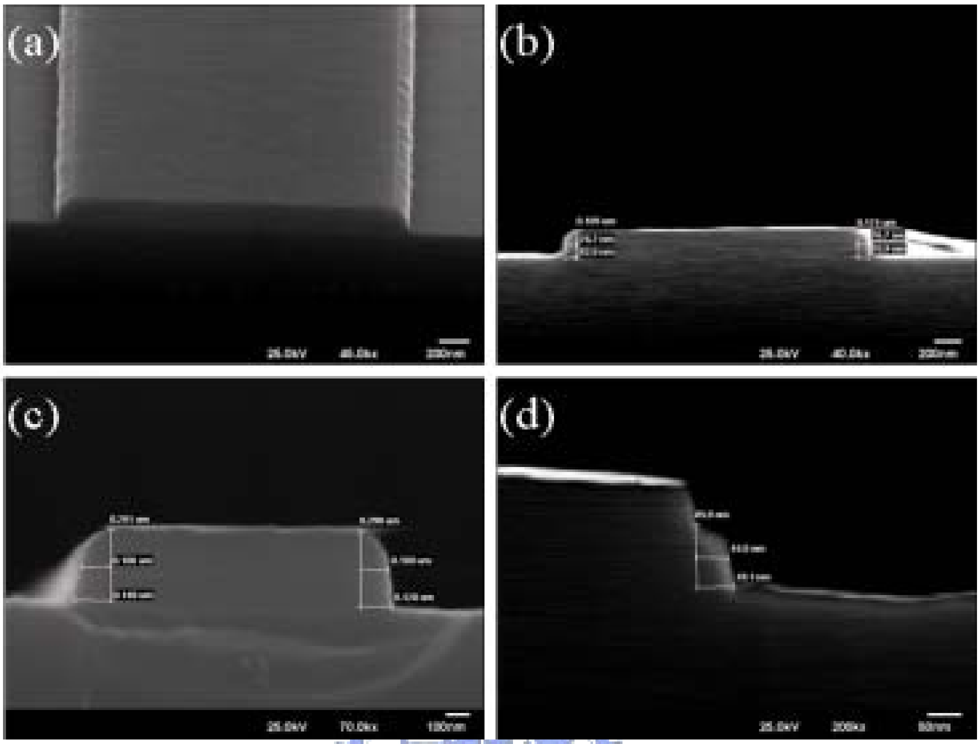

Figure 2.13 (a) The top view of poly-Si nanowire. (b) The cross-section view of poly-Si nanowire with 174 nm in height (H) and 76.9 nm in width (W). (c) The $Si_{0.93}Ge_{0.07}$ nanowire with H = 280 nm and W = 108 nm. (d) The $Si_{0.89}Ge_{011}$ nanowire with H = 86 nm and W = 44 nm.

2.4 Results and Discussions

The electrical properties of poly-Si/SiGe nanowires were measured by an Agilent 4156C semiconductor parametric analyzer. We swept the I_D-V_D from –5 V to 5 V, and changed the bottom gate V_G = –10 V, –5 V, 0V, 5V and 10V, respectively. In order to make sure that the measured current came from the nanowire, we made a test structure which the diagram is shown in Figure 2.14 (b). The current measured between the two 3 um distance isolated pads without nanowire is few pA which shows in Figure 2.14 (a). The I_D-V_D curve of Poly-Si nanowire with 15 um in length is shown in Figure 2.14 (c) by different bottom gate voltages applied. It is observed that the undoped poly-Si nanowires show the property of p-type like. The drive current increased as the bottom gate applied negative voltage, however, the drive current decreased as the bottom gate applied positive voltage. The result could be the surface charge. The same phenomenon was also found in SiGe nanowires, too. The I_D-V_D curve of $Si_{0.93}Ge_{0.07}$ nanowire with 15 um in length is shown in Figure 2.14 (d). The I_D-V_D curve of $Si_{0.89}Ge_{0.11}$ nanowire with 15 um in length is shown in Figure 2.14 (e). Because of the drive current higher than the leakage current (2 pA), we could make sure that what we measured were all the drive currents. For comparing the current in different sizes of nanowire, we considered the nanowire as a resistance. Let us consider the following equation (1).σ is the conductor, I is the current, L is the length, V is the applied voltage and A is the area of nanowire. Thus, we should normalize the length and area of the different nanowires by multiplying the L and dividing the A. The normalized current with bottom gate applied –15V is shown in Figure 2.15 (f). The higher drive current is achieved for SiGe nanowire instead of Poly-Si nanowire. Also, the drive current increased as the Ge concentration increased. It is useful for detecting the molecular on the nanowire.

$$\sigma = \Delta I \cdot (L / \Delta V \cdot A) \qquad (1)$$

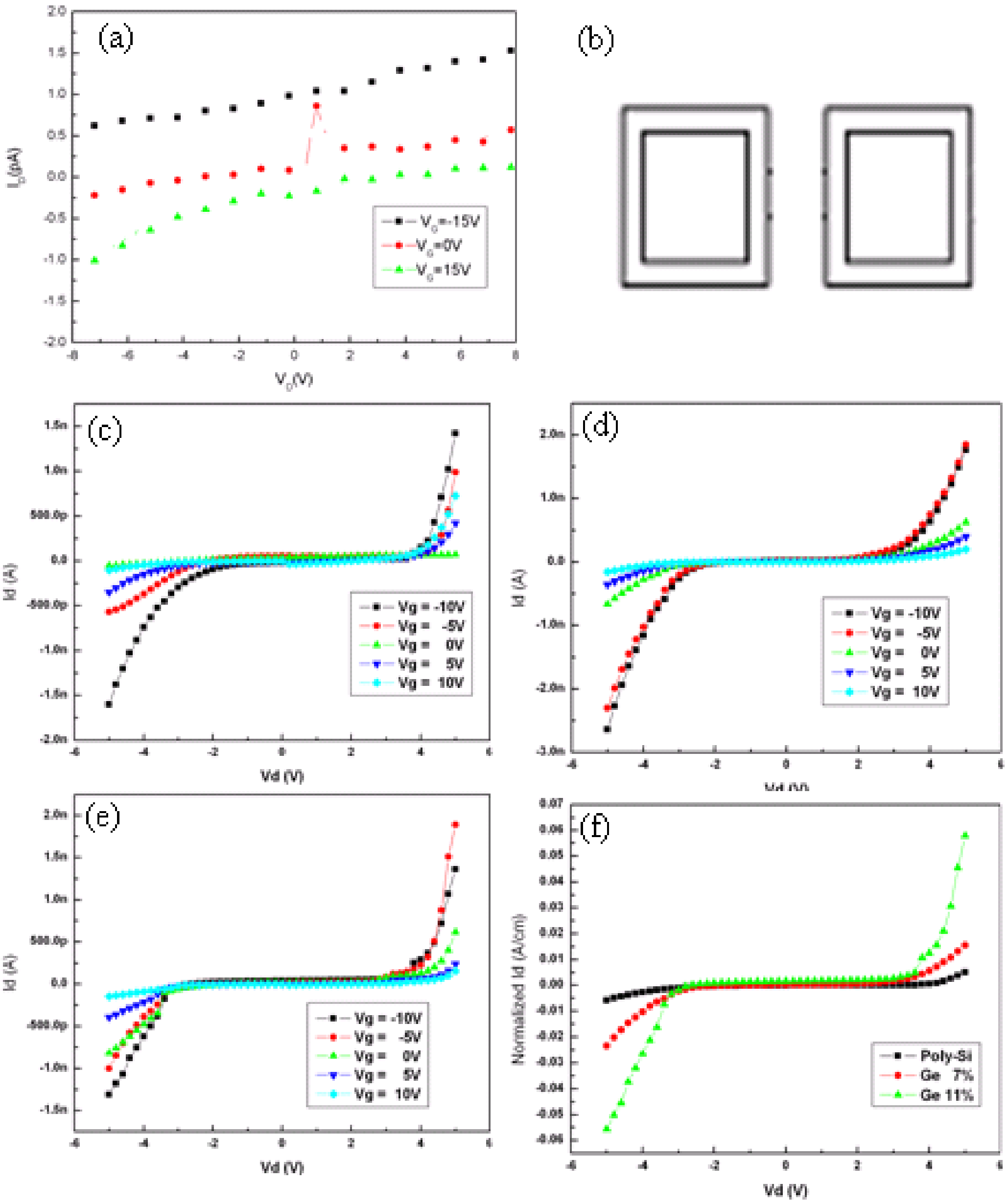

Figure 2.14 (a) The leakage current of the isolated pad without nanowire. The current is about 2 pA. (b) The diagram for leakage current test structure. (c) The drive current of Poly-Si nanowire with 15 um in length. (d) The current of $Si_{0.93}Ge_{0.07}$ nanowire with 15 um in length. (e) The current of $Si_{0.89}Ge_{0.11}$ nanowire with 15 um in length. (f) The normalized current of Poly-Si and SiGe nanowires. The higher drive current is obtained by SiGe nanowire with higher Ge concentration.

In the follows, we discuss the influence of implantation. Two conditions are considered. The first one is only the Source/Drain implanted. The PR was used for hard mask to stop the channel be implanted. Boron was doped with doses $5x10^{15}$ cm^{-2} at energy 10 keV. Activation annealing at 950℃ in N_2 flow was then employed for 30 minutes after PR stripped. The diagram is shown in insert of Figure 2.15 (c).

The I_D-V_D curve of $Si_{0.89}Ge_{0.11}$ nanowire with 5 um in length is shown in Figure 2.15 (a) by different bottom gate voltages applied. It is observed that the undoped poly-Si nanowires show the property of p-type like, too. The same phenomenon was also found in Poly nanowires. The I_D-V_D curve of Poly-Si nanowire with 5 um in length is shown in Figure 2.15(b). For comparing the current of Poly-Si and SiGe nanowires, we normalized the current by the same way. The higher current was found in SiGe nanowire instead of Poly-Si nanowire shown in Figure 2.15 (c).

The second condition: both source/Drain and nanowire channel were implanted by Boron with doses $5x10^{15}$ cm^{-2} at energy 10 keV. Activation annealing at 950℃ in N_2 flow was then employed for 30 minutes after ion implantation. The diagram is shown in the insert of Figure 2.15 (f). Figure 2.15 (d) and Figure 2.15 (e) show the current of $Si_{0.07}Ge_{0.11}$ nanowire and Poly silicon nanowire with 15 um in length. Both the current of SiGe and Poly-Si nanowire increased to the level of uA. The normalized current is shown in Figure 2.15 (f). The higher drive current is also achieved for SiGe nanowire.

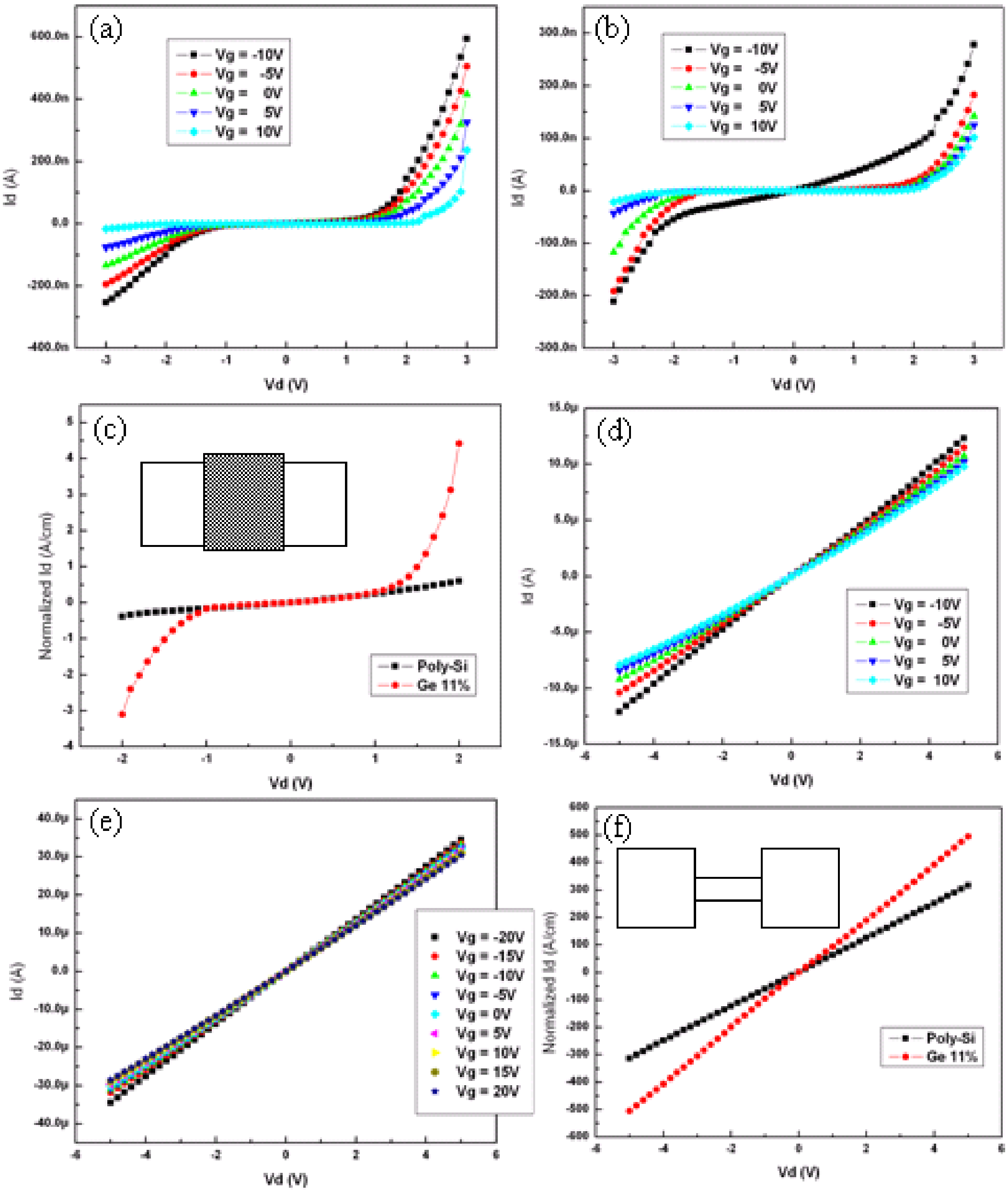

Figure 2.15 (a) and (b) shows the drive current of $Si_{0.89}Ge_{0.11}$ and Poly-Si nanowire with 5 um in length after S/D implant. (c) The normalized current of Poly-Si and $Si_{0.89}Ge_{0.11}$ nanowires after Source/Drain implanted. The insert picture is the diagram of nanowire with PR covered. (d) and (e) shows the drive current of $Si_{0.89}Ge_{0.11}$ and Poly-Si nanowire with 15 um in length after S/D and channel implant. (e) The normalized current of Poly-Si and $Si_{0.89}Ge_{0.11}$ nanowires after Source/Drain and channel implanted. The insert is the diagram of nanowire without PR covered.

The serial test structure was used to know the contact resistance between aluminum and the SiGe/Poly-Si pads, which diagram is shown in the insert of Figure 2.16 (a). The micro wire with 5 um in length and 5 um in width is connected to each pad, and the pad dimension is 100 um x 100 um. The Boron implantation and activation annealing were the same as the conditions above. We measured the current for one block distance to eleven block distance, and calculated the resistance of them (voltage divide current). After plotting the resistance v.s. the block distance shown in Figure 2.16 (a), then the linear fit line is calculated on it. The intersection of the y-axial and fit line was the resistance without any micro wire, which meant the contact resistance between the aluminum and Poly-Si pads. The clearly view is shown in Figure 2.16 (b). The same process was used to measure the contact resistance of Al/Si$_{0.89}$Ge$_{0.01}$ shown in Figure (c) and (d). The contact resistance is 31.702 Ω for Poly-Si, and the contact resistance is 71.57 Ω for Si$_{0.89}$Ge$_{0.11}$. However, the resistance of Poly-Si with 11 pad distance is 31 kΩ which is higher than the resistance of SiGe (22.7 kΩ). The lower wire resistance and higher contact resistance of SiGe were observed in the experiment.

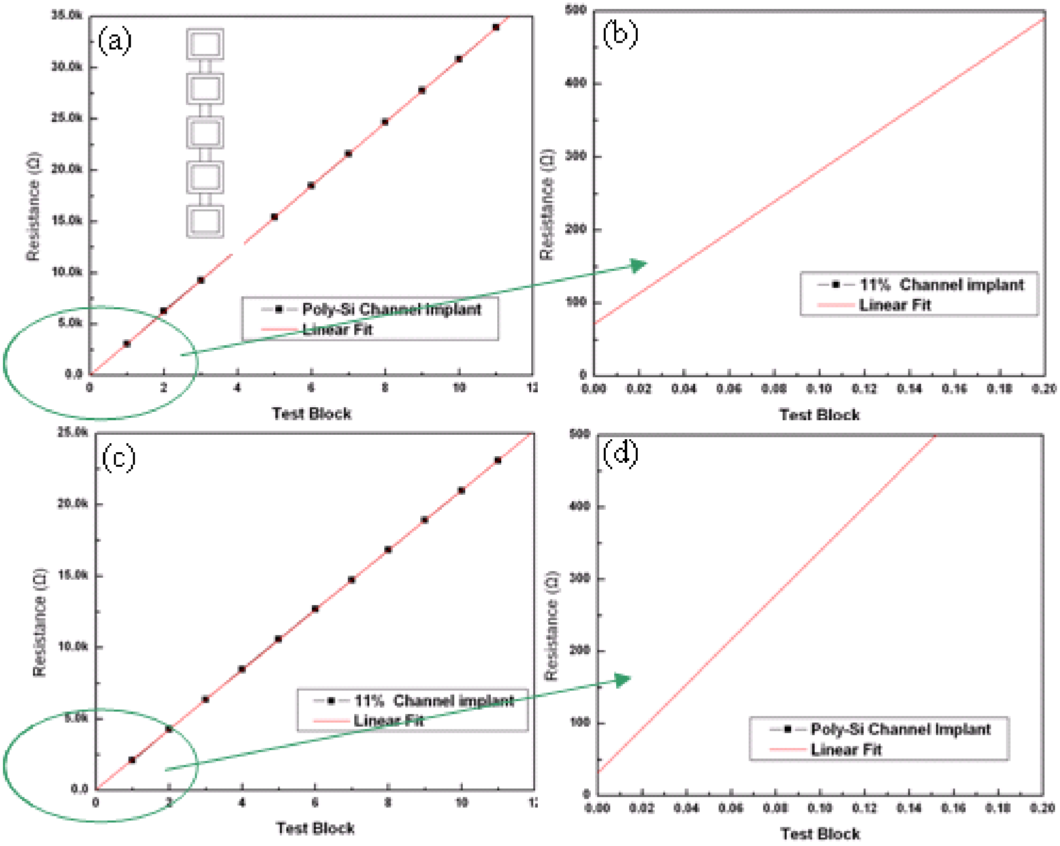

Figure 2.16 (a) and (b) show the resistance V.S. the contact pads of Poly-Si/Al. (c) and (d) show the resistance v.s. the contact pads of $Si_{0.89}Ge_{0.11}$/Al. The intersection of the y-axial and fitted line is the contact resistance between the aluminum and Poly-Si/SiGe pad.

2.5 Summary

The side-wall spacer Poly-Si/SiGe nanowires were successfully fabricated by the side-wall spacer technique on Si wafer. The SEM image is used to know the dimension of nanowire. In order to normalize the drive current of nanowires, we consider the nanowire as a resistor. The conductance is chosen for comparison between the nanowires. The higher drive achieved of SiGe nanowire instead of Poly-Si nanowire, and the higher current obtained for the SiGe nanowire with higher Ge concentration. The reason for less improvement of conductance after ion implantation may be that the implant dominates the current and decreases the influence of Ge element. However, the drive current of $Si_{0.89}Ge_{0.11}$ nanowire still has

50% improvement than Poly-Si nanowire after ion implantation. The test structure of serial contact pad with 5 um length micro wire was used to compare the contact resistance of SiGe and Poly-Si. The higher contact resistance and lower conductance are the properties of SiGe nanowire.

Chapter 3

Electrical Properties of SiGe Film with Various Oxidation Conditions

3.1 .1 An Overview of the Applications of High Mobility SiGe Alloy

As the channel length of metal-oxide-semiconductor field effect transistors (MOSFETs) is deeply scaled down to sub-100 nm, enhancement of the carrier mobility in the channel is desired for improving the performance of complementary MOS (CMOS) circuits[28]. For this purpose, Ge is a promising channel material for MOSFETs because of high mobility of both the electrons and holes. Enhanced device performances have been demonstrated by using a strained Si channel grown upon a relaxed (SiGe) substrate[29], where the electron mobility is increased due to the reduced intervalley phonon scattering[30]. However, at lower Ge content, only moderate increase in hole mobility could be achieved in strained Si compared to bulk Si[31]. On the other hand, with high Ge content (83%), SiGe channel high hole mobility enhancement in PMOSFETs can be realized[32]. To achieve the highest enhancement, pure Ge channel is attractive.

3.1.2 Ge Condensation Process in SiGe Film

Conventionally, relaxed Si$_{1-x}$Ge$_x$ film with high Ge content has been obtained by growing compositionally graded Si$_{1-x}$Ge$_x$ much thicker than the critical thickness in order to introduce dislocations to relax strain in Si$_{1-x}$Ge$_x$ layer[33]. Although the density of dislocations in the relaxed SiGe layer by this approach has been greatly reduced over time, the control of dislocations is still challenging and requires optimization for dislocation suppression. In addition, the thick Si$_{1-x}$Ge$_x$ films need for strain relaxation through dislocations (on the order of a few microns, with a typical grading rate of

10% germanium increment per micron) poses a serious bottleneck for throughput[34].

An approach to achieve high Ge content in relaxed $Si_{1-x}Ge_x$ layer has been reported that takes the advantage of the selective removal of Si atoms from SiGe film by $Si_{1-x}Ge_x$ thermal oxidation[35]. When supply of Si atoms diffused from the SiGe to the oxidation interface meets the consumption of Si atoms during oxidation, only Si atoms would be oxidized because Si oxidation is preferred to Ge oxidation[36], which leads to an increased Ge content in the $Si_{1-x}Ge_x$ layer as the film is thinned down.

3.1.3 Mechanism of SiGe Oxidation

The oxidation of SiGe thin films has been demonstrated at several laboratories[37-40]. In these cases, enough Ge on the oxidation of Si had to be snow-plowed in order for oxidation enhancement to be observed. They proposed that breaking of the weaker Si-Ge bound as compared with Si-Si explain the rate enhancement. This may only be the last event, not necessarily controlling. For example, represents a steady-state situation in which Si-Si bonds must still be broken below the Ge-enriched layer to supply the needed Si flux to the interface to maintain the high oxidation rates. Attention should be focused on the growth interface and interactions there since the Ge effect is found only in the initial and linear regime of oxidation. In all cases reported so far, it is shown that Si is preferentially oxidized and only one Ge-rich layer is formed at the oxide/substrate interface for SiGe with a Ge concentration below 50%. On the other hand, there are two oxide layers formed after oxidation for SiGe with Ge concentration above 50%.

According to the theory binary alloy oxidation[41-42], the oxide growth will depend on the alloy composition. For the case of the SiGe alloy, Si is more reactive than Ge. The reason is the large difference between the heat of formation of SiO_2 (-204 kcal/mol) and GeO_2 (-119 kcal/mol). For SiGe with low Ge concentration (< 50%), only silicon is oxidized initially. Ge is completed rejected from the oxide and piles up at the oxide/substrate interface. On the other hand, oxygen concentration at the oxidation front decreases with the oxide thickness increases. Then, the decreasing oxygen concentration at the oxidation front counteracts the effect of increasing Ge concentration in the Ge-rich SiGe layer so that Ge is not oxidized during the entire oxidation process.

For SiGe with high Ge concentration (> 50%), Si and Ge will be oxidized during the oxidation process. In alloys containing 50 and 75 at.% Ge, the rate of diffusion of Si to the oxide/alloy interface is sufficiently slow with respect to the rate of oxidation that it rapidly becomes impossible to grow pure SiO_2. Thus, the initial oxide formed is a mixed (Si, Ge)O_2 oxide. Eventually, the activity of oxygen at the interface decreases because of the thickness of the oxide, resulting in a slow down of the oxidation rate. This makes it possible for Si to diffuse to the interface as fast as is required to form pure SiO_2.

Eventually, oxide thickness will reach a critical value, which is proportional to the Ge concentration in SiGe film, such that the oxygen and Ge concentration at the oxide/SiGe interface are too low for Ge to be oxidized. At this stage a steady-state condition has been reached at which selective oxidation of Si succeeds and Ge piles up at the oxide/SiGe interface again. So that it is shown that Ge at the oxide/SiGe is in elemental form, while Ge at the oxide surface is in an intermediate oxidized form.

3.1.3 Oxidation Behavior of SiGe

The oxidation behavior of SiGe films has been studied to a great extent[43-45]. Ge is completed rejected from the oxide and piles up at the oxide/substrate interface after oxidation process. A Ge-on-insulator (GOI) was fabricated by Ge condensation technique in previous literature[46]. In addition, as the thickness of SiGe layer is smaller than diffusion length of the Ge atoms, the SiGe layer will become uniform, as show in Figure 3.1. The total amount of Ge atoms in the SGOI normalized by the value before oxidation is plotted as a function of oxidation time. It is found that the amount is kept constant during oxidation. This result enables an estimation of the final Ge fraction x_f based on the simple relationship $x_f = x_i\ (T_i/T_f\ )$. Here, x_i, T_i and T_f are the initial Ge fraction, and the initial and final SGOI thicknesses, respectively shown in Figure 3.2. The conservation of Ge atoms in the SGOI layers and the low Ge concentration in the oxide layer indicate that the SiGe oxide layer rejected the Ge atoms which remained in the SGOI layer.

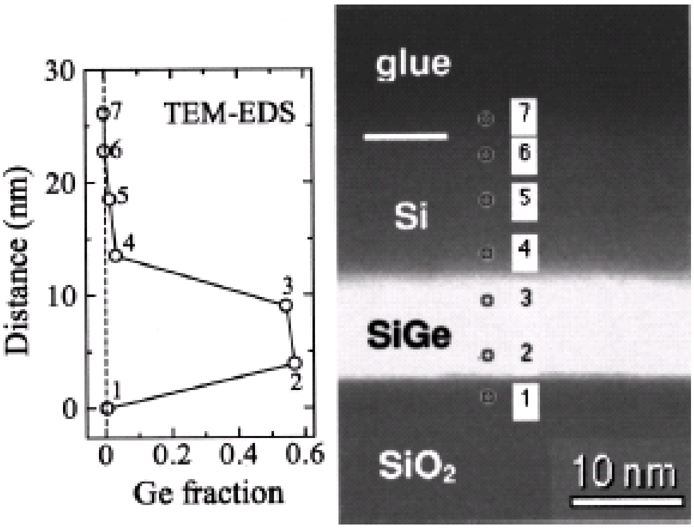

Figure 3.1 Scanning TEM image and Ge profile across the layers Obtained by EDS measurement. (Ref. 43)

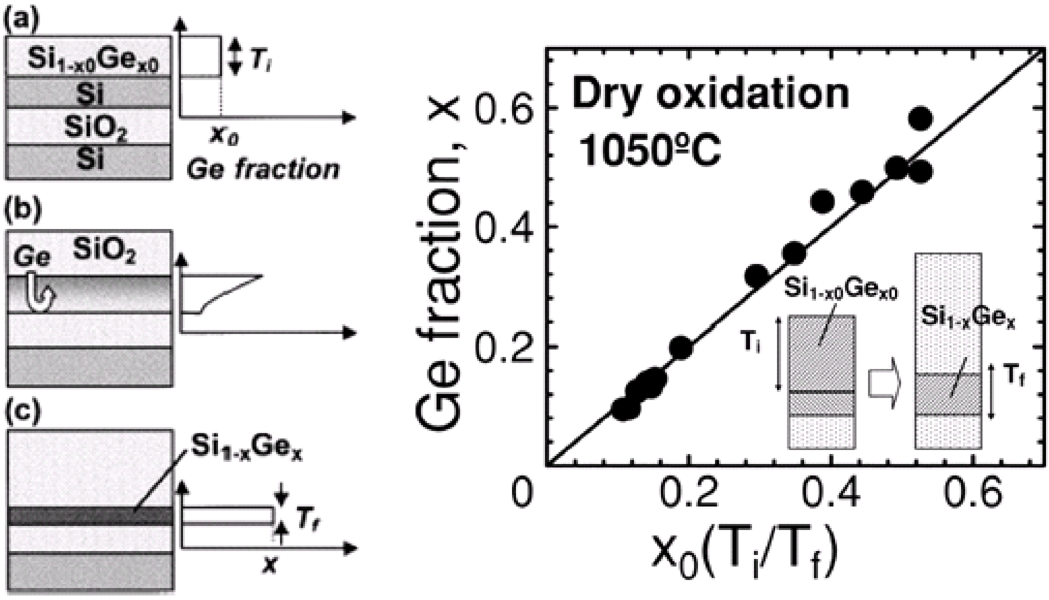

Figure 3.2 The Ge fractions after dry oxidation. (Ref. 43)

After the oxidation process, the dislocation density significantly decreases, as show in Figure 3.3. This decrease is attributed to the high temperature annealing, lead to the rearrangement of the lattice.

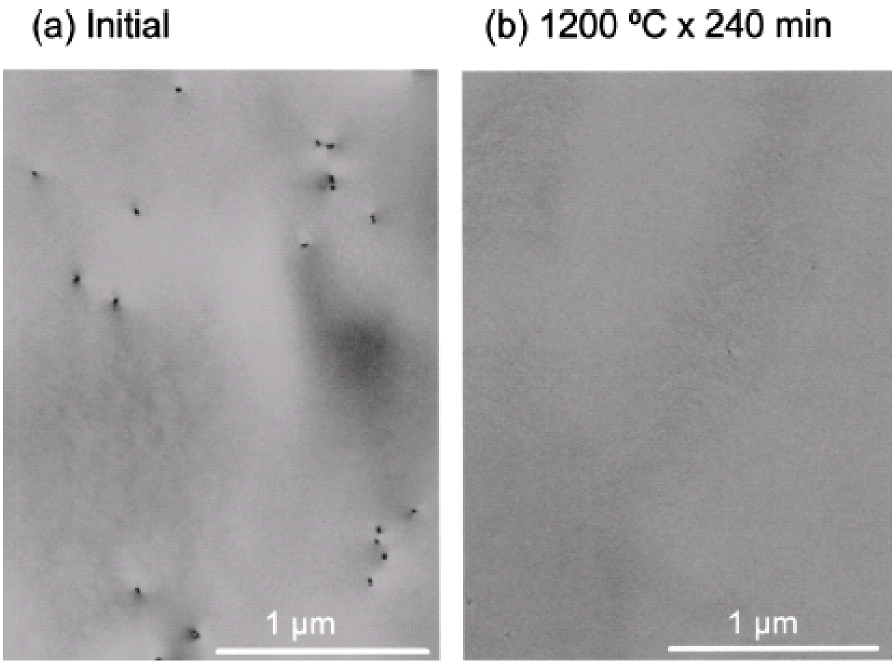

Figure 3.3 Plane-view TEM observations (a) before and (b) after oxidation at the temperature of 1200 °C. (Ref. 44)

3.1.5 Motivation

SiGe oxidation is widely used in either SiGe/Si hetro-junction devices, poly-SiGe gated MOSs, or SiGe channel devices. However, the optimal oxidation condition is not known yet. In this study, we adopt different oxidation temperature, oxidation time, oxygen flow, and oxidation rate and investigate the influence on the electrical characteristics of SiGe-based p-MOSFETs.

3.2 The Process Flow of SiGe-Based P-MOSFET

P-type (Boron doped) Si substrate (100)-oriented with 1-10Ω-cm resistivity was used in this study. After initial RCA cleaning, 3000Å oxide was thermally grown at 980℃ by a horizontal furnace through wet oxidation, served as an isolation layer. After one more time RCA cleaning, a 150Å thick amorphous-Si was deposited by LPCVD at 550℃, as a buffer layer between SiO_2 and SiGe film. SiGe (Ge content at 7% and 11%) film was then deposited onto amorphous-Si layer about 800 Å by UHV-CVD, shown in Figure 3.4 (a).

By means of photolithography, the active region could be defined after photo-resist was removed. After S-D and channel patterning, TCP poly etcher was employed for SiGe etching by Cl_2 and HBr. Later, the main part of this study proceeds by oxidizing the remaining SiGe part through different temperatures and times (top view shown in Figure 3.4 (b)). Oxidation parameters like temperature, time, and oxygen flow were tried in order to find out the optimum oxidation condition of SiGe channel. Moreover, pre-deposited-oxide before oxidation, oxidation rate controlling, and annealing after oxidation were also performed trying to make better electrical characteristics performance of SiGe-based p-TFT possible. All experimental factors are listed in Table 3.1 to Table 3.6.

Next, devices were dipped in BOE solution to remove surface SiO2 formed during oxidation of SiGe film. After 1000Å SiO_2 deposited by PECVD served as gate dielectic, 600°C annealing with O_2 was performed to cure the defects in gate oxide. Then, 2000Å poly-Si was deposited by LPCVD to work as control gate, shown in Figure 3.4 (c). After gate region and channel length defined by lithography, poly-etcher and BOE solution were used for etching. Top view is shown in Figure 3.5 (d). Then, Boron was doped heavily with 5x1015 cm-2 at 10 keV. Activation annealing at 950°C in N_2 flow was then employed for 30 minutes after ion implantation.

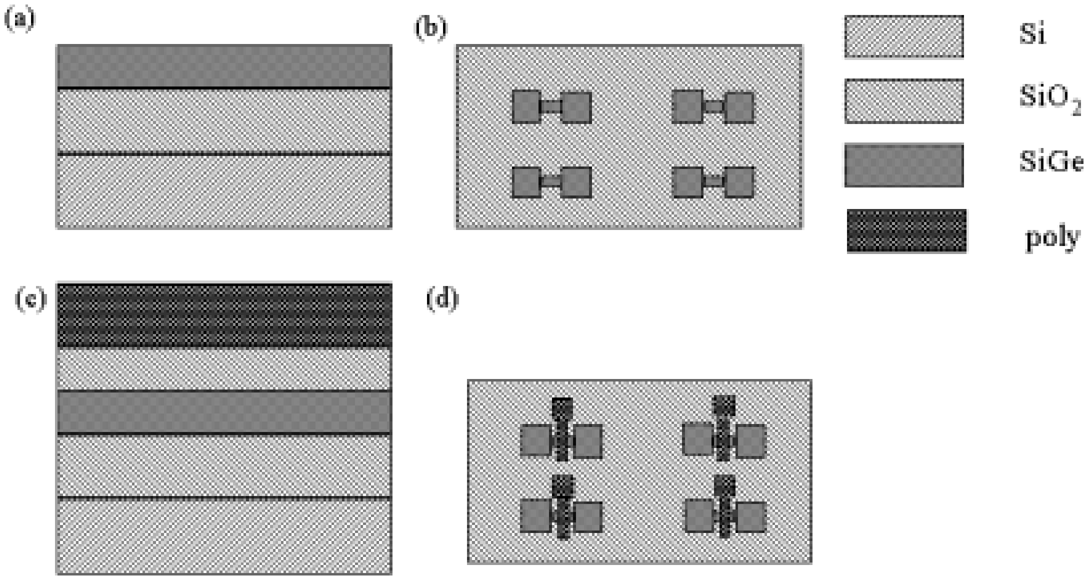

Figure 3.4 (a) The stack of $SiGe/SiO_2/Si$. (b) Top view of SiGe-S/D and channel pattern. (c) The PE gate oxide and Poly gate were deposited. (d) Poly gate pattern.

3000Å SiO2 by PECVD was deposited as passivation layer. Lithography comes next to form contact holes. SiO_2 was then etched by BOE solution for about 55 seconds. Finally, a 500 nm Al film was deposited by evaporation and then contact pads were patterned. Al sintering was performed at 430°C for 30minutes.The detailed fabrication process flow is as follows:

1. (100) P^+ Si wafer

2. RCA cleaning
3. Wet oxidation at 980^{o}C for 3000Å
4. RCA cleaning
5. 150Å amorphous-Si by LPCVD
6. RCA cleaning
7. 800Å SiGe(Ge content at 7% and 11%) by UHVCVD
8. Mask #1:Define active region
9. Dry etching by TCP poly etcher
10. PR removing and RCA cleaning
11. SiGe dry oxidation
12. BOE dipped to remove SiO$_2$
13. RCA cleaning
14. PECVD SiO$_2$ 1000Å deposition
15. Gate oxide annealing at 600^{o} with O$_2$ for 1hr
16. LPCVD poly-Si 2000Å deposition
17. Mask #2:Define gate and channel length
18. Wet etching by poly-etcher solution for 90 seconds
19. Wet etching by BOE solution for 25 seconds
20. PR removing
21. Boron doping of 5x10^{15} cm^{-2} at 10 keV
22. Activation at 950^{o}C for 30 minutes
23. STD cleaning
24. PECVD SiO$_2$ 3000 angstrom deposition
25. Mask #3:Define contact hole
26. Wet etching by BOE solution for 50 seconds
27. PR removing

28. Al coating for 5000Å

29. Mask #4:Define contact pad

30. Al etching

31. PR removing

32. Sintering of Al at 430°C for 30 minutes

The cross-section view of p-type SiGe-thin-film-transistor is shown in Figure 3.5.

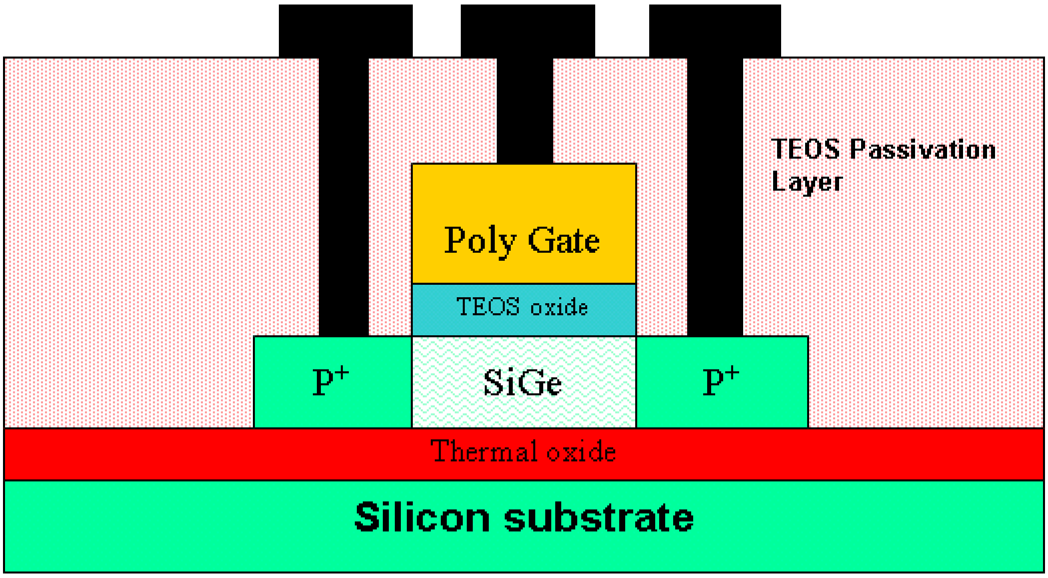

Figure 3.5 The cross-section view of p-type SiGe-thin-film-transistor.

Alloy concentration	Oxidation condition	Variable: Temperature
$Si_{0.89}Ge_{0.11}$	16 minutes 3750 sccm O_2 flow	1000 °C
		950 °C
		un-oxidized

Table 3.1 Influence of Oxidation Temperature Experiment

Alloy concentration	Oxidation condition	Variable: Time
$Si_{0.93}Ge_{0.07}$	1000 $^{\circ}$C 3750 sccm O_2 flow	36 minutes
		16 minutes
		4 minutes
		un-oxidized

Table 3.2 Influence of Oxidation Time Experiment

Alloy concentration	Oxidation condition	Variable: O_2 Flow
$Si_{0.89}Ge_{0.11}$	1000 $^{\circ}$C 16 minutes	3750 sccm
		2500 sccm
		un-oxidized

Table 3.3 Influence of Oxygen Flow Experiment

Alloy concentration	Oxidation condition	Variable: Thickness
$Si_{0.93}Ge_{0.07}$	1000 $^{\circ}$C 36 minutes 3750 sccm O_2 flow	1000Å
		500Å
		300Å
		no pre-oxide

Table 3.4 Influence of Thickness of Pre-Oxide Experiment

Alloy concentration	Oxidation condition	Variable: Rate
$Si_{0.93}Ge_{0.07}$	3750 sccm O_2 flow	950 $^{\circ}$C 15 minutes
		900 $^{\circ}$C 30 minutes
		850 $^{\circ}$C 75 minutes

Table 3.5 Influence of Oxidation Rate Experiment

Alloy concentration	Oxidation condition	Variable: Annealling
$Si_{0.93}Ge_{0.07}$	950 $^{\circ}$C 5 minutes 3750 sccm O_2 flow	6hrs anneal
		no annealing

Table 3.6 Influence of Annealing After Oxidation Experiment

3.3 Results and Discussions

Id-Vg and Id-Vd characteristics in these experiments were measured by HP4156A. In the following measurements of current, all devices were normalized to W/L = 1 µ/1 µ. In Id-Vg measurements, Vd was applied at (-5 V). While Id-Vd was measuring, |Vg-Vt| was set at 3V.

3.3.1 Influence of Oxidation Temperature on Electrical Properties

Figure 3.6 (a) shows Id-Vg characteristics of three different devices: un-oxidized, oxidation at 950℃, and oxidation at 1000℃. $Si_{0.89}Ge_{0.11}$ film was used in these experiments, and both of the oxidized devices were oxidized for 16 minutes with 3750 sccm O_2 flow. It can be seen that both oxidized devices show superior electrical performance than the un-oxidized one by higher On/Off ratio. The device of 1000 ℃-oxidized shows even higher on current than the one of 950 ℃-oxidized one while both devices have roughly the same off state current.

Figure 3.6 (b) shows Id-Vd characteristics which are consistent with the prediction: the device oxidized at 1000 ℃ has highest Id of the three devices – 2.58µA at Vd = (-6)V. 950 ℃- oxidized device has 1.83 µA, and the un-oxidized one has 0.40µA. It was known that since SiGe got oxidized, concentration of Ge would be increased, and then mobility would also get enhanced which resulted in a higher on state current, On/Off ratio gets improved then. With higher oxidation temperature, the rate of oxidation would be higher, which made more Si in SiGe film oxidized. Then the mobility would be even higher, and better performance was achieved.

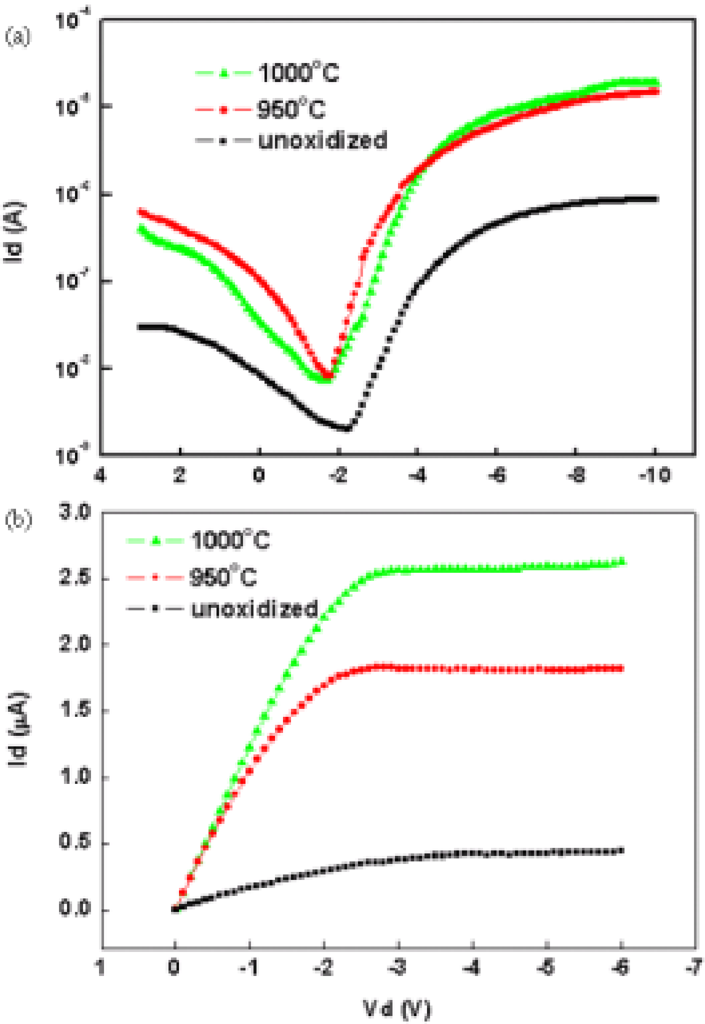

Figure 3.6 (a) Id-Vg characteristics of different oxidation temperatures. (b) Id-Vd characteristics.

3.3.2 Influence of Oxidation Time on Electrical Properties

Figure 3.7 (a) shows Id-Vg characteristics of four different devices: un-oxidized, oxidized for 4 minutes, oxidized for 16 minutes, and oxidized for 36 minutes, respectively. $Si_{0.93}Ge_{0.07}$ film was used in these experiments. All of the oxidized devices were oxidized at 1000°C with 3750 sccm O_2 flow. From the diagram, the trend of the curves indicates that longer oxidation time results in higher on state current. Besides, after calculation, the On/Off ratio of 36m-oxidized, 16m-oxidized, and 4m-oxidized is 3.3, 1.6, 1.5 times higher than that of the un-oxidized device, respectively. Due to the same reason as described previously, in the longer oxidation time devices, more amount of Si was oxidized and then higher Ge concentration was achieved. Figure 3.7 (b) depicts Id-Vd characteristics for devices with different oxidation times. As predicted, 36m-oxidized device has highest on current, which is 5.08μA at Vd = (-8)V. For the other devices, they are 1.52μA, 0.75μA, and 0.61μA for 16m-oxidized, 4m-oxidized, and un-oxidized devices, respectively.

It is presumed that unless Si in the SiGe layer is fully oxidized, the performance of the SiGe-based p-MOSFET would always be improved with the increasing of oxidation time since the positive correlation between the amount of oxidized Si and the mobility of SiGe channel.

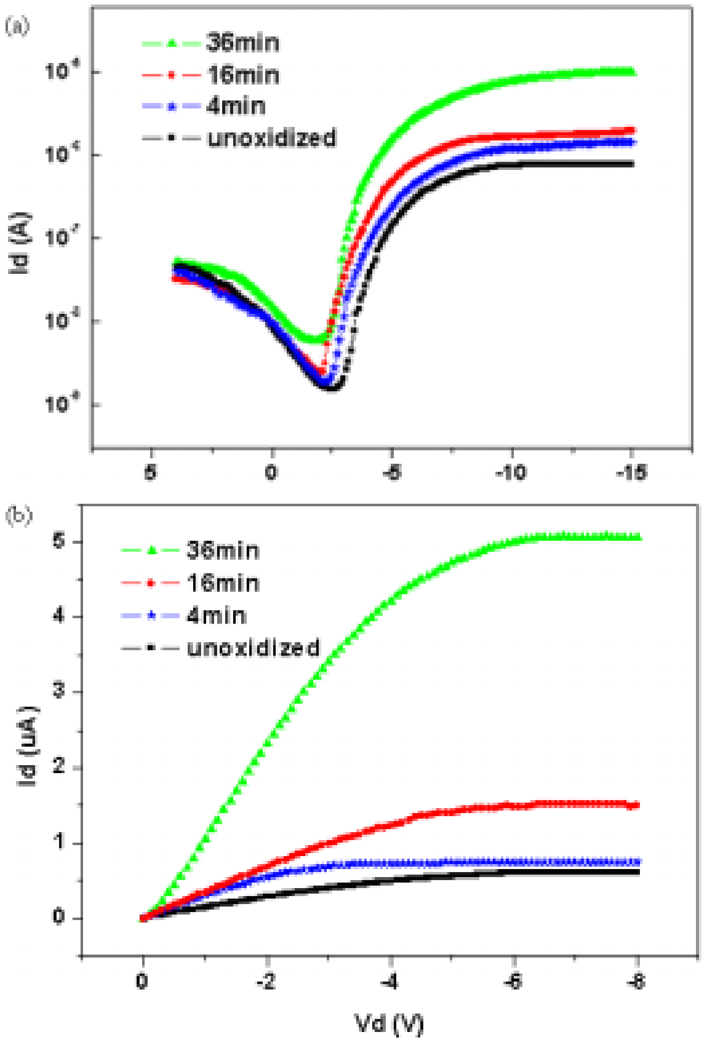

Figure 3.7 (a) Id-Vg characteristics after different oxidation times; the temperature is 1000℃ (b) Id-Vd characteristics.

3.3.3 Influence of Oxygen flow on Electrical Properties

$Si_{0.89}Ge_{0.11}$ film was used in this experiment. Devices were oxidized at 1000^{o}C for 16 minutes. Figure 3.8 (a) depicts Id-Vg characteristics of devices with different oxygen flows during oxidation: 3750 sccm, 2500 sccm, and un-oxidized. The device under larger oxygen flow shows larger on-state current and lower-off state current, which are undoubtedly better than the devices oxidized under 2500 sccm oxygen flow and the un-oxidized one. It is supposed to be contributed by more Si being oxidized, as discussed before. The On/Off ratios of 3750sccm-device and 2500sccm-device are 5.89 and 1.86 times higher than the un-oxidized one. As to Id-Vd characteristics, which is shown in Figure 3.8 (b), the device with 3750 sccm O_2 flow has 2.56μA at Vd = (-6)V. The devices with 2500 sccm O_2 flow and un-oxidized have 1.83μA and 0.43μA, respectively. From the experiments above, the amount of oxidized Si explains the improvement of electrical charateristic performance well. In the following study, several different oxidation conditions were applied, and some other results would be achieved.

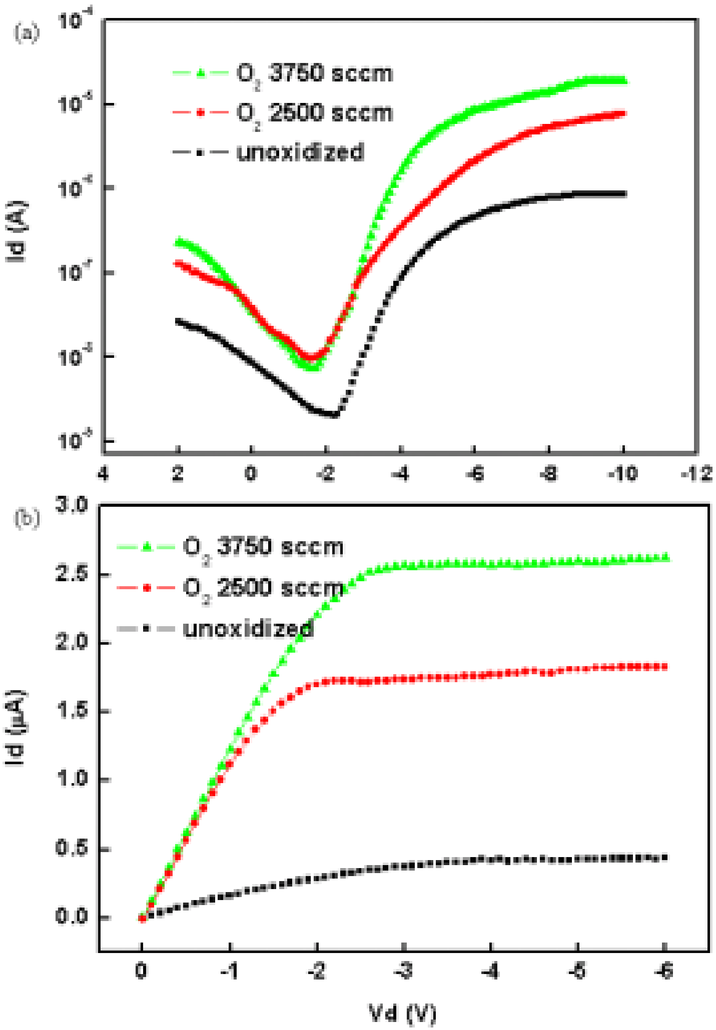

Figure 3.8 (a) Id-Vg characteristics after different oxygen flow rates at 1000℃ (b) Id-Vd characteristics.

3.3.4 Influence of the Thickness of Pre-oxide on Electrical Properties

As it is known that the oxidation rate would decreases with increasing the oxidation time, a new experiment is designed to investigate the influence of the initial oxidation rate on electrical performance of SiGe-based TFT. SiO_2 was deposited onto SiGe film first by PE-CVD just after UHV-CVD SiGe film deposited. The thicknesses of SiO_2 were 300Å, 500Å, and 1000Å, respectively, and a non-pre-oxide device was also fabricated. $Si_{0.93}Ge_{0.07}$ was used in this experiment and oxidation was performed at 1000°C for 36 minutes with 3750 sccm O_2 flow. Figure 3.9 (a) depicts Id-Vg characteristics of devices with different thickness of pre-oxide. The On/Off ratio is getting higher while the thicknesses of pre-oxide is getting larger, which is 2.6, 1.9, 1.7 times higher than that of non-pre-oxide device, respectively. But on the other hand, the on-state current decreases. It is presumed that less amount of Si in SiGe film would be oxidized owing to thicker pre-oxide existing that results in lower on current. As shown in Figure 3.9 (b), Id at Vd = (-8 V) of non-pre-oxide, 300 Å, 500 Å, and 1000 Å are 5.46μA, 2.79μA, 1.07μA, and 0.95μA, respectively. But there is still benefit from depositing pre-oxide. Since the oxidation rate was lowered by pre-oxide, the segregation Ge atoms would distribute evenly in SiGe channel, which lowers the off-state current, and results in a higher On/Off ratio.

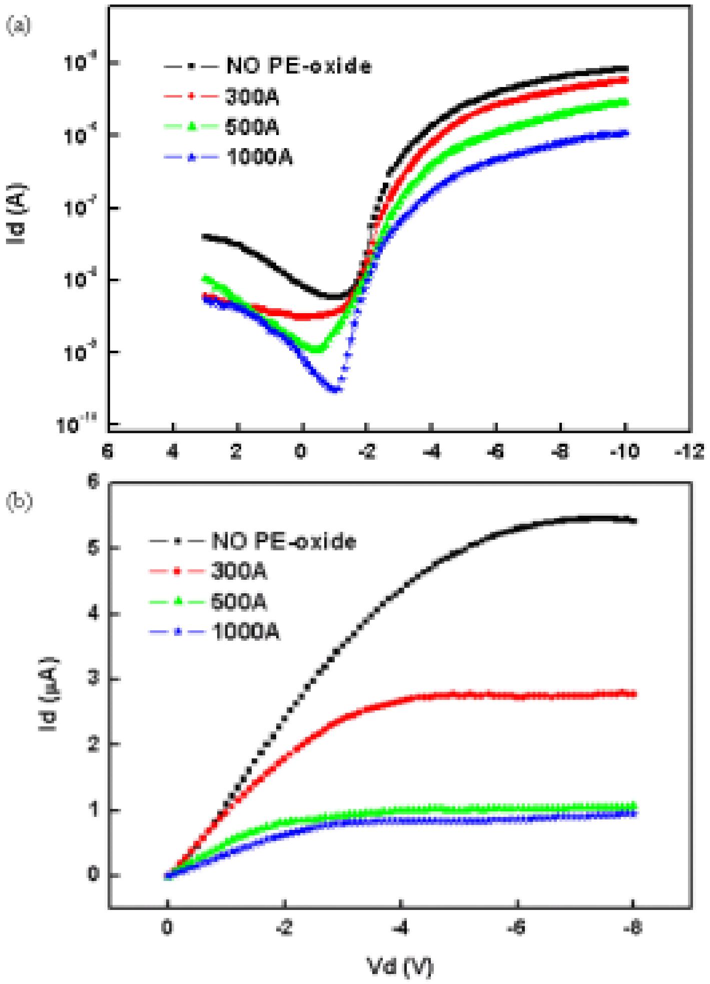

Figure 3.9 (a) Id-Vg characteristics with different thicknesses of pr-oxide deposited before oxidation ; the temperature is 1000℃ and the time is 36 min. (b) Id-Vd characteristics.

3.3.5 Influence of Oxidation Rate on Electrical Properties

In the previous study, it is concluded that under lower oxidation rate, SiGe-based p-TFT would achieve better On/Off ratio performance. However, the amount of oxidized Si in last experiment was still a variable. The factor of the amount of oxidized Si was removed by a new designed method. Several oxidation conditions were performed first and the thickness of SiO_2 was measured. Three oxidation conditions of roughly the same thickness of SiO_2 were selected. They are 950°C 15 minutes, 900°C 30 minutes, and 850°C 75 minutes, respectively, which indicate the same amount of Si oxidized. $Si_{0.93}Ge_{0.07}$ was used in this experiment and oxidation was performed with 3750 sccm O_2 flow. Figure 3.10 (a) depicts Id-Vg characteristics at Vd = -5 V. On-state current of the three devices almost equals, but the device with lower oxidation rate has lower off-state current, which supports our conclusion from the previous study. In Figure 3.10 (b), it is shown that the on-state current of the three devices are also almost the same at about 2.1 ~ 2.3 μA. As predicted, same amount of oxidized Si results in same Id. Slow oxidation rate makes Ge atoms distribute evenly and then makes lower off-state current which achieves a higher On/Off ratio.

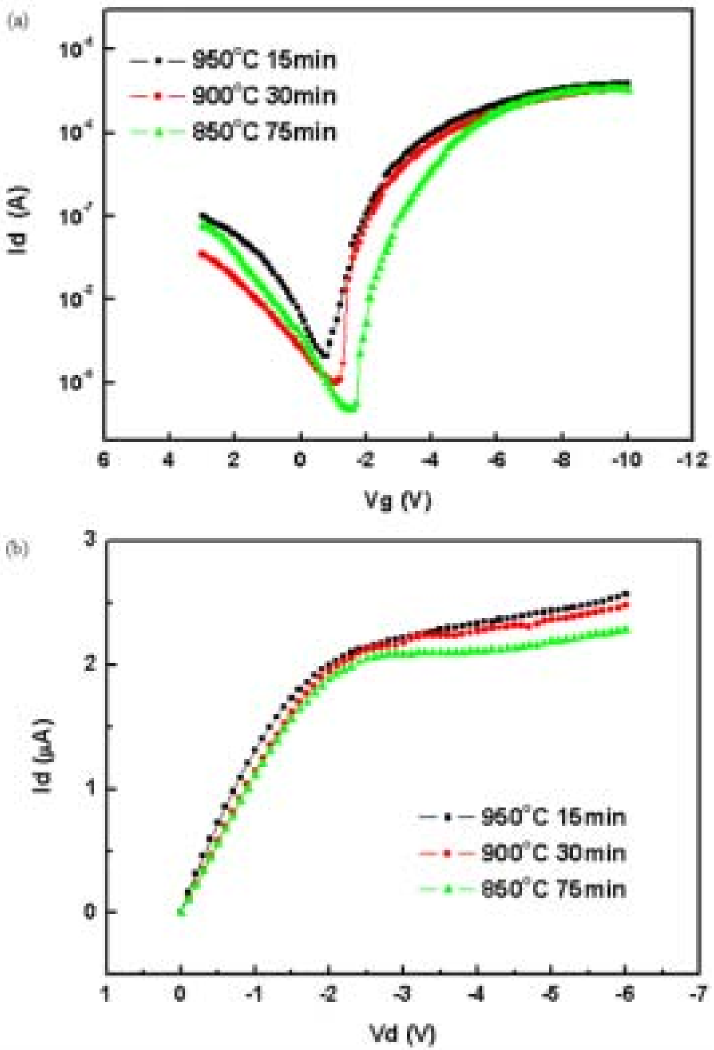

Figure 3.10 (a) Id-Vg characteristics of different oxidation rates. (b) Id-Vd characteristics.

3.3.6 Influence of Annealing after Oxidation on Electrical Properties

In the final section, annealing was performed after SiGe film oxidation. $Si_{0.93}Ge_{0.07}$ was used in this experiment and oxidation was performed at 950°C for 5 minutes with 3750 sccm O_2 flow. Device was annealed for 6 hours after oxidation, and a non-annealing device was also fabricated. Figure 3.11 (a) depicts Id-Vg characteristics at Vd = -5 V. The On/Off ratio of 6 hrs-annealing-device was slightly improved by 1.4 times than non-annealing device. In Figure 3.11 (b), Id-Vd characteristic diagram is shown. Nearly 80% Id improvement is achieved by annealing for 6 hours, which is 3.90μA, in comparion with 2.17μA of the non-annealing device. It is supposed that annealing at high temperature cures the defects in the SiGe channel, and facilitates evenly distribution of Ge in SiGe channel and thus improves the on-state current and the leakage current.

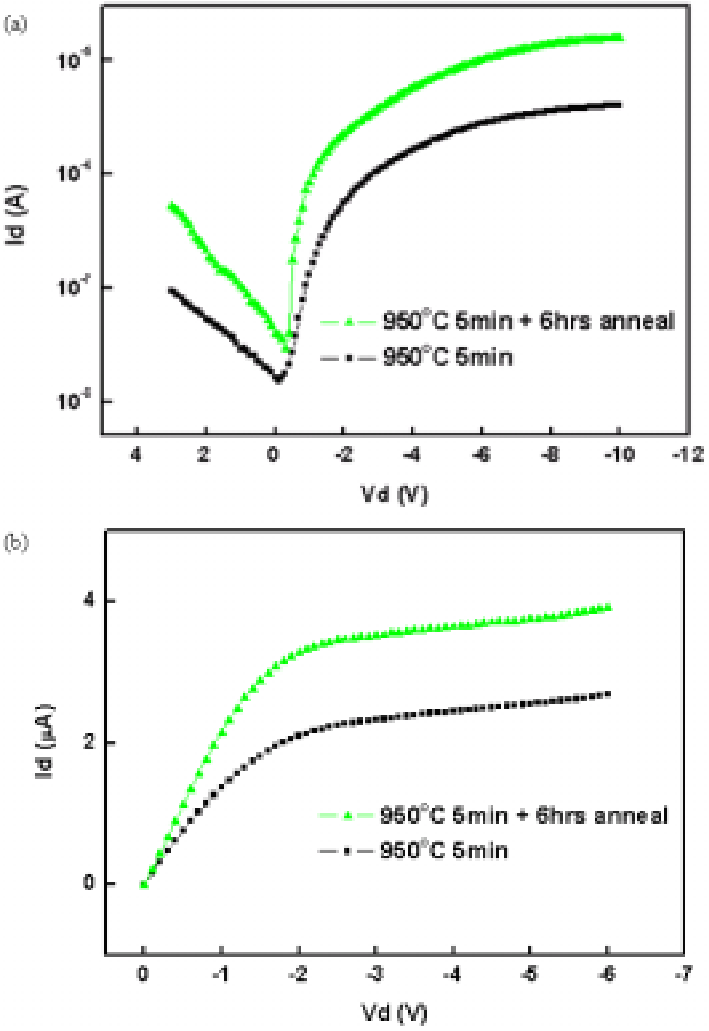

Figure 3.11 (a) Id-Vg characteristics of annealing applied. (b) Id-Vd characteristics.

3.4 Summary

It is found that all the electrical characteristics such as On/Off ratio, and on state current would get improvement after the SiGe channel was oxidized. This is because after oxidation, Si atoms in SiGe channel would be combined with O atoms to form SiO_2 while Ge atoms would be separated from that. The more amount of Si in the SiGe film was oxidized, the more Ge atoms would exist in the SiGe channel and then makes Ge concentration higher that results in higher hole mobility in SiGe-base p-TFT. With the amount of oxidized Si increasing, the hole mobility also increases and then better electrical performance would be achieved. Experiments of oxidation temperature, oxidation time, and oxygen flow already proved this phenomenon. Oxidation rate was also considered in our experiment. The results show that the devices under slower oxidation rate have lower leakage current and better On/Off ratio. It is conjectured that the separated Ge atoms would distribute evenly in the SiGe channel under slow oxidation process and then a high quality channel was formed. This is why the devices have lower leakage current. It is found that the device under annealing for 6 hours has higher on-state current, and On/Off ratio. It is presumed that high temperature would cure the defects in the channel, and thus improves electrical performance. The results will be applied into SiGe nano-wire for high performance SiGe nanowire.

Chapter 4

The Higher Current of SiGe Nanowire by Oxidation

4.1 Introduction

As the channel length of metal-oxide-semiconductor field effect transistors (MOSFETs) is deeply scaled down to sub-100 nm, enhancement of the carrier mobility in the channel is desired for improving the performance of complementary MOS (CMOS) circuits[28]. For this purpose, Ge is a promising channel material for MOSFETs because of high mobility of both the electrons and holes. Enhanced device performances have been demonstrated by using a strained Si channel grown upon a relaxed (SiGe) substrate[29], where the electron mobility is increased due to the reduced intervalley phonon scattering[30]. However, at lower Ge content, only moderate increase in hole mobility could be achieved in strained Si compared to bulk Si[31]. On the other hand, with high Ge content (83%), SiGe channel high hole mobility enhancement in PMOSFETs can be realized[32]. To achieve the highest enhancement, pure Ge channel is attractive.

The oxidation of SiGe thin films has been demonstrated at several laboratories[37-40]. In these cases, enough Ge on the oxidation of Si had to be snow-plowed in order for oxidation enhancement to be observed. They proposed that breaking of the weaker Si-Ge bound as compared with Si-Si explain the rate enhancement. This may only be the last event, not necessarily controlling. According to the theory binary alloy oxidation[41-42], the oxide growth will depend on the alloy composition. For the case of the SiGe alloy, Si is more reactive than Ge. The reason is the large difference between the heat of formation of SiO_2 (-204 kcal/mol) and GeO_2 (-119 kcal/mol). For SiGe with low Ge concentration ($< 50\%$), only silicon is oxidized initially. Ge is completed rejected from the oxide and piles up at the oxide/substrate interface. On the other hand, oxygen concentration at the oxidation front decreases with the oxide thickness increases. Then, the decreasing oxygen concentration at the oxidation front counteracts the effect of increasing Ge concentration in the Ge-rich SiGe layer so that Ge is not oxidized during the entire oxidation process. In this chapter we tried to fabricate a SiGe nanowire with higher drive current by Ge condensation technique.

4.2 Experiment

The side-wall spacer formation is an easy process for nanowire fabrication with the advantages of high-yield and low-cost. The method only using the combination of the conventional lithography and processes technology was demonstrated without complex processes such as EBL, SPL and VLS etc. In the beginning, a p-type (100)-oriented bare silicon wafer with 1-10Ω-cm resistivity was prepared.

9. After standard RCA cleaning, 980℃ Wet Oxidation was performed for 1 hours to grow the bottom oxide as an insulator oxide by ASM/LB45 Furnace system. The thickness of the oxide is 3000Å which was shown in Figure 4.1.
10. Mask #1: Define the active area. We etched the oxide 1000 - 1500 Å by dry oxide etcher (TEL 5000) after Mask I defined. Then, a 1500 - 2000 Å oxide step was formed shown in Figure 4.2.
11. Following standard RCA clean, we deposited 150Å amorphous Si film on bottom oxide in the condition of 650°C and 160 mTorr. The process increased adhesion between SiGe film and SiO2 layer shown in Figure 4.3.
12. Then, 500-1000 Å SiGe films with different Ge concentrations were deposited with the ultra-high-vacuum chemical vapor deposition (ANELAVA SiGe UHV-CVD) at 650°C. Also, the 800 Å poly-Si film was deposited, too. The structure is shown in Figure 4.4.
13. We defined the S/D contact regions with Mask II, and etched the whole height of

the SiGe film (20% over etched) and the poly-Si film (20% over etched) by TCP poly etcher in the follows. Only the S/D and SiGe/poly-Si deposited in the sidewall spacer were stayed. The residual SiGe film is what we want – SiGe nanowire. The structure is shown in Figure 4.5.

14. Next, we etched each pair of the parallel SiGe NW by TCP poly etcher after Mask III was defined. Thus, the poly-Si/SiGe nanowires were isolated. The structure is shown in Figure 4.6.
15. In the follows, oxidation was employed with various conditions.
16. Finally, the aluminum was then deposited with a thickness of 5000 Å by thermal coater. Mask IV was used to reserve the S/D region, and then 400℃ sintering 30 min was done shown in Figure 4.7.
17. Al sintering at 430℃ in N_2 ambient for 25 minutes.

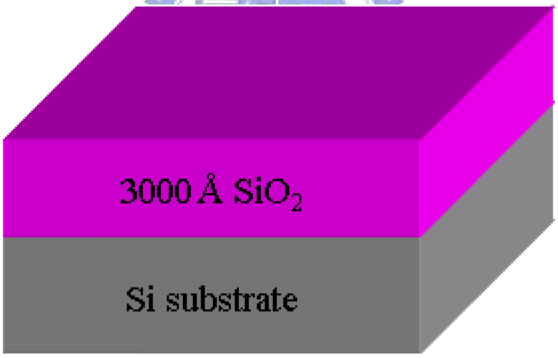

Figure 4.1 3000Å SiO_2 layer was grown on Si substrate.

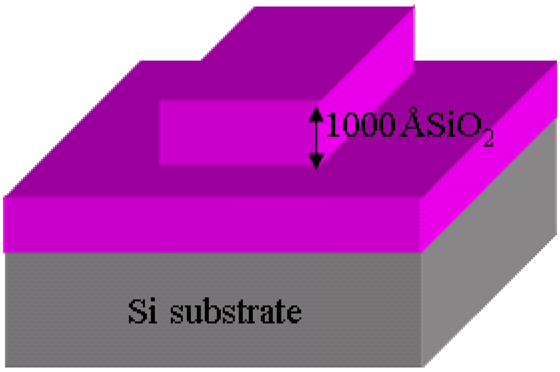

Figure 4.2 Definition of the active area. The height of oxide step is 1000Å

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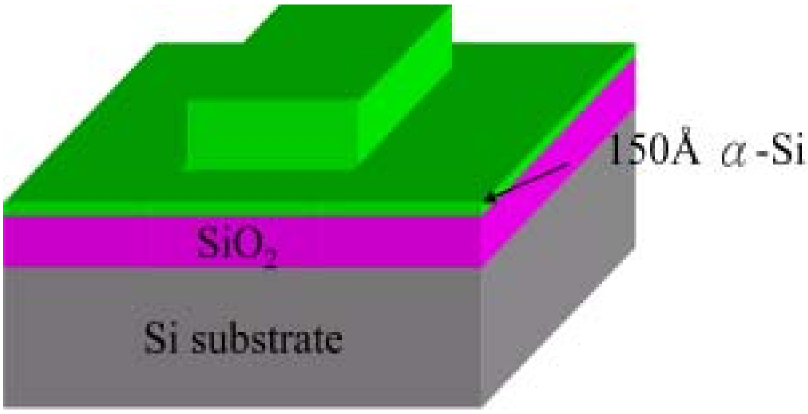

Figure 4.3 150Å Amorphous Si layer is deposited on SiO_2 layer.

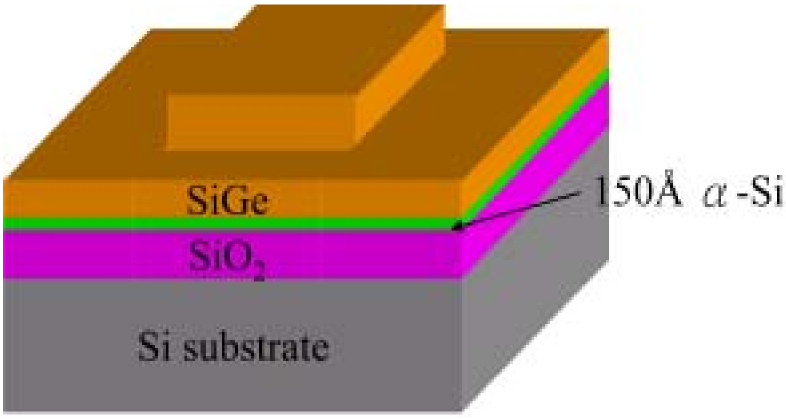

Figure 4.4 SiGe films with different Ge concentration were deposited on α-Si layer.

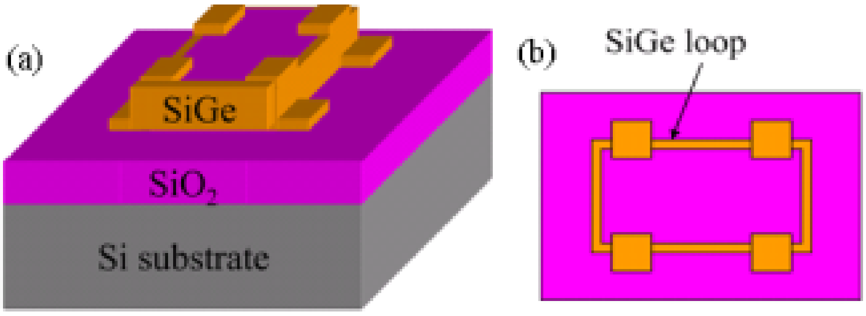

Figure 4.5 The definition of the S/D region and nanowire. (a) The 3-D view (b) The top view

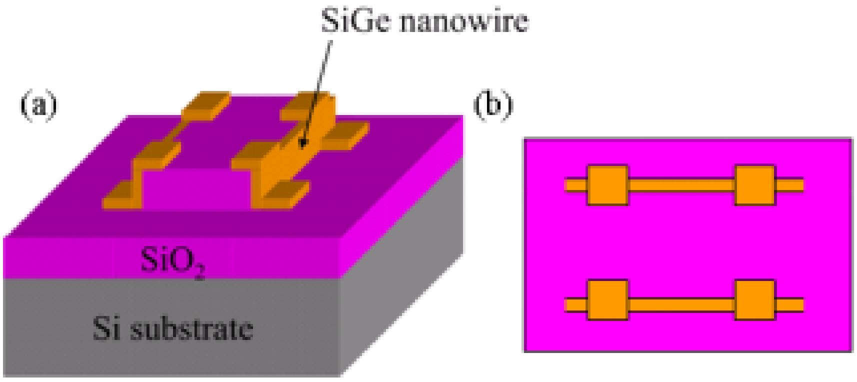

Figure 4.6 Remove one side of the parallel SiGe spacer to cut off the leakage current (a) The 3-D view (b) The top view.

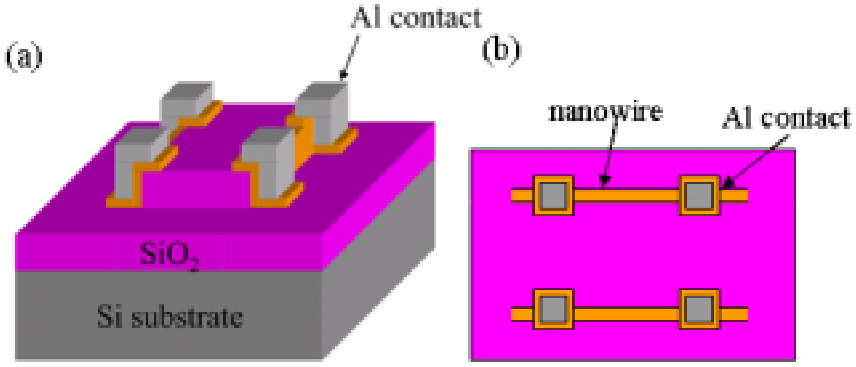

Figure 4.7 Defined Al contact pad. (a) The 3-D view (b) The top view.

4.3 Results and Discussions

The dimensions of SiGe nanowire was observed by Scanning Electron Microscope (SEM) after SiGe dry etching. Figure 4.8 (a) shows the cross-section view SEM picture of $Si_{0.93}Ge_{0.07}$ nanowire, which shows the dimension of 192 nm in height and 77.7 nm in width, (b) shows the SEM image of SiGe nanowire with 168 nm in height and 55.9 nm in width after 2 min. 900 ℃ oxidation and (c) shows that with 160 nm in height and 42.8 nm in width after 2 min. 950 ℃ oxidation.

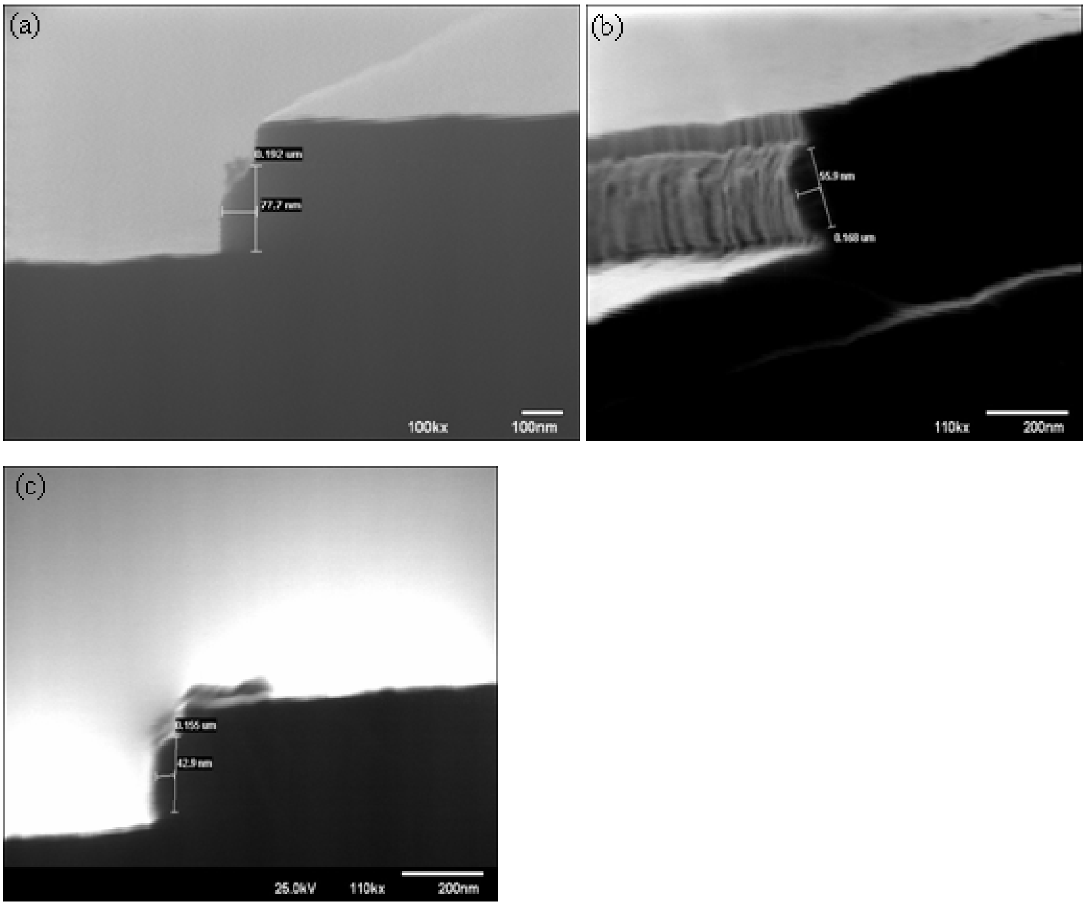

Figure 4.8 (a) The cross-section view of $Si_{0.93}Ge_{0.07}$ nanowire with 192 nm in height and 77.7 nm in width. (b) the SEM image of SiGe nanowire with 168 nm in height and 55.9 nm in width after 2 min. 900 ℃ oxidation and (c) shows that with 160 nm in height and 42.8 nm in width after 2 min. 950 ℃ oxidation.

The electrical properties of SiGe nanowires were measured by an Agilent 4156C semiconductor parametric analyzer. Figure 4.9 (a) shows the current without gate voltage applied. The lower current was found after higher temperature oxidation. In order to compare conductivity of the un-oxide and oxide nanowires, we normalized the current by multiply length and divide the area. The higher conductivity was obtained for Ge condensation technique. The conductivity is 23500 (S/m) after 950℃, 2 min. oxidation which is higher than un-oxide (15900).

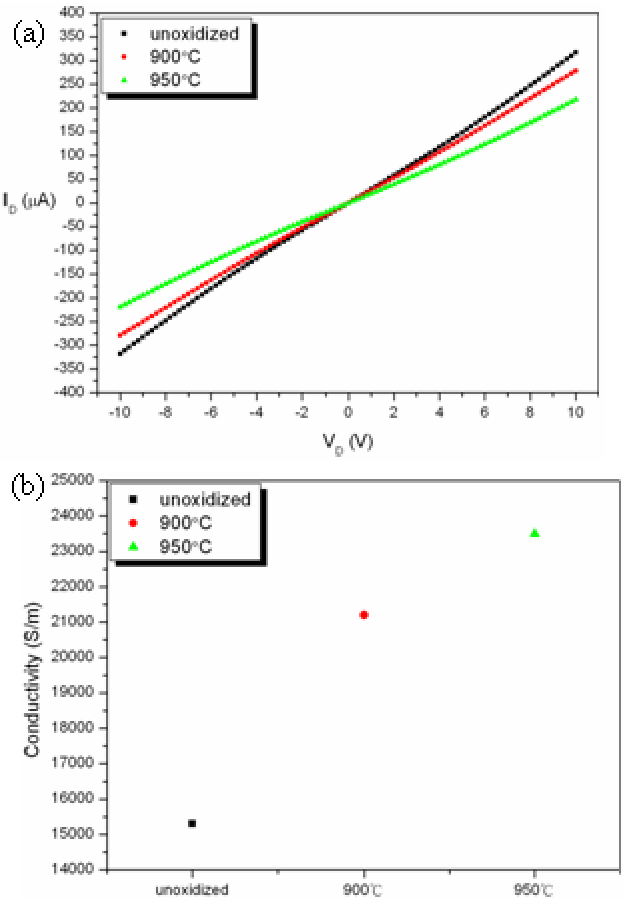

Figure 4.9 (a) I_D-V_D curve of $Si_{0.93}Ge_{0.07}$ nanowire with unoxidized, 900 °C 2 min. and 950 °C 2 min. respectively. (b) The conductivity of $Si_{0.93}Ge_{0.07}$ nanowire with unoxidized, 900 °C 2 min. and 950 °C 2 min. respectively.

4.4 Summary

The side-wall spacer N-type SiGe nanowires after oxidation were fabricated to compare the sensitivity between the nanowires. The SEM image was used to know the dimension of nanowire with/without oxidation. The lower current appeared after oxidation. However, the higher conductivity obtained after oxidation.

Chapter 5

The Ge enhances the Sensitivity for Bio-Sensor

5.1 Introduction

Since the development of nano-technology, more and more people combine the one-dimension nano-structure with bio-molecular. Due to the large surface-to-volume ratio and quasi-1D characteristics, the Silicon nanowire (NW) sensor provides a high sensitivity in chemical detection such as pH buffer solution, protein, ions, and DNA etc[5-7]. Silicon nanowires (SiNWs) are particularly appealing for sensing applications since the silicon dioxide can effectively passivate surface dangling bonds, and at the same time can be chemically modified through the well known silanol chemistry to provide surface functionalization and, therefore, selectivity for particular analytes. Beside the Si NW nan-sensor, other materials were used to detect different materials. Gas sensors have been fabricated by using the SnO_2, In_2O_3, WO_3 and ZnO nanowires [10-14]. The responses of the sensors have been characterized for gaseous polluting species like CO and NO_2. Conducting polymers have attractive features such as mechanical flexibility, easy processing, and modifiable electrical conductivity. Polyaniline/poly-(ethylene oxide) (PANI/PEO) nanowire sensors can detect NH_3 gas at concentrations as low as 0.5 ppm with rapid response and recovery time[5-16]. Pd nanowires have been studied to detect hydrogen gas due to safety reasons[17]. The sensor was based on the resistance change of Pd nanowires upon hydrogen incorporation. The high surface-to-volume ratio of nanowires results in a strong dependence of carrier concentration on charge transfer from the surface and changes in nanowire conductance. For the study of SiGe field effect transistor[19], we could found that the higher current change as the same gate voltage applied shown in Figure 5.1. However, the mechanism for the Si nanowire sensor is detecting the surface charge as the molecular stays on it. Therefore, if we used the SiGe nanowire instead of Si nanowire, we would get higher current change at the same bio-molecular bound on the surface. In this paper, we used the sidewall spacer technique[23] to fabricate the SiGe nanowire (NW) with high carrier mobility instead of Si nanowire to investigate the sensitivity.

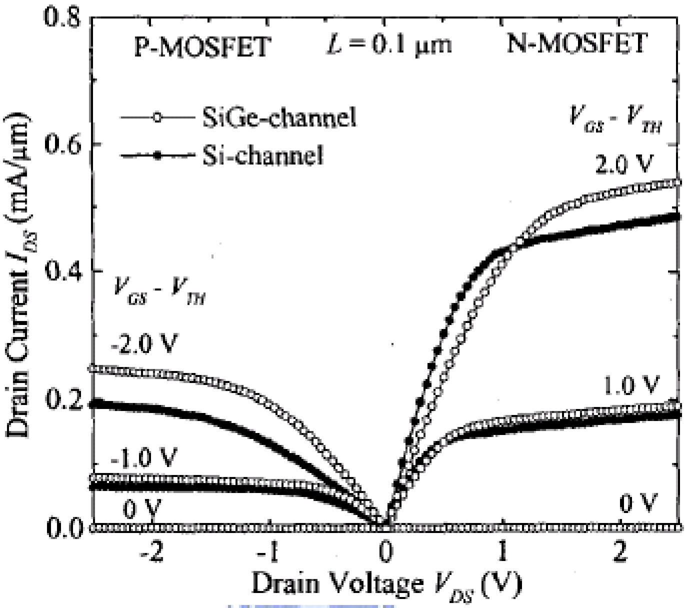

Figure 5.1 Drain current of N- and P-MOSFETs are improved with Si/SiGe-channel. (Ref. 19)

5.2 Experiment

The side-wall spacer formation is an easy process for nanowire fabrication with the advantages of high-yield and low-cost. The method only using the combination of the conventional lithography and processes technology was demonstrated without complex processes such as EBL, SPL and VLS etc. In the beginning, a p-type (100)-oriented bare silicon wafer with 1-10Ω-cm resistivity was prepared.

18. After standard RCA cleaning, 980°C Wet Oxidation was performed for 1 hours to grow the bottom oxide as an insulator oxide by ASM/LB45 Furnace system. The

thickness of the oxide is 5500Å which was shown in Figure 5.2.

19. Mask #1: Define the active area. We etched the oxide 3000 Å by dry oxide etcher (TEL 5000) after Mask I defined. Then, a 2500 Å oxide step was formed shown in Figure 5.3.
20. Following standard RCA clean, we deposited 150Å amorphous Si film on bottom oxide in the condition of 650℃ and 160 mTorr. The process increased adhesion between SiGe film and SiO2 layer shown in Figure 5.4.
21. Then, 6000 Å SiGe films with different Ge concentrations were deposited with the ultra-high-vacuum chemical vapor deposition (ANELAVA SiGe UHV-CVD) at 650℃. The structure is shown in Figure 5.5.
22. We defined the S/D contact regions with Mask II, and etched the whole height of the SiGe film (20% over etched) and the poly-Si film (20% over etched) by TCP poly etcher in the follows. Only the S/D and SiGe/poly-Si deposited in the sidewall spacer were stayed. The residual SiGe film is what we want – SiGe nanowire. The structure is shown in Figure 5.6.
23. Next, we etched each pair of the parallel SiGe NW by TCP poly etcher after Mask III was defined. Thus, the poly-Si/SiGe nanowires were isolated. The structure is shown in Figure 5.7.
24. Finally, the aluminum was then deposited with a thickness of 5000 Å by thermal coater. Mask IV was used to reserve the S/D region shown in Figure 5.8.
25. Al sintering at 430℃ in N_2 ambient for 25 minutes.

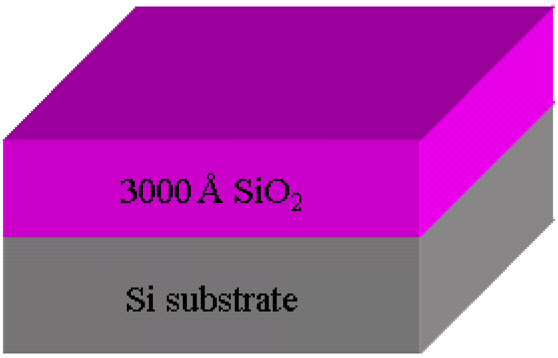

Figure 5.2 3000Å SiO_2 layer was grown on Si substrate.

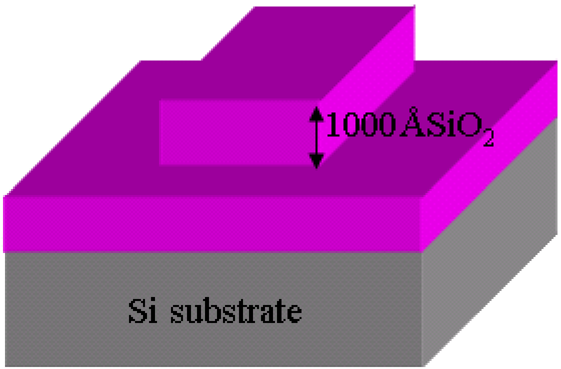

Figure 5.3 Definition of the active area. The height of oxide step is 1000Å

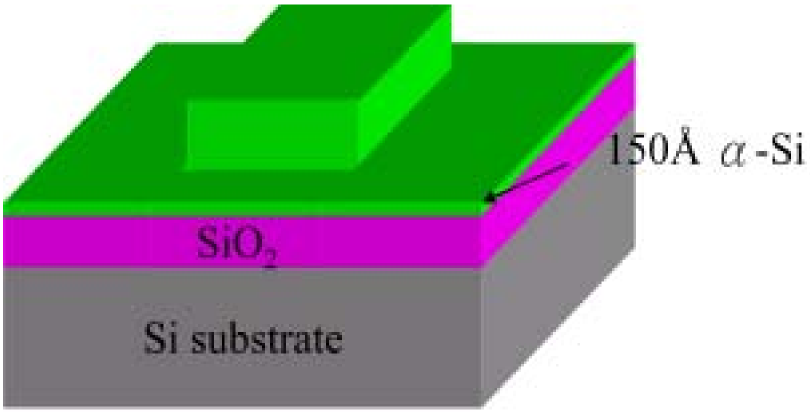

Figure 5.4 150Å Amorphous Si layer is deposited on SiO_2 layer.

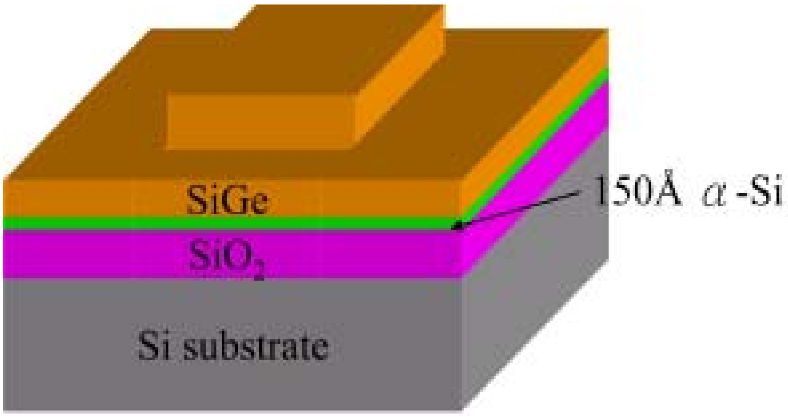

Figure 5.5 SiGe films with different Ge concentration were deposited on α-Si layer.

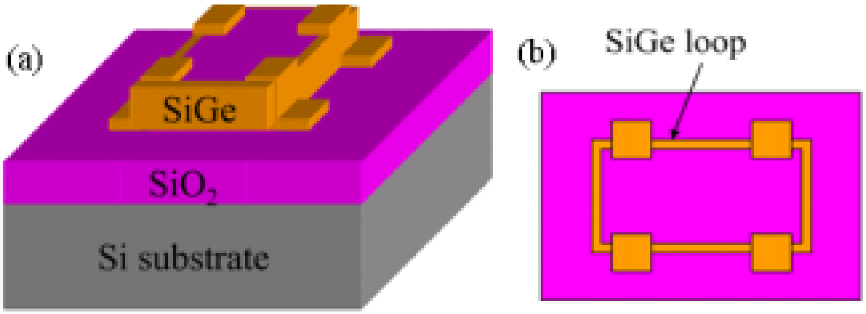

Figure 5.6 The definition of the S/D region and nanowire. (a) The 3-D view (b) The top view

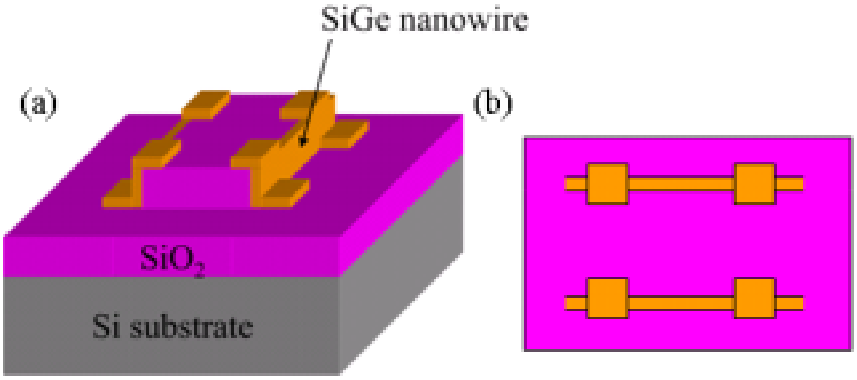

Figure 5.7 Remove one side of the parallel SiGe spacer to cut off the leakage current (a) The 3-D view (b) The top view.

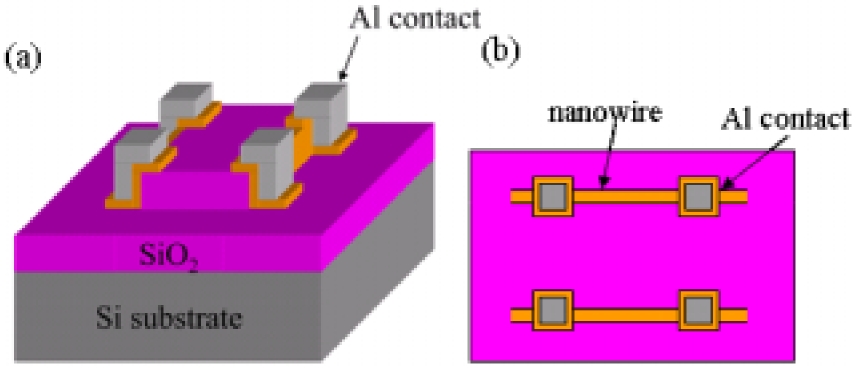

Figure 5.8 Defined Al contact pad. (a) The 3-D view (b) The top view.

5.3 The Dimension of Nanowires

The dimension of SiGe nanowire was controlled by the deposition for the width and the step of oxide for the height. In order to etch the SiGe film clearly, we added the 20% over-etching at the step of dry etching. The dimensions of SiGe nanowires with different Ge concentrations were observed by Scanning Electron Microscope (SEM) after SiGe dry etching. Figure 5.9 (a) shows the cross-section view of SEM picture of $Si_{0.93}Ge_{0.07}$ nanowire, which shows the dimension of 192 nm in height and 77.7 nm in width. Figure 5.9 (b) shows the $Si_{0.89}Ge_{0.11}$ nanowire with 184 nm in height and 45.4 nm in width, (c) shows the $Si_{0.8}Ge_{0.2}$ nanowire with 159 nm in height and 65.9 nm in width, (d) shows the $Si_{0.7}Ge_{0.3}$ nanowire with 153 nm in height and 54.5 nm in width and (e) shows the $Si_{0.6}Ge_{0.4}$ nanowire with 172 nm in height and 53.4 nm in width respectively. Because of the hardly-controlled deposition of SiGe film and dry etching for different SiGe film, we made the different dimensions of SiGe nanowires.

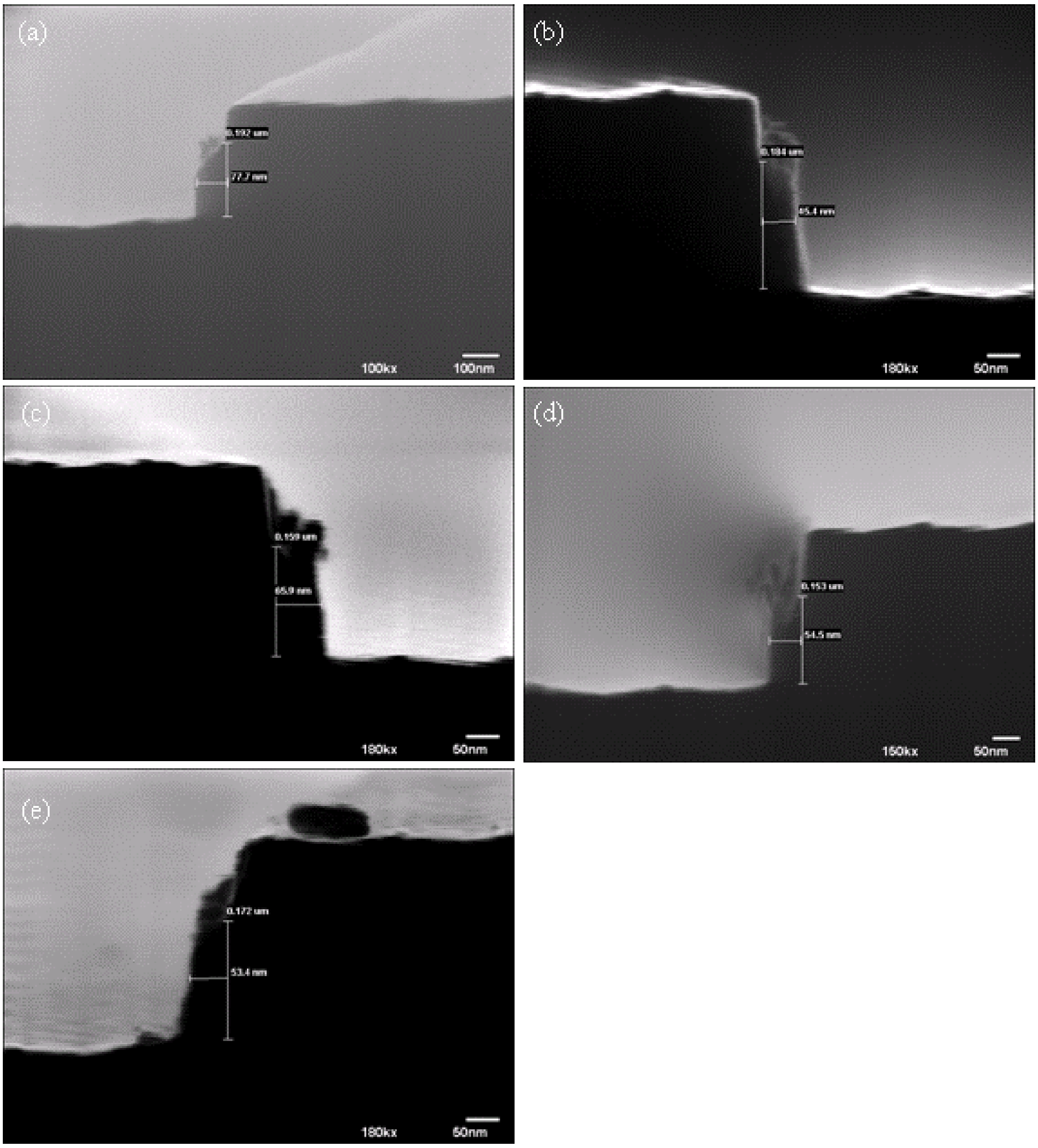

Figure 5.9 (a) The cross-section view of $Si_{0.93}Ge_{0.07}$ nanowire with 192 nm in height (H) and 77.7 nm in width (W). (b) The $Si_{0.89}Ge_{0.11}$ nanowire with H = 184 nm and W = 45.4 nm (c) The $Si_{0.8}Ge_{0.2}$ nanowire with H = 159 nm and W = 65.9 nm. (d) The $Si_{0.7}Ge_{0.3}$ nanowire with H = 153 nm and W = 54.5 nm. (e) The $Si_{0.6}Ge_{0.4}$ nanowire with H = 172nm and W = 53.4 nm.

5.4 Results and Discussions

The electrical properties of SiGe nanowires were measured by an Agilent 4156C semiconductor parametric analyzer. We swept the I_D-V_D from –10 V to 10 V, and changed the bottom gate V_G = –15, 0V and 15V respectively. The I_D-V_D curve of $Si_{0.93}Ge_{0.07}$ nanowire is shown in Figure 5.10 (a), and the diagram is shown below the curve. It is observed that the bottom gate has less influence on the drive current for too thick insulation oxide. In order to make sure that the measured-current came from the nanowire, we made a test structure below the Figure 5.10 (b). It is seen that only few pA current obtained for two isolated pads. Also, the effect of bottom gate is few pA current which could not measure in Figure 5.10 (a). Other currents of SiGe nanowires with different Ge concentrations have the same phenomenon.

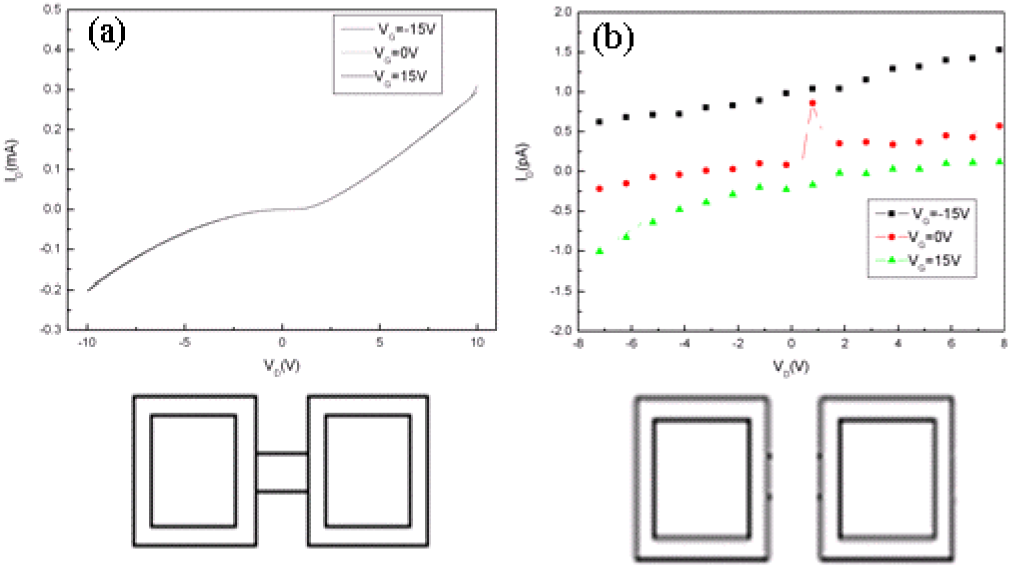

Figure 5.10 (a) The I_D-V_D curve of $Si_{0.93}Ge_{0.07}$ nanowire. (b) The cut-off current between the two contact pads.

As the discussion in the introduction, the powerful application of nanowire is used for the nano-sensor. For comparing the sensitivity between the SiGe nanowires with different Ge concentrations, we chose the 3-amino-propyl-trime-thoxy-silane (APTS) to modify the surface condition of silicon dioxide layer around the SiGe NWs. The hydroxyl molecules were replaced by the methoxy side of the APTS molecules that the surface voltage changed from negative to positive, shown in Figure 5.11 (a). This change of the surface condition resulted in accumulating state for N-type $Si_{0.93}Ge_{0.07}$ nanowires that I_D on accumulated state had higher current than un-modified, which is shown in Figure 5.11 (b). We calculate the conductance for the comparison of the change with/without APTS on the SiGe nanowire. The normal symbol shows the conductance in the beginning and the APTS symbol shows the conductance after APTS modified. It is observed that the higher conductance obtains after APTS modified, the amounts of the APTS molecules binding on the oxide surface performed like a constant voltage applied on the $Si_{0.93}Ge_{0.07}$ nanowire. For clearly proving the result, the bis-sulfo-succinimidyl suberate (BS3) was applied to link the APTS molecule shown in Figure 5.11 (a). In Figure 5.11 (b), we could observe that the conductance of BS3 became lower after BS3 linked. The reason for the BS3 molecules only link with APTS molecules that the total amounts of BS3 molecules were limited by APTS molecules. In addition, the BS3 molecule was easier to release the sodium ion or to break the single bond between the carbon atom and the oxygen atom that these two results all caused the negative gate voltage, which depleted the N-type SiGeNWs.

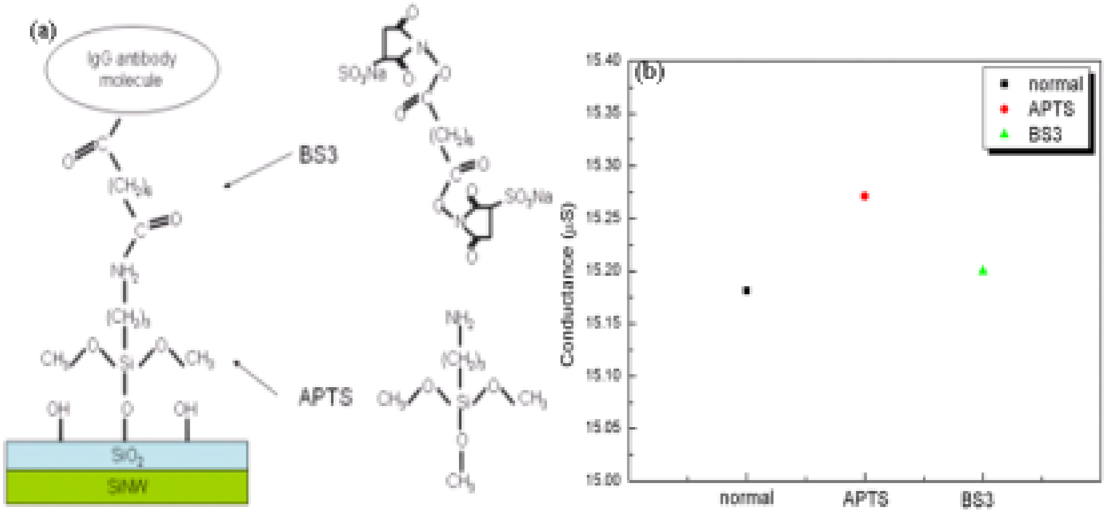

Fig. 5.11 (a) The mechanism image of the 3-amino-propyl-trime-thoxy-silane APTS and bis-sulfo-succinimidyl suberate BS3 molecular linkage on the nanowire. (b) The conductance of N-type $Si_{0.93}Ge_{0.07}$ nanowire with/without APTS and BS3 modified. The conductance increases for positive charge of APTS and decreases for the negative charge of BS3.

Figure 5.12 (a) shows the conductance of $Si_{0.89}Ge_{0.11}$ nanowire with/without ATPS and BS3 modified. We also found that the conductance increased after APTS modified (accumulation) and decreased after BS3 modified (depletion). Figure 5.12 (b), (c) and (d) show the conductance of $Si_{0.8}Ge_{0.2}$, $Si_{0.7}Ge_{0.3}$ and $Si_{0.6}Ge_{0.4}$ nanowire respectively. The similar phenomenon is also observed in other SiGe nanowires with different Ge concentrations.

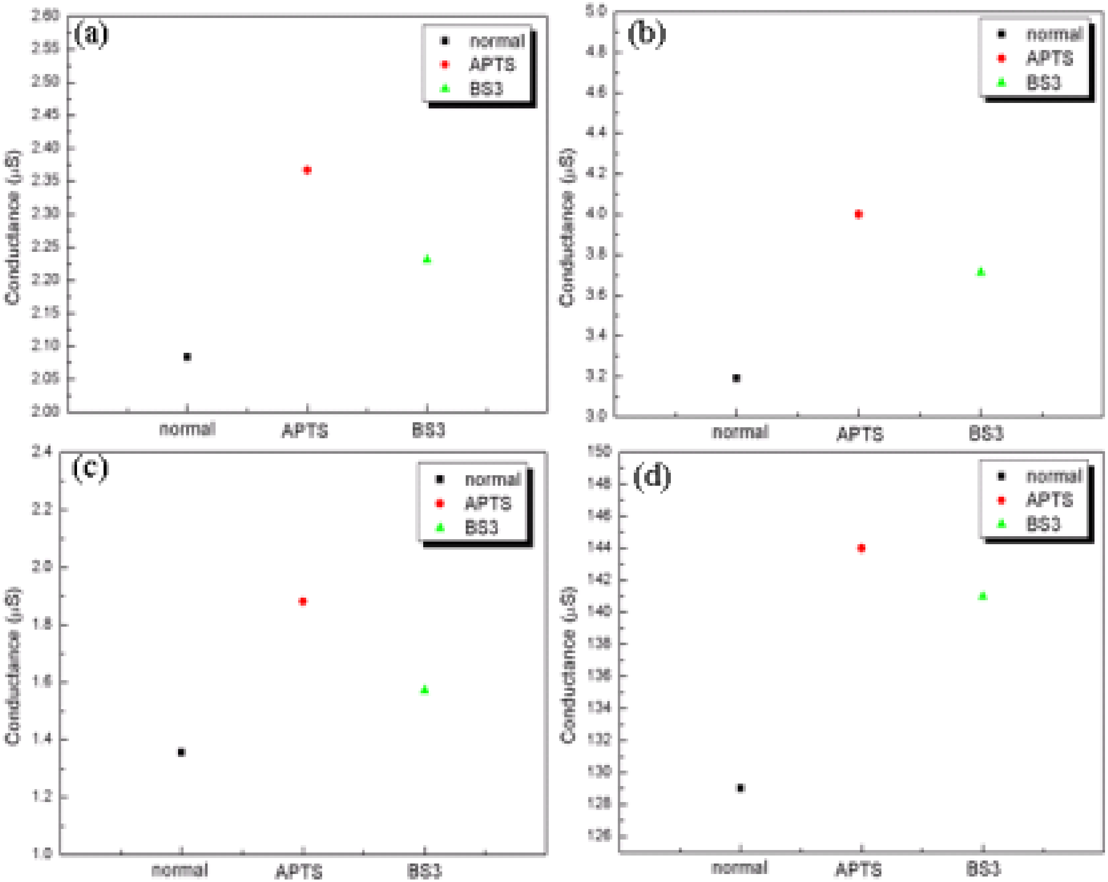

Figure 5.12 (a) The conductance of N-type $Si_{0.89}Ge_{0.11}$ nanowire with/without APTS and BS3 modified. The conductance increases for positive charge of APTS and decreases for the negative charge of BS3. (b) (c) (d) shows the conductance of N-type $Si_{0.8}Ge_{0.2}$, $Si_{0.7}Ge_{0.3}$ and $Si_{0.6}Ge_{0.4}$ SiGe nanowire respectively.

In order to compare the sensitivity for different SiGe nanowires, the value ΔS/S is considered. ΔS is the variation of conductance and S is the normal conductance of SiGe nanowire. The value shows the percentage change of conductance in the same change of surface after the APTS and BS3 modified which can be utilized to compare the sensitivity. The percentage of $Si_{0.93}Ge_{0.07}$ nanowire is 2.3%, the percentage of $Si_{0.89}Ge_{0.11}$ nanowire is 10.7%, the percentage of $Si_{0.8}Ge_{0.2}$ nanowire is 23.3%, the percentage of $Si_{0.7}Ge_{0.3}$ nanowire is 36.4% and the percentage of $Si_{0.6}Ge_{0.4}$ nanowire is 11.6% after APTS modified, which are shown in Figure 5.13 (a). It is observed that the sensitivity improves with the increment of Ge concentration from 7% to 30%. The sensitivity does not increase at the higher concentration of Ge (40%). The reason for reducing the sensitivity at 40%-Ge concentration may be higher defects appears at the interface. It may cause the bad adhesion between APTES and the surface of SiGe nanowire. Figure 5.13 (b) shows the percentage of the variation in conductance of SiGe nanowire with different Ge concentrations after BS3 connected to it. The Ge enhances the sensitivity is also observed as Ge increases form 7% to 30%. However, the sensitivity decreases for higher Ge concentration (40%).

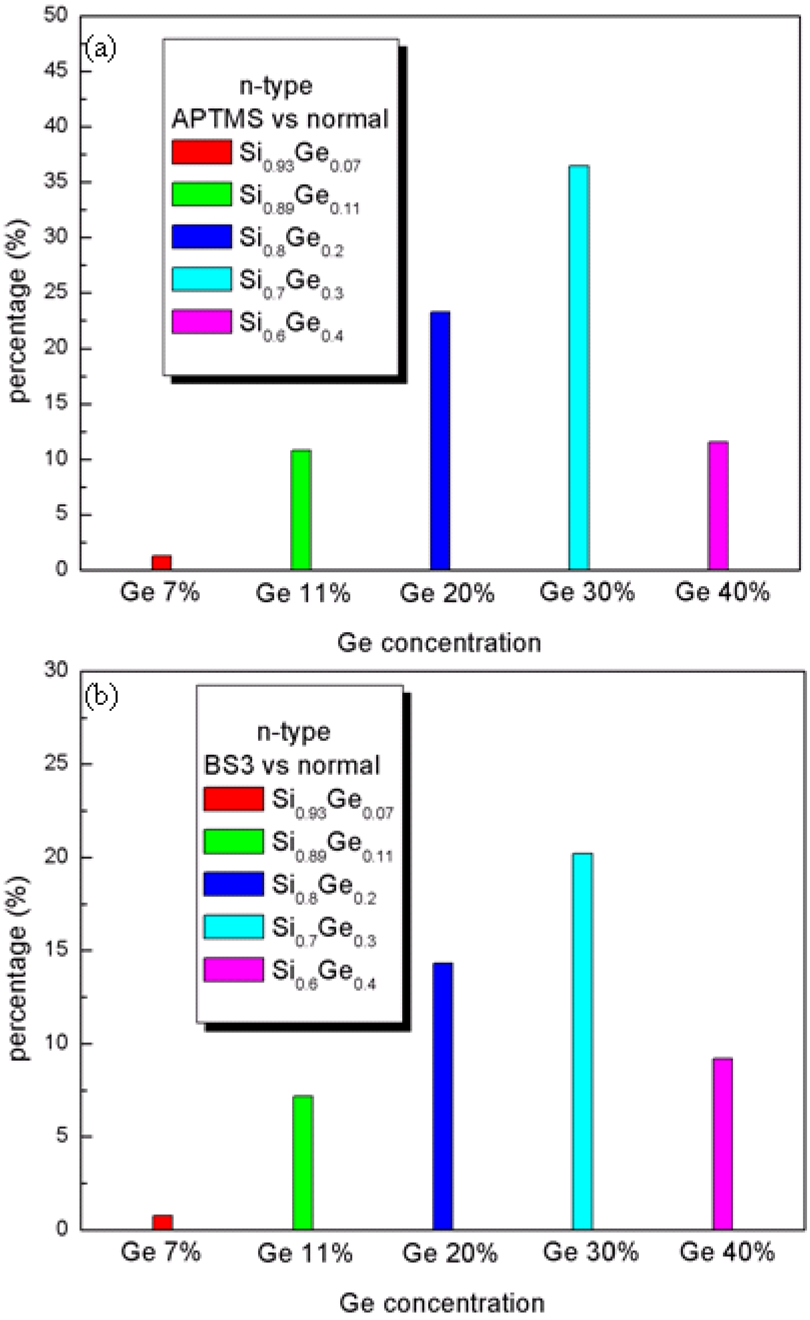

Figure 5.13 (a) The percentage of the variation in conductance of SiGe nanowire with different Ge concentrations after APTS modified. (b) The percentage of the variation in conductance of SiGe nanowire with different Ge concentrations after BS3 connected to it.

Finally, the antibody immunoglobulin IgG (protein) molecules were applied to link after the BS3 molecules, which also showed the results as prior mention and provided a positive gate voltage of the N-type $Si_{0.93}Ge_{0.07}$ nanowire shown in Figure 5.14 (a). The conductance increased after IgG molecular connects to BS3, and the same results appeared for $Si_{0.89}Ge_{0.11}$ nanowire. For expensive of IgG, we only used $Si_{0.93}Ge_{0.07}$ and $Si_{0.89}Ge_{0.11}$ nanowire to confirm that Ge enhances the sensitivity for bio-senor. Figure 5.14 (b) demonstrated that the $Si_{0.89}Ge_{0.11}$ nanowire (8%) has higher percentage change than the $Si_{0.93}Ge_{0.07}$ nanowire (3%).

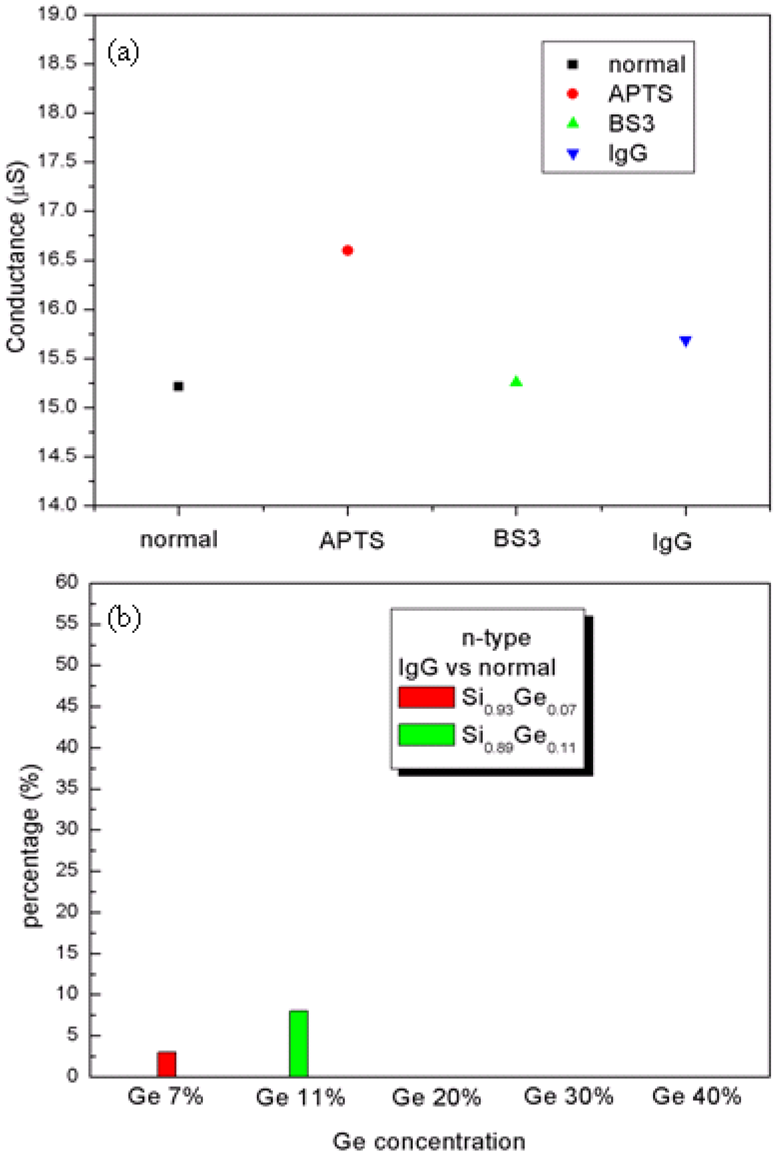

Figure 5.14 (a) The conductance of $Si_{0.93}Ge_{0.07}$ nanowire after IgG connected to it. (b) The percentage of the variation in conductance of SiGe nanowire with different Ge concentrations after IgG connected to it.

The reason of higher sensitivity of nanowire is higher surface-to-volume ratio. In order to make sure that the improvement of sensitivity came from Ge element or not, we had to calculate the surface-to-volume ratio. The $Si_{0.89}Ge_{0.11}$, $Si_{0.7}Ge_{0.3}$ and $Si_{0.6}Ge_{0.4}$ nanowires show higher ratio, but $Si_{0.93}Ge_{0.07}$ and $Si_{0.8}Ge_{0.2}$ show lower ratio. So, we can know that the enhancement of sensitivity came form the addition element “Ge”.

5.5 Summary

The side-wall spacer N-type SiGe nanowires with different Ge concentrations were fabricated to compare the sensitivity between the nanowires. The SEM image not only used to know the size but also to calculate the surface-to-volume ratio. The 3-amino-propyl-trimethoxy-silane (APTS) was used to modify the surface, which can connect the bio-linker. The conductance of SiGe nanowire increases owing to APTS with positive charge. The bis (sulfosuccinimidyl) suberate sodium (BS3) as the bio-linker connects to APTS, and the conductance decreases because of negative charge. Finally, the protein immunoglobulin G (IGG) is linked to BS3, and the conductance reduces for negative charge. In order to compare the sensitivity for different SiGe nanowires, the ΔS/S is considered. ΔS is the variation of conductance and S is the normal conductance of SiGe nanowire. It is clearly observed that the sensitivity is improved by using higher Ge concentration nanowire instead of lower Ge concentration nanowire (7%~30%). However, our experiment found that the higher Ge concentration (40%) has not increased the sensitivity. The reason maybe the higher defect appears at the surface as over-high Ge concentration.

Chapter 6

The Improvement of the Sensitivity for Bio-Sensor by SiGe nanowire Oxidation

6.1 Introduction

Since the development of nano-technology, more and more people combine the one-dimension nano-structure with bio-molecular. Due to the large surface-to-volume ratio and quasi-1D characteristics, the Silicon nanowire (NW) sensor provides a high sensitivity in chemical detection such as pH buffer solution, protein, ions, and DNA etc[5-7]. Silicon nanowires (SiNWs) are particularly appealing for sensing applications since the silicon dioxide can effectively passivate surface dangling bonds, and at the same time can be chemically modified through the well known silanol chemistry to provide surface functionalization and, therefore, selectivity for particular analytes. Beside the Si NW nan-sensor, other materials were used to detect different materials. Gas sensors have been fabricated by using the SnO_2, In_2O_3, WO_3 and ZnO nanowires [10-14]. The responses of the sensors have been characterized for gaseous polluting species like CO and NO_2. Conducting polymers have attractive features such as mechanical flexibility, easy processing, and modifiable electrical conductivity. Polyaniline/poly-(ethylene oxide) (PANI/PEO) nanowire sensors can detect NH_3 gas at concentrations as low as 0.5 ppm with rapid response and recovery time[5-16]. Pd nanowires have been studied to detect hydrogen gas due to safety reasons[17]. The sensor was based on the resistance change of Pd nanowires upon hydrogen incorporation. The high surface-to-volume ratio of nanowires results in a strong dependence of carrier concentration on charge transfer from the surface and changes in nanowire conductance. For the study of SiGe field effect transistor[19], we could found that the higher current change as the same gate voltage applied shown in Figure

5.1. However, the mechanism for the Si nanowire sensor is detecting the surface charge as the molecular stays on it. Therefore, if we used the SiGe nanowire instead of Si nanowire, we would get higher current change at the same bio-molecular bound on the surface. In this paper, we used the sidewall spacer technique[23] to fabricate the SiGe nanowire (NW) with high carrier mobility instead of Si nanowire to investigate the sensitivity. The oxidation behavior of SiGe films has been studied to a great extent[38-44]. Ge is completely rejected from the oxide and piles up at the oxide/substrate interface after oxidation process. Thus, we could obtain a SiGe nanowire with higher Ge concentration by oxidation and the sensitivity would increase after oxidation.

6.2 Experiment

The side-wall spacer formation is an easy process for nanowire-fabrication with the advantages of high-yield and low-cost. The method only using the combination of the conventional lithography and processes technology was demonstrated without complex processes such as EBL, SPL and VLS etc. We have successfully fabricated the SiGe nanowires by this method. In the beginning, a p-type (100)-oriented bare silicon wafer with 1-10Ω-cm resistivity was prepared. After standard RCA cleaning, 980 ℃ Wet Oxidation was performed for 6 hours to grow the bottom oxide as a insulator oxide by ASM/LB45 furnace system. The thickness of the oxide is 5500Å. We etched the oxide 3000 Å by the dry oxide etcher after Mask I defined. Then, a 2500 Å oxide step was formed. Following standard RCA cleaning, we deposited 150Å amorphous Si film on bottom oxide in the condition of 650 ℃ and 160 mTorr. The process increases adhesion between SiGe film and SiO_2 layer. Then, 600 Å $Si_{0.93}Ge_{0.07}$ film was deposited with the ultra-high-vacuum chemical vapor deposition (ANELAVA SiGe UHV-CVD) at 650℃. The structure is shown in Figure 6.1 (a).

Second, we defined the S/D contact regions with Mask II, and etched the whole height of the SiGe film (800Å, 20% over etched) by TCP poly etcher in the follows. Only the S/D and SiGe deposited in the sidewall spacer were stayed. And the residual SiGe film is what we want – SiGe nanowire. The structure is shown in Figure 6.1 (b). Third, we etched each pair of the parallel SiGe nanowire by TCP poly etcher after Mask III was defined. Thus, the SiGe NWs were isolated. The structure is shown in Figure 6.1 (c). Finally, Boron was doped heavily with $5x10^{15}$ cm^{-2} at 10 keV. Activation annealing at 950℃ in N_2 flow was then employed for 30 minutes after ion implantation. The aluminum was then deposited with a thickness of 5000 Å by thermal coater. Mask IV was used to reserve the S/D regions, and then 400℃ sintering 30 min was done.

The dimension of SiGe nanowire was controlled by the deposition for the width and the step of oxide for the height. In order to etch the SiGe film clearly, we added the 20% over-etching at the step of dry etching. The dimensions of SiGe nanowire was observed by Scanning Electron Microscope (SEM) after SiGe dry etching. Figure 6.1 (d) shows the cross-section view SEM picture of $Si_{0.93}Ge_{0.07}$ nanowire, which shows the dimension of 192 nm in height and 77.7 nm in width.

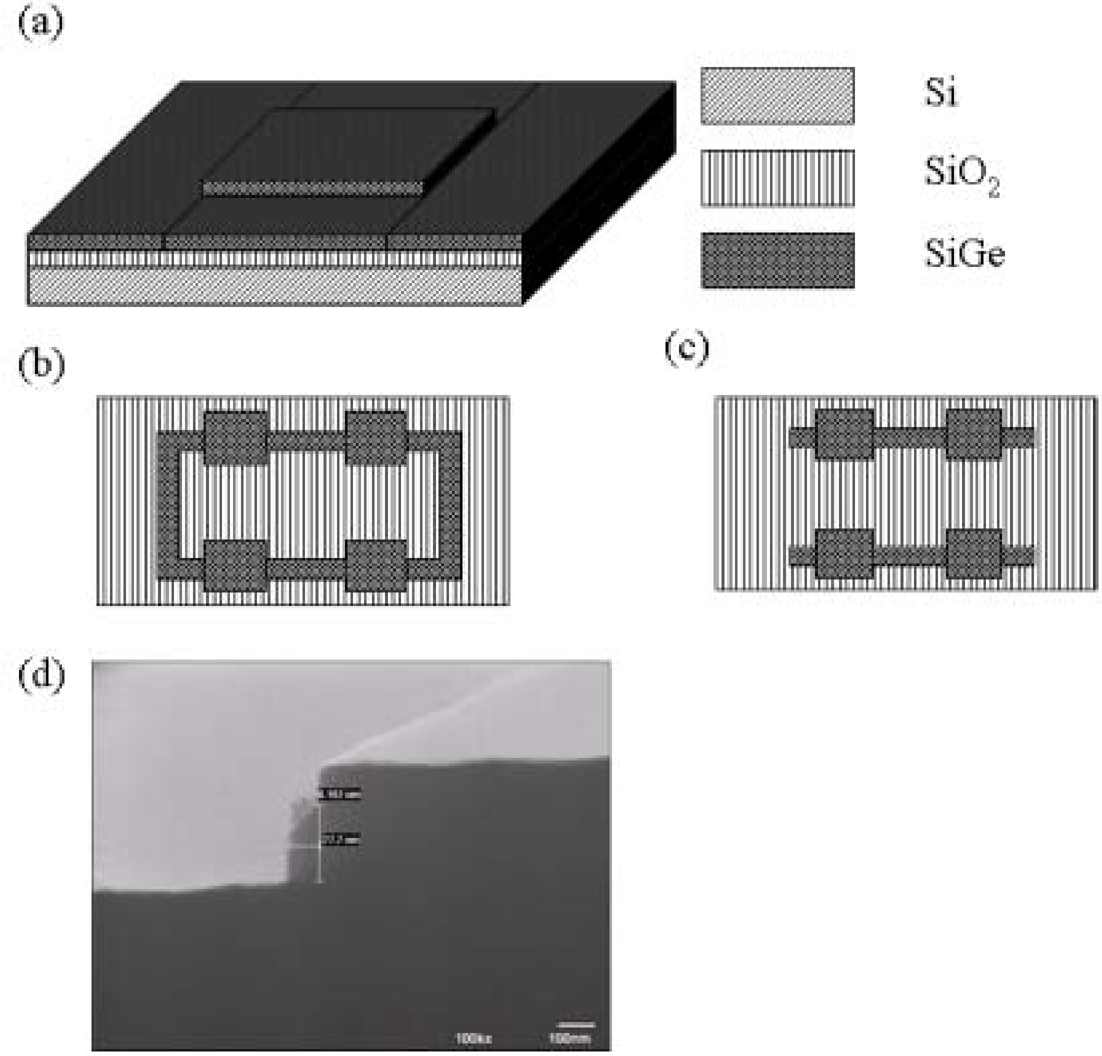

Figure 6.1 (a) SiGe/SiO$_2$/Si stack. For the step of oxide, the height of different SiGe is formed on the plane film and spacer place. (b) The Spacer SiGe nanowire and the huge block (for the contact) were remained after Dry etching. (c) The SiGe nanowires were isolated. (d) The cross-section view of Si$_{0.93}$Ge$_{0.07}$ nanowire with 192 nm in height and 77.7 nm in width.

6.3 Results and Discussions

The electrical properties of SiGe nanowires were measured by an Agilent 4156C semiconductor parametric analyzer. We swept the I_D-V_D from –10 V to 10 V, and set the bottom gate V_G = 0 V. As the discussion in the introduction, the powerful application of nanowire is used for the nano-sensor. For comparing the sensitivity between the SiGe nanowires, we chose the 3-amino-propyl-trime-thoxy-silane (APTMS) to modify the surface condition of silicon dioxide layer around the SiGeNWs. The hydroxyl molecules were replaced by the methoxy side of the APTMS molecules that the surface voltage changed from negative to positive, shown in Figure 6.2 (a). This change of the surface condition resulted in accumulating state for N-type $Si_{0.93}Ge_{0.07}$ nanowires that I_D on accumulated state had higher current than un-modified, which is shown in Figure 6.2 (b). We calculate the conductance (S) for the comparison of the change with/without APTMS on the SiGe nanowire. The normal symbol shows the conductance in the beginning and the APTMS symbol shows the conductance after APTMS modified. It is observed that higher conductance obtains after APTMS modified, the amounts of the APTMS molecules bound on the oxide surface performed like a constant voltage applied on the $Si_{0.93}Ge_{0.07}$ nanowire. For clearly proving the result, the bis-sulfo-succinimidyl suberate (BS3) was applied to link the APTMS molecule shown in Figure 6.2 (a). In Figure 6.2 (b), we could observe that the conductance of BS3 became lower after BS3 linked. It may be that the BS3 molecule was easier to release the sodium ion or to break the single bond between the carbon atom and the oxygen atom that these two results all caused the negative gate voltage, which depleted the N-type SiGeNWs. Finally, the antibody immunoglobulin IgG (protein) molecules were applied to link after the BS3 molecules, which also provided a positive gate voltage of the N-type $Si_{0.93}Ge_{0.07}$ nanowire. The conductance reduced after IgG modified as shown in Figure 6.2 (a).

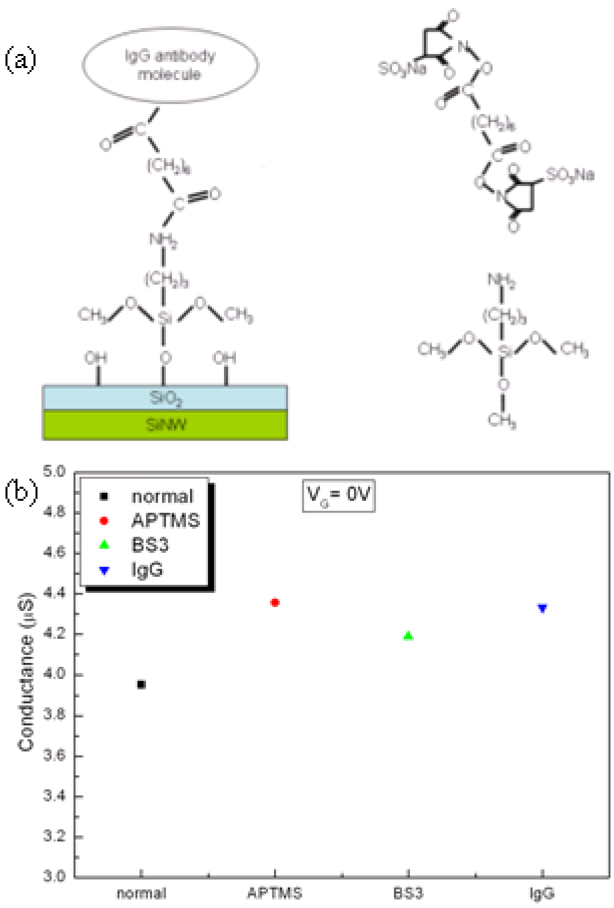

Figure 6.2 (a) The mechanism image of the 3-amino-propyl-trime-thoxy-silane APTMS, bis-sulfo-succinimidyl suberate BS3 and immunoglobulin G (IgG) molecular linkage on the nanowire. (b) The conductance of N-type $Si_{0.93}Ge_{0.07}$ nanowire after APTMS, BS3 and IgG modified.

The oxidation for the condition of 2 min. at 900 ℃ and 2 min. at 950 ℃ were employed before the ion implantation. The dimensions of SiGe nanowires after oxidation were observed by Scanning Electron Microscope (SEM). Figure 6.3 (a) shows the SEM image of SiGe nanowire with 168 nm in height and 55.9 nm in width after 2 min. 900 ℃ oxidation and Figure 6.3 (b) shows that with 160 nm in height and 42.8 nm in width after 2 min. 950 ℃ oxidation. The conductance was calculated after APTMS, BS3 and IgG modified for the oxided-nanowire and the results were shown in Figure 6.3 (c) and (d) respectively. The conductance increment for APTMS modification, decrement for BS3 modification, and increment for IgG modification are also observed. For less preparation of IgG, only the SiGe nanowire for 900 °C oxidation was experimented.

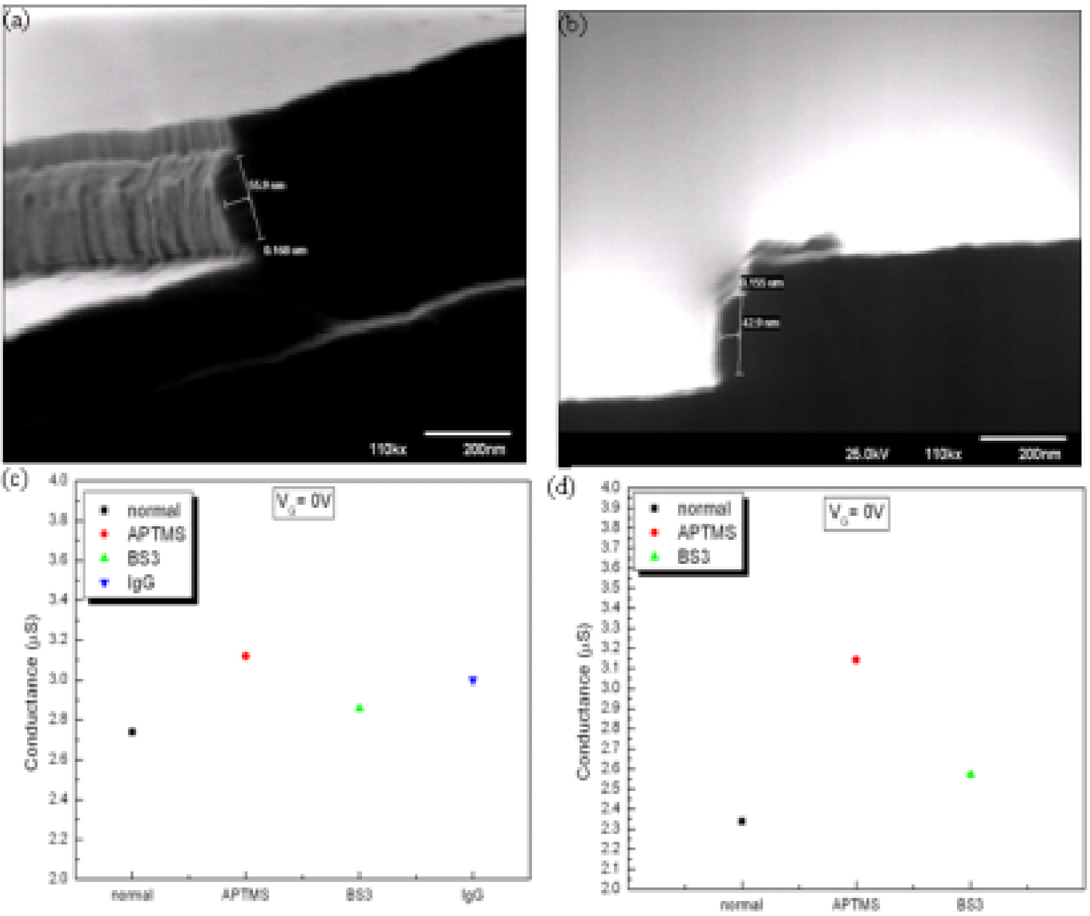

Figure 6.3 (a) The SEM image of SiGe nanowire after 2 min. 900 °C oxidation. (b) The SEM image of SiGe nanowire after 2 min. 950 °C oxidation. (c) The conductance for 900 °C-oxide nanowire after APTMS, BS3 and IgG modified. (d) The conductance for 950 °C-oxide nanowire after APTMS and BS3 modified.

In order to compare the sensitivity SiGe nanowire with/without oxidation, the value ΔS/S is considered. ΔS is the variation of conductance with/without biotin modified and S is the normal conductance of SiGe nanowire. The value shows the percentage change of conductance in the same change of surface potential after the APTMS and BS3 modified. Figure 6.4 (a) shows the percentage change of $Si_{0.93}Ge_{0.07}$ nanowire after APTMS modified. The percentage change of the conductance is 9.6% for the normal state, 13.9% for the 900 ℃ oxidation and 34.76% for 950 ℃ oxidation after APTMS modified. It shows that the oxidation improves the sensitivity of SiGe nanowire. The same result is also observed after BS3 and IgG modified which is shown in Figs. 4 (b) and (c).

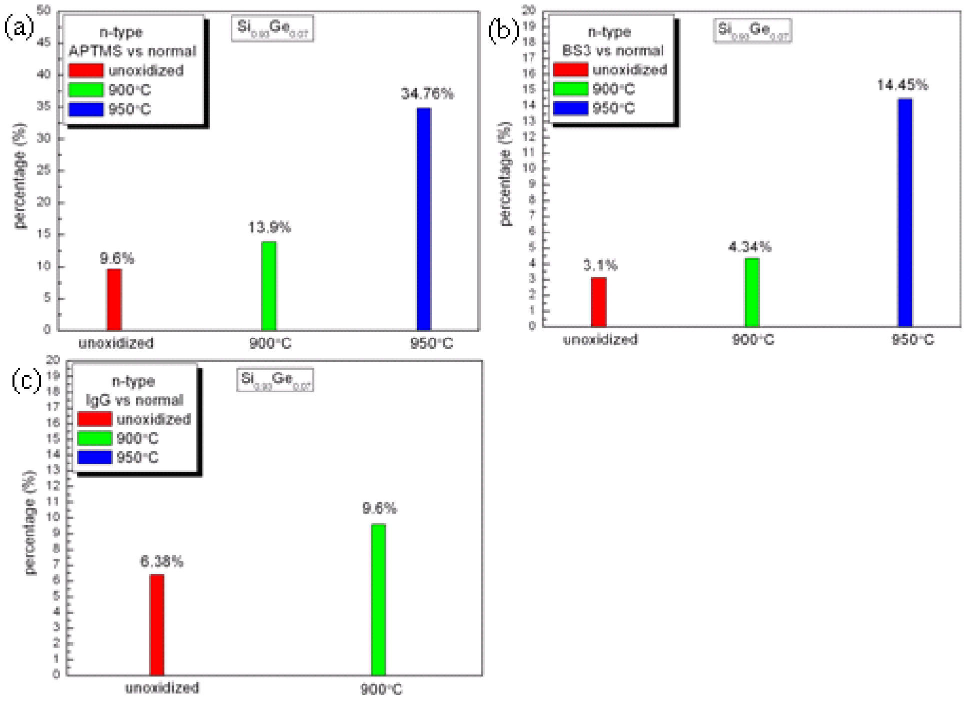

Figure 6.4 (a) The percentage of the variation in conductance of $Si_{0.93}Ge_{0.07}$ nanowire for normal, 900 ℃ and 950 ℃ oxidations after APTMS modified. (b) The percentage of the variation in conductance of $Si_{0.93}Ge_{0.07}$ nanowire for normal, 900 ℃ and 950 ℃ oxidations after BS3 modified. (c) The percentage of the variation in conductance of $Si_{0.93}Ge_{0.07}$ nanowire for normal and 900 ℃ oxidation after IgG modified.

Next, we oxidized the $Si_{0.89}Ge_{0.11}$ nanowires by the same conditions. The dimensions of $Si_{0.89}Ge_{0.11}$ nanowire was observed by Scanning Electron Microscope (SEM). Figure 6.5 (a) shows the SEM image of $Si_{0.89}Ge_{0.11}$ nanowire with 223 nm in height and 70.7 nm in width. The conductance was 3.33 in the beginning, 3.93 after APTMS modified, 3.45 after BS3 modified and 3.6 after IgG modified which is shown in Figure 6.5 (b). The conductance changed just because of the different surface potential after the biotin molecular modified. Figure 6.5 (c) shows the cross-section SEM image of $Si_{0.89}Ge_{0.11}$ nanowire after 900℃ 2 min. oxidation. The dimension of the oxidized-nanowire is 166 nm in height and 42.8 nm in width. Figure 6.5 (d) shows the conductance of 900℃- -oxidized $Si_{0.89}Ge_{0.11}$ nanowire after APTMS and BS3 modified. Figure 6.5 (e) shows the cross-section SEM image of $Si_{0.89}Ge_{0.11}$ nanowire after 900℃ 2 min. oxidation. The dimension of the oxidized-nanowire is 118 nm in height and 38 nm in width. Figure 6.5 (f) shows the conductance of 950℃ -oxidized $Si_{0.89}Ge_{0.11}$ nanowire after APTMS and BS3 modified. All the conductance changed after bio-molecular modified on the surface.

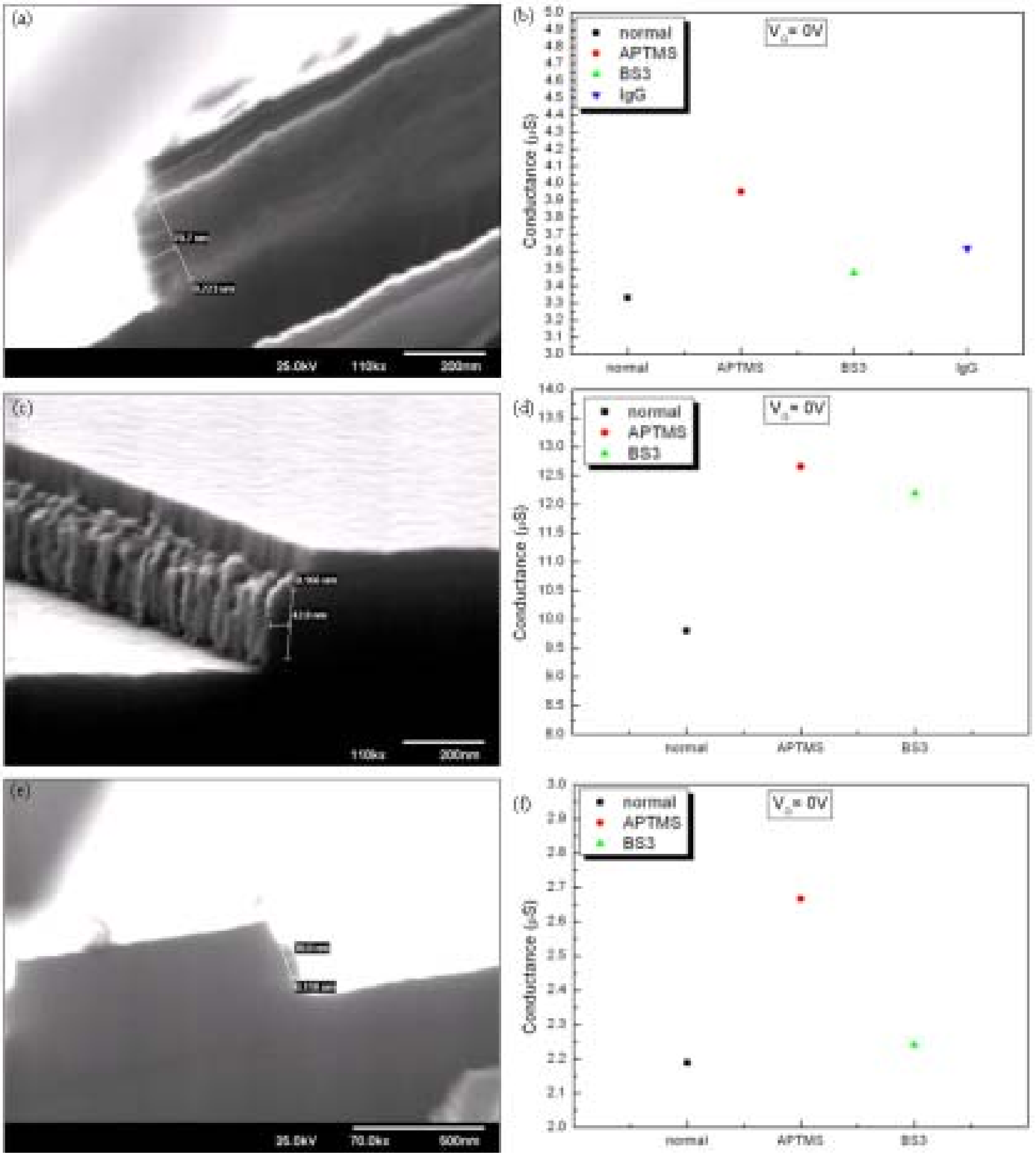

Figure 6.5 (a) The SEM image of Si$_{0.89}$Ge$_{0.11}$ nanowire (b) The conductance of Si$_{0.89}$Ge$_{0.11}$ nanowire after APTMS, BS3 and IgG modified. (c) The SEM image of Si$_{0.89}$Ge$_{0.11}$ nanowire after 2 min. 900 ℃ oxidation. (d) The conductance for 900 ℃-oxide nanowire after APTMS, BS3 and IgG modified. (e) The SEM image of Si$_{0.89}$Ge$_{0.11}$ nanowire after 2 min. 950 ℃ oxidation. (f) The conductance for 950 ℃-oxide nanowire after APTMS and BS3 modified.

By the same way to compare the sensitivity SiGe nanowire with/without oxidation, the value ΔS/S is considered. ΔS is the variation of conductance with/without biotin modified and S is the normal conductance of SiGe nanowire. Figure 6.6 (a) shows the percentage change of $Si_{0.89}Ge_{0.11}$ nanowire after APTMS modified. The percentage change of the conductance is 18.6% for the normal state, 36.36% for the 900 ℃ oxidation and 22.77% for 950 ℃ oxidation after APTMS modified. It shows that the oxidation improves the sensitivity of $Si_{0.89}Ge_{0.11}$ nanowire for the lower temperature -900℃ but decreases the sensitivity for higher temperature-950℃. The same result is also observed after BS3 modified which is shown in Figure. 6.6 (b). The possible reason is that the higher defect appears after higher temperature and longer time oxidation.

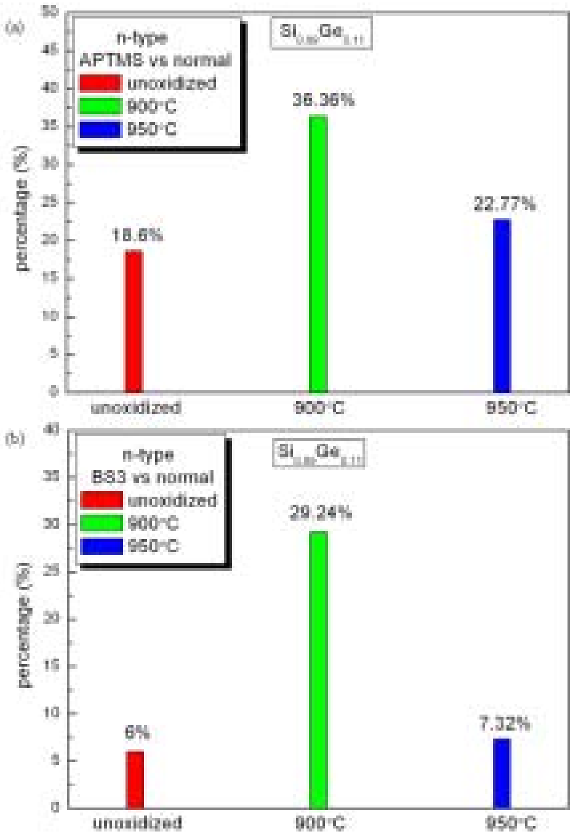

Figure 6.6 (a) The percentage of the variation in conductance of $Si_{0.89}Ge_{0.11}$ nanowire for normal, 900 ℃ and 950 ℃ oxidations after APTMS modified. (b) The percentage of the variation in conductance of $Si_{0.89}Ge_{0.11}$ nanowire for normal, 900 ℃ and 950 ℃ oxidations after BS3 modified.

In the follows, we oxidized the $Si_{0.8}Ge_{0.2}$ nanowires by the same ways. The dimensions of $Si_{0.8}Ge_{0.2}$ nanowire was observed by Scanning Electron Microscope (SEM). Figure 6.7 (a) shows the SEM image of $Si_{0.8}Ge_{0.2}$ nanowire with 159 nm in height and 65.9 nm in width. The conductance was 3.2 in the beginning, 4 after APTMS modified and 3.75 after BS3 modified which is shown in Figure 6.7 (b). The conductance changed just because of the different surface potential after the biotin molecular modified. Figure 6.7 (c) shows the cross-section SEM image of $Si_{0.8}Ge_{0.2}$ nanowire after 900°C 2 min. oxidation. The dimension of the oxidized-nanowire is 137 nm in height and 47.1 nm in width. Figure 6.7 (d) shows the conductance of 900 °C- -oxidized $Si_{0.8}Ge_{0.2}$ nanowire after APTMS and BS3 modified. The conductance of $Si_{0.8}Ge_{0.2}$ 950 °C-oxidized-nanowire was not measured. The reason will be discussed later.

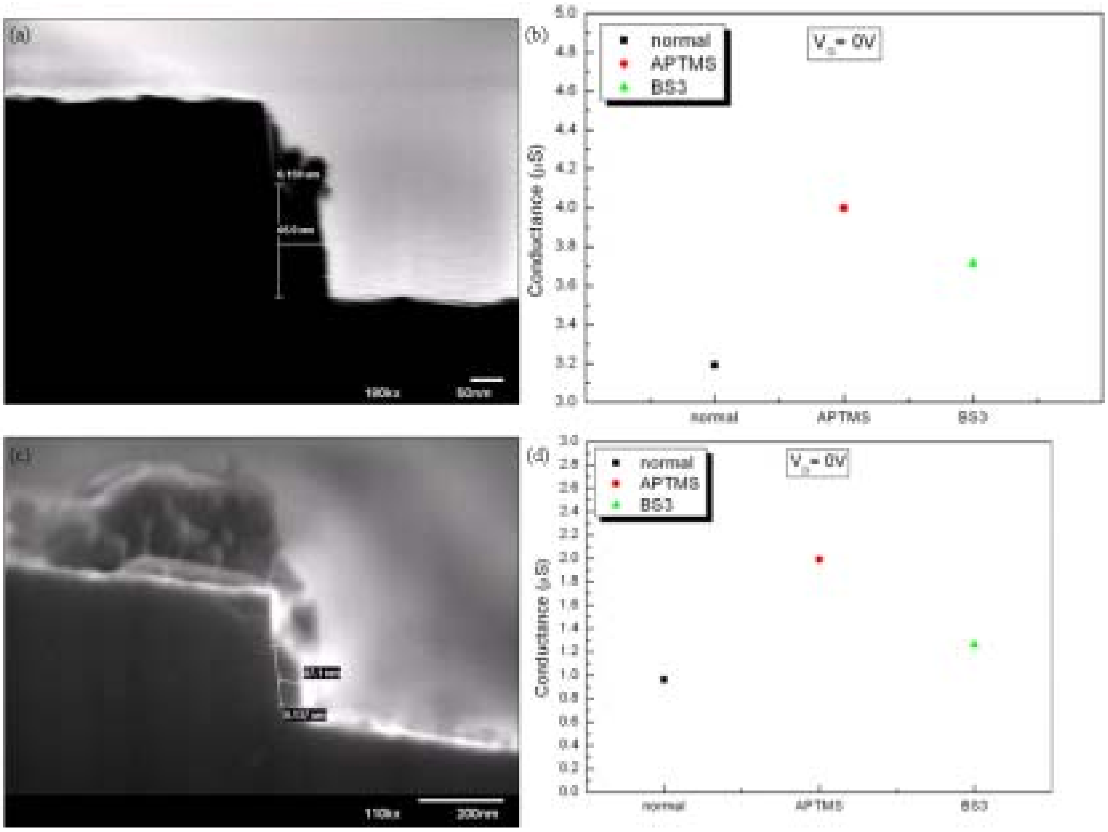

Figure 6.7 (a) The SEM image of $Si_{0.8}Ge_{0.2}$ nanowire (b) The conductance of $Si_{0.8}Ge_{0.2}$ nanowire after APTMS, BS3 and IgG modified. (c) The SEM image of $Si_{0.8}Ge_{0.2}$ nanowire after 2 min. 900 °C oxidation. (d) The conductance for 900 °C-oxide nanowire after APTMS, BS3 and IgG modified.

The value ΔS/S is still used to realize the sensitivity with/without oxidation. Figure 6.8 (a) shows the percentage change of $Si_{0.8}Ge_{0.2}$ nanowire after APTMS modified. The percentage change of the conductance is 23.67% for the normal state amd 102.9% for the 900 ℃ oxidation after APTMS modified. It shows that the oxidation improves the sensitivity of $Si_{0.8}Ge_{0.2}$ nanowire for the lower temperature -900℃. The same result is also observed after BS3 modified which is shown in Figure. 6.8 (b).

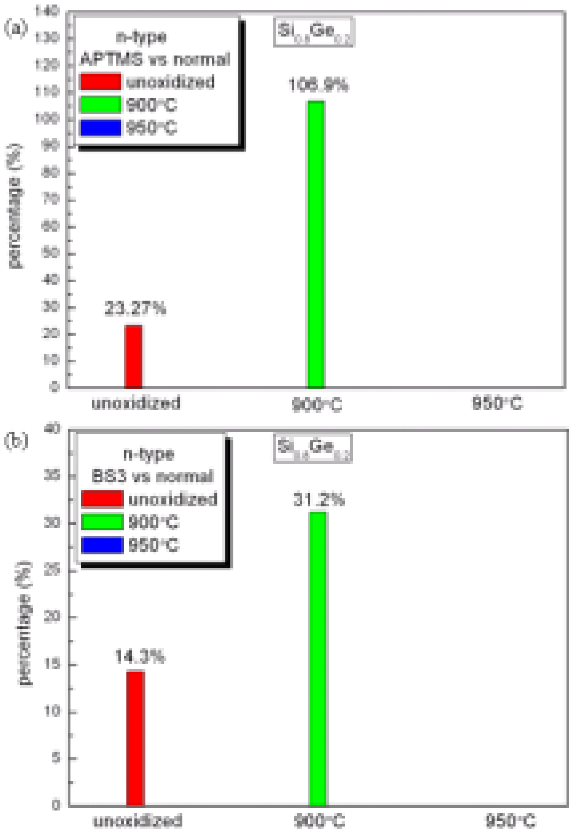

Figure 6.8 (a) The percentage of the variation in conductance of $Si_{0.8}Ge_{0.2}$ nanowire for normal, 900 ℃ and 950 ℃ oxidations after APTMS modified. (b) The percentage of the variation in conductance of $Si_{0.8}Ge_{0.2}$ nanowire for normal, 900 ℃ and 950 ℃ oxidations after BS3 modified.

The conductance of $Si_{0.7}Ge_{0.3}$ and $Si_{0.6}Ge_{0.4}$ nanowires was not measured after 900 ℃ and 950 ℃ oxidation. We used the SEM image to find the reason. Figure 6.9 (a) shows the SEM image of $Si_{0.6}Ge_{0.4}$ nanowire before oxidation and Figure 6.9 (b) shows the SEM image after 900 ℃-2 min oxidation. The $Si_{0.6}Ge_{0.4}$ nanowire was fully oxidized. The Ge enhances the oxidation rate has been studied. We thought that the higher Ge concentration induced the higher oxidation rate.

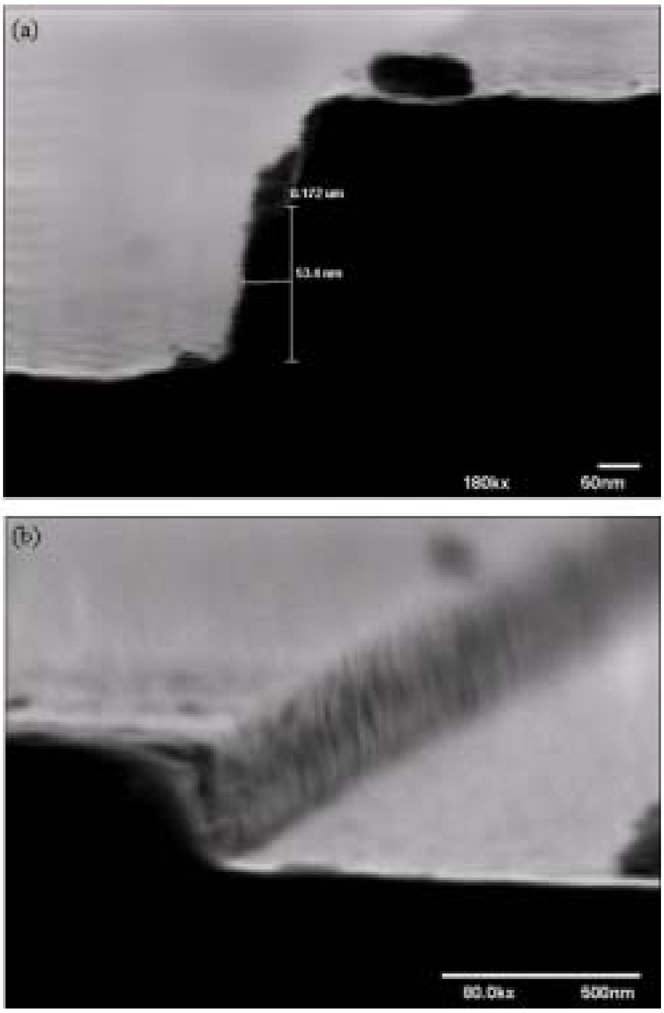

Figure 6.9 (a) The SEM image of $Si_{0.6}Ge_{0.4}$ nanowire (b) The SEM image of $Si_{0.6}Ge_{0.4}$ nanowire after 900 ℃ 2 min. oxidation.

6.4 Summary

The side-wall spacer N-type SiGe nanowires after oxidation were fabricated to compare the sensitivity between the nanowires. The SEM image was used to know the dimension of nanowire. The 3-amino-propyl-trimethoxy-silane (APTMS) was used to modify the surface, which could connect the bio-linker. The conductance of SiGe nanowire increases owing to APTMS with positive charge. The bis (sulfosuccinimidyl) suberate sodium (BS3) as the bio-linker connected to APTMS and the conductance decreased because of negative charge. Finally, the protein immunoglobulin G (IgG) is linked to BS3, and the conductance reduces for negative charge. In order to compare the sensitivity with/without oxidation, the ΔS/S is considered. ΔS is the variation of conductance and S is the normal conductance of SiGe nanowire. The percentage change of the conductance is 9.6% for the normal state, 13.9% for the 900 ℃ oxidation and 34.76% for 950 ℃ oxidation after APTMS modified. It is clearly observed that the sensitivity is improved by oxidation. For $Si_{0.89}Ge_{0.11}$ nanowire, 900 ℃ 2min. oxidation enhanced the sensitivity. However, the 950 ℃ decreased the enhance the sensitivity for the higher defect appear in the surface. For $Si_{0.8}Ge_{0.2}$ nanowire, the 900 ℃ 2min. oxidation also enhanced the sensitivity. But the conductance was not measured after 900 ℃ oxidation. For observing the SEM image of $Si_{0.7}Ge_{0.3}$ and $Si_{0.6}Ge_{0.4}$ nanowires after oxidation, the fully-oxidized were happened for higher Ge concentration.

Chapter 7

Conclusions and Feature Works

7.1 Conclusions

The side-wall spacer Poly-Si/SiGe nanowires were successfully fabricated by the side-wall spacer technique on Si wafer. The SEM image is used to know the dimension of nanowire. In order to normalize the drive current of nanowires, we consider the nanowire as a resistor. The conductance is chosen for comparison between the nanowires. The higher drive achieved of SiGe nanowire instead of Poly-Si nanowire, and the higher current obtained for the SiGe nanowire with higher Ge concentration.

With the amount of oxidized Si increasing, the hole mobility also increases and then better electrical performance would be achieved. Experiments of oxidation temperature, oxidation time, and oxygen flow already proved this phenomenon. Oxidation rate was also considered in our experiment. The results show that the devices under slower oxidation rate have lower leakage current and better On/Off ratio.

The lower current appeared after oxidation. However, the higher conductivity obtained after oxidation.

The 3-amino-propyl-trimethoxy-silane (APTS) was used to modify the surface, which can connect the bio-linker. The conductance of SiGe nanowire increases owing to APTS with positive charge. The bis (sulfosuccinimidyl) suberate sodium (BS3) as the bio-linker connects to APTS, and the conductance decreases because of negative charge. Finally, the protein immunoglobulin G (IGG) is linked to BS3, and the conductance reduces for negative charge. In order to compare the sensitivity for different SiGe nanowires, the ΔS/S is considered. ΔS is the variation of conductance and S is the normal conductance of SiGe nanowire. It is clearly observed that the sensitivity is improved by using higher Ge concentration nanowire instead of lower Ge concentration nanowire (7%~30%). However, our experiment found that the higher Ge concentration (40%) has not increased the sensitivity. The reason maybe the higher defect appears at the surface as over-high Ge concentration.

The percentage change of the conductance is 9.6% for the normal state, 13.9% for the 900 ℃ oxidation and 34.76% for 950 ℃ oxidation after APTMS modified. It is clearly observed that the sensitivity is improved by oxidation. For $Si_{0.89}Ge_{0.11}$ nanowire, 900 ℃ 2min. oxidation enhanced the sensitivity. However, the 950 ℃ decreased the enhance the sensitivity for the higher defect appear in the surface. For $Si_{0.8}Ge_{0.2}$ nanowire, the 900 ℃ 2min. oxidation also enhanced the sensitivity. But the conductance was not measured after 900 ℃ oxidation. For observing the SEM image of $Si_{0.7}Ge_{0.3}$ and $Si_{0.6}Ge_{0.4}$ nanowires after oxidation, the fully-oxidized were happened for higher Ge concentration.

7.2 Feature Works

Not only different materials or surface modified but also structure could enhance the sensitivity. In the end of thesis, we introduce a novel structure for high sensitivity bio-sensor. The high sensitivity of nanowire came form the high ratio of surface to volume. We would like to use double layer instead of single layer to obtain the nanowire with high ratio of surface to volume. Figure 7.1 shows the diagram of the conventional structure and Figure 7.2 shows the diagram of novel structure. The sizes of the nanowires are the same. But, the new structure shows the center of wire is the material of lower conductance. According to the mechanism of detecting the bio-molecular, the same electric filed changed for the same bio-molecular modified. The novel structure could lead the current go through the surface. Thu the more current change for the same bio-molecular modified.

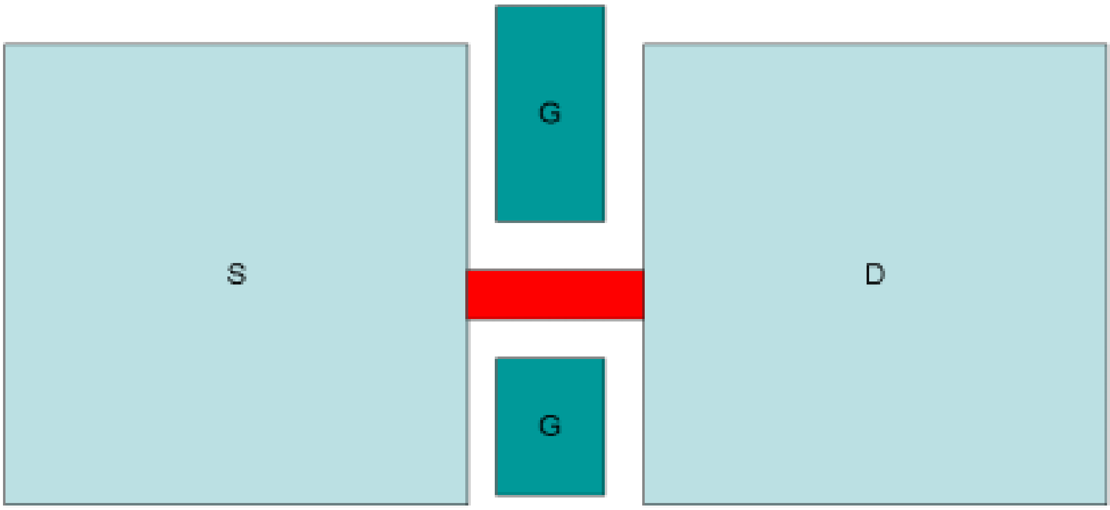

Figure 7.1 The conventional structure for bio-sensor.

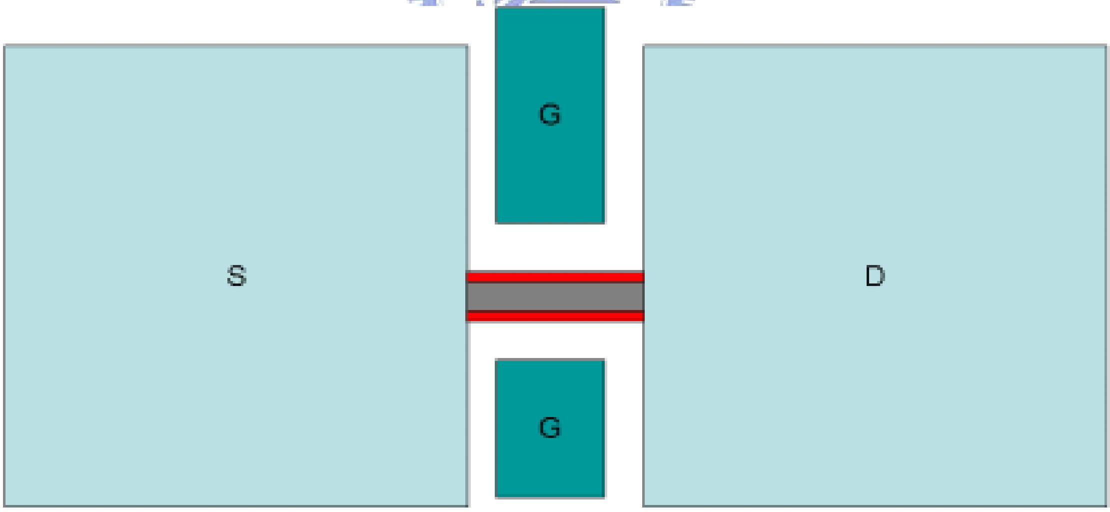

Figure 7.2 The novel structure for bio-sensor.

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[1] J.T. Sheu, **J. M. Kuo,** K.S. You, C.C. Chen and K. M. Chang, "A new fabrication technique for silicon nanowire" *Microelecronic Engineering* 73-74, pp. 594 – 598, 2004.

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