Process Design and Device Characterization for Advanced VLSI Integration

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ABSTRACT

This thesis proposes process integration and device characterization of metal-insulator-metal capacitors and asymmetric-LDD MOS transistor for SoC design. The rapid technology evolution of Si MOSFET is driven by higher device speed and cost reduction. Besides the benefit on digital performance, the scaling of CMOS technology has significantly improved the RF performance of MOS devices. The most significant improvement along with CMOS technology scaling is the higher cut-off frequency (f_t), higher maximum oscillation frequency (f_{max}), and better matching. This has made CMOS the prime choice for RF system-on-chip (SoC). The single chip transceiver design requires integration of high-performance analog components for base-band signal processing, high-performance RF transistors and passive components for low noise amplifiers and mixers, and high voltage components for power management.

In this dissertation, we discussed the process consideration of integrating the high-quality Metal-Insulator-Metal (MiM) capacitors into the Cu Backend-of-Line (Cu BEOL) of standard CMOS logic process. AlCu was widely used as the electro-plates of MiM structures before copper was introduced into the process technology for better speed

consideration. This is because AlCu is also used as the interconnection of the BEOL logic process. In the Cu era, there are different issues with the Cu electro-plates if used as a part of MiM capacitors. We compared the process and performance among different materials of MiM electro-plates and demonstrated how to integrate the MiM process into the Cu BEOL.

A difficult part to design a single-chip transceiver requires the integration of the power amplifier. However, the low drain breakdown voltage of CMOS transistors limits the use of CMOS in power amplifiers. This limitation for high voltage operation significantly reduces the maximum output power and efficiency of CMOS devices. We had designed a new asymmetric-LDD MOSFET to increase the drain breakdown voltage. The output power is improved by 38% at peak power-added efficiency. The significant improvements of RF power performance by this new MOS transistor make the CMOS SoC design a step further.

In conclusion, the integration of RF-SoC design including RF performance optimization method, RF noise modeling, the process consideration of integrating the MiM capacitors into Cu BEOL, and a new asymmetric CMOS device were discussed in this dissertation.